

The **Pemaquid S19258** is a XAUI to XFI 10G LAN/WAN/OTN Framer/Mapper/Phy device for 10GbE, 10G Fibre Channel, WIS (OC-192/STM-64), and OTN-2 network applications. It is ideal for Metro-Ethernet Switch/Router and DWDM systems. The highly integrated device supports pure 10GbE LAN Metro-Ethernet networks, as well as WAN and OTN networks via its rich suite of 10GbE over WAN and OTN mapping modes. With its integrated 10G Phy XFI interface and provisional G.709 GFEC/EFEC features, it provides a seamless interface to XFP and SFP+ optical modules.

10GbE and fibre channel mapping modes support both fixed and non-fixed stuff bytes

OTN and TOH line overhead drop/insert support

Full OTN and SONET/SDH (WIS compliant) overhead monitoring

On-Chip 10GbE MAC for full 10GbE overhead status monitoring

16-bit, 66MHz microprocessor interface for control and status monitoring

Fully Compliant to IEEE802.3-2005, ITU G.709, and XFP4.0 Standards

On Chip Fractional Clock Management Unit - only one referenced clock required to generate all line rates

Supports seven (7) 10GbE mapping modes including

- Bit Transparency mode - 10GbE mapped directly into OTU-2 yielding a 11.096Gb/s or 11.049Gb/s signal
- 10GbE into OTU-2 via GFP mapping with two flow control modes to yield a 10.7Gb/s signal
- 10GbE into OTU-2, via GFP with preamble transparency that uses OTN-OH to provide full 10GbE over a 10.709Gb/s signal
- 10GbE into a WIS frame to yield a 9.954Gb/s signal
- 10GbE into WIS frame, and then into an OTU-2 to yield a 10.7Gb/s signal
- 10GbE LAN pass-thru mode to yield a 10.3Gb/s signal

Optical Line Interface

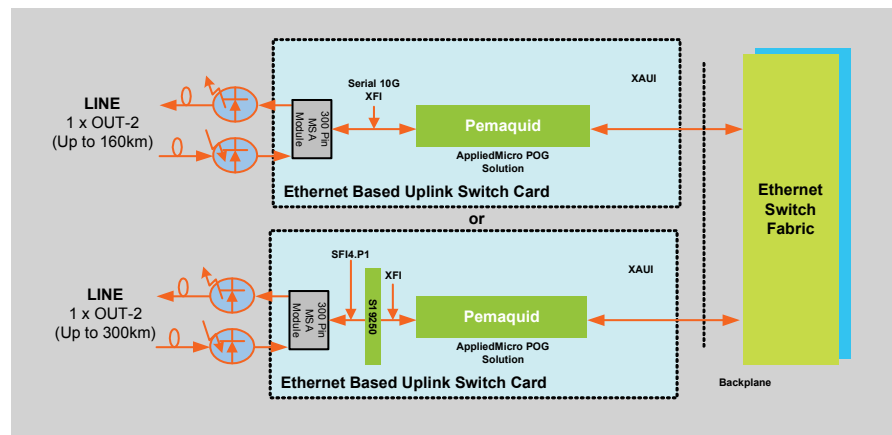
- 10G Serial Interface: 10.3Gb/s, 9.954Gb/s, 10.7Gb/s, 10.664Gb/s, 10.52Gb/s, 10.037Gb/s, 9.995Gb/s, 11.096Gb/s, 11.049Gb/s, 11.32Gb/s, 11.27Gb/s
- Glue-less interface to pluggable XFP and SFP+ modules

Backplane Interface

- 4 x XAUI (3.125Gb/s or 3.1875Gb/s) lanes for interfacing to Ethernet and Fibre Channel Switch Fabrics
- Supports ODU-2 over XAUI (4 x 3.35Gb/s) for ODU-N fabrics

Applications

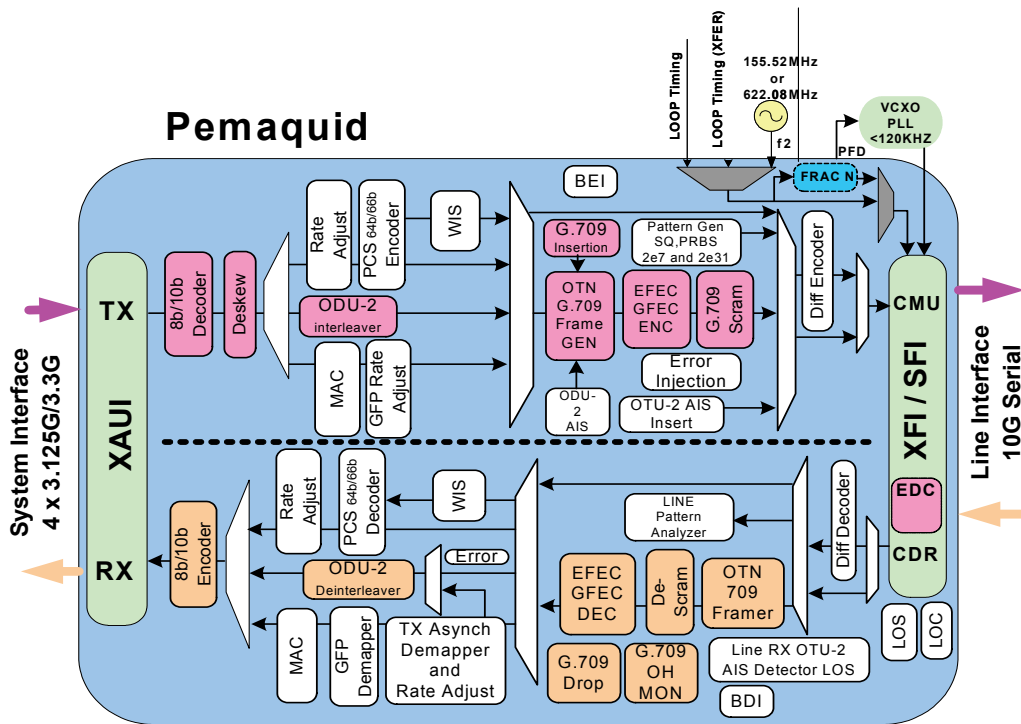
- Single Chip 10G Super-Phy for LAN, WAN and OTN platforms and networks
- Carrier grade metro-ethernet switch/router line cards
- OTU-2 DWDM client tributary and line cards
- 10GbE / OC-192 multi-service provision platform client tributary and line cards
- 10GbE IEEE802.3ae-ER/ZR uplink line card for enterprise switch applications
- Optical edge devices
- Storage networks



Pemaquid S19258 System Block Diagram



Figure 1. Pemaquid S19258 Block Diagram



Technology, Package and Power

- Technology: 0.13 Micron CMOS.
- Package: 324 pin FC-BGA (Flip Chip Ball Grid Array), 19x19 mm body, 1.0 mm ball pitch.
- Power supply Voltages: 1.2 V Core, 2.5 V CMOS I/O (3.3 V tolerant) and 1.8V for Analog I/O macros.
- Power dissipation: 2.5 - 3.69 Watts (Max) and 2.1-2.8 Watts (Typical), depending on the operation mode and interfaces used.
- S19258PBI, S19258PBIB (Leaded); S19258PSIB (Lead Free).

General Description

The AppliedMicro Pemaquid (S19258) Integrated Circuit is a Metro-Ethernet and Wide-Area Network access device aimed at Carrier Grade Ethernet Switch/Routers and Dense Wave Development Multiplexor applications.

The device provides a XAUI system/backplane interface and a 10Gb/s High Speed Serial Line Interface. Via its rich suite of mapping modes, the Pemaquid device can provisionally map 10GbE or 10G Fibre Channel into OTN and WIS Compliant signals. The mapped 10GbE or 10G Fibre Channel traffic can

be transported over OTN, WIS (SONET/SDH) networks. In addition, Pemaquid also supports OTN and WIS bypass modes to enable pure LAN Phy applications.

Pemaquid also supports an ODU-2 over XAUI mode to enable support for DWDM and MSTP platforms with ODU-N switch fabrics. In addition, when two Pemaquid_GFPs are bolted back to back, via their XAUI interfaces, OTU-2 repeater/regenerator applications can also be supported. ODU-2 signals received by the XAUI TX interface are directly fed into the Pemaquid_GFP's Line side OTN frame generator, bypassing the system side 10G MAC, GFP and WIS blocks. Provisionally, G.709 FEC or EFEC can then be appended to the ODU-2 signal to produce a jitter compliant OTU-2 serial 10Gb/s output signal. In the reverse direction, the Pemaquid_GFP can receive a 10G OTU-2 signal on the serial 10Gb/s Line RX receive input, terminate the GFEC/EFEC, perform OTU-2 frame monitoring and send the ODU-2 signal directly to the XAUI RX output interface. Again, the 10G MAC, GFP and WIS blocks are bypassed in the receive direction.

Pemaquid's High Speed 10Gb/s XFI Line Interface also supports the industry standard G.709 Forward Error Correction (GFEC) function, as well as AppliedMicro's widely industry adopted Enhanced FEC (EFEC), to enable long haul transmission by compensating for the optical noise in the optical link. Also, Pemaquid's XFI front end has built in Electronic Dispersion Compensation (EDC) that mitigates chromatic dispersion to enable longer transmission distances.

The Pemaquid also supports an ODU-2 to OTU-2 regenerator mode. In this mode, ODU-2 traffic entering via the XAUI receive interface can be G.709 framed, OTN-OH inserted, EFEC/GFEC encoded, and output over the 10G serial Line Interface as a fully compliant G.709/OTU-2 signal. In the reverse direction, the OTU-2 signal can be terminated, the OTN-OH dropped out via an external port, and the ODU-2 passed out the XAUI transmit interface.

Serial 10G Line Side Interface

- Pemaquid's 10G serial line interface supports the following LAN/WAN/OTN Frequencies/Protocols
 - 10.3Gb/s LAN
 - 10.51875 Gb/s Fibre channel
 - 9.954 Gb/s WIS (SONET/SDH)
 - 10.709Gb/s and 10.664Gb/s OTU-2
 - 10.037Gb/s and 9.995 Gb/s ODU-2
 - 11.096Gb/s and 11.049Gb/s 10GbE over OTU-2
 - 11.32Gb/s and 11.27Gb/s Fibre Channel
 - Fully integrated CMU, CDR and SERDES

The lower Line Rates modes are associated with the fixed stuff byte columns being used for user data.

XAUI System/Backplane Interface

- Pemaquid System/Backplane Interface is XAUI compliant.
- It supports 4 x 3.125Gb/s in 10GbE operation or 4 x 3.1875 in 10G Fibre Channel operation
- Supports 4 x 3.35Gb/s in ODU-2 over XAUI mode
- Fully XAUI and Fibre Channel Jitter Compliant

Clocking

- On chip fractional Clock Management Unit from one common reference clock input for all Baud rates
- Digitally controlled frac N PLL for TX and RX (enables single reference clock frequency)
- One reference clock (1/64th or 1/16th)
- Recovered Clock Reference Output

"Right Sized" Transport of 10GE-LAN signals through OTN Network

- GFP encapsulation used for packing 10GE-LAN signal into "Right Sized" OTU-2 signal resulting in channel rate of 10.7 GHz.
- Two different flow-control options used on client to allow for 10GE-LAN signal to be packed into OTU-2.
- Proprietary 10GE-LAN mapping into an OTU-2, via GFP, without transport rate increase or client flow control.
- 10GE-LAN into WIS to allow for SONET/SDH grooming of 10GE client.

G.709 ODU-2 Synchronous and Asynchronous Mapping

- 1 x OC192/STM-64 mapping (239,237) per G.709.
- Direct map (239,238) into ODU-2.

G.709 Overhead Processing

- Insert/Drop Port for access to all of ODU-2 overhead
- Dedicated GCC ports.

Ingress and Egress Line Data Performance Monitoring

- 1 x OC192C TOH Add/Drop and processing.
- 8B/10B Monitoring.
- 10GbE Monitoring.
- SONET/SDH Overhead Monitoring per IEEE802.3ae WIS.
- LOS, OOF, LOF detection.
- B1, B2 monitoring with programmable Signal Degrade and Signal Fail thresholds.
- J0, J1 Monitoring, SDH and SONET modes.
- K1, K2 monitoring for APS changes, line AIS and line RDI.
- Automatic, interrupt-driven, or manual AIS insertion.

Industry Standard RS(255,239) Forward Error Correction with 6.2 dB Coding Gain (at 10-15 CER)

- G.709 Compliant Frame Structure.

Enhanced Gain Forward Error Correction with G.709 ODU

- 10.71, 10.66, 11.1, 11.27Gbps enhanced FEC with >8dB coding gain.
- G.709 overhead processing and nominal rate expansion.
- Comprehensive channel statistics gathering.
- Corrected bits, bytes.
- Corrected zeros, ones (with outputs).
- Uncorrectable sub-frame count.

System/Backplane and Line side loopback

- System/Backplane side and Line side loopbacks

Support For System Test and Diagnostics

- Can synthesize WIS (SONET/SDH) frame.
- Error injection capability for verification of remote error reporting.
- Test-set compliant pseudo-random sequence generation/analysis.

General Purpose Processor Interface

- Glueless 16-bit interface to MPC860, 25 MHz to 66 MHz.
- Dual mode interface also supports Intel processors.
- Interrupt driven or Polled mode operation.

Additional Protocol Support

- FEC Frame Synchronous scrambling.
- Programmable sequence detection.

10GE-LAN MAPPING

The Pemaquid device supports 7 distinct methods to map 10GE-LAN into either OTU-2 or OC-192 signals for transport. Several of the mapping modes are similar to modes implemented in Rubicon.

The first mode is the Bit Transparency Mode. In this mode, the Line rate operates at 7% above the PCS Encoded Rate. Specifically, the XAU1 (Ethernet) data is transparently mapped into an OTU-2 frame and output at either 11.096 or 11.049Gbs, depending if fix stuff bytes are provisioned or not.

The second and third mapping methods are similar and involve GFP encapsulation directly into a standard rate 10.7GHz OTU-2 frame. The two methods employ different manners of system/backplane flow control to limit the system/backplane data rate so that correct encapsulation into the OTU-2 frame can take place. The first method of flow control is called "pre-emptive" flow control. In this mode the Pemaquid asserts flow control signals back to the system/backplane in regular intervals, thereby guaranteeing that the system/backplane does not overflow the capacity of the OTU-2 frame. The second method allows for the user to place a FIFO-fill line on the ingress system/backplane fifo inside the Pemaquid. When the fifo-fill line is crossed the Pemaquid asserts flow control signals back to the system/backplane in order to bleed off the ingress system/backplane fifo.

The fourth manner of 10E-LAN mapping also involves GFP mapping, and in addition, utilizes some of the OPU overhead bytes to enable full 10GbE preamble transparency and yield a G.709/OTU-2 compliant 10.7Gb/s signal. No back-

pressure/flow control mechanism is required to rate limit the system/backplane in this mode of operation.

The fifth manner in which 10GE-LAN mapping is supported is the WIS mode. In this mode, 10GE-LAN traffic is directly encapsulated into a WIS frame and output at a 9.953 Gb/s rate.

Additionally, in a similar sixth mode, the WIS frame can further be encapsulated into an OTU-2 frame and output at a G.709 compliant 10.7Gb/s signal.

Finally, Pemaquid also supports a pure LAN mode, where the 10GE-LAN signal is passed through the Pemaquid device and output on the Line interface at a 10.3Gb/s rate.

AIS SUPPORT

For applications in which the Line signal is G.709 compliant or for OTN applications, Line Fail and un-equipped OTN AIS is supported. For OTN edge applications, the device can be provisioned to provide a Local Fault (LF) indication or an OTN Generic AIS to the Line Interface. This facilitates convergence of the WIS (SONET/SDH) and OTN functions into a single network element.

ODU MAPPING

ITU compliant system/backplane mapping of 10GbE and 10G Fibre Channel signals into ODU-2 signals, via GFP and WIS frames, is supported whereby a stuff column is added to every G.709 sub-frame resulting in an ODU rate expansion of (239/237). The chip can be configured to insert the G.709 compliant stuff-byte value or to insert user data into this column. The values assigned to the stuff bytes can be defined from a register set on chip. Coverage of these stuff columns in the BIP calculation or in the FEC is optional and can be enabled via software. When the no-coverage option is enabled, the BIP and parity check values are calculated as if the standard stuff values were present.

A direct map mode is supported for ODU-2 with no stuff columns to enable mapping with a 239/238 rate expansion. Start-of-frame signals are provided at the input and output ports to enable synchronization to the ODU.

LOOPBACK FUNCTIONS

Near-end and far-end loopbacks are supported for the System/Backplane interface and for the line interface. This enables line and device testing and fault isolation. Each functional block may be bypassed as required to support the application.

Figure 2. ODU Switch Application (with ODU-1 MUX to OTU-2 Signal Generation)

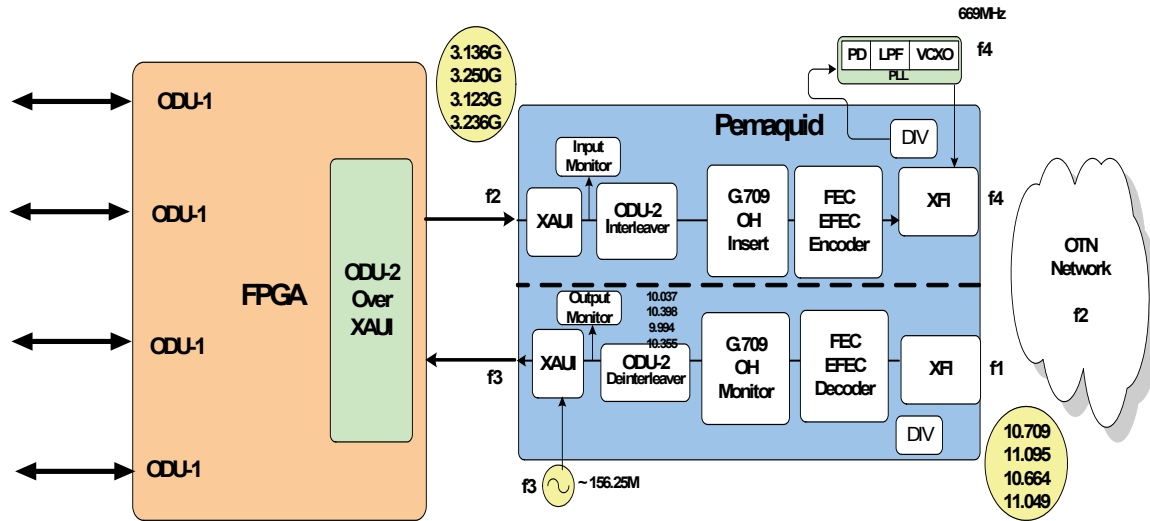
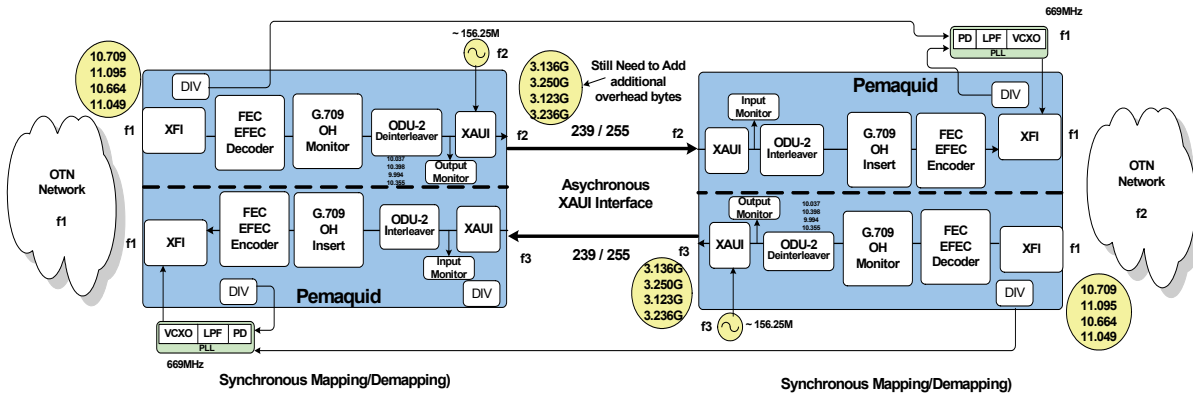


Figure 3. Full Duplex EFEC Regeneration Application (Synchronous)

8 Clock Domains are powered on

Shown below is a full duplex regenerator application in this configuration the backward indications such as BDI, BEI for SM, PM all TCMS. And FTLF can be propagated automatically within the devices. However power consumption for the entire solution will be higher vs the Simplex EFEC Regen solution



Full Duplex Regeneration (Synchronous Network) Back to Back EFEC Connection (Same Board)

For technical support inquiries, submit your product related questions to support@appliedmicro.com.

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