

Automotive MOSFET

OptiMOS™ 5 Power-Transistor



Features

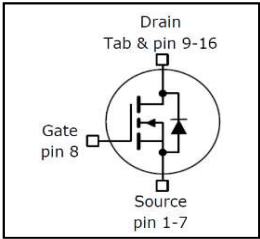
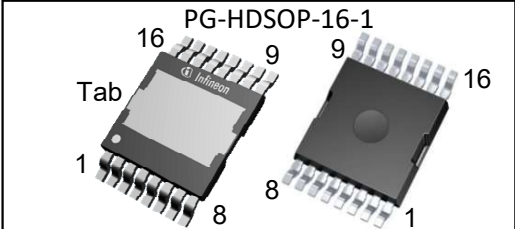
- OptiMOS™ power MOSFET for automotive applications
- N-channel – enhancement mode – normal level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% avalanche tested
- Very low reverse recovery charge (Q_{rr})

Potential applications

General automotive applications.

Product validation

Qualified for automotive applications. Product validation according to AEC-Q101.



Product Summary

V_{DS}	120	V
$R_{DS(on)}$	1.8	mΩ
I_D (chip limited)	309	A

Type	Package	Marking
IAUTN12S5N018T	PG-HDSOP-16-1	5N12N018



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Maximum ratings

at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$V_{GS}=10\text{ V}$, Chip limitation ^{1,2)}	309	A
		$V_{GS}=10\text{ V}$, DC current ³⁾	300	
		$T_a=100\text{ °C}$, $V_{GS}=10\text{ V}$, R_{thJA} on top ^{2,4)}	85	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_c=25\text{ °C}$, $t_p=100\text{ }\mu\text{s}$	1150	
Avalanche energy, single pulse ²⁾	E_{AS}	$I_D=150\text{ A}$	510	mJ
Avalanche current, single pulse	I_{AS}	–	300	A
Gate source voltage	V_{GS}	–	± 20	V
Power dissipation	P_{tot}	$T_c=25\text{ °C}$	358	W
Operating and storage temperature	T_j, T_{stg}	–	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	–	–	55/175/56	

Thermal characteristics²⁾

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal resistance, junction - case	R_{thJC}	Top	-	-	0.42	K/W
		Bottom (Pin 1-7)	-	9	-	
		Bottom (Pin 9-16)	-	3	-	
Thermal resistance, junction - ambient ⁴⁾	R_{thJA}	Top	-	2.8	-	
		Bottom (through PCB)	-	40	-	

Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Static characteristics

Drain-source breakdown voltage	$V_{(Br)DSS}$	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$	120	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=270\text{ }\mu\text{A}$	2.6	3.1	3.6	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=120\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$	-	0.3	3	μA
		$V_{DS}=120\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=100\text{ °C}^{2)}$	-	10	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=7\text{ V}$, $I_D=50\text{ A}$	-	2.0	2.8	m Ω
		$V_{GS}=10\text{ V}$, $I_D=100\text{ A}$	-	1.5	1.8	
Gate resistance ²⁾	R_G	-	-	1.1	-	Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics ²⁾						
Input capacitance	C _{iss}	V _{GS} =0 V, V _{DS} =60 V, f=1 MHz	–	8260	10740	pF
Output capacitance	C _{oss}		–	2369	3080	
Reverse transfer capacitance	C _{rss}		–	45	68	
Turn-on delay time	t _{d(on)}	V _{DD} =60 V, V _{GS} =10 V, I _D =100 A, R _G =3.5 Ω	–	28	–	ns
Rise time	t _r		–	55	–	
Turn-off delay time	t _{d(off)}		–	45	–	
Fall time	t _f		–	53	–	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=60\text{ V}, I_D=100\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	–	43	55	nC
Gate to drain charge	Q_{gd}		–	23	35	
Gate charge total	Q_g		–	111	145	
Gate plateau voltage	$V_{plateau}$		–	5.2	–	V

Reverse Diode

Diode continuous forward current ²⁾	I_S	$T_C=25\text{ °C}$	–	–	309	A
Diode pulse current ²⁾	$I_{S,pulse}$	$T_C=25\text{ °C}, t_p=100\ \mu\text{s}$	–	–	1150	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=100\text{ A}, T_j=25\text{ °C}$	–	0.85	0.95	V
Reverse recovery time ²⁾	t_{rr}	$V_R=60\text{ V}, I_F=50\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$	–	45	67	ns
Reverse recovery charge ²⁾	Q_{rr}		–	34	68	nC

¹⁾ Practically the current is limited by the overall system design including the customer-specific PCB.

²⁾ The parameter is not subject to production testing – specified by design.

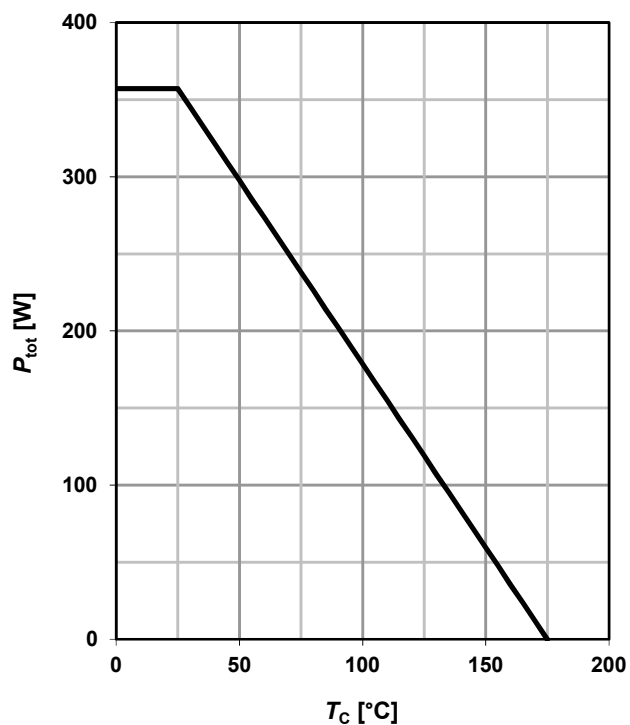
³⁾ Current is limited by chip.

⁴⁾ Device on a four-layer 2s2p FR4 PCB with topside cooling. Thermal insulation material is 100 μm thick and has a conductivity of 0.7 W/m/K. Top surface of heat sink is fixed at ambient temperature. Bottom surface of PCB is left at free convection. Values may vary depending on the customer-specific design.

Electrical characteristics diagrams

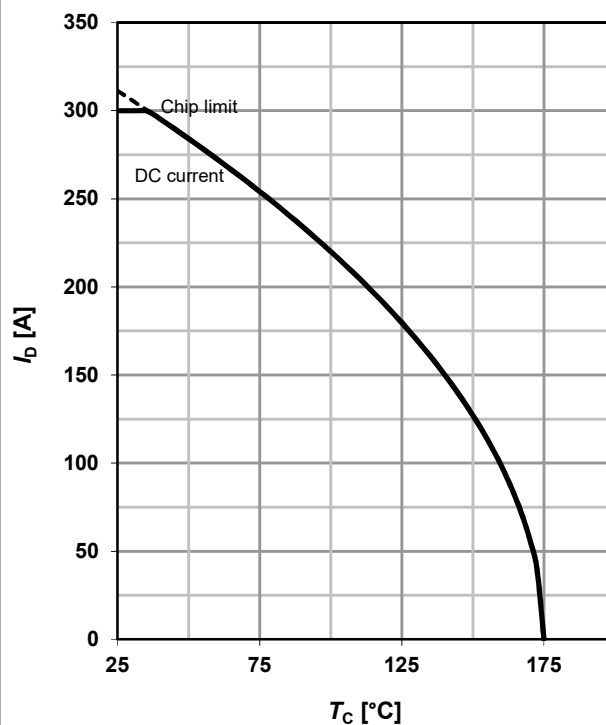
1 Power dissipation

$$P_{\text{tot}} = f(T_c); V_{\text{GS}} \geq 6 \text{ V}$$



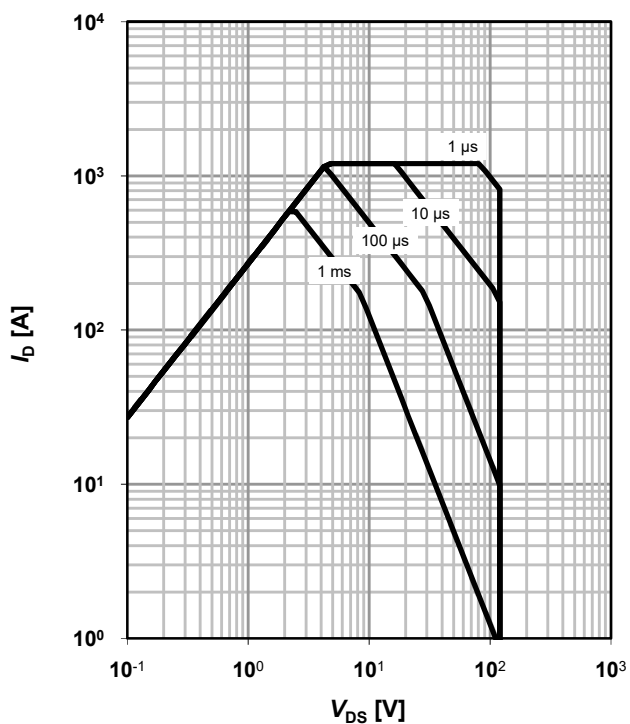
2 Drain current

$$I_D = f(T_c); V_{\text{GS}} \geq 6 \text{ V}$$



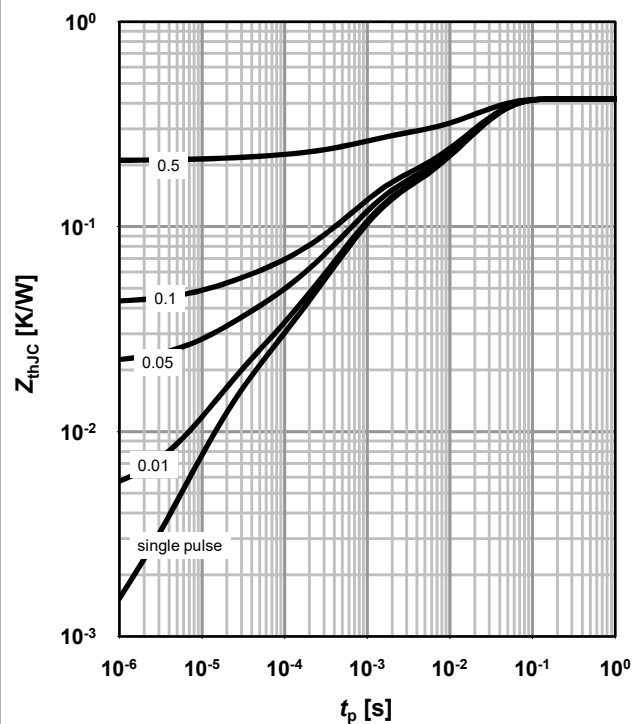
3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_c = 25^\circ\text{C}; D = 0; \text{parameter: } t_p$$

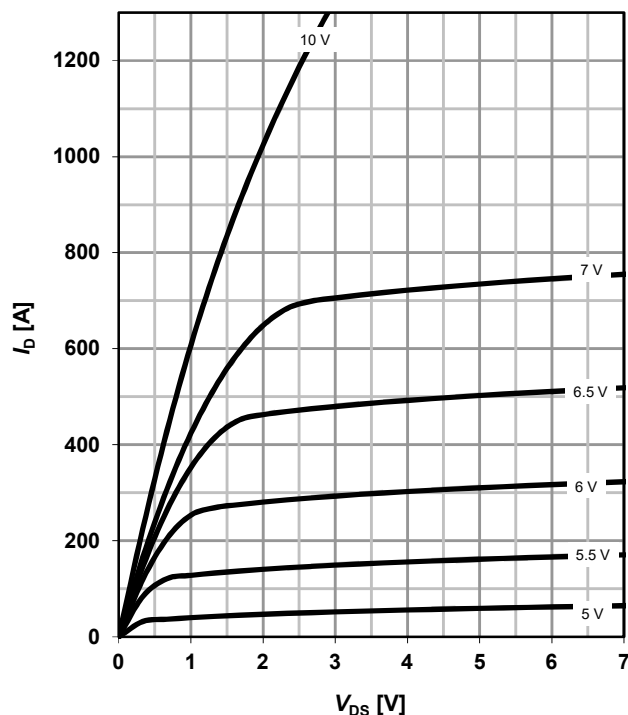


4 Max. transient thermal impedance

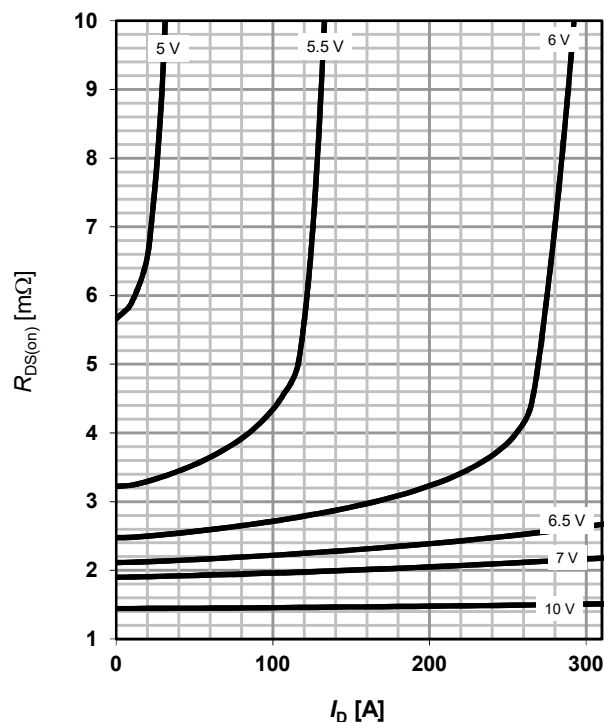
$$Z_{\text{thJC}} = f(t_p); \text{parameter: } D = t_p/T$$



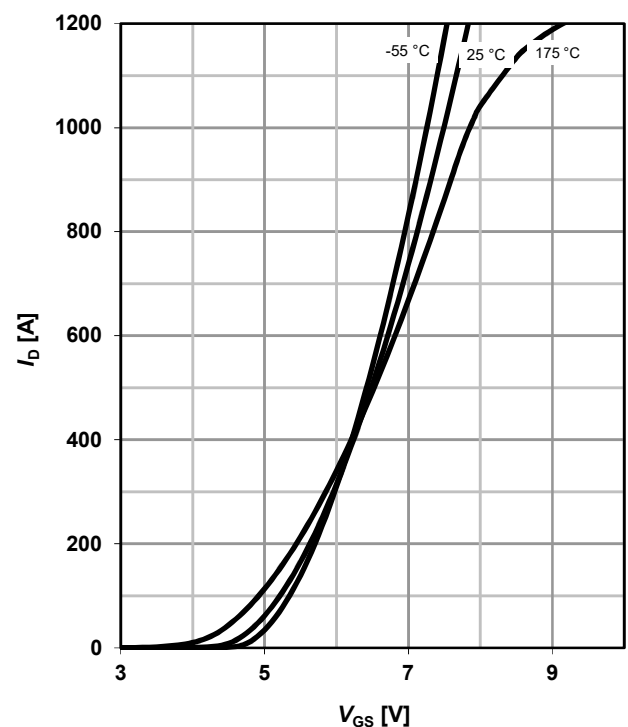
5 Typ. output characteristics

 $I_D = f(V_{DS}); T_j = 25^\circ\text{C}; \text{parameter: } V_{GS}$


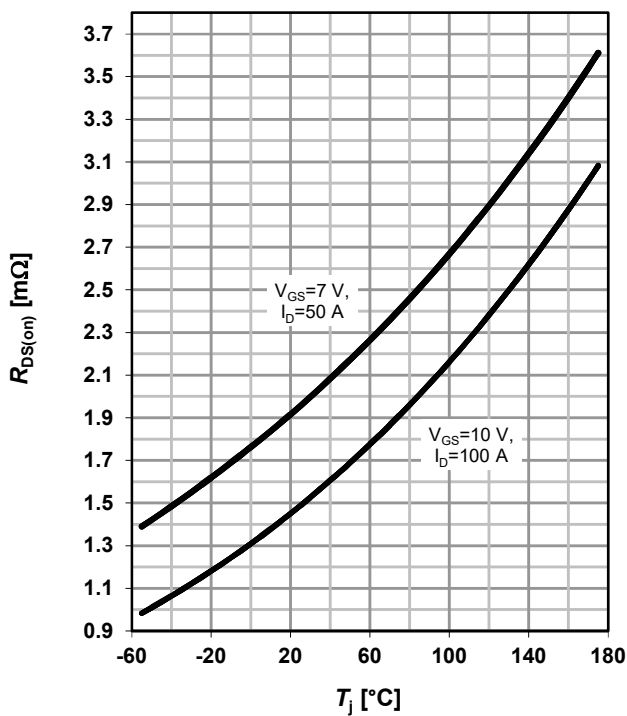
6 Typ. drain-source on-state resistance

 $R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}; \text{parameter: } V_{GS}$


7 Typ. transfer characteristics

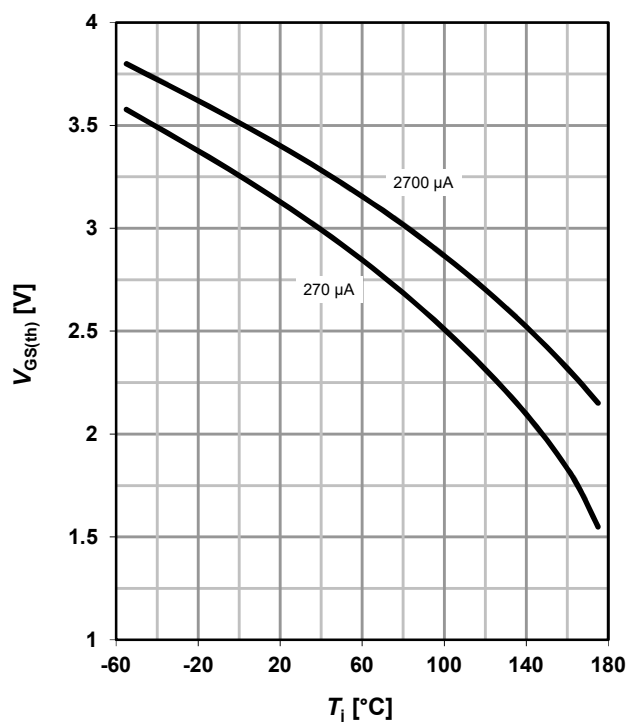
 $I_D = f(V_{GS}); V_{DS} = 6\text{ V}; \text{parameter: } T_j$


8 Typ. drain-source on-state resistance

 $R_{DS(on)} = f(T_j); \text{parameter: } I_D, V_{GS}$


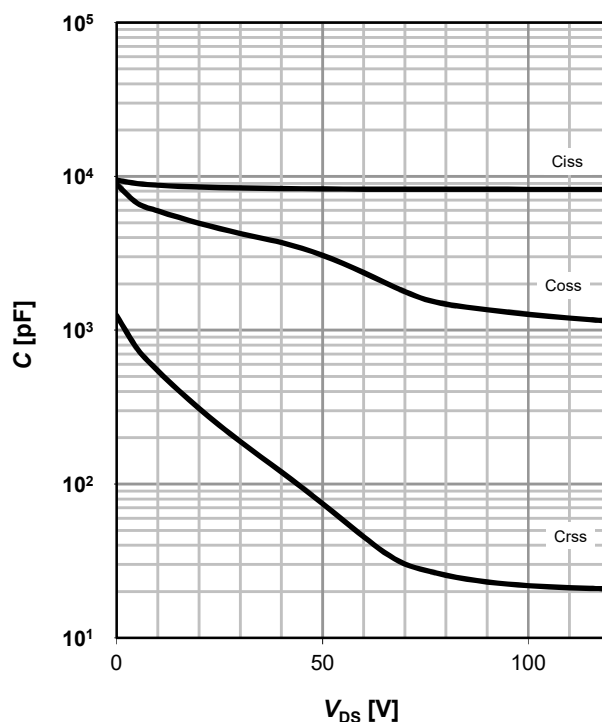
9 Typ. gate threshold voltage

$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$; parameter: I_D



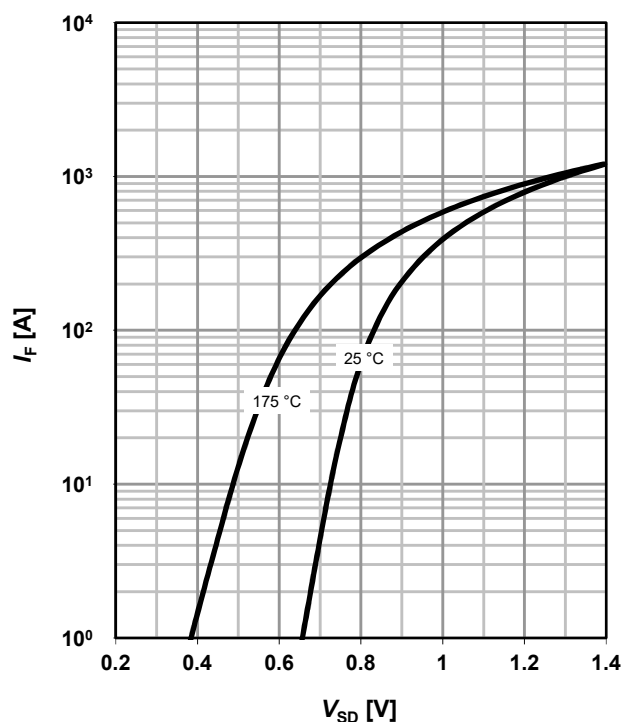
10 Typ. capacitances

$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz



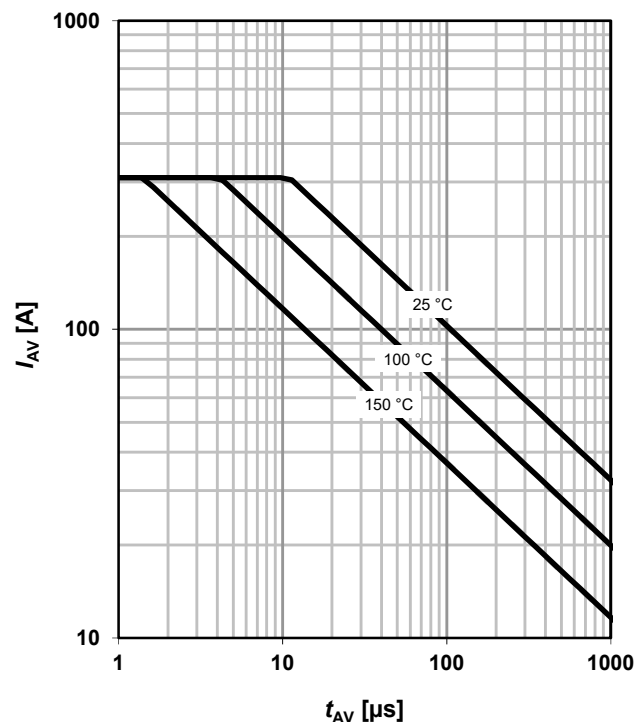
11 Typical forward diode characteristics

$I_F = f(V_{SD})$; parameter: T_j



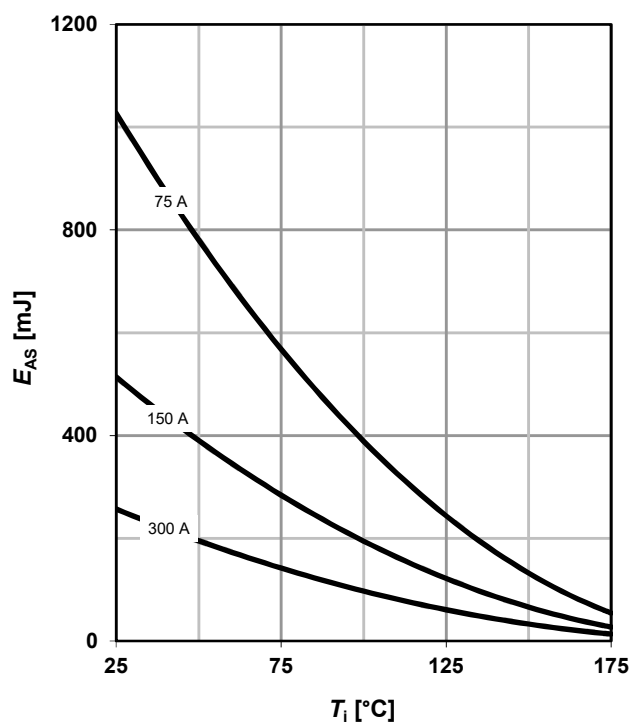
12 Typ. avalanche characteristics

$I_{AS} = f(t_{AV})$; parameter: $T_{j(start)}$



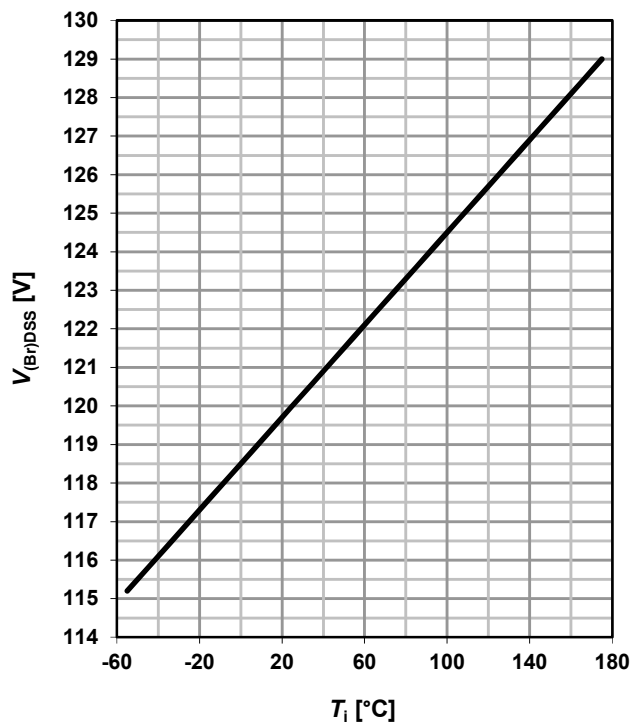
13 Typical avalanche energy

$E_{AS} = f(T_j)$; parameter: ID



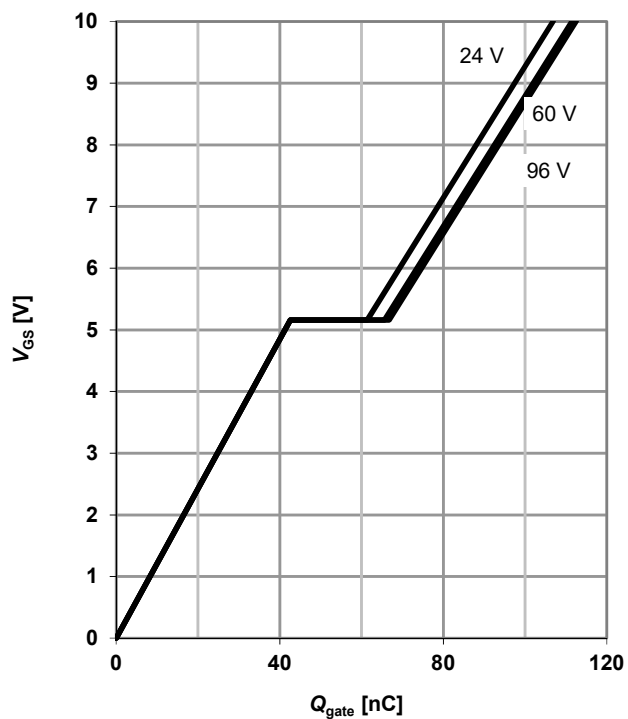
14 Drain-source breakdown voltage

$V_{(Br)DSS} = f(T_j)$; $I_D = 1$ mA

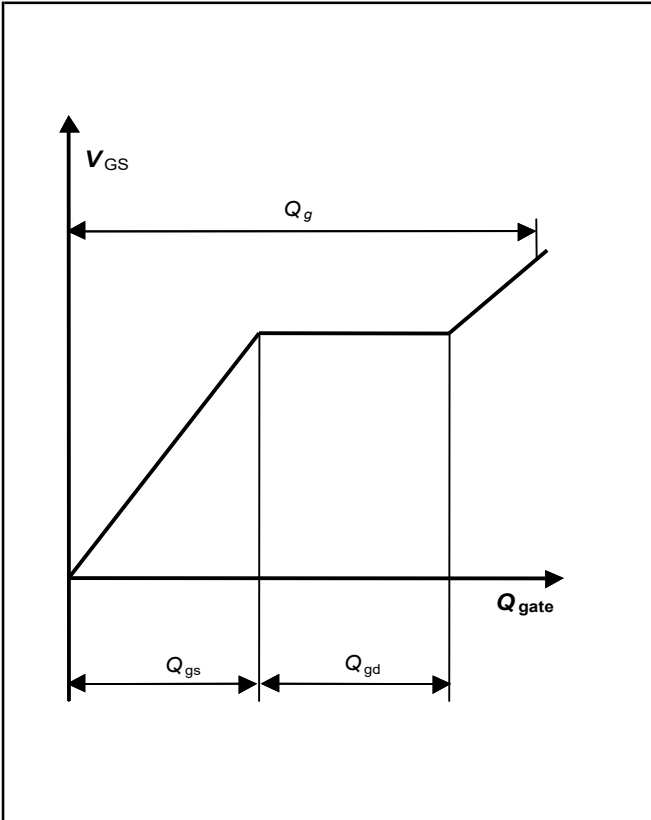


15 Typ. gate charge

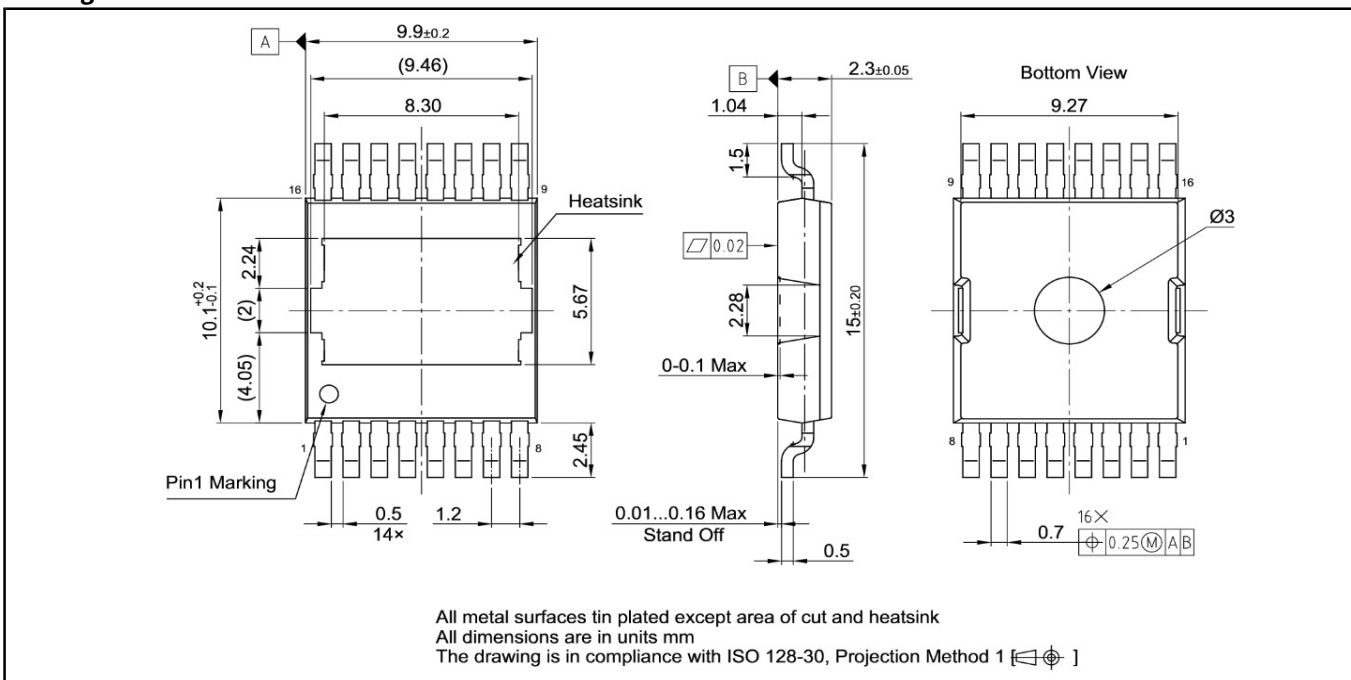
$V_{GS} = f(Q_{gate})$; $I_D = 100$ A pulsed; parameter: V_{DD}



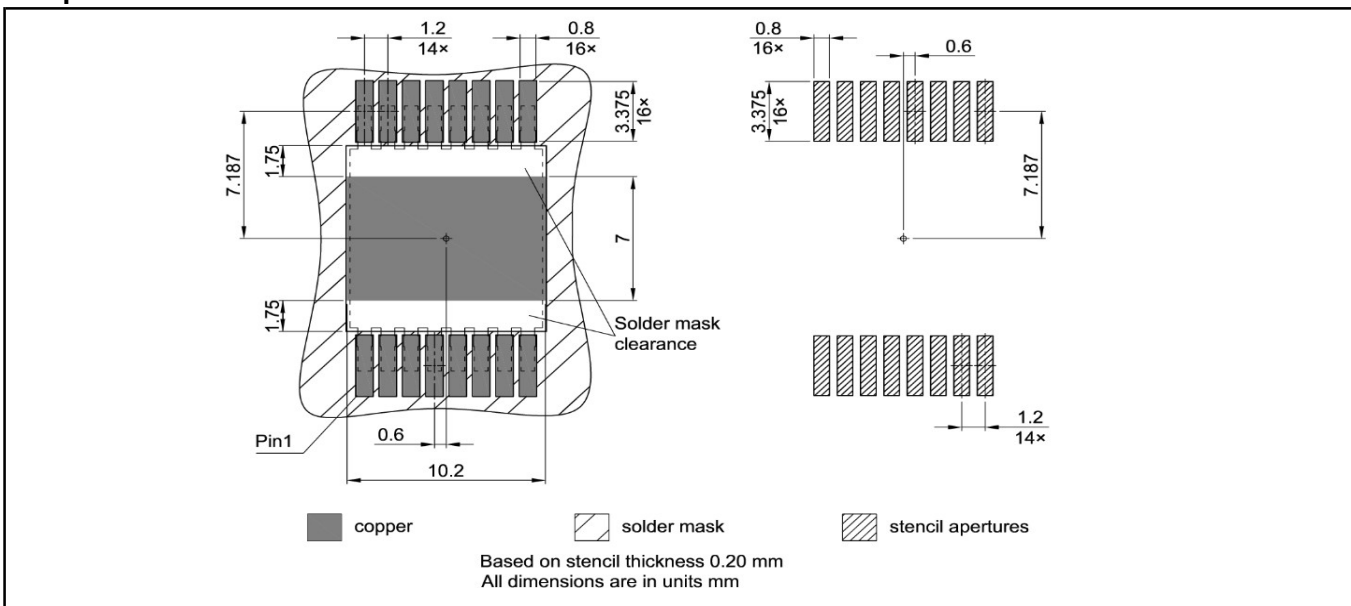
16 Gate charge waveforms



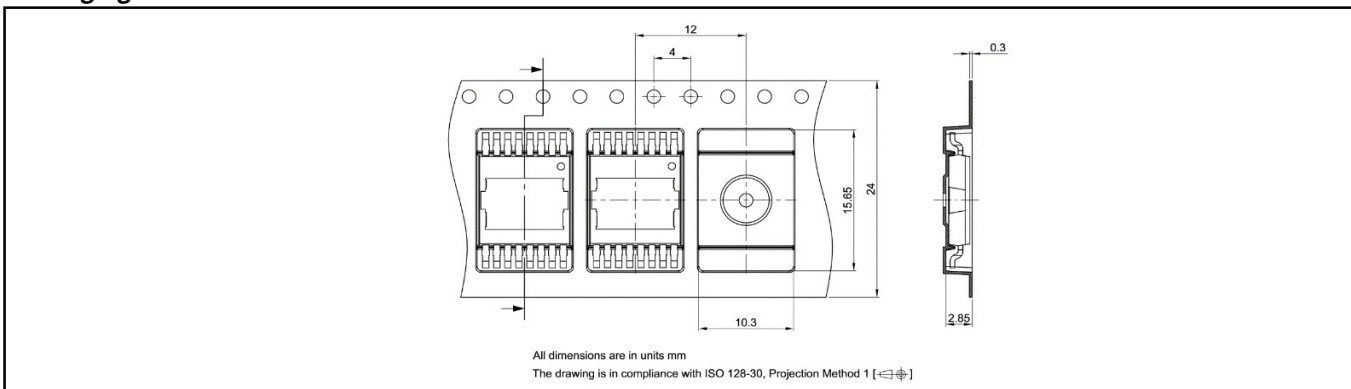
Package Outline



Footprint



Packaging



Revision History

Revision	Date	Changes
Revision 1.0	2022-12-15	Final data sheet
Revision 1.01	2023-08-29	Reduced typical on-state resistance

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