

MAX16926

Automotive 4-Output Display Power Solution with Watchdog

General Description

The MAX16926 is a 4-channel power-management IC designed to accommodate the main rails used in modern automotive TFT displays. The MAX16926 and the MAX20069 TFT power supply and LED backlight driver combine to provide a two-chip solution to automotive display power requirements.

The MAX16926 integrates a high-voltage buck converter that transforms battery voltages into a 3.3V intermediate rail. In addition, a high-voltage, always-on, low-quiescent-current linear regulator supplies power at 3.3V.

The low-voltage section consists of a fully-integrated DC/DC converter and an LDO running off the intermediate rail. The low-voltage DC/DC converter provides 1.1V, while the LDO produces 1.8V. In addition, an integrated watchdog timer guards against runaway code.

A single START control pin initiates the start-up sequence, thereby simplifying device control. The MAX16926's external pMOSFET control block allows battery voltage to be switched to a downstream device, such as a backlight boost converter.

The MAX16926 is available in a TQFN package and operates in the -40°C to 105°C temperature range.

Applications

- Infotainment Displays
- Central Information Displays
- Instrument Clusters

Benefits and Features

- High Integration
 - Complete Display Power Solution from Automotive Battery
 - One High-Voltage 2.1A Buck Converter (3.3V)
 - One High-Voltage 100mA Low-I_Q Linear Regulator (3.3V)
 - One Low-Voltage 1.6A Buck Converter (1.1V)
 - One 175mA Low-Voltage Linear Regulator (1.8V)
 - Power-Good Outputs
- Integrated Watchdog Timer
- Robust and Low EMI
- Programmable Switching Frequency
- Internal Spread Spectrum Oscillator
- Slew-Rate Controlled Switching
- Thermal Shutdown Protection
- Compact TQFN20 4mm x 4mm Package

Ordering Information appears at end of datasheet.

Simplified Block Diagram

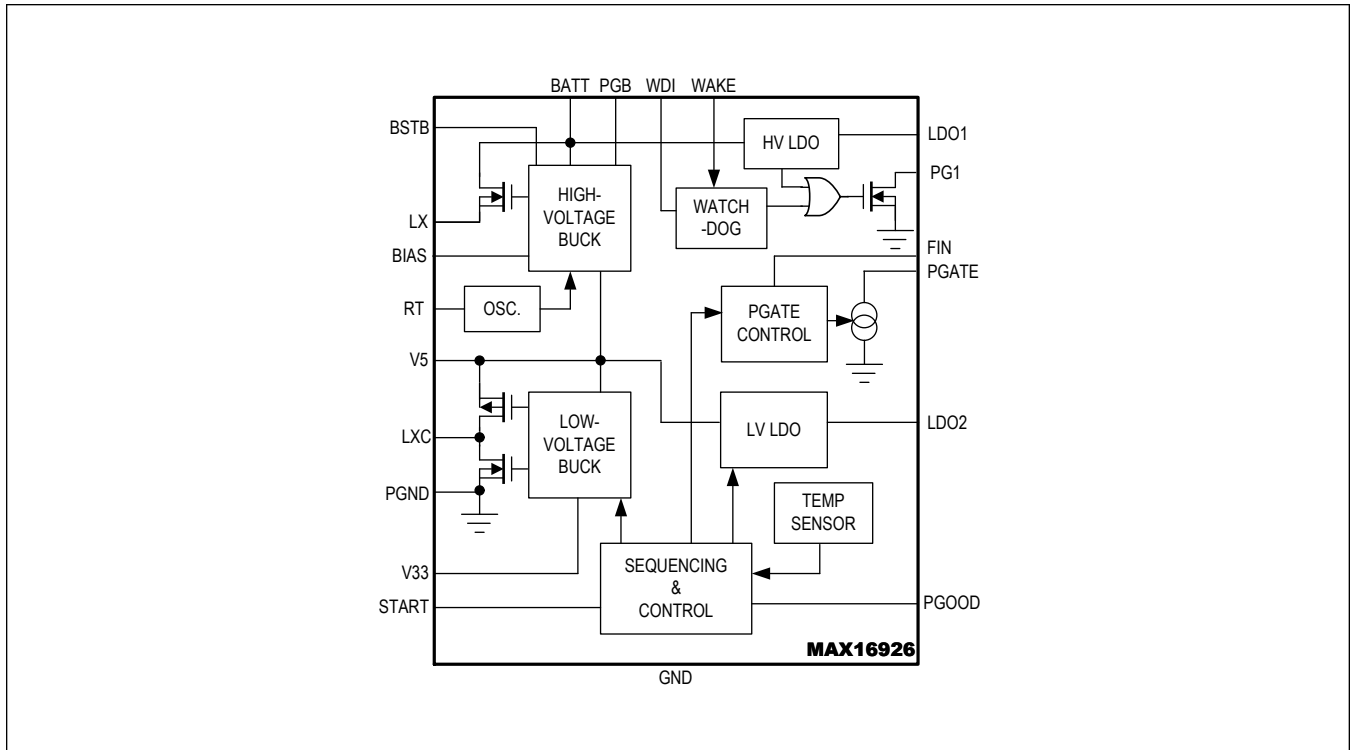


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Absolute Maximum Ratings

BATT, PGATE to GND	-0.3V to 40V	BSTB to LX	-0.3V to +6V
LXC, V33, LDO2 to GND	-0.3V to V5 + 0.3V	LX to GND	-0.3V to V _{BATT} + 0.3V
START, WAKE to GND	-0.3V to +6V	Continuous Power Dissipation (Single-Layer Board) (T _A = +70°C, derate 20.8mW/°C above +70°C.)	1667mW
RT, WDI, FIN to GND	-0.3V to BIAS + 0.3V	Continuous Power Dissipation (Multilayer Board) (T _A = +70°C, derate 30.3mW/°C above +70°C.)	mW to 2424mW
PGB, PGOOD, PG1, BIAS, V5, LDO1 to GND	-0.3V to +6V	Operating Temperature Range	-40°C to 105°C
PGND to GND	-0.3V to +0.3V		
LX, LXC Short-Circuit Duration	<u>Continuous</u>		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

TQFN

Package Code	T2044+4C
Outline Number	21-100172
Land Pattern Number	90-0409
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ _{JA})	48
Junction to Case (θ _{JC})	2
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ _{JA})	33
Junction to Case (θ _{JC})	2

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{BATT} = 12V, T_A = T_j = -40°C to +105°C unless otherwise noted. Typical values are at +25°C under normal conditions unless otherwise noted. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER INPUT						
Input Voltage Range			3.5		36	V
		<1s	36		40	
Operating Supply Current	I _{SUP}	No load, no switching, START = WAKE = 1		4.5	8	mA
Standby Supply Current	I _{STDBY}	START = WAKE = 0, only LDO1 active with no load, V _{BATT} = 12V		14.5	25.5	µA
Undervoltage Lockout, Rising	BATTUVLO _R			3	3.45	V
Undervoltage Lockout, Falling	BATTUVLO _F		2.5	2.9		V
Thermal Shutdown, Rising	TSHDN _R			160		°C

Electrical Characteristics (continued)

($V_{BATT} = 12V$, $T_A = T_J = -40^{\circ}C$ to $+105^{\circ}C$ unless otherwise noted. Typical values are at $+25^{\circ}C$ under normal conditions unless otherwise noted. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermal Shutdown, Falling	TSHDN _F			140		°C
BIAS REGULATOR						
BIAS Output Voltage		$V_{BATT} > 6V$		3.3		V
HIGH-VOLTAGE BUCK CONVERTER						
Output Voltage	OUT _{HV33}	Output current range 0A to 1.2A	3.234	3.3	3.366	V
Switching Frequency	f _{SW}	R _{RT} = 10kΩ ±1%	360	400	440	kHz
		R _{RT} = 30kΩ ±1%		440		
		R _{RT} = 56kΩ ±1%		2000		
		R _{RT} = 82kΩ ±1%	2000	2200	2400	
Switching Frequency Dither			±3			%
High-Side Switch On-Resistance	HSRON _H	I _{LX} = 0.5A		0.09	0.2	Ω
Current-Limit Threshold	HSILIM		2.4	3	4	A
Line Regulation		V_{BATT} 6V to 36V, I _{LOAD} 1.2A		83		μV/V
Load Regulation		Output current range 0A to 2.1A		8.8		mV
Soft-Start Time	T _{SS_H}			2.2	2.35	ms
PGB Threshold, V5 Rising	UV _{V5R}		93	95	97.6	%
PGB Threshold, V5 Falling	UV _{V5F}		90	92	94.5	%
PGB Debounce Time				20		μs
Maximum Duty-Cycle			98	99		%
LOW-VOLTAGE BUCK CONVERTER						
Input Voltage Range			3.234	5	5.25	V
Output Voltage	OUT _{L11}	Full output current range (0 to 1.6A)	1.075	1.1	1.125	V
Switching Frequency	f _{SW}	R _{RT} = 30kΩ (or 82kΩ)	2000	2200	2400	kHz
Switching Frequency Dither				±3		%
High-Side Switch On-Resistance	R _{PCH}			0.1	0.25	Ω
Low-Side Switch On-Resistance	R _{NCH}			0.08	0.135	Ω
Current-Limit Threshold	ILIM _{V33}		1.8	2.3	3.7	A
Load Regulation		Output current range 0A to 1.6A		2		mV
Soft-Start Time	T _{SS_{V33}}			1	1.1	ms
V33 Power-Good Threshold, Rising			93	95	97.5	%

Electrical Characteristics (continued)

($V_{BATT} = 12V$, $T_A = T_j = -40^{\circ}C$ to $+105^{\circ}C$ unless otherwise noted. Typical values are at $+25^{\circ}C$ under normal conditions unless otherwise noted. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V33 Power-Good Threshold, Falling			89.8	92	94.5	%
Maximum Duty Cycle					100	%
HIGH-VOLTAGE LINEAR REGULATOR (LDO1)						
LDO1 Output Voltage		0 to 50mA output current	3.234	3.3	3.366	V
LDO1 Current Limit			100		300	mA
Dropout Voltage		$I_{LDO1} = 75mA$			0.21	V
Line Regulation		$I_{LDO1} = 50mA$, $V_{BATT} = 4V$ to $36V$		170		$\mu V/V$
Load Regulation		Full output current range, 1 to 100mA		6.8		mV
PG1 Threshold, Rising				3.05	3.15	V
PG1 Threshold, Falling			2.87	3		V
LOW-VOLTAGE LINEAR REGULATOR (LDO2)						
LDO2 Output Voltage			1.762	1.8	1.836	V
LDO2 Current Limit		V_{LDO2} 10% below regulation point	175	250	320	mA
Load Regulation		Full output current range (0 to 100mA)		6.7		mV
Soft-Start Time	TSS_{LDO2}			1	1.1	ms
LDO2 Power-Good Threshold, Rising			93	95	97.5	%
LDO2 Power-Good Threshold, Falling			90	92	94.5	%
PGATE OUTPUT						
PGATE Pulldown Current			115	200	300	μA
PGATE Leakage Current		$V_{PGATE} = 12V$		0.1	1	μA
WATCHDOG						
Watchdog Timeout Period			1450	1600	1750	ms
WDI Pulse Width			1			μs
PG1 Output Pulse Width				100		ms
LOGIC INPUTS AND OUTPUTS						
WAKE, START, FIN, WDI Input High Level			2			V
WAKE, START, FIN, WDI Input Low Level					0.7	V
WAKE, START, FIN, WDI Input Leakage Current				0.1	1	μA
PG1, PGB, PGOOD Output Low Voltage		Sinking 2mA			0.4	V

Electrical Characteristics (continued)

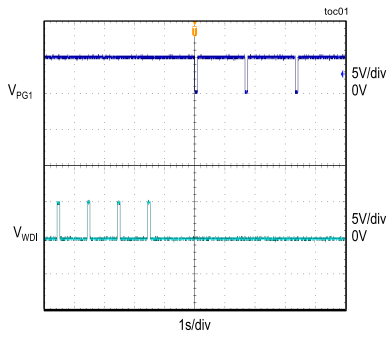
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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PG1, PGB, PGOOD Leakage Current		25°C Ambient Temperature		0.1	1	μA

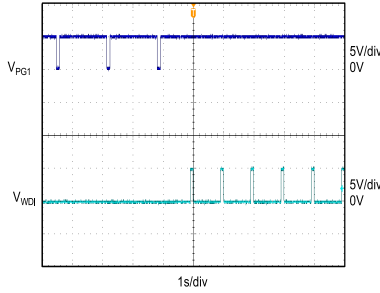
Typical Operating Characteristics

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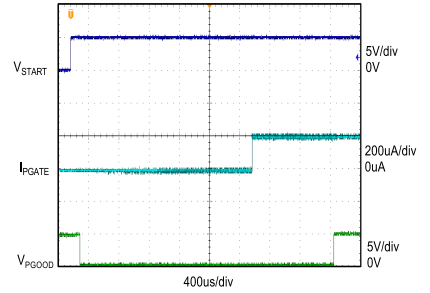
WATCHDOG ASSERTION



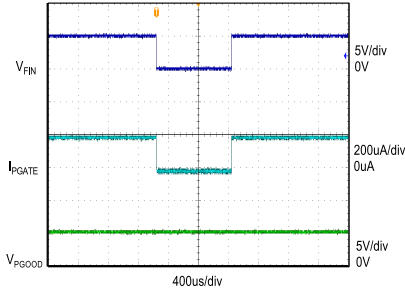
WATCHDOG DE-ASSERTION



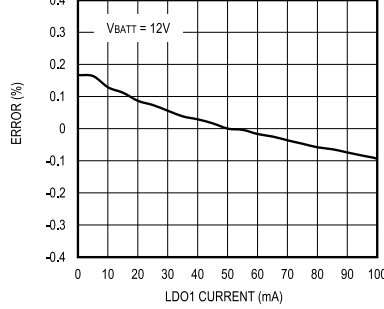
PGATE POWER UP



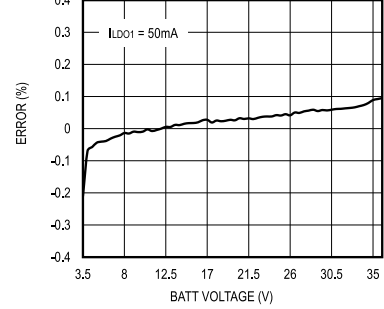
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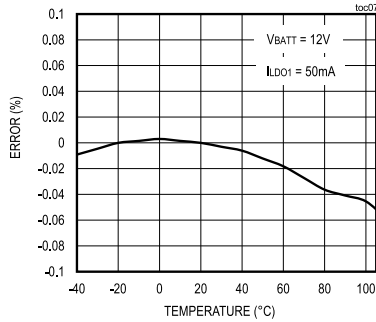
LDO1 LOAD REGULATION



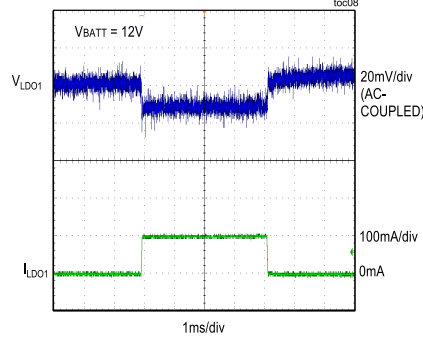
LDO1 LINE REGULATION



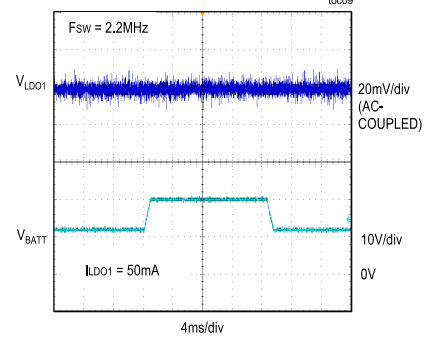
LDO1 REGULATION OVER TEMPERATURE



LDO1 LOAD STEP

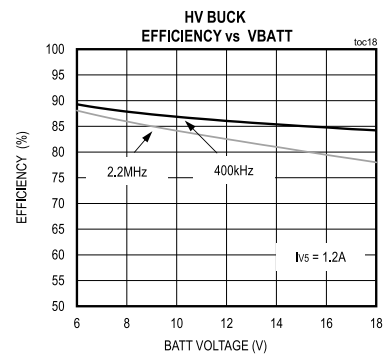
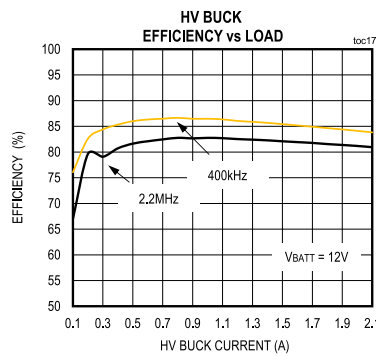
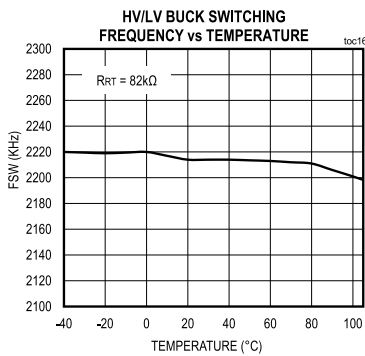
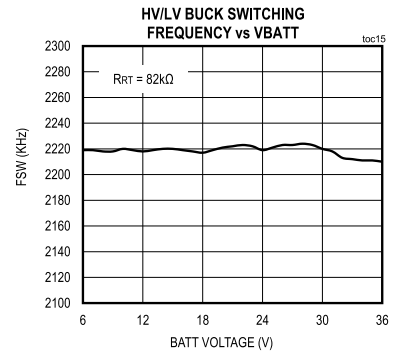
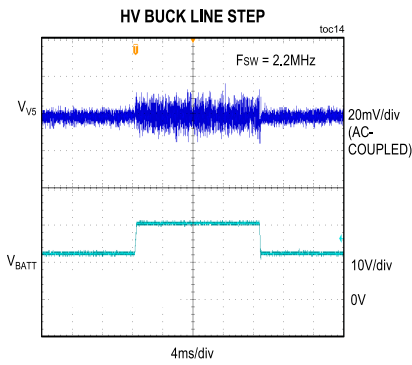
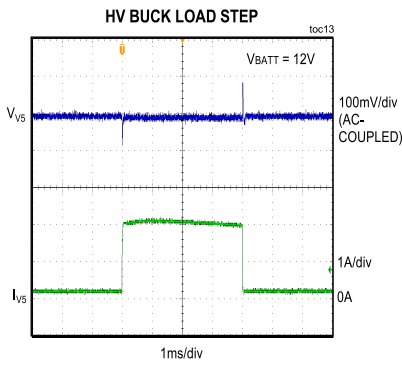
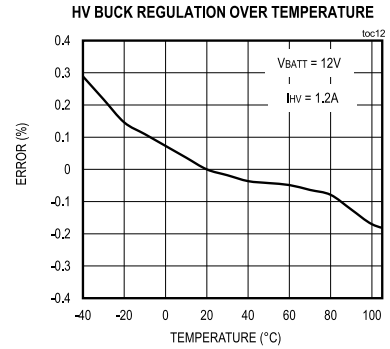
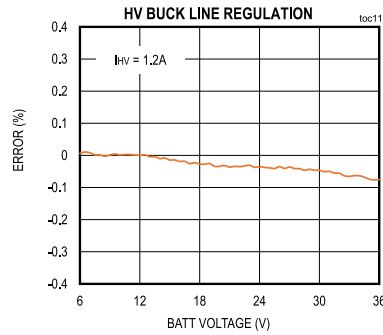
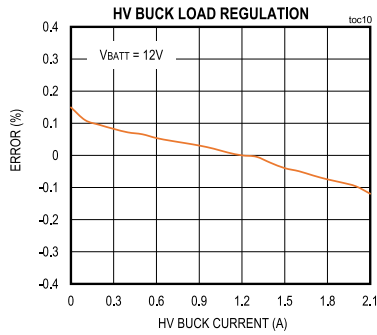


LDO1 LINE STEP



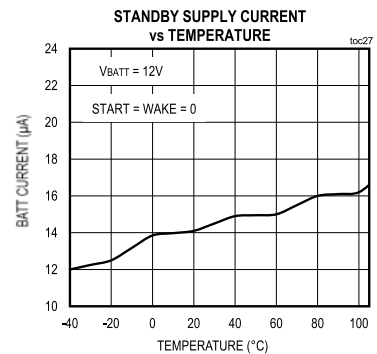
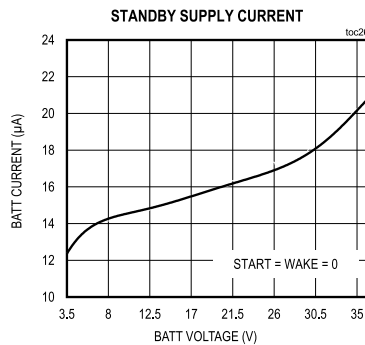
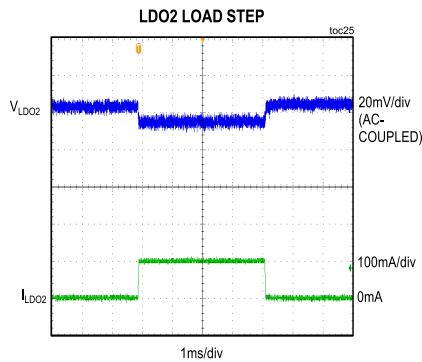
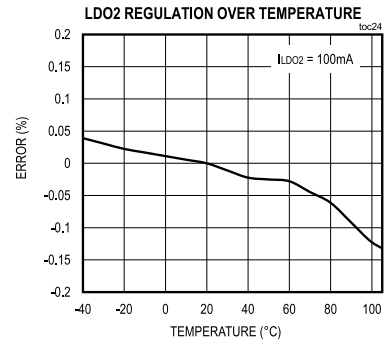
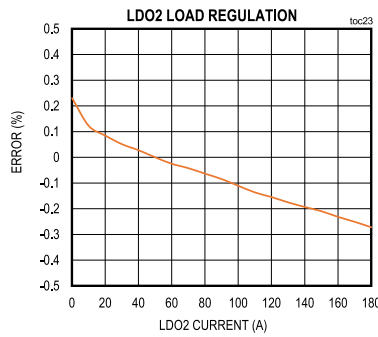
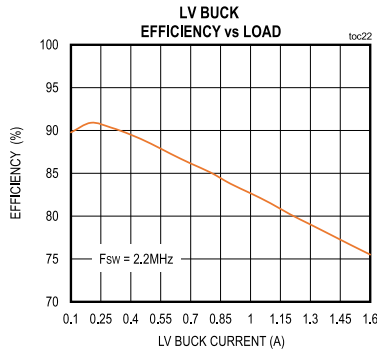
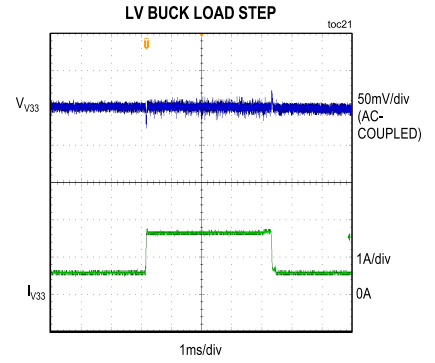
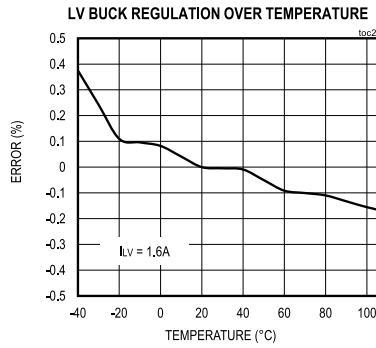
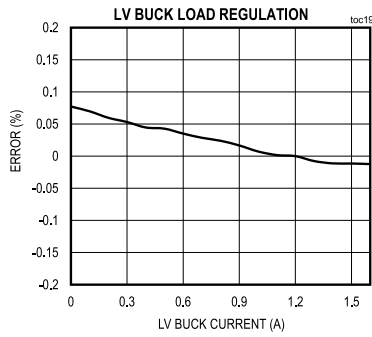
Typical Operating Characteristics (continued)

(($V_{BATT} = +12V$, $T_A = +25^\circ C$, unless otherwise noted.))



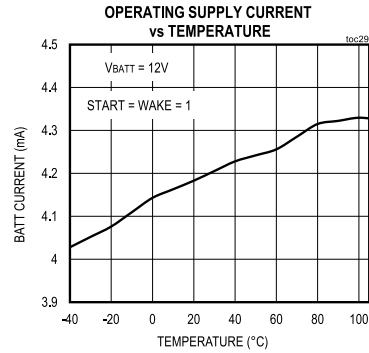
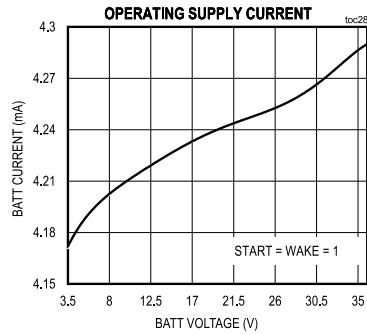
Typical Operating Characteristics (continued)

(($V_{BATT} = +12V$, $T_A = +25^\circ C$, unless otherwise noted.))



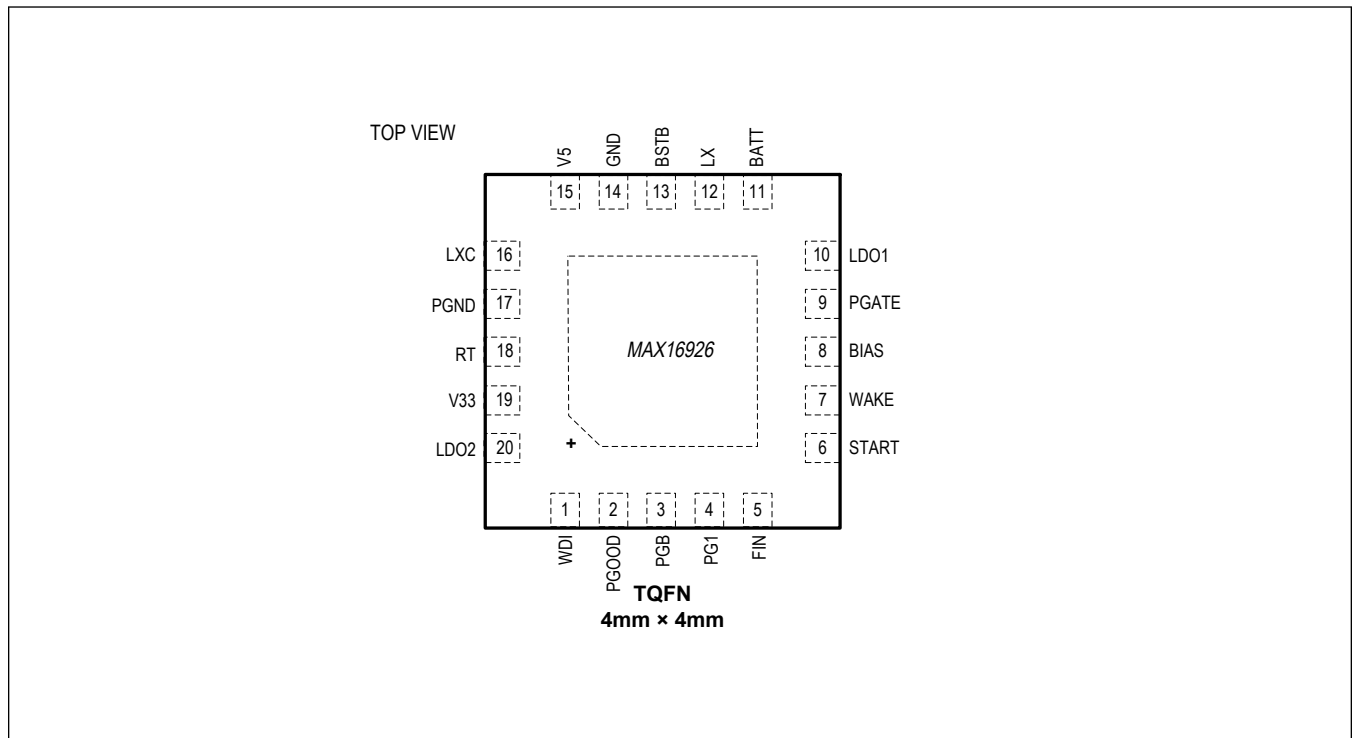
Typical Operating Characteristics (continued)

((V_{BATT} = +12V, T_A = +25°C, unless otherwise noted.))



Pin Configuration

MAX16926



Pin Description

PIN	NAME	FUNCTION
1	WDI	Watchdog Input. WDI is the reset input for the watchdog counter, which is cleared whenever there is a positive-going transition on WDI. The watchdog timer is active when one or both of the WAKE and START inputs is high. When the watchdog times out, PG1 asserts low. The watchdog can be disabled using appropriate resistor values on the RT pin (see Table 2).
2	PGOOD	Sequence Error Output (Open-Drain). When low, this pin indicates that the power-on sequence was not completed successfully or that one of the regulators (V5, V33, or LDO2) is out of regulation.
3	PGB	Open-Drain Power-Good Output for High-Voltage Buck Converter.
4	PG1	Open-Drain Power-Good Output for High-Voltage Linear Regulator.
5	FIN	Active-Low Fault-In Input. When FIN goes low, the PGATE output is disabled. If unused, connect FIN to GND.
6	START	Active-High Sequence Start Pin. When START is taken high, the power-on sequence is initiated. When START goes low, the power-off sequence is executed.
7	WAKE	Wake Input. When WAKE is high, the watchdog timer is enabled. When WAKE is low, the watchdog timer is off. When both WAKE and START are low, the IC is in low-quiescent-current mode.
8	BIAS	Output of Internal Bias Regulator for the High-Voltage Buck. Connect a ceramic capacitor of value 1 μ F between BIAS and GND.
9	PGATE	Current-sink drive output for external PMOS switch that supplies power to the display backlight section or to other battery-connected loads.
10	LDO1	Output of High-Voltage 3.3V Regulator. LDO1 is always active when the BATT voltage is above the undervoltage lockout level. The input to this regulator is BATT. Connect a bypass capacitor of at least 44 μ F from LDO1 to GND.
11	BATT	Battery Supply Input. Bypass BATT to GND with a ceramic capacitor of value 10 μ F.
12	LX	Switching Node of High-Voltage Buck Converter. Connect the buck inductor and rectifying diode to this pin, placing them as close as possible to the IC.
13	BSTB	Boost Capacitor Connection for High-Voltage Buck. Connect a 0.1 μ F capacitor from BSTB to LX.
14	GND	Ground Connection.
15	V5	3.3V Output of High-Voltage Buck Converter. Place the output filter capacitors at this pin. V5 is also the feedback point for the converter.
16	LXC	Switching node of low-voltage buck converter. Connect the buck inductor to this pin, placing it as close as possible to the IC.
17	PGND	Power Ground Connection.
18	RT	Frequency-Set Pin. Connect a resistor from RT to GND to set the switching frequency of the converters.
19	V33	1.8V Output of Low-Voltage Buck Converter. Place the output filter capacitors at this pin. V33 is also the feedback point for the converter. To use the low-voltage converter as a switch, connect V33 to GND.
20	LDO2	Output of Low-Voltage Linear Regulator. The input to this regulator is V5. Connect a bypass capacitor of at least 22 μ F from LDO2 to GND.

Detailed Description

The MAX16926 is a 4-channel power-management IC designed to accommodate the main rails used in modern automotive TFT displays. The MAX16926 and the MAX20069 TFT power supply and LED backlight driver combine to provide a two-chip solution to automotive display power supply requirements.

The high-voltage buck converter transforms battery voltages into a 3.3V intermediate rail. In addition, a high-voltage, always-on, low-quiescent-current linear regulator supplies power at 3.3V.

The low-voltage section consists of a fully-integrated DC/DC converter and an LDO running off the intermediate rail. The low-voltage DC/DC converter provides 1.1V while the LDO produces 1.8V. In addition, an integrated watchdog timer guards against runaway code.

To simplify device control, a single START control pin initiates the start-up sequence, while the WAKE pin controls operation of the watchdog (see [Table 1](#)).

Table 1. Device State

START	WAKE	DEVICE STATE						NOTES
		Watchdog	LDO1	HV BUCK	LDO2	LV BUCK	PGATE	
0	0	Off	On	Off	Off	Off	Off	
0	1	On*	On	Off	Off	Off	Off	
1	0	On*	On	On	On	On	On	A fault on the HV buck will cause LDO2, LV buck and PGATE to be disabled until the HV buck recovers.
1	1	On*	On	On	On	On	On	

*Unless the resistor on RT has the value 110kΩ or 150kΩ.

High-Voltage Buck Converter

The high-voltage buck converter regulates the battery input voltage to 3.3V. It is enabled when START is high according to the sequence shown in [Figure 1](#). When START is low, an internal 175Ω pulldown resistor is connected to V5.

The converter is current-mode and requires an external Schottky diode from LX to power ground. The converter can supply up to 2.1A (assuming a 0.3 LIR factor), subject to overall chip power dissipation, which may not exceed 1250mW at an ambient temperature of 105°C. The high-voltage buck converter also supplies the voltage-section of the MAX16926. Therefore, low-voltage buck and LDO2 current supply must be subtracted from the high-voltage buck maximum output current in order to obtain the high-voltage buck maximum output current available for the external system. The switching frequency of the converter is set by the resistor on the RT pin according to [Table 2](#).

The PGB open-drain output goes low whenever the V5 output is out of regulation. A pullup resistor is needed from PGB to a 3.3V or 5V supply.

The high-voltage buck incorporates a hiccup mode to protect the external power components when there is an output short circuit. If the high-voltage buck is below regulation (25% below if $V_{BATT} < 24V$, 10% below if $V_{BATT} > 24V$) and there are four consecutive current-limit events, switching is stopped. There is then a waiting period of 3.4ms before the device tries to restart by initiating a soft-start.

Switching Frequency Setting

Table 2. Switching Frequency Solution

RT PIN RESISTOR	RT PIN RESISTOR	LV BUCK SWITCHING FREQUENCY	WATCHDOG
10kΩ ±1%	400kHz	2.0MHz	Enabled
30kΩ ±1%	440kHz	2.2MHz	Enabled
56kΩ ±1%	2MHz	2MHz	Enabled
82kΩ ±1%	2.2MHz	2.2MHz	Enabled

Table 2. Switching Frequency Solution (continued)

RT PIN RESISTOR	RT PIN RESISTOR	LV BUCK SWITCHING FREQUENCY	WATCHDOG
110kΩ ±1%	400kHz	2.0MHz	Disabled
150kΩ ±1%	2.2MHz	2.2MHz	Disabled

High-Voltage Linear Regulator

The high-voltage linear regulator produces a 3.3V output from the voltage supplied at BATT. The output current from LDO1 is limited to 100mA but is also subject to limitation by the overall chip power dissipation. PG1 is the power-good output from LDO1 which asserts high 2ms after the output voltage is in regulation.

A pullup resistor is needed from PG1 to a 3.3V or 5V supply.

Low-Voltage Buck Converter

The low-voltage buck converter regulates the voltage at V33 to 1.1V. This converter is enabled when START is high according to the sequence shown in Figure 1. When START is low, an internal 175Ω pull down resistor is connected to V33. The low-voltage converter operates at a switching frequency of 2MHz or 2.2MHz.

The converter is current-mode and can supply up to 1.6A (assuming a 0.3 LIR factor), subject to overall chip power dissipation, which must not exceed 1250mW at an ambient temperature of 105°C

Low-Voltage Linear Regulator

The low-voltage linear regulator produces a regulated output from the 3.3V on V5. The output voltage is 1.8V. The output current from LDO2 is limited to 175mA.

Watchdog

The MAX16926 incorporates a watchdog timer that resets the local MCU powered by the LDO1 output if the WDI input is not pulsed periodically, thus detecting runaway code. The watchdog is active when one or both of the WAKE and START inputs is high (assuming that the timer is not disabled by the RT resistor value). When the watchdog is active, a rising edge on WDI causes it to reset. Therefore, to avoid watchdog timeout, the WDI input must be pulsed high periodically. If a pulse on WDI is missing for more than 1600ms (typ), the PG1 output goes low for 100ms to reset the MCU. The PG1 output also goes low if the LDO1 output is out of regulation.

PGATE Output

The PGATE open-drain low-side driver can be used to drive an external pMOSFET that switches the battery voltage to an external backlight power supply or other load. This helps reduce backlight standby current and disables the backlight when a backlight fault occurs (for which the FIN pin is used). If FIN is taken low, the PGATE output stops sinking current and the external pMOSFET is turned off.

Connect a resistor from the PGATE output to the source of the pMOSFET, with the gate of the pMOSFET connected to PGATE. Calculate the resistor value using the following equation:

$$R_{PGATE} = \frac{V_t}{115\mu A}$$

where V_t is the minimum value of the pMOSFET gate threshold voltage. Choose an R_{PGATE} value larger than the value calculated using this equation. If the battery voltage exceeds 20V, it may be necessary to add an 18V zener diode across the gate-source of the external pMOSFET to avoid damage to the gate.

START Input and Sequencing

When WAKE and START are low, the MAX16926 is in low-current mode with only the LDO1 output active. When WAKE goes high, the watchdog is enabled unless the RT resistor is 110kΩ or 150kΩ.

When START is taken high, the device activates the internal bias circuitry and logic. At this time, the high-voltage buck

converter is turned on. When V5 reaches its power-good level, the PGATE output, the low-voltage buck converter, and low-voltage LDO are turned on. When all outputs reach their power-good levels (the PGATE output is not monitored), the PGOOD output goes high to signal the successful end of the sequence.

If either of the outputs V33 or LDO2 do not reach their power-good level during start-up, the PGOOD output stays low, but the outputs remain active unless START is taken low.

If V5 goes below its power-good level during normal operation, V33 and LDO2 are disabled until V5 returns to a level above its power-good threshold. During this time PGOOD is low.

Sequence

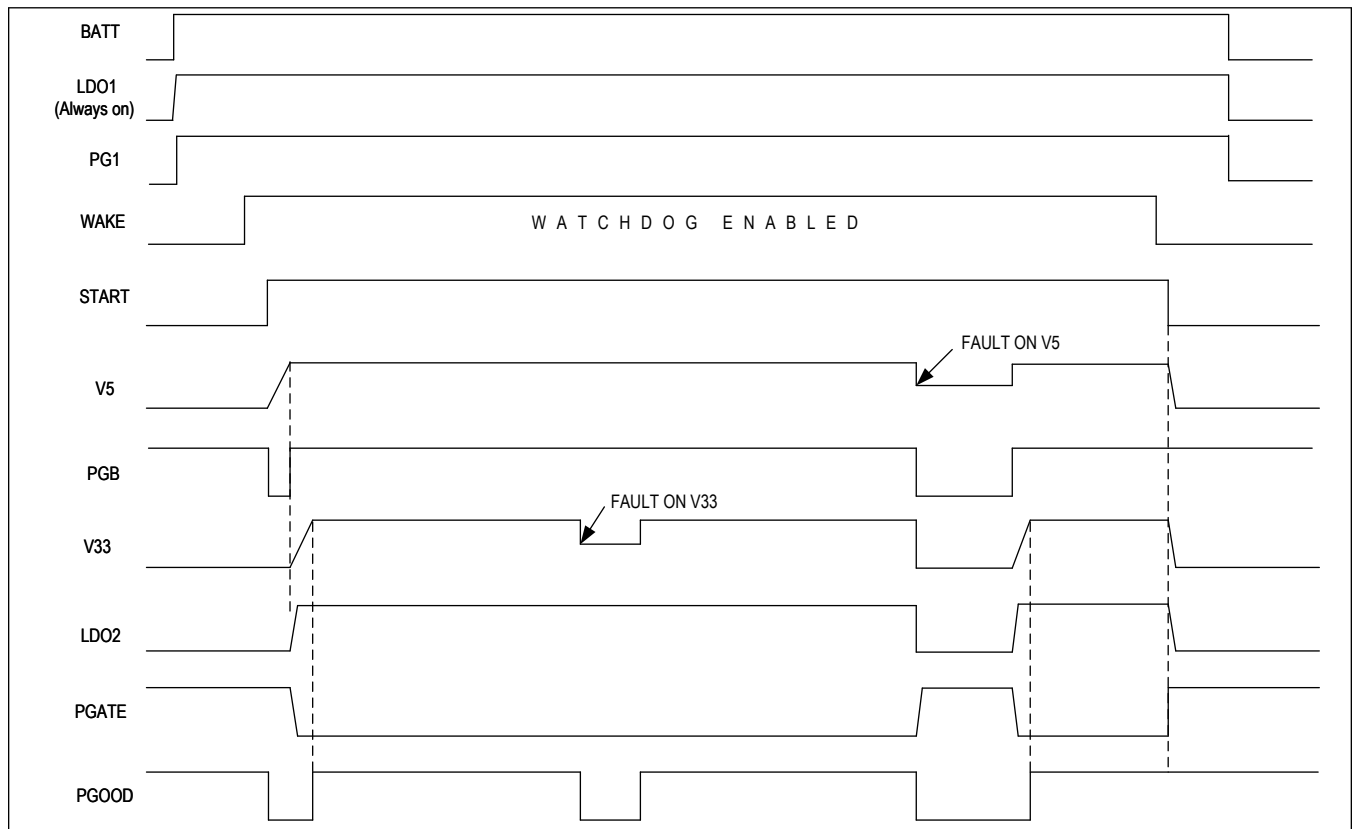


Figure 1. MAX16926 Sequence

Applications Information

High-Voltage Buck External Component Selection

Three key inductor parameters must be specified for operation with the devices: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). To select the inductor value, the ratio of inductor peak-to-peak AC current to DC average current (L_{IR}) must be selected first. A good compromise between size and loss is a 30% peak-to-peak ripple current to average-current ratio ($L_{IR} = 0.3$). The switching frequency, input voltage, output voltage, and selected L_{IR} then determine the inductor value as follows:

$$L = (V_{BATT} - V_{V5}) \times V_{V5} / (V_{BATT} \times F_{SW} \times I_{OUTV5} \times L_{IR})$$

where F_{SW} is the switching frequency of the high-voltage buck selected with the RT resistor, and I_{OUTV5} is the total high-voltage output current which is composed by:

$$I_{OUTV5} = (I_{OUTV3} \times V_{V3}/V_{V5})/\eta_{LV} + I_{LDO2} + I_{V5_EXT_SYS}$$

where I_{OUTV3} is the low-voltage buck output current, I_{LDO2} is the LDO2 output current, $I_{V5_EXT_SYS}$ is the high-voltage buck output current required by the system and η_{LV} is the efficiency of the low-voltage buck (see [Typical Operating Characteristics](#)).

Make sure that inductor peak current is below the high-voltage buck minimum current-limit value (2.4A).

$$I_{L_PEAK} = I_{OUTV5} \times (1 + L_{IR}/2)$$

The inductor saturation current must be higher than the high-voltage maximum current-limit value (4A) and a low inductor DC resistance will improve efficiency.

In order to minimize output voltage ripple and guarantee stability, always use a total of 44 μ F output capacitance when 2MHz switching frequency is selected and 66 μ F output capacitance when 400kHz switching frequency is selected.

Low-Voltage Buck External Component Selection

Three key inductor parameters must be specified for operation with the devices: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). To select the inductor value, the ratio of inductor peak-to-peak AC current to DC average current (L_{IR}) must be selected first. A good compromise between size and loss is a 30% peak-to-peak ripple current to average-current ratio ($L_{IR} = 0.3$). The switching frequency, input voltage, output voltage, and selected L_{IR} then determine the inductor value as follows:

$$L = (V_{V5} - V_{V3}) \times V_{V3} / (V_{V5} \times F_{SW} \times I_{OUTV3} \times L_{IR})$$

where F_{SW} is the switching frequency of the low-voltage buck selected with the RT resistor, and I_{OUTV3} is the total low-voltage output current.

Make sure that inductor peak current is below the low-voltage buck minimum current-limit value (1.8A).

$$I_{L_PEAK} = I_{OUTV3} \times (1 + L_{IR}/2)$$

The inductor saturation current must be higher than the low-voltage maximum current-limit value (3.7A) and a low inductor DC resistance will improve efficiency.

In order to minimize output voltage ripple and guarantee stability, always use a total of 22 μ F output capacitance.

Layout Considerations

Proper PCB layout is a critical consideration in achieving low switching losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity and power dissipation. Follow these guidelines for good PCB layout:

1. Use a large, contiguous copper plane under the device package. Ensure that all heat-dissipating components have adequate cooling. The bottom pad of the device must be soldered down to this copper plane to assure effective heat dissipation and to derive full power from the devices. Use multiple vias or a single large via in this plane for heat dissipation.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/20	Initial release	—

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