FEATURES

- 50Mmps Update Rate
- Pin Compatible 12-Bit, 14-Bit and 16-Bit Devices
- High Spectral Purity: 87dB SFDR at 1MHz f_{OUT}
- 5pV-s Glitch Impulse
- Differential Current Outputs
- 20ns Settling Time
- Low Power: 180mW from ±5V Supplies
- TTL/CMOS (3.3V or 5V) Inputs
- Small Package: 28-Pin SSOP

APPLICATIONS

- Cellular Base Stations
- Multicarrier Base Stations
- Wireless Communication
- Direct Digital Synthesis (DDS)
- xDSL Modems
- Arbitrary Waveform Generation
- Automated Test Equipment
- Instrumentation

DESCRIPTION

The LTC®1666/LTC1667/LTC1668 are 12-/14-/16-bit, 50Mmps differential current output DACs implemented on a high performance BiCMOS process with laser trimmed, thin-film resistors. The combination of a novel current-steering architecture and a high performance process produces DACs with exceptional AC and DC performance. The LTC1668 is the first 16-bit DAC in the marketplace to exhibit an SFDR (spurious free dynamic range) of 87dB for an output signal frequency of 1MHz.

Operating from ±5V supplies, the LTC1666/LTC1667/ LTC1668 can be configured to provide full-scale output currents up to 10mA. The differential current outputs of the DACs allow single-ended or true differential operation. The –1V to 1V output compliance of the LTC1666/ LTC1667/LTC1668 allows the outputs to be connected directly to external resistors to produce a differential output voltage without degrading the converter’s linearity. Alternatively, the outputs can be connected to the summing junction of a high speed operational amplifier, or to a transformer.

The LTC1666/LTC1667/LTC1668 are pin compatible and are available in a 28-pin SSOP and are fully specified over the industrial temperature range.

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TYPICAL APPLICATION

LTC1668, 16-Bit, 50Mmps DAC

![Diagram of LTC1668, 16-Bit, 50Mmps DAC](image-url)

LTC1668 SFDR vs f_{OUT} and f_{CLOCK}

![Graph of LTC1668 SFDR vs f_{OUT} and f_{CLOCK}](image-url)
**ABSOLUTE MAXIMUM RATINGS**

(Note 1)

Supply Voltage (V\_DD) ................................................  6V
Negative Supply Voltage (V\_SS) .............................. –6V
Total Supply Voltage (V\_DD to V\_SS) .......................  12V
Digital Input Voltage .................... –0.3V to (V\_DD + 0.3V)
Analog Output Voltage  
(I\_OUT\_A and I\_OUT\_B) ........  (V\_SS – 0.3V) to (V\_DD + 0.3V)

Power Dissipation .............................................  500mW
Operating Temperature Range
LTC1666C/LTC1667C/LTC1668C ...........  0°C to 70°C
LTC1666I/LTC1667I/LTC1668I ..........  –40°C to 85°C
Storage Temperature Range ................  –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..............  300°C

**PACKAGE/ORDER INFORMATION**

Consult LTC Marketing for parts specified with wider operating temperature ranges.
The LTC1666/LTC1667/LTC1668 are precision 16-bit, 25 Msps 1.8V CMOS ADCs with an internal or external reference. They feature a low 28 mA supply current and operate from a single 5 V supply. The LTC1666/LTC1667/LTC1668 have a fully differential input architecture, ensuring balanced single-ended operation up to ±4 Vpp while rejecting common-mode voltages up to ±5 V. The devices operate from a +5 V power supply and do not need a bypass capacitor. The LTC1666/LTC1667/LTC1668 use a low noise, high speed 1.8 V bandgap reference for excellent performance. The on-chip reference to VREF = 2.5 V is used with an external reference with 1% accuracy. High accuracy is also provided when using a BLMEL005 or BLMEL006 silicon-carbide voltage reference. For external ringing rejection, the REF- and REF+ inputs are differentially input. The LTC1666/LTC1667/LTC1668 are available in a 44-lead TSSOP package.

### ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at \( T_A = 25^\circ C \). \( V_{DD} = 5 \) V, \( V_{SS} = -5 \) V, \( LADCOM = AGND = DGND = 0 \) V, \( I_{OUTFS} = 10 \) mA.

#### SYMBOL | PARAMETER | CONDITIONS | LTC1666 | LTC1667 | LTC1668 | UNITS
--- | --- | --- | --- | --- | --- | ---
\( 1 \) | Resolution | ● | 12 | 14 | 16 | Bits
\( 1 \) | Monotonicity | | 12 | 14 | 14 | Bits
\( 1 \) | INL Integral Nonlinearity (Note 2) | | ±2 | ±2 | ±8 | LSB
\( 1 \) | DNL Differential Nonlinearity (Note 2) | | ±1 | ±1 | ±4 | LSB
\( 1 \) | Offset Error | | 0.1 ±0.2 | 0.1 ±0.2 | 0.1 ±0.2 | % FSR
\( 1 \) | Offset Error Drift | | 5 | 5 | 5 | ppm/°C
\( 1 \) | GE Gain Error Internal Reference, \( R_{REFIN} = 2k \) External Reference, \( V_{REF} = 2.5V, R_{REFIN} = 2k \) | | 2 | 2 | 2 | % FSR
\( 1 \) | Gain Error Drift Internal Reference External Reference | | 50 | 50 | 50 | ppm/°C
\( 1 \) | PSRR Power Supply Rejection Ratio \( V_{DD} = 5\text{V} \pm 5\% \) \( V_{SS} = -5\text{V} \pm 5\% \) | | ±0.1 | ±0.1 | ±0.1 | % FSR/V
\( 1 \) | AC Linearity | SFDR Spurious Free Dynamic Range to Nyquist | \( f_{CLK} = 25\text{Msps}, f_{OUT} = 1\text{MHz} \) 0dB FS Output 6dB FS Output 12dB FS Output | 76 | 78 | 78 | dB
\( 1 \) | SFDR Spurious Free Dynamic Range Within a Window | \( f_{CLK} = 25\text{Msps}, f_{OUT} = 1\text{MHz} \) \( f_{CLK} = 50\text{Msps}, f_{OUT} = 1\text{MHz} \) \( f_{CLK} = 50\text{Msps}, f_{OUT} = 5\text{MHz} \) \( f_{CLK} = 50\text{Msps}, f_{OUT} = 20\text{MHz} \) | 85 | 85 | 79 | dB
\( 1 \) | THD Total Harmonic Distortion | \( f_{CLK} = 25\text{Msps}, f_{OUT} = 1\text{MHz} \) \( f_{CLK} = 50\text{Msps}, f_{OUT} = 5\text{MHz} \) | -75 | -77 | -84 | dB

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The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ C$. $V_{DD} = 5V$, $V_{SS} = -5V$, LADCOM = AGND = DGND = 0V, $I_{OUTFS} = 10mA$.

### Analog Output

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>LTC1666/LTC1667/LTC1668</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{OUTFS}$</td>
<td>Full-Scale Output Current</td>
<td>● 1 10 mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Output Compliance Range</td>
<td>$I_S = 10mA$</td>
<td>● -1 1 V</td>
</tr>
<tr>
<td></td>
<td>Output Resistance; $R_{OUTA}$, $R_{OUTB}$</td>
<td>$I_{OUTA,B}$ to LADCOM</td>
<td>● 0.7 1.1 1.5 kΩ</td>
</tr>
<tr>
<td></td>
<td>Output Capacitance</td>
<td></td>
<td>5 pF</td>
</tr>
</tbody>
</table>

### Reference Output

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>LTC1666/LTC1667/LTC1668</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Reference Voltage</td>
<td>REFOUT Tied to $I_{REFIN}$ Through 2kΩ</td>
<td>2.475 2.5 2.525 V</td>
</tr>
<tr>
<td></td>
<td>Reference Output Drift</td>
<td></td>
<td>25 ppm/^\circ C</td>
</tr>
<tr>
<td></td>
<td>Reference Output Load Regulation</td>
<td>$I_{LOAD} = 0mA$ to $5mA$</td>
<td>6 mV/mA</td>
</tr>
</tbody>
</table>

### Reference Input

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>LTC1666/LTC1667/LTC1668</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Reference Small-Signal Bandwidth</td>
<td>$I_S = 10mA$, $C_{COMP1} = 0.1\mu F$</td>
<td>20 kHz</td>
</tr>
</tbody>
</table>

### Power Supply

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>LTC1666/LTC1667/LTC1668</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$</td>
<td>Positive Supply Voltage</td>
<td>● 4.75 5 5.25 V</td>
<td></td>
</tr>
<tr>
<td>$V_{SS}$</td>
<td>Negative Supply Voltage</td>
<td>● -4.75 -5 -5.25 V</td>
<td></td>
</tr>
<tr>
<td>$I_{DD}$</td>
<td>Positive Supply Current</td>
<td>$I_S = 10mA$, $f_{CLK} = 25$Msp, $f_{OUT} = 1MHz$</td>
<td>● 3 5 mA</td>
</tr>
<tr>
<td>$I_{SS}$</td>
<td>Negative Supply Current</td>
<td>$I_S = 10mA$, $f_{CLK} = 25$Msp, $f_{OUT} = 1MHz$</td>
<td>● 33 40 mA</td>
</tr>
<tr>
<td>$P_{DIS}$</td>
<td>Power Dissipation</td>
<td>$I_S = 10mA$, $f_{CLK} = 25$Msp, $f_{OUT} = 1MHz$</td>
<td>180 mW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_S = 1mA$, $f_{CLK} = 25$Msp, $f_{OUT} = 1MHz$</td>
<td>85 mW</td>
</tr>
</tbody>
</table>

### Dynamic Performance (Differential Transformer Coupled Output, 50Ω Double Terminated, Unless Otherwise Noted)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>LTC1666/LTC1667/LTC1668</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{CLOCK}$</td>
<td>Maximum Update Rate</td>
<td>● 50 75 Msp</td>
<td></td>
</tr>
<tr>
<td>$t_S$</td>
<td>Output Settling Time</td>
<td>To 0.1% FSR</td>
<td>20 ns</td>
</tr>
<tr>
<td>$t_{PD}$</td>
<td>Output Propagation Delay</td>
<td></td>
<td>8 ns</td>
</tr>
<tr>
<td></td>
<td>Glitch Impulse</td>
<td>Single Ended Difference</td>
<td>15 5 pV-s</td>
</tr>
<tr>
<td>$t_r$</td>
<td>Output Rise Time</td>
<td></td>
<td>4 ns</td>
</tr>
<tr>
<td>$t_f$</td>
<td>Output Fall Time</td>
<td></td>
<td>4 ns</td>
</tr>
<tr>
<td>$I_{NO}$</td>
<td>Output Noise</td>
<td></td>
<td>50 pA/\sqrt{Hz}</td>
</tr>
</tbody>
</table>

### Digital Inputs

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>LTC1666/LTC1667/LTC1668</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>Digital High Input Voltage</td>
<td>● 2.4 V</td>
<td></td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Digital Low Input Voltage</td>
<td>● 0.8 V</td>
<td></td>
</tr>
<tr>
<td>$I_{IN}$</td>
<td>Digital Input Current</td>
<td>● ±10 µA</td>
<td></td>
</tr>
<tr>
<td>$C_{IN}$</td>
<td>Digital Input Capacitance</td>
<td></td>
<td>5 pF</td>
</tr>
<tr>
<td>$t_{DS}$</td>
<td>Input Setup Time</td>
<td>● 8 ns</td>
<td></td>
</tr>
<tr>
<td>$t_{DH}$</td>
<td>Input Hold Time</td>
<td>● 4 ns</td>
<td></td>
</tr>
<tr>
<td>$t_{CLKH}$</td>
<td>Clock High Time</td>
<td>● 5 ns</td>
<td></td>
</tr>
<tr>
<td>$t_{CLKL}$</td>
<td>Clock Low Time</td>
<td>● 8 ns</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: For the LTC1666, ±1LSB = ±0.024% of full scale; for the LTC1667, ±1LSB = ±0.006% of full scale = ±61ppm of full scale; for the LTC1668, ±1LSB = ±0.0015% of full scale = ±15.3ppm of full scale.
TYPICAL PERFORMANCE CHARACTERISTICS (LTC1668)

Single Tone SFDR at 50MSPS

2-Tone SFDR

4-Tone SFDR, $f_{\text{CLOCK}} = 50$MSPS

4-Tone SFDR, $f_{\text{CLOCK}} = 5$MSPS

SFDR vs $f_{\text{OUT}}$ and Digital Amplitude (dBFS) at $f_{\text{CLOCK}} = 50$MSPS

SFDR vs $f_{\text{OUT}}$ and Digital Amplitude (dBFS) at $f_{\text{CLOCK}} = 25$MSPS

SFDR vs $f_{\text{OUT}}$ and Digital Amplitude (dBFS) at $f_{\text{CLOCK}} = 5$MSPS

SFDR vs $f_{\text{OUT}}$ and I$_{\text{OUTFS}}$ at $f_{\text{CLOCK}} = 25$MSPS

SFDR vs $f_{\text{OUT}}$ and I$_{\text{OUTFS}}$ at $f_{\text{CLOCK}} = 50$MSPS

SFDR vs $f_{\text{OUT}}$ and Digital Amplitude (dBFS) at $f_{\text{CLOCK}} = 5$MSPS
TYPICAL PERFORMANCE CHARACTERISTICS

SFDR vs Digital Amplitude (dBFS) and \( f_{\text{CLOCK}} \) at \( f_{\text{OUT}} = f_{\text{CLOCK}}/11 \)

SFDR vs Digital Amplitude (dBFS) and \( f_{\text{CLOCK}} \) at \( f_{\text{OUT}} = f_{\text{CLOCK}}/5 \)

Single-Ended Outputs Full-Scale Transition

Differential Output Full-Scale Transition

Single-Ended Midscale Glitch Impulse

Differential Midscale Glitch Impulse

Integral Nonlinearity

Digital Input Code

INTEGRAL NONLINEARITY (LSB)
TYPICAL PERFORMANCE CHARACTERISTICS (LTC1668)

**PIN FUNCTIONS**

**LTC1666**

REFOUT (Pin 15): Internal Reference Voltage Output. Nominal value is 2.5V. Requires a 0.1µF bypass capacitor to AGND.

IREFIN (Pin 16): Reference Input Current. Nominal value is 1.25mA for IFS = 10mA. IFS = IREFIN * 8.

AGND (Pin 17): Analog Ground.

LADCOM (Pin 18): Attenuator Ladder Common. Normally tied to GND.

IOUTB (Pin 19): Complementary DAC Output Current. Full-scale output current occurs when all data bits are 0s.

IOUTA (Pin 20): DAC Output Current. Full-scale output current occurs when all data bits are 1s.

COMP1 (Pin 21): Current Source Control Amplifier Compensation. Bypass to VSS with 0.1µF.

COMP2 (Pin 22): Internal Bypass Point. Bypass to VSS with 0.1µF.

VSS (Pin 23): Negative Supply Voltage. Nominal value is –5V.

DGND (Pin 24): Digital Ground.

VDD (Pin 25): Positive Supply Voltage. Nominal value is 5V.

CLK (Pin 26): Clock Input. Data is latched and the output is updated on positive edge of clock.

DB11 to DB0 (Pins 27, 28, 1 to 10): Digital Input Data Bits.
**PIN FUNCTIONS**

**LTC1667**

**REFOUT (Pin 15):** Internal Reference Voltage Output. Nominal value is 2.5V. Requires a 0.1µF bypass capacitor to AGND.

**IREFIN (Pin 16):** Reference Input Current. Nominal value is 1.25mA for IFS = 10mA. IFS = IREFIN • 8.

**AGND (Pin 17):** Analog Ground.

**LADCOM (Pin 18):** Attenuator Ladder Common. Normally tied to GND.

**IOUT B (Pin 19):** Complementary DAC Output Current. Full-scale output current occurs when all data bits are 0s.

**IOUT A (Pin 20):** DAC Output Current. Full-scale output current occurs when all data bits are 1s.

**COMP1 (Pin 21):** Current Source Control Amplifier Compensation. Bypass to VSS with 0.1µF.

**COMP2 (Pin 22):** Internal Bypass Point. Bypass to VSS with 0.1µF.

**VSS (Pin 23):** Negative Supply Voltage. Nominal value is -5V.

**DGND (Pin 24):** Digital Ground.

**VDD (Pin 25):** Positive Supply Voltage. Nominal value is 5V.

**CLK (Pin 26):** Clock Input. Data is latched and the output is updated on positive edge of clock.

**DB13 to DB0 (Pins 27, 28, 1 to 12):** Digital Input Data Bits.

**LTC1668**

**REFOUT (Pin 15):** Internal Reference Voltage Output. Nominal value is 2.5V. Requires a 0.1µF bypass capacitor to AGND.

**IREFIN (Pin 16):** Reference Input Current. Nominal value is 1.25mA for IFS = 10mA. IFS = IREFIN • 8.

**AGND (Pin 17):** Analog Ground.

**LADCOM (Pin 18):** Attenuator Ladder Common. Normally tied to GND.

**IOUT B (Pin 19):** Complementary DAC Output Current. Full-scale output current occurs when all data bits are 0s.

**IOUT A (Pin 20):** DAC Output Current. Full-scale output current occurs when all data bits are 1s.

**COMP1 (Pin 21):** Current Source Control Amplifier Compensation. Bypass to VSS with 0.1µF.

**COMP2 (Pin 22):** Internal Bypass Point. Bypass to VSS with 0.1µF.

**VSS (Pin 23):** Negative Supply Voltage. Nominal value is -5V.

**DGND (Pin 24):** Digital Ground.

**VDD (Pin 25):** Positive Supply Voltage. Nominal value is 5V.

**CLK (Pin 26):** Clock Input. Data is latched and the output is updated on positive edge of clock.

**DB15 to DB0 (Pins 27, 28, 1 to 14):** Digital Input Data Bits.
**LTC1666/LTC1667/LTC1668**

**BLOCK DIAGRAM**

![Block Diagram](image)

**TIMING DIAGRAM**

![Timing Diagram](image)

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Theory of Operation

The LTC1666/LTC1667/LTC1668 are high speed current steering 12-/14-/16-bit DACs made on an advanced BiCMOS process. Precision thin film resistors and well matched bipolar transistors result in excellent DC linearity and stability. A low glitch current switching design gives excellent AC performance at sample rates up to 50Msps. The devices are complete with a 2.5V internal bandgap reference and edge triggered latches, and set a new standard for DAC applications requiring very high dynamic range at output frequencies up to several megahertz.

Referring to the Block Diagrams, the DACs contain an array of current sources that are steered to IOUTA or IOUTB with NMOS differential current switches. The four most significant bits are made up of 15 current segments of equal weight. The remaining lower bits are binary weighted, using a combination of current scaling and a differential resistive attenuator ladder. All bits and segments are precisely matched, both in current weight for DC linearity, and in switch timing for low glitch impulse and low spurious tone AC performance.

Setting the Full-Scale Current, IOUTFS

The full-scale DAC output current, IOUTFS, is nominally 10mA, and can be adjusted down to 1mA. Placing a resistor, RSET, between the REFOUT pin, and the IREFIN pin sets IOUTFS as follows.

The internal reference control loop amplifier maintains a virtual ground at IREFIN by servoing the internal current source, IINT, to sink the exact current flowing into IREFIN. IINT is a scaled replica of the DAC current sources and

\[ I_{OUTFS} = 8 \times \left( \frac{V_{REF}}{R_{SET}} \right) \]

For example, if RSET = 2k and is tied to VREF = REFOUT = 2.5V, IREFIN = 2.5/2k = 1.25mA and IOUTFS = 8 \times (1.25mA) = 10mA.

The reference control loop requires a capacitor on the COMP1 pin for compensation. For optimal AC performance, CCOMP1 should be connected to VSS and be placed very close to the package (less than 0.1")

For fixed reference voltage applications, CCOMP1 should be 0.1µF or more. The reference control loop small-signal bandwidth is approximately \( \frac{1}{(2\pi) \times C_{COMP1} \times 80} \) or 20kHz for CCOMP1 = 0.1µF.

Reference Operation

The onboard 2.5V bandgap voltage reference drives the REFOUT pin. It is trimmed and specified to drive a 2k resistor tied from REFOUT to IREFIN, corresponding to a 1.25mA load (IOUTFS = 10mA). REFOUT has nominal output impedance of 6Ω, or 0.24% per mA, so it must be buffered to drive any additional external load. A 0.1µF capacitor is required on the REFOUT pin for compensation. Note that this capacitor is required for stability, even if the internal reference is not being used.

External Reference Operation

Figure 1, shows how to use an external reference to control the LTC1666/LTC1667/LTC1668 full-scale current.
The LTC1666/LTC1667/LTC1668 use straight binary digital coding. The complementary current outputs, \( I_{OUTA} \) and \( I_{OUTB} \), sink current from 0 mA to \( I_{OUTFS} \). For \( I_{OUTFS} = 10 \text{mA} \) (nominal), \( I_{OUTA} \) swings from 0 mA when all bits are low (e.g., Code = 0) to 10 mA when all bits are high (e.g., Code = 65535 for LTC1668) (decimal representation). \( I_{OUTB} \) is complementary to \( I_{OUTA} \). \( I_{OUTA} \) and \( I_{OUTB} \) are given by the following formulas:

**LTC1666:**
\[
I_{OUTA} = I_{OUTFS} \cdot \frac{\text{DAC Code}}{4096} \quad (2)
\]
\[
I_{OUTB} = I_{OUTFS} \cdot \frac{4095 - \text{DAC Code}}{4096} \quad (3)
\]

**LTC1667:**
\[
I_{OUTA} = I_{OUTFS} \cdot \frac{\text{DAC Code}}{16384} \quad (4)
\]
\[
I_{OUTB} = I_{OUTFS} \cdot \frac{16383 - \text{DAC Code}}{16384} \quad (5)
\]

**LTC1668:**
\[
I_{OUTA} = I_{OUTFS} \cdot \frac{\text{DAC Code}}{65536} \quad (6)
\]
\[
I_{OUTB} = I_{OUTFS} \cdot \frac{65535 - \text{DAC Code}}{65536} \quad (7)
\]

In typical applications, the LTC1666/LTC1667/LTC1668 differential output currents either drive a resistive load directly or drive an equivalent resistive load through a transformer, or as the feedback resistor of an I-to-V converter. The voltage outputs generated by the \( I_{OUTA} \) and \( I_{OUTB} \) output currents are then:

\[
V_{OUTA} = I_{OUTA} \cdot R_{LOAD} \quad (8)
\]
\[
V_{OUTB} = I_{OUTB} \cdot R_{LOAD} \quad (9)
\]

The differential voltage is:

\[
V_{DIFF} = V_{OUTA} - V_{OUTB} = (I_{OUTA} - I_{OUTB}) \cdot R_{LOAD} \quad (10)
\]

Substituting the values found earlier for \( I_{OUTA} \), \( I_{OUTB} \) and \( I_{OUTFS} \) (LTC1668):

\[
V_{DIFF} = \left(2 \cdot \text{DAC Code} - 65535\right) \cdot 8 \cdot \left(R_{LOAD} / R_{SET}\right) \cdot (V_{REF}) \quad (11)
\]

From these equations some of the advantages of differential-mode operation can be seen. First, any common-mode noise or error on \( I_{OUTA} \) and \( I_{OUTB} \) is cancelled. Second, the signal power is twice as large as in the single-ended case. Third, any errors and noise that multiply times \( I_{OUTA} \) and \( I_{OUTB} \), such as reference or \( I_{OUTFS} \) noise, cancel near midscale, where AC signal waveforms tend to spend the most time. Fourth, this transfer function is bipolar; e.g. the output swings positive and negative around a zero output at mid-scale input, which is more convenient for AC applications.

Note that the term \( R_{LOAD} / R_{SET} \) appears in both the differential and single-ended transfer functions. This means that the Gain Error of the DAC depends on the ratio of \( R_{LOAD} \) to \( R_{SET} \), and the Gain Error tempco is affected by the temperature tracking of \( R_{LOAD} \) with \( R_{SET} \). Note also that the absolute tempco of \( R_{LOAD} \) is very critical for DC nonlinearity. As the DAC output changes from 0 mA to 10 mA the \( R_{LOAD} \) resistor will heat up slightly, and even a very low tempco can produce enough INL bowing to be significant at the 16-bit level. This effect disappears with medium to high frequency AC signals due to the slow thermal time constant of the load resistor.

**Analog Outputs**

The LTC1666/LTC1667/LTC1668 have two complementary current outputs, \( I_{OUTA} \) and \( I_{OUTB} \) (see DAC Transfer Function). The output impedance of \( I_{OUTA} \) and \( I_{OUTB} \) is typically 1.1 k\( \Omega \) to LADCOM. (See Figure 3.)
LADCOM

The LADCOM pin is the common connection for the internal DAC attenuator ladder. It usually is tied to analog ground, but more generally it should connect to the same potential as the load resistors on IOUT A and IOUT B. The LADCOM pin carries a constant current to VSS of approximately 0.32 \* (IOUTFS), plus any current that flows from IOUT A and IOUT B through the RIOUT A and RIOUT B resistors.

Output Compliance

The specified output compliance voltage range is ±1V. The DC linearity specifications, INL and DNL, are trimmed and guaranteed on IOUT A into the virtual ground of an I-to-V converter, but are typically very good over the full output compliance range. Above 1V the output current will start to increase as the DAC current steering switch impedance decreases, degrading both DC and AC linearity. Below −1V, the DAC switches will start to approach the transition from saturation to linear region. This will degrade AC performance first, due to nonlinear capacitance and increased glitch impulse. AC distortion performance is optimal at amplitudes less than ±0.5VP-P on IOUT A and IOUT B due to nonlinear capacitance and other large-signal effects. At first glance, it may seem counter-intuitive to decrease the signal amplitude when trying to optimize SFDR. However, the error sources that affect AC performance generally behave as additive currents, so decreasing the load impedance to reduce signal voltage amplitude will reduce most spurious signals by the same amount.
Operating with Reduced Output Currents

The LTC1666/LTC1667/LTC1668 are specified to operate with full-scale output current, $I_{OUTFS}$, from the nominal 10mA down to 1mA. This can be useful to reduce power dissipation or to adjust full-scale value. However, the DC and AC accuracy is specified only at $I_{OUTFS} = 10mA$, and DC and AC accuracy will fall off significantly at lower $I_{OUTFS}$ values. At $I_{OUTFS} = 1mA$, the LTC1668 INL and DNL typically degrade to the 14-bit to 13-bit level, compared to 16-bit to 15-bit typical accuracy at 10mA $I_{OUTFS}$. Increasing $I_{OUTFS}$ from 1mA, the accuracy improves rapidly, roughly in proportion to $1/I_{OUTFS}$. Note that the AC performance (SFDR) is affected much more by reduced $I_{OUTFS}$ than it is by reduced digital amplitude (see Typical Performance Characteristics). Therefore it is usually better to make large gain adjustments digitally, keeping $I_{OUTFS}$ equal to 10mA.

Output Configurations

Based on the specific application requirements, the LTC1666/LTC1667/LTC1668 allow a choice of the best of several output configurations. Voltage outputs can be generated by external load resistors, transformer coupling or with an op amp I-to-V converter. Single-ended DAC output configurations use only one of the outputs, preferably $I_{OUTA}$, to produce a single-ended voltage output. Differential mode configurations use the difference between $I_{OUTA}$ and $I_{OUTB}$ to generate an output voltage, $V_{DIFF}$, as shown in equation 11. Differential mode gives much better accuracy in most AC applications. Because the DAC chip is the point of interface between the digital input signals and the analog output, some small amount of noise coupling to $I_{OUTA}$ and $I_{OUTB}$ is unavoidable. Most of that digital noise is common mode and is canceled by the differential mode circuit. Other significant digital noise components can be modeled as $V_{REF}$ or $I_{OUTFS}$ noise. In single-ended mode, $I_{OUTFS}$ noise is gone at zero scale and is fully present at full scale. In differential mode, $I_{OUTFS}$ noise is cancelled at midscale input, corresponding to zero analog output. Many AC signals, including broadband and multitone communications signals with high peak to average ratios, stay mostly near midscale.

Differential Transformer-Coupled Outputs

Differential transformer-coupled output configurations usually give the best AC performance. An example is shown in Figure 5. The advantages of transformer coupling include excellent rejection of common mode distortion and noise over a broad frequency range and convenient differential-to-single-ended conversion with isolation or level shifting. Also, as much as twice the power can be delivered to the load, and impedance matching can be accomplished by selecting the appropriate transformer turns ratio. The center tap on the primary side of the transformer is tied to ground to provide the DC current path for $I_{OUTA}$ and $I_{OUTB}$. For low distortion, the DC average of the $I_{OUTA}$ and $I_{OUTB}$ currents must be exactly equal to avoid biasing the core. This is especially important for compact RF transformers with small cores. The circuit in Figure 5 uses a Mini-Circuits T1-1T RF transformer with a 1:1 turns ratio. The load resistance on $I_{OUTA}$ and $I_{OUTB}$ is equivalent to a single differential resistor of 50Ω, and the 1:1 turns ratio means the output impedance from the transformer is 50Ω. Note that the load resistors are optional, and they dissipate half of the output power. However, in lab environments or when driving long transmission lines it is very desirable to have a 50Ω output impedance. This could also be done with a 50Ω resistor at the transformer secondary, but putting the load resistors on $I_{OUTA}$ and $I_{OUTB}$ is preferred since it reduces the current through the transformer. At signal frequencies lower than about 1MHz, the transformer core size required to maintain low distortion gets larger, and at some lower frequencies this becomes impractical.

![Figure 5. Differential Transformer-Coupled Outputs](image-url)
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Resistor Loaded Outputs

A differential resistor loaded output configuration is shown in Figure 6. It is simple and economical, but it can drive only differential loads with impedance levels and amplitudes appropriate for the DAC outputs.

The recommended single-ended resistor loaded configuration is essentially the same circuit as the differential resistor loaded, case—simply use the IOUT_A output, referred to ground. Rather than tying the unused IOUT_B output to ground, it is preferred to load it with the equivalent RLOAD of IOUT_A. Then IOUT_B will still swing with a waveform complementary to IOUT_A.

Figure 6. Differential Resistor-Loaded Output

Op Amp I to V Converter Outputs

Adding an op amp differential to single-ended converter circuit to the differential resistor loaded output gives the circuit of Figure 7.

This circuit complements the capabilities of the transformer-coupled application at lower frequencies, since available op amps can deliver good AC distortion performance at signal frequencies of a few MHz down to DC. The optional capacitor adds a single real pole of filtering, and helps reduce distortion by limiting the high frequency signal amplitude at the op amp inputs. The circuit swings ±1V around ground.

Figure 7. Differential to Single-Ended Op Amp I-V Converter

Figure 8 shows a simplified circuit for a single-ended output using I-to-V converter to produce a unipolar buffered voltage output. This configuration typically has the best DC linearity performance, but its AC distortion at higher frequencies is limited by U1’s slewing capabilities.

Digital Interface

The LTC1666/LTC1667/LTC1668 have parallel inputs that are latched on the rising edge of the clock input. They accept CMOS levels from either 5V or 3.3V logic and can accept clock rates of up to 50MHz.

Referring to the Timing Diagram and Block Diagram, the data inputs go to master-slave latches that update on the rising edge of the clock. The input logic thresholds, VIH = 2.4V min, VIH = 0.8V max, work with 3.3V or 5V CMOS levels over temperature. The guaranteed setup time, tDS, is 8ns minimum and the hold time, tDH, is 4ns minimum. The minimum clock high and low times are guaranteed at 6ns and 8ns, respectively. These specifications allow the LTC1666/LTC1667/LTC1668 to be clocked at up to 50Mmps minimum.

For best AC performance, the data and clock waveforms need to be clean and free of undershoot and overshoot. Clock and data interconnect lines should be twisted pair, coax or microstrip, and proper line termination is important. If the digital input signals to the DAC are considered as analog AC voltage signals, they are rich in spectral components over a broad frequency range, usually in-
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Including the output signal band of interest. Therefore, any direct coupling of the digital signals to the analog output will produce spurious tones that vary with the exact digital input pattern.

Clock jitter should be minimized to avoid degrading the noise floor of the device in AC applications, especially where high output frequencies are being generated. Any noise coupling from the digital inputs to the clock input will cause phase modulation of the clock signal and the DAC waveform, and can produce spurious tones. It is normally best to place the digital data transitions near the falling clock edge, well away from the active rising clock edge. Because the clock signal contains spectral components only at the sampling frequency and its multiples, it is usually not a source of in band spurious tones. Overall, it is better to treat the clock as you would an analog signal and route it separately from the digital data input signals. The clock trace should be routed either over the analog ground plane or over its own section of the ground plane. The clock line needs to have accurately controlled impedance and should be well terminated near the LTC1666/ LTC1667/LTC1668.

Printed Circuit Board Layout Considerations—
Grounding, Bypassing and Output Signal Routing

The close proximity of high frequency digital data lines and high dynamic range, wide-band analog signals makes clean printed circuit board design and layout an absolute necessity. Figures 11 to 15 are the printed circuit board layers for an AC evaluation circuit for the LTC1668. Ground planes should be split between digital and analog sections as shown. All bypass capacitors should have minimum trace length and be ceramic 0.1\( \mu \)F or larger with low ESR. Bypass capacitors are required on \( V_{SS} \), \( V_{DD} \) and \( \text{REFOUT} \), and all connected to the AGND plane. The COMP2 pin ties to a node in the output current switching circuitry, and it requires a 0.1\( \mu \)F bypass capacitor. It should be bypassed to \( V_{SS} \) along with COMP1. The AGND and DGND pins should both tie directly to the AGND plane, and the tie point between the AGND and DGND planes should nominally be near the DGND pin. LADCOM should either be tied directly to the AGND plane or be bypassed to AGND. The \( I_{OUTA} \) and \( I_{OUTB} \) traces should be close together, short, and well matched for good AC CMRR. The transformer output ground should be capable of optionally being isolated or being tied to the AGND plane, depending on which gives better performance in the system.

Suggested Evaluation Circuit

Figure 10 is the schematic and Figures 11 to 15 are the circuit board layouts for a suggested evaluation circuit, DC245A. The circuit can be programmed with component selection and jumpers for a variety of differentially coupled transformer output and differential and single-ended resistor loaded output configurations.
Figure 10. Suggested Evaluation Circuit
Figure 11. Suggested Evaluation Circuit Board—Silkscreen
Figure 12. Suggested Evaluation Circuit Board—Component Side
Figure 13. Suggested Evaluation Circuit Board—GND Plane
Figure 14. Suggested Evaluation Circuit Board—Power Plane
Figure 15. Suggested Evaluation Circuit Board—Solder Side
G Package
28-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1640)

NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
   *DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE
   **DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.
Figure 16. Arbitrary Waveform Generator Has ±10V Output Swing, 50Msps DAC Update Rate

RELATED PARTS

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>COMMENTS</th>
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<tr>
<td>ADCs</td>
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<td>LTC1406</td>
<td>8-Bit, 20Msps ADC</td>
<td>Undersampling Capability Up to 70MHz Input</td>
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<td>14-Bit, 2.5Msps ADC</td>
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<td>LTC1420</td>
<td>12-Bit, 10Msps ADC</td>
<td>72dB SINAD at 5MHz fIN</td>
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<td>LTC1604/LTC1608</td>
<td>16-Bit, 333ksps/500ksps ADCs</td>
<td>16-Bit, No Missing Codes, 90dB SINAD, –100dB THD</td>
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<td>On-Chip 4-Quadrant Resistors</td>
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<td>Low Glitch, ±1LSB Maximum INL, DNL</td>
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<td>Serial 16-Bit Voltage Output DAC</td>
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<td>Single 16-Bit VOUT DAC with Serial Interface in SO-8</td>
<td>5V (3V) Single Supply, Rail-to-Rail Output Swing</td>
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<td>Rail-to-Rail Input and Output, Low Distortion</td>
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<td>3.6mA Supply Current, 8nV/√Hz Input Noise Voltage</td>
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