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The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content

The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

S70FL01GS

Military 1 Gbit (128 Mbyte) 3.0 V SPI Flash Memory

Features

- CMOS 3.0 V Core
- Serial Peripheral Interface (SPI) with Multi-I/O
  - SPI Clock polarity and phase modes 0 and 3
  - Double Data Rate (DDR) option
  - Extended Addressing: 32-bit address
  - Serial Command set and footprint compatible with S25FL-A, S25FL-K, and S25FL-P SPI families
  - Multi I/O Command set and footprint compatible with S25FL-P SPI family
- READ Commands
  - Normal, Fast, Dual, Quad, Fast DDR, Dual DDR, Quad DDR
  - AutoBoot – power up or reset and execute a Normal or Quad read command automatically at a preselected address
  - Common Flash Interface (CFI) data for configuration information
- Programming (1.5 Mbytes/s)
  - 512-byte Page Programming buffer
  - Quad-Input Page Programming (QPP) for slow clock systems
- Erase (0.5 Mbytes/s)
  - Uniform 256-kbyte sectors
- Cycling Endurance
  - 100 Program-Erase Cycles, minimum
- Data Retention
  - 20 Year Data Retention, minimum

Security Features

- One Time Program (OTP) array of 2048 bytes
- Block Protection
  - Status Register bits to control protection against program or erase of a contiguous range of sectors.
  - Hardware and software control options
  - Advanced Sector Protection (ASP)
  - Individual sector protection controlled by boot code or password
- Cypress® 65 nm MirrorBit® Technology with Eclipse™ Architecture
- Core Supply Voltage: 2.7 V to 3.6 V
- Temperature Range / Grade:
  - Military (–55 °C to +125 °C)
- Packages
  - 16-lead SOIC (300 mils)
  - BGA-24, 8 × 6 mm
    - 5 × 5 ball (ZSA024) footprint

General Description

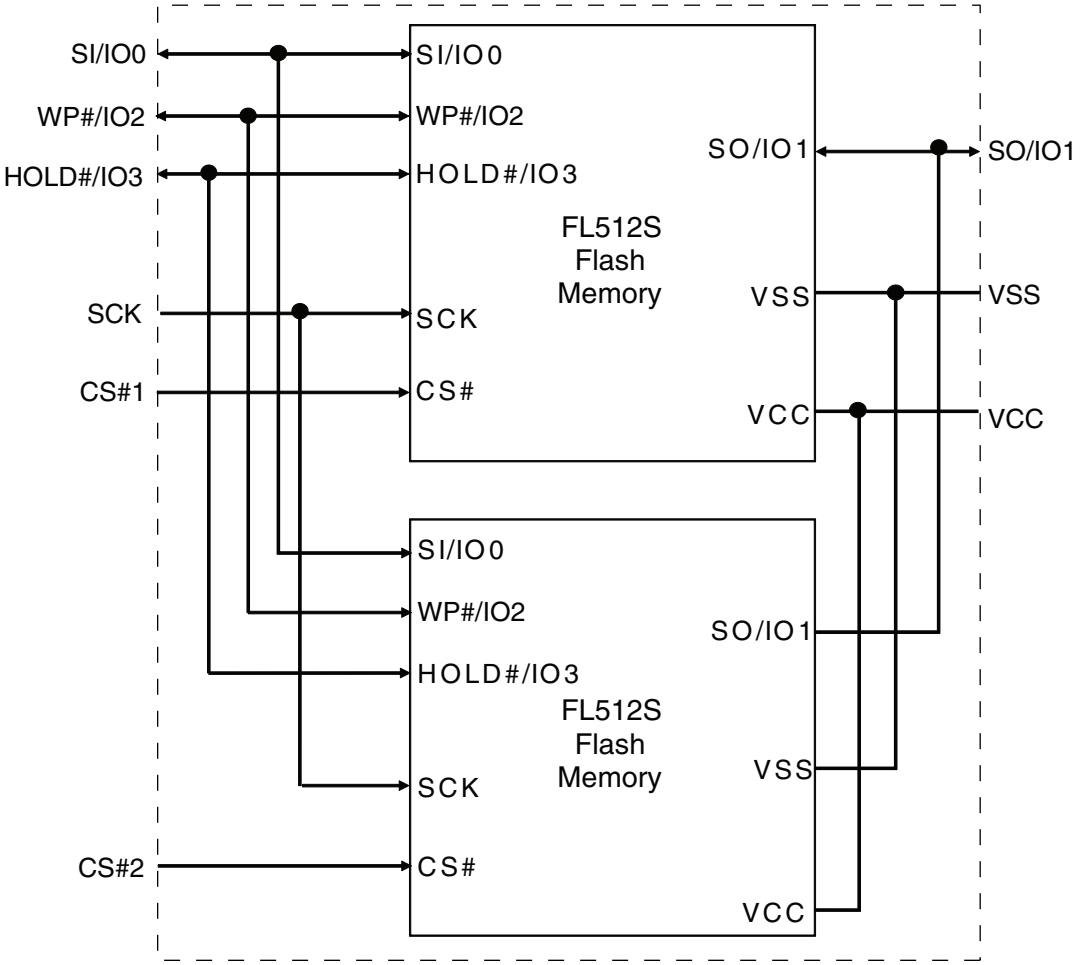
This document contains information for the S70FL01GS device, which is a dual die stack of two S25FL512S die. For detailed specifications, refer to the discrete die datasheet provided in the Affected Documents/Related Documents table.

Affected Documents/Related Documents

Document Title	Publication Number
S25FL512S Military 512 Mbit (64 Mbyte) 3.0V SPI Flash Memory	002-19087

Contents

Block Diagram



Connection Diagrams

Figure 1. 16-Pin Plastic Small Outline Package (SO)

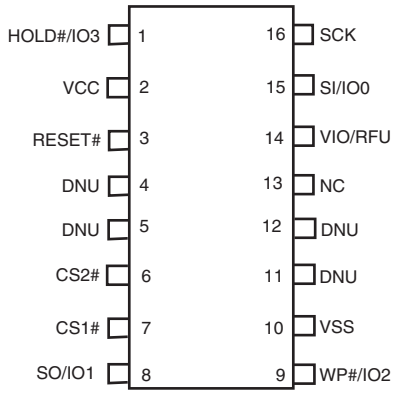
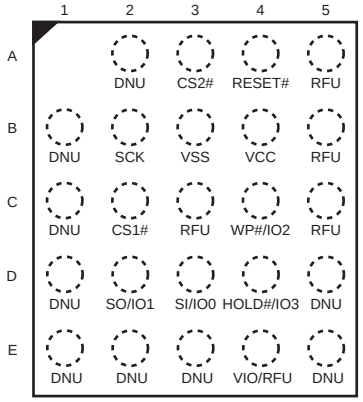


Figure 2. 24-Ball BGA, 5 x 5 Ball Footprint (ZSA024), Top View



Note:

V_{IO} is not supported in the S70FL01GS device and is RFU. Refer to Versatile I/O Power Supply (VIO) for more details.

Input/Output Summary

Table 1. Signal List

Signal Name	Type	Description
RESET#	Input	**Hardware Reset:** Low = device resets and returns to standby state, ready to receive a command. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used.
SCK	Input	Serial Clock.
CS1#	Input	Chip Select. FL512S #1.
CS2#	Input	Chip Select. FL512S #2.
SI / IO0	I/O	**Serial Input** for single bit data commands or IO0 for Dual or Quad commands.
SO / IO1	I/O	**Serial Output** for single bit data commands. IO1 for Dual or Quad commands.
WP# / IO2	I/O	**Write Protect** when not in Quad mode. IO2 in Quad mode. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad commands.
HOLD# / IO3	I/O	**Hold** (pause) serial transfer in single bit or Dual data commands. IO3 in Quad-I/O mode. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad commands.
V_{CC}	Supply	Core Power Supply.
V_{IO}	Supply	Versatile I/O Power Supply. **Note:** V_{IO} is not supported in the S70FL01GS device. Refer to Versatile I/O Power Supply (VIO) for more details.
V_{SS}	Supply	Ground.
NC	Unused	**Not Connected.** No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a Printed Circuit Board (PCB). However, any signal connected to an NC must not have voltage levels higher than V_{CC}.
RFU	Reserved	**Reserved for Future Use.** No device internal signal is currently connected to the package connector but there is potential future use of the connector for a signal. It is recommended to not use RFU connectors for PCB routing channels so that the PCB may take advantage of future enhanced features in compatible footprint devices.
DNU	Reserved	**Do Not Use.** A device internal signal may be connected to the package connector. The connection may be used by Cypress for test or other purposes and is not intended for connection to any host system signal. Any DNU signal related function will be inactive when the signal is at V_{IL}. The signal has an internal pull-down resistor and may be left unconnected in the host system or may be tied to V_{SS}. Do not use these connections for PCB signal routing channels. Do not connect any host system signal to this connection.

Device Operations

Programming

Each Flash die must be programmed independently due to the nature of the dual die stack.

Simultaneous Die Operation

The user may only access one Flash die of the dual die stack at a time via its respective Chip Select.

Sequential Reads

Sequential reads are not supported across the end of the first Flash die to the beginning of the second. If the user desires to sequentially read across the two die, data must be read out of the first die via CS1# and then read out of the second die via CS2#.

Sector/Bulk Erase

A sector erase command must be issued for sectors in each Flash die separately. Full device Bulk Erase via a single command is not supported due to the nature of the dual die stack. A Bulk Erase command must be issued for each die.

Status Registers

Each Flash die of the dual die stack is managed by its own Status Registers. Reads and updates to the Status Registers must be managed separately. It is recommended that Status Register control bit settings of each die are kept identical to maintain consistency when switching between die.

Configuration Register

Each Flash die of the dual die stack is managed by its own Configuration Register. Updates to the Configuration Register control bits must be managed separately. It is recommended that Configuration Register control bit settings of each die are kept identical to maintain consistency when switching between die.

Bank Address Register

It is recommended that the Bank Address Register bit settings of each die are kept identical to maintain consistency when switching between die.

Security and DDR Registers

It is recommended that the bit settings for ASP Register, Password Register, PPB Lock Register, PPB Access Register, DYB Access Register, and DDR Data Learning Register in each die are kept identical to maintain consistency when switching between die.

Block Protection

Each Flash die of the dual die stack will maintain its own Block Protection. Updates to the TBPROT and BPNV bits of each die must be managed separately. By default, each die is configured to be protected starting at the top (highest address) of each array, but no address range is protected. It is recommended that the Block Protection settings of each die are kept identical to maintain consistency when switching between die. In addition, any update to the FREEZE bit must be managed separately for each die. If the FREEZE bit is set to a logic 1, it cannot be cleared to a logic 0 until a power-on-reset is executed on each die that has the FREEZE bit set to 1.

Read Identification (RDID)

The Read Identification (RDID) command outputs the one-byte manufacturer identification, followed by the two-byte device identification and the bytes for the Common Flash Interface (CFI) tables. Each die of the FL01GS dual die stack will have identical identification data as the FL512S die, with the exception of the CFI data at byte 27h, as shown in <blue>Table 2.

Table 2. Product Group CFI Device Geometry Definition

Byte	Data	Description
27h	1Bh	Device Size = 2^N byte

RESET#

Note that the hardware RESET# input (pin 3 on the 16-pin SO package and ball A4 on the 5x5 BGA package) is bonded out and active for the S70FL01GS device. For applications that do NOT require use of the RESET# pin, it is recommended to not use RESET# for PCB routing channels that would cause the RESET# signal to be asserted Low (V_{IL}). Doing so will cause the device to reset to standby state. The RESET# signal has an internal pull-up resistor and may be left unconnected in the host system if not used.

Versatile I/O Power Supply (V_{IO})

Note that the Versatile I/O (V_{IO}) power supply (pin 14 on the 16-pin SO package and ball E4 on the 5x5 BGA package) is not supported, and pin 14 and ball E4 are RFU (Reserved for Future Use) in the standard configuration of the S70FL01GS device. Contact your local sales office to confirm availability with the V_{IO} feature enabled.

Temperature Ranges

Table 3. Temperature Range

Parameter	Symbol	Device	Spec		Unit
			Min	Max	
Ambient Temperature	T_A	Military (E)	-55	+125	°C

DC Characteristics

This section summarizes the DC Characteristics of the device.

Table 4. DC Characteristics

Parameter	Symbol	Test Conditions	Min	Typ [1]	Max	Unit
Input Low Voltage	V_{IL}	–	-0.5	–	0.2 x V_{CC}	V
Input High Voltage	V_{IH}	–	0.7 x V_{CC}	–	V_{CC} + 0.4	V
Output Low Voltage	V_{OL}	I_{OL} = 1.6 mA, V_{CC} = V_{CC} min	–	–	0.15 x V_{CC}	V
Output High Voltage	V_{OH}	I_{OH} = –0.1 mA	0.85 x V_{CC}	–		V
Input Leakage Current	I_{LI}	V_{CC} = V_{CC} Max, V_{IN} = V_{IH} or V_{IL}	–	–	±4	µA
Output Leakage Current	I_{LO}	V_{CC} = V_{CC} Max, V_{IN} = V_{IH} or V_{IL}	–	–	±4	µA
Active Power Supply Current (READ)	I_{CC1}	Serial SDR @ 50 MHz Serial SDR @ 133 MHz Quad SDR @ 80 MHz Quad SDR @ 104 MHz Quad DDR @ 66 MHz Quad DDR @ 80 MHz Outputs unconnected during read data return [2]	–	–	18 36 50 61 75 90	mA
Active Power Supply Current (Page Program)	I_{CC2}	CS# = V_{CC}	–	–	100	mA
Active Power Supply Current (WRR)	I_{CC3}	CS# = V_{CC}	–	–	100	mA
Active Power Supply Current (SE)	I_{CC4}	CS# = V_{CC}	–	–	100	mA
Active Power Supply Current (BE) [3]	I_{CC5}	CS# = V_{CC}	–	–	200	mA
Standby Current	I_{SB} (Industrial)	RESET#, CS# = V_{CC}; SI, SCK = V_{CC} or V_{SS}, Industrial Temp	–	140	200	µA
Standby Current	I_{SB} (Industrial Plus)	RESET#, CS# = V_{CC}; SI, SCK = V_{CC} or V_{SS}, Industrial Plus Temp	–	140	600	µA

Notes:
1. Typical values are at T_{AI} = 25 °C and V_{CC} = 3 V.
2. Output switching current is not included.
3. Bulk Erase current is for both die erasing simultaneously.

AC Test Conditions

Figure 3. Input, Output, and Timing Reference Levels

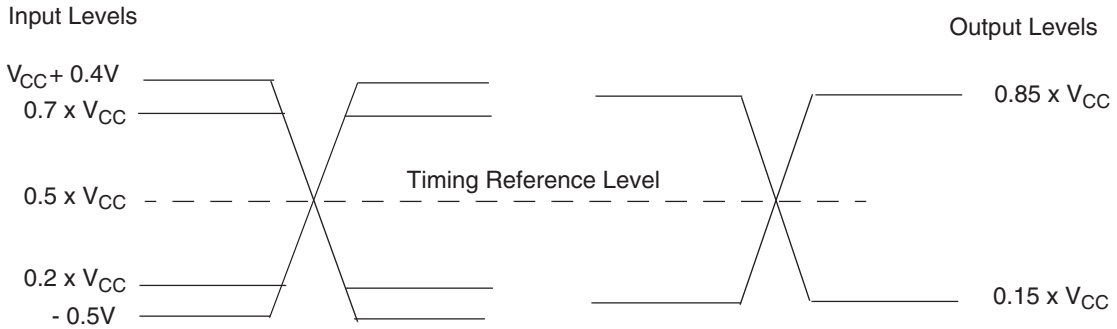


Figure 4. Test Setup

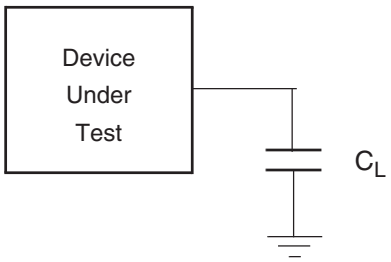


Table 5. AC Measurement Conditions

Parameter	Symbol	Min	Max	Unit
Load Capacitance	C_L	30 15 [4]		pF
Input Rise and Fall Times		–	2.4	ns
Input Pulse Voltage		0.2 x V_{CC} to 0.8 V_{CC}		V
Input Timing Ref Voltage		0.5 V_{CC}		V
Output Timing Ref Voltage		0.5 V_{CC}		V

Notes:

1. Output High-Z is defined as the point where data is no longer driven.
2. Input slew rate: 1.5 V/ns.
3. AC characteristics tables assume clock and data signals have the same slew rate (slope).

Note:

4. DDR Operation.

SDR AC Characteristics

Table 6. SDR AC Characteristics (Single Die Package, V_{CC} = 2.7V to 3.6V)

Parameter	Symbol	Min	Typ	Max	Unit
SCK Clock Frequency for READ and 4READ instructions	$F_{SCK, R}$	DC	–	50	MHz
SCK Clock Frequency for single commands [8]	$F_{SCK, C}$	DC	–	133	MHz
SCK Clock Frequency for the following dual and quad commands: DOR, 4DOR, QOR, 4QOR, DIOR, 4DIOR, QIOR, 4QIOR	$F_{SCK, C}$	DC	–	104	MHz
SCK Clock Frequency for the QPP, 4QPP commands	$F_{SCK, QPP}$	DC	–	80	MHz
SCK Clock Period	P_{SCK}	1/ F_{SCK}	–	∞	
Clock High Time [9]	t_{WH}, t_{CH}	45% P_{SCK}	–	–	ns
Clock Low Time [9]	t_{WL}, t_{CL}	45% P_{SCK}	–	–	ns
Clock Rise Time (slew rate)	t_{CRT}, t_{CLCH}	0.1	–	–	V/ns
Clock Fall Time (slew rate)	t_{CFT}, t_{CHCL}	0.1	–	–	V/ns
CS# High Time (Read Instructions) CS# High Time (Program/Erase)	t_{CS} [11]	10 50	–	–	ns
CS# Active Setup Time (relative to SCK)	t_{CSS}	3	–	–	ns
CS# Active Hold Time (relative to SCK)	t_{CSH}	3	–	–	ns
Data in Setup Time	t_{SU}	1.5	–	3000 [10]	ns
Data in Hold Time	t_{HD}	2	–	–	ns
Clock Low to Output Valid	t_V	–	–	8.0 [6] 7.65 [7] 6.5 [8]	ns
Output Hold Time	t_{HO}	2	–	–	ns
Output Disable Time	t_{DIS}	0	–	8	ns
WP# Setup Time	t_{WPS}	20 [5]	–	–	ns
WP# Hold Time	t_{WPH}	100 [5]	–	–	ns
HOLD# Active Setup Time (relative to SCK)	t_{HLCH}	3	–	–	ns
HOLD# Active Hold Time (relative to SCK)	t_{CHHH}	3	–	–	ns
HOLD# Non-Active Setup Time (relative to SCK)	t_{HHCH}	3	–	–	ns
HOLD# Non-Active Hold Time (relative to SCK)	t_{CHHL}	3	–	–	ns
HOLD# Enable to Output Invalid	t_{HZ}	–	–	8	ns
HOLD# Disable to Output Valid	t_{LZ}	–	–	8	ns

Notes:
5. Only applicable as a constraint for WRR instruction when SRWD is set to a 1.
6. Full V_{CC} range (2.7 - 3.6V) and CL = 30 pF.
7. Regulated V_{CC} range (3.0 - 3.6V) and CL = 30 pF.
8. Regulated V_{CC} range (3.0 - 3.6V) and CL = 15 pF.
9. ±10% duty cycle is supported for frequencies ≤ 50 MHz.
10. Maximum value only applies during Program/Erase Suspend/Resume commands.
11. When switching between die, a minimum time of t_{CS} must be kept between the rising edge of one chip select and the falling edge of the other for operations and data to be valid.

DDR AC Characteristics

Table 7. DDR AC Characteristics 66 MHz and 80 MHz Operation

Parameter	Symbol	66 MHz			80 MHz			Unit
		Min	Typ	Max	Min	Typ	Max	
SCK Clock Frequency for DDR READ instruction	$F_{SCK, R}$	DC	–	66	DC	–	80	MHz
SCK Clock Period for DDR READ instruction	$P_{SCK, R}$	15	–	∞	12.5	–	∞	ns
Clock High Time	t_{WH}, t_{CH}	45% P_{SCK}	–	–	45% P_{SCK}	–	–	ns
Clock Low Time	t_{WL}, t_{CL}	45% P_{SCK}	–	–	45% P_{SCK}	–	–	ns
CS# High Time (Read Instructions)	t_{CS}	10	–	–	10	–	–	ns
CS# Active Setup Time (relative to SCK)	t_{CSS}	3	–	–	3	–	–	ns
CS# Active Hold Time (relative to SCK)	t_{CSH}	3	–	–	3	–	–	ns
IO in Setup Time	t_{SU}	2	–	3000 [13]	1.5	–	3000 [13]	ns
IO in Hold Time	t_{HD}	2	–	–	1.5	–	–	ns
Clock Low to Output Valid	t_V	0	–	6.5 [12]	–	–	6.5 [12]	ns
Output Hold Time	t_{HO}	1.5	–	–	1.5	–	–	ns
Output Disable Time	t_{DIS}	–	–	8	–	–	8	ns
Clock to Output Low Impedance	t_{LZ}	0	–	8	0	–	8	ns
First IO to last IO data valid time	t_{IO_skew}	–	–	600	–	–	600	ps

Capacitance Characteristics

Table 8. Capacitance

	Parameter	Test Conditions	Min	Max	Unit
C_{IN}	Input Capacitance (applies to SCK, CS#1, CS#2, RESET#)	1 MHz	–	16	pF
C_{OUT}	Output Capacitance (applies to All I/O)	1 MHz	–	16	pF

Note:

For more information on capacitance, please consult the IBIS models.

Notes:

12. Regulated V_{CC} range (3.0 - 3.6 V) and CL =15 pF.
13. Maximum value only applies during Program/Erase Suspend/Resume commands.

Data Integrity

Erase Endurance

Table 9. Erase Endurance

Parameter	Minimum	Unit
Program/Erase cycles per main Flash array sectors	100	PE cycle
Program/Erase cycles per PPB array or non-volatile register array [14]	100	PE cycle

Data Retention

Table 10. Data Retention at 125 °C

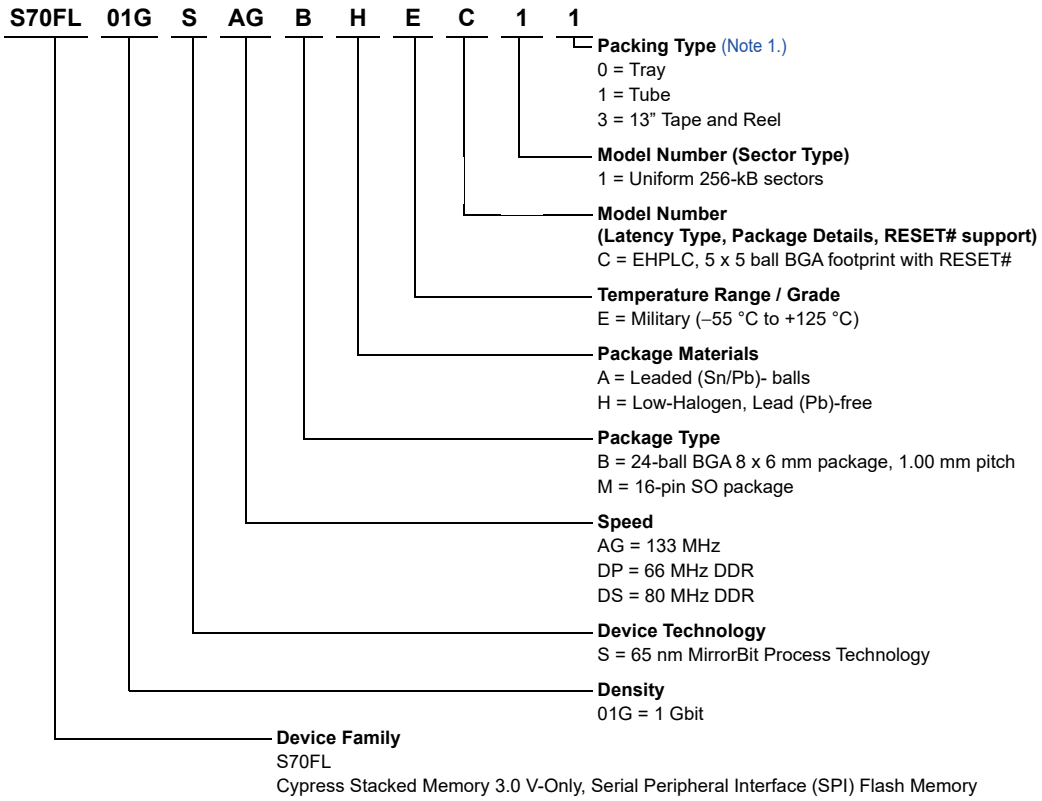
Parameter	Test Conditions	Minimum Time	Unit
Data Retention Time	100 Program/Erase Cycles	> 20	Years

Contact Cypress Sales and FAE for further information on the data integrity. An application note is available at www.cypress.com/appnotes.

Note:
14. Each write command to a non-volatile register causes a PE cycle on the entire non-volatile register array. OTP bits and registers internally reside in a separate array that is not PE cycled.

Ordering Information

The ordering part number is formed by a valid combination of the following:



Notes:

1. EHPLC = Enhanced High Performance Latency Code table.
2. Uniform 256-kB sectors = All sectors are uniform 256-kB with a 512B programming buffer.

Valid Combinations — Military

Table 11 lists the configurations that are Military qualified and are planned to be available in volume. The table will be updated as new combinations are released. Consult your local sales representative to confirm availability of specific combinations and to check on newly released combinations.

Table 11. S70FL01GS Valid Combinations — Military

Valid Combinations - Military					Package Marking [15]
Base Ordering Part Number	Speed Option	Package and Temperature	Model Number	Packing Type	
S70FL01GS	AG	BHE	C1	0	FL01GS + A + (temp) + H + (Model Number)
		BAE			
		MHE			

Other Resources

Cypress Flash Memory Roadmap

www.cypress.com/product-roadmaps/cypress-flash-memory-roadmap

Links to Software

www.cypress.com/software-and-drivers-cypress-flash-memory

Links to Application Notes

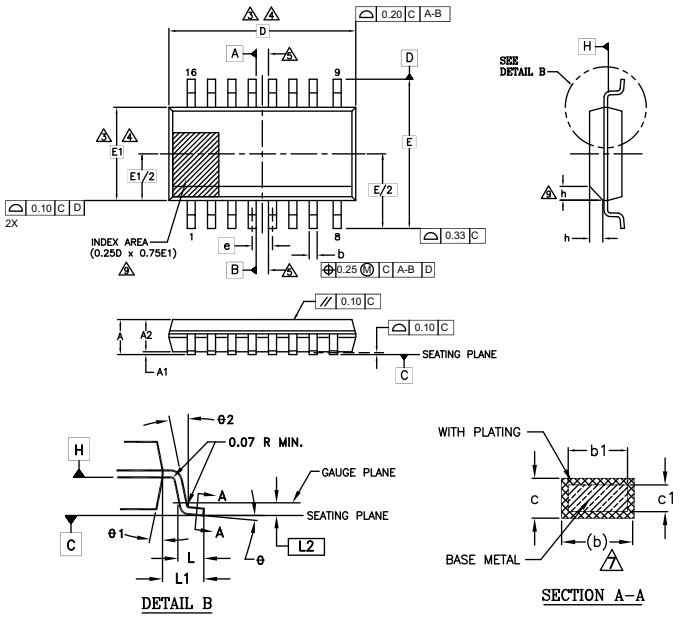
www.cypress.com/appnotes

Note

15. Package Marking omits the leading “S70” and package type

Physical Diagram

SOIC 16 Lead, 300-mil Body Width

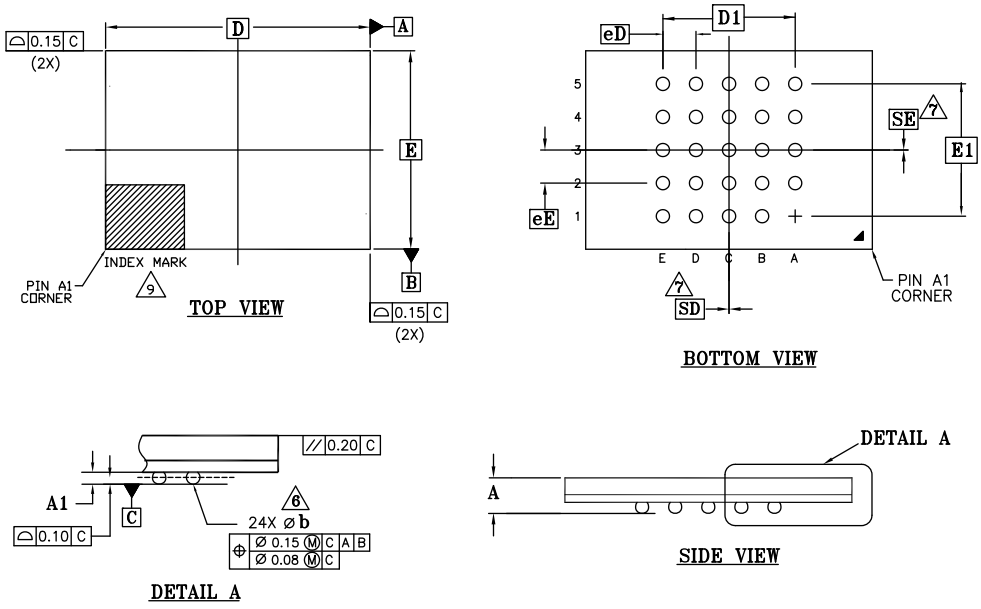


SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	2.35	-	2.65
A1	0.10	-	0.30
A2	2.05	-	2.55
b	0.31	-	0.51
b1	0.27	-	0.48
c	0.20	-	0.33
c1	0.20	-	0.30
D	10.30 BSC		
E	10.30 BSC		
E1	7.50 BSC		
e	1.27 BSC		
L	0.40	-	1.27
L1	1.40 REF		
L2	0.25 BSC		
N	16		
h	0.25	-	0.75
θ	0°	-	8°
θ1	5°	-	15°
θ2	0°	-	-

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUSIVE OF ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A AND B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE LEAD FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED.
10. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THE SEATING PLANE.

24-Ball BGA 8 x 6 mm (ZSA024)



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.20
A1	0.20	-	-
D		8.00 BSC	
E		6.00 BSC	
D1		4.00 BSC	
E1		4.00 BSC	
MD		5	
ME		5	
n		24	
Ø b	0.35	0.40	0.45
eD		1.00 BSC	
eE		1.00 BSC	
SD		0.00	
SE		0.00	

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. [e] REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

△6 DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

△7 "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

△9 A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

Document History Page

Document Title: S70FL01GS, Military 1 Gbit (128 Mbyte) 3.0 V SPI Flash Memory Document Number: 002-29555			
Revision	**ECN**	**Submission Date**	**Description of Change**
**	6791282	02/05/2020	Initial release.

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Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

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Cypress Developer Community

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Technical Support

cypress.com/support