

## HYBRID VOLTAGE REGULATORS CJCA001 CJCA002 CJCA007 CJCA008

# VARIABLE OUTPUT HYBRID VOLTAGE REGULATORS

## ± 8V TO ± 56V

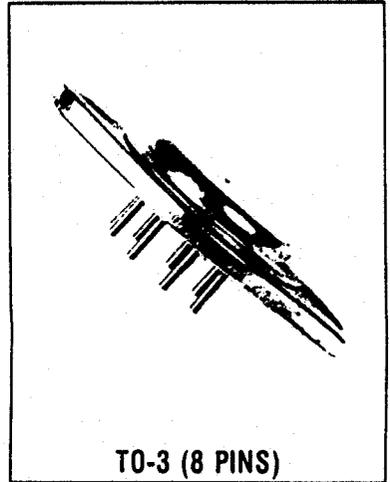
### 5 AMPERES

#### FEATURES

POSITIVE, NEGATIVE SUPPLY OPERATION  
5A CURRENT RATING  
60V LINE VOLTAGE CAPABILITY  
LINE AND LOAD REGULATION  
OUTPUT VOLTAGE ADJUSTED FROM 8 TO 56 VOLTS BY A RESISTOR DIVIDED NETWORK. ALL DEVICES ARE PLANAR OXIDE PASSIVATED. BERILLIA CERAMIC ISOLATION PADS.

#### APPLICATIONS

- INDUSTRIAL CONTROLS
- INSTRUMENTATION
- COMPUTERS, DATA TERMINALS
- MILITARY EQUIPMENT, SPACE AND TELECOMMUNICATIONS
- DISTRIBUTED POWER SYSTEMS
- MEDICAL ELECTRONICS
- DC MOTOR SUPPLIES



TO-3 (8 PINS)

#### MAXIMUM RATINGS

		CJCA001 CJCA007	CJCA002 CJCA008
$  \pm V_{in}  $	INPUT VOLTAGE (FIGS. 2, 3 PINS 1-7)	60 V	
$I_{opk}$	PEAK LOAD CURRENT (FIGS. 2, 3 PIN 2)	5 A	
$T_A$	OPERATING TEMPERATURE	-55°C to +150°C	
$T_{stg}$	STORAGE TEMPERATURE	-55°C to +150°C	
$R_{\theta JC}$	THERMAL RESISTANCE, JUNCTION TO CASE	3°C/W	
$P_D$	POWER DISSIPATION (100°C)	50 W	

REGULATORS	CJCA	001	002	007	008	UNITS
Output Voltage Range		+8 to +56	-8 to -56	-	-	$V_{dc}$
with FET Internal Current Source		-	-	+8 to +56	-8 to -56	$V_{dc}$

CJCA 007 and 008 incorporate a FET constant current source, which provides current mode regulation automatically. A minimum input-output voltage differential of 4 volts is recommended to bias the FET into its constant current region. At lower voltages the FET becomes resistive, and regulation reverts back to basic mode.

## HYBRID VOLTAGE REGULATORS

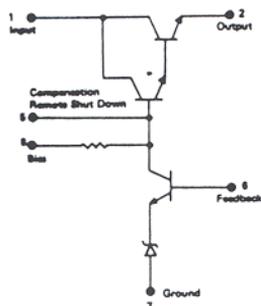
CJCA001 CJCA002 CJCA007 CJCA008

### ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ , $|\pm V_{IN}| = 28\text{V}$ , $|\pm V_O| = 20\text{V}$ , $|\pm I_O| = 1\text{A}$ UNLESS OTHERWISE NOTED)

CHARACTERISTICS	SYMBOL	MIN.	MAX.	UNITS
INPUT VOLTAGE	$ \pm V_{IN} $	10	60	V
CJCA001 CJCA002 CJCA007 CJCA008		12	60	V
OUTPUT VOLTAGE RANGE	$ \pm V_O $	8	56	V
INPUT-OUTPUT DIFFERENTIAL	$ \Delta V $	2	50	V
CJCA001 CJCA002 CJCA007 CJCA008		4	50	V
LOAD REGULATION ( $I_O = 0\text{A}-5.0\text{A}$ )	$\frac{\Delta V_O}{V_O}$		0.5	%
LINE REGULATION ( $ V_{IN}  \pm 20\%$ , $I_O = 1.0\text{A}$ )	$\frac{\Delta V_O}{V_O}$	CJCA001 CJCA002	2.0	%
CJCA007 CJCA008		0.5	%	
RIPPLE ATTENUATION (fig. 11, fig. 12)		CJCA001 CJCA002	32	db
CJCA007 CJCA008		62	db	
TEMPERATURE COEFFICIENT ( $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ )	$\frac{\Delta V_O}{V_O \Delta T}$		$\pm 0.02$	$\%/^\circ\text{C}$

#### SCHEMATIC

##### POSITIVE REGULATOR



CJCA 001

FIGURE 1

#### BASIC MODE

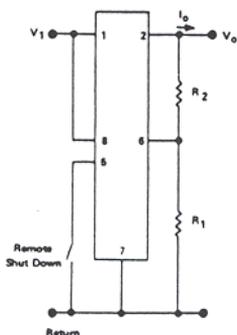


FIGURE 2

#### CURRENT MODE

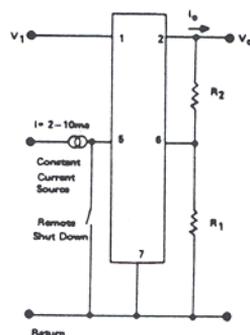
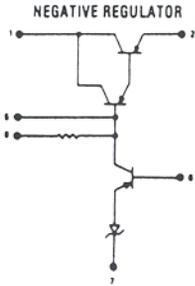


FIGURE 3

**HYBRID VOLTAGE REGULATORS**  
CJCA001 CJCA002 CJCA007 CJCA008

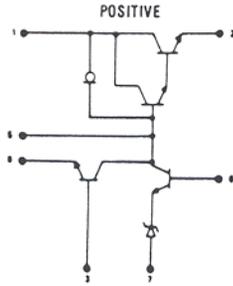
REGULATORS WITH FET INTERNAL CURRENT SOURCE AND LIMIT



CJCA 002

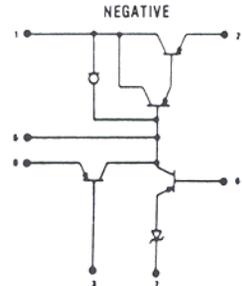
FIGURE 4

Hook up per Fig. 2 and 3, but  $V_1$  and  $V_0$  are negative voltage



CJCA 007

FIGURE 5



CJCA 008

FIGURE 6

**LOAD REGULATION**

TYPICAL CURVES

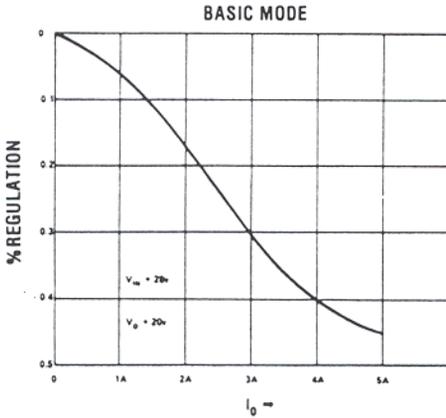


FIGURE 7

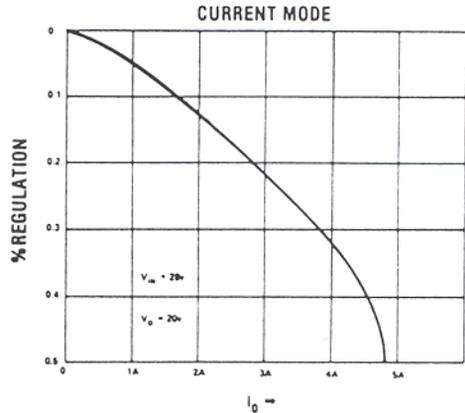


FIGURE 8

**LINE REGULATION**

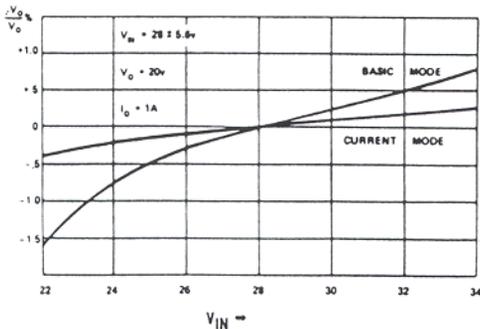


FIGURE 9

**POWER DERATING**

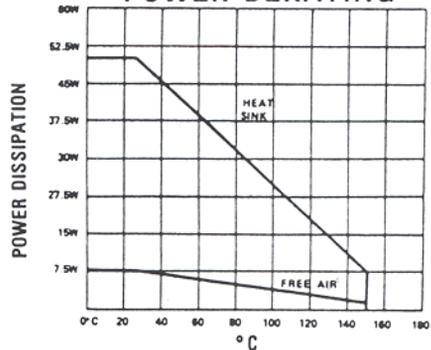
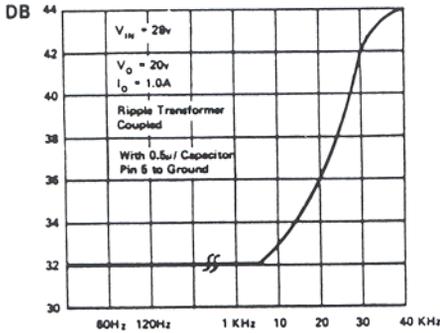


FIGURE 10

## HYBRID VOLTAGE REGULATORS CJCA001 CJCA002 CJCA007 CJCA008

### RIPPLE ATTENUATION

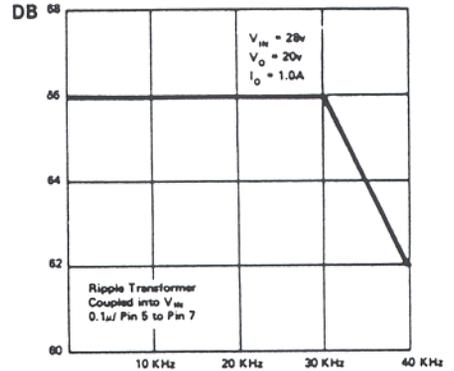
BASIC MODE



FREQUENCY

FIGURE 11

CURRENT MODE



FREQUENCY

FIGURE 12

HOOK UP FOR CJCA 007 and CJCA 008

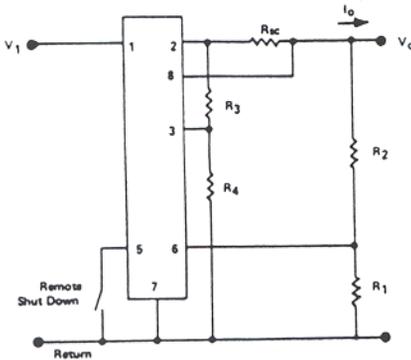
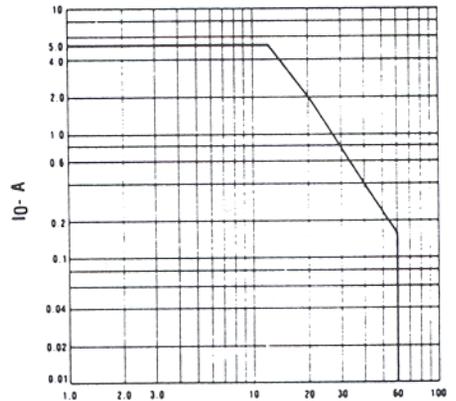


FIGURE 13

See note 2 for above application

D.C. SAFE OPERATING AREA FOR PASS TRANSISTORS



V1-V0 VOLTS

FIGURE 14

**NOTES:**

- Reference diode is  $6.2 \pm .3$  volts, and the  $V_{BE}$  of the feedback transistor is  $0.6 \pm .1$  volt, giving  $V_{6-7} = 6.4$  to  $7.2$  volts, temperature compensated. External divider  $R_1$  and  $R_2$  in Figs. 2, 3 and 13 determines the output voltage  $V_0$ .

$$V_0 = V_{6-7} \left( \frac{R_1 + R_2}{R_1} \right) \approx 7v \left( \frac{R_1 + R_2}{R_1} \right)$$

## HYBRID VOLTAGE REGULATORS CJCA001 CJCA002 CJCA007 CJCA008

- (cont'd.) Recommended maximum value for  $R_1$  is  $7K\Omega$  ( $I_{min.} = 1ma$ ), typical usage being  $1K\Omega$  to  $5K\Omega$ .  $R_2$  must be determined experimentally for each regulator for a particular value of  $V_0$ , due to the variations in  $V_{6-7}$ .
- Current limiting capability is provided on the CJCA 007 and CJCA 008.  $R_{sc}$  may be selected to limit  $I_0$  and  $I_{sc}$  as shown in Fig. 13. The user must be sure that the dissipation rating is not exceeded in worst-case operation (see Fig. 10). Also, for  $V_1 - V_0 (= V_1$  for a shorted load) greater than 20 volts, a further limitaton is second breakdown of the pass transistor (see Fig. 14).

### Example:

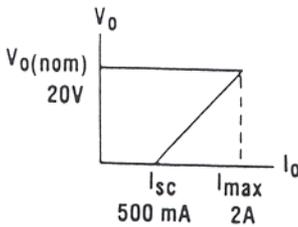


FIGURE 15

### assumptions

$$I_{MAX} = 2A$$

$$I_{sc} = 500ma$$

$$V_0(nom) = 20v$$

$$\alpha = \frac{V_{BE}}{V_0} \left[ \frac{I_{MAX}}{I_{sc}} - 1 \right]$$

$$\alpha = \frac{.6}{20} \left[ \frac{2000}{500} - 1 \right] = .09$$

$$R_{sc} = \frac{V_{BE}}{(1 - \alpha) I_{sc}} = \frac{.6}{(1 - .09) 500 \times 10^{-3}} = 1.32\Omega$$

$$R_3 = \frac{\alpha}{1 - \alpha} 10K = \frac{.09}{1 - .09} 10K = 989\Omega$$

$$R_4 = 10K\Omega$$

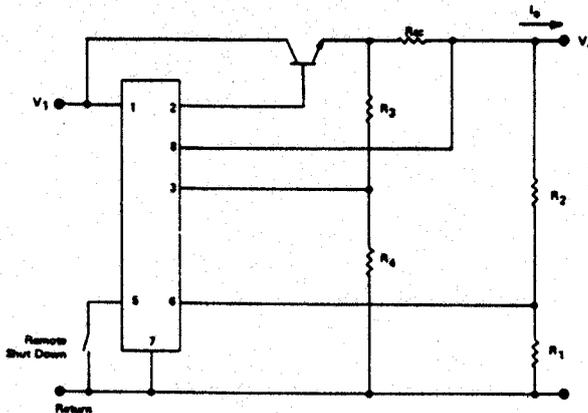
Resistors  $R_1$  and  $R_2$  are found from note 1.

- Current limiting for CJCA 001 and CJCA 002 can be provided by adding a NPN(PNP) transistor and resistors hooked-up as shown in Figs. 5, 6 and 13. Resistor values are found in notes 1 and 2.
- Oscillation suppression may be best obtained if needed by connecting a capacitor from pin 5 to pin 7; 0.01uf is usually sufficient. A capacitor at the input (pin 1 to 7) or output (pin 2 to 7) may also be helpful. When using a capacitor on the ouput, and not current limiting, care must be taken that the capacitance is not so large that an excessive turn-on surge current develops, damaging the pass transistor.
- Inductive surges on the output may be suppressed by adding a reverse-biased diode on the output returned to ground.

**HYBRID VOLTAGE REGULATORS**

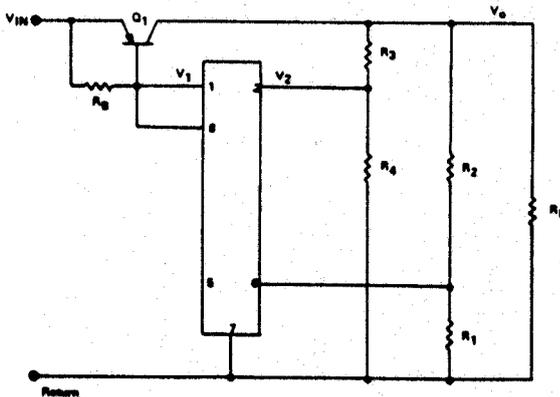
**CJCA001 CJCA002 CJCA007 CJCA008**

- Output current and power capability may be increased by driving an external power pass transistor. Figure 16 below illustrates for the regulator CJCA 007. For the negative regulators, reverse the polarities and use external pnp pass transistor. Be sure to maintain safe operating area conditions for both the regulator and the external transistors. All resistor values are found in notes 1 and 2 and Figs. 5, 6 and 13.



**FIGURE 16**

- Output current and power may be increased, and input-output voltage differential reduced, by the use of one or more external pnp pass transistors for the positive regulators. Figure 17 below illustrates for CJCA 001.



$$(V_{IN} - V_o) \min = V_{CE \text{ sat}}(Q_1)$$

$$V_1 = V_{IN} - V_{BE}(Q_1)$$

$$V_2 = V_o \left( \frac{R_4}{R_3 + R_4} \right)$$

$$V_2 \min \approx 8 \text{ volts}$$

**FIGURE 17**

Thus,  $V_o$  is not restricted by the input-output differential of the regulator, which is  $V_1 - V_2$ .

## HYBRID VOLTAGE REGULATORS

**CJCA001 CJCA002 CJCA007 CJCA008**

### 8. Regulator Failures

- a. Regulator failures are caused by overdissipating the series pass transistor. Excessive heating in the pass transistor causes it to short out. A good heat sink must be used. Highest power dissipation occurs when the regulator output is shorted. Foldback current limiting should be used giving less power dissipation than at full load.
- b. Use conservatively voltage rated capacitors on the input to the regulator in order to minimize ripple. If the input capacitor is operated with excessive ripple and near the maximum dc voltage rating, the capacitor will sputter (short momentarily) causing the output capacitor of the regulator to discharge back through the reverse-biased pass transistor or the control circuitry with destructive effects.
- c. Avoid severe voltage transients on the unregulated input. Subsequent transients can destroy the regulator because of load failures due to previous transients.