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MT41K128M16JT-125

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Data Sheets (1)

Data Sheet

2Gb: x4, x8, x16 DDR3L SDRAM

DDR3 SDRAM
DRAM

2Gb: x4, x8, x16 DDR3L SDRAM

File Type: PDF Updated: 07/2016

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Specs

Orderable Parts for: MT41K128M16JT-125

[SEE ALL DDR3 SDRAM PARTS](#)

	Status	Media	FBGA Code	SPD Data	Chipset Validation	PLP	Start Date	Alternative Part
MT41K128M16JT-125 AUT:K	Production	N/A	D9VKD	N/A	N/A	No		N/A
MT41K128M16JT-125:K	Production	N/A	D9PTK	N/A	N/A	No		N/A

Detailed Specifications

Density	2Gb	Part Status	Production	RoHS	Yes	Depth	128Mb
Width	x16	Voltage	1.35V	Package	FBGA	Pin Count	96-ball
Clock Rate	800 MHz	Cycle Time	1.25ns	Op. Temp.	0C to +95C	CL	CL = 11
Data Rate	DDR3-1600	Features					

Sim Models & Software

Sim Models

IBIS

IBIS: 2Gb DDR3L SDRAM V89C (ZIP)

DDR3 SDRAM
DRAM

Revision 2.2 (Die Rev. K)

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Verilog

DDR3 SDRAM Verilog Model (ZIP)

Automotive
DDR3 SDRAM
DRAM
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1.74

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HSpice

HSpice: 2Gb DDR3L SDRAM V89C (ZIP)

DDR3 SDRAM
DRAM

2.1 (Die Rev. K)

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RoHS Certificates

RoHS Certificates

RoHS Certificate of Compliance (PDF)

MT41K128M16JT-125

Part-specific certification of how this product meets the requirements of the current DIRECTIVE 2002/95/EC, a.k.a. Restriction of Hazardous Substances (RoHS) Directive.

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RoHS Certificates

China RoHS Certificate (PDF)

MT41K128M16JT-125

Part-specific certification as required by China's Management Methods for Controlling Pollution by Electronic Information Products.

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Documentation & Support

[See All DDR3 SDRAM Documentation](#)

Technical Notes

SEARCH (16) DDR3 SDRAM TECHNICAL NOTES

Technical Notes



[TN-04-59: LPDDR3/4 MR4 Use Guidelines \(PDF\)](#)

[DDR2 SDRAM](#)
[DDR3 SDRAM](#)
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(TN-04-56) Explains how to use mode register 4 to read LPDDR3 and LPDDR4 temperature data.

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Technical Notes

[TN-00-33: Power Integrity Simulation with IBIS 5.0 Models \(PDF\)](#)

[3D NAND](#)
[DDR3 SDRAM](#)
[DDR4 SDRAM](#)
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(TN-00-33) This technical note describes the new features in IBIS 5.0 enabling PI simulation. It also provides an overview of some of the modeling accuracy challenges and compares SSO simulation results using various electronic design automation (EDA) software tools.

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Updated: 01/25/2016

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Technical Notes

[User's Manual: New Features of DDR3 SDRAM \(PDF\)](#)

[DDR3 SDRAM](#)
[DRAM](#)

(E1503E10) This manual is intended for users who design application systems using DDR3 SDRAM manufactured by Elpida.

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Updated: 02/26/2014

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Technical Notes

[TN-41-16: DDR3 8Gb DDP 2CS to 8Gb SDP 1CS Transition Guide \(PDF\)](#)

[DDR3 SDRAM](#)
[DRAM](#)

(TN-41-16) This technical note explains how to transition a dual-rank 8Gb 2CS (dual die) MT41K512M16 DDP device to a single-rank 8Gb 1CS (monolithic) MT41K512M16 SDP device.

File Type: PDF

Updated: 02/12/2014

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Technical Notes

(TN-41-13) DDR3 is an evolutionary transition from DDR2.

File Type: PDF

Updated: 08/02/2013

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SEARCH (16) DDR3 SDRAM TECHNICAL NOTES

Parts with the same Data Sheet (16)

MT41K128M16JT-125 (Current)		MT41K128M16HA-15E IT	MT41K256M8DA-125	MT41K512M4DA-125
Part Status	Production	Obsolete	Production	Production
Density	2Gb	2Gb	2Gb	2Gb
RoHS	Yes	Yes	Yes	Yes
Depth	128Mb	128Mb	256Mb	512Mb
Width	x16	x16	x8	x4
Voltage	1.35V	1.35V	1.35V	1.35V
Package	FBGA	FBGA	FBGA	FBGA
Pin Count	96-ball	96-ball	78-ball	78-ball
Clock Rate	800 MHz	667 MHz	800 MHz	800 MHz
Cycle Time	1.25ns	1.5ns	1.25ns	1.25ns
Op. Temp.	0C to +95C	-40C to +95C	0C to +95C	0C to +95C
CL	CL = 11	CL = 9	CL = 11	CL = 11
Data Rate	DDR3-1600	DDR3-1333	DDR3-1600	DDR3-1600
Features				

MT41K128M16JT-125
(Current)

Part Status **Production**

Density **2Gb**


RoHS **Yes**


Where to Buy

Depth	128Mb	Status	Media	FBGA Code	SPD Data	Chipset Validation	PLP	Start Date	Alternative Part
Width	x16								
Voltage	1.35V	Production	N/A	D9VKD	N/A	N/A	No		N/A
Package	FBGA	Production	N/A	D9PTK	N/A	N/A	No		N/A
Pin Count	96-ball								
Clock Rate	800 MHz								
Cycle Time	1.25ns								
Op. Temp.	0C to +95C								
CL	CL = 11								
Data Rate	DDR3-1600								
Features									

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