81 GHz to 86 GHz, E-Band Power Amplifier
With Power Detector

**FEATURES**
- Gain: 21 dB typical
- Output power for 1 dB compression (P1dB): 25 dBm typical
- Saturated output power (Psat): 26 dBm typical
- Output third-order intercept (OIP3): 29 dBm typical
- Input return loss: 12 dB typical
- Output return loss: 8 dB typical
- DC supply: 4 V at 450 mA
- No external matching required
- Die size: 3.039 mm × 1.999 mm × 0.05 mm

**APPLICATIONS**
- E-band communication systems
- High capacity wireless backhaul radio systems
- Test and measurement

**GENERAL DESCRIPTION**
The HMC8142 is an integrated E-band gallium arsenide (GaAs), pseudomorphic high electron mobility transistor (pHEMT), monolithic microwave integrated circuit (MMIC), medium power amplifier with a temperature compensated on-chip power detector that operates from 81 GHz to 86 GHz. The HMC8142 provides 21 dB of gain, 25 dBm of output power at 1 dB compression, 29 dBm of output third-order intercept, and 26 dBm of saturated output power at 20% power added efficiency (PAE) from a 4 V power supply. The HMC8142 exhibits excellent linearity and is optimized for E-band communications and high capacity wireless backhaul radio systems. The amplifier configuration and high gain make it an excellent candidate for last stage signal amplification before the antenna. All data is taken with the chip in a 50 Ω test fixture connected via a 3 mil wide × 0.5 mil thick × 7 mil long ribbon on each port.

**FUNCTIONAL BLOCK DIAGRAM**

![Functional Block Diagram](image)
SPECIFICATIONS

$T_A = 25^\circ C$, $V_{DDx} = 4$ V, $I_{DD} = 450$ mA, unless otherwise noted.

Table 1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPERATING CONDITIONS Radio Frequency (RF) Range</td>
<td>81</td>
<td>86</td>
<td>GHz</td>
<td></td>
</tr>
<tr>
<td>PERFORMANCE</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain</td>
<td>19</td>
<td>21</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Gain Variation over Temperature</td>
<td>0.02</td>
<td>dB/°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Power for 1 dB Compression ($P_{1\text{dB}}$)</td>
<td>22.5</td>
<td>25</td>
<td>dBm</td>
<td></td>
</tr>
<tr>
<td>Saturated Output Power ($P_{sat}$)</td>
<td>26</td>
<td>dBm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Third-Order Intercept ($OIP3$) at Maximum Gain</td>
<td>29</td>
<td>dBm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Return Loss</td>
<td>12</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Return Loss</td>
<td>8</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>POWER SUPPLY</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total Supply Current ($I_{DD}$)</td>
<td>450</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1 Data taken at output power ($P_{out}$) = 12 dBm/tone, 1 MHz spacing.
2 Adjust $V_{GGx}$ from $-2$ V to 0 V to achieve the total drain current, $I_{DD} = 450$ mA.
ABSOLUTE MAXIMUM RATINGS

Table 2.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
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<tbody>
<tr>
<td>Drain Bias Voltage (VDD1 to VDD4)</td>
<td>4.5 V</td>
</tr>
<tr>
<td>Gate Bias Voltage (VGG1 to VGG4)</td>
<td>−3 V to 0 V</td>
</tr>
<tr>
<td>Maximum Junction Temperature (to Maintain 1 Million Hours Mean Time to Failure (MTTF))</td>
<td>175°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>−65°C to +150°C</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>−55°C to +85°C</td>
</tr>
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</table>

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Table 3. Thermal Resistance

<table>
<thead>
<tr>
<th>Package Type</th>
<th>θJC 1</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>25-Pad Bare Die [CHIP]</td>
<td>48.33°C/W</td>
<td></td>
</tr>
</tbody>
</table>

1 Based on ABLETHERM® 2600BT as die attach epoxy with thermal conductivity of 20 W/mK.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.
Table 4. Pad Function Descriptions

<table>
<thead>
<tr>
<th>Pad No.</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1, 3, 4, 6, 8, 10, 12, 14, 17, 19, 21, 23, 25</td>
<td>GND</td>
<td>Ground Connection (See Figure 3).</td>
</tr>
<tr>
<td>2</td>
<td>RFIN</td>
<td>RF Input. AC couple RFIN and match it to 50 Ω (See Figure 4).</td>
</tr>
<tr>
<td>5, 7, 9, 11</td>
<td>VDD1 to VDD4</td>
<td>Drain Bias Voltage for the Power Amplifier (See Figure 5).</td>
</tr>
<tr>
<td>13</td>
<td>RFOUT</td>
<td>RF Output. AC couple RFOUT and match it to 50 Ω (see Figure 6).</td>
</tr>
<tr>
<td>15</td>
<td>VDET</td>
<td>Detector Voltage for the Power Detector (See Figure 7). VDET is the dc voltage representing the RF output power rectified by the diode, which is biased through an external resistor. Refer to the typical application circuit for the required external components (see Figure 40).</td>
</tr>
<tr>
<td>16</td>
<td>VREF</td>
<td>Reference Voltage for the Power Detector (See Figure 7). VREF is the dc bias of diode biased through an external resistor used for the temperature compensation of VDET. Refer to the typical application circuit for the required external components (see Figure 40).</td>
</tr>
<tr>
<td>18, 20, 22, 24</td>
<td>VGG4 to VGG1</td>
<td>Gate Bias Voltage for the Power Amplifier (See Figure 8). Refer to the typical application circuit for the required external components (see Figure 40).</td>
</tr>
<tr>
<td>Die Bottom</td>
<td>GND</td>
<td>Ground. The die bottom must be connected to the RF/dc ground (see Figure 3).</td>
</tr>
</tbody>
</table>
INTERFACE SCHEMATICS

Figure 3. GND Interface

Figure 4. RFIN Interface

Figure 5. VDD1 to VDD4 Interface

Figure 6. RFOUT Interface

Figure 7. VDET, VREF Interface

Figure 8. VGG4 to VGG1 Interface
TYPICAL PERFORMANCE CHARACTERISTICS

Figure 9. Broadband Gain and Return Loss Response vs. Frequency,
Drain Current (IDD) = 450 mA

Figure 10. Gain vs. Frequency at Various Drain Currents (IDD)

Figure 11. Output Return Loss vs. Frequency at Various Temperatures,
Drain Current (IDD) = 450 mA

Figure 12. Gain vs. Frequency at Various Temperatures,
Drain Current (IDD) = 450 mA

Figure 13. Input Return Loss vs. Frequency at Various Temperatures,
Drain Current (IDD) = 450 mA

Figure 14. Reverse Isolation vs. Frequency at Various Temperatures,
Drain Current (IDD) = 450 mA
Figure 15. Output P1dB vs. Frequency at Various Temperatures, Drain Current (IDD) = 450 mA

Figure 16. PSAT vs. Frequency at Various Temperatures, Drain Current (IDD) = 450 mA

Figure 17. Output IP3 vs. Frequency at Various Temperatures, Drain Current (IDD) = 450 mA, POUT/Tone = 12 dBm

Figure 18. Output P1dB vs. Frequency at Various Drain Currents (IDD)

Figure 19. PSAT vs. Frequency at Various Drain Currents (IDD)

Figure 20. Output IP3 vs. Frequency at Various Drain Currents (IDD), POUT/Tone = 12 dBm
Figure 21. Output IP3 vs. Frequency at Various POUT/Tones, Drain Current (IDD) = 450 mA

Figure 22. Output IP3 vs. POUT/Tone at Various Drain Currents (IDD) at RF = 83.5 GHz

Figure 23. Gain, Output P1dB, and PSAT vs. Drain Current (IDD) at RF = 81 GHz

Figure 24. Output IP3 vs. POUT/Tone at Various Drain Currents (IDD) at RF = 81 GHz

Figure 25. Output IP3 vs. POUT/Tone at Various Drain Currents (IDD) at RF = 86 GHz

Figure 26. Gain, Output P1dB, and PSAT vs. Drain Current (IDD) at RF = 83.5 GHz
Figure 27. Gain, Output P1dB, and P_{SAT} vs. Drain Current (I_{DD}) at RF = 86 GHz

Figure 28. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power at RF = 83.5 GHz, Drain Current (I_{DD}) = 450 mA

Figure 29. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power at RF = 81 GHz, Drain Current (I_{DD}) = 450 mA

Figure 30. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power at RF = 81 GHz, Drain Current (I_{DD}) = 450 mA

Figure 31. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power at RF = 86 GHz, Drain Current (I_{DD}) = 450 mA

Figure 32. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power at RF = 83.5 GHz, Drain Current (I_{DD}) = 350 mA
**Figure 33.** $P_{\text{out}}$, Gain, PAE, and $I_{\text{dd}}$ vs. Input Power at RF = 86 GHz, Drain Current ($I_{\text{dd}}$) = 350 mA

**Figure 36.** Output IMD3 vs. $P_{\text{out}}$/Tone at Various Frequencies, Drain Current ($I_{\text{dd}}$) = 450 mA

**Figure 34.** Power Dissipation vs. Input Power at Various Frequencies, Drain Current ($I_{\text{dd}}$) = 450 mA, $T_A = 85^\circ$C

**Figure 37.** Power Dissipation vs. Input Power at Various Frequencies, Drain Current ($I_{\text{dd}}$) = 350 mA, $T_A = 85^\circ$C

**Figure 35.** Detector Output Voltage ($V_{\text{out}}$) vs. Output Power at Various Temperatures, Drain Current ($I_{\text{dd}}$) = 450 mA, RF = 81 GHz

**Figure 38.** Detector Output Voltage ($V_{\text{out}}$) vs. Output Power at Various Temperatures, Drain Current ($I_{\text{dd}}$) = 450 mA, RF = 86 GHz
THEORY OF OPERATION

The architecture of the HMC8142 power amplifier is shown in Figure 39. The HMC8142 uses four cascaded gain stages to form an amplifier with a combined gain of 21 dB and saturated output power ($P_{SAT}$) of 26 dBm. At the output of the last stage, a coupler taps off a small portion of the output signal. The coupled signal is presented to an on-chip diode detector for external monitoring of the output power. A matched reference diode is included to help correct for detector temperature dependencies. See the application circuit shown in Figure 40 for further details on biasing the different blocks and using the detector features.

Figure 39. Power Amplifier Circuit Architecture
APPLICATIONS INFORMATION
TYPICAL APPLICATION CIRCUIT

A typical application circuit for the HMC8142 is shown in Figure 40. Combine supply lines as shown in the application circuit schematic to minimize external component count and simplify power supply routing.

The HMC8142 uses several amplifier, detector, and attenuator stages. All stages use depletion mode pHEMT transistors. It is important to follow the following power-up bias sequence to ensure transistor damage does not occur.

1. Apply a −2 V bias to the VGG1 to VGG4 pads.
2. Apply 4 V to the VDD1 to VDD4 pads.
3. Adjust VGG1 to VGG4 between −2 V and 0 V to achieve a total amplifier drain current of 450 mA.

To power down the HMC8142, follow the procedure in reverse.

For additional guidance on general bias sequencing, see the MMIC Amplifier Biasing Procedure application note.

Figure 40. Typical Application Circuit
Figure 41. Assembly Diagram
MOUNTING AND BONDING TECHNIQUES FOR MILLIMETERWAVE GAAS MMICS

Attach the die directly to the ground plane eutectically or with conductive epoxy.

To bring RF to and from the chip, use 50 Ω microstrip transmission lines on 0.127 mm (5 mil) thick alumina thin film substrates (see Figure 42).

To minimize bond wire length, place microstrip substrates as close to the die as possible. The typical die to substrate spacing is 0.076 mm to 0.152 mm (3 mil to 6 mil).

HANDLING PRECAUTIONS

To avoid permanent damage, adhere to the precautions in the following sections.

Storage
All bare die ship in either waffle or gel-based ESD protective containers, sealed in an ESD protective bag. After opening the sealed ESD protective bag, all die must be stored in a dry nitrogen environment.

Cleanliness
Handle the chips in a clean environment. Never use liquid cleaning systems to clean the chip.

Static Sensitivity
Follow ESD precautions to protect against ESD strikes.

Transients
Suppress instrument and bias supply transients while bias is applied. To minimize inductive pickup, use shielded signal and bias cables.

General Handling
Handle the chip on the edges only using a vacuum collet or with a sharp pair of bent tweezers. Because the surface of the chip has fragile air bridges, never touch the surface of the chip with a vacuum collet, tweezers, or fingers.

MOUNTING

The chip is back metallized and can be die mounted with gold/tin (AuSn) eutectic preforms or with electrically conductive epoxy. The mounting surface must be clean and flat.

Eutectic Die Attach
It is best to use an 80% gold/20% tin preform with a work surface temperature of 255°C and a tool temperature of 265°C. When hot 90% nitrogen/10% hydrogen gas is applied, maintain tool tip temperature at 290°C. Do not expose the chip to a temperature greater than 320°C for more than 20 sec. No more than 3 sec of scrubbing is required for attachment.

Epoxy Die Attach
ABLETHERM 2600BT is recommended for die attachment. Apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip after placing it into position. Cure the epoxy per the schedule provided by the manufacturer.

WIRE BONDING

RF bonds made with 3 mil × 0.5 mil gold ribbon are recommended for the RF ports. These bonds must be thermosonically bonded with a force of 40 g to 60 g. DC bonds of 1 mil (0.025 mm) diameter, thermosonically bonded, are recommended. Create ball bonds with a force of 40 g to 50 g and wedge bonds with a force of 18 g to 22 g. Create all bonds with a nominal stage temperature of 150°C. Apply a minimum amount of ultrasonic energy to achieve reliable bonds. Keep all bonds as short as possible, less than 12 mil (0.31 mm).
OUTLINE DIMENSIONS

Figure 43. 25-Pad Bare Die [CHIP]
(C-25-2)
Dimensions shown in millimeters

ORDERING GUIDE

<table>
<thead>
<tr>
<th>Model</th>
<th>Temperature Range</th>
<th>Package Description</th>
<th>Package Option</th>
</tr>
</thead>
<tbody>
<tr>
<td>HMC8142</td>
<td>−55°C to +85°C</td>
<td>25-Pad Bare Die [CHIP]</td>
<td>C-25-2</td>
</tr>
<tr>
<td>HMC8142-SX</td>
<td>−55°C to +85°C</td>
<td>25-Pad Bare Die [CHIP]</td>
<td>C-25-2</td>
</tr>
</tbody>
</table>

1 The HMC8142-SX consists of two pairs of the die in a gel pack for sample orders.
2 This is a waffle pack option; contact Analog Devices, Inc., sales representatives for additional packaging options.