DDR5 SDRAM RDIMM Addendum

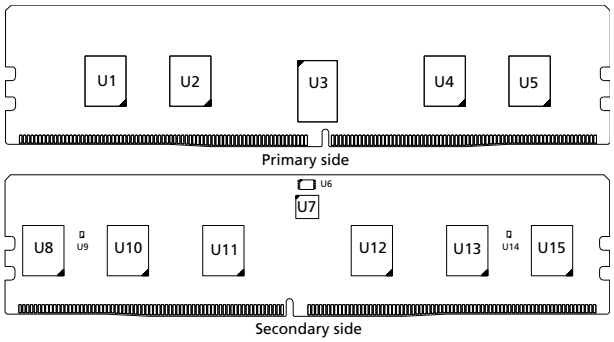
MTC10F1084S1RC – 16GB
16Gb Die Revision A

Features

Information provided here is in addition to or supersedes information provided in the Micron DDR5 RDIMM Core data sheet.

- DDR5 functionality and operations supported as defined in the component data sheet
- Features and specifications defined in the Micron DDR5 RDIMM core data sheet
- 288-pin, DDR5 registered dual in-line memory module (DDR5 RDIMM)
- Fast data transfer rate: PC5-4800
- 16GB (2Gig x 80)
- Single-rank
- 32 internal banks; 8 groups of 4 banks each

Figure 1: 288-Pin DDR5 RDIMM (R/C-D0)



Options — Marking

- Operating temperature
  - Commercial (0°C ≤ T_{OPER} ≤ 95°C) — C
- Frequency/CAS latency
  - 0.416ns @ CL = 40 (DDR5-4800) — 48B

Table 1: Addressing

Parameter	16GB
Row address[1]	64K (R0-R15)
Column address[1]	1K (C0-C9)
Device bank group address[1]	8 (BG0-BG2)
Device bank address per bank group[1]	4 (BA0-BA1)
Device configuration	16Gb (2Gb x 8), 32 banks
Module rank address	1 (CS0_n)

Notes: 1. These parameters represent the logical address state of the CA bus for different commands. Refer to the command truth table in the component data sheet.

Table 2: Part Numbers and Timing Parameters – 16GB Modules

Base device: MT60B2G8,[1] 16Gb DDR5 SDRAM Die Revision A

Part Number	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-$_n$RCD-$_n$RP)
MTC10F1084S1RC48BA1	16GB	2Gb x 80	38.4 GB/s	0.416ns/4800 MT/s	40-39-39

Notes: 1. The data sheet for the base device can be found on micron.com.

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DQ Map

Table 3: Component-to-Module DQ Map

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	9A	20	U2	0	25A	42
	1	10A	163		1	26A	185
	2	11A	165		2	27A	187
	3	8A	18		3	24A	40
	4	15A	172		4	31A	194
	5	12A	25		5	28A	47
	6	13A	27		6	29A	49
	7	14A	170		7	30A	192
U4	0	1B	102	U5	0	17B	124
	1	2B	245		1	18B	267
	2	3B	247		2	19B	269
	3	0B	100		3	16B	122
	4	7B	254		4	23B	276
	5	4B	107		5	20B	129
	6	5B	109		6	21B	131
	7	6B	252		7	22B	274
U8	0	26B	278	U10	0	10B	256
	1	25B	135		1	9B	113
	2	24B	133		2	8B	111
	3	27B	280		3	11B	258
	4	28B	140		4	12B	118
	5	31B	287		5	15B	265
	6	30B	285		6	14B	263
	7	29B	142		7	13B	120
U11	0	CB6B	234	U12	0	CB2A	196
	1	CB5B	91		1	CB1A	53
	2	CB4B	89		2	CB0A	51
	3	CB7B	236		3	CB3A	198
	4	CB0B	96		4	CB4A	58
	5	CB3B	243		5	CB7A	205
	6	CB2B	241		6	CB6A	203
	7	CB1B	98		7	CB5A	60

Table 3: Component-to-Module DQ Map (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U13	0	18A	174	U15	0	2A	152
	1	17A	31		1	1A	9
	2	16A	29		2	0A	7
	3	19A	176		3	3A	154
	4	20A	36		4	4A	14
	5	23A	183		5	7A	161
	6	22A	181		6	6A	159
	7	21A	38		7	5A	16

I_{DD} Specifications

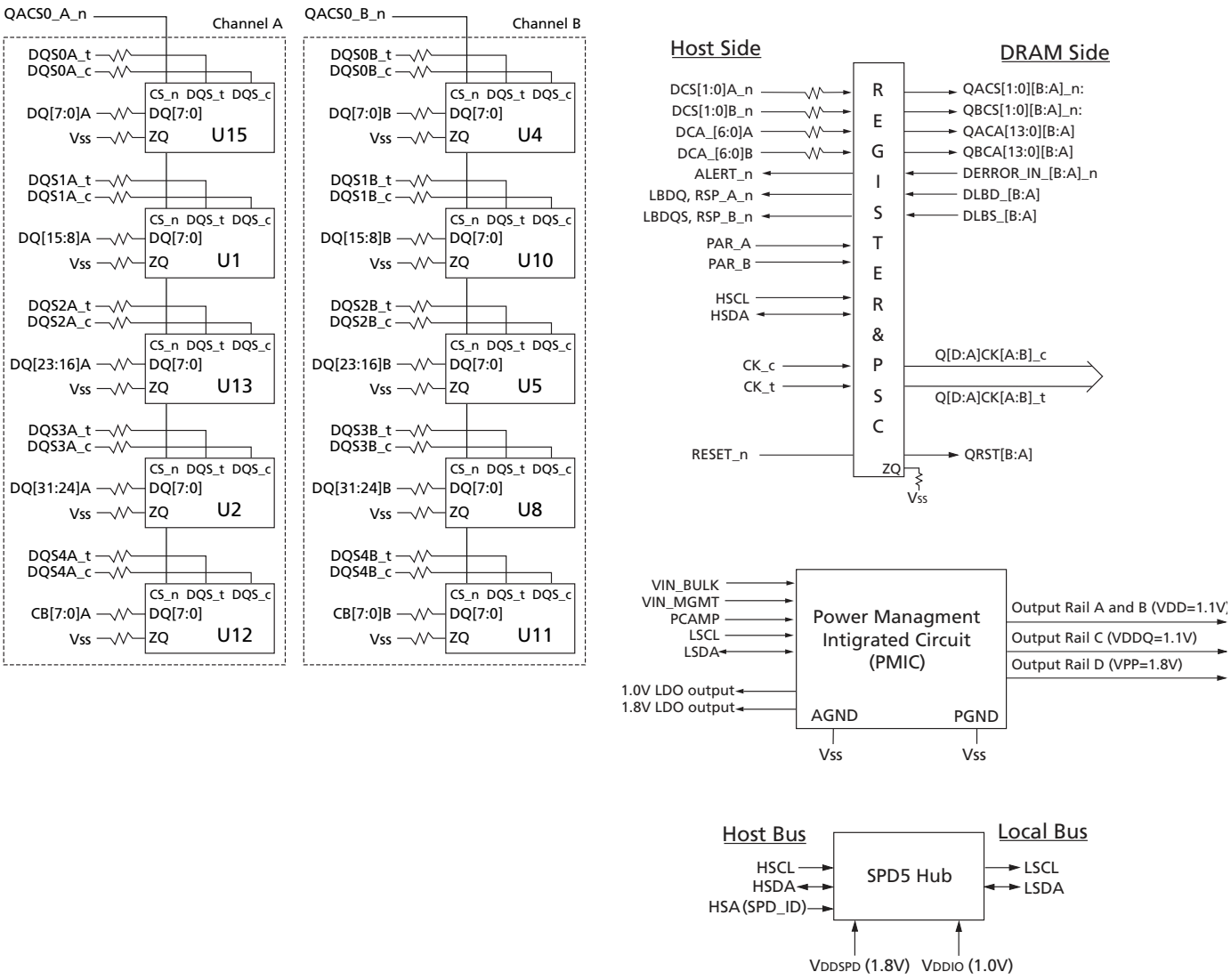
Table 4: DDR5 I_{DD} Specifications and Conditions – 16GB (Die Revision A)

Module I_{DD} is based on PMIC VIN_BULK 12V input current and typical operating range of temperature. Each I_{DD} parameter includes PMIC efficiency, RCD current and all DRAM current on all supplies (V_{DD}, V_{DDQ}, and V_{PP}).

Parameter	Symbol	4800	Units
Operating one bank ACTIVATE-PRECHARGE current	I_{DD0}	164	mA
Operating four bank ACTIVATE-PRECHARGE current	I_{DD0F}	213	mA
Precharge standby current	I_{DD2N}	147	mA
Precharge standby non-target command	I_{DD2NT}	246	mA
Precharge power-down current	I_{DD2P}	140	mA
Active standby current	I_{DD3N}	150	mA
Active power-down current	I_{DD3P}	144	mA
Operating burst read current	I_{DD4R}	460	mA
Operating burst write current	I_{DD4W}	578	mA
Operating burst write with write CRC current	I_{DD4WC}	536	mA
Burst refresh (normal refresh mode) current	I_{DD5B}	364	mA
Burst refresh (fine granularity refresh mode) current	I_{DD5F}	242	mA
Burst refresh (same bank refresh mode) current	I_{DD5C}	189	mA
Self refresh current	I_{DD6N}	64	mA
Operating bank interleave read current	I_{DD7}	499	mA
Maximum power saving deep power down mode current	I_{DD8}	72	mA

Functional Block Diagram

Figure 2: Functional Block Diagram



Notes: 1. The ZQ ball on each DDR5 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.
2. Functional block diagram is for reference only.

Revision History

Rev. E – 08/2021

- Production Release

Rev. D – 02/2021

- Preliminary Release

Rev. C – 01/2021

- Preliminary Release

Rev. B – 06/2020

- Preliminary Release

Rev. A – 06/2020

- Preliminary Release

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein.
Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.