

## Galvanic isolated octal high-side power solid state relay for high inductive loads



PowerSO-36

TFQFPN32



### Product status link

[ISO808](#)

[ISO808-1](#)

### Product label



## Features

- $V_{CC(AMR)} = 45\text{ V}$
- Wide process side op. range  $V_{CC} = 9.2\text{ to }36\text{ V}$
- $R_{DS(on)} = 0.125\ \Omega$  per channel (TYP)
- Fast demagnetization of inductive loads  $V_{DEMAG(TYP)} = V_{CC} - 54\text{ V}$
- Per channel process side op. current
  - ISO808/ISO808Q  $I_{OUT} < 0.7\text{ A}$
  - ISO808-1/ISO808Q-1  $I_{OUT} < 1\text{ A}$
- Low process and logic sides supply current
- Under-voltage shut down with auto restart and hysteresis
- Logic side 5 V and 3.3 V TTL/CMOS and MCU compatible I/Os
- Common output enable/disable pin
- Reset function for IC outputs disable
- High common mode transient immunity
- Short circuit protection on output channels
  - ISO808/ISO808Q  $I_{LIM(MIN)} = 0.7\text{ A}$
  - ISO808-1/ISO808Q-1  $I_{LIM(MIN)} = 1\text{ A}$
- Per-channel over-temperature protection with thermal independence of separate channels
- Case over-temperature protection
- Over-voltage protection ( $V_{CC}$  clamping)
- Loss of GND and  $V_{CC}$  protections
- Common fault open drain diagnostic
- Designed to meet IEC 61000-4-2, IEC 61000-4-4, IEC 61000-4-5 and IEC 61000-4-8
- UL1577 and UL508 certified
- Safety limits according to IEC 60747-17 (former VDE 0884-11)
- PowerSO-36 and TFQFPN32 Package

## Applications

- Programmable logic control
- Industrial PC peripheral input/output
- Numerical control machines
- Drivers for all type of loads (resistive, capacitive, inductive)

## Description

The ISO808, ISO808-1 (PowerSO-36) and ISO808Q, ISO808Q-1 (TFQFPN32) are galvanic isolated 8-channel drivers featuring a low supply current. Each driver contains 2 independent galvanic isolated voltage domains ( $V_{CC}$  and  $V_{DD}$  for the Process and Control Logic stages, respectively). The ICs are intended for driving any kind of load with one side connected to ground.

Active channel current limitation (OVL) combined with thermal shutdown (OVT), independent for each channel, protects the device against overload.

Built-in thermal shutdown protects each channel from overtemperature and overload: each overheated channel automatically turns OFF after its junction temperature triggers the protection threshold ( $T_{JSD}$ ). The channel turns back ON if its junction temperature decreases lower than restart threshold ( $T_{JR}$ ).

An additional case temperature sensor protects the whole chip against overtemperature (OVC event): if the case temperature triggers the  $T_{CSD}$  threshold then overloaded channels are turned OFF and restart only when case temperature decreased down to the reset threshold ( $T_{CR}$ ). Non overloaded channels continue to operate normally.

Other embedded functions are loss of ground protection,  $V_{CC}$  and  $V_{DD}$  UVLOs (with hysteresis), and watchdog.

An internal circuit provides an OR-wired not latched OVT that is reported on the common  $\overline{FAULT}$  indicator pin.  $\overline{FAULT}$  is an open drain, active low, fault indication pin.

The Synchronous Control Mode (by driving  $\overline{SYNC}$  and  $\overline{LOAD}$  pins independently) is used to reduce the jittering of the outputs and to drive at the same time the outputs of different devices.

## 1 Block diagram

Figure 1. Block diagram

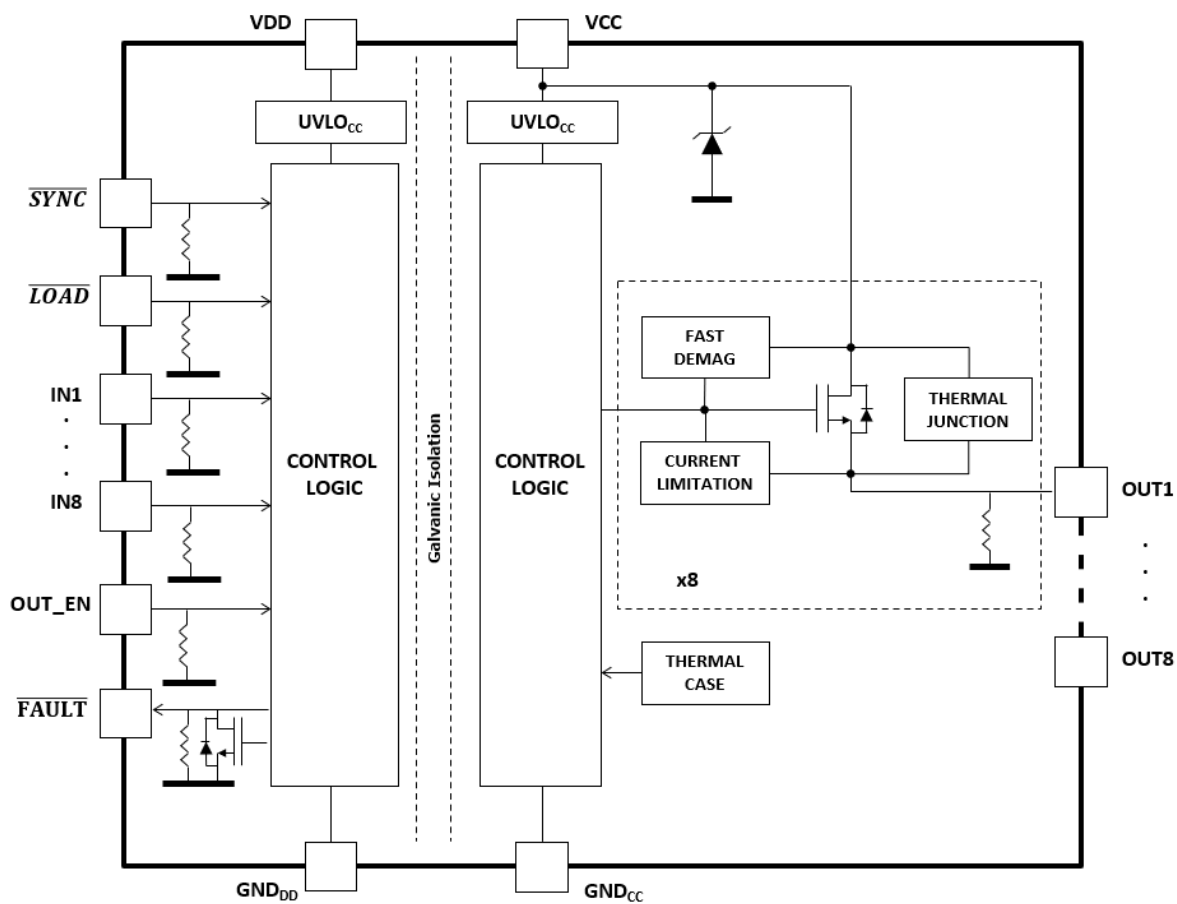




**Table 1. Pin description**

| Pin        |                         | Name                      | Description                                                                               |
|------------|-------------------------|---------------------------|-------------------------------------------------------------------------------------------|
| PowerSO-36 | TFQFPN32                |                           |                                                                                           |
| 1          | -                       | N.C.                      | Not connected                                                                             |
| 2          | 20                      | V <sub>DD</sub>           | Positive Control Logic Stage supply                                                       |
| 3          | 21                      | OUT_EN                    | Output enable                                                                             |
| 4          | 22                      | $\overline{\text{SYNC}}$  | Input to output synchronization signal, active low                                        |
| 5          | 23                      | $\overline{\text{LOAD}}$  | Load input data signal, active low                                                        |
| 6          | 24                      | IN1                       | Channel 1 input                                                                           |
| 7          | 25                      | IN2                       | Channel 2 input                                                                           |
| 8          | 26                      | IN3                       | Channel 3 input                                                                           |
| 9          | 27                      | IN4                       | Channel 4 input                                                                           |
| 10         | 28                      | IN5                       | Channel 5 input                                                                           |
| 11         | 29                      | IN6                       | Channel 6 input                                                                           |
| 12         | 30                      | IN7                       | Channel 7 input                                                                           |
| 13         | 31                      | IN8                       | Channel 8 input                                                                           |
| 14         | 32                      | $\overline{\text{FAULT}}$ | Common fault (OVT and Internal Communication Error) pin - active low                      |
| 15         | 1                       | GND <sub>DD</sub>         | Input logic ground, negative logic supply                                                 |
| 16         | -                       | NC                        | Not connected                                                                             |
| 17         | -                       | NC                        | Not connected                                                                             |
| 18         | 2                       | NC                        | Not connected                                                                             |
| 19         | 3                       | GND <sub>CC</sub>         | Output (process side) power ground                                                        |
| -          | TAB(GND <sub>CC</sub> ) | TAB(GND <sub>CC</sub> )   | Connect to GND <sub>CC</sub> on the application board                                     |
| 20         | -                       | NC                        | Not connected                                                                             |
| 21         | 4                       | OUT8                      | Channel 8 power output <sup>(1)</sup>                                                     |
| 22         | 5                       |                           |                                                                                           |
| 23         | 6                       | OUT7                      | Channel 7 power output <sup>(1)</sup>                                                     |
| 24         | 7                       |                           |                                                                                           |
| 25         | 8                       | OUT6                      | Channel 6 power output <sup>(1)</sup>                                                     |
| 26         | 9                       |                           |                                                                                           |
| 27         | 10                      | OUT5                      | Channel 5 power output <sup>(1)</sup>                                                     |
| 28         | 11                      |                           |                                                                                           |
| 29         | 12                      | OUT4                      | Channel 4 power output <sup>(1)</sup>                                                     |
| 30         | 13                      |                           |                                                                                           |
| 31         | 14                      | OUT3                      | Channel 3 power output <sup>(1)</sup>                                                     |
| 32         | 15                      |                           |                                                                                           |
| 33         | 16                      | OUT2                      | Channel 2 power output <sup>(1)</sup>                                                     |
| 34         | 17                      |                           |                                                                                           |
| 35         | 18                      | OUT1                      | Channel 1 power output <sup>(1)</sup>                                                     |
| 36         | 19                      |                           |                                                                                           |
| TAB        | TAB(V <sub>CC</sub> )   | V <sub>CC</sub>           | Exposed tab internally connected to V <sub>CC</sub> positive Process Stage supply voltage |

1. Connect the two pins on the same net of the application board

### 3 Absolute maximum ratings

**Table 2. Absolute maximum ratings**

| Symbol                        | Parameter                                                                                                                                       | Min. | Max.                              | Unit |
|-------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|------|-----------------------------------|------|
| V <sub>CC</sub>               | Process Stage supply voltage                                                                                                                    | -0.3 | +45                               | V    |
| V <sub>DD</sub>               | Control Logic Stage supply voltage                                                                                                              | -0.3 | +6                                | V    |
| V <sub>IN</sub>               | DC Input pins (IN <sub>X</sub> , $\overline{\text{LOAD}}$ , $\overline{\text{SYNC}}$ and OUT_EN) current                                        | -0.3 | V <sub>DD</sub>                   | V    |
| V <sub>FAULT</sub>            | $\overline{\text{FAULT}}$ pin voltage                                                                                                           | -0.3 | +6.0                              | V    |
| I <sub>GND<sub>DD</sub></sub> | DC digital ground Reverse Current                                                                                                               |      | -25                               | mA   |
| I <sub>OUT</sub>              | Channel Output Current (continuous)                                                                                                             |      | Internally limited                | A    |
| I <sub>GND<sub>CC</sub></sub> | DC Power Ground Reverse Current                                                                                                                 |      | -250                              | mA   |
| I <sub>RX</sub>               | Reverse Output Current (from OUTx pins to V <sub>CC</sub> )                                                                                     |      | -6 <sup>(1)</sup>                 | A    |
| I <sub>IN</sub>               | DC Input pins current (IN <sub>X</sub> , $\overline{\text{LOAD}}$ , $\overline{\text{SYNC}}$ and OUT_EN)                                        | -10  | +10                               | mA   |
| I <sub>FAULT</sub>            | $\overline{\text{FAULT}}$ pin current                                                                                                           | -10  | +10                               | mA   |
| V <sub>ESD</sub>              | Electrostatic discharge with Human Body Model (R = 1.5 K $\Omega$ ; C = 100 pF)                                                                 |      | 2000                              | V    |
| V <sub>IO</sub>               | Isolation DC voltage applied between GND <sub>DD</sub> and GND <sub>CC</sub> pins for PowerSO-36                                                |      | 180                               | V    |
|                               | Isolation DC voltage applied between GND <sub>DD</sub> and GND <sub>CC</sub> pins for TFQFPN32                                                  |      | 75                                |      |
| EAS                           | Single pulse avalanche energy per channel, all channels driven simultaneously @T <sub>AMB</sub> = 125 °C, I <sub>OUT</sub> = 0.6 A (PowerSO-36) |      | 2.11                              | J    |
|                               | Single pulse avalanche energy per channel, all channels driven simultaneously @T <sub>AMB</sub> = 125 °C, I <sub>OUT</sub> = 0.6 A (TFQFPN32)   |      | 0.48                              |      |
| P <sub>TOT</sub>              | Power dissipation                                                                                                                               |      | Internally limited <sup>(2)</sup> | W    |
| T <sub>J</sub>                | Junction operating temperature                                                                                                                  |      | Internally limited <sup>(2)</sup> | °C   |
| T <sub>STG</sub>              | Storage temperature                                                                                                                             |      | -40 to 150                        | °C   |

1. this value is intended with each couple of OUTx pins shorted on the application board
2. Protection functions are intended to avoid IC damage in fault conditions and are not intended for continuous operation. Continuous or repetitive operation of protection functions may reduce the IC lifetime.

## 4 Thermal data

**Table 3. Thermal data**

| Symbol           | Parameter                                              | Max. value          |                   | Unit |
|------------------|--------------------------------------------------------|---------------------|-------------------|------|
|                  |                                                        | PowerSO-36          | TFQFPN32          |      |
| $R_{th\ j-case}$ | Thermal resistance, junction-to-case <sup>(1)</sup>    | 0.8                 | 1                 | °C/W |
| $R_{th\ j-amb}$  | Thermal resistance, junction-to-ambient <sup>(2)</sup> | 16.9 <sup>(3)</sup> | 25 <sup>(4)</sup> |      |

1.  $R_{th}$  between the die and the bottom case surface measured by cold plate as per JESD51-12.

2. JESD51-7.

3. Maximum power dissipation = 3.8W (@ $T_{amb} = 85^{\circ}C$ ,  $T_J < 150^{\circ}C$ )

4. Maximum power dissipation = 2.6W (@ $T_{amb} = 85^{\circ}C$ ,  $T_J < 150^{\circ}C$ )

## 5 Electrical characteristics

9.2 V ≤ V<sub>CC</sub> ≤ 36 V; 2.75 V ≤ V<sub>DD</sub> ≤ 5.5 V; -40 °C < T<sub>J</sub> < 125 °C, unless otherwise specified.

**Table 4. Power section**

| Symbol                 | Parameter                                       | Test conditions                                                    | Min. | Typ.  | Max. | Unit |
|------------------------|-------------------------------------------------|--------------------------------------------------------------------|------|-------|------|------|
| V <sub>CC</sub>        | Operating voltage range                         |                                                                    | 9.2  |       | 36   | V    |
| V <sub>CC(THON)</sub>  | V <sub>CC</sub> undervoltage turn-on threshold  | V <sub>DD</sub> = 3.3 V, V <sub>CC</sub> increasing                |      | 8.4   | 9.2  | V    |
| V <sub>CC(THOFF)</sub> | V <sub>CC</sub> undervoltage turn-off threshold | V <sub>DD</sub> = 3.3 V, V <sub>CC</sub> decreasing                | 7.7  | 8.1   |      | V    |
| V <sub>CC(HYS)</sub>   | V <sub>CC</sub> undervoltage hysteresis         |                                                                    |      | 0.15  |      | V    |
| V <sub>CCclamp</sub>   | Clamp on VCC pin                                | I <sub>clamp</sub> = 20 mA                                         | 47   | 52    | 57   | V    |
| R <sub>DS(ON)</sub>    | ON-state resistance (see Figure 4)              | I <sub>OUT</sub> = 0.5 A, T <sub>J</sub> = 25 °C                   |      | 0.125 | 0.16 | Ω    |
|                        |                                                 | I <sub>OUT</sub> = 0.5 A, T <sub>J</sub> = 125 °C                  |      |       | 0.26 |      |
| I <sub>CC</sub>        | Power supply current                            | All channels in OFF-state, V <sub>CC</sub> = 36 V                  |      | 5.5   |      | mA   |
|                        |                                                 | All channels in ON-state, V <sub>CC</sub> = 36 V                   |      | 16    |      |      |
| I <sub>LGND</sub>      | Ground disconnection output current             | V <sub>CC</sub> = V <sub>GND</sub> = 0 V, V <sub>OUT</sub> = -24 V |      |       | 500  | μA   |
| V <sub>OUT(OFF)</sub>  | OFF-state output voltage                        | Channel OFF and I <sub>OUT</sub> = 0 A                             |      |       | 3    | V    |
| I <sub>OUT(OFF)</sub>  | OFF-state output current                        | Channel OFF and V <sub>OUT</sub> = 0 V                             |      |       | 5    | μA   |

**Table 5. Digital supply voltage**

| Symbol                 | Parameter                                       | Test conditions                                                     | Min. | Typ. | Max. | Unit |
|------------------------|-------------------------------------------------|---------------------------------------------------------------------|------|------|------|------|
| V <sub>DD</sub>        | Operating voltage range                         |                                                                     | 2.75 |      | 5.5  | V    |
| V <sub>DD(THON)</sub>  | V <sub>DD</sub> undervoltage turn-on threshold  | V <sub>CC</sub> = 24 V, V <sub>DD</sub> increasing                  | 2.55 |      | 2.75 | V    |
| V <sub>DD(THOFF)</sub> | V <sub>DD</sub> undervoltage turn-off threshold | V <sub>CC</sub> = 24V, V <sub>DD</sub> decreasing                   | 2.45 |      | 2.65 | V    |
| V <sub>DD(HYS)</sub>   | V <sub>DD</sub> undervoltage hysteresis         |                                                                     | 0.04 | 0.1  |      | V    |
| I <sub>DD</sub>        | V <sub>DD</sub> supply current                  | V <sub>DD</sub> = 5 V and input channel with a steady logic level   |      | 4.5  | 6    | mA   |
|                        |                                                 | V <sub>DD</sub> = 3.3 V and input channel with a steady logic level |      | 4.4  | 5.9  | mA   |

**Table 6. Diagnostic pin and output protection function**

| Symbol              | Parameter                                   |                     | Test conditions                                     | Min.                | Typ.                | Max.                | Unit |
|---------------------|---------------------------------------------|---------------------|-----------------------------------------------------|---------------------|---------------------|---------------------|------|
| V <sub>FAULT</sub>  | FAULT pin open drain voltage output low     |                     | I <sub>FAULT</sub> = 5 mA                           |                     |                     | 0.4                 | V    |
| I <sub>LFAULT</sub> | FAULT output leakage current                |                     | V <sub>FAULT</sub> = 5 V                            |                     |                     | 1                   | μA   |
| I <sub>PEAK</sub>   | Maximum DC output current before limitation |                     | V <sub>CC</sub> = 24 V; R <sub>LOAD</sub> = 0 Ω     |                     |                     | 2.3                 | A    |
| I <sub>LIM</sub>    | Short-circuit current limitation            | ISO808, ISO808Q     |                                                     | 0.7                 | 1.9                 | A                   |      |
|                     |                                             | ISO808-1, ISO808Q-1 |                                                     | 1                   |                     |                     |      |
| Hyst                | I <sub>LIM</sub> tracking limits            |                     |                                                     |                     | 0.3                 |                     | A    |
| T <sub>JSD</sub>    | Junction shutdown temperature               |                     |                                                     | 150                 | 175                 | 200                 | °C   |
| T <sub>JR</sub>     | Junction reset temperature                  |                     |                                                     |                     | 150                 |                     | °C   |
| T <sub>JHYST</sub>  | Junction thermal hysteresis                 |                     |                                                     |                     | 15                  |                     | °C   |
| T <sub>CSD</sub>    | Case shutdown temperature                   |                     |                                                     | 125                 | 130                 | 135                 | °C   |
| T <sub>CR</sub>     | Case reset temperature                      |                     |                                                     |                     | 115                 |                     | °C   |
| T <sub>CHYST</sub>  | Case thermal hysteresis                     |                     |                                                     |                     | 15                  |                     | °C   |
| V <sub>DEMAG</sub>  | Output voltage at turn-off                  |                     | I <sub>OUT</sub> = 0.5 A; I <sub>LOAD</sub> >= 1 mH | V <sub>CC</sub> -50 | V <sub>CC</sub> -54 | V <sub>CC</sub> -58 | V    |

**Table 7. Power switching characteristics ( $V_{\text{CC}} = 24 \text{ V}; R_{\text{LOAD}} = 48 \Omega; -40^{\circ}\text{C} < T_{\text{J}} < 125^{\circ}\text{C}$ )**

| Symbol                         | Parameter                | Test conditions           | Min. | Typ. | Max. | Unit                   |
|--------------------------------|--------------------------|---------------------------|------|------|------|------------------------|
| $dV/dt(\text{ON})$             | Turn-on voltage slope    | (see Figure 5)            |      | 0.7  |      | $\text{V}/\mu\text{s}$ |
| $t_{\text{r}}$                 | Rise time                |                           |      | 19   | 32   | $\mu\text{s}$          |
| $dV/dt(\text{OFF})$            | Turn-off voltage slope   |                           |      | 1.5  |      | $\text{V}/\mu\text{s}$ |
| $t_{\text{f}}$                 | Fall time                |                           |      | 7    | 23   | $\mu\text{s}$          |
| $t_{\text{d}}(\text{ON})$      | Turn-ON delay time       | (see Figure 6, Figure 7)  |      | 15   | 24   | $\mu\text{s}$          |
| $t_{\text{d}}(\text{OFF})$     | Turn-OFF delay time      |                           |      | 43   | 80   | $\mu\text{s}$          |
| $t_{\text{w}}(\text{OUT\_EN})$ | OUT_EN pulse width       | (see Figure 9, Figure 10) | 150  |      |      | ns                     |
| $t_{\text{p}}(\text{OUT\_EN})$ | OUT_EN propagation delay |                           |      | 40   | 80   | $\mu\text{s}$          |

Figure 4.  $R_{DS(on)}$  measurement

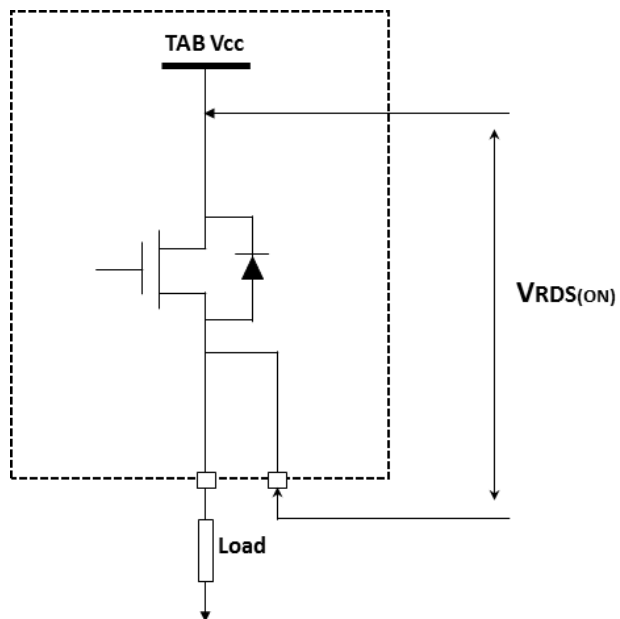


Figure 5.  $dV/dT$  definition

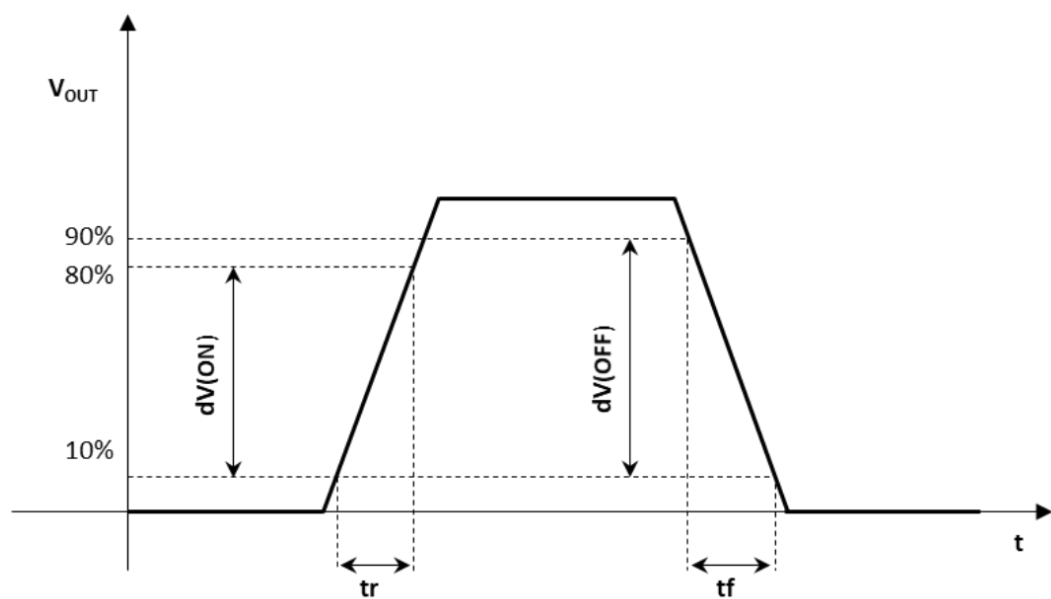


Figure 6.  $t_d(\text{ON})$ - $t_d(\text{OFF})$  Synchronous Control Mode (SCM)

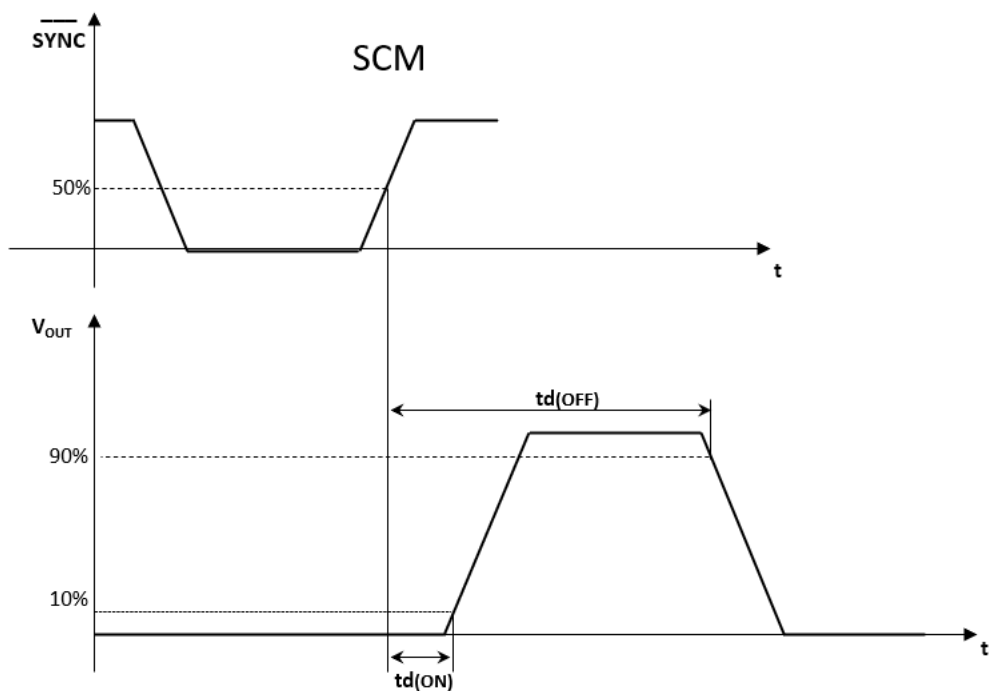


Figure 7.  $t_d(\text{ON})$ - $t_d(\text{OFF})$  Direct Control Mode (DCM)

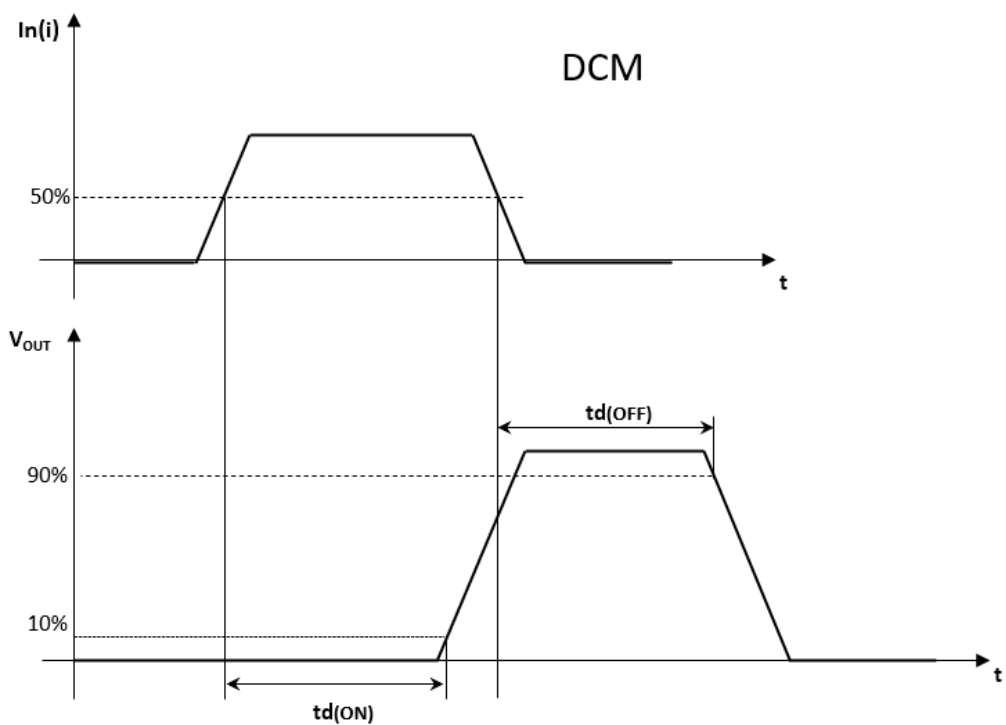


**Table 8. Logic inputs and output**

| Symbol        | Parameter                                                                       | Test conditions       | Min.                | Typ. | Max.                | Unit          |
|---------------|---------------------------------------------------------------------------------|-----------------------|---------------------|------|---------------------|---------------|
| $V_{IL}$      | $\overline{LOAD}$ , $\overline{SYNC}$ , $IN_X$ and $OUT\_EN$ low level voltage  |                       | -0.3                |      | $0.3 \times V_{DD}$ | V             |
| $V_{IH}$      | $\overline{LOAD}$ , $\overline{SYNC}$ , $IN_X$ and $OUT\_EN$ high level voltage |                       | $0.7 \times V_{DD}$ |      | $V_{DD} + 0.3$      | V             |
| $V_{I(HYST)}$ | $\overline{LOAD}$ , $\overline{SYNC}$ , $IN_X$ and $OUT\_EN$ hysteresis voltage | $V_{DD} = 5\text{ V}$ |                     | 100  |                     | mV            |
| $I_{IN}$      | $\overline{LOAD}$ , $\overline{SYNC}$ , $IN_X$ and $OUT\_EN$ current            | $V_{IN} = 5\text{ V}$ | 10                  | 55   | 90                  | $\mu\text{A}$ |

**Table 9. Parallel interface timings ( $V_{DD} = 5\text{ V}$ ;  $V_{CC} = 24\text{ V}$ ;  $-40\text{ }^\circ\text{C} < T_J < 125\text{ }^\circ\text{C}$ )**

| Symbol            | Parameter                                          | Test conditions                                                         | Min. | Typ. | Max. | Unit          |
|-------------------|----------------------------------------------------|-------------------------------------------------------------------------|------|------|------|---------------|
| $t_{dis(SYNC)}$   | $\overline{SYNC}$ disable time                     | Sync. control mode                                                      | 10   |      |      | $\mu\text{s}$ |
| $t_{dis(DCM)}$    | $\overline{SYNC}$ , $\overline{LOAD}$ disable time | Direct control mode                                                     | 80   |      |      | ns            |
| $t_w(SYNC)$       | $\overline{SYNC}$ negative pulse width             | Sync. control mode                                                      | 20   |      | 195  | $\mu\text{s}$ |
| $t_{su(LOAD)}$    | $\overline{LOAD}$ setup time                       | Sync. control mode                                                      | 80   |      |      | ns            |
| $t_h(LOAD)$       | $\overline{LOAD}$ hold time                        | Sync. control mode                                                      | 400  |      |      | ns            |
| $t_w(LOAD)$       | $\overline{LOAD}$ pulse width                      | Sync. control mode                                                      | 240  |      |      | ns            |
| $t_{su(IN)}$      | Input setup time                                   |                                                                         | 80   |      |      | ns            |
| $t_h(IN)$         | Input hold time                                    |                                                                         | 10   |      |      | ns            |
| $t_w(IN)$         | Input pulse width                                  | Sync. control mode                                                      | 160  |      |      | ns            |
|                   |                                                    | Direct control mode                                                     | 20   |      |      | $\mu\text{s}$ |
| $t_{INLD}$        | IN to $\overline{LOAD}$ time                       | Direct control mode from IN variation to $\overline{LOAD}$ falling edge | 80   |      |      | ns            |
| $t_{LDIN}$        | $\overline{LOAD}$ to IN time                       | Direct control mode from $\overline{LOAD}$ falling edge to IN variation | 400  |      |      | ns            |
| $t_{jitter(SCM)}$ | Jitter on single channel                           | Sync. control mode                                                      |      |      | 6    | $\mu\text{s}$ |
| $t_{jitter(DCM)}$ |                                                    | Direct control mode                                                     |      |      | 20   |               |

**Table 10. Internal communication timings ( $V_{DD} = 5\text{ V}$ ;  $V_{CC} = 24\text{ V}$ ;  $-40\text{ }^\circ\text{C} < T_J < 125\text{ }^\circ\text{C}$ )**

| Symbol        | Parameter     | Test condition | Min. | Typ. | Max. | Unit          |
|---------------|---------------|----------------|------|------|------|---------------|
| $f_{refresh}$ | Refresh delay |                |      | 15   |      | kHz           |
| $t_{WD}$      | Watchdog time |                | 272  | 320  | 400  | $\mu\text{s}$ |

**Table 11. Insulation and safety-related specifications**

| Symbol             | Parameter                                        | Test conditions                                                                      | Value      |          | Unit |
|--------------------|--------------------------------------------------|--------------------------------------------------------------------------------------|------------|----------|------|
|                    |                                                  |                                                                                      | PowerSO 36 | TFQFPN32 |      |
| CLR <sup>(1)</sup> | Clearance (minimum external air gap)             | Measured from input terminals to output terminals, shortest distance through air     | 2.6        | 3.3      | mm   |
| CPG <sup>(1)</sup> | Creepage (minimum external tracking)             | Measured from input terminals to output terminals, shortest distance path along body | 2.6        | 3.3      | mm   |
| CTI <sup>(2)</sup> | Comparative tracking index (tracking resistance) |                                                                                      | ≥400       | ≥600     | V    |
|                    | Isolation group                                  | Material group                                                                       | II         | I        | -    |

1. Creepage and clearance requirements should be applied according to the specific equipment isolation standard of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the PCB do not reduce this distance.
2. When high voltage is applied across the isolator, electric discharges on or close to the surface of the package, can cause localized deterioration in the mold compound, resulting in a partially conducting path from one side of the isolator to the other. This phenomenon is called tracking. The ability of a material to withstand tracking is quantified by a comparative tracking index (CTI). Using a mold compound with a higher CTI allows the use of smaller packages and saves board space.

**Table 12. Insulation characteristics**

| Symbol                          | Parameter                        | Test condition                                                                      | Value            |                  | Unit                                |
|---------------------------------|----------------------------------|-------------------------------------------------------------------------------------|------------------|------------------|-------------------------------------|
|                                 |                                  |                                                                                     | PowerSO 36       | TFQFPN32         |                                     |
| In accordance with IEC 60747-17 |                                  |                                                                                     |                  |                  |                                     |
| V <sub>PR</sub>                 | Input-to-output test voltage     | Method a, type test,<br>t <sub>m</sub> = 10 s<br>partial discharge < 5 pC           | 1500             | 1500             | V <sub>PEAK</sub>                   |
|                                 |                                  | Method b, 100% production test,<br>t <sub>m</sub> = 1 s<br>partial discharge < 5 pC | 1758             | 1758             | V <sub>PEAK</sub>                   |
| V <sub>IOTM</sub>               | Transient overvoltage            | Type test; t <sub>ini</sub> = 60 s                                                  | 3537             | 4245             | V <sub>PEAK</sub>                   |
| V <sub>IOSM</sub>               | Maximum surge insulation voltage | Type test                                                                           | 3537             | 4245             | V <sub>PEAK</sub>                   |
| R <sub>IO</sub>                 | Insulation resistance            | Type test<br>V <sub>IO</sub> = 500 V, T <sub>STG</sub> = 60 s                       | >10 <sup>9</sup> | >10 <sup>9</sup> | Ω                                   |
| UL1577                          |                                  |                                                                                     |                  |                  |                                     |
| V <sub>ISO</sub>                | Insulation withstand voltage     | 1 min. type test                                                                    | 2000/2830        | 2500/3536        | V <sub>RMS</sub> /V <sub>PEAK</sub> |
| V <sub>ISO test</sub>           | Insulation withstand test        | 1 s 100% production                                                                 | 2500/3537        | 3000/4245        | V <sub>RMS</sub> /V <sub>PEAK</sub> |
| Common Mode Transient Immunity  |                                  |                                                                                     |                  |                  |                                     |
| dV <sub>ISO</sub> /dt           | CMTI                             | Type test at V <sub>CM</sub> = 500 V                                                | ±25              | ±25              | V/ns                                |

**Table 13. Safety limits**

| Symbol                             | Parameter                                   | Test conditions                                                                                                         | Value | Unit |
|------------------------------------|---------------------------------------------|-------------------------------------------------------------------------------------------------------------------------|-------|------|
| <b>Input safety, Logic side</b>    |                                             |                                                                                                                         |       |      |
| $T_{SI}$                           | Safety temperature of Logic side            | -                                                                                                                       | 150   | °C   |
| $P_{SI}$                           | Safety power of Logic side <sup>(1)</sup>   | $V_{DD} \leq 6.0 \text{ V}$ , $V_{LOGIC(x)} \leq 6.0 \text{ V}$ , $I_{LOGIC(x)} \leq 10 \text{ mA}$ , $T_J \leq T_{SI}$ | 0.9   | W    |
| <b>Output safety, Process side</b> |                                             |                                                                                                                         |       |      |
| $T_{SO}$                           | Safety temperature of Process side          | -                                                                                                                       | 150   | °C   |
| $P_{SO}$                           | Safety power of Process side <sup>(1)</sup> | $V_{CC} \leq 36 \text{ V}$ , $I_{OUT(x)} \leq 1.5 \text{ A}$ , $T_J \leq T_{SO}$                                        | 5     | W    |

1. The above limits are measured according to IEC 60747-17. Respecting the above limits prevents potential damage to the isolation barrier upon failure on logic or process side circuitry. The user should apply these values to protect the IC and ensure the safety of the embedded isolation barrier. LOGIC(x) stands for any pin on the logic side; OUT(x) stands for any of the 8 output pins on the process side.

## 6 Functional description

### 6.1 Parallel interface

The integrated smart parallel interface offers three interfacing signals easily managed by a micro-controller. The  $\overline{\text{LOAD}}$  signal enables the input buffer storing the value of the channel inputs. The  $\overline{\text{SYNC}}$  signal copies the input buffer value into the transmission buffer and manages the synchronization between low voltage side and the channel outputs on the isolated side.

The  $\text{OUT\_EN}$  signal enables the channel outputs. An internal refresh signal updates the configuration of the channel outputs with a  $f_{\text{refresh}}$  frequency. This signal can be disabled forcing low the  $\overline{\text{SYNC}}$  input when  $\overline{\text{LOAD}}$  is high.  $\overline{\text{SYNC}}$  and  $\overline{\text{LOAD}}$  pins can be in direct control mode (DCM) or synchronous mode (SCM).

#### 6.1.1 Input signals (IN1 to IN8)

Inputs from IN1 to IN8 are the driving signals of the corresponding OUT1 to OUT8 outputs. Data are directly loaded on related outputs if  $\overline{\text{SYNC}}$  and  $\overline{\text{LOAD}}$  inputs are low (DCM operation) or stored into input buffer when  $\overline{\text{LOAD}}$  is low, and  $\overline{\text{SYNC}}$  is high.

#### 6.1.2 Load input data ( $\overline{\text{LOAD}}$ )

The input is active low; it stores the data from IN1 to IN8 into the input buffer

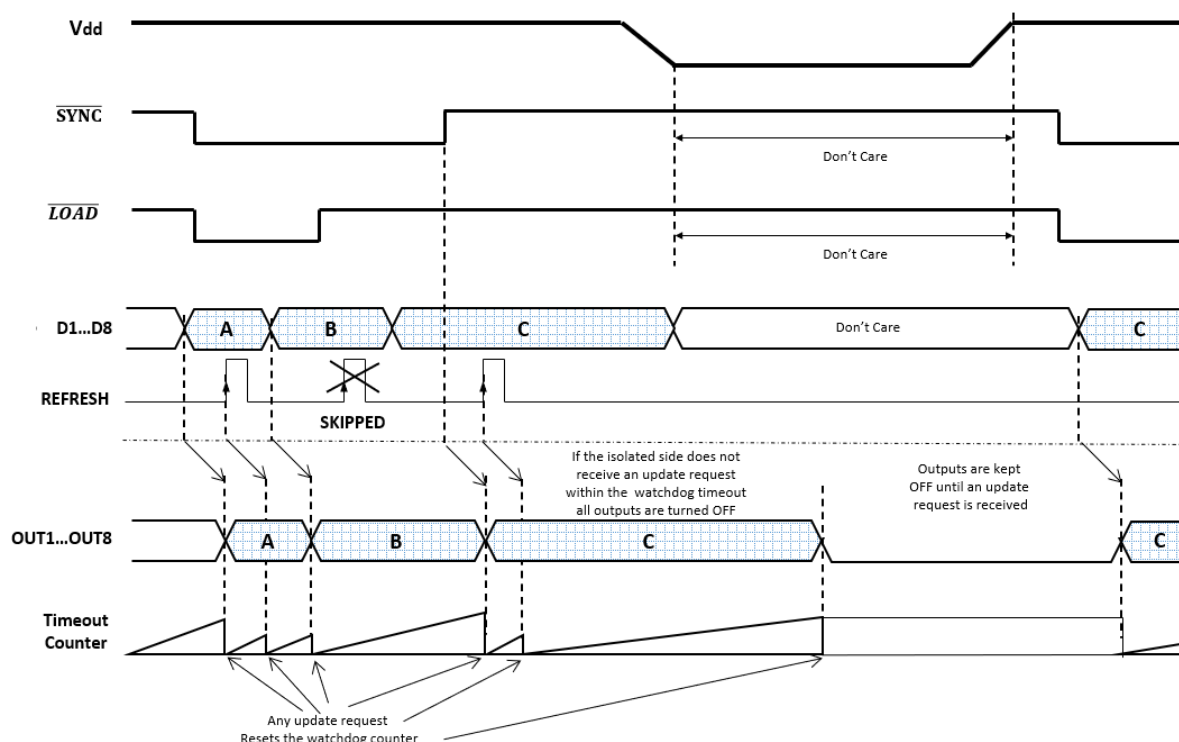
#### 6.1.3 Output synchronization ( $\overline{\text{SYNC}}$ )

The input is active low; it enables the integrated transmission buffer loading input buffer data and manages the transmission between the two isolated sides of the device.

### 6.1.4 Watchdog

The IC is composed by two chips (Logic Stage and Process Stage) supplied by two independent and galvanic isolated sources ( $V_{DD}/GND_{DD}$  and  $V_{CC}/GND_{CC}$  pins, respectively). The IC provides a watchdog function in order to guarantee a safe condition for the Process Stage when  $V_{DD}$  (or  $GND_{DD}$ ) supply voltage is missing. If the Logic Stage does not update the output status within  $t_{WD}$ , all the outputs of the Process Stage are disabled until a new update request is received. The Logic Stage chip periodically sends a refresh signal to the Process Stage chip. The refresh signal is also considered a valid update signal to reset the timeout counter on the Process Stage, so the isolated side watchdog does not protect the system from a failure of the host controller (e.g., MCU freezing).

**Figure 8. Watchdog behavior**



### 6.1.5 Output enable (OUT\_EN)

This pin provides a fast way to disable all the outputs simultaneously. When the OUT\_EN pin is driven low for at least  $t_{W(OUT\_EN)}$ , all eight outputs are disabled. This timing execution is compatible with an external reset push from the operator, safety requirements, and permits, in a PLC system, a micro-controller polling for obtain all internal information during a reset procedure.

**Figure 9. OUT\_EN without effect on output**

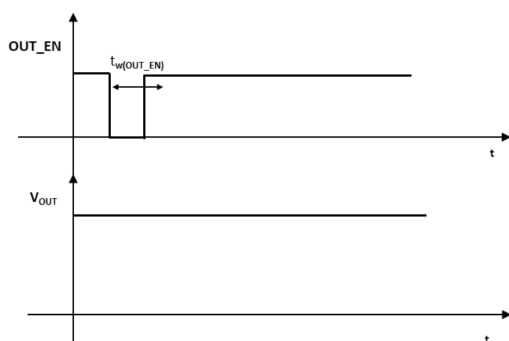
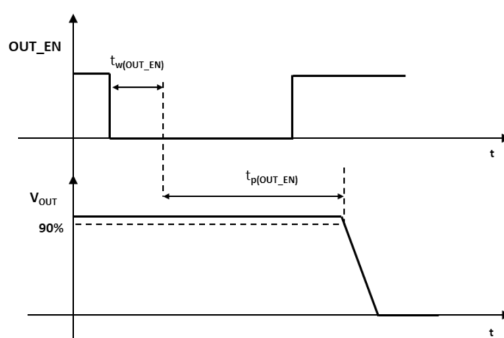


**Figure 10. OUT\_EN effective on output channel**



## 6.2 Direct Control Mode (DCM)

When  $\overline{\text{SYNC}}$  and  $\overline{\text{LOAD}}$  inputs are driven by the same signal, the device operates in direct control mode (DCM). In DCM the  $\overline{\text{SYNC}}$  /  $\overline{\text{LOAD}}$  signal operates as an active low input enable:

- When the signal is high, the current output configuration is kept regardless the input values
- When the signal is low, each channel input directly drives the respective output

This operation mode can also be set shorting both signals to the digital ground; in this case the channel outputs are always directly driven by the inputs except when  $\text{OUT\_EN}$  is low (outputs disabled).

**Table 14. Interface signal operation in DCM**

| $\overline{\text{SYNC}} / \overline{\text{LOAD}}$ | $\text{OUT\_EN}$   | Device behavior                       |
|---------------------------------------------------|--------------------|---------------------------------------|
| Don't care                                        | Low <sup>(1)</sup> | The outputs are disabled (turned off) |
| High                                              | High               | The outputs are left unchanged        |
| Low                                               | High               | The channel inputs drive the outputs  |

1. The outputs are turned off on  $\text{OUT\_EN}$  falling edge and they are kept disabled as long as it is low

**Figure 11. Direct Control Mode, IC configurations**

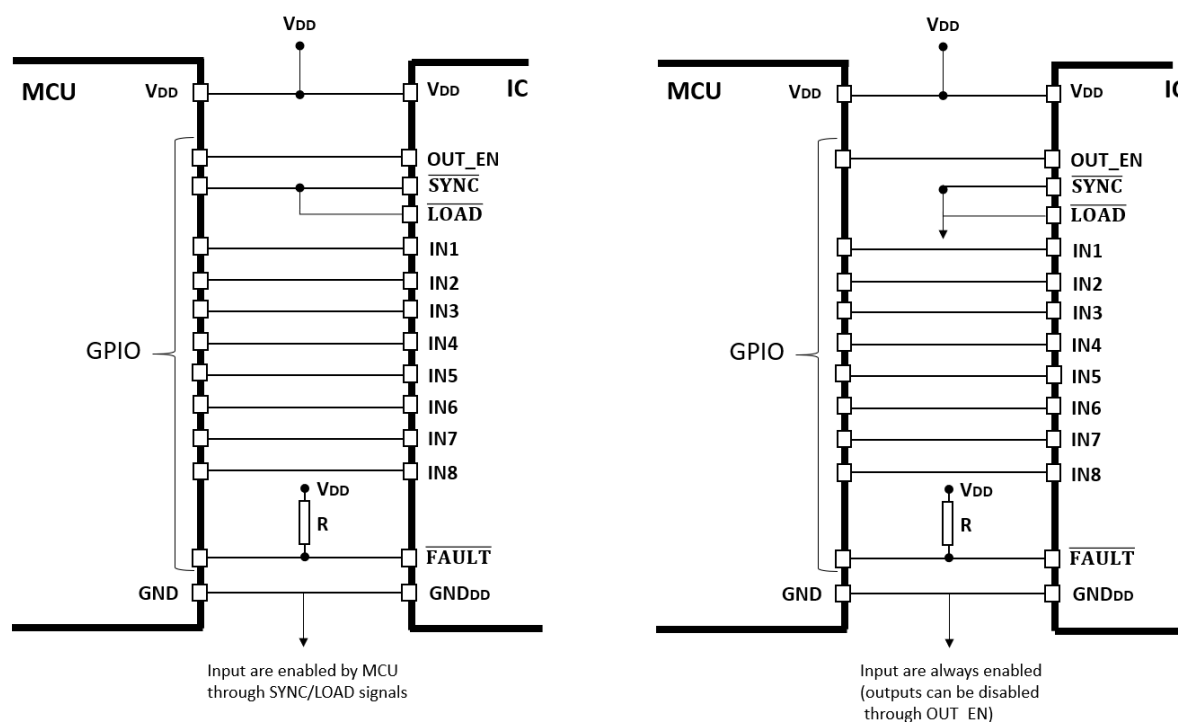
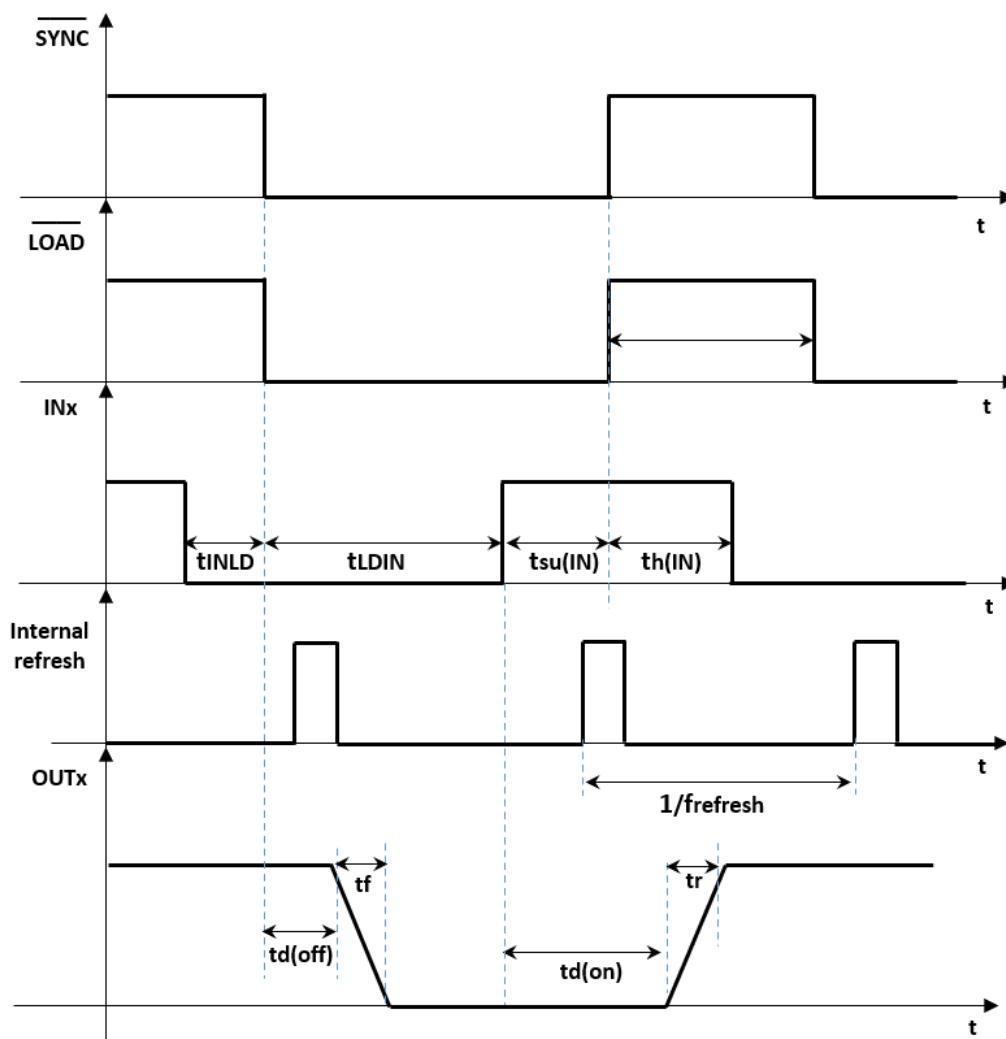


**Figure 12. Direct Control Mode, time diagram**


### 6.3 Synchronous control mode (SCM)

When  $\overline{SYNC}$  and  $\overline{LOAD}$  inputs are independently driven, the device can operate in synchronous control mode (SCM). The SCM is used to reduce the jittering of the outputs and to drive all outputs of different devices at the same time. In SCM the  $\overline{LOAD}$  signal is forced low to update the input buffer while the SYNC signal is high. The  $\overline{LOAD}$  signal is raised and the SYNC one is forced low for at least  $t_{SYNC(SCM)}$ . During this period, the internal refresh is disabled and any pending transmission between the low voltage and the isolated side is completed. When the  $\overline{SYNC}$  signal is raised the channel output configuration is changed according to the one stored in the input. If the  $t_{SYNC(SCM)}$  limit is met, the maximum jitter of the channel outputs is  $t_{jitter(SCM)}$ . If more devices share the same  $\overline{SYNC}$  signal, all device outputs change simultaneously with a maximum jitter related to maximum delay and maximum jitter for single device.

**Table 15. Interface signal operation in synchronous mode**

| LOAD       | SYNC       | OUT_EN             | Device behavior                                                                                                |
|------------|------------|--------------------|----------------------------------------------------------------------------------------------------------------|
| Don't care | Don't care | Low <sup>(1)</sup> | The outputs are disabled (turned off)                                                                          |
| High       | High       | High               | The outputs are left unchanged                                                                                 |
| Low        | High       | High               | The input buffer is enabled, the outputs are left unchanged                                                    |
| High       | Low        | High               | The internal refresh signal is disabled, the transmission buffer is updated and the outputs are left unchanged |
| Low        | Low        | High               | Should be avoided (DCM operation only)                                                                         |

1. The outputs are turned off on OUT\_EN falling edge and they are kept disabled as long as it is low.

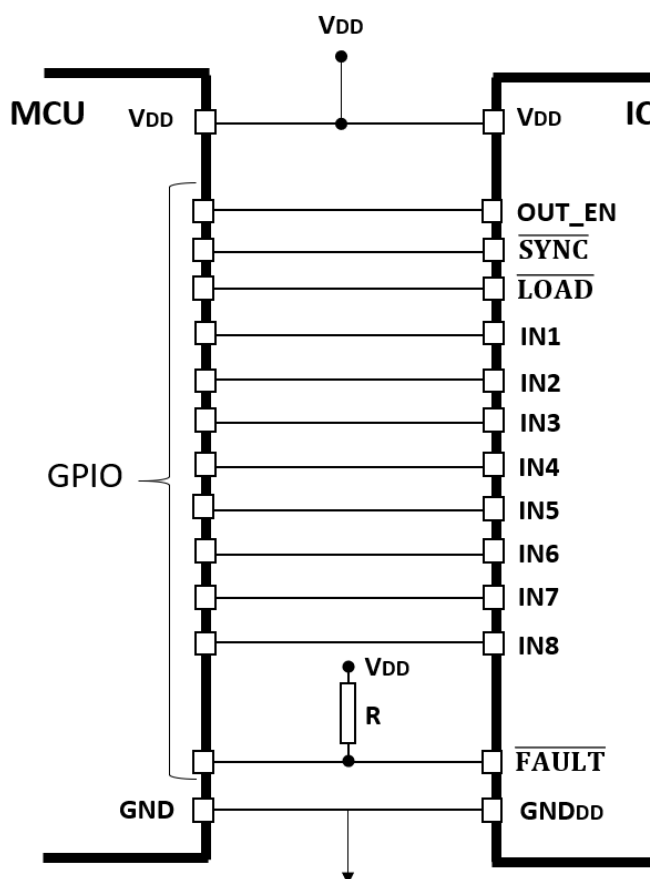
**Figure 13. Synchronous control mode, IC configuration**


Figure 14. Synchronous Control Mode, time diagram

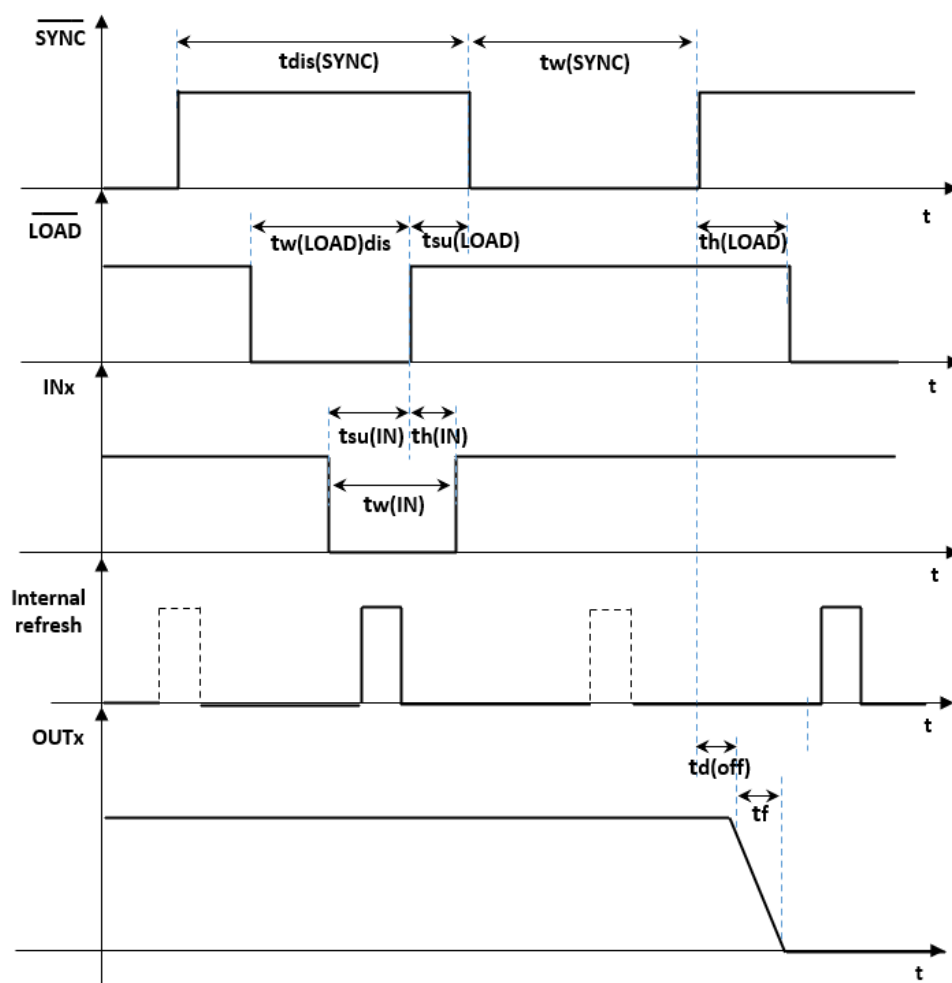
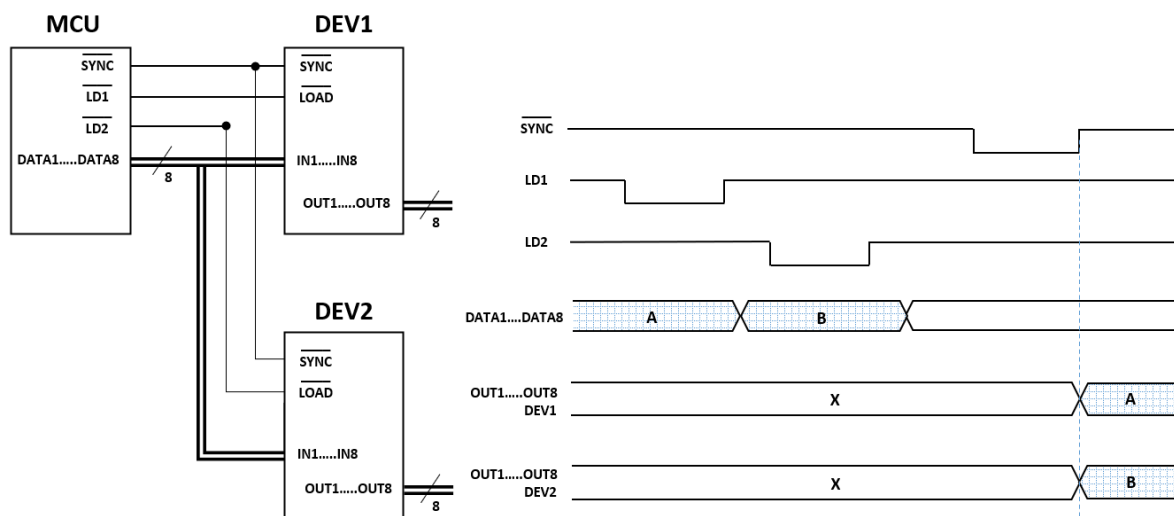


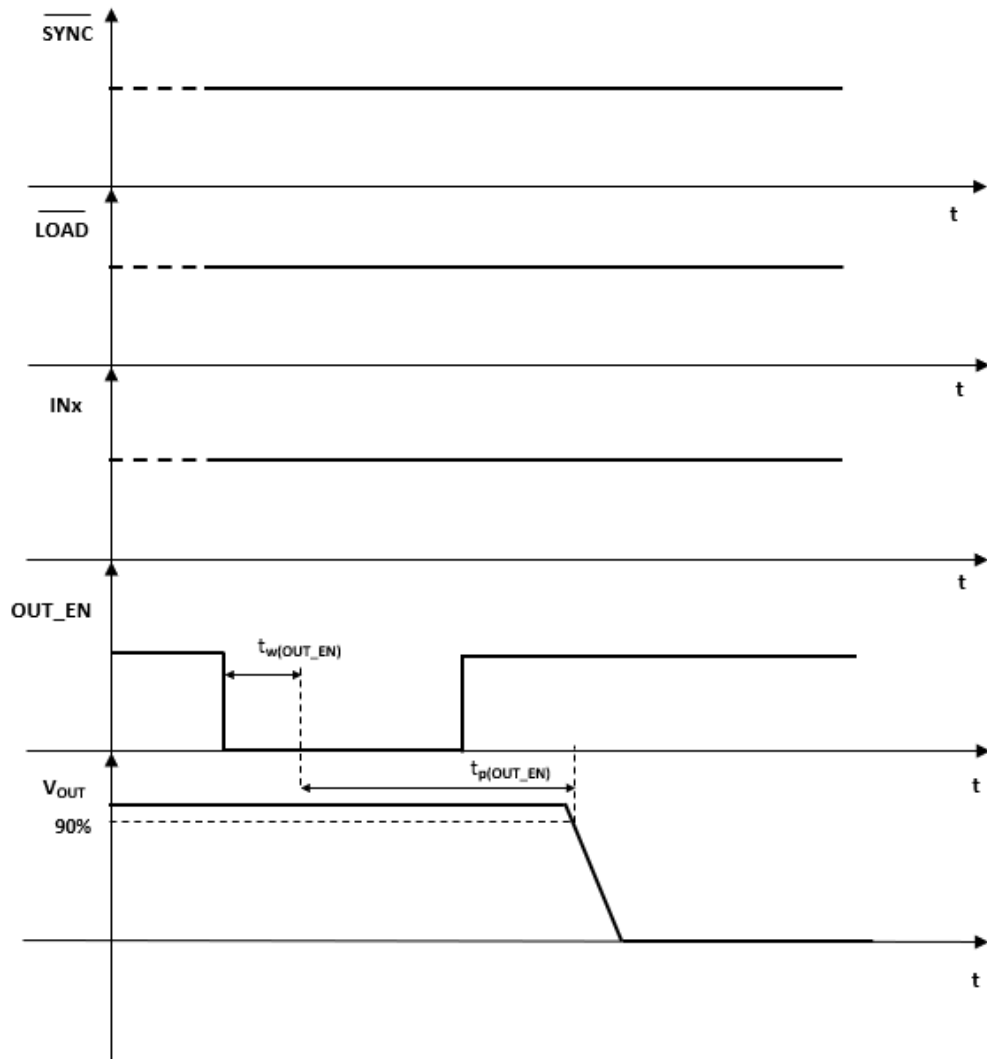
Figure 15. Multiple device Synchronous Control Mode



### 6.3.1 OUT\_EN behavior in Synchronous Control Mode

In SCM the OUT\_EN signal acts as a reset for the internal data register driving the output switches. When the OUT\_EN pin is driven low for at least  $t_{w(OUT\_EN)}$  (see Figure 16), all the eight outputs are disabled. OUTx remains low even if OUT\_EN is raised with INx already high: a new transition of  $\overline{LOAD}$  and SYNC is required (see Figure 14).

**Figure 16. OUT\_EN behavior in Synchronous Control Mode, time diagram**



### 6.4 FAULT indication

The  $\overline{FAULT}$  pin is an active low open drain output indicating fault conditions. This pin is activated when at least one of the following conditions occurs:

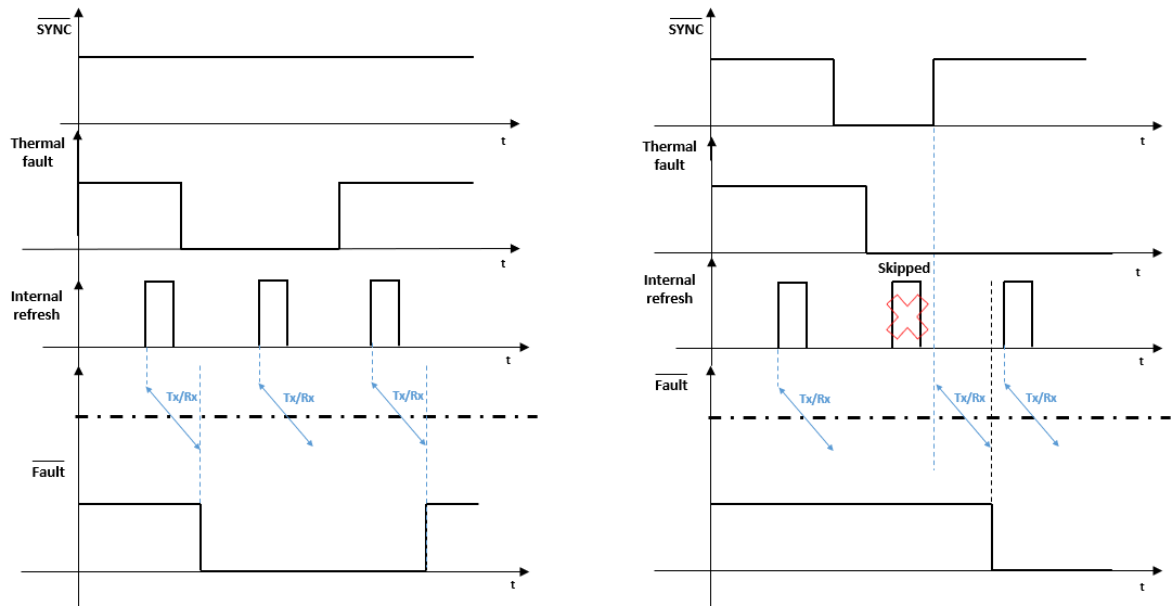
- Junction over-temperature ( $T_{JX} > T_{JSD}$ ) of one or more channels of the Process Stage or case shut-down protection ( $T_C > T_{CSD}$ ) is active
- Internal communication error.

The communication error is intended as an internal data corruption event in the data transfer through isolation. In case of communication error, the outputs are initially kept in the previous status and then reset (turned off) at the first communication error during data transfer of the refresh signal

### 6.4.1 Junction overtemperature

The thermal status of the device is updated during each transmission sequence between the two isolated stages. In SCM operation, when LOAD signal is high and SYNC one is low, the communication between the two stages is disabled. In this case the thermal status of the device cannot be updated, and the FAULT indication could be different to the actual status. In any case, the thermal protections of the channel outputs in the Process Stage are always operative.

**Figure 17. Thermal status update**



## 6.5 Truth table

**Table 16. Truth table**

x = maintain the previous condition.

| Condition                               | Input IN <sub>x</sub> | OUT <sub>x</sub> | FAULT                         |
|-----------------------------------------|-----------------------|------------------|-------------------------------|
| Normal operation                        | H                     | ON               | H (not active)                |
|                                         | L                     | OFF              |                               |
| Thermal Junction ( $T_{JX} > T_{JSD}$ ) | H                     | OFF              | L (active)                    |
|                                         | L                     | OFF              | H (not active)                |
| Thermal Case $T_C > T_{CSD}$            | See Figure 24         |                  | H (not active) <sup>(1)</sup> |
| V <sub>CC</sub> UVLO FAULT              | L                     | OFF              | X                             |
|                                         | H                     |                  |                               |
| V <sub>DD</sub> UVLO (Watchdog)         | X                     | OFF              | H (not active)                |
| Internal communication error            | X                     | X                | L (active)                    |

1. Usually, the thermal case is consequence of thermal junction event latching the FAULT pin low until the thermal junction event resets. If the thermal case is triggered without any thermal junction event (for example in case of very high ambient temperature) then the FAULT pin is not activated

## 7 Power section

### 7.1 Current limitation

The current limitation process is activated when the current sense connected on the output stage measures a current value higher than a fixed threshold. When this condition is verified, the gate voltage is modulated to avoid output current increasing over the limitation value.

The following figures show typical output current waveforms with different load conditions.

**Figure 18. Switching on resistive load**

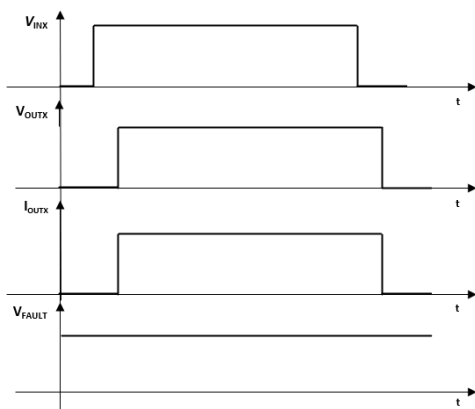


**Figure 19. Switching on bulb lamp**

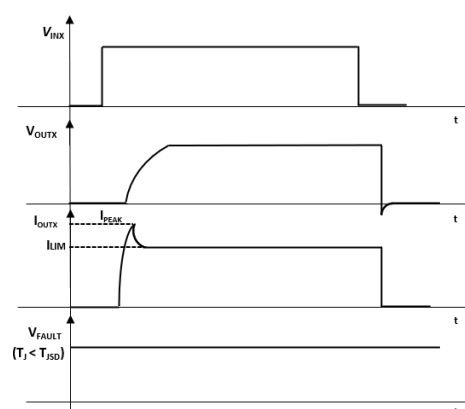


**Figure 20. Switching on light inductive load**

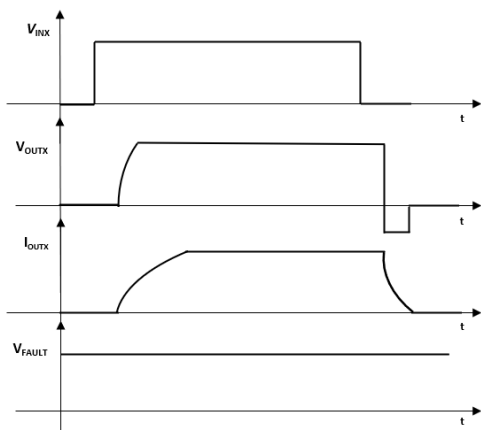


**Figure 21. Switching on heavy inductive load**

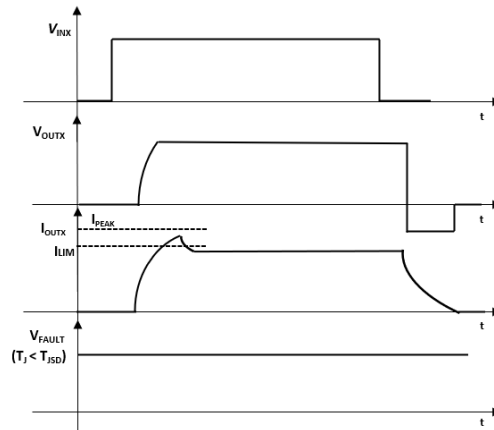
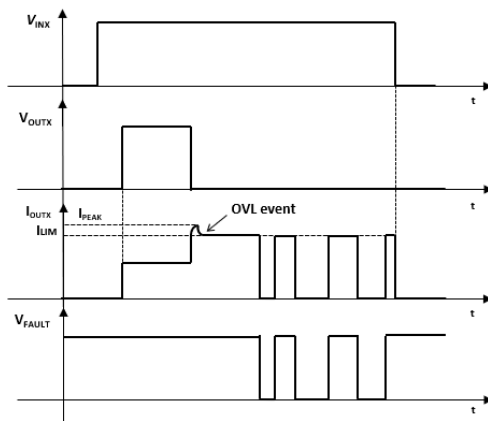
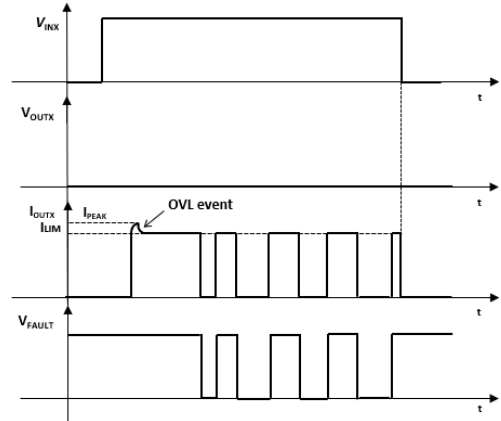


**Figure 22. Short-circuit (with OVT) during ON-state**

**Figure 23. Switching on short-circuit (with OVT)**


## 7.2

### Thermal protection

The device is protected against overheating due to overload conditions. During driving period, if the output is overloaded, the device suffers two different thermal stresses, the first one related to the junction, and the second related to the case.

The two faults have different trigger thresholds: the junction protection threshold ( $T_{JSD}$ ) is higher than that of the case protection ( $T_{CSD}$ ). Generally, the first protection that is activated in thermal stress conditions is the junction thermal shutdown. The output is turned off when the temperature is higher than the related threshold and turned back on when it falls below the reset threshold ( $T_{JR}$ ). This behavior continues while the fault on the output is present.

If the thermal protection is active and the temperature of the package increases over the fixed case protection threshold, the case protection is activated, and the output is switched off and back on when the junction temperature of each channel in fault and case temperature are below the respective reset thresholds.

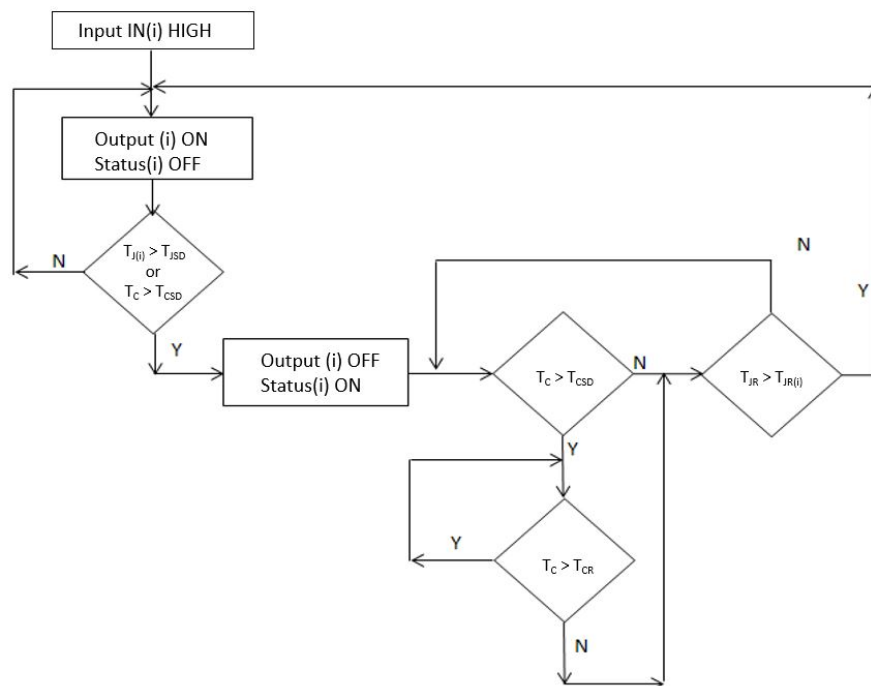
**Figure 24. Thermal protection flowchart**


Figure 25. Thermal protection and fault behavior ( $T_{JSD}$  triggered before  $T_{CSD}$ )

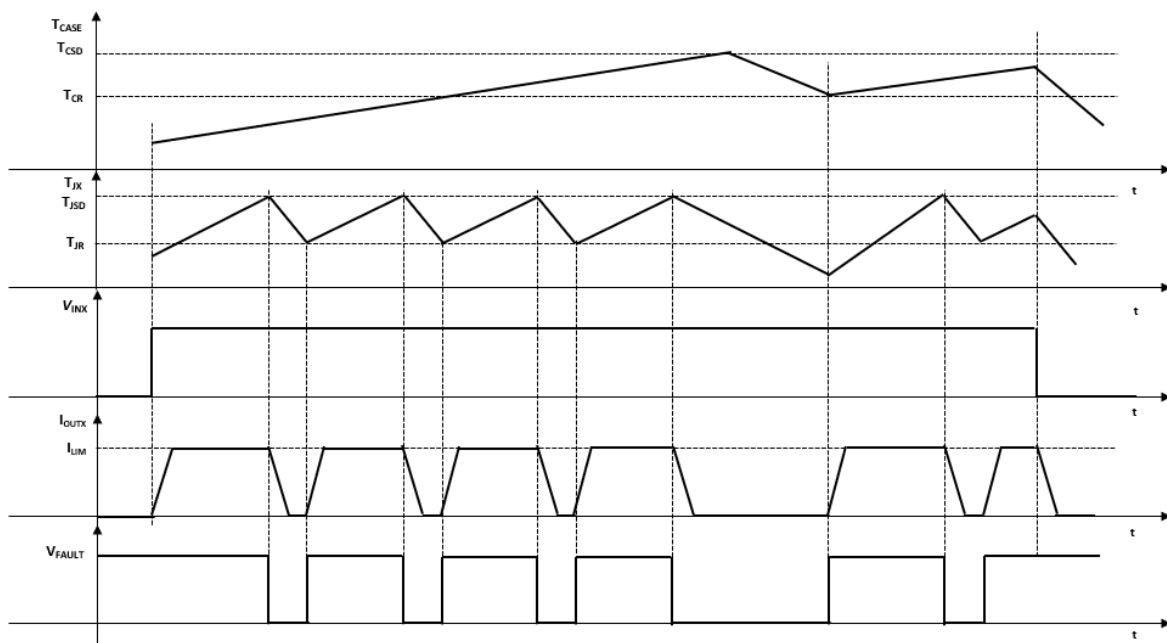
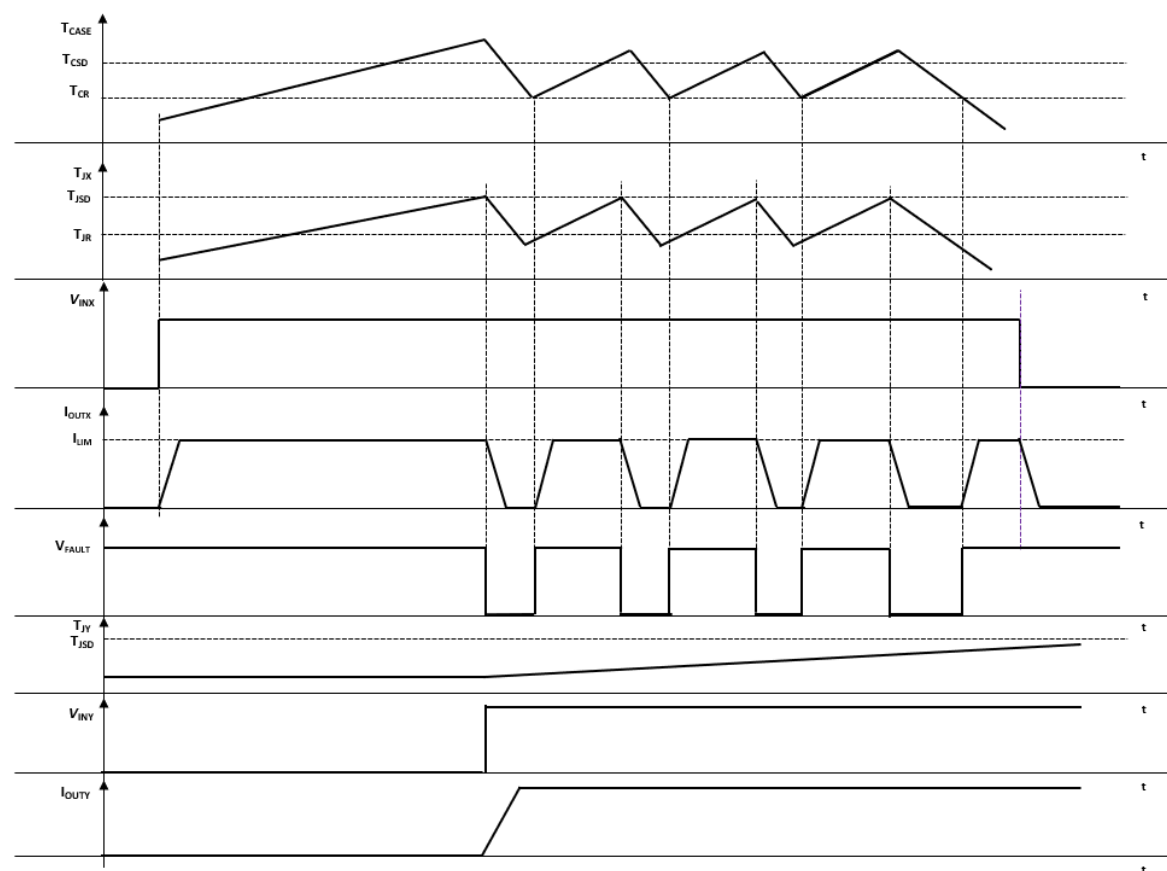


Figure 26. Thermal protection and fault behavior ( $T_{CSD}$  triggered before  $T_{JSD}$ )



## 8 Reverse polarity protection

Reverse polarity protection can be implemented on the board using two different solutions (or both, which is recommended):

1. Placing a resistor ( $R_{GND}$ ) between IC GND pin and load GND
2. Placing a diode in parallel to a resistor between IC GND pin and load GND

If option 1 is selected, the minimum resistance value must be selected according to the following equation:

$$R_{GND} \geq \frac{V_{CC}}{I_{GNDCC}} \quad (1)$$

where  $I_{GNDCC}$  is the DC reverse ground pin current and can be found in Table 2.

The power dissipated by  $R_{GND}$  during reverse polarity is:

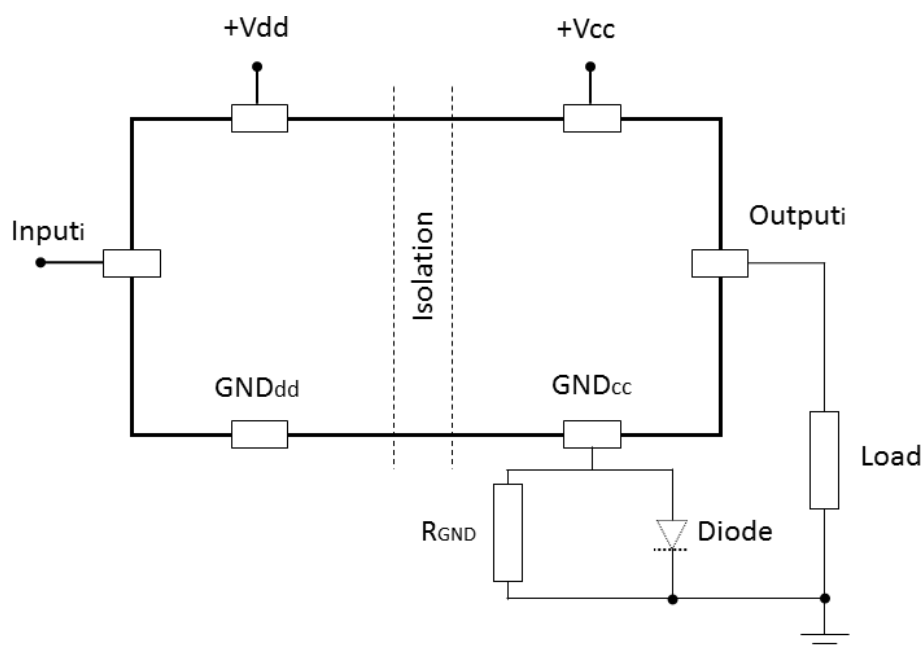
$$P_D = \frac{(V_{CC})^2}{R_{GND}} \quad (2)$$

If option 2 is selected, the diode has to be chosen by taking into account  $V_{RRM} > |V_{CC}|$  and its power dissipation capability:

$$P_D \geq I_S \times V_F \quad (3)$$

**Note:** In normal operation (no reverse polarity), there is a voltage drop ( $\Delta V$ ) between GND of the device and GND of the system. Using option 1,  $\Delta V = R_{gnd} \cdot I_{cc}$ . Using option 2,  $\Delta V = V_F @ (I_F)$ .

**Figure 27. Reverse polarity protection**



**Note:** *Input(i) is intended as any input pin on logic side.*  
This schematic can be used with any type of load.

## 9 Reverse polarity on VDD

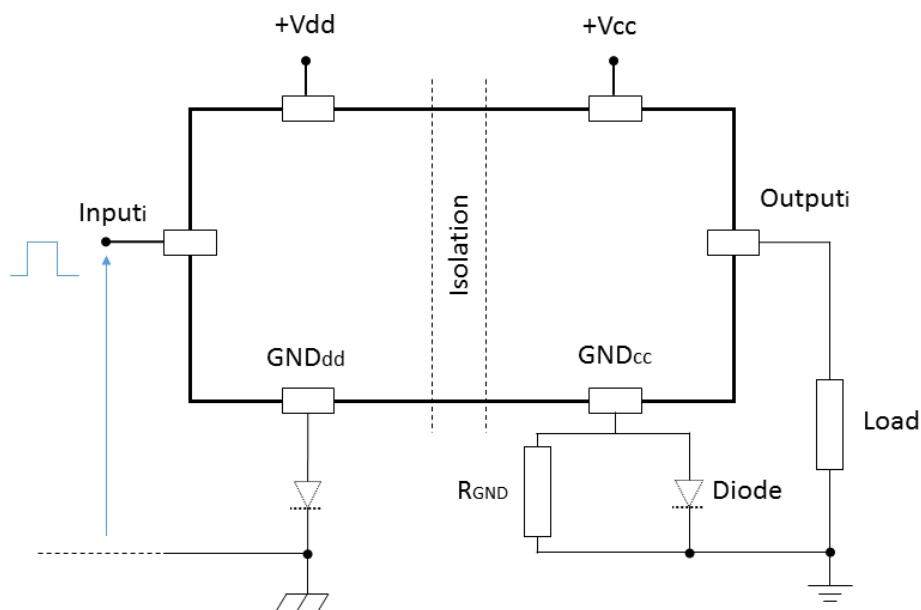
The reverse polarity on  $V_{DD}$  can be implemented on the board by placing a diode between the  $GND_{DD}$  pin and GND digital ground.

The diode must be chosen by taking into account  $V_{RRM} > |V_{DD}|$  and its power dissipation capability:

$$P_D \geq I_{DD} \times V_F \quad (4)$$

**Note:** In normal operation (no reverse polarity), due to the diode, there is a voltage drop ( $\Delta V = V_F @ I_{DD}$ ) between  $GND_{DD}$  of the device and digital ground of the system. In order to guarantee proper triggering of the input signal,  $\Delta V(\max.)$  must result lower than  $V_{IH(MIN)}$ .

**Figure 28.  $V_{DD}$  reverse polarity protection**



**Note:** Input(i) is intended as any input pin on logic side.

## 10 Demagnetization energy

Figure 29. Single pulse demagnetization energy vs. load current (Typical values at  $T_{AMB} = 125\text{ }^{\circ}\text{C}$ )

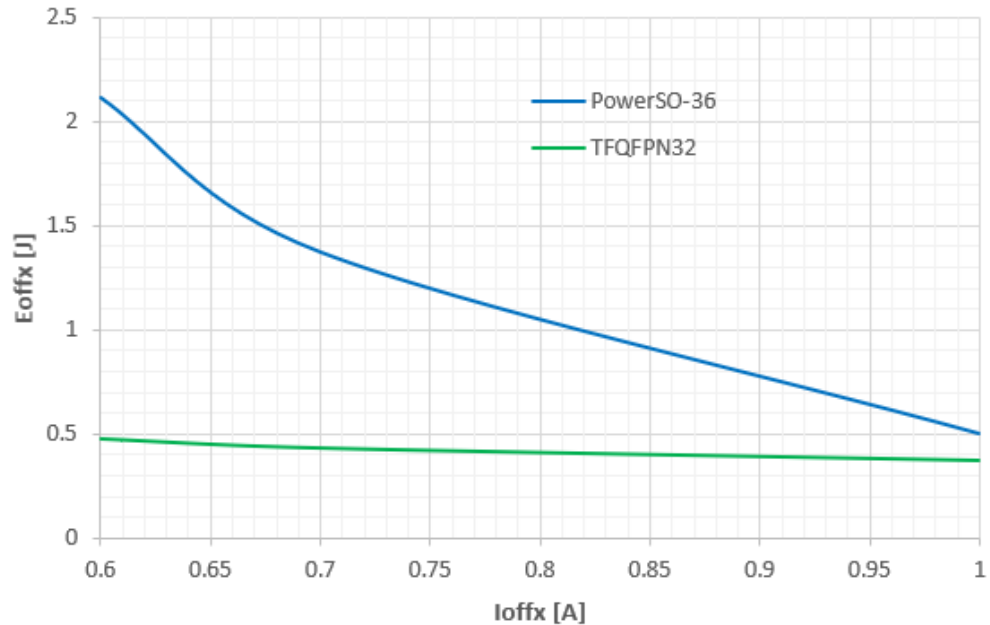


Figure 29 shows the single pulse (not repetitive) demagnetization capability per channel, all channels switched simultaneously

Figure 30. Single pulse inductive load capability vs. load current ( $T_{AMB} = 125\text{ }^{\circ}\text{C}$ )

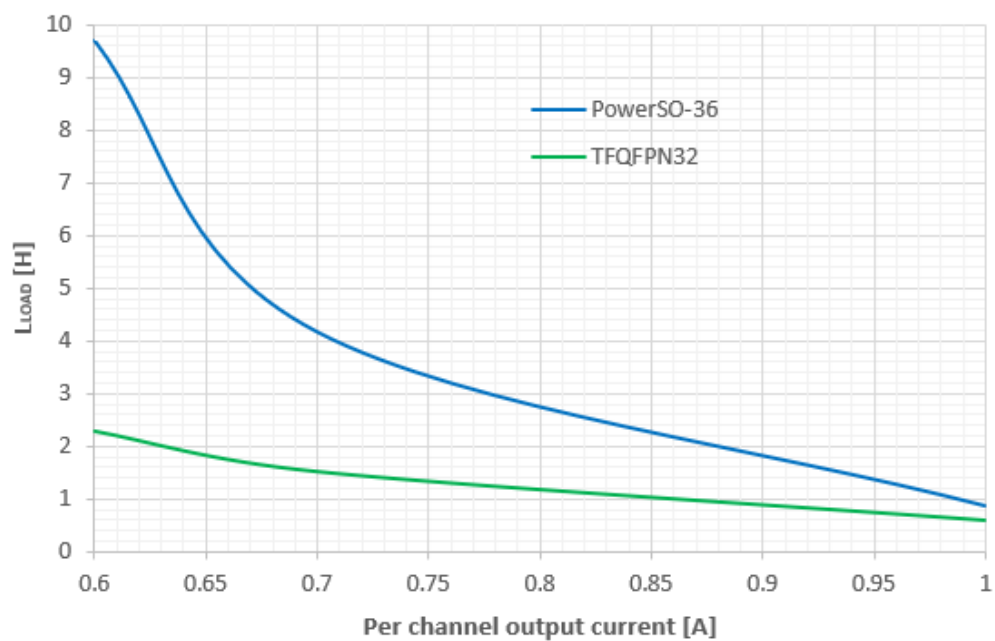
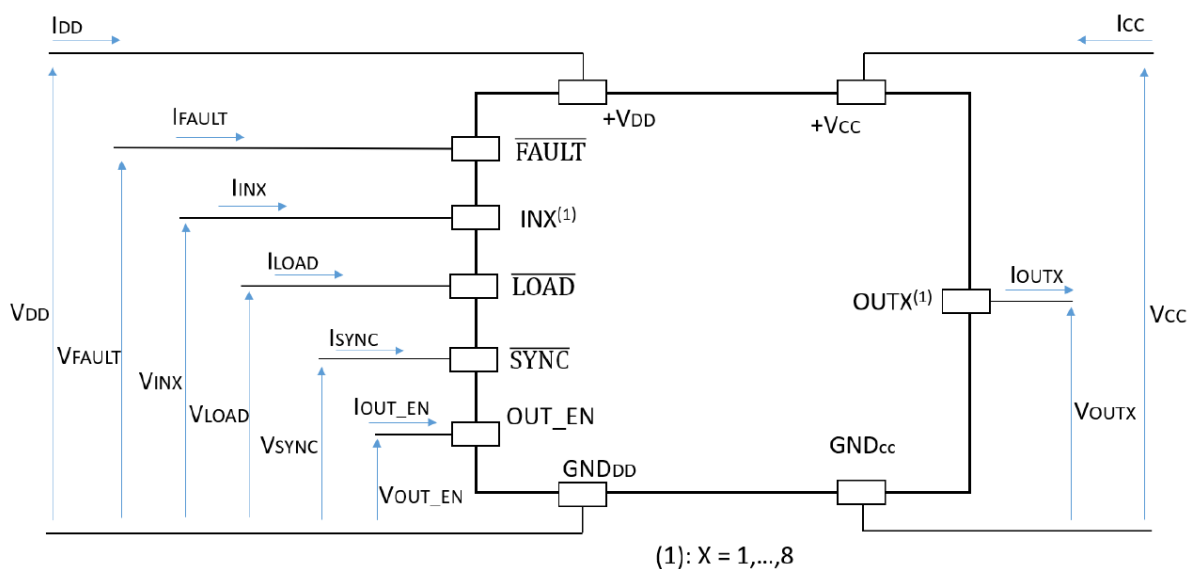


Figure 30 shows the single pulse (not repetitive) inductive load capability per channel, all channels switched simultaneously

## 11 Conventions

### 11.1 Supply voltage and power output conventions

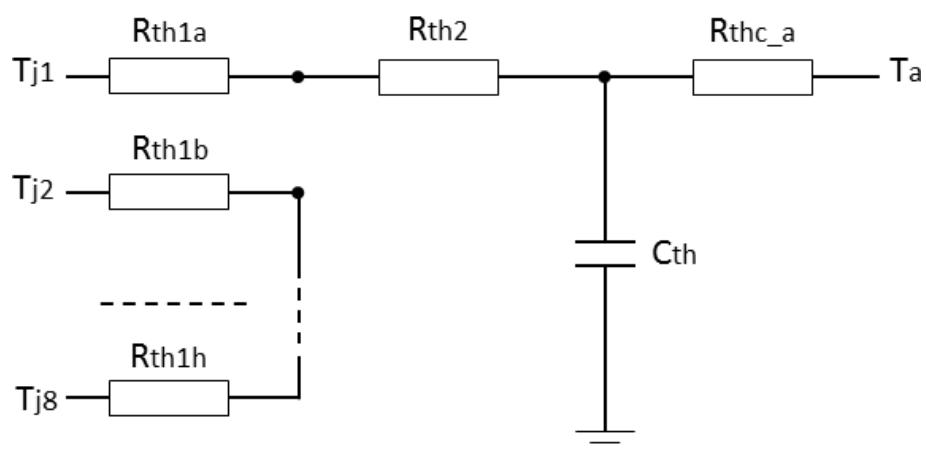
Figure 31. Supply voltage and power output conventions



## 12 Thermal information

### 12.1 Thermal impedance

Figure 32. Simplified thermal model of the process stage



## 13 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 13.1 PowerSO-36 package information

Figure 33. PowerSO-36 package outline

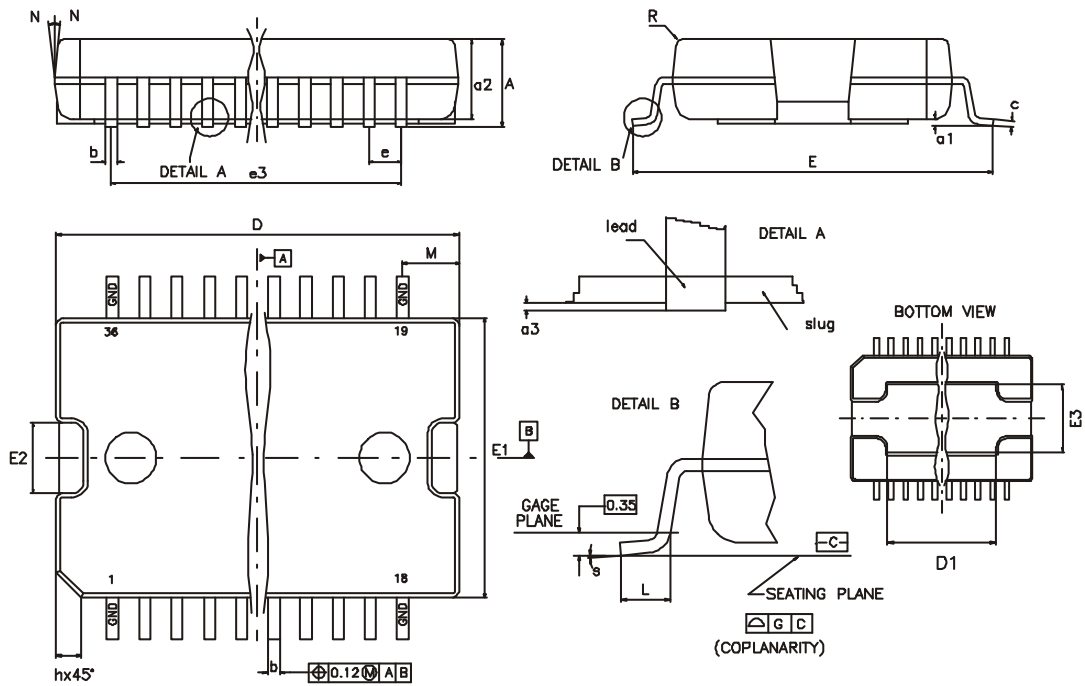


**Table 17. PowerSO-36 package mechanical data**

| Dim.              | mm    |       |       |
|-------------------|-------|-------|-------|
|                   | Min.  | Typ.  | Max.  |
| A                 |       |       | 3.6   |
| a1                | 0.10  |       | 0.30  |
| a2                |       |       | 3.30  |
| b                 | 0.22  |       | 0.38  |
| c                 | 0.23  |       | 0.32  |
| D <sup>(1)</sup>  | 15.80 |       | 16.00 |
| D1                | 9.40  |       | 9.80  |
| E                 | 13.90 |       | 14.50 |
| E1 <sup>(1)</sup> | 10.90 |       | 11.10 |
| E2                |       |       | 2.90  |
| E3                | 5.80  |       | 6.20  |
| e                 |       | 0.65  |       |
| e3                |       | 11.05 |       |
| G                 | 0     |       | 0.10  |
| H                 | 15.50 |       | 15.90 |
| h                 |       |       | 1.10  |
| L                 | 0.80  |       | 1.10  |
| N                 |       |       | 10°   |
| S                 | 0°    |       | 8°    |

1. "D" and "E1" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (0.006"). Critical dimensions are "a3", "E" and "G"

Figure 34. PowerSO-36 suggested footprint

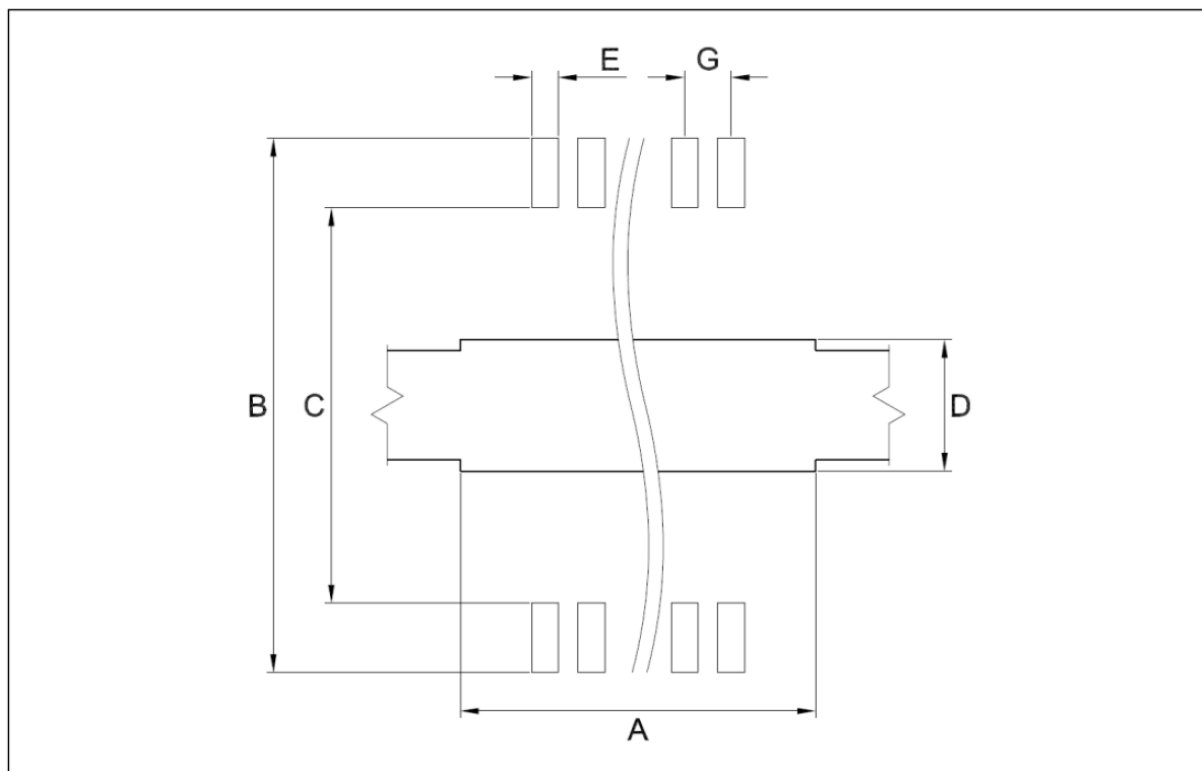
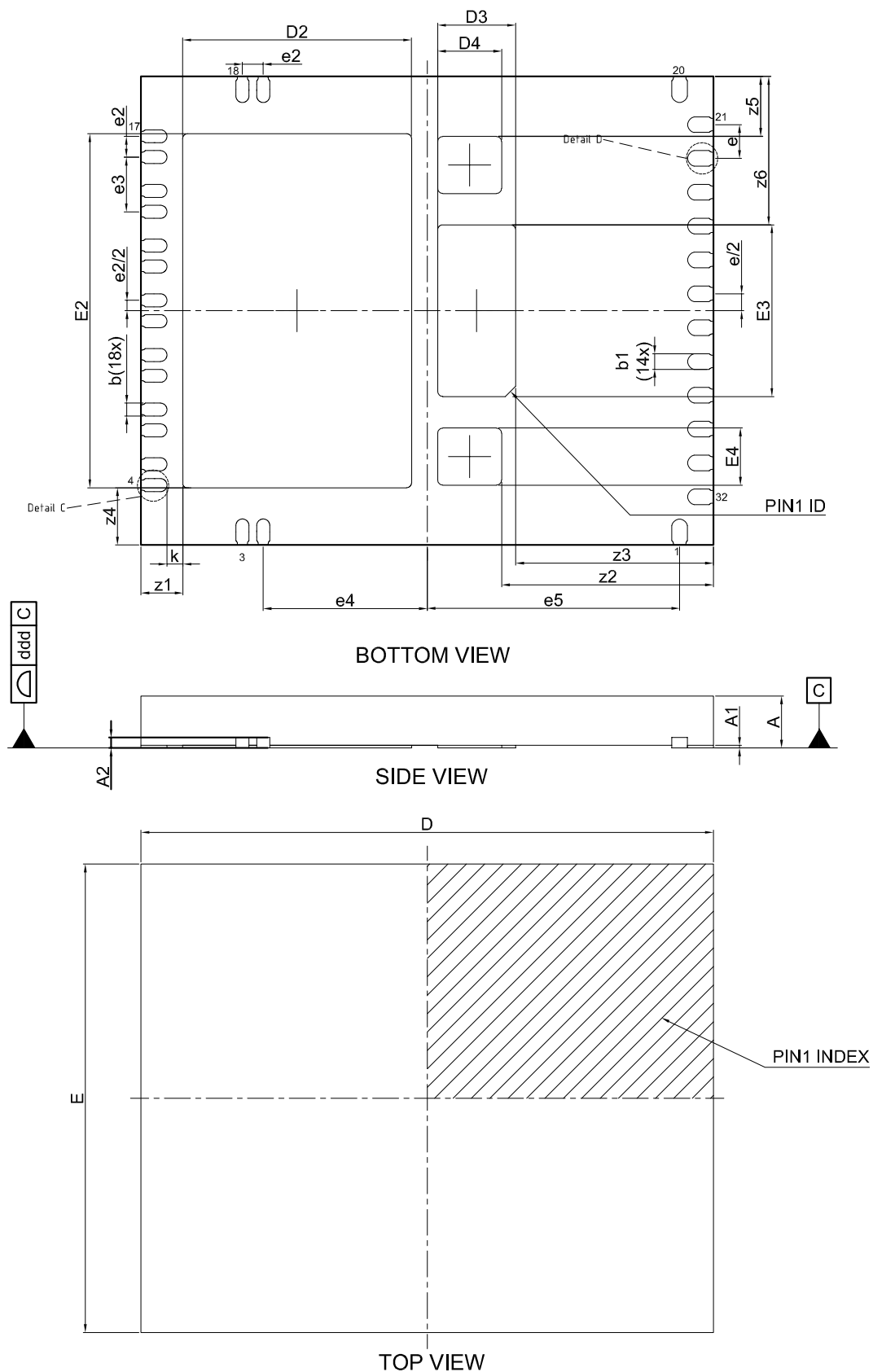


Table 18. PowerSO-36 footprint data

| Dim | mm        |
|-----|-----------|
| A   | 9.5       |
| B   | 14.7-15.0 |
| C   | 12.5-12.7 |
| D   | 6.3       |
| E   | 0.42      |
| G   | 0.65      |

## 13.2 TFQFPN32 package information

Figure 35. TFQFPN32 package outline



Section A-A  
not in scale

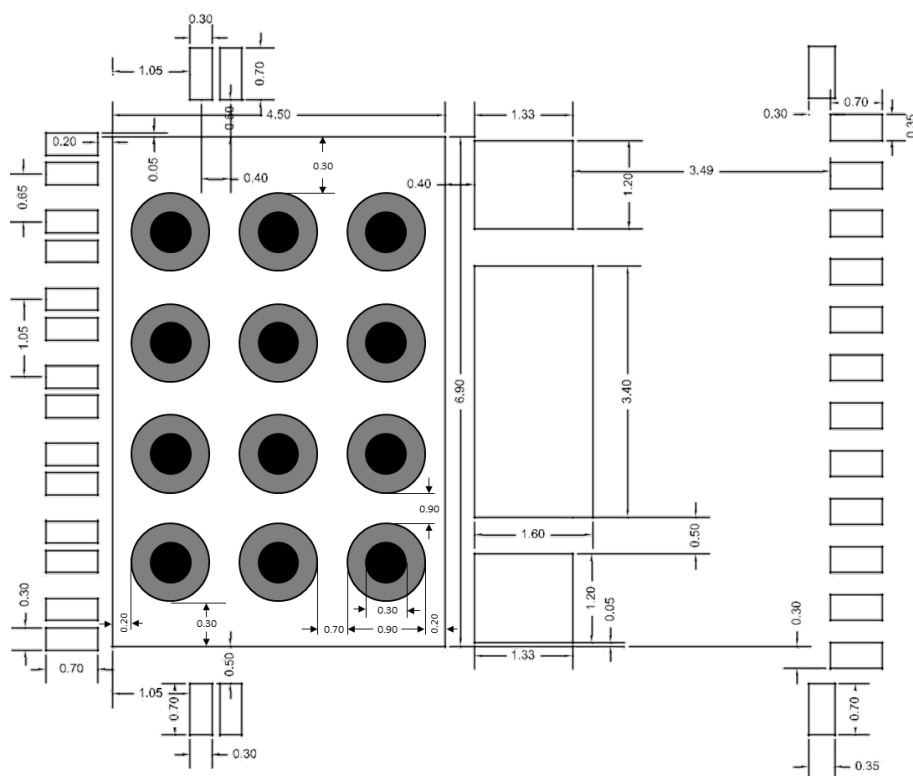


**Table 19. TFQFPN32 package mechanical data**

| Dim.              | mm    |          |       |
|-------------------|-------|----------|-------|
|                   | Min.  | Typ.     | Max.  |
| A                 | 0.95  | 1.00     | 1.05  |
| A1                | 0     | -        | 0.05  |
| A2                | -     | 0.20 REF | -     |
| b <sup>(1)</sup>  | 0.20  | 0.25     | 0.30  |
| b1 <sup>(1)</sup> | 0.25  | 0.30     | 0.35  |
| D                 | 10.90 | 11.0     | 11.10 |
| E <sup>(1)</sup>  | 8.90  | 9.00     | 9.10  |
| D2                | 4.30  | 4.40     | 4.50  |
| E2                | 6.70  | 6.80     | 6.90  |
| D3                | 1.40  | 1.50     | 1.60  |
| E3                | 3.20  | 3.30     | 3.40  |
| D4                | 1.13  | 1.23     | 1.33  |
| E4                | 1.00  | 1.10     | 1.20  |
| e                 | -     | 0.65     | -     |
| e2                | -     | 0.40     | -     |
| e3                | -     | 1.05     | -     |
| e4                | -     | 3.15     | -     |
| e5                | -     | 4.85     | -     |
| k                 | 0     | 0.30     | -     |
| z1                | -     | 0.80     | -     |
| z2                | -     | 4.07     | -     |
| z3                | -     | 3.80     | -     |
| z4                | -     | 1.10     | -     |
| z5                | -     | 1.15     | -     |
| z6                | -     | 2.85     | -     |
| L <sup>(1)</sup>  | 0.45  | 0.50     | 0.55  |

1. Dimensions "b" and "L" are measured on terminal plating surface.

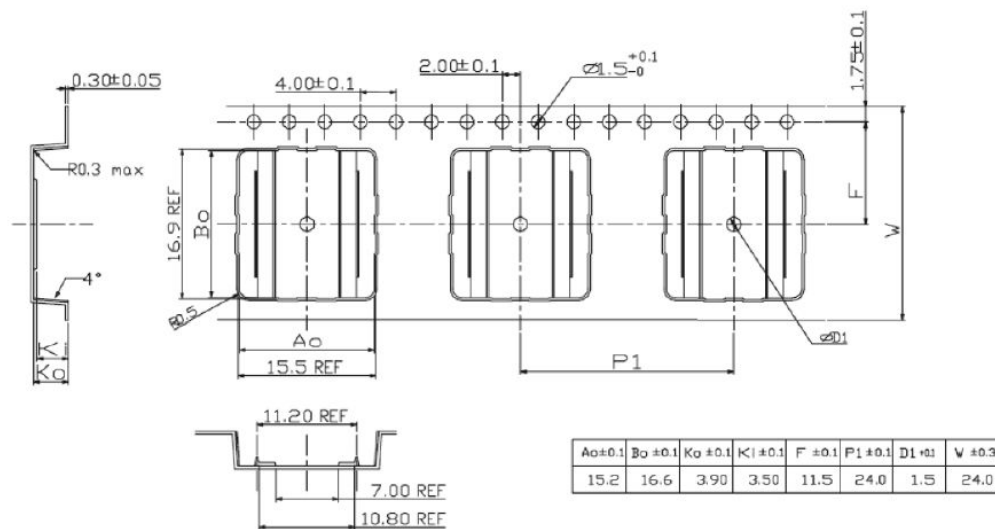
**Table 20. Tolerance of form and position**

| Symbol | Tolerance of form and position | Definition                                                                                                                                                                                                                      | Notes                                                                           |
|--------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------|
| Aaa    | 0.15                           | The bilateral profile tolerance that controls the position of the plastic body sides. The centers of the profile zones are defined by the basic dimensions D and E.                                                             | -                                                                               |
| Bbb    | 0.10                           | The tolerance that controls the position of the entire terminal pattern with respect to datums A and B. The center of the tolerance zone for each terminal is defined by the basic dimension "e" as related to datum's A and B. | -                                                                               |
| Ccc    | 0.10                           | The tolerance located parallel to the seating plane in which the top surface of the package must be located.                                                                                                                    | -                                                                               |
| ddd    | 0.08                           | The tolerance that controls the position of the terminals to each other. The centers of the profile zones are defined by basic dimension "e".                                                                                   | This tolerance is normally compounded with tolerance zone defined by bbb.       |
| eee    | 0.08                           | The unilateral tolerance located above the seating plane where in the bottom surface of all terminals must be located.                                                                                                          | This tolerance is commonly known as the "coplanarity" of the package terminals. |
| fff    | 0.10                           | The tolerance that controls the position of the exposed metal heat feature. The center of the tolerance zone will be datum's defined by the centerlines of the package body.                                                    | -                                                                               |
| REF    | -                              | -                                                                                                                                                                                                                               | No tolerance for A2                                                             |

## 14 Packing information

### 14.1 PowerSO-36 packing information

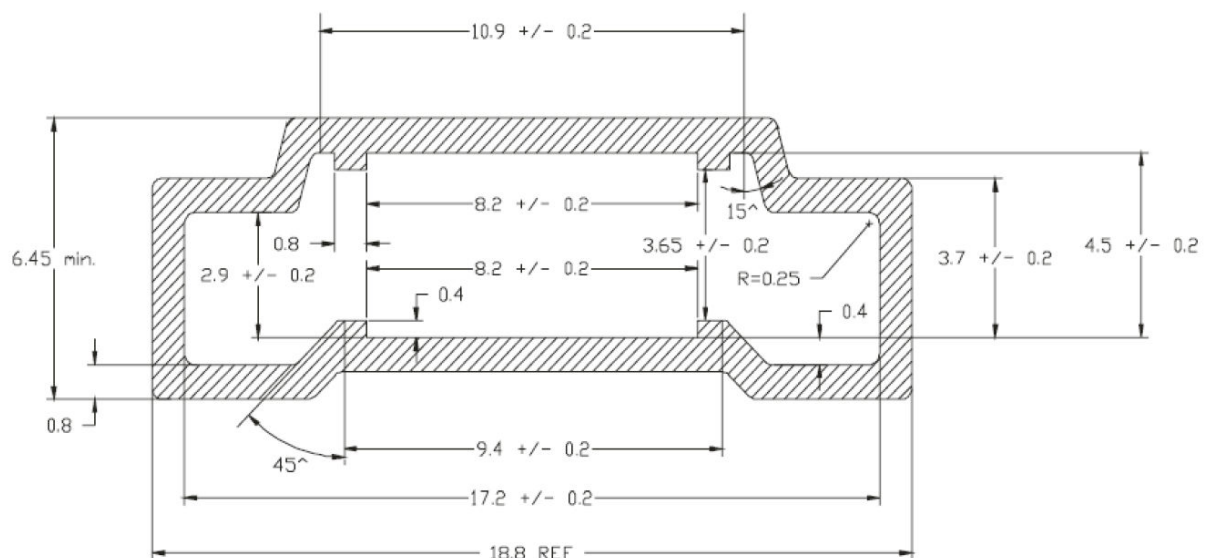
Figure 38. PowerSO-36 carrier tape



NOTE:

- 1) Cumulative tolerance of 10 sprocket holes: 0.2mm
- 2) Camber: 1mm/100mm max

Figure 39. PowerSO-36 shipping tube



## 14.2 TFQFPN32 packing information

Figure 40. Tape and reel packing method concept

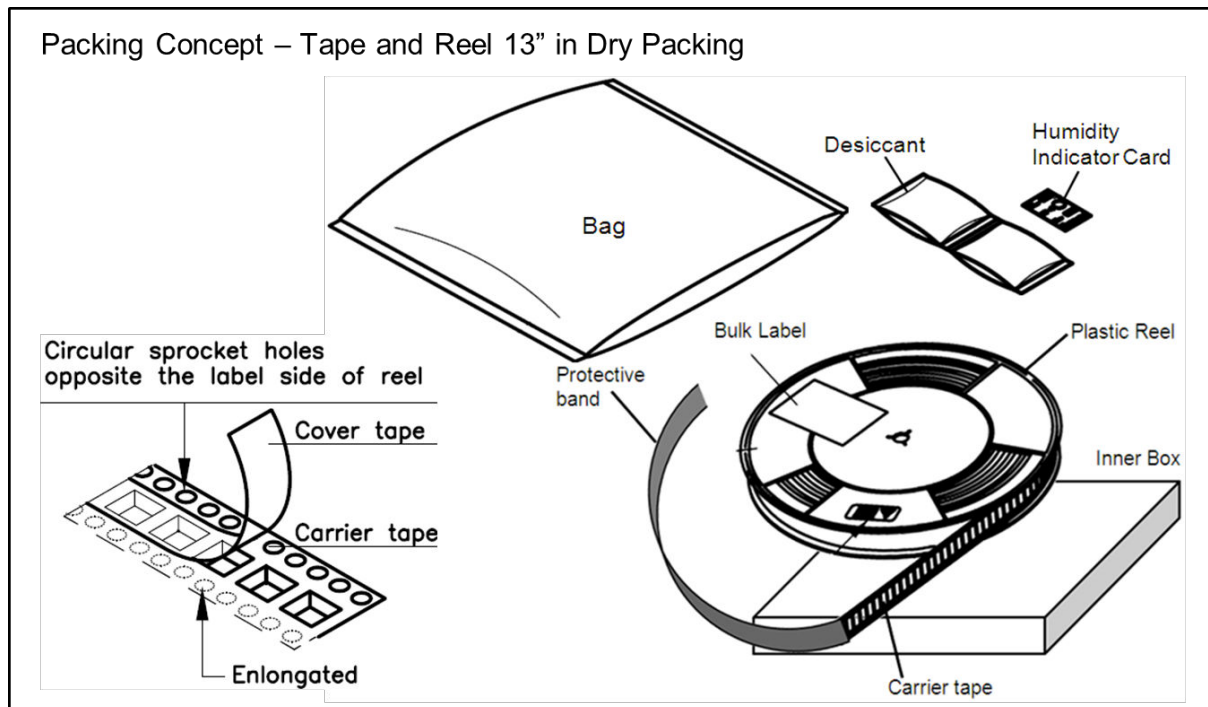


Figure 41. Winding direction

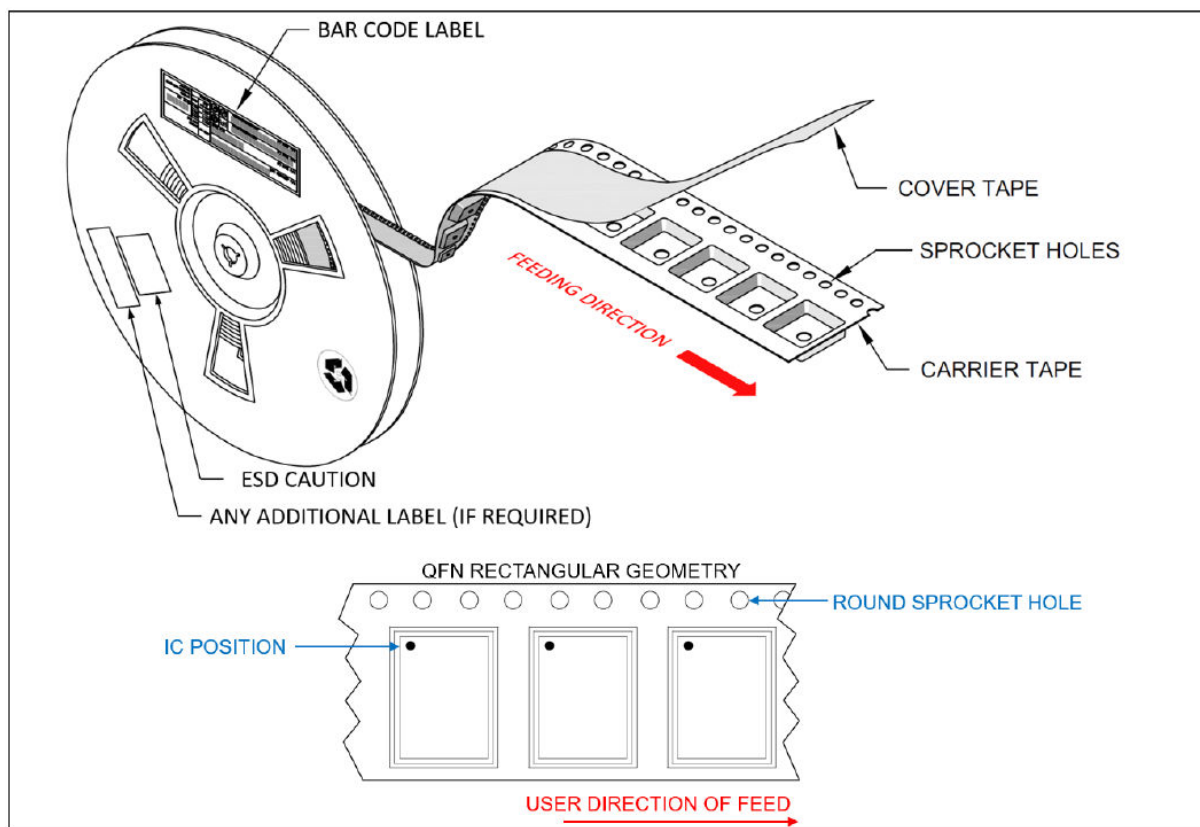


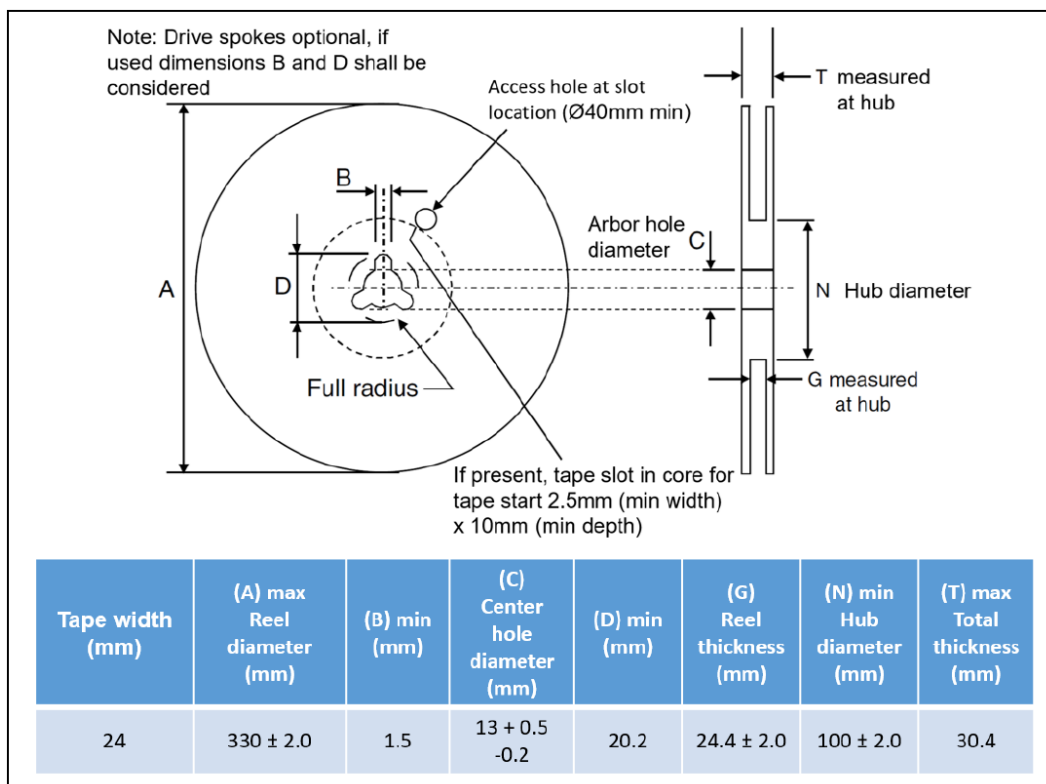
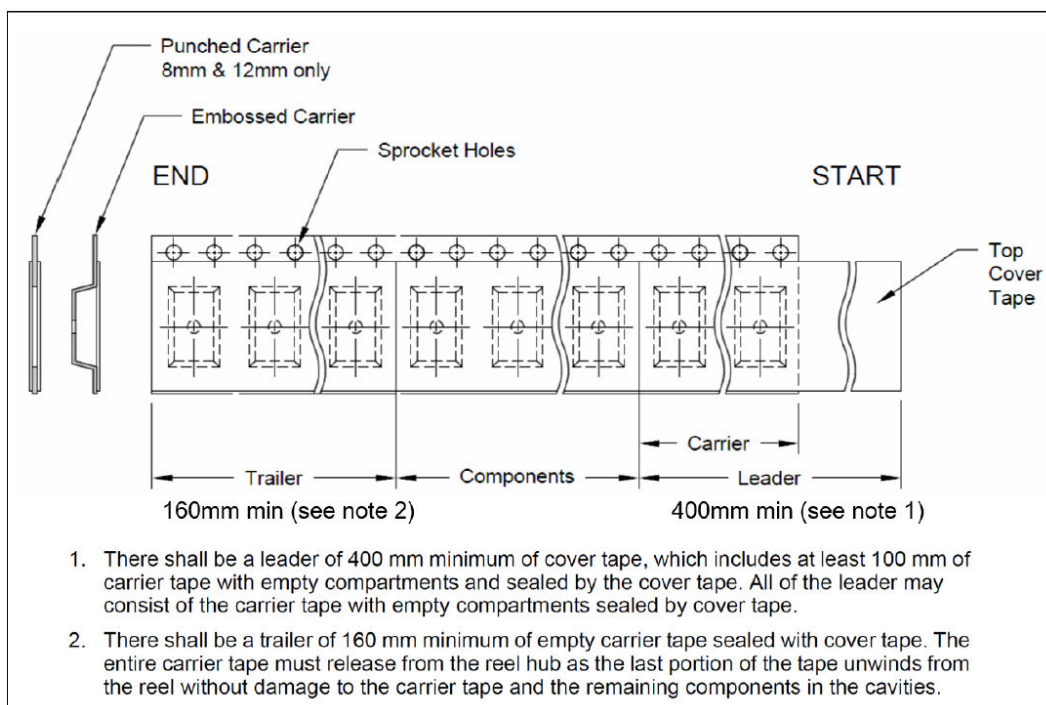
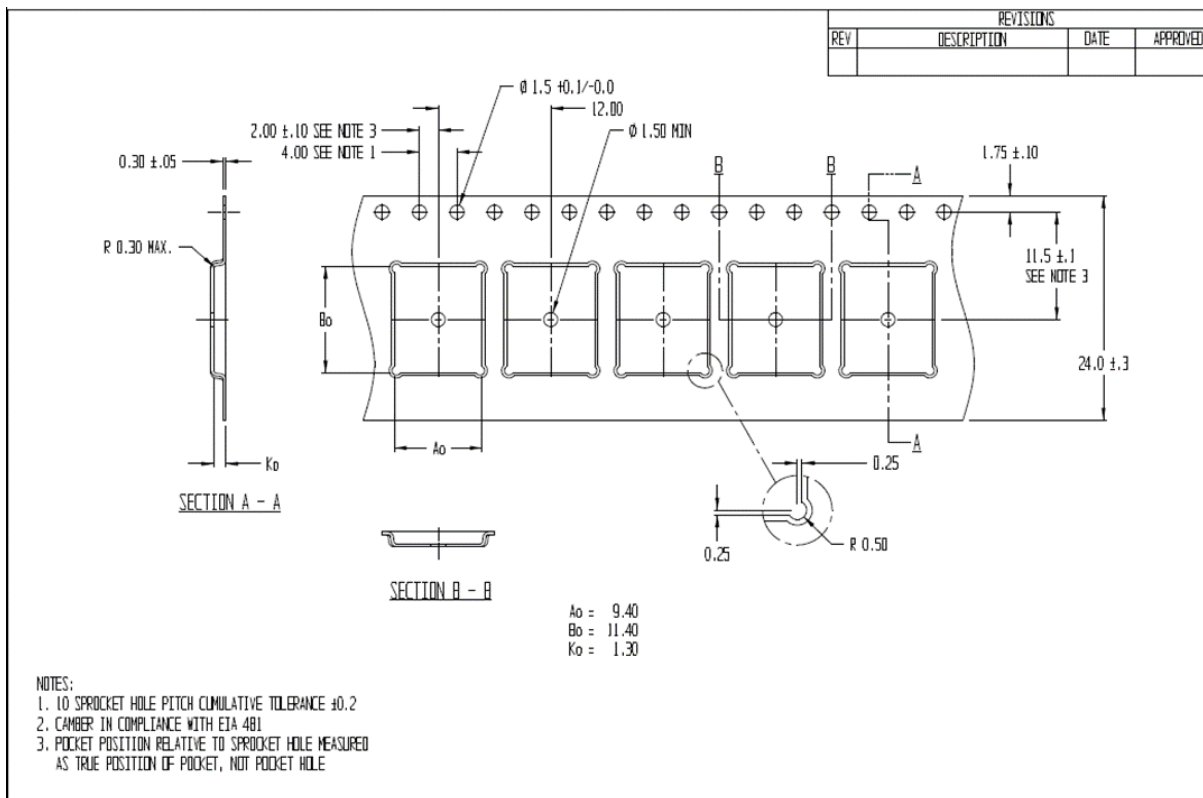
**Figure 42. Reel dimensions (as per EIA-481 specification)**

**Figure 43. Leader and Trailer dimensions (as per EIA-481 specification)**


**Figure 44. TFQFPN32 carrier tape**



## 15 Ordering information

**Table 21. Ordering information**

| Part number | Package    | Packaging     |
|-------------|------------|---------------|
| ISO808      | PowerSO-36 | Tube          |
| ISO808-1    | PowerSO-36 | Tube          |
| ISO808TR    | PowerSO-36 | Tape and reel |
| ISO808TR-1  | PowerSO-36 | Tape and reel |
| ISO808QTR   | TFQFPN32   | Tape and reel |
| ISO808QTR-1 | TFQFPN32   | Tape and reel |

## Revision history

**Table 22. Document revision history**

| Date         | Revision | Changes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|--------------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 21-Dec-2022  | 1        | Initial release.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 12- Sep-2023 | 2        | Throughout the document added reference to TFQFPN32 package : changed <a href="#">Section Cover image</a> ; updated table in <a href="#">Section Product status link / summary</a> ; updated <a href="#">Section Features</a> with ISO808Q/ISO808Q-1; updated first row in <a href="#">Description</a> ; added <a href="#">Figure 3</a> ; updated <a href="#">Table 1</a> ; updated <a href="#">Table 2</a> ; updated <a href="#">Table 3</a> ; updated <a href="#">Table 6</a> , <a href="#">Table 11</a> and <a href="#">Table 12</a> ; deleted <a href="#">Table 14</a> in <a href="#">Section 6.1</a> ; added <a href="#">Section 6.3.1</a> and <a href="#">Section 6.5</a> ; updated <a href="#">Figure 18</a> , <a href="#">Figure 19</a> , <a href="#">Figure 20</a> , <a href="#">Figure 21</a> , <a href="#">Figure 22</a> , <a href="#">Figure 23</a> , <a href="#">Figure 25</a> , <a href="#">Figure 26</a> , <a href="#">Figure 29</a> ; added <a href="#">Figure 30</a> ; added <a href="#">Section 13.2</a> , <a href="#">Section 14.2</a> ; updated <a href="#">Table 21</a> . |
| 22-Dec-2023  | 3        | Added reference to safety limits certification according to IEC 60747-17 in front page and <a href="#">Table 13</a> . Replaced <a href="#">Figure 3</a> and added a new row in <a href="#">Table 1</a> . In <a href="#">Table 3</a> added a footnote regarding the maximum power dissipation based on the package version.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 18-Mar-2024  | 4        | Fixed typo on VDE number in the front page                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |

## Contents

|           |                                                     |           |
|-----------|-----------------------------------------------------|-----------|
| <b>1</b>  | <b>Block diagram</b>                                | <b>3</b>  |
| <b>2</b>  | <b>Pin connection</b>                               | <b>4</b>  |
| <b>3</b>  | <b>Absolute maximum ratings</b>                     | <b>6</b>  |
| <b>4</b>  | <b>Thermal data</b>                                 | <b>7</b>  |
| <b>5</b>  | <b>Electrical characteristics</b>                   | <b>8</b>  |
| <b>6</b>  | <b>Functional description</b>                       | <b>15</b> |
| 6.1       | Parallel interface                                  | 15        |
| 6.1.1     | Input signals (IN1 to IN8)                          | 15        |
| 6.1.2     | Load input data ( $\overline{\text{LOAD}}$ )        | 15        |
| 6.1.3     | Output synchronization ( $\overline{\text{SYNC}}$ ) | 15        |
| 6.1.4     | Watchdog                                            | 16        |
| 6.1.5     | Output enable (OUT_EN)                              | 16        |
| 6.2       | Direct Control Mode (DCM)                           | 17        |
| 6.3       | Synchronous control mode (SCM)                      | 18        |
| 6.3.1     | OUT_EN behavior in Synchronous Control Mode         | 21        |
| 6.4       | FAULT indication                                    | 21        |
| 6.4.1     | Junction overtemperature                            | 22        |
| 6.5       | Truth table                                         | 22        |
| <b>7</b>  | <b>Power section</b>                                | <b>23</b> |
| 7.1       | Current limitation                                  | 23        |
| 7.2       | Thermal protection                                  | 24        |
| <b>8</b>  | <b>Reverse polarity protection</b>                  | <b>26</b> |
| <b>9</b>  | <b>Reverse polarity on VDD</b>                      | <b>27</b> |
| <b>10</b> | <b>Demagnetization energy</b>                       | <b>28</b> |
| <b>11</b> | <b>Conventions</b>                                  | <b>29</b> |
| 11.1      | Supply voltage and power output conventions         | 29        |
| <b>12</b> | <b>Thermal information</b>                          | <b>30</b> |
| 12.1      | Thermal impedance                                   | 30        |
| <b>13</b> | <b>Package information</b>                          | <b>31</b> |
| 13.1      | PowerSO-36 package information                      | 31        |
| 13.2      | TFQFPN32 package information                        | 34        |
| <b>14</b> | <b>Packing information</b>                          | <b>38</b> |
| 14.1      | PowerSO-36 packing information                      | 38        |
| 14.2      | TFQFPN32 packing information                        | 39        |



---

|    |                            |    |
|----|----------------------------|----|
| 15 | Ordering information ..... | 42 |
|    | Revision history .....     | 43 |

## List of figures

|            |                                                                                                     |    |
|------------|-----------------------------------------------------------------------------------------------------|----|
| Figure 1.  | Block diagram                                                                                       | 3  |
| Figure 2.  | Pin connection PowerSO-36 (top through view)                                                        | 4  |
| Figure 3.  | Pin connection TFQFPN32 (top through view)                                                          | 4  |
| Figure 4.  | $R_{DS(on)}$ measurement                                                                            | 10 |
| Figure 5.  | $dV/dt$ definition                                                                                  | 10 |
| Figure 6.  | td(ON)-td(OFF) Synchronous Control Mode (SCM)                                                       | 11 |
| Figure 7.  | td(ON)-td(OFF) Direct Control Mode (DCM)                                                            | 11 |
| Figure 8.  | Watchdog behavior                                                                                   | 16 |
| Figure 9.  | OUT_EN without effect on output                                                                     | 16 |
| Figure 10. | OUT_EN effective on output channel                                                                  | 16 |
| Figure 11. | Direct Control Mode, IC configurations                                                              | 17 |
| Figure 12. | Direct Control Mode, time diagram                                                                   | 18 |
| Figure 13. | Synchronous control mode, IC configuration                                                          | 19 |
| Figure 14. | Synchronous Control Mode, time diagram                                                              | 20 |
| Figure 15. | Multiple device Synchronous Control Mode                                                            | 20 |
| Figure 16. | OUT_EN behavior in Synchronous Control Mode, time diagram                                           | 21 |
| Figure 17. | Thermal status update                                                                               | 22 |
| Figure 18. | Switching on resistive load                                                                         | 23 |
| Figure 19. | Switching on bulb lamp                                                                              | 23 |
| Figure 20. | Switching on light inductive load                                                                   | 23 |
| Figure 21. | Switching on heavy inductive load                                                                   | 23 |
| Figure 22. | Short-circuit (with OVT) during ON-state                                                            | 24 |
| Figure 23. | Switching on short-circuit (with OVT)                                                               | 24 |
| Figure 24. | Thermal protection flowchart                                                                        | 24 |
| Figure 25. | Thermal protection and fault behavior ( $T_{JSD}$ triggered before $T_{CSD}$ )                      | 25 |
| Figure 26. | Thermal protection and fault behavior ( $T_{CSD}$ triggered before $T_{JSD}$ )                      | 25 |
| Figure 27. | Reverse polarity protection                                                                         | 26 |
| Figure 28. | $V_{DD}$ reverse polarity protection                                                                | 27 |
| Figure 29. | Single pulse demagnetization energy vs. load current (Typical values at $T_{AMB} = 125\text{ °C}$ ) | 28 |
| Figure 30. | Single pulse inductive load capability vs. load current ( $T_{AMB} = 125\text{ °C}$ )               | 28 |
| Figure 31. | Supply voltage and power output conventions                                                         | 29 |
| Figure 32. | Simplified thermal model of the process stage                                                       | 30 |
| Figure 33. | PowerSO-36 package outline                                                                          | 31 |
| Figure 34. | PowerSO-36 suggested footprint                                                                      | 33 |
| Figure 35. | TFQFPN32 package outline                                                                            | 34 |
| Figure 36. | TFQFPN32 package detail outline                                                                     | 35 |
| Figure 37. | TFQFPN32 suggested footprint (measured in mm)                                                       | 35 |
| Figure 38. | PowerSO-36 carrier tape                                                                             | 38 |
| Figure 39. | PowerSO-36 shipping tube                                                                            | 38 |
| Figure 40. | Tape and reel packing method concept                                                                | 39 |
| Figure 41. | Winding direction                                                                                   | 39 |
| Figure 42. | Reel dimensions (as per EIA-481 specification)                                                      | 40 |
| Figure 43. | Leader and Trailer dimensions (as per EIA-481 specification)                                        | 40 |
| Figure 44. | TFQFPN32 carrier tape                                                                               | 41 |

## List of tables

|                  |                                                                                                                                                                    |    |
|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| <b>Table 1.</b>  | Pin description . . . . .                                                                                                                                          | 5  |
| <b>Table 2.</b>  | Absolute maximum ratings . . . . .                                                                                                                                 | 6  |
| <b>Table 3.</b>  | Thermal data . . . . .                                                                                                                                             | 7  |
| <b>Table 4.</b>  | Power section . . . . .                                                                                                                                            | 8  |
| <b>Table 5.</b>  | Digital supply voltage . . . . .                                                                                                                                   | 8  |
| <b>Table 6.</b>  | Diagnostic pin and output protection function . . . . .                                                                                                            | 9  |
| <b>Table 7.</b>  | Power switching characteristics ( $V_{CC} = 24\text{ V}$ ; $R_{LOAD} = 48\ \Omega$ ; $-40\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$ ) . . . . . | 9  |
| <b>Table 8.</b>  | Logic inputs and output . . . . .                                                                                                                                  | 12 |
| <b>Table 9.</b>  | Parallel interface timings ( $V_{DD} = 5\text{ V}$ ; $V_{CC} = 24\text{ V}$ ; $-40\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$ ) . . . . .        | 12 |
| <b>Table 10.</b> | Internal communication timings ( $V_{DD} = 5\text{ V}$ ; $V_{CC} = 24\text{ V}$ ; $-40\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$ ) . . . . .    | 12 |
| <b>Table 11.</b> | Insulation and safety-related specifications . . . . .                                                                                                             | 13 |
| <b>Table 12.</b> | Insulation characteristics . . . . .                                                                                                                               | 13 |
| <b>Table 13.</b> | Safety limits . . . . .                                                                                                                                            | 14 |
| <b>Table 14.</b> | Interface signal operation in DCM . . . . .                                                                                                                        | 17 |
| <b>Table 15.</b> | Interface signal operation in synchronous mode . . . . .                                                                                                           | 19 |
| <b>Table 16.</b> | Truth table . . . . .                                                                                                                                              | 22 |
| <b>Table 17.</b> | PowerSO-36 package mechanical data . . . . .                                                                                                                       | 32 |
| <b>Table 18.</b> | PowerSO-36 footprint data . . . . .                                                                                                                                | 33 |
| <b>Table 19.</b> | TFQFPN32 package mechanical data . . . . .                                                                                                                         | 36 |
| <b>Table 20.</b> | Tolerance of form and position . . . . .                                                                                                                           | 37 |
| <b>Table 21.</b> | Ordering information . . . . .                                                                                                                                     | 42 |
| <b>Table 22.</b> | Document revision history . . . . .                                                                                                                                | 43 |

**IMPORTANT NOTICE – READ CAREFULLY**

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to [www.st.com/trademarks](http://www.st.com/trademarks). All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2024 STMicroelectronics – All rights reserved