RZ/G1E

User’s Manual: Hardware

for Rich Graphics Applications
RZ/G Series

ARM®

Specifications of Individual RZ/G Series Product

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   - Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   - The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on
   - The state of the product is undefined at the moment when power is supplied.
   - The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   - In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   - In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses
   - Access to reserved addresses is prohibited.
   - The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals
   - After applying a reset, only release the reset line after the operating clock signal has become stable.
   - When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   - When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products
   - Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.
   - The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.
How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.

The manual comprises an overview of hardware, pin assignments, pin multiplexing, and pin function controller. For the rest of the sections on other on-chip peripheral functions, see the RZ/G Series User’s Manual: Hardware.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

We provide the following three types of user’s manual for RZ/G Series products. Make sure to refer to the latest versions of these documents.

<table>
<thead>
<tr>
<th>Document Type</th>
<th>Description</th>
<th>Document Title</th>
<th>Document No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>User’s manual for specifications of individual RZ/G Series product</td>
<td>Overview of hardware, pin assignments, pin multiplexing, and pin function controller</td>
<td>RZ/G1E User’s Manual: Hardware</td>
<td>R01UH0544EJ0 100 Rev.1.00 (This user’s manual)</td>
</tr>
<tr>
<td>User’s manual for specifications common to RZ/G Series products</td>
<td>Hardware specifications (address map, general-purpose I/O port pins, clock, reset, core functions, graphics, video processing, sound processing, and network modules, serial interfaces, storage, timers, other on-chip peripheral functions, testing, and debugging) and descriptions of operation</td>
<td>RZ/G Series User’s Manual: Hardware</td>
<td>R01UH0543EJ0 100 Rev.1.00</td>
</tr>
<tr>
<td>User’s manual for electrical characteristics</td>
<td>Electrical characteristics of the RZ/G Series products</td>
<td>Provided as separate technical information.</td>
<td></td>
</tr>
</tbody>
</table>

2. Notation of Numbers and Symbols

Bit notation: Bits are shown in high-to-low order from left to right.

Number notation: Binary numbers are given as B'XXXX, hexadecimal numbers are given as H'XXXX, and decimal numbers are given as XXXX.

Signal notation: A number sign (#) after the name indicates that a signal or pin is active-low, unless otherwise specified.

Example: PRESET#
3. Register Notation

Each register description includes a bit chart, illustrating the arrangement of bits, and a table of bits, describing the meanings of the bit settings.

### Bit Chart

<table>
<thead>
<tr>
<th>Bit</th>
<th>Initial Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>14</td>
<td>0</td>
<td>These bits are always read as 0.</td>
</tr>
<tr>
<td>13 to 11</td>
<td>1 or 0</td>
<td>Address identifier</td>
</tr>
<tr>
<td>10</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>9</td>
<td>1</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

**Note:** The bit names and sentences in the above figure are examples and have nothing to do with the contents of this manual.

1. **Bit**: Indicates the bit number or number.
   - In the case of a 32-bit register, the bits are arranged in order from 31 to 0. In the case of a 16-bit register, the bits are arranged in order from 15 to 0.

2. **Bit name**: Indicates the name of the bit or bit field.
   - When the number of bits has to be clearly indicated in the field, appropriate notation is included (e.g., ASID[31:0]). A reserved bit is indicated by "#.
   - Certain kinds of bits, such as those of timer counters, are not assigned bit names. In such cases, the entry under Bit Name is blank.

3. **Initial value**: Indicates the value of each bit immediately after a power-on reset, i.e., the initial value.
   - C: The initial value is 0.
   - 1: The initial value is 1.
   - ?: The initial value is undefined.

4. **R/W**: For each bit and bit field, this entry indicates whether the bit or field is readable or writable, or both writing to and reading from the bit or field are impossible. The notation is as follows:
   - R/W: The bit or field is readable and writable.
   - R/WR: The bit or field is readable and writable. However, writing is only performed by the clearing.
   - R/WR: The bit or field is readable and writable. Writing 0 to the bit initializes the bit.
   - R/WR: The bit or field is readable and writable. Writing 1 to the bit initializes the bit.
   - R/W: The bit or field is readable.
   - R/W: The bit or field is readable and writable. When writing to the register, write the value under Initial Value in the bit chart to the reserved bits.
   - W: The bit or field is writable.
   - W: The bit or field is writable.

5. **Description**: Describes the function of the bit or field and specifies the values for writing.

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Contents

1. Overview ............................................................................................................................................... 1-1
  1.1 Introduction ....................................................................................................................................... 1-1
  1.2 System Configuration Diagram ....................................................................................................... 1-2
  1.3 List of Specifications .......................................................................................................................... 1-3
    1.3.1 ARM Core .................................................................................................................................... 1-3
    1.3.2 CPU Core Peripherals ................................................................................................................ 1-4
    1.3.3 External Bus Module ................................................................................................................... 1-5
    1.3.4 Internal Bus Module ................................................................................................................... 1-7
    1.3.5 Local Memory ............................................................................................................................ 1-8
    1.3.6 Graphics Units ........................................................................................................................... 1-9
    1.3.7 Video Processing ....................................................................................................................... 1-11
    1.3.8 Sound Interface ........................................................................................................................ 1-14
    1.3.9 Storage ....................................................................................................................................... 1-16
    1.3.10 Network ..................................................................................................................................... 1-17
    1.3.11 Timer ........................................................................................................................................ 1-17
    1.3.12 Peripheral Module .................................................................................................................... 1-19
    1.3.13 Others ....................................................................................................................................... 1-22
  1.4 Power Supply Voltages and Temperature Range .............................................................................. 1-22

2. Area Map ............................................................................................................................................... 2-1

3. Pin Assignment ....................................................................................................................................... 3-1
  3.1 Top View (Left) ................................................................................................................................. 3-1
  3.2 Top View (Right) ............................................................................................................................... 3-2
  3.3 Mode Pin Settings ............................................................................................................................. 3-3

4. Pin Multiplexing ..................................................................................................................................... 4-1
  4.1 List of Multiplexed Pin Functions .................................................................................................... 4-1
  4.2 Pin States ......................................................................................................................................... 4-18
  4.3 Handling of Unused Pins .................................................................................................................. 4-27

5. Pin Function Controller (PFC) ............................................................................................................. 5-1
  5.1 Overview ......................................................................................................................................... 5-1
    5.1.1 Features ...................................................................................................................................... 5-1
    5.2 Register Configuration .................................................................................................................... 5-2
    5.3 Register Description ....................................................................................................................... 5-4
      5.3.1 LSI Multiplexed Pin Setting Mask Register (PMMR) ................................................................. 5-5
      5.3.2 GPIO/Peripheral Function Select Register 0 (GPSR0) ............................................................ 5-5
      5.3.3 GPIO/Peripheral Function Select Register 1 (GPSR1) ............................................................ 5-7
      5.3.4 GPIO/Peripheral Function Select Register 2 (GPSR2) ............................................................ 5-9
      5.3.5 GPIO/Peripheral Function Select Register 3 (GPSR3) ............................................................ 5-11
      5.3.6 GPIO/Peripheral Function Select Register 4 (GPSR4) ............................................................ 5-13
      5.3.7 GPIO/Peripheral Function Select Register 5 (GPSR5) ............................................................ 5-15
      5.3.8 GPIO/Peripheral Function Select Register 6 (GPSR6) ............................................................ 5-17
      5.3.9 Peripheral Function Select Register 0 (IPSR0) ........................................................................ 5-19
      5.3.10 Peripheral Function Select Register 1 (IPSR1) ....................................................................... 5-20
      5.3.11 Peripheral Function Select Register 2 (IPSR2) ....................................................................... 5-21
      5.3.12 Peripheral Function Select Register 3 (IPSR3) ....................................................................... 5-22
      5.3.13 Peripheral Function Select Register 4 (IPSR4) ....................................................................... 5-23
      5.3.14 Peripheral Function Select Register 5 (IPSR5) ....................................................................... 5-24
5.3.15 Peripheral Function Select Register 6 (IPSR6) ................................................................. 5-25
5.3.16 Peripheral Function Select Register 7 (IPSR7) ................................................................. 5-26
5.3.17 Peripheral Function Select Register 8 (IPSR8) ................................................................. 5-27
5.3.18 Peripheral Function Select Register 9 (IPSR9) ................................................................. 5-28
5.3.19 Peripheral Function Select Register 10 (IPSR10) ............................................................ 5-29
5.3.20 Peripheral Function Select Register 11 (IPSR11) ............................................................ 5-30
5.3.21 Peripheral Function Select Register 12 (IPSR12) ............................................................ 5-31
5.3.22 Peripheral Function Select Register 13 (IPSR13) ............................................................ 5-32
5.3.23 Module Select Register (MOD_SEL) .............................................................................. 5-39
5.3.24 Module Select Register 2 (MOD_SEL2) ......................................................................... 5-41
5.3.25 Module Select Register 3 (MOD_SEL3) ......................................................................... 5-44
5.3.26 LSI Pin Pull-Up Control Register 0 (PUPR0) ................................................................. 5-46
5.3.27 LSI Pin Pull-Up Control Register 1 (PUPR1) ................................................................. 5-48
5.3.28 LSI Pin Pull-Up Control Register 2 (PUPR2) ................................................................. 5-50
5.3.29 LSI Pin Pull-Up Control Register 3 (PUPR3) ................................................................. 5-52
5.3.30 LSI Pin Pull-Up Control Register 4 (PUPR4) ................................................................. 5-54
5.3.31 LSI Pin Pull-Up Control Register 5 (PUPR5) ................................................................. 5-56
5.3.32 LSI Pin Pull-Up Control Register 6 (PUPR6) ................................................................. 5-58
5.3.33 SD Control Register 0 (IOCTRL0) ............................................................................... 5-60
5.3.34 SD Control Register 1 (IOCTRL1) ............................................................................... 5-62
5.3.35 TDSEL Control Register (IOCTRL2) ........................................................................... 5-63
5.3.36 POC Control Register (IOCTRL3) ............................................................................... 5-64
5.3.37 IICDVFS and TDBG IO cell control register (IOCTRL7) ............................................... 5-66
5.4 Operation .......................................................................................................................... 5-67
5.4.1 Function Setting for Multiplexed Pins ........................................................................ 5-67
5.4.2 Setting Pull-Up/Down Resistors..................................................................................... 5-68

Main Revisions and Additions in this Edition ........................................................................ A-1
1. Overview

1.1 Introduction

The RZ/G1E is that features the basic functions for Rich Graphics Applications.

The RZ/G1E includes:

- Two 1.0-GHz ARM Cortex®-A7 MPCore® cores,
- Memory controller for DDR3-SDRAM (DDR3-1333) with 32 bits × 1 channel,
- Three-dimensional graphics engines,
- Video processing unit,
- 2 channels Display Output,
- 2 channels Video Input,
- Sound processing unit,
- SD card host interface,
- USB2.0 interfaces, and
- CAN interface.

Also, a full implementation of the extremely expandable and Internal AXI bus has been adopted for the RZ/G1E.

This bus structure is optimized for maximum system performance, leading to the realization of high-performance and cost-effective premium in-vehicle infotainment systems.

Notes: 1. ARM is a registered trademark and Cortex is a trademark of ARM Limited. All other brands or product names are the property of their respective holders.
1.2 System Configuration Diagram

Figure 1.1 RZ/G1E System Configuration
## 1.3 List of Specifications

### 1.3.1 ARM Core

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>System CPU Cortex-A7</td>
<td>• ARM Cortex-A7 Dual MPCore 1.0 GHz</td>
</tr>
<tr>
<td></td>
<td>• L1 I/D cache 32/32 KBytes, L2 cache 512 KBytes</td>
</tr>
<tr>
<td></td>
<td>• NEON™/VFPv4 supported</td>
</tr>
<tr>
<td></td>
<td>• Security extension supported</td>
</tr>
<tr>
<td>ARM debugger (CoreSight™)</td>
<td>• CoreSight system compliant</td>
</tr>
<tr>
<td></td>
<td>• JTAG/SWD I/F supported</td>
</tr>
<tr>
<td></td>
<td>• CoreSight ETR 16 KBytes for program flow trace</td>
</tr>
<tr>
<td></td>
<td>• CoreSight ETR 4 KBytes for system trace</td>
</tr>
</tbody>
</table>
### 1.3.2 CPU Core Peripherals

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
</table>
| Operating clock pulse generation circuit (CPG) | - Generates the clocks from external clock (EXTAL).  
- Maximum Cortex-A7 clock: 1.0 GHz  
- Maximum AXI-bus clock: 260 MHz  
- Maximum SDRAM bus clock: DDR3-1333  
- Maximum media clock: 260 MHz  
- Maximum peripheral clock (HPϕ): 130 MHz  
- Module-standby mode supported  
- Includes module reset registers to control reset operation of individual on-chip peripheral modules |
| Reset (RESET)                              | - Includes one reset-signal external output port for external modules  
- Includes Boot Address Register etc. |
| Pin function controller (PFC)              | - Setting multiplexed pin functions for LSI pins  
Function of the RZ/G1E pin selectable by setting the registers in the PFC module  
Module selection  
Enable and disable the functions of RZ/G1E LSI pins to which pin functions from multiple pin groups are assigned by setting the registers in the PFC module.  
Pull-up control for each LSI pin  
On/off of the pull-up resistor on each LSI pin can be controlled by setting the registers in the PFC module.  
Control of SDIO functions  
SDIO functions, including the driving ability of pins for the SDIF, can be controlled by setting registers of the PFC |
| General-purpose I/O (GPIO)                 | - General-purpose I/O ports: 208 ports  
- Supports GPIO interrupts. |
1.3.3 External Bus Module

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Local bus state controller (LBSC)</td>
<td>• EX-BUS interface: max. 16-bit bus</td>
</tr>
<tr>
<td></td>
<td>• Frequency: 65 MHz</td>
</tr>
<tr>
<td></td>
<td>• External area divided into several areas and managed</td>
</tr>
<tr>
<td></td>
<td>— Allocation to space of area 0, area 1, and area 6 or allocation to space of area 0 only is selected at startup time.</td>
</tr>
<tr>
<td></td>
<td>— Area 0 supports 128-MByte memory space (startup mode).</td>
</tr>
<tr>
<td></td>
<td>— Space of area 6 is divided into up to six areas (capacity of each area variable) and managed</td>
</tr>
<tr>
<td></td>
<td>— I/F settings, bus width settings, and wait state insertion are possible for each area</td>
</tr>
<tr>
<td></td>
<td>• SRAM interface</td>
</tr>
<tr>
<td></td>
<td>— Wait states can be inserted through register settings</td>
</tr>
<tr>
<td></td>
<td>Period of waiting is set in cycle unit, and the maximum value is 15.</td>
</tr>
<tr>
<td></td>
<td>— EX_WAIT pin can be used for wait state insertion</td>
</tr>
<tr>
<td></td>
<td>— Connectable bus widths: 16 bits or 8 bits</td>
</tr>
<tr>
<td></td>
<td>• Burst ROM interface</td>
</tr>
<tr>
<td></td>
<td>— Wait states can be inserted through register settings</td>
</tr>
<tr>
<td></td>
<td>— Number of bursts can be set through register settings</td>
</tr>
<tr>
<td></td>
<td>— Connectable bus widths: 16 bits or 8 bits</td>
</tr>
<tr>
<td></td>
<td>• Byte-control SRAM interface (available with areas 1 and 6 only)</td>
</tr>
<tr>
<td></td>
<td>— Byte-control SRAM interface</td>
</tr>
<tr>
<td></td>
<td>— Wait states can be inserted through register settings</td>
</tr>
<tr>
<td></td>
<td>— EX_WAIT pin can be used for wait state insertion</td>
</tr>
<tr>
<td></td>
<td>— Connectable bus widths: 16 bits or 8 bits</td>
</tr>
<tr>
<td></td>
<td>• ATA interface (two ports)</td>
</tr>
<tr>
<td></td>
<td>— Wait states can be inserted through register settings</td>
</tr>
<tr>
<td></td>
<td>— Supports PIO modes 0 through 4</td>
</tr>
<tr>
<td></td>
<td>— Supports multi-word modes 0 through 2</td>
</tr>
<tr>
<td></td>
<td>— Supports Ultra DMA modes 0 through 4 (Ultra ATA66)</td>
</tr>
<tr>
<td></td>
<td>— Ready timeout detection (detection time (ns) = EX-BUS operating frequency (ns) × 100 clock cycles)</td>
</tr>
<tr>
<td></td>
<td>• Supports external buffer enable/direction control</td>
</tr>
</tbody>
</table>

- Supports external buffer enable/direction control
### 1. Overview

<table>
<thead>
<tr>
<th>Item Description</th>
<th>Item Description</th>
</tr>
</thead>
</table>
| **LBSC-DMAC**    | - Number of channels: LBSC-DMAC three channels  
|                  | - Address space: Physical address space  
|                  | - Transfer direction: Peripheral to memory (AXI-bus), memory (AXI-bus) to peripheral  
|                  | - Data packing for peripheral read data: Memory write data length is selectable as transfer data length to memory side.  
|                  | - Transfer data length: Peripheral (APB-bus) side: 1, 2, 4 bytes Memory (AXI-bus) side: 4 or 16 (channel 2), 32 (channel 0 and 1) bytes  
|                  | - Transfer burst length: 1, 8 (transfer with a burst length of 8 supported only for LBSCDMAC00, 01)  
|                  | - Number of transfers  
|                  |   - Maximum number of transfers: 16 M (16,777,216 transfers), 64M (67,108,864 transfers), (64 M transfers supported only for LBSC-DMAC00)  
|                  |   - Minimum number of transfers: One  
|                  | - Address mode: Dual address mode  
|                  | - Transfer modes: Single transfer mode, continuous transfer mode  
|                  | - Transfer end interrupt: Occurs at the end of the number of transfers specified in the register  
|                  | **DDR3-SDRAM bus state controller (DBSC)**  
|                  |   - 1 channel (32-bit bus)  
|                  |   - DDR3-SDRAM can be connected directly.  
|                  |   - Memory Size: Up to 2 GB (8-Gbit memory × 2)  
|                  |   - Data bus width: 32 bits × 1  
|                  |   - Auto Refresh/Self Refresh/Partial Array Self Refresh supported  
|                  |   - Deep-Power-Down-Mode supported  
|                  |   - Auto Pre-charge Mode/Bank Active Mode  
|                  |   - DDR Back Up supported  
| **Memory connections** | **DDR3-SDRAM compliant to JEDEC JESD79-3E**  
|                  |   - Supports from 512-Mbit to 8-Gbit memory unit configurations  
|                  |   - 32-bit DDR3-1333 (four units with 8-bit width)  

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## 1.3.4 Internal Bus Module

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
</table>
| AXI-bus                            | • On-chip main bus  
  — Bus protocol: AXI3 with QoS control  
  — Frequency: 260 MHz  
  — Bus width: 256 bits/128 bits  
• On-chip CPU & GPU main bus  
  — Corelink™ CCI-400 Cache Coherent Interconnect - r0p3  
  — Bus protocol: AMBA®4 ACE™ and ACE-Lite™  
  — Frequency: 520 MHz  
  — Bus width: 128 bits |
| Direct memory access controller (SYS-DMAC) | • 30 channels for ARM domain  
• Address space: 4 GBytes on architecture  
• Data transfer length: Byte, word (2 Bytes), longword (4 Bytes), 8 Bytes, 16 Bytes, 32 Bytes and 64 Bytes  
• Maximum number of transfer times: 16,777,216 times  
• Transfer request:  
  Selectable from on-chip peripheral module request and auto request  
• Bus mode:  
  Selectable from normal mode and slow mode  
• Priority: Selectable from fixed channel priority mode and round-robin mode  
• Interrupt request: Supports interrupt request to CPU at the end of data transfer  
• Repeat function: Automatically resets the transfer source, destination, and count at the end of DMA transfer (by descriptor function)  
• Descriptor function (each channel) supported  
• MMU (each channel) supported  
• Channel bandwidth arbiter (each channel) |
| Direct memory access controller (Audio-DMAC) | • 13 channels for Audio domain  
• Address space: 4 GBytes on architecture  
• Data transfer length: Byte, word (2 Bytes), longword (4 Bytes), 8 Bytes, 16 Bytes, 32 Bytes and 64 Bytes  
• Maximum number of transfer times: 16,777,216 times  
• Transfer request:  
  Selectable from on-chip peripheral module request and auto request  
• Bus mode:  
  Selectable from normal mode and slow mode  
• Priority: Selectable from fixed channel priority mode and round-robin mode  
• Interrupt request: Supports interrupt request to CPU at the end of data transfer  
• Repeat function: Automatically resets the transfer source, destination, and count at the end of DMA transfer (by descriptor function)  
• Descriptor function (each channel) supported  
• MMU (each channel) supported  
• Channel bandwidth arbiter (each channel) |
### 1. Overview

#### Item Description

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
</table>
| Direct memory access controller (Audio-DMAC-Peripheral-Peripheral) | Audio-DMAC (for transfer from Peripheral to Peripheral)
  - 29 channels for audio domain
  - Data transfer length: longword (4 Bytes)
  - Transfer count: Transfer count is not specified (DMA transfer is made from the transfer-start to transfer-stop settings.)
  - Transfer request: Selectable from on-chip audio peripheral module request
  - Priority: round-robin mode
  - Interrupt request: not supports interrupt request to CPU at the end of data transfer |
| IPMMU | An IPMMU is a memory management unit (MMU) which provides address translation and access protection functionalities to processing units and interconnect networks. |
| Interrupt controller (INTC) | INTC-SYS |
| | 10 interrupt pins which can detect external interrupts |
| | Fall/rise/high level/low level detection is selectable |
| | On-chip peripheral interrupts: Priority can be specified for each module |
| | Max. 384 shared peripheral interrupts supported |
| | 16 software interrupts that have been generated and 6 private peripheral interrupts supported |
| | 32-level priority selectable |
| | Trust Zone supported |

#### 1.3.5 Local Memory

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>INTRAM</td>
<td>RAM0 of 72 KBytes</td>
</tr>
<tr>
<td></td>
<td>RAM1 of 4 KBytes</td>
</tr>
<tr>
<td></td>
<td>RAM2 of 256 KBytes</td>
</tr>
</tbody>
</table>
### 1.3.6 Graphics Units

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>3D graphics engine (3DGE)</strong></td>
<td>- Imagination Technologies PowerVR Series5 SGX540 (260 MHz)&lt;br&gt;- USSE2 delivers twice the peak floating point and instruction throughput of Series5 USSE&lt;br&gt;- YCbCr and color space accelerators for improved performance&lt;br&gt;- Upgraded PowerVR Series5XT shader-driven tile-based deferred rendering (TBDR) architecture&lt;br&gt;- Support for all industry standard mobile and desktop graphics APIs and operating systems</td>
</tr>
<tr>
<td><strong>Display unit (DU)</strong></td>
<td><strong>Screen size and number of composite planes</strong>&lt;br&gt;- Maximum screen size: 4095 × 2047&lt;br&gt;- Number of planes specifiable: 1 (ARGB8888)</td>
</tr>
<tr>
<td></td>
<td><strong>CRT scanning method</strong>&lt;br&gt;- Non-interlaced, interlaced sync, interlaced sync &amp; video</td>
</tr>
<tr>
<td></td>
<td><strong>Synchronization method</strong>&lt;br&gt;- Master, TV sync</td>
</tr>
<tr>
<td></td>
<td><strong>Internal color palette</strong>&lt;br&gt;- Includes four color palette planes which can display 256 of 260 thousands colors at the same time.</td>
</tr>
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<td></td>
<td><strong>Digital RGB</strong>&lt;br&gt;- Two output channel&lt;br&gt;- Output on rising and falling edges of the synchronizing signal (resolution for the same display)&lt;br&gt;- 8-bit precision for each RGB color</td>
</tr>
<tr>
<td></td>
<td><strong>Blending ratio settings</strong>&lt;br&gt;- Number of color palette planes with blending ratio: 4</td>
</tr>
<tr>
<td></td>
<td><strong>Dot clock</strong>&lt;br&gt;- Switchable between external input and internal clock</td>
</tr>
<tr>
<td></td>
<td><strong>Color management</strong>&lt;br&gt;- ( \gamma ) correction, gain correction&lt;br&gt;- Applies correction of color (skin color adjustment and color correction set in memory) in terms of color phase, brightness, and chromaticity for a specified range of colors or for the full range of colors</td>
</tr>
<tr>
<td></td>
<td><strong>Interface</strong>&lt;br&gt;- RGB888 × 2</td>
</tr>
<tr>
<td><strong>De-Compression Unit (DCU)</strong></td>
<td><strong>De-compression to row picture data from compressed data by Run-length method</strong></td>
</tr>
<tr>
<td></td>
<td><strong>Input data format:</strong> Compressed data by Run-Length method (ARGB8888, RGB888, RGB565, RGBA4444, RGBA5551, and A8)</td>
</tr>
<tr>
<td></td>
<td><strong>Output data format:</strong> Row data (ARGB8888, RGB888, RGB565, RGBA4444, RGBA5551, and A8)</td>
</tr>
<tr>
<td></td>
<td><strong>2 interrupt sources:</strong> Conversion finished, and Check sum error&lt;br&gt;- Including DMAC (DCU_DMAC)</td>
</tr>
</tbody>
</table>
### Item Description

**Video input (VIN)**
- Input data format
  - 8-, 10-, or 12-bit YCbCr422 (CbYCrY format)
  - 16-bit YCbCr422 (8 bits (Y) + 8 bits (CbCr) format)
  - 20-bit YCbCr422 (10 bits (Y) + 10 bits (CbCr) format)
  - 24-bit YCbCr422 (12 bits (Y) + 12 bits (CbCr) format)
  - 18-bit RGB666
  - 24-bit RGB888

**Clipping function**
- Up to 2048 × 2048

**Horizontal scaling**
- Uses a 9-tap multi-phase filter.
  - Up to two times, but only scaling down is possible for HD1080i or HD720P data.

**Vertical scaling**
- Scaling by linear interpolation
  - Up to three times, but only scaling down is possible for HD1080i or HD720P data.

**Output format**
- RGB-565, ARGB-1555, YCbCr422, RGB888 (channel 0,1), YC separation, and extraction of the Y component
### 1.3.7 Video Processing

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
</table>
| Video signal processor 1 (VSP1) | The VSP1 is the successor IP of Renesas’ VIO6-IP series, and has the following features.  
(1) Supports Various Data Formats and Conversion  
  — Supports YCbCr444/422/420, RGB, αRGB, αplane  
  — Color space conversion and changes to the number of colors by dithering  
  — Color keying  
(2) Full HD Video Processing  
  — Up and down scaling with arbitrary scaling ratio  
  — Super resolution processing  
  — Blending of four picture layers and raster operations (ROPs)  
(3) Full HD Picture Quality/Color Correction with 1D/3D Look Up Table (LUT)  
  — Dynamic γ correction and gain correction  
  — Correction of color (to adjust skin tones or colors in memory)  
  — Hue, brightness, and saturation adjustment  
  — 1D histogram  
(4) Direct Connection to Display Module  
  — Display unit (DU) supported |
The VCP3 is a multi-codec module which provides encoding and decoding capabilities on the basis of multiple video coding schemes, e.g., H.264/AVC, MPEG-4, MPEG-2 and VC-1.

This IP (Intellectual Property) is a multi codec that processes the frame or each field by controlling software for VCP3 executed on host CPU.

The VCP3 has the following features:

- Support for multiple codecs
  - H.264/MPEG-4 AVC HP (High Profile) and MVC SHP (Stereo High Profile) encoding and decoding
  - H.262/MPEG-2 MP (Main Profile) decoding
  - MPEG-4 ASP (Advanced Simple Profile) decoding
  - VC-1 SP/MP/AP (Simple, Main, Advanced Profile) decoding
  - H.263 Baseline decoding
  - AVS Jizhun Profile decoding
  - VP8 decoding
- Support for HDTV resolutions
  - 1920 pixels × 1080 lines × 60 frames/second × 1 channel
  - Maximum performance will change with securable bus bandwidth.
- Data handling on a picture-by-picture basis
  - Encodes/decodes data one picture (frame or field) at a time.
- High picture quality
  - Supports the H.264 high-efficiency coding tools (CABAC, 8 × 8 frequency conversion, and quantization matrix).
  - High-efficiency motion vector detection by a combination of discrete search and trace search
  - Highly efficient real-time intra-prediction by Prediction from Original Image (POI)
  - Optimal-mode selection by Rate-Distortion (RD) cost evaluation
  - Picture quality control based on activity analysis results which match visual models
- Low power dissipation
  - Dynamically disables the clocks for the entire VCP3.
  - Dynamically disables the clocks for individual submodules.
- Includes its own dedicated 64-KByte cache

---

The FDP1 is the de-interlacing module which converts the interlaced video to progressive video, and has the following features.

1. Supports various data formats
   - Input: YCbCr444/422/420
   - Output: YCbCr444/422/420 and RGB/αRGB
2. Full HD video processing performance
3. High image quality de-interlacing algorithm
   - Motion adaptive de-interlacing
   - Accurate still detection
   - Diagonal line interpolation (DLI)
## 2-dimensional DMAC (2D-DMAC)

- Supports conversion between various RGB formats.
- Image extraction function: Capable of extracting an image and storing it as a separate image in the RAM.
- Image rotation/reversal function: Reverses an image vertically/horizontally or rotates it by 90°/270°.
- Simple scaling function: Capable of scaling an image two times in the X or Y direction.
- Format conversion
- Supports conversion from RGB to RGB and from YCbCr to YCbCr.
### 1.3.8 Sound Interface

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Sampling rate converter unit (SCU)</strong></td>
<td>• Includes six SRC modules&lt;br&gt;  ➢ Supports the quality suitable for audio sound (THD+N -132dB) : four modules&lt;br&gt;  ➢ Supports the quality suitable for voice sound (THD+N -96dB) : two modules&lt;br&gt;  ➢ The SRC module is capable of correcting phase change and delay (timing jitter) generated during data transfer over external memories or external devices.&lt;br&gt;  ➢ The channel count conversion unit (CTU), mixer (MIX), and digital mute and volume function (DVC) can be used on two fixed output channels.</td>
</tr>
<tr>
<td><strong>Sampling rate conversion (SRC)</strong></td>
<td>• Capable of asynchronous sampling rate conversion&lt;br&gt;  • Supports resolutions up to 24 bits&lt;br&gt;  • Two kinds of filter type for SRC.&lt;br&gt;  ➢ Supports the quality suitable for audio sound (THD+N -132dB) : Realized the filter by passband <a href="mailto:-1dB@0.4575FS">-1dB@0.4575FS</a>, cutoff <a href="mailto:-18dB@0.5FS">-18dB@0.5FS</a>.&lt;br&gt;  ➢ Supports the quality suitable for voice sound (THD+N -96dB) : Realized the filter by passband <a href="mailto:-1dB@0.4561FS">-1dB@0.4561FS</a>, cutoff <a href="mailto:-72dB@0.5FS">-72dB@0.5FS</a>. (Characteristics of each filter is written in the equivalent/up-sampling cases.)&lt;br&gt;  ➢ Automatically generates antialiasing filter coefficients&lt;br&gt;  ➢ For monaural to eight-channel sound sources</td>
</tr>
<tr>
<td><strong>Channel count conversion unit (CTU)</strong></td>
<td>• Downmixing and splitter functions&lt;br&gt;  ➢ Conversion of eight input channels into four output channels&lt;br&gt;  ➢ Conversion of six input channels into two output channels&lt;br&gt;  ➢ Conversion of two input channels into four sets of two output channels&lt;br&gt;  ➢ Conversion of one input channel into eight sets of one output channel&lt;br&gt;  ➢ No conversion</td>
</tr>
<tr>
<td><strong>Mixer (MIX)</strong></td>
<td>• Mixing (adds) two to four sources into one&lt;br&gt;  • Ratio for adding sources is selectable&lt;br&gt;  • Ratio is dynamically changeable&lt;br&gt;  • Mixing with volume ramp is available (ramp period is selectable)</td>
</tr>
<tr>
<td><strong>Digital volume and mute function (DVC)</strong></td>
<td>• Volume control function including digital volume, volume ramp, and zero-crossing mute&lt;br&gt;  • The digital volume function is specified by a 24-bit fixed-point value within the range from 0 to 8 times (mute, or -120 to 18 dB)&lt;br&gt;  • The volume ramp function can be used for soft mute, fade-in, fade-out, or desired volume adjustment&lt;br&gt;  • The volume ramp period can be changed within the sampling range from the 0th to 23rd power of 2&lt;br&gt;  • The zero-crossing mute function silences the sound at the zero-crossing point of the audio data</td>
</tr>
</tbody>
</table>
## Overview

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Serial sound interface unit (SSIU)</td>
<td>Overall specification</td>
</tr>
<tr>
<td></td>
<td>• Includes ten SSI modules functioning as interfaces with external devices.</td>
</tr>
<tr>
<td></td>
<td>— Supports short and long formats</td>
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<td></td>
<td>— Supports TDM format (six modules of ten modules can be used for this function)</td>
</tr>
<tr>
<td></td>
<td>• Max. 4 independent stereo sound sources in a TDM format can be distributed to each course. Moreover Max. 4 independent stereo sound source can be combined output in TDM format.</td>
</tr>
<tr>
<td>Serial sound interface (SSI)</td>
<td>Operating mode: non-compressed mode (Not support compressed mode)</td>
</tr>
<tr>
<td></td>
<td>• Supports versatile serial audio formats (I2S/left justified/right justified)</td>
</tr>
<tr>
<td></td>
<td>• Supports master/slave functions</td>
</tr>
<tr>
<td></td>
<td>• Programmable word clock, bit clock generation functions</td>
</tr>
<tr>
<td></td>
<td>• Multichannel format functions (up to four channels)</td>
</tr>
<tr>
<td></td>
<td>• Supports 8-/16-/20-/22-/24-/32-bit data formats</td>
</tr>
<tr>
<td></td>
<td>• Supports TDM mode</td>
</tr>
<tr>
<td></td>
<td>• Supports WS continue mode</td>
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<tr>
<td></td>
<td>• The DMA controller or interrupts control the transfer of data to and from the SSI module.</td>
</tr>
<tr>
<td></td>
<td>• Supports short and long frames for monaural data (valid data lengths are 8 and 16 bits)</td>
</tr>
<tr>
<td></td>
<td>• Up to nine independent clock signals can be input.</td>
</tr>
<tr>
<td>Audio clock generator (ADG)</td>
<td>Selection or division of audio clock signals</td>
</tr>
</tbody>
</table>
### Storage

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
</table>
| USB2.0 host & function module (USB2.0) | 2 channels (Host only 1 channel/Host-Function 1 channel)  
  • PHY integrated  
  • USB Host (EHCI/OHCI) 2LINK  
  • Compliance with USB2.0  
  • USB Function 1LINK  
  • Compliance with USB2.0 (High-Speed)  
  • Interrupt request  
  • Internal dedicated DMA |
| SD host interface (SDHI) | 3 channels  
  • Interfaces 0: Support SDR104 class transfer rate at Max. 97.5 MBytes/sec. @ 195 MHz, and SDXC. Does not support CPRM.  
  • Interfaces 1 and 2: Support SDR50 class transfer rate at Max. 48 MBytes/sec. @ 97.5 MHz, and SDXC. Does not support CPRM.  
  • Supports SD memory/SDIO interface (1-/4-bit SD buses).  
  • Error check function: CRC7 (command/response), CRC16 (data)  
  • Card detection function  
  • Supports write protection |
| Multi-media card interface (MMCIF) | 1 channel  
  • MMC 4.41 base  
  • eMMC controllable  
  • Data bus: 1/4/8-bit MMC mode (not support SPI mode)  
  • Support block transfer (not support stream transfer)  
  • Block size in multi-block transfer: 512 Bytes |
## 1.3.10 Network

<table>
<thead>
<tr>
<th>Item Description</th>
<th>Description</th>
</tr>
</thead>
</table>
| CAN interface (CAN) | • 2 channels  
| | • Supports CAN specification 2.0B  
| | • ISO-11898-1 compliant  
| | • Maximum bit rate: 1 Mbps  
| Message box | • Normal mode: 32 receive-only mailboxes and 32 mailboxes for transmission/reception  
| | • FIFO mode: 32 receive-only mailboxes and 24 mailboxes for transmission/reception, 4-stage FIFO for transmission, and 4-stage FIFO for reception  
| Reception | • Data frame and remote frame can be received  
| | • Selectable receiving ID format  
| | • Selectable overwrite mode (message overwritten) or overrun mode (message discarded)  
| Acceptance filter | • Mask can be enabled or disabled for each mailbox  
| Transmission | • Data frame and remote frame can be transmitted  
| | • Selectable transmitting ID format (only standard ID, only extended ID, or both IDs)  
| | • Selectable ID priority mode or mailbox number priority mode  
| Sleep mode for reducing power consumption |  
| Ethernet AVB | • Supports IEEE802.1BA, IEEE802.1AS, IEEE802.1Qav and IEEE1722 functions  
| | • Supports transfer at 1000 Mbps and 100 Mbps  
| | • Magic packet detection  
| | • Supports Reception Filtering to separate streaming frames from different sources  
| | • Supports interface conforming to IEEE802.3 PHY GMII (Gigabit Media Independent Interface) and MII (Media Independent Interface)  
| Ethernet MAC | • IEEE802.3u MAC (Ether) function  
| | • Supports transfer at 10 and 100 Mbps  
| | • Flow control conforming to IEEE802.3x or back pressure system  
| | • Supports interface conforming to IEEE802.3u  
| | • Magic packet detection  
| | • Includes DMAC  
| | • Supports RMII (Reduced Media Independent Interface)  

## 1.3.11 Timer

<table>
<thead>
<tr>
<th>Item Description</th>
<th>Description</th>
</tr>
</thead>
</table>
| Watchdog timer (WDT) | • Single channel  
| | • Internal 16-bit watchdog timer operated by RCLK  
| | • Programmable overflow time-period: more than 1 hour count capable  
| Timer pulse unit (TPU) | • 4-channels  
| | • 16-bit timers  
| | • Each channel outputs PWM  

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<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
</table>
| Compare match timer 0 (CMT0) | - Two channels  
|                              | - 32-bit timer (16 bits/32 bits can be selected)  
|                              | - Source clock: RCLK clock  
|                              | - Compare match function provided  
|                              | - Interrupt requests |
| Compare match timer 1 (CMT1) | - Eight channels  
|                              | - 48-bit timer (16 bits/32 bits/48 bits can be selected)  
|                              | - Source clock: RCLK/system clock  
|                              | - Compare match function provided  
|                              | - Interrupt requests |
| Timer unit (TMU)             | - 4 sets of 3-channel 32-bit timer  
|                              | - Auto-reload type 32-bit down counter  
|                              | - Internal prescaler  
|                              | - Interrupt request  
|                              | - 2 channels for input capture |
### 1.3.12 Peripheral Module

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
</table>
| I2C bus interface (IIC) | 1 channel for 3.3 V LVTTL buffers and 1 channel for open drain type IO buffer  
Supports single master transmission/reception  
Interrupt request  
DMAC request |
| Multi-master I2C bus interface (I2C) | 6 channels for general purpose  
Philips I2C bus interface method supported  
Master/slave functions  
Multi-master functions  
Transfer rate up to 400 kbps supported  
Programmable clock generation from the system clock |
| Serial communication interface with FIFO (SCIFA) | 6 channels  
Internal 64-Byte transmit/receive FIFOs  
High-speed UART  
Internal prescaler  
Clock synchronous serial communications possible  
Support edge selection function  
Interrupt request, DMAC request and DMA multi-Byte transfer supported  
Asynchronous mode  
Clock synchronous mode |
| Serial communication interface with FIFO (SCIFB) | 3 channels  
Internal 256-Byte transmit/receive FIFOs  
High-speed UART  
Internal prescaler  
Clock synchronous serial communications possible  
Support edge selection function  
Interrupt request, DMAC request and DMA multi-Byte transfer supported  
Asynchronous mode (modem control is enabled)  
Clock synchronous mode |
1. Overview

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Serial communication interface with FIFO (SCIF)</td>
<td>Overall specification</td>
</tr>
<tr>
<td></td>
<td>• 6 channels</td>
</tr>
<tr>
<td></td>
<td>• Asynchronous, clock-synchronized modes</td>
</tr>
<tr>
<td></td>
<td>• Asynchronous serial communication mode</td>
</tr>
<tr>
<td></td>
<td>The SCIF performs serial data communication based on a character-by-character asynchronous system. This feature enables serial data communication with standard asynchronous communication chips that support Universal Asynchronous Receiver/Transmitter (UART) or Asynchronous Communication Interface Adapter (ACIA). There is a choice of eight serial data transfer formats.</td>
</tr>
<tr>
<td></td>
<td>— Data length: 7 bits or 8 bits</td>
</tr>
<tr>
<td></td>
<td>— Stop bits: 1 bit or 2 bits</td>
</tr>
<tr>
<td></td>
<td>— Parity: Even/odd/none</td>
</tr>
<tr>
<td></td>
<td>— Receive error detection: Parity, framing, and overrun errors</td>
</tr>
<tr>
<td></td>
<td>— Break detection:</td>
</tr>
<tr>
<td></td>
<td>A break is detected when a framing error lasts for more than 1 frame length at Space 0 (low level).</td>
</tr>
<tr>
<td></td>
<td>When a framing error occurs, a break can also be detected by reading the RX pin level directly from the serial port register (SCSPT).</td>
</tr>
<tr>
<td></td>
<td>• Clock synchronous serial communication mode</td>
</tr>
<tr>
<td></td>
<td>The SCIF performs serial data communication synchronized with a clock. This feature enables serial data communication with other LSIs that support synchronous communication. There is a single serial data communication format for clock synchronous serial communication.</td>
</tr>
<tr>
<td></td>
<td>— Data length: 8 bits</td>
</tr>
<tr>
<td></td>
<td>— Receive error detection: Overrun errors</td>
</tr>
<tr>
<td></td>
<td>• Full-duplex communication capability</td>
</tr>
<tr>
<td></td>
<td>The SCIF has an independent transmitter and receiver that enable simultaneous transmission and reception. The transmitter and receiver both have a 16-stage FIFO buffer structure, enabling continuous serial data transmission and reception.</td>
</tr>
<tr>
<td></td>
<td>• On-chip baud rate generator, enabling any bit rate to be selected</td>
</tr>
<tr>
<td></td>
<td>The SCIF enables choice of a clock source for transmission/reception: a clock from the on-chip baud rate generator based on the internal clock or an external clock.</td>
</tr>
<tr>
<td></td>
<td>• Eight interrupt sources</td>
</tr>
<tr>
<td></td>
<td>The SCIF has eight types of interrupt sources: receive-data-ready, receive-FIFO-data-full, break, transmit-FIFO-data-empty, transmit-end, receive-error, overrun-error and time-out and enables any of them to be requested independently.</td>
</tr>
<tr>
<td></td>
<td>• DMA data transfer</td>
</tr>
<tr>
<td></td>
<td>When the transmit FIFO register is empty or the receive FIFO register has received data, issuing a DMA transfer request activates the DMA controller (DMAC) to execute a data transfer.</td>
</tr>
<tr>
<td></td>
<td>• The amount of data in the transmit/receive FIFO registers and the number of receive errors in receive data in the receive FIFO register are available.</td>
</tr>
<tr>
<td></td>
<td>• In asynchronous mode, a receive data ready (DR) or a timeout error (TO) can be detected during reception.</td>
</tr>
<tr>
<td>Item Description</td>
<td>Description</td>
</tr>
<tr>
<td>------------------</td>
<td>-------------</td>
</tr>
</tbody>
</table>
| Clock-synchronized serial interface with FIFO (MSIOF) | - 3 channels  
- Max. speed: 26 Mbps  
- Internal 64-Byte transmit FIFOs/internal 256-Byte receive FIFOs  
- Supports master and slave modes  
- Internal prescaler  
- Supports serial formats: IIS, SPI (master and slave modes)  
- Interrupt request, DMA request |
| Quad-SPI (QSPI) | - Single/Dual/Quad-SPI: serial slave transfer enabled  
- Supports master mode  
- SPCLK clock rate: 1…4080 in master mode; Max. 78 MHz |
| High-speed serial communication interface with FIFO (HSCIF) | - 3 channels  
- Asynchronous serial communication mode  
- Capable of full-duplex communication  
- On-chip baud rate generator, enabling any bit rate to be selected  
- Eight interrupt sources  
- DMA data transfer  
- Modem control functions (HRTS and HCTS) are stored.  
- The amount of data in the transmit/receive FIFO registers and the number of receive errors in receive data in the receive FIFO register are available.  
- A receive data ready (DR) or a timeout error (TO) can be detected during reception. |
| PWM timer (PWM) | - 7 channels  
- High-level width (10 bits) of PWM output can be set.  
- High-level periods (10 bits) of PWM can be set.  
- Periods in the range from two to $2^{24} \times 1024$ cycles of the $\Phi$ clock can be set.  
- Continuous pulse or single pulse output selectable |
| Boot Function (BOOT) | - System startup with selectable boot mode at power-on reset  
- Program downloaded to internal memory (LRAM)  
- Autorun function for the downloaded program |
1.3.13 Others

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
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<tbody>
<tr>
<td>JTAG</td>
<td>JTAG interface for CoreSight</td>
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<tr>
<td>Process</td>
<td>28nm Si-CMOS</td>
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<tr>
<td>Package</td>
<td>FC-BGA2121-501</td>
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</table>

1.4 Power Supply Voltages and Temperature Range

- Power supply voltage (typ.)
  - 1.8 V: (ETM, SD, LVCMOS I/F, Xtal, JTAG, Trace and RST)
  - 1.03 V: (core)
  - 1.5 V: (DDR3-I/O SSTL Mode:DDR3)
  - 3.3 V: (Others)
- Temperature range
  - Ta = –40°C to 85°C
  - Tc = –40°C to 105°C
2. Area Map

See section 2, Area Map in the RZ/G Series User’s Manual: Hardware.
### 3. Pin Assignment

#### 3.1 Top View (Left)

<table>
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<tr>
<th>1</th>
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<th>4</th>
<th>5</th>
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<td>D9</td>
<td>D4</td>
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<td>M0A6</td>
<td>M0A10</td>
<td>M0A11</td>
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<td>PRESET</td>
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<td>A1MD0</td>
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1/2 (left)
### 3.2 Top View (Right)

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<th>18</th>
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</table>

- : Multiplexed pin that function is selected by the Pin Function Controller (PFC) register and mode pin setting.
- : Mode pin assigned.

2/2 (right)
### 3.3 Mode Pin Settings

Input fixed values for BSMODE pins. These values cannot be changed after power is supplied. The values of pins MD0 to MD14, MD18 to MD21, MDT0 and MDT1 are input upon power-on reset using the PRESET pin. Power-on reset results in switching to a different function.

Legend: "0" means logic low level input, "1" means logic high level input.
"—" means either "0" or "1", but its level must be fixed.

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<tr>
<th>BSMODE</th>
<th>Reserved Fix to 0</th>
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<table>
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<tr>
<th>MD0</th>
<th>Free-Running Mode or Step-Up Mode</th>
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<td>Free-running mode</td>
</tr>
<tr>
<td>1</td>
<td>Step-up mode</td>
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<table>
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<tr>
<td>0</td>
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<td>0</td>
<td>area 0 boot (boot from external MaskROM)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>QSPI (48.75 MHz 16 KB transfer)</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Reserved</td>
</tr>
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<td>QSPI (78 MHz 16 KB transfer)</td>
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<td>QSPI (39 MHz 4 KB transfer)</td>
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<td>Area 0: 128 Mbytes</td>
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<tr>
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<td>Connects a crystal resonator to the EXTAL/XTAL pin</td>
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### Pin Assignment

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<th>MD10</th>
<th>MD21, MD20</th>
<th>MD11 [1:0]</th>
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<th>SDHI1</th>
<th>MMC</th>
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<td>—</td>
<td>—</td>
<td>Reserved</td>
<td>Reserved</td>
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<tr>
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<td>Normal mode</td>
<td>Normal mode</td>
</tr>
<tr>
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<td>0</td>
<td>01</td>
<td>—</td>
<td>—</td>
<td>Reserved</td>
<td>Normal mode</td>
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<tr>
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<td>11</td>
<td>Normal mode</td>
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<td>Reserved</td>
<td>Normal mode</td>
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<tr>
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<td>Normal mode</td>
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### Resonator/Input Clock

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<th>MD14</th>
<th>MD13</th>
<th>Resonator/Input Clock</th>
<th>Internal Divider</th>
<th>PLL1</th>
<th>PLL0</th>
<th>PLL3/MD19: DDR3-1333</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>15 MHz</td>
<td>× 1/1</td>
<td>× 208*</td>
<td>× 200</td>
<td>× 88</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>20 MHz</td>
<td>× 1/1</td>
<td>× 156*</td>
<td>× 150</td>
<td>× 66</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>26 MHz</td>
<td>× 1/2</td>
<td>× 240*</td>
<td>× 230</td>
<td>× 102</td>
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<tr>
<td>1</td>
<td>1</td>
<td>30 MHz</td>
<td>× 1/2</td>
<td>× 208*</td>
<td>× 200</td>
<td>× 88</td>
</tr>
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</table>

**Note:** * VCO = 3120 MHz

### External Bus Clock

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<td>0</td>
<td>65 MHz (Fix to 0)</td>
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### DDR3-SDRAM Bus Clock

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<td>DDR3-1333 mode (Fix to 1)</td>
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</table>
4. Pin Multiplexing

4.1 List of Multiplexed Pin Functions

Table 4.1 lists the multiplexed pin functions of the RZ/G1E.

The default pin function of each pin after power-on reset is "Function 1" respectively, unless otherwise mentioned.

For details on pin function control, refer to section 3.3, Mode Pin Settings and section 5, Pin Function Controller (PFC).

[Legend]

- Leftmost column of table
  No.: Serial number
  Pin No.: BGA package ball grid number
  Mode Pin (only for corresponding pin): Mode pin is assigned

- Middle column of table
  Function n (n=1, 2, 3, ...)/GPIO: Module or GPIO
  Module: Module abbreviation except for GPIO
  Pin Name: Module or GPIO pin name
  I/O: Input or output,
    i.e., I: Input, I(S): Schmitt input, IO: Input and output, IO (OD): Input and open drain output, O: Output, P: Power supply pin. (I)/(H)/(L)/(X)/(Z) with I, O or IO: Default pin state (only for default pin, except for clock or analog output), H: High level output, L: Low level output, X: Undefined value output, Z: High impedance

"Reserved" in module column is assigned optional function and ".-" in module column is internal function or undefined, they must not be specified. This indication is different from that of in section 5, Pin Function Controller (PFC).

- Rightmost column of table
  During POR: Pin state during power-on reset (PRESET# pin input is low-level)
  V(power)/|IOH|: Pin voltage (power domain) and output drive current (nominal value respectively)
  Pull-up: Internal pull-up control function is available or not from a power-on reset
    "On": Pull-up control function is available and default state is pulled-up.
    (No.110, ACK pin is available for internal pull-down function.)
    "Off": Pull-up control function is available and default state is not pulled-up.
    ".-": Pull-up control function is not available.
  For details of pull-up control function, refer to PUPR0 through PUPR6 registers in section 5, Pin Function Controller (PFC).

Notes: 1. Pin name that has an identifier for example "XXXX_B", "XXXX_C" etc. are mirror pins of the XXXX pin.
    Only one pin out of the XXXX pin or its mirror pins can be used. When using mirror pin, specify the suite of pin that has the same identifier for the selected module. It is prohibited to use a suite of pin as mixed two or more identifiers for a selected module.

2. Do not use any pins that of unused modules.

3. Unused pins must be handled as described in section 4.3, Handling of Unused Pins.

4. The terminal state after the reset cancellation has been described as a premise not using the BKPRST (BKRST#=H(fixed)).
### Table 4.1 List of Multiplexed Pin Functions

#### DBSC3 (No.1 to 40): Single Function

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Module</th>
<th>During POR</th>
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<td>Pin No.</td>
<td>Pin Name</td>
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<td>Pull-up</td>
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<td>3</td>
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<td>M0RESE#</td>
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1/3 (DBSC3)
### Function 1

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</table>

Note: No. 47, 48, 61, 62, 74 and 75 (M0DQSx and M0DQsx#) pin states during POR and default state: The drivers output states are both high-impedance (Z), and the internal circuit controls pin levels as low-level for the MnDQSx pin and high-level for the MnDQsx# pin respectively.
## DBSC3 (No.81 to 93): Single Function

### Function 1

<table>
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<tr>
<th>No.</th>
<th>Module</th>
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<th>Pin No.</th>
<th>Pin Name</th>
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<th>IOH</th>
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<td></td>
<td>P</td>
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</tr>
</tbody>
</table>

### 3/3 (DBSC3)

**Note:** No.88 and 89 (M0DQS3 and M0DQS3#) pin states during POR and default state: The drivers output states are both high-impedance (Z), and the internal circuit controls pin levels as low-level for the M0DQS3 pin and high-level for the M0DQS3# pin respectively.
### Pin Multiplexing

#### CPG, RESET, SYSTEM, Debug, USB (No.94 to 116): Single Function

<table>
<thead>
<tr>
<th>No.</th>
<th>Module</th>
<th>Pin Name</th>
<th>During POR</th>
</tr>
</thead>
<tbody>
<tr>
<td>94</td>
<td>CPG</td>
<td>V25 EXTAL</td>
<td>1.8V(VCCQ18)/-</td>
</tr>
<tr>
<td>95</td>
<td>CPG</td>
<td>V24 XTAL</td>
<td>1.8V(VCCQ18)/-</td>
</tr>
<tr>
<td>96</td>
<td>PLL</td>
<td>E8 VDD_CPGPLL0</td>
<td>1.8V(VDD_CPGPLL0)/-</td>
</tr>
<tr>
<td>97</td>
<td>PLL</td>
<td>E9 VSS_CPGPLL0</td>
<td>GND(VDD_CPGPLL0)/-</td>
</tr>
<tr>
<td>98</td>
<td>PLL</td>
<td>K15/L15 VDD_CPGPLL1</td>
<td>1.8V(VDD_CPGPLL1)/-</td>
</tr>
<tr>
<td>99</td>
<td>PLL</td>
<td>K16/L16 VSS_CPGPLL1</td>
<td>GND(VDD_CPGPLL1)/-</td>
</tr>
<tr>
<td>100</td>
<td>PLL</td>
<td>K12/L12 VDD_CPGPLL3</td>
<td>1.8V(VDD_CPGPLL3)/-</td>
</tr>
<tr>
<td>101</td>
<td>PLL</td>
<td>K11/L11 VSS_CPGPLL3</td>
<td>GND(VDD_CPGPLL3)/-</td>
</tr>
<tr>
<td>102</td>
<td>RESET</td>
<td>V23 PRESET#</td>
<td>1.8V(VCCQ18)/-</td>
</tr>
<tr>
<td>103</td>
<td>RESET</td>
<td>B6 PRESETOUT#</td>
<td>3.3V(VCCQ18)/4mA</td>
</tr>
<tr>
<td>104</td>
<td>SYSTEM</td>
<td>R21 BSMODE</td>
<td>1.8V(VCCQ18)/-</td>
</tr>
<tr>
<td>105</td>
<td>Debug</td>
<td>N21 TRST#</td>
<td>1.8V(VCCQ18)/-</td>
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</table>

<table>
<thead>
<tr>
<th>No.</th>
<th>Module</th>
<th>Pin Name</th>
<th>During POR</th>
</tr>
</thead>
<tbody>
<tr>
<td>106</td>
<td>Debug</td>
<td>N22 TCK</td>
<td>1.8V(VCCQ18)/-</td>
</tr>
<tr>
<td>107</td>
<td>Debug</td>
<td>P21 TMS</td>
<td>1.8V(VCCQ18)/-</td>
</tr>
<tr>
<td>108</td>
<td>Debug</td>
<td>R22 TDI</td>
<td>1.8V(VCCQ18)/-</td>
</tr>
<tr>
<td>109</td>
<td>Debug</td>
<td>P22 TDO</td>
<td>1.8V(VCCQ18)/4mA</td>
</tr>
<tr>
<td>110</td>
<td>Debug</td>
<td>U23 ACK</td>
<td>1.8V(VCCQ18)/4mA</td>
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<tr>
<td>111</td>
<td>USB</td>
<td>T25 USB_EXTAL</td>
<td>1.8V(VCCQ18)/-</td>
</tr>
<tr>
<td>112</td>
<td>USB</td>
<td>T24 USB_XTAL</td>
<td>1.8V(VCCQ18)/-</td>
</tr>
<tr>
<td>113</td>
<td>USB</td>
<td>P20 VD331</td>
<td>3.3V(VD331)/-</td>
</tr>
<tr>
<td>114</td>
<td>USB</td>
<td>R20 VD181</td>
<td>1.8V(VD181)/-</td>
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<tr>
<td>115</td>
<td>USB</td>
<td>P23 AVDD</td>
<td>1.8V(AVDD)/-</td>
</tr>
<tr>
<td>116</td>
<td>USB</td>
<td>M20 AVSS</td>
<td>GND(AVDD)/-</td>
</tr>
</tbody>
</table>

- **I**: Input
- **O**: Output
- **P**: Pull-up
- **Z**: Open
- **S**: Select
- **L**: Low
- **H**: High
- **On**: High
- **Off**: Low
- **pull-down**: Pull-down
USB 2.0, INTC, SDHI and GPIO (No.117 to 136): Up to 2-Function Multiplexed

Following pins multiplexed with the GPIO are set for GPIO function after power-on reset except for USB pins. For details, refer to GSPR5 and GSPR6 registers in section 5, Pin Function Controller (PFC).

<table>
<thead>
<tr>
<th>No.</th>
<th>Module</th>
<th>Pin Name</th>
<th>During POR</th>
<th>Function 1 GPIO</th>
<th>V(power)/</th>
<th>IOH</th>
<th>Pull-up</th>
<th>I/O</th>
<th>I/O (pull-up)</th>
</tr>
</thead>
<tbody>
<tr>
<td>117</td>
<td>USB 2.0 ch0</td>
<td>P24</td>
<td>-</td>
<td>I</td>
<td>3.3V(VDD331)/-</td>
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<td>I</td>
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<tr>
<td>118</td>
<td>USB 2.0 ch0</td>
<td>P25</td>
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<td>I</td>
<td>3.3V(VDD331)/-</td>
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<td>119</td>
<td>USB 2.0 ch0</td>
<td>M25</td>
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<td>I</td>
<td>3.3V(VCCQ)/-</td>
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<tr>
<td>120</td>
<td>USB 2.0 ch0</td>
<td>U21</td>
<td>GP5_24</td>
<td>3.3V(VCCQ)/4mA</td>
<td>On</td>
<td></td>
<td>I</td>
<td></td>
<td></td>
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<tr>
<td>121</td>
<td>USB 2.0 ch0</td>
<td>U22</td>
<td>GP5_25</td>
<td>3.3V(VCCQ)/4mA</td>
<td>On</td>
<td></td>
<td>I</td>
<td></td>
<td></td>
</tr>
<tr>
<td>122</td>
<td>USB 2.0 ch1</td>
<td>N24</td>
<td>-</td>
<td>I</td>
<td>3.3V(VCCQ)/-</td>
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<td>I</td>
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<tr>
<td>123</td>
<td>USB 2.0 ch1</td>
<td>N25</td>
<td>-</td>
<td>I</td>
<td>3.3V(VCCQ)/-</td>
<td></td>
<td>I</td>
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<td>124</td>
<td>USB 2.0 ch1</td>
<td>M24</td>
<td>-</td>
<td>I</td>
<td>3.3V(VCCQ)/-</td>
<td></td>
<td>I</td>
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<td></td>
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<tr>
<td>125</td>
<td>USB 2.0 ch1</td>
<td>T21</td>
<td>GP5_26</td>
<td>3.3V(VCCQ)/4mA</td>
<td>On</td>
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<td>I</td>
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<tr>
<td>126</td>
<td>USB 2.0 ch1</td>
<td>T22</td>
<td>GP5_27</td>
<td>3.3V(VCCQ)/4mA</td>
<td>On</td>
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<td>I</td>
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<td></td>
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<tr>
<td>127</td>
<td>INTC</td>
<td>R23</td>
<td>-</td>
<td>I(S)</td>
<td>1.8V(VCCQ18)/-</td>
<td></td>
<td>I</td>
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<td></td>
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<tr>
<td>128</td>
<td>SDHI0</td>
<td>AE12</td>
<td>GP6_0</td>
<td>1.8/3.3V(VCCQ_SD0)/16mA</td>
<td>0</td>
<td></td>
<td>I</td>
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<tr>
<td>129</td>
<td>SDHI0</td>
<td>AD12</td>
<td>GP6_1</td>
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<tr>
<td>130</td>
<td>SDHI0</td>
<td>AC11</td>
<td>GP6_2</td>
<td>1.8/3.3V(VCCQ_SD0)/16mA</td>
<td>Off</td>
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<td>131</td>
<td>SDHI0</td>
<td>AD11</td>
<td>GP6_3</td>
<td>1.8/3.3V(VCCQ_SD0)/16mA</td>
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<td>132</td>
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<td>AE11</td>
<td>GP6_4</td>
<td>1.8/3.3V(VCCQ_SD0)/16mA</td>
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<td>133</td>
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<td>AA12</td>
<td>GP6_5</td>
<td>1.8/3.3V(VCCQ_SD0)/16mA</td>
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<td>I</td>
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<tr>
<td>134</td>
<td>SDHI0 Power</td>
<td>AB12</td>
<td>GP6_6</td>
<td>1.8/3.3V(VCCQ_SD0)/16mA</td>
<td>Off</td>
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<tr>
<td>135</td>
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<td>AA13</td>
<td>GP6_7</td>
<td>1.8/3.3V(VCCQ_SD0)/16mA</td>
<td>Off</td>
<td></td>
<td>I</td>
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</table>

Note: (No.128 to 135): Pin voltage is selectable (3.3 V: default). For details, refer to IOCTRL3 register in section 5, Pin Function Controller (PFC).
SDHI, INTC, RCAN, MMC, SCIF, I2C and GPIO (No.137 to 156): Up to 5-Function Multiplexed

Pin states during POR and default pin function (GPIO or DBG: debugging mode) after power-on reset depend on mode pins setting except for No.145 and 156. For details, refer to Mode Pin Settings in section 3.3, GPSR6 register in section 5, Pin Function Controller (PFC) and section 62, CoreSight for DBG.

### Function Pin Multiplexing

<table>
<thead>
<tr>
<th>No.</th>
<th>Module</th>
<th>Pin Name</th>
<th>V(power)/[IOH]</th>
<th>During POR</th>
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<tbody>
<tr>
<td>137</td>
<td>SDHI1</td>
<td>SD1_CLK</td>
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<td>GP6_8</td>
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<td>I(GPIO)/Z(DBG)</td>
<td>1.8/3.3V(VCCQ_SD1)/16mA</td>
</tr>
<tr>
<td>138</td>
<td>SDHI1</td>
<td>SD1_CMD</td>
<td>-</td>
<td>GP6_9</td>
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<td>I(GPIO)/I(DBG)</td>
<td>1.8/3.3V(VCCQ_SD1)/16mA</td>
</tr>
<tr>
<td>139</td>
<td>SDHI1</td>
<td>SD1_DATA0</td>
<td>-</td>
<td>GP6_10</td>
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<td>I(GPIO)/I(DBG)</td>
<td>1.8/3.3V(VCCQ_SD1)/16mA</td>
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<td>SDHI1</td>
<td>SD1_DATA1</td>
<td>-</td>
<td>GP6_11</td>
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<td>I(GPIO)/I(DBG)</td>
<td>1.8/3.3V(VCCQ_SD1)/16mA</td>
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<td>SDHI1</td>
<td>SD1_DATA2</td>
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<td>GP6_12</td>
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</tr>
<tr>
<td>142</td>
<td>SDHI1</td>
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<td>GP6_13</td>
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<td>1.8/3.3V(VCCQ_SD1)/16mA</td>
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<tr>
<td>144</td>
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<td>SD1_CD</td>
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<td>GP6_15</td>
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<td>I(GPIO)/I(DBG)</td>
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<tr>
<td>145</td>
<td>SDHI1</td>
<td>I2C2_SCL_B</td>
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<td>GP6_16</td>
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<td>GP6_17</td>
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<td>1.8/3.3V(VCCQ_MMC_SD2)/16mA</td>
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<tr>
<td>147</td>
<td>SDHI1</td>
<td>SD2_CMD</td>
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<td>GP6_18</td>
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<tr>
<td></td>
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<td>I(GPIO)/I(DBG)</td>
<td>1.8/3.3V(VCCQ_MMC_SD2)/16mA</td>
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<td>148</td>
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<td>GP6_19</td>
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<tr>
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<td>1.8/3.3V(VCCQ_MMC_SD2)/16mA</td>
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<td>149</td>
<td>SDHI1</td>
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<td>GP6_20</td>
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<td>SD2_DATA2</td>
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<td>GP6_21</td>
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<td>1.8/3.3V(VCCQ_MMC_SD2)/16mA</td>
</tr>
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<td>SD2_DATA3</td>
<td>-</td>
<td>GP6_22</td>
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<td>I(GPIO)/I(DBG)</td>
<td>1.8/3.3V(VCCQ_MMC_SD2)/16mA</td>
</tr>
<tr>
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<td>SDHI1</td>
<td>SD2_DATA4</td>
<td>-</td>
<td>GP6_23</td>
</tr>
<tr>
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<td>I(GPIO)/I(DBG)</td>
<td>1.8/3.3V(VCCQ_MMC_SD2)/16mA</td>
</tr>
<tr>
<td>153</td>
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<td>SD2_WP</td>
<td>-</td>
<td>GP6_24</td>
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<tr>
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<td>I(GPIO)/I(DBG)</td>
<td>1.8/3.3V(VCCQ_MMC_SD2)/16mA</td>
</tr>
<tr>
<td>154</td>
<td>SDHI1</td>
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<td>GP6_25</td>
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<td>I(GPIO)</td>
<td>3.3V(VCCQ)/16mA</td>
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<td>155</td>
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<td>SCIF0</td>
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<td>I(GPIO)/I(DBG)</td>
<td>3.3V(VCCQ)/16mA</td>
</tr>
<tr>
<td>156</td>
<td>SDHI1</td>
<td>SCIF0</td>
<td>-</td>
<td>GP6_27</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>I(GPIO)/I(DBG)</td>
<td>3.3V(VCCQ)/16mA</td>
</tr>
</tbody>
</table>

Note: (No.137 to 144 and 146 to 155): Pin voltage selectable (3.3 V: default) for each SDHI channel and multiplexed GPIO pins suite. For details, refer to IOCTRL3 register in section 5, Pin Function Controller (PFC).
### Pin Multiplexing

**LBSC, SCIFA, INTC, I2C, SCIF, TMU, PWM, HSCIF, SCIFB and GPIO (No.157 to 176): Up to 6-Function Multiplexed and Mode Pin assigned (No.173 to 176)**

Default pin function (function 1 or GPIO) after power-on reset is defined by MD[3:1] pins setting.

When MD[3:1]=000, the LBSC will execute area 0 booting.

#### Function Table

<table>
<thead>
<tr>
<th>Function</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>GPIO</th>
</tr>
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<tbody>
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<tr>
<td>Pin No.</td>
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</tr>
<tr>
<td>Mode Pin</td>
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<tr>
<td>157</td>
<td>LBSC</td>
<td>SCIFA3</td>
<td>INTC</td>
<td>-</td>
<td>-</td>
<td>I(GPIO)</td>
</tr>
<tr>
<td>D6</td>
<td>D0</td>
<td>SCIFA3_SCK_B</td>
<td>IRQ4</td>
<td>-</td>
<td>-</td>
<td>GP0_0</td>
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<td>I0(I)</td>
<td>O</td>
<td>-</td>
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<td>IO(I)</td>
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<td>158</td>
<td>LBSC</td>
<td>SCIFA3</td>
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<td>I(GPIO)</td>
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<td>GP0_1</td>
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<td>IO(I)</td>
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**Function Multiplexing**

Default pin function (function 1 or GPIO) after power-on reset is defined by MD[3:1] pins setting. When MD[3:1]=000, the LBSC will execute area 0 booting; MD[3:1]#000, the QSPI will execute QSPI booting.

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- **No.**
- **Pin No.**
- **Mode Pin**
- **Pull-up**
- **V(power)/IOH**
- **During POR**

**LBSC, SCIFB, PWM, TPU, SCIFA, MSIOF, IIC, HSCIF, RCAN, QSPI and GPIO (No.177 to 196): Up to 8-Function Multiplexed and Mode Pin assigned (No.177, 180, 182, 186, 188, 191 and 192)**
LBSC, QSPI, VIN, TPU, SCIFB, PWM, SCIF, SCIFA, I2C, RCAN and GPIO (No.197 to 215): Up to 9-Function Multiplexed and Mode Pin assigned (No.208 to 212 and 215)

Default pin function (function 1 or GPIO) after power-on reset is defined by MD[3:1] pins setting except for No.199, 202 to 207, 210, 214 and 215.

When MD[3:1]=000, the LSBC will execute area 0 booting; MD[3:1]=000, the QSPI will execute QSPI booting.

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Note: (No.201): Output value of CS1#/A26 pin after power-on reset is 'H' when MD4 = 0 (area 0: 64-MByte), 'L' when MD4 = 1 (area 0: 128-Mbyte).
### 4. Pin Multiplexing

DU, SCIF, I2C, SCIFA, RCAN and GPIO (No.216 to 235): Up to 6-Function Multiplexed

These pins are set for GPIO after power-on reset. For details, refer to GPSR2 register in section 5, Pin Function Controller (PFC).

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**Note:** During POR (Power-On Reset), these pins are set for their respective functions according to the pin multiplexing settings. Pull-up resistors are also indicated for certain pins.
DU, VIN, EtherAVB and GPIO (No.236 to 256): Up to 3-Function Multiplexed and Mode Pin assigned (No.243, 244, 246 and 247)

These pins are set for GPIO after power-on reset. For details, refer to GPSR2 and GPSR3 registers in section 5, Pin Function Controller (PFC).

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R01UH0544EJ0100 Rev.1.00
Sep 30, 2016

Renesas
### Pin Multiplexing

These pins are set for GPIO after power-on reset. For details, refer to GPSR3 register in section 5, Pin Function Controller (PFC).

| Function | 1 | 2 | 3 | 4 | 5 | 6 | 7 | GPIO | During POR | Pin No. | V(power)|I[OH]|Pull-up |
|----------|---|---|---|---|---|---|---|------|---------|---------|---------|--------|
| 257 VIN0 | I2C3 | SCIF-A5 | Reserved | EthernetAVB | - | - | GP3.9 | 3.3V(VCCQ)/4mA | I(GPIO) |
| 258 VIN0 | I2C2 | SCIF-A5 | - | AVB_RXD7 | - | - | GP3.9 | 3.3V(VCCQ)/4mA | I(IO) |
| 259 VIN0 | I2C0 | SCIF0 | - | AVB_TXD2 | - | - | GP3.9 | 3.3V(VCCQ)/4mA | I(IO) |
| 260 VIN0 | I2C0 | SCIF0 | - | GP3.25 | - | - | GP3.9 | 3.3V(VCCQ)/4mA | I(IO) |
| 261 EtherMAC | VIN0 | MSIOF2 | I2C5 | EthernetAVB | Reserved | I(GPIO) |
| 262 EtherMAC | VIN0 | MSIOF2 | I2C5 | EthernetAVB | Reserved | I(GPIO) |
| 263 EtherMAC | VIN0 | MSIOF2 | I2C5 | EthernetAVB | Reserved | I(GPIO) |
| 264 EtherMAC | VIN0 | MSIOF2 | I2C5 | EthernetAVB | Reserved | I(GPIO) |
| 265 EtherMAC | VIN0 | SCIF4 | - | EthernetAVB | Reserved | I(GPIO) |
| 266 EtherMAC | VIN0 | SCIF4 | - | EthernetAVB | Reserved | I(GPIO) |
| 267 EtherMAC | VIN0 | SCIF4 | - | EthernetAVB | Reserved | I(GPIO) |
| 268 EtherMAC | VIN0 | SCIF4 | - | EthernetAVB | Reserved | I(GPIO) |
| 269 EtherMAC | VIN0 | SCIF4 | - | EthernetAVB | Reserved | I(GPIO) |
| 270 EtherMAC | VIN0 | SCIF4 | - | EthernetAVB | Reserved | I(GPIO) |
| 271 EtherMAC | VIN0 | SCIF4 | - | EthernetAVB | Reserved | I(GPIO) |
| 272 EtherMAC | VIN0 | SCIF4 | - | EthernetAVB | Reserved | I(GPIO) |
| 273 EtherMAC | VIN0 | SCIF4 | - | EthernetAVB | Reserved | I(GPIO) |
| 274 EtherMAC | VIN0 | SCIF4 | - | EthernetAVB | Reserved | I(GPIO) |
| 275 EtherMAC | VIN0 | SCIF4 | - | EthernetAVB | Reserved | I(GPIO) |
| 276 EtherMAC | VIN0 | SCIF4 | - | EthernetAVB | Reserved | I(GPIO) |
| 277 EtherMAC | VIN0 | SCIF4 | - | EthernetAVB | Reserved | I(GPIO) |
| 278 EtherMAC | VIN0 | SCIF4 | - | EthernetAVB | Reserved | I(GPIO) |
| 279 EtherMAC | VIN0 | SCIF4 | - | EthernetAVB | Reserved | I(GPIO) |
| 280 EtherMAC | VIN0 | SCIF4 | - | EthernetAVB | Reserved | I(GPIO) |
### I2C, SCIF, PWM, TMU, EthernetAVB, RCAN, TPU, SCU, DU, INTC, MSIOF, SCIFA, HSCIF, SSI, IIC and GPIO (No.278 to 298): Up to 9-Function Multiplexed

These pins are set for GPIO after power-on reset. For details, refer to GPSR3 and GPSR4 registers in section 5, Pin Function Controller (PFC).

#### Function 1 2 3 4 5 6 7 8 GPIO

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<tr>
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<td>SCIF0_TXD_C TPUTO0 CAN1_CLK DVC_MUTE CAN1_TX_D GP3.313.3V(VCCQ)/8mA</td>
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#### GPIO (No.278 to 298): Up to 9-Function Multiplexed

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### Pin Multiplexing

These pins are set for GPIO after power-on reset. For details, refer to GPSR4 and GPSR5 registers in section 5, Pin Function Controller (PFC).

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<tr>
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<td>DU1</td>
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<tr>
<td>SCIF5_CE1</td>
<td>-</td>
<td>DU1</td>
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<tr>
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<td>-</td>
<td>DU1</td>
<td>-</td>
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<tr>
<td>SCIF5_CE1</td>
<td>-</td>
<td>DU1</td>
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</tr>
<tr>
<td>SCIF5_CE1</td>
<td>-</td>
<td>DU1</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
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<td></td>
</tr>
</tbody>
</table>
| SCIF5_CE1 | - | DU1 | - | - | - | - | - |Downloaded from Arrow.com.
### Pin Multiplexing

#### Up to 9-Function Multiplexed

These pins are set for GPIO after power-on reset except for No.322 to 324. For details, refer to GPSR5 register in section 5, Pin Function Controller (PFC).

<table>
<thead>
<tr>
<th>Function No.</th>
<th>Pin No.</th>
<th>Pin Function Controller (PFC)</th>
<th>During POR</th>
<th>V(power)[IOH]</th>
<th>Pull-up</th>
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<td>SSI</td>
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<td>-</td>
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</tr>
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<td>326</td>
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<tr>
<td>327</td>
<td>SSI</td>
<td>SCIF1 IIC0(I2C6) VIN1 CAN00 Reserved EtherMAC -</td>
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<tr>
<td>AB5</td>
<td>SSI_WS1</td>
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<td>-</td>
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<tr>
<td>328</td>
<td>SSI</td>
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<td>SSI_DATA9</td>
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ADG, I2C, SCIFA, VIN, EtherMAC, IIC and GPIO (No.335 to 340): Up to 9-Function Multiplexed
These pins are set for GPIO after power-on reset except for No.339 and 340. For details, refer to GPSR5 register in section 5, Pin Function Controller (PFC).

<table>
<thead>
<tr>
<th>No.</th>
<th>ADG</th>
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<th>SCIFA4</th>
<th>VIN1</th>
<th>Reserved</th>
<th>Reserved</th>
<th>EtherMAC</th>
<th>During POR</th>
<th>GPIO</th>
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</thead>
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<tr>
<td>335</td>
<td>ADG</td>
<td>I2C0</td>
<td>SCIFA4</td>
<td>VIN1</td>
<td>Reserved</td>
<td>Reserved</td>
<td>EtherMAC</td>
<td>Pull-up</td>
<td>(GPIO)</td>
</tr>
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<td>I2C0_SCL_B</td>
<td>SCIFA4_RXD_D</td>
<td>V11_CLKENB</td>
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<td>Reserved</td>
<td>ETH_TXD0_B</td>
<td>GP5_20</td>
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<tr>
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<td>O</td>
<td>I</td>
<td>I</td>
<td>O</td>
<td>I(OI)</td>
<td>On</td>
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<td>I2C0</td>
<td>SCIFA4</td>
<td>VIN1</td>
<td>Reserved</td>
<td>Reserved</td>
<td>EtherMAC</td>
<td>(GPIO)</td>
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<td>SCIFA4_TXD_D</td>
<td>V11_FIELD</td>
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<td>-</td>
<td>ETH_MDC_B</td>
<td>GP5_21</td>
<td>3.3V(VCCQ)8mA</td>
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<td>I</td>
<td>-</td>
<td>-</td>
<td>O</td>
<td>IO(OI)</td>
<td>On</td>
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<td>I2C4</td>
<td>SCIFA5</td>
<td>VIN1</td>
<td>Reserved</td>
<td>Reserved</td>
<td>EtherMAC</td>
<td>(GPIO)</td>
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<td>I2C4_SCL_B</td>
<td>SCIFA5_RXD_D</td>
<td>V11_HSYNC#</td>
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<td>ETH_MDC_B</td>
<td>GP5_22</td>
<td>3.3V(VCCQ)8mA</td>
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<td>I</td>
<td>-</td>
<td>-</td>
<td>I(OI)</td>
<td>On</td>
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<td>338</td>
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<td>SCIFA5</td>
<td>VIN1</td>
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<td>Reserved</td>
<td>(GPIO)</td>
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<td>V11_VSYNC#</td>
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<td>-</td>
<td>Reserved</td>
<td>GP5_23</td>
<td>3.3V(VCCQ)8mA</td>
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<td>I</td>
<td>O</td>
<td>I</td>
<td>-</td>
<td>-</td>
<td>IO(OI)</td>
<td>On</td>
</tr>
<tr>
<td>339</td>
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<td>-</td>
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<td>-</td>
<td>-</td>
<td>-</td>
<td>Z</td>
</tr>
<tr>
<td>W21</td>
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<td>-</td>
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<td>1.8V(VCCQ18)*2</td>
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<tr>
<td></td>
<td>IO(OD, Z)</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
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<tr>
<td>340</td>
<td>IIC1</td>
<td>-</td>
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<td>-</td>
<td>-</td>
<td>-</td>
<td>Z</td>
</tr>
<tr>
<td>V22</td>
<td>IIC1_SDA</td>
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<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>1.8V(VCCQ18)*2</td>
</tr>
<tr>
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<td>IO(OD, Z)</td>
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<td>-</td>
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</tbody>
</table>

Note: No.339 and 340 (IIC1_SCL and IIC1_SDA) pin voltage: Input/output 3.3V tolerant pins
When using these pins as 3.3 V tolerant, all the external pull-up power supply for these pins must be kept the same power on/off sequence as the VCCQ of this LSI.

- End of Table 4.1 -
4.2 Pin States

Table 4.2 is pin state of the RZ/G1E.

[Legend]

No.: Serial number, Pin No.: BGA package ball grid number, Pin Name: Pin name of function 1 in pin in Table 4.1, I/O: Input or output direction of the pin name column pin (function 1).
I: Input, IO: Input and output, O: Output, -: N/A.
During POR: Pin state during power-on reset (PRESET# pin input is low-level).
Default Pin Function: Pin function after power-on reset
Default State: Pin state of default pin function
(I)/(H)/(L)/(X)/(Z) with I, O or IO: Default pin state
H: High level output, L: Low level output, X: Undefined value output, Z: High impedance
Default pull-up: Internal pull-up control function is available or not from a power-on reset and its pull-up state.
"On": Pull-up control function is available and default state is pulled-up.
(No.110, ACK pin is available internal pull-down function.)
"Off": Pull-up control function is available and default state is not pulled-up.
"-": Pull-up control function is not available.
For details of pull-up control function, refer to PUPR0 through PUPR12 registers in section 5, Pin Function Controller (PFC).

Notes: 1. All power supply pins and ground pins include VCCQ, VCCQ18, VDD, VDDQ_M0, VDDQ_M0BKUP, and VSS pins which are not listed in Table 4.2 must be used.
2. All mode pins must be used during power-on reset. For details of mode pin settings, refer to section 3.3, Mode Pin Settings.
3. Boot module related pins (LBSC area 0 or QSPI) should be used during boot operation. For details of QSPI boot, refer to section 18, Booting.
4. For multiplexed pins and modules of each pin, refer to Table 4.1.
### Table 4.2 Pin States

<table>
<thead>
<tr>
<th>No.</th>
<th>Pin No.</th>
<th>Pin Name (Function 1)</th>
<th>I/O</th>
<th>During POR</th>
<th>Default Pin Function</th>
<th>Default State</th>
<th>Default Pull-up</th>
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<tbody>
<tr>
<td>1</td>
<td>D15</td>
<td>M0CKE0</td>
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<td>X</td>
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<td>-</td>
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<tr>
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<td>X</td>
<td>M0CKE1</td>
<td>O(L)</td>
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</table>

Notes:
1. No. 47, 48, 61, 62, 74, 75, 88 and 89 (M0DQSx and M0DQSx#) pin states during POR and default state:
The drivers output states are both high-impedance (Z), and the internal circuit controls pin levels as low-level for the M0DQSx and high-level for the M0DQSx# pin respectively.
2. No. 137 to 142 and 146 to 151 Default pin function and pin state:
    Depends on MD[21:20], MD[12:10], and MDT[1:0] settings.
    "I" is in function mode (GPIO); "Z" is in debug mode.
3. No. 138 to 142 and 147 to 151 Default pull-up:
    "-" is in debugging operation only; "Off" is in other than debugging operation.
4. No.157 to 198, 200, 201, 208, 209, and 211 to 213 Default pin function:
   MD[3:1] = 000: LBSC (D[15:0], A[25:0], CS0#, CS1#/A26, BS#, RD#, WE[1:0]#, and EX_WAIT0)
   MD[3:1] ≠ 000: GPIO (GP0_[31:0], GP1_[23:21])

5. No.201 CS1#/A26 Default state:
   MD4 = 0: (area 0 64-Mbyte mode): high output
   MD4 = 1: (area 0 128-Mbyte mode): low output
4.3 Handling of Unused Pins

Table 4.3 shows a handling of unused pins of the RZ/G1E.

"Unused pin" means all modules that are multiplexed to the pin should be disable and unused in this section. For handling of some unused pin which belongs to the enable module should be handled following the notification of the module manual. Unless otherwise specified in the module manual, follow the Table 4.3 for handling of unused pins.

[Legend]

No.: Serial number, Pin No.: BGA package ball grid number, Pin Name: Pin name of function 1 in pin multiplex table, Default State: Pin state of default pin function (function 1, GPIO or DBG).
Mode Pin: Mode pin assigned.
Boot: These pins will be used in boot operation (LBSC area 0 or QSPI).
Default pull-up: Internal pull-up control function is available or not from a power-on reset and its pull-up state.
"On": Pull-up control function is available and default state is pulled-up.
(No.110, ACK pin is available internal pull-down function.)
"Off": Pull-up control function is available and default state is not pulled-up.
"-": Pull-up control function is not available.
For details of pull-up control function, refer to PUPR0 through PUPR12 registers in section 5, Pin Function Controller (PFC).

Notes: 1. All power supply pins and ground pins including VCCQ, VCCQ18, VDD, VDDQ_M0, VDDQ_M0BKUP and VSS pins which are not described in Table 4.3 must be used.
2. All mode pins (MD[21:18],[14:0] and MDT[1:0]) must be used during power-on reset. For details of mode pins setting, refer to section 3.3, Mode Pin Settings.
3. Boot related pins (LBSC or QSPI) should be used during boot operation. For details of QSPI boot, refer to section 18, Booting.
### Table 4.3 Handling of Unused Pins

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<tr>
<th>No.</th>
<th>Pin No.</th>
<th>Pin Name (Function 1)</th>
<th>Default State</th>
<th>Mode Pin</th>
<th>Boot</th>
<th>Default Pull-up</th>
<th>Pin Handling when not in Use</th>
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## Pin Multiplexing

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<th>Mode Pin</th>
<th>Default Boot</th>
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<th>Pin Handling when not in Use</th>
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<td>-</td>
<td>On</td>
<td>Open</td>
<td></td>
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<tr>
<td>293</td>
<td>AC25</td>
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<td>I - -</td>
<td>-</td>
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<td>Open</td>
<td></td>
</tr>
<tr>
<td>No.</td>
<td>Pin No.</td>
<td>Pin Name (Function 1)</td>
<td>Default State</td>
<td>Mode</td>
<td>Default Pin</td>
<td>Pull-up</td>
<td>Pin Handling when not in Use</td>
</tr>
<tr>
<td>-----</td>
<td>---------</td>
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<td>294</td>
<td>AD25</td>
<td>SCIF1_RXD</td>
<td>I</td>
<td>-</td>
<td>-</td>
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<td>Open</td>
</tr>
<tr>
<td>295</td>
<td>AC24</td>
<td>SCIF1_TXD</td>
<td>I</td>
<td>-</td>
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<td>Open</td>
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<tr>
<td>296</td>
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</tr>
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<td>297</td>
<td>AE23</td>
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<td>Open</td>
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<td>298</td>
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<td>-</td>
<td>-</td>
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<td>Open</td>
</tr>
<tr>
<td>299</td>
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<td>-</td>
<td>-</td>
<td>On</td>
<td>Open</td>
</tr>
<tr>
<td>300</td>
<td>AC22</td>
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<td>I</td>
<td>-</td>
<td>-</td>
<td>On</td>
<td>Open</td>
</tr>
<tr>
<td>301</td>
<td>AC21</td>
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<td>-</td>
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<tr>
<td>302</td>
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<td>-</td>
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<tr>
<td>303</td>
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<td>304</td>
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<td>I</td>
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</tr>
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<td>Open</td>
</tr>
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<td>306</td>
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</tr>
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<td>309</td>
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<td>314</td>
<td>AA7</td>
<td>SSI_WS0129</td>
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</tr>
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<td>315</td>
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<td>Open</td>
</tr>
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<td>Open</td>
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<td>-</td>
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<td>Open</td>
</tr>
<tr>
<td>318</td>
<td>AD5</td>
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<td>I</td>
<td>-</td>
<td>-</td>
<td>On</td>
<td>Open</td>
</tr>
<tr>
<td>319</td>
<td>AD22</td>
<td>SSI_SCK4</td>
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<tr>
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<td>I</td>
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<td>-</td>
<td>Pulled-up to VCCQ or pulled-down to VSS</td>
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<td>Pulled-up to VCCQ or pulled-down to VSS</td>
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<td>323</td>
<td>W20</td>
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<td>AC6</td>
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<td>I</td>
<td>-</td>
<td>-</td>
<td>On</td>
<td>Open</td>
</tr>
<tr>
<td>326</td>
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<td>-</td>
<td>-</td>
<td>On</td>
<td>Open</td>
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<td>327</td>
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<td>SSI_WS1</td>
<td>I</td>
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<td>-</td>
<td>On</td>
<td>Open</td>
</tr>
<tr>
<td>328</td>
<td>AC5</td>
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<td>I</td>
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<td>On</td>
<td>Open</td>
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<td>-</td>
<td>On</td>
<td>Open</td>
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<td>330</td>
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<td>SSI_WS2</td>
<td>I</td>
<td>-</td>
<td>-</td>
<td>On</td>
<td>Open</td>
</tr>
<tr>
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<td>AC4</td>
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<td>I</td>
<td>-</td>
<td>-</td>
<td>On</td>
<td>Open</td>
</tr>
<tr>
<td>332</td>
<td>AE3</td>
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<td>-</td>
<td>On</td>
<td>Open</td>
</tr>
<tr>
<td>333</td>
<td>AD3</td>
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<td>I</td>
<td>-</td>
<td>-</td>
<td>On</td>
<td>Open</td>
</tr>
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<td>334</td>
<td>AD2</td>
<td>SSI_SDATA9</td>
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<td>-</td>
<td>-</td>
<td>On</td>
<td>Open</td>
</tr>
<tr>
<td>335</td>
<td>AD1</td>
<td>AUDIO_CLKA</td>
<td>I</td>
<td>-</td>
<td>-</td>
<td>On</td>
<td>Open</td>
</tr>
<tr>
<td>336</td>
<td>AE2</td>
<td>AUDIO_CLKB</td>
<td>I</td>
<td>-</td>
<td>-</td>
<td>On</td>
<td>Open</td>
</tr>
<tr>
<td>337</td>
<td>AC1</td>
<td>AUDIO_CLKC</td>
<td>I</td>
<td>-</td>
<td>-</td>
<td>On</td>
<td>Open</td>
</tr>
<tr>
<td>338</td>
<td>AC2</td>
<td>AUDIOCLKOUT</td>
<td>I</td>
<td>-</td>
<td>-</td>
<td>On</td>
<td>Open</td>
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<tr>
<td>339</td>
<td>W21</td>
<td>IIC1_SCL</td>
<td>Z</td>
<td>-</td>
<td>-</td>
<td>Pulled-up to VCCQ18</td>
<td></td>
</tr>
<tr>
<td>340</td>
<td>V22</td>
<td>IIC1_SDA</td>
<td>Z</td>
<td>-</td>
<td>-</td>
<td>Pulled-up to VCCQ18</td>
<td></td>
</tr>
</tbody>
</table>
Notes: 1. No.47, 48, 61, 62, 74, 75, 88 and 89 (M0DQSx and M0DQSx#) pin states during POR and default state: The drivers output states are both high-impedance (Z), and the internal circuit controls pin levels as low-level for the M0DQSx pin and high-level for the M0DQSx# pin respectively.
2. No.137 to 142 and 146 to 151 Default pin function and pin state: Depends on MD[21:20], MD[12:10], and MDT[1:0] settings. "I" is in function mode (GPIO); "Z" is in debug mode.
3. No.138 to 142 and 147 to 151 Default pull-up: "-" is in debugging operation only; "Off" is in other than debugging operation.
4. No.201 CS1#/A26 Default state: MD4 = 0: (area 0 64-Mbyte mode): high output MD4 = 1: (area 0 128-Mbyte mode): low output
5. Pin Function Controller (PFC)

5.1 Overview

The pin function controller (PFC) is a module that consists of registers for selecting the function of the multiplexed pins and controlling the pull-up resistor on each LSI pin.

Notes: 1. Some functions are optional or internal.
2. Pin function name that has two or more functions is indicated by using "_" instead of "/".

5.1.1 Features

- Register access through the APB bus interface
- Setting multiplexed pin functions for LSI pins
  Function of the RZ/G1E pin selectable by setting the registers in the PFC module
  (The function of the LSI pin can be selected by the GPIO/peripheral function select registers 0 to 6 (GPSR0 to GPSR6) and peripheral function select registers 0 to 13 (IPSR0 to IPSR13) in the PFC module. For details, see sections 5.3.2, GPIO/Peripheral Function Select Register 0 (GPSR0) through 5.3.22, Peripheral Function Select Register 13 (IPSR13).)
- Module selection
  Enable and disable the functions of RZ/G1E LSI pins to which pin functions from multiple pin groups are assigned by setting the registers in the PFC module.
  (Selection is handled by the module select register (MOD_SEL), module select register 2 (MOD_SEL2), and module select register 3 (MOD_SEL3). For details, see sections 5.3.23, Module Select Register (MOD_SEL), through 5.3.25, Module Select Register 3 (MOD_SEL3).)
- Pull-up control for each LSI pin.
  On/off of the pull-up or pull-down resistors on each LSI pin can be controlled by setting the registers in the PFC module.
  (The pull-up, pull-down resistors on each LSI pin can be turned on or off individually by setting the LSI pin pull-up/down control registers 0 to 6 (PUPR0 to PUPR6) in the PFC module. For details, see sections 5.3.26, LSI Pin Pull-Up Control register 0 (PUPR0) through 5.3.32, LSI Pin Pull-Up Control Register 6 (PUPR6).)
- Control of IO functions, including MMC, IIC, LBSC, VI, SCIF, SRU, IRQ, DU, Ethernet and ADG.
  SDIO functions, including the driving ability, POC of pins, can be controlled by setting registers of the PFC module.
  For details, see sections 5.3.33 to section 5.3.37 (IOCTRL0 to IOCTRL3 and IOCTRL7).
## 5.2 Register Configuration

All the registers in the PFC are mapped into the APB bus space. Table 5.1 shows the configuration of the registers provided in the PFC. Details on each register in the PFC are given in sections 5.2.1 to 5.3.48.

<table>
<thead>
<tr>
<th>Name</th>
<th>Abbr.</th>
<th>R/W</th>
<th>Initial Value</th>
<th>Address</th>
<th>Access Size</th>
<th>Condition</th>
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</thead>
<tbody>
<tr>
<td>LSI Multiplexed Pin Setting Mask Register</td>
<td>PMMR</td>
<td>R/W</td>
<td>H'0000 0000</td>
<td>H'E606 0000</td>
<td>32</td>
<td>—</td>
</tr>
<tr>
<td>GPIO/peripheral function select register 0</td>
<td>GPSR0</td>
<td>R/W</td>
<td>H'FFFF FFFF (when md[3:1] = 000), H'0000 0000 (when md[3:1] ≠ 000)</td>
<td>H'E606 0004</td>
<td>32</td>
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</tr>
<tr>
<td>GPIO/peripheral function select register 1</td>
<td>GPSR1</td>
<td>R/W</td>
<td>H'00EC 0FFF (when md[3:1] = 000), H'0000 0000 (when md[3:1] ≠ 000)</td>
<td>H'E606 0008</td>
<td>32</td>
<td>—</td>
</tr>
<tr>
<td>GPIO/peripheral function select register 2</td>
<td>GPSR2</td>
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<td>H'0000 0000</td>
<td>H'E606 000C</td>
<td>32</td>
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<td>GPIO/peripheral function select register 3</td>
<td>GPSR3</td>
<td>R/W</td>
<td>H'0000 0000</td>
<td>H'E606 0010</td>
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<tr>
<td>GPIO/peripheral function select register 4</td>
<td>GPSR4</td>
<td>R/W</td>
<td>H'0000 0000</td>
<td>H'E606 0014</td>
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<td>GPIO/peripheral function select register 5</td>
<td>GPSR5</td>
<td>R/W</td>
<td>H'0F00 0000</td>
<td>H'E606 0018</td>
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<td>H'E606 001C</td>
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<td>Peripheral function select register 0</td>
<td>IPSR0</td>
<td>R/W</td>
<td>H'0000 0000</td>
<td>H'E606 0020</td>
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<td>IPSR1</td>
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<td>H'E606 0028</td>
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### Pin Function Controller (PFC)

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<th>Name</th>
<th>Abbr.</th>
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<th>Access Size</th>
<th>Condition</th>
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<tr>
<td>LSI pin pull-up control register 3</td>
<td>PUPR3</td>
<td>R/W</td>
<td>H'FFFF FFFF</td>
<td>H'E606 010C</td>
<td>32</td>
<td>—</td>
</tr>
<tr>
<td>LSI pin pull-up control register 4</td>
<td>PUPR4</td>
<td>R/W</td>
<td>H'FFFF FFFF</td>
<td>H'E606 0110</td>
<td>32</td>
<td>—</td>
</tr>
<tr>
<td>LSI pin pull-up control register 5</td>
<td>PUPR5</td>
<td>R/W</td>
<td>H'00FF FF1F</td>
<td>H'E606 0114</td>
<td>32</td>
<td>—</td>
</tr>
<tr>
<td>LSI pin pull-up control register 6</td>
<td>PUPR6</td>
<td>R/W</td>
<td>H'0000 0000</td>
<td>H'E606 0118</td>
<td>32</td>
<td>—</td>
</tr>
<tr>
<td>SD control register 0</td>
<td>IOCTRL0</td>
<td>R/W</td>
<td>H'FFFF FFFF</td>
<td>H'E606 0060</td>
<td>32</td>
<td>—</td>
</tr>
<tr>
<td>SD control register 1</td>
<td>IOCTRL1</td>
<td>R/W</td>
<td>H'FFFF F000</td>
<td>H'E606 0064</td>
<td>32</td>
<td>—</td>
</tr>
<tr>
<td>TDSEL control register</td>
<td>IOCTRL2</td>
<td>R/W</td>
<td>H'0000 0000</td>
<td>H'E606 0068</td>
<td>32</td>
<td>—</td>
</tr>
<tr>
<td>POC control register</td>
<td>IOCTRL3</td>
<td>R/W</td>
<td>H'FFFF FFFF</td>
<td>H'E606 006C</td>
<td>32</td>
<td>—</td>
</tr>
<tr>
<td>IICDVFS and TDBG IO cell control register</td>
<td>IOCTRL7</td>
<td>R/W</td>
<td>H'0000 0000</td>
<td>H'E606 0070</td>
<td>32</td>
<td>—</td>
</tr>
</tbody>
</table>
5.3 Register Description

[Legend]

Initial value: Register value after a reset
— : Undefined value
R/W: Readable/writable. The written value can be read.
R: Read-only. The write value should always be 0.
R/WC0: Readable/writable. Writing 0 initializes the bit. Writing 1 is ignored.
R/WC1: Readable/writable. Writing 1 initializes the bit. Writing 0 is ignored.
W: Write-only. Reading this bit is prohibited. When the bit is reserved, the write value should always be 0.
—/W: Write-only. The read value is undefined.

All the bits are active high unless otherwise specified, and deactivated on reset.

All access to registers is made in longword units.

The write value to a reserved bit should always be 0.
5.3.1 LSI Multiplexed Pin Setting Mask Register (PMMR)

Function: PMMR enables/disables writing to the multiplexed pin setting registers.

<table>
<thead>
<tr>
<th>Bit: 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16</th>
</tr>
</thead>
<tbody>
<tr>
<td>Initial value: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>R/W: R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit: 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Initial value: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>R/W: R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W</td>
</tr>
</tbody>
</table>

Note: This register must be set before setting each of the GPIO/peripheral function select registers GPSR0 to GPSR6, peripheral function select registers IPSR0 to IPSR13, module select registers MOD_SEL, MOD_SEL2 and MOD_SEL3, IO cell control registers IOCTRL0 to IOCTRL3 and IOCTRL7.

5.3.2 GPIO/Peripheral Function Select Register 0 (GPSR0)

Function: GPSR0 selects the functions of the multiplexed LSI pins.

<table>
<thead>
<tr>
<th>Bit: 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16</th>
</tr>
</thead>
<tbody>
<tr>
<td>Initial value: 1/0 1/0 1/0 1/0 1/0 1/0 1/0 1/0 1/0 1/0 1/0 1/0 1/0 1/0 1/0</td>
</tr>
<tr>
<td>R/W: R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit: 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Initial value: 1/0 1/0 1/0 1/0 1/0 1/0 1/0 1/0 1/0 1/0 1/0 1/0 1/0 1/0 1/0</td>
</tr>
<tr>
<td>R/W: R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31 to 0</td>
<td>GP0[31:0]</td>
<td>H'FFFF FFFF (when md[3:1] = 000), H'0000 0000 (when md[3:1] ≠ 000)</td>
<td>R/W</td>
<td>The functions of the LSI pins are selected according to the table below.</td>
</tr>
</tbody>
</table>

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.
<table>
<thead>
<tr>
<th>Bit Name</th>
<th>GPIO (Set Value = 0)</th>
<th>Peripheral Function (Set Value = 1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GP0[0]</td>
<td>GP-0-0</td>
<td>peripheral function selected by IP0[23:22]</td>
</tr>
<tr>
<td>GP0[1]</td>
<td>GP-0-1</td>
<td>peripheral function selected by IP0[24]</td>
</tr>
<tr>
<td>GP0[2]</td>
<td>GP-0-2</td>
<td>peripheral function selected by IP0[25]</td>
</tr>
<tr>
<td>GP0[3]</td>
<td>GP-0-3</td>
<td>peripheral function selected by IP0[27:26]</td>
</tr>
<tr>
<td>GP0[4]</td>
<td>GP-0-4</td>
<td>peripheral function selected by IP0[29:28]</td>
</tr>
<tr>
<td>GP0[5]</td>
<td>GP-0-5</td>
<td>peripheral function selected by IP0[31:30]</td>
</tr>
<tr>
<td>GP0[6]</td>
<td>GP-0-6</td>
<td>peripheral function selected by IP1[1:0]</td>
</tr>
<tr>
<td>GP0[7]</td>
<td>GP-0-7</td>
<td>peripheral function selected by IP1[3:2]</td>
</tr>
<tr>
<td>GP0[8]</td>
<td>GP-0-8</td>
<td>peripheral function selected by IP1[5:4]</td>
</tr>
<tr>
<td>GP0[9]</td>
<td>GP-0-9</td>
<td>peripheral function selected by IP1[7:6]</td>
</tr>
<tr>
<td>GP0[10]</td>
<td>GP-0-10</td>
<td>peripheral function selected by IP1[10:8]</td>
</tr>
<tr>
<td>GP0[12]</td>
<td>GP-0-12</td>
<td>peripheral function selected by IP1[14:13]</td>
</tr>
<tr>
<td>GP0[13]</td>
<td>GP-0-13</td>
<td>peripheral function selected by IP1[17:15]</td>
</tr>
<tr>
<td>GP0[14]</td>
<td>GP-0-14</td>
<td>peripheral function selected by IP1[19:18]</td>
</tr>
<tr>
<td>GP0[16]</td>
<td>GP-0-16</td>
<td>peripheral function selected by IP1[23:22]</td>
</tr>
<tr>
<td>GP0[17]</td>
<td>GP-0-17</td>
<td>peripheral function selected by IP1[24]</td>
</tr>
<tr>
<td>GP0[18]</td>
<td>GP-0-18</td>
<td>A2</td>
</tr>
<tr>
<td>GP0[19]</td>
<td>GP-0-19</td>
<td>peripheral function selected by IP1[26]</td>
</tr>
<tr>
<td>GP0[20]</td>
<td>GP-0-20</td>
<td>peripheral function selected by IP1[27]</td>
</tr>
<tr>
<td>GP0[21]</td>
<td>GP-0-21</td>
<td>peripheral function selected by IP1[29:28]</td>
</tr>
<tr>
<td>GP0[22]</td>
<td>GP-0-22</td>
<td>peripheral function selected by IP1[31:30]</td>
</tr>
<tr>
<td>GP0[23]</td>
<td>GP-0-23</td>
<td>peripheral function selected by IP2[1:0]</td>
</tr>
<tr>
<td>GP0[24]</td>
<td>GP-0-24</td>
<td>peripheral function selected by IP2[3:2]</td>
</tr>
<tr>
<td>GP0[25]</td>
<td>GP-0-25</td>
<td>peripheral function selected by IP2[5:4]</td>
</tr>
<tr>
<td>GP0[26]</td>
<td>GP-0-26</td>
<td>peripheral function selected by IP2[7:6]</td>
</tr>
<tr>
<td>GP0[27]</td>
<td>GP-0-27</td>
<td>peripheral function selected by IP2[9:8]</td>
</tr>
<tr>
<td>GP0[28]</td>
<td>GP-0-28</td>
<td>peripheral function selected by IP2[11:10]</td>
</tr>
<tr>
<td>GP0[29]</td>
<td>GP-0-29</td>
<td>peripheral function selected by IP2[13:12]</td>
</tr>
<tr>
<td>GP0[30]</td>
<td>GP-0-30</td>
<td>peripheral function selected by IP2[15:14]</td>
</tr>
<tr>
<td>GP0[31]</td>
<td>GP-0-31</td>
<td>peripheral function selected by IP2[17:16]</td>
</tr>
</tbody>
</table>
5.3.3 GPIO/Peripheral Function Select Register 1 (GPSR1)

Function: GPSR1 selects the functions of the multiplexed LSI pins.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31 to 0</td>
<td>GP1[31:0]</td>
<td>H’00EC 0FFF</td>
<td>R/W</td>
<td>The functions of the LSI pins are selected according to the table below.</td>
</tr>
</tbody>
</table>

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>GPIO (Set Value = 0)</th>
<th>Peripheral Function (Set Value = 1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GP1[0]</td>
<td>GP-1-0</td>
<td>Peripheral function selected by IP2[20:18]</td>
</tr>
<tr>
<td>GP1[1]</td>
<td>GP-1-1</td>
<td>Peripheral function selected by IP2[23:21]</td>
</tr>
<tr>
<td>GP1[3]</td>
<td>GP-1-3</td>
<td>Peripheral function selected by IP2[29:27]</td>
</tr>
<tr>
<td>GP1[4]</td>
<td>GP-1-4</td>
<td>Peripheral function selected by IP2[31:30]</td>
</tr>
<tr>
<td>GP1[5]</td>
<td>GP-1-5</td>
<td>Peripheral function selected by IP3[1:0]</td>
</tr>
<tr>
<td>GP1[6]</td>
<td>GP-1-6</td>
<td>Peripheral function selected by IP3[3:2]</td>
</tr>
<tr>
<td>GP1[8]</td>
<td>GP-1-8</td>
<td>Peripheral function selected by IP3[7:6]</td>
</tr>
<tr>
<td>GP1[9]</td>
<td>GP-1-9</td>
<td>Peripheral function selected by IP3[9:8]</td>
</tr>
<tr>
<td>GP1[10]</td>
<td>GP-1-10</td>
<td>Peripheral function selected by IP3[10]</td>
</tr>
<tr>
<td>GP1[12]</td>
<td>GP-1-12</td>
<td>Peripheral function selected by IP3[12]</td>
</tr>
<tr>
<td>GP1[14]</td>
<td>GP-1-14</td>
<td>Peripheral function selected by IP3[17:15]</td>
</tr>
<tr>
<td>GP1[16]</td>
<td>GP-1-16</td>
<td>Peripheral function selected by IP3[23:21]</td>
</tr>
<tr>
<td>GP1[17]</td>
<td>GP-1-17</td>
<td>Peripheral function selected by IP3[26:24]</td>
</tr>
<tr>
<td>GP1[18]</td>
<td>GP-1-18</td>
<td>Peripheral function selected by IP3[29:27]</td>
</tr>
<tr>
<td>GP1[19]</td>
<td>GP-1-19</td>
<td>Peripheral function selected by IP3[30]</td>
</tr>
<tr>
<td>GP1[20]</td>
<td>GP-1-20</td>
<td>Peripheral function selected by IP3[31]</td>
</tr>
<tr>
<td>GP1[21]</td>
<td>GP-1-21</td>
<td>WE0_N</td>
</tr>
</tbody>
</table>

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<table>
<thead>
<tr>
<th>Bit Name</th>
<th>GPIO (Set Value = 0)</th>
<th>Peripheral Function (Set Value = 1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GP1[22]</td>
<td>GP-1-22</td>
<td>WE1_N</td>
</tr>
<tr>
<td>GP1[23]</td>
<td>GP-1-23</td>
<td>Peripheral function selected by IP4[1:0]</td>
</tr>
<tr>
<td>GP1[24]</td>
<td>GP-1-24</td>
<td>Peripheral function selected by IP7[31]</td>
</tr>
<tr>
<td>GP1[25]</td>
<td>GP-1-25</td>
<td>DACK0</td>
</tr>
<tr>
<td>GP1[26]</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>GP1[27]</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>GP1[28]</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>GP1[29]</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>GP1[30]</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>GP1[31]</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>
### 5.3.4 GPIO/Peripheral Function Select Register 2 (GPSR2)

Function: GPSR2 selects the functions of the multiplexed LSI pins.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31 to 0</td>
<td>H'0000 0000</td>
<td>R/W</td>
<td>The functions of the LSI pins are selected according to the table below.</td>
</tr>
</tbody>
</table>

#### Bit Name | GPIO (Set Value = 0) | Peripheral Function (Set Value = 1) |
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>GP2[31]</td>
<td>GP-2-0</td>
<td>Peripheral function selected by IP4[4:2]</td>
</tr>
<tr>
<td>GP2[29]</td>
<td>GP-2-2</td>
<td>Peripheral function selected by IP4[9:8]</td>
</tr>
<tr>
<td>GP2[27]</td>
<td>GP-2-4</td>
<td>Peripheral function selected by IP4[13:12]</td>
</tr>
<tr>
<td>GP2[26]</td>
<td>GP-2-5</td>
<td>Peripheral function selected by IP4[15:14]</td>
</tr>
<tr>
<td>GP2[25]</td>
<td>GP-2-6</td>
<td>Peripheral function selected by IP4[17:16]</td>
</tr>
<tr>
<td>GP2[23]</td>
<td>GP-2-8</td>
<td>Peripheral function selected by IP4[22:20]</td>
</tr>
<tr>
<td>GP2[22]</td>
<td>GP-2-9</td>
<td>Peripheral function selected by IP4[25:23]</td>
</tr>
<tr>
<td>GP2[21]</td>
<td>GP-2-10</td>
<td>Peripheral function selected by IP4[27:26]</td>
</tr>
<tr>
<td>GP2[19]</td>
<td>GP-2-12</td>
<td>Peripheral function selected by IP4[31:30]</td>
</tr>
<tr>
<td>GP2[18]</td>
<td>GP-2-13</td>
<td>Peripheral function selected by IP5[1:0]</td>
</tr>
<tr>
<td>GP2[17]</td>
<td>GP-2-14</td>
<td>Peripheral function selected by IP5[3:2]</td>
</tr>
<tr>
<td>GP2[10]</td>
<td>GP-2-21</td>
<td>Peripheral function selected by IP5[19:18]</td>
</tr>
<tr>
<td>GP2[8]</td>
<td>GP-2-23</td>
<td>Peripheral function selected by IP5[23:22]</td>
</tr>
</tbody>
</table>

**Note:** To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.
### 5. Pin Function Controller (PFC)

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>GPIO (Set Value = 0)</th>
<th>Peripheral Function (Set Value = 1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GP[26]</td>
<td>GP-2-26</td>
<td>Peripheral function selected by IP5[29:28]</td>
</tr>
<tr>
<td>GP[27]</td>
<td>GP-2-27</td>
<td>Peripheral function selected by IP5[31:30]</td>
</tr>
<tr>
<td>GP[28]</td>
<td>GP-2-28</td>
<td>Peripheral function selected by IP6[1:0]</td>
</tr>
<tr>
<td>GP[29]</td>
<td>GP-2-29</td>
<td>Peripheral function selected by IP6[3:2]</td>
</tr>
<tr>
<td>GP[31]</td>
<td>GP-2-31</td>
<td>Peripheral function selected by IP6[7:6]</td>
</tr>
</tbody>
</table>
### 5.3.5 GPIO/Peripheral Function Select Register 3 (GPSR3)

Function: GPSR3 selects the functions of the multiplexed LSI pins.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>GP3[31:0]</td>
<td>H'0000 0000</td>
<td>R/W</td>
<td>The functions of the LSI pins are selected according to the table below.</td>
</tr>
</tbody>
</table>

#### Note

To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>GPIO (Set Value = 0)</th>
<th>Peripheral Function (Set Value = 1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GP3[0]</td>
<td>GP-3-0</td>
<td>Peripheral function selected by IP6[8]</td>
</tr>
<tr>
<td>GP3[1]</td>
<td>GP-3-1</td>
<td>Peripheral function selected by IP6[9]</td>
</tr>
<tr>
<td>GP3[2]</td>
<td>GP-3-2</td>
<td>Peripheral function selected by IP6[10]</td>
</tr>
<tr>
<td>GP3[4]</td>
<td>GP-3-4</td>
<td>Peripheral function selected by IP6[12]</td>
</tr>
<tr>
<td>GP3[5]</td>
<td>GP-3-5</td>
<td>Peripheral function selected by IP6[13]</td>
</tr>
<tr>
<td>GP3[6]</td>
<td>GP-3-6</td>
<td>Peripheral function selected by IP6[14]</td>
</tr>
<tr>
<td>GP3[7]</td>
<td>GP-3-7</td>
<td>Peripheral function selected by IP6[15]</td>
</tr>
<tr>
<td>GP3[8]</td>
<td>GP-3-8</td>
<td>Peripheral function selected by IP6[16]</td>
</tr>
<tr>
<td>GP3[9]</td>
<td>GP-3-9</td>
<td>Peripheral function selected by IP6[19:17]</td>
</tr>
<tr>
<td>GP3[10]</td>
<td>GP-3-10</td>
<td>Peripheral function selected by IP6[22:20]</td>
</tr>
<tr>
<td>GP3[12]</td>
<td>GP-3-12</td>
<td>Peripheral function selected by IP6[28:26]</td>
</tr>
<tr>
<td>GP3[13]</td>
<td>GP-3-13</td>
<td>Peripheral function selected by IP6[31:29]</td>
</tr>
<tr>
<td>GP3[14]</td>
<td>GP-3-14</td>
<td>Peripheral function selected by IP7[2:0]</td>
</tr>
<tr>
<td>GP3[15]</td>
<td>GP-3-15</td>
<td>Peripheral function selected by IP7[5:3]</td>
</tr>
<tr>
<td>GP3[16]</td>
<td>GP-3-16</td>
<td>Peripheral function selected by IP7[8:6]</td>
</tr>
<tr>
<td>GP3[17]</td>
<td>GP-3-17</td>
<td>Peripheral function selected by IP7[11:9]</td>
</tr>
<tr>
<td>GP3[18]</td>
<td>GP-3-18</td>
<td>Peripheral function selected by IP7[14:12]</td>
</tr>
<tr>
<td>GP3[19]</td>
<td>GP-3-19</td>
<td>Peripheral function selected by IP7[17:15]</td>
</tr>
<tr>
<td>GP3[20]</td>
<td>GP-3-20</td>
<td>Peripheral function selected by IP7[20:18]</td>
</tr>
<tr>
<td>GP3[21]</td>
<td>GP-3-21</td>
<td>Peripheral function selected by IP7[23:21]</td>
</tr>
<tr>
<td>GP3[22]</td>
<td>GP-3-22</td>
<td>Peripheral function selected by IP7[26:24]</td>
</tr>
<tr>
<td>GP3[23]</td>
<td>GP-3-23</td>
<td>Peripheral function selected by IP7[29:27]</td>
</tr>
<tr>
<td>GP3[24]</td>
<td>GP-3-24</td>
<td>Peripheral function selected by IP8[2:0]</td>
</tr>
</tbody>
</table>
### Bit Name | GPIO (Set Value = 0) | Peripheral Function (Set Value = 1)
--- | --- | ---
GP3[25] | GP-3-25 | Peripheral function selected by IP8[5:3]
GP3[26] | GP-3-26 | Peripheral function selected by IP8[8:6]
GP3[27] | GP-3-27 | Peripheral function selected by IP8[11:9]
GP3[28] | GP-3-28 | Peripheral function selected by IP8[14:12]
GP3[29] | GP-3-29 | Peripheral function selected by IP8[16:15]
GP3[30] | GP-3-30 | Peripheral function selected by IP8[19:17]
GP3[31] | GP-3-31 | Peripheral function selected by IP8[22:20]
### 5.3.6 GPIO/Peripheral Function Select Register 4 (GPSR4)

Function: GPSR4 selects the functions of the multiplexed LSI pins.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>GP4[31]</td>
<td>H’0000 0000</td>
<td>R/W</td>
<td>The functions of the LSI pins are selected according to the table below.</td>
</tr>
</tbody>
</table>

#### Note:
To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>GPIO (Set Value = 0)</th>
<th>Peripheral Function (Set Value = 1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GP4[0]</td>
<td>GP-4-0</td>
<td>Peripheral function selected by IP8[25:23]</td>
</tr>
<tr>
<td>GP4[1]</td>
<td>GP-4-1</td>
<td>Peripheral function selected by IP8[28:26]</td>
</tr>
<tr>
<td>GP4[2]</td>
<td>GP-4-2</td>
<td>Peripheral function selected by IP8[31:29]</td>
</tr>
<tr>
<td>GP4[3]</td>
<td>GP-4-3</td>
<td>Peripheral function selected by IP9[2:0]</td>
</tr>
<tr>
<td>GP4[4]</td>
<td>GP-4-4</td>
<td>Peripheral function selected by IP9[5:3]</td>
</tr>
<tr>
<td>GP4[7]</td>
<td>GP-4-7</td>
<td>Peripheral function selected by IP9[14:12]</td>
</tr>
<tr>
<td>GP4[8]</td>
<td>GP-4-8</td>
<td>Peripheral function selected by IP9[16:15]</td>
</tr>
<tr>
<td>GP4[9]</td>
<td>GP-4-9</td>
<td>Peripheral function selected by IP9[18:17]</td>
</tr>
<tr>
<td>GP4[10]</td>
<td>GP-4-10</td>
<td>Peripheral function selected by IP9[21:19]</td>
</tr>
<tr>
<td>GP4[12]</td>
<td>GP-4-12</td>
<td>Peripheral function selected by IP9[27:25]</td>
</tr>
<tr>
<td>GP4[14]</td>
<td>GP-4-14</td>
<td>Peripheral function selected by IP10[2:0]</td>
</tr>
<tr>
<td>GP4[15]</td>
<td>GP-4-15</td>
<td>Peripheral function selected by IP10[5:3]</td>
</tr>
<tr>
<td>GP4[16]</td>
<td>GP-4-16</td>
<td>Peripheral function selected by IP10[8:6]</td>
</tr>
<tr>
<td>GP4[17]</td>
<td>GP-4-17</td>
<td>Peripheral function selected by IP10[11:9]</td>
</tr>
<tr>
<td>GP4[18]</td>
<td>GP-4-18</td>
<td>Peripheral function selected by IP10[14:12]</td>
</tr>
<tr>
<td>GP4[19]</td>
<td>GP-4-19</td>
<td>Peripheral function selected by IP10[17:15]</td>
</tr>
<tr>
<td>GP4[20]</td>
<td>GP-4-20</td>
<td>Peripheral function selected by IP10[20:18]</td>
</tr>
<tr>
<td>GP4[21]</td>
<td>GP-4-21</td>
<td>Peripheral function selected by IP10[23:21]</td>
</tr>
<tr>
<td>GP4[22]</td>
<td>GP-4-22</td>
<td>Peripheral function selected by IP10[26:24]</td>
</tr>
<tr>
<td>GP4[23]</td>
<td>GP-4-23</td>
<td>Peripheral function selected by IP10[29:27]</td>
</tr>
<tr>
<td>GP4[24]</td>
<td>GP-4-24</td>
<td>Peripheral function selected by IP10[31:30]</td>
</tr>
</tbody>
</table>
## Pin Function Controller (PFC)

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>GPIO (Set Value = 0)</th>
<th>Peripheral Function (Set Value = 1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GP4[25]</td>
<td>GP-4-25</td>
<td>Peripheral function selected by IP11[2:0]</td>
</tr>
<tr>
<td>GP4[26]</td>
<td>GP-4-26</td>
<td>Peripheral function selected by IP11[5:3]</td>
</tr>
<tr>
<td>GP4[27]</td>
<td>GP-4-27</td>
<td>Peripheral function selected by IP11[7:6]</td>
</tr>
<tr>
<td>GP4[28]</td>
<td>GP-4-28</td>
<td>Peripheral function selected by IP11[10:8]</td>
</tr>
<tr>
<td>GP4[29]</td>
<td>GP-4-29</td>
<td>Peripheral function selected by IP11[13:11]</td>
</tr>
<tr>
<td>GP4[30]</td>
<td>GP-4-30</td>
<td>Peripheral function selected by IP11[15:14]</td>
</tr>
<tr>
<td>GP4[31]</td>
<td>GP-4-31</td>
<td>Peripheral function selected by IP11[17:16]</td>
</tr>
</tbody>
</table>
5.3.7  GPIO/Peripheral Function Select Register 5 (GPSR5)

Function: GPSR5 selects the functions of the multiplexed LSI pins.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>GP5[31]</td>
<td>H’0F00 0000</td>
<td>R/W</td>
<td>The functions of the LSI pins are selected according to the table below.</td>
</tr>
</tbody>
</table>

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>GPIO (Set Value = 0)</th>
<th>Peripheral Function (Set Value = 1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GP5[0]</td>
<td>GP-5-0</td>
<td>Peripheral function selected by IP11[20:18]</td>
</tr>
<tr>
<td>GP5[3]</td>
<td>GP-5-3</td>
<td>Peripheral function selected by IP11[29:27]</td>
</tr>
<tr>
<td>GP5[5]</td>
<td>GP-5-5</td>
<td>Peripheral function selected by IP12[5:3]</td>
</tr>
<tr>
<td>GP5[9]</td>
<td>GP-5-9</td>
<td>Peripheral function selected by IP12[14:13]</td>
</tr>
<tr>
<td>GP5[10]</td>
<td>GP-5-10</td>
<td>Peripheral function selected by IP12[17:15]</td>
</tr>
<tr>
<td>GP5[12]</td>
<td>GP-5-12</td>
<td>Peripheral function selected by IP12[23:21]</td>
</tr>
<tr>
<td>GP5[14]</td>
<td>GP-5-14</td>
<td>Peripheral function selected by IP12[29:27]</td>
</tr>
<tr>
<td>GP5[16]</td>
<td>GP-5-16</td>
<td>Peripheral function selected by IP13[5:3]</td>
</tr>
<tr>
<td>GP5[17]</td>
<td>GP-5-17</td>
<td>Peripheral function selected by IP13[8:6]</td>
</tr>
<tr>
<td>GP5[19]</td>
<td>GP-5-19</td>
<td>Peripheral function selected by IP13[14:12]</td>
</tr>
<tr>
<td>GP5[21]</td>
<td>GP-5-21</td>
<td>Peripheral function selected by IP13[20:18]</td>
</tr>
<tr>
<td>GP5[22]</td>
<td>GP-5-22</td>
<td>Peripheral function selected by IP13[23:21]</td>
</tr>
<tr>
<td>GP5[23]</td>
<td>GP-5-23</td>
<td>Peripheral function selected by IP13[26:24]</td>
</tr>
<tr>
<td>GP5[24]</td>
<td>GP-5-24</td>
<td>USB0_PWEN</td>
</tr>
</tbody>
</table>

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.
<table>
<thead>
<tr>
<th>Bit Name</th>
<th>GPIO (Set Value = 0)</th>
<th>Peripheral Function (Set Value = 1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GP5[25]</td>
<td>GP-5-25</td>
<td>USB0_OVC</td>
</tr>
<tr>
<td>GP5[26]</td>
<td>GP-5-26</td>
<td>USB1_PWEN</td>
</tr>
<tr>
<td>GP5[27]</td>
<td>GP-5-27</td>
<td>USB1_OVC</td>
</tr>
<tr>
<td>GP5[28]</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>GP5[29]</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>GP5[30]</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>GP5[31]</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>
5.3.8 GPIO/Peripheral Function Select Register 6 (GPSR6)

Function: GPSR6 selects the functions of the multiplexed LSI pins.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31 to 0</td>
<td>GP6[31:0]</td>
<td>H'0000 0000</td>
<td>R/W</td>
<td>The functions of the LSI pins are selected according to the table below.</td>
</tr>
</tbody>
</table>

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>GPIO (Set Value = 0)</th>
<th>Peripheral Function (Set Value = 1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GP6[0]</td>
<td>GP-6-0</td>
<td>SD0_CLK</td>
</tr>
<tr>
<td>GP6[1]</td>
<td>GP-6-1</td>
<td>SD0_CMD</td>
</tr>
<tr>
<td>GP6[2]</td>
<td>GP-6-2</td>
<td>SD0_DATA0</td>
</tr>
<tr>
<td>GP6[3]</td>
<td>GP-6-3</td>
<td>SD0_DATA1</td>
</tr>
<tr>
<td>GP6[4]</td>
<td>GP-6-4</td>
<td>SD0_DATA2</td>
</tr>
<tr>
<td>GP6[5]</td>
<td>GP-6-5</td>
<td>SD0_DATA3</td>
</tr>
<tr>
<td>GP6[6]</td>
<td>GP-6-6</td>
<td>SD0_CD</td>
</tr>
<tr>
<td>GP6[7]</td>
<td>GP-6-7</td>
<td>SD0_WP</td>
</tr>
<tr>
<td>GP6[8]</td>
<td>GP-6-8</td>
<td>SD1_CLK</td>
</tr>
<tr>
<td>GP6[9]</td>
<td>GP-6-9</td>
<td>SD1_CMD</td>
</tr>
<tr>
<td>GP6[10]</td>
<td>GP-6-10</td>
<td>SD1_DATA0</td>
</tr>
<tr>
<td>GP6[11]</td>
<td>GP-6-11</td>
<td>SD1_DATA1</td>
</tr>
<tr>
<td>GP6[12]</td>
<td>GP-6-12</td>
<td>SD1_DATA2</td>
</tr>
<tr>
<td>GP6[13]</td>
<td>GP-6-13</td>
<td>SD1_DATA3</td>
</tr>
<tr>
<td>GP6[14]</td>
<td>GP-6-14</td>
<td>Peripheral function selected by IP0[0]</td>
</tr>
<tr>
<td>GP6[15]</td>
<td>GP-6-15</td>
<td>Peripheral function selected by IP0[9:8]</td>
</tr>
<tr>
<td>GP6[16]</td>
<td>GP-6-16</td>
<td>Peripheral function selected by IP0[10]</td>
</tr>
<tr>
<td>GP6[17]</td>
<td>GP-6-17</td>
<td>Peripheral function selected by IP0[11]</td>
</tr>
<tr>
<td>GP6[18]</td>
<td>GP-6-18</td>
<td>Peripheral function selected by IP0[12]</td>
</tr>
<tr>
<td>GP6[19]</td>
<td>GP-6-19</td>
<td>Peripheral function selected by IP0[13]</td>
</tr>
<tr>
<td>GP6[20]</td>
<td>GP-6-20</td>
<td>Peripheral function selected by IP0[14]</td>
</tr>
<tr>
<td>GP6[21]</td>
<td>GP-6-21</td>
<td>Peripheral function selected by IP0[15]</td>
</tr>
<tr>
<td>GP6[22]</td>
<td>GP-6-22</td>
<td>Peripheral function selected by IP0[16]</td>
</tr>
<tr>
<td>GP6[23]</td>
<td>GP-6-23</td>
<td>Peripheral function selected by IP0[17]</td>
</tr>
<tr>
<td>GP6[24]</td>
<td>GP-6-24</td>
<td>Peripheral function selected by IP0[19:18]</td>
</tr>
</tbody>
</table>
## Bit Name | GPIO (Set Value = 0) | Peripheral Function (Set Value = 1)
--- | --- | ---
GP6[25] | GP-6-25 | Peripheral function selected by IP0[21:20]
GP6[26] | - | -
GP6[27] | - | -
GP6[28] | - | -
GP6[29] | - | -
GP6[30] | - | -
GP6[31] | - | -
5.3.9 Peripheral Function Select Register 0 (IPSR0)

Function: IPSR0 selects the functions of the multiplexed LSI pins.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31 to 0</td>
<td>H'0000 0000</td>
<td>R/W</td>
<td>The functions of the LSI pins are selected according to the table below.</td>
</tr>
</tbody>
</table>

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Function 1 (Set Value = H'0)</th>
<th>Function 2 (Set Value = H'1)</th>
<th>Function 3 (Set Value = H'2)</th>
<th>Function 4 (Set Value = H'3)</th>
<th>Function 5 (Set Value = H'4)</th>
<th>Function 6 (Set Value = H'5)</th>
<th>Others (Set Value = H'6 to H'F)</th>
</tr>
</thead>
<tbody>
<tr>
<td>IP0[0]</td>
<td>SD1_CD</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>CAN0_RX</td>
</tr>
<tr>
<td>IP0[9:8]</td>
<td>SD1_WP</td>
<td>IRC7</td>
<td>CAN0_TX</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>SD2_CLK</td>
</tr>
<tr>
<td>IP0[10]</td>
<td>MMC_CLK</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>SD2_CLK</td>
</tr>
<tr>
<td>IP0[11]</td>
<td>MMC_CMD</td>
<td>SD2_CMD</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>MMC_CLK</td>
</tr>
<tr>
<td>IP0[12]</td>
<td>MMC_D0</td>
<td>SD2_DATA0</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>MMC_CMD</td>
</tr>
<tr>
<td>IP0[13]</td>
<td>MMC_D1</td>
<td>SD2_DATA1</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>MMC_D0</td>
</tr>
<tr>
<td>IP0[14]</td>
<td>MMC_D2</td>
<td>SD2_DATA2</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>MMC_D1</td>
</tr>
<tr>
<td>IP0[15]</td>
<td>MMC_D3</td>
<td>SD2_DATA3</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>MMC_D2</td>
</tr>
<tr>
<td>IP0[16]</td>
<td>MMC_D4</td>
<td>SD2_CD</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>MMC_D3</td>
</tr>
<tr>
<td>IP0[17]</td>
<td>MMC_D5</td>
<td>SD2_WP</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>MMC_D4</td>
</tr>
<tr>
<td>IP0[19:18]</td>
<td>MMC_D6</td>
<td>SCIIFO_RXD</td>
<td>-</td>
<td>I2C2_SCL_B</td>
<td>CAN1_RX</td>
<td>-</td>
<td>MMC_D5</td>
</tr>
<tr>
<td>IP0[21:20]</td>
<td>MMC_D7</td>
<td>SCIIFO_TXD</td>
<td>I2C2_SDA_B</td>
<td>CAN1_TX</td>
<td>-</td>
<td>-</td>
<td>SCIIFO_RXD</td>
</tr>
<tr>
<td>IP0[23:22]</td>
<td>D0</td>
<td>SCIIFA3_SCK_B</td>
<td>IRC4</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>SCIIFO_TXD</td>
</tr>
<tr>
<td>IP0[24]</td>
<td>D1</td>
<td>SCIIFA3_RXD_B</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>SCIIFA3_SCK_B</td>
</tr>
<tr>
<td>IP0[25]</td>
<td>D2</td>
<td>SCIIFA3_TXD_B</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>SCIIFA3_RXD_B</td>
</tr>
<tr>
<td>IP0[27:26]</td>
<td>D3</td>
<td>I2C3_SCL_B</td>
<td>SCIIF5_RXD_B</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>SCIIFA3_TXD_B</td>
</tr>
<tr>
<td>IP0[29:28]</td>
<td>D4</td>
<td>I2C3_SDA_B</td>
<td>SCIIF5_TXD_B</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>I2C3_SCL_B</td>
</tr>
<tr>
<td>IP0[31:30]</td>
<td>D5</td>
<td>SCIIF4_RXD_B</td>
<td>I2C0_SCL_B</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>SCIIF5_RXD_B</td>
</tr>
</tbody>
</table>

Legend: - Setting prohibited
### 5.3.10 Peripheral Function Select Register 1 (IPSR1)

Function: IPSR1 selects the functions of the multiplexed LSI pins.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31 to 0</td>
<td>H'0000 0000</td>
<td>R/W</td>
<td>The functions of the LSI pins are selected according to the table below.</td>
</tr>
</tbody>
</table>

**Note:** To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Function 1 (Set Value = H'0)</th>
<th>Function 2 (Set Value = H'1)</th>
<th>Function 3 (Set Value = H'2)</th>
<th>Function 4 (Set Value = H'3)</th>
<th>Function 5 (Set Value = H'4)</th>
<th>Function 6 (Set Value = H'5)</th>
<th>Function 7 (Set Value = H'6)</th>
<th>Others (Set Value = H'7 to H'F)</th>
</tr>
</thead>
<tbody>
<tr>
<td>IP1[10]</td>
<td>D6 SCIF4_TXD_B</td>
<td>I2C0_SDA_D</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP1[15]</td>
<td>D7 IRQ3</td>
<td>TCLK1</td>
<td>PWM6_B</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP1[14]</td>
<td>D8 HSCIF2_HRX</td>
<td>I2C1_SCL_B</td>
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<td>-</td>
<td>-</td>
<td>-</td>
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<tr>
<td>IP1[13]</td>
<td>D9 HSCIF2_HTX</td>
<td>I2C1_SDA_B</td>
<td>-</td>
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</tr>
<tr>
<td>IP1[12]</td>
<td>D0 HSCIF2_HSCK</td>
<td>SCIF1_SCK_C</td>
<td>IRQ6</td>
<td>PWM5_C</td>
<td>-</td>
<td>-</td>
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<td>-</td>
</tr>
<tr>
<td>IP1[11]</td>
<td>D1 HSCIF2_HRTS_N</td>
<td>SCIF1_RXD_C</td>
<td>I2C1_SCL_D</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP1[10]</td>
<td>D2 HSCIF2_HRTS_N</td>
<td>SCIF1_TXD_C</td>
<td>I2C1_SDA_D</td>
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<td>IP1[9]</td>
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<td>PWM2_C</td>
<td>TCLK2_B</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP1[8]</td>
<td>D14 SCIFA1_RXD</td>
<td>I2C5_SCL_B</td>
<td>-</td>
<td>-</td>
<td>-</td>
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<td>-</td>
</tr>
<tr>
<td>IP1[7]</td>
<td>D15 SCIFA1_TXD</td>
<td>I2C5_SDA_B</td>
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<td>-</td>
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<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP1[6]</td>
<td>D16 SCIFB1_SCK</td>
<td>PWM3_B</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP1[5]</td>
<td>D17 A1 SCIFB1_TXD</td>
<td>-</td>
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<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP1[4]</td>
<td>D18 A2 SCIFB0_SCK</td>
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<td>IP1[3]</td>
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</tr>
<tr>
<td>IP1[2]</td>
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<td>PWM4_B</td>
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<td>IP1[1]</td>
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<td>TPUTO2_C</td>
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<td>-</td>
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<td>-</td>
</tr>
</tbody>
</table>

Legend:  
- Setting prohibited
### 5.3.11 Peripheral Function Select Register 2 (IPSR2)

Function: IPSR2 selects the functions of the multiplexed LSI pins.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31 to 0</td>
<td>H'0000 0000</td>
<td>R/W</td>
<td>The functions of the LSI pins are selected according to the table below.</td>
</tr>
</tbody>
</table>

**Note:** To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Function 1 (Set Value = H'0)</th>
<th>Function 2 (Set Value = H'1)</th>
<th>Function 3 (Set Value = H'2)</th>
<th>Function 4 (Set Value = H'3)</th>
<th>Function 5 (Set Value = H'4)</th>
<th>Function 6 (Set Value = H'5)</th>
<th>Function 7 (Set Value = H'6)</th>
<th>Function 8 (Set Value = H'7)</th>
<th>Others (Set Value = H'8 to H'F)</th>
</tr>
</thead>
<tbody>
<tr>
<td>IP2[1:0]</td>
<td>A7</td>
<td>SCIFB0_RTS_N</td>
<td>SCIFAF4_TXD_B</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP2[3:2]</td>
<td>A8</td>
<td>MSIOF1_RXD</td>
<td>SCIFAO_RXD_B</td>
<td>-</td>
<td>-</td>
<td>-</td>
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<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP2[5:4]</td>
<td>A9</td>
<td>MSIOF1_TXD</td>
<td>SCIFA0_TXD_B</td>
<td>-</td>
<td>-</td>
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<td>-</td>
</tr>
<tr>
<td>IP2[7:6]</td>
<td>A10</td>
<td>MSIOF1_SCK</td>
<td>IIC0_SCL_B</td>
<td>-</td>
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<td>-</td>
</tr>
<tr>
<td>IP2[9:8]</td>
<td>A11</td>
<td>MSIOF1_SYNC</td>
<td>IIC0_SDA_B</td>
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<td>-</td>
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</tr>
<tr>
<td>IP2[11:10]</td>
<td>A12</td>
<td>MSIOF1_SS1</td>
<td>SCIFAS5_RXD_B</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
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<td>-</td>
</tr>
<tr>
<td>IP2[13:12]</td>
<td>A13</td>
<td>MSIOF1_SS2</td>
<td>SCIFAS5_TXD_B</td>
<td>-</td>
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</tr>
<tr>
<td>IP2[15:14]</td>
<td>A14</td>
<td>MSIOF2_TXD</td>
<td>HSCIF0_HRX_B</td>
<td>DREQ1_N</td>
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<td>-</td>
</tr>
<tr>
<td>IP2[17:16]</td>
<td>A15</td>
<td>MSIOF2_TXD</td>
<td>HSCIF0_HTX_B</td>
<td>DACK1</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP2[20:18]</td>
<td>A16</td>
<td>MSIOF2_SCK</td>
<td>HSCIF0_HSCK_B</td>
<td>Reserved</td>
<td>Reserved</td>
<td>CAN_CLK_C</td>
<td>TPUTO2_B</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP2[23:21]</td>
<td>A17</td>
<td>MSIOF2_SYNC</td>
<td>SCIF4_RXD_E</td>
<td>CAN1_RX_B</td>
<td>Resized</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP2[26:24]</td>
<td>A18</td>
<td>MSIOF2_SS1</td>
<td>SCIF4_TXD_E</td>
<td>CAN1_TX_B</td>
<td>Resized</td>
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<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP2[29:27]</td>
<td>A19</td>
<td>MSIOF2_SS2</td>
<td>PWM4</td>
<td>TPUTO2</td>
<td>Resized</td>
<td>-</td>
<td>-</td>
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<td>-</td>
</tr>
<tr>
<td>IP2[31:30]</td>
<td>A20</td>
<td>SPCLK</td>
<td>Reserved</td>
<td>-</td>
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<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

**Legend:** - Setting prohibited
### 5.3.12 Peripheral Function Select Register 3 (IPSR3)

Function: IPSR3 selects the functions of the multiplexed LSI pins.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>H’0000 0000</td>
<td>R/W</td>
<td>The functions of the LSI pins are selected according to the table below.</td>
</tr>
</tbody>
</table>

**Note:** To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Function 1 (Set Value = H’0)</th>
<th>Function 2 (Set Value = H’1)</th>
<th>Function 3 (Set Value = H’2)</th>
<th>Function 4 (Set Value = H’3)</th>
<th>Function 5 (Set Value = H’4)</th>
<th>Function 6 (Set Value = H’5)</th>
<th>Function 7 (Set Value = H’6)</th>
<th>Function 8 (Set Value = H’7)</th>
<th>Others (Set Value = H’8 to H’F)</th>
</tr>
</thead>
<tbody>
<tr>
<td>IP3[1:0]</td>
<td>A21 MOSI_IO0 Reserved</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP3[3:2]</td>
<td>A22 MISO_IO1 Reserved</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
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<td>-</td>
</tr>
<tr>
<td>IP3[5:4]</td>
<td>A23 IO2 Reserved</td>
<td>ATADIR1_N</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
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</tr>
<tr>
<td>IP3[7:6]</td>
<td>A24 EX_WAIT2</td>
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<tr>
<td>IP3[9:8]</td>
<td>A25 SSL ATARD1_N</td>
<td>-</td>
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<tr>
<td>IP3[10]</td>
<td>CS0_N VI1_DATA8</td>
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<td>-</td>
</tr>
<tr>
<td>IP3[11]</td>
<td>CS1_N_A26 VI1_DATA9</td>
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<tr>
<td>IP3[12]</td>
<td>EX_CS0_N VI1_DATA10</td>
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</tr>
<tr>
<td>IP3[14:13]</td>
<td>EX_CS1_N TPUTO3_B SCIIFB2_RXD</td>
<td>V11_DATA11</td>
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<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP3[17:16]</td>
<td>EX_CS2_N PWM0 SCIIF4_RXD_C</td>
<td>TPUTO3 SCIIFB2_TXD</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
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<td>-</td>
</tr>
<tr>
<td>IP3[20:19]</td>
<td>EX_CS3_N SCIIF2_SCK SCIIF4_TXD_C</td>
<td>Reserved</td>
<td>Reserved</td>
<td>TPUTO3 SCIIFB2_TXD</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP3[23:21]</td>
<td>EX_CS4_N SCIIF2_RXD</td>
<td>I2C2_SCL_E</td>
<td>Reserved</td>
<td>Reserved</td>
<td>SCIIFB2_CTS SCIIF2_CTS</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP3[26:24]</td>
<td>EX_CS5_N SCIIF2_TXD</td>
<td>I2C2_SDA_E</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>SCIIFB2_RTS SCIIF2_RTS</td>
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</tr>
<tr>
<td>IP3[29:27]</td>
<td>BS_N DRACK0 PWM1_C TPUTO0_C</td>
<td>ATAC501_N Reserved</td>
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</tr>
<tr>
<td>IP3[30]</td>
<td>RD_N ATAC511_N</td>
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<tr>
<td>IP3[31]</td>
<td>RD_WR_N ATAG1_N</td>
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</tr>
</tbody>
</table>

Legend: - Setting prohibited
### 5.3.13 Peripheral Function Select Register 4 (IPSR4)

Function: IPSR4 selects the functions of the multiplexed LSI pins.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31 to 0</td>
<td>H'0000 0000</td>
<td>R/W</td>
<td>The functions of the LSI pins are selected according to the table below.</td>
</tr>
</tbody>
</table>

**Note:** To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Function 1 (Set Value = H'0)</th>
<th>Function 2 (Set Value = H'1)</th>
<th>Function 3 (Set Value = H'2)</th>
<th>Function 4 (Set Value = H'3)</th>
<th>Function 5 (Set Value = H'4)</th>
<th>Function 6 (Set Value = H'5)</th>
<th>Others (Set Value = H'6 to H'F)</th>
</tr>
</thead>
<tbody>
<tr>
<td>IP4[1:0]</td>
<td>EX_WAIT0</td>
<td>CAN_CLK_B</td>
<td>SCIF_CLK</td>
<td>Reserved</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP4[4:2]</td>
<td>DU0_DR0</td>
<td>Reserved</td>
<td>SCIF5_RXD_C</td>
<td>I2C2_SCL_D</td>
<td>Reserved</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP4[7:5]</td>
<td>DU0_DR1</td>
<td>Reserved</td>
<td>SCIF5_TXD_C</td>
<td>I2C2_SDA_D</td>
<td>Reserved</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP4[9:8]</td>
<td>DU0_DR2</td>
<td>Reserved</td>
<td>Reserved</td>
<td>-</td>
<td>-</td>
<td>-</td>
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</tr>
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<td>IP4[11:10]</td>
<td>DU0_DR3</td>
<td>Reserved</td>
<td>Reserved</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP4[13:12]</td>
<td>DU0_DR4</td>
<td>Reserved</td>
<td>Reserved</td>
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<td>-</td>
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<td>-</td>
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<td>IP4[15:14]</td>
<td>DU0_DR5</td>
<td>Reserved</td>
<td>Reserved</td>
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</tr>
<tr>
<td>IP4[17:16]</td>
<td>DU0_DR6</td>
<td>Reserved</td>
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<td>-</td>
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<td>-</td>
</tr>
<tr>
<td>IP4[19:18]</td>
<td>DU0_DR7</td>
<td>Reserved</td>
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</tr>
<tr>
<td>IP4[22:20]</td>
<td>DU0 DG0</td>
<td>Reserved</td>
<td>SCIF0_RXD_C</td>
<td>I2C3_SCL_D</td>
<td>Reserved</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP4[25:23]</td>
<td>DU0 DG1</td>
<td>Reserved</td>
<td>SCIF0_TXD_C</td>
<td>I2C3_SDA_D</td>
<td>Reserved</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP4[27:26]</td>
<td>DU0 DG2</td>
<td>Reserved</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP4[29:28]</td>
<td>DU0 DG3</td>
<td>Reserved</td>
<td>-</td>
<td>-</td>
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<td>Reserved</td>
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</tr>
</tbody>
</table>

**Legend:** - Setting prohibited
### 5.3.14 Peripheral Function Select Register 5 (IPSR5)

Function: IPSR5 selects the functions of the multiplexed LSI pins.

#### Bit Map

<table>
<thead>
<tr>
<th>Bit: 31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
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#### Bit: 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

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<td>R/W</td>
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</table>

#### Bit Initial Value R/W Description

<table>
<thead>
<tr>
<th>Bit</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31 to 0</td>
<td>H'0000 0000</td>
<td>R/W</td>
<td>The functions of the LSI pins are selected according to the table below.</td>
</tr>
</tbody>
</table>

**Note:** To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

#### Bit Name

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Function 1 (Set Value = H'0)</th>
<th>Function 2 (Set Value = H'1)</th>
<th>Function 3 (Set Value = H'2)</th>
<th>Function 4 (Set Value = H'3)</th>
<th>Function 5 (Set Value = H'4)</th>
<th>Function 6 (Set Value = H'5)</th>
<th>Others (Set Value = H'6 to H'F)</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPS[1:0]</td>
<td>DU0_DG5 Reserved</td>
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<td>IPS[3:2]</td>
<td>DU0_DG6 Reserved</td>
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<td>DU0_DG7 Reserved</td>
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</tr>
<tr>
<td>IPS[8:6]</td>
<td>DU0_DB0 Reserved</td>
<td>SCIFA4_RXD_C</td>
<td>I2C4_SCL_D</td>
<td>CAN0_RX_C</td>
<td>Reserved</td>
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<tr>
<td>IPS[11:9]</td>
<td>DU0_DB1 Reserved</td>
<td>SCIFA4_TXD_C</td>
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<td>CAN0_TX_C</td>
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<td>IPS[25:24]</td>
<td>DU0_DOTCLKIN Reserved</td>
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<td>IPS[31:30]</td>
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</table>

**Legend:** - Setting prohibited
### 5.3.15 Peripheral Function Select Register 6 (IPSR6)

Function: IPSR6 selects the functions of the multiplexed LSI pins.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31 to 0</td>
<td>H’0000 0000</td>
<td>R/W</td>
<td>The functions of the LSI pins are selected according to the table below.</td>
</tr>
</tbody>
</table>

**Notes:** To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Function 1 (Set Value = H'0)</th>
<th>Function 2 (Set Value = H'1)</th>
<th>Function 3 (Set Value = H'2)</th>
<th>Function 4 (Set Value = H'3)</th>
<th>Function 5 (Set Value = H'4)</th>
<th>Function 6 (Set Value = H'5)</th>
<th>Function 7 (Set Value = H'6)</th>
<th>Others (Set Value = H'7 to HF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>IP6[1:0] DUO_EXVSYNC_DUO_VSYNC</td>
<td>Reserved</td>
<td>Reserved</td>
<td>-</td>
<td>-</td>
<td>-</td>
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<tr>
<td>IP6[3:2] DUO_EXODDF_DUO_ODDF_DISP_CDE</td>
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<td>IP6[5:4] DUO_DISP</td>
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<td>IP6[7:6] DUO_CDE</td>
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<td>IP6[8] V10_CLK</td>
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<td>IP6[9] V10_DATA0_V10_B0</td>
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<td>IP6[10] V10_DATA1_V10_B1</td>
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<td>IP6[19:17] V10_CLKENB</td>
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<td>SCIFA5_RXD_C</td>
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<td>IP6[22:20] V10_FIELD</td>
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<td>SCIFA5_TXD_C</td>
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<td>I2C0_SCL_C</td>
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<td>SCIFA0_TXD_B</td>
<td>I2C0_SDA_C</td>
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<td>IP6[31:29] ETH_MDI0</td>
<td>V10_G0</td>
<td>MSIOF2_RXD_B</td>
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**Legend:** - Setting prohibited
5.3.16 Peripheral Function Select Register 7 (IPSR7)

Function: IPSR7 selects the functions of the multiplexed LSI pins.

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<tr>
<th>Bit Name</th>
<th>Function 1 (Set Value)</th>
<th>Function 2 (Set Value)</th>
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<th>Function 4 (Set Value)</th>
<th>Function 5 (Set Value)</th>
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<th>Function 7 (Set Value)</th>
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<tr>
<td></td>
<td>= H'0</td>
<td>= H'1</td>
<td>= H'2</td>
<td>= H'3</td>
<td>= H'4</td>
<td>= H'5</td>
<td>= H'6</td>
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<tr>
<td>IP7[2:0]</td>
<td>ETH_CRS_DV</td>
<td>VI0_G1</td>
<td>MISOF2_TXD_B</td>
<td>I2C5_SDA_D</td>
<td>AVB_TXD0</td>
<td>Reserved</td>
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<td></td>
<td></td>
<td>VI0_G2</td>
<td>MISOF2_SCK_B</td>
<td>CAN0_RX_B</td>
<td>AVB_TXD1</td>
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<td>VI0_G3</td>
<td>MISOF2_SYNC_B</td>
<td>CAN0_TX_B</td>
<td>AVB_TXD2</td>
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<td>VI0_G4</td>
<td>MISOF2_SS1_B</td>
<td>SCI4_RXD_D</td>
<td>AVB_TXD3</td>
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<td>VI0_G5</td>
<td>MISOF2_SS2_B</td>
<td>SCI4_TXD_D</td>
<td>AVB_TXD4</td>
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<td>VI0_G6</td>
<td>SCI2_SCK_C</td>
<td>AVB_TXD5</td>
<td>SSI_SCK5_B</td>
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<td></td>
<td>VI0_G7</td>
<td>SCI2_RXD_C</td>
<td>IIC0_SCL_D</td>
<td>AVB_TXD6</td>
<td>SSI_WS5_B</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VI0_R0</td>
<td>SCI2_TXD_C</td>
<td>IIC0_SDA_D</td>
<td>AVB_TXD7</td>
<td>SSI_SDATA5_B</td>
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<tr>
<td></td>
<td></td>
<td>VI0_R1</td>
<td>SCI3_SCK_C</td>
<td>AVB_TX_ER</td>
<td>SSI_SCK6_B</td>
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<td></td>
<td>VI0_R2</td>
<td>SCI3_TXD_B</td>
<td>I2C4_SCL_E</td>
<td>AVB_GTX_CLK</td>
<td>SSI_WS6_B</td>
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<td>SCIF0_RXD</td>
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<td>SCIF1_RXD</td>
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</table>

Legend: - Setting prohibited

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

The functions of the LSI pins are selected according to the table below.

<table>
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<tr>
<th>Bit Range</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31 to 0</td>
<td>H'0000 0000</td>
<td>R/W</td>
<td>The functions of the LSI pins are selected according to the table below.</td>
</tr>
</tbody>
</table>
### 5.3.17 Peripheral Function Select Register 8 (IPSR8)

Function: IPSR8 selects the functions of the multiplexed LSI pins.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31 to 0</td>
<td>H’0000 0000</td>
<td>R/W</td>
<td>The functions of the LSI pins are selected according to the table below.</td>
</tr>
</tbody>
</table>

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Function 1 (Set Value = H’0)</th>
<th>Function 2 (Set Value = H’1)</th>
<th>Function 3 (Set Value = H’2)</th>
<th>Function 4 (Set Value = H’3)</th>
<th>Function 5 (Set Value = H’4)</th>
<th>Function 6 (Set Value = H’5)</th>
<th>Function 7 (Set Value = H’6)</th>
<th>Function 8 (Set Value = H’7)</th>
</tr>
</thead>
<tbody>
<tr>
<td>IP8[2:0]</td>
<td>ETH_MDC V10_R3</td>
<td>SCIF3_TXD_B</td>
<td>I2C4_SDA_E</td>
<td>AVB_MDC</td>
<td>SSI_SDATA6_B</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>IP8[5:3]</td>
<td>HSCIF0_HRX V10_R4</td>
<td>I2C1_SCL_C</td>
<td>AUDIO_CLKA_B</td>
<td>AVB_MDI0</td>
<td>SSI_SCK78_B</td>
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<td></td>
</tr>
<tr>
<td>IP8[8:6]</td>
<td>HSCIF0_HTX V10_R5</td>
<td>I2C1_SDA_C</td>
<td>AUDIO_CLKB_B</td>
<td>AVB_LINK</td>
<td>SSI_WS78_B</td>
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</tr>
<tr>
<td>IP8[11:9]</td>
<td>HSCIF0_HCTS_N V10_R6</td>
<td>SCIF0_RXD_D</td>
<td>I2C0_SCL_E</td>
<td>AVB_MAGIC</td>
<td>SSI_SDATA7_B</td>
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</tr>
<tr>
<td>IP8[14:12]</td>
<td>HSCIF0_HRTS_N V10_R7</td>
<td>SCIF0_TXD_D</td>
<td>I2C0_SDA_E</td>
<td>AVB_PHY_INT</td>
<td>SSI_SDATA8_B</td>
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<tr>
<td>IP8[16:15]</td>
<td>HSCIF0_HSCK</td>
<td>SCIF_CLKB</td>
<td>AVB_CRS</td>
<td>AUDIO_CLKC_B</td>
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</tr>
<tr>
<td>IP8[19:17]</td>
<td>I2C0_SCL</td>
<td>SCIF0_RXD_C</td>
<td>PWM5</td>
<td>TCLK1_B</td>
<td>AVB_GTXREFCLK</td>
<td>CAN1_RX_D</td>
<td>TPUTO0_B</td>
<td>-</td>
</tr>
<tr>
<td>IP8[22:20]</td>
<td>I2C0_SDA</td>
<td>SCIF0_TXD_C</td>
<td>TPUT00</td>
<td>CAN_CLK</td>
<td>DVC_MUTE</td>
<td>CAN1_TX_D</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP8[25:23]</td>
<td>I2C1_SCL</td>
<td>SCIF4_RXD</td>
<td>PWM5_B</td>
<td>DU1_DRV</td>
<td>Reserved</td>
<td>Reserved</td>
<td>TPUT1_B</td>
<td>-</td>
</tr>
<tr>
<td>IP8[28:26]</td>
<td>I2C1_SDA</td>
<td>SCIF4_TXD</td>
<td>IRQ5</td>
<td>DU1_DRV</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>-</td>
</tr>
<tr>
<td>IP8[31:29]</td>
<td>MSIOF0_RXD</td>
<td>SCIF5_RXD</td>
<td>I2C2_SCL_C</td>
<td>DU1_DRV</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>-</td>
</tr>
</tbody>
</table>

Legend: - Setting prohibited
5.3.18 Peripheral Function Select Register 9 (IPSR9)

Function: IPSR9 selects the functions of the multiplexed LSI pins.

| Bit: 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 |
|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|
| Initial value: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |
| R/W: R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W |

| Bit: 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|
| Initial value: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |
| R/W: R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W |

<table>
<thead>
<tr>
<th>Bit</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31 to 0</td>
<td>H'0000 0000</td>
<td>R/W</td>
<td>The functions of the LSI pins are selected according to the table below.</td>
</tr>
</tbody>
</table>

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Function 1 (Set Value = H'0)</th>
<th>Function 2 (Set Value = H'1)</th>
<th>Function 3 (Set Value = H'2)</th>
<th>Function 4 (Set Value = H'3)</th>
<th>Function 5 (Set Value = H'4)</th>
<th>Function 6 (Set Value = H'5)</th>
<th>Function 7 (Set Value = H'6)</th>
<th>Function 8 (Set Value = H'7)</th>
</tr>
</thead>
<tbody>
<tr>
<td>IP9[2:0]</td>
<td>MSIOF0_TXD</td>
<td>SCIF5_TXD</td>
<td>I2C2_SDA_C</td>
<td>DU1_DR3</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>IP9[5:3]</td>
<td>MSIOF0_SCK</td>
<td>IRQ0</td>
<td>Reserved</td>
<td>DU1_DR4</td>
<td>Reserved</td>
<td>TPUTO1_C</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP9[8:6]</td>
<td>MSIOF0_SYNC</td>
<td>PWM1</td>
<td>Reserved</td>
<td>DU1_DR5</td>
<td>Reserved</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP9[11:9]</td>
<td>MSIOF0_SS1</td>
<td>SCIFA0_RXD</td>
<td>Reserved</td>
<td>DU1_DR6</td>
<td>Reserved</td>
<td>Reserved</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP9[14:12]</td>
<td>MSIOF0_SS2</td>
<td>SCIFA0_TXD</td>
<td>Reserved</td>
<td>DU1_DR7</td>
<td>Reserved</td>
<td>Reserved</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP9[16:15]</td>
<td>HSCIF1_HRX</td>
<td>I2C4_SCL</td>
<td>PWM6</td>
<td>DU1_DG0</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP9[18:17]</td>
<td>HSCIF1_HTX</td>
<td>I2C4_SDA</td>
<td>TPUTO1</td>
<td>DU1_DG1</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP9[21:19]</td>
<td>HSCIF1_HSCK</td>
<td>PWM2</td>
<td>Reserved</td>
<td>DU1_DG2</td>
<td>Reserved</td>
<td>Reserved</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP9[24:22]</td>
<td>HSCIF1_HCTS_N</td>
<td>SCIFA4_RXD</td>
<td>Reserved</td>
<td>DU1_DG3</td>
<td>SSI_SCK1_B</td>
<td>Reserved</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP9[27:25]</td>
<td>HSCIF1_HRTS_N</td>
<td>SCIFA4_TXD</td>
<td>Reserved</td>
<td>DU1_DG4</td>
<td>SSI_WS1_B</td>
<td>Reserved</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP9[30:28]</td>
<td>SCIF1_SCK</td>
<td>PWM3</td>
<td>TCLK2</td>
<td>DU1_DG5</td>
<td>SSI_SDATA1_B</td>
<td>Reserved</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

Legend: - Setting prohibited
5.3.19 Peripheral Function Select Register 10 (IPSR10)

Function: IPSR10 selects the functions of the multiplexed LSI pins.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31 to 0</td>
<td>H'0000 0000</td>
<td>R/W</td>
<td>The functions of the LSI pins are selected according to the table below.</td>
</tr>
</tbody>
</table>

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Function 1 (Set Value = H'0)</th>
<th>Function 2 (Set Value = H'1)</th>
<th>Function 3 (Set Value = H'2)</th>
<th>Function 4 (Set Value = H'3)</th>
<th>Function 5 (Set Value = H'4)</th>
<th>Function 6 (Set Value = H'5)</th>
<th>Function 7 (Set Value = H'6)</th>
<th>Function 8 (Set Value = H'7)</th>
</tr>
</thead>
<tbody>
<tr>
<td>IP10[2:0]</td>
<td>SCIF1_RXD I2C5_SCL DU1_DB6 SSI_SCK2_B</td>
<td>Reserved</td>
<td>Reserved</td>
<td>-</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IP10[5:3]</td>
<td>SCIF1_TXD I2C5_SDA DU1_DB7 SSI_WS2_B</td>
<td>Reserved</td>
<td>Reserved</td>
<td>-</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IP10[8:6]</td>
<td>SCIF2_RXD IIC0_SCL DU1_DB0 SSI_SDATA2_B</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IP10[11:9]</td>
<td>SCIF2_TXD IIC0_SDA DU1_DB1 SSI_SCK9_B</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IP10[14:12]</td>
<td>SCIF2_SCK IRQ1 DU1_DB2 SSI_WS9_B</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IP10[17:15]</td>
<td>SCIF3_SCK IRQ2 DU1_DB3 SSI_SDATA9_B</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IP10[20:18]</td>
<td>SCIF3_TXD I2C1_SCL_E DU1_DB4 AUDIO_CLKA_C SSI_SCK4_B</td>
<td>Reserved</td>
<td>Reserved</td>
<td>-</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IP10[23:21]</td>
<td>SCIF3_TXD I2C1_SDA_E DU1_DB5 AUDIO_CLKB_C SSI_WS4_B</td>
<td>Reserved</td>
<td>Reserved</td>
<td>-</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IP10[26:24]</td>
<td>I2C2_SCL SCIF5_RXD DU1_DB6 AUDIO_CLKC_C SSI_SDATA4_B</td>
<td>Reserved</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IP10[29:27]</td>
<td>I2C2_SDA SCIF5_TXD DU1_DB7 AUDIO_CLKOUT_C</td>
<td>Reserved</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IP10[31:30]</td>
<td>SSI_SCK5 SCIF3_SCK DU1_DOTCLKIN</td>
<td>Reserved</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend: - Setting prohibited
### 5.3.20 Peripheral Function Select Register 11 (IPSR11)

Function: IPSR11 selects the functions of the multiplexed LSI pins.

<table>
<thead>
<tr>
<th>Bit: 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16</th>
</tr>
</thead>
<tbody>
<tr>
<td>Initial value: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>R/W: R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit: 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Initial value: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>R/W: R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Function 1 (Set Value = H'0)</th>
<th>Function 2 (Set Value = H'1)</th>
<th>Function 3 (Set Value = H'2)</th>
<th>Function 4 (Set Value = H'3)</th>
<th>Function 5 (Set Value = H'4)</th>
<th>Function 6 (Set Value = H'5)</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IP11[2:0]</td>
<td>SSI_WS5 SCIFA3_RXD I2C3_SCL_C DU1_DOTCLKOUT0 Reserved</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>R/W</td>
<td>The functions of the LSI pins are selected according to the table below.</td>
</tr>
<tr>
<td>IP11[5:3]</td>
<td>SSI_DATA5 SCIFA3_TXD I2C3_SDA_C DU1_DOTCLKOUT1 Reserved</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>R/W</td>
<td>-</td>
</tr>
<tr>
<td>IP11[7:6]</td>
<td>SSI_SCK6 SCIFA1_SCK_B DU1_EXHSYNC_DU1_HSYNC</td>
<td>Reserved</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>R/W</td>
<td>-</td>
</tr>
<tr>
<td>IP11[10:8]</td>
<td>SSI_WS6 SCIFA1_RXD_B I2C4_SCL_C DU1_EXVSYNC_DU1_VSYNC Reserved</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>R/W</td>
<td>-</td>
</tr>
<tr>
<td>IP11[13:11]</td>
<td>SSI_DATA6 SCIFA1_TXD_B I2C4_SDA_C DU1_EXODDF_DU1_ODDF_DISP_DCE Reserved</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>R/W</td>
<td>-</td>
</tr>
<tr>
<td>IP11[15:14]</td>
<td>SSI_SCK78 SCIFA2_SCK_B I2C5_SDA_C DU1_DISP</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>R/W</td>
<td>-</td>
</tr>
<tr>
<td>IP11[17:16]</td>
<td>SSI_WS78 SCIFA2_RXD_B I2C5_SCL_C DU1_CDE</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>R/W</td>
<td>-</td>
</tr>
<tr>
<td>IP11[20:18]</td>
<td>SSI_DATA7 SCIFA2_TXD_B IRQ8 AUDIO_CLKA_D CAN_CLK_D Reserved</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>R/W</td>
<td>-</td>
</tr>
<tr>
<td>IP11[23:21]</td>
<td>SSI_SCK0129 MSIOF1_RXD_B SCI1_RXD_D Reserved</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>R/W</td>
<td>-</td>
</tr>
<tr>
<td>IP11[26:24]</td>
<td>SSI_WS0129 MSIOF1_TXD_B SCI1_TXD_D Reserved</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>R/W</td>
<td>-</td>
</tr>
<tr>
<td>IP11[29:27]</td>
<td>SSI_DATA0 MSIOF1_SCK_B PWM0_B Reserved</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>R/W</td>
<td>-</td>
</tr>
</tbody>
</table>

Legend: - Setting prohibited

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.
### 5.3.21 Peripheral Function Select Register 12 (IPSR12)

Function: IPSR12 selects the functions of the multiplexed LSI pins.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31 to 0</td>
<td>H’0000 0000</td>
<td>R/W</td>
<td>The functions of the LSI pins are selected according to the table below.</td>
</tr>
</tbody>
</table>

**Note:** To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

#### Bit Name | Function 1 (Set Value = H’0) | Function 2 (Set Value = H’1) | Function 3 (Set Value = H’2) | Function 4 (Set Value = H’3) | Function 5 (Set Value = H’4) | Function 6 (Set Value = H’5) | Function 7 (Set Value = H’6) |
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>IP12[2:0]</td>
<td>SSI_SCK34</td>
<td>MSIOF1_SYNC_B</td>
<td>SCIFA1_SCK_C</td>
<td>Reserved</td>
<td>Reserved</td>
<td>DREQ1_N_B</td>
<td>-</td>
</tr>
<tr>
<td>IP12[5:3]</td>
<td>SSI_WS34</td>
<td>MSIOF1_SSI1_B</td>
<td>SCIFA1_RXD_C</td>
<td>Reserved</td>
<td>CAN1_RX_C</td>
<td>DACK1_B</td>
<td>-</td>
</tr>
<tr>
<td>IP12[8:6]</td>
<td>SSI_SDATA3</td>
<td>MSIOF1_SSI2_B</td>
<td>SCIFA1_TXD_C</td>
<td>Reserved</td>
<td>CAN1_TX_C</td>
<td>DREQ2_N</td>
<td>-</td>
</tr>
<tr>
<td>IP12[10:9]</td>
<td>SSI_SCK4</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP12[12:11]</td>
<td>SSI_WS4</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP12[14:13]</td>
<td>SSI_SDATA4</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP12[17:15]</td>
<td>SSI_SDATA8</td>
<td>SCIF1_SCK_B</td>
<td>PWM1_B</td>
<td>IRQ9</td>
<td>Reserved</td>
<td>DACK2</td>
<td>ETH_MDIO_B</td>
</tr>
<tr>
<td>IP12[20:18]</td>
<td>SSI_SCK1</td>
<td>SCIF1_RXD_B</td>
<td>IIC0_SCL_C</td>
<td>V11_CLK</td>
<td>CAN0_RX_D</td>
<td>Reserved</td>
<td>ETH_CRS_DV_B</td>
</tr>
<tr>
<td>IP12[23:21]</td>
<td>SSI_WS1</td>
<td>SCIF1_TXD_B</td>
<td>IIC0_SDA_C</td>
<td>V11_DATA0</td>
<td>CAN0_TX_D</td>
<td>Reserved</td>
<td>ETH_RX_ER_B</td>
</tr>
<tr>
<td>IP12[26:24]</td>
<td>SSI_SDATA1</td>
<td>HSCIF1_HRX_B</td>
<td>V11_DATA1</td>
<td>Reserved</td>
<td>ATAWR0_N</td>
<td>ETH_RXD0_B</td>
<td>-</td>
</tr>
<tr>
<td>IP12[29:27]</td>
<td>SSI_SCK2</td>
<td>HSCIF1_HTX_B</td>
<td>V11_DATA2</td>
<td>Reserved</td>
<td>ATAG0_N</td>
<td>ETH_RXD1_B</td>
<td>-</td>
</tr>
</tbody>
</table>

**Legend:** - Setting prohibited
5.3.22 Peripheral Function Select Register 13 (IPSR13)

Function: IPSR13 selects the functions of the multiplexed LSI pins.

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Function 1 (Set Value)</th>
<th>Function 2 (Set Value)</th>
<th>Function 3 (Set Value)</th>
<th>Function 4 (Set Value)</th>
<th>Function 5 (Set Value)</th>
<th>Function 6 (Set Value)</th>
<th>Function 7 (Set Value)</th>
<th>Function 8 (Set Value)</th>
</tr>
</thead>
<tbody>
<tr>
<td>IP13[2:0]</td>
<td>SSI_WS2</td>
<td>HSCIF1_HCTS_N</td>
<td>SCIFA0_RXD_D</td>
<td>VI1_DATA3</td>
<td>Reserved</td>
<td>ATACS00_N</td>
<td>ETH_LINK_B</td>
<td>-</td>
</tr>
<tr>
<td>IP13[5:3]</td>
<td>SSI_SDATA2</td>
<td>HSCIF1_HRTS_N</td>
<td>SCIFA0_TXD_D</td>
<td>VI1_DATA4</td>
<td>Reserved</td>
<td>ATACS10_N</td>
<td>ETH_REFCLK_B</td>
<td>-</td>
</tr>
<tr>
<td>IP13[8:6]</td>
<td>SSI_SCK9</td>
<td>SCIF2_SCK_B</td>
<td>SCIFA0_RXD_B</td>
<td>VI1_DATA5</td>
<td>Reserved</td>
<td>Ex_WAIT1</td>
<td>ETH_TXD1_B</td>
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</tr>
<tr>
<td>IP13[11:9]</td>
<td>SSI_WS9</td>
<td>SCIF2_RXD_B</td>
<td>I2C3_SCL_E</td>
<td>VI1_DATA6</td>
<td>ATARD0_N</td>
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<tr>
<td>IP13[14:12]</td>
<td>SSI_SDATA9</td>
<td>SCIF2_TXD_B</td>
<td>I2C3_SDA_E</td>
<td>VI1_DATA7</td>
<td>ATADIR0_N</td>
<td>ETH_MAGIC_B</td>
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</tr>
<tr>
<td>IP13[17:15]</td>
<td>AUDIO_CLKA</td>
<td>I2C0_SCL_B</td>
<td>SCIFA4_RXD_D</td>
<td>VI1_CLKENB</td>
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<td>Reserved</td>
<td>ETH_TXD0_B</td>
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</tr>
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<td>IP13[20:18]</td>
<td>AUDIO_CLKB</td>
<td>I2C0_SDA_B</td>
<td>SCIFA4_TXD_D</td>
<td>VI1_FIELD</td>
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<td>Reserved</td>
<td>Reserved</td>
<td>ETH_MDC_B</td>
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<tr>
<td>IP13[23:21]</td>
<td>AUDIO_CLKC</td>
<td>I2C4_SCL_B</td>
<td>SCIFA5_RXD_D</td>
<td>VI1_HSYNC_N</td>
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<td>IP13[26:24]</td>
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<td>I2C4_SDA_B</td>
<td>SCIFA5_TXD_D</td>
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</table>

Legend: - Setting prohibited

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.
Table 5.2 shows the correspondence between the function signals and the bit settings in the GPIO/peripheral function select registers and peripheral function selecting registers.

Table 5.2  Correspondence between Function Signals and Register Bit Settings

<table>
<thead>
<tr>
<th>GPIO (GP-Set-Value=-0)</th>
<th>Peripheral-Module (GP-Set-Value=-1)</th>
<th>Function-Selected-by-IP-Bits</th>
<th>GPIO/Peripheral-Function-Selecting-Bit</th>
<th>Peripheral-Function-Selecting-Bit</th>
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<tbody>
<tr>
<td>GP[0] D0</td>
<td>SCIFA3_SCK_B</td>
<td>IRQ4</td>
<td>GP[0]</td>
<td>IP[23:22]</td>
</tr>
<tr>
<td>GP[22] D22</td>
<td>SCIFB0_CTS_N</td>
<td>SCIF4_RXD_B</td>
<td>GP[22]</td>
<td>IP[31:30]</td>
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<tr>
<td>GP[27] D27</td>
<td>MSIFO1_SYNC</td>
<td>I2C0_SDA_B</td>
<td>GP[27]</td>
<td>IP[29:8]</td>
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<tr>
<td>GP[29] D29</td>
<td>MSIFO1_SSS2</td>
<td>SCIF4_TXD_B</td>
<td>GP[29]</td>
<td>IP[31:12]</td>
</tr>
<tr>
<td>GP[31] D31</td>
<td>MSIFO2_TXD</td>
<td>HSCIF0_HTX_B</td>
<td>GP[31]</td>
<td>IP[17:16]</td>
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<td>GP[33] D33</td>
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<td>IP[22:21]</td>
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<td>GP[34] D34</td>
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<td>SCIF4_RXD_B</td>
<td>GP[34]</td>
<td>IP[22:24]</td>
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<tr>
<td>GP[37] D37</td>
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<td>GP[37]</td>
<td>IP[31:30]</td>
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### Pin Function Controller (PFC)

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<thead>
<tr>
<th>GPIO (GP-Set-Value=0)</th>
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<th>GPIO/Peripheral Function-Selecting-Bit</th>
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<td>GP[16] IP[3][2]</td>
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<td>PWI1_C</td>
<td>TPUT05_C</td>
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<td>GP[22] IP[3][33]</td>
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<td>GP[23] EX_WAIT0</td>
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<td>SCIF_CLK</td>
<td>Reserved</td>
<td>GP[23] IP[3][4][31:1]</td>
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<td>I2C2_SCL_D</td>
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<td>I2C2_SDA_D</td>
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<td>I2C2_SCL_D</td>
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<td>I2C2_SCL_D</td>
<td>GP[29] IP[3][11:10]</td>
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<td>GP[31] IP[3][15:14]</td>
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<td>I2C2_SCL_D</td>
<td>GP[33] IP[3][19:18]</td>
</tr>
<tr>
<td>GP[34] DU0 DG0</td>
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<td>SCIF5_RXD_C</td>
<td>I2C3_SCL_D</td>
<td>GP[34] IP[3][22:20]</td>
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<tr>
<td>GP[37] DU0 DG3</td>
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<td>I2C3_SCL_D</td>
<td>GP[37] IP[3][29:28]</td>
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<td>I2C3_SCL_D</td>
<td>GP[38] IP[3][31:30]</td>
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<td>GP[40] DU0 DG6</td>
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<td>I2C3_SCL_D</td>
<td>GP[40] IP[3][35:33]</td>
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<td>GP[41] DU0 DG7</td>
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<td>GP[41] IP[3][37:35]</td>
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<td>GP[61] DU0 DB19</td>
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<td>GP[61] IP[3][43:37]</td>
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</table>
### Pin Function Controller (PFC)

<table>
<thead>
<tr>
<th>GPIO (GP-Set-Value=n)</th>
<th>Function-Selected-by-IP-Bits</th>
<th>GPIO/Peripheral-Function-Selecting-Bit</th>
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<tbody>
<tr>
<td></td>
<td>Function-1 (IP-Set-Value=n-0)</td>
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<td>Function-2 (IP-Set-Value=n-1)</td>
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<td>GP2[27]</td>
<td>DU0_EXHSYNC_</td>
<td>GP2[27] IP[5:31:30]</td>
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<td>DU0_ODDF_DIS Reserved</td>
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<td>GP2[29] IP[5:32:32]</td>
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<td>Function-3 (IP-Set-Value=n-2)</td>
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<td>GP2[31]</td>
<td>DU0_CDE Reserved</td>
<td>GP2[31] IP[5:36:36]</td>
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<td>GP3[0]</td>
<td>V0L_CLK AVB_RX_CLK</td>
<td>GP3[0] IP[5:38:38]</td>
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<td>GP3[12]</td>
<td>V0L_VSYNC_N SCIF0_TXD_B 12C0_SDA_C AUDIO_CLKOUT_B AVB_TX_EN - - - GP3[12] IP[5:54:54]</td>
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### 5. Pin Function Controller (PFC)

<table>
<thead>
<tr>
<th>GPIO</th>
<th>Peripheral-Module (GPIO-Set-Value=1)</th>
<th>Function-Selected-by-IP-Bits</th>
<th>GPIO/Peripheral-Function-Selecting-Bit</th>
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<tbody>
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<td>GP3[19]</td>
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<td>GP4[19]</td>
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<td>GP4[19]</td>
</tr>
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</table>

#### Table Notes:
- **GPIO Function-Selected-by-IP-Bits**: Each GPIO pin is associated with specific functions that can be selected through an IP bit. The table lists these functions for various GPIO pins.
- **Peripheral-Function-Selecting-Bit**: For each GPIO pin, the corresponding peripheral function is selected through a set of IP bits. These bits are crucial for configuring the GPIO pins to operate in different modes or interfaces.

---

**Example rows**:
- **GP3[19]**: The GPIO pin GP3[19] can be configured to select different functions, such as SCIF2_SCK, AVB_TXD5, SSI_SCK5_B, etc., through specific IP bits.
- **GP4[6]**: This GPIO pin can be configured to select functions like PWM3, TCLK2, DUT1_DG5, SSI_WS1_B, and others, depending on the IP bit settings.

---

**Further Details**:
- The table includes detailed entries for each GPIO pin, specifying which peripheral functions can be selected and the corresponding IP bit configurations.
- It's important to refer to the device's datasheet for comprehensive information on how to configure the GPIO pins for various applications.
## 5. Pin Function Controller (PFC)

<table>
<thead>
<tr>
<th>GPIO</th>
<th>Function-Selected-by-IP-Bits</th>
<th>GPIO/Peripheral-Function-Selecting-Bit</th>
<th>Peripheral-Module (GP-Set-Value=1)</th>
</tr>
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<tbody>
<tr>
<td>GP4[22]</td>
<td>I2C2_SCL</td>
<td>SCIF4_RXD</td>
<td>DU1_DB6</td>
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<td>GP4[23]</td>
<td>I2C2_SDA</td>
<td>SCIF5_TXD</td>
<td>DU1_DB7</td>
</tr>
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<td>GP4[26]</td>
<td>SSI_DATA5</td>
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### 5. Pin Function Controller (PFC)

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<td></td>
</tr>
<tr>
<td>GP5[14] SD1_CD</td>
<td>CAN0_RX</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>GP5[14] IP[0][0]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GP5[15] SD1_WP</td>
<td>IRQ7</td>
<td>CAN0_TX</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>GP5[15] IP[1][0]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GP5[16] MMC_CLK</td>
<td>SD2_CLK</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>GP5[16] IP[0][10]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GP5[17] MMC_CMD</td>
<td>SD2_CMD</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>GP5[17] IP[0][11]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GP5[18] MMC_D0</td>
<td>SD2_DATA0</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>GP5[18] IP[0][12]</td>
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<td></td>
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<tr>
<td>GP5[19] MMC_D1</td>
<td>SD2_DATA1</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>GP5[19] IP[0][13]</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>GP5[20] MMC_D2</td>
<td>SD2_DATA2</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>GP5[20] IP[0][14]</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>GP5[21] MMC_D3</td>
<td>SD2_DATA3</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>GP5[21] IP[0][15]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GP5[22] MMC_D4</td>
<td>SD2_CD</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>GP5[22] IP[0][16]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GP5[23] MMC_D5</td>
<td>SD2_WP</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>GP5[23] IP[0][17]</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:** - Setting prohibited
5.3.23 Module Select Register (MOD_SEL)

Function: MOD_SEL selects the group for multiple LSI pins with multiplexed pin functions.

Each input or input/output signal of the ADG, ADI, CAN, DR, I2C and AVB an is assigned to two or more groups of pins. Select one of these groups when using these signals. Do not use the module pins in the unselected group; if a module pin in the unselected group is used, correct operation is not guaranteed.

For some modules, however, although the output signals are assigned to two or more groups of pins, there is no bit for pins. Select one of these groups when using these signals. Do not use the module pins in the unselected group; if a module pin in the unselected group is used, correct operation is not guaranteed.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31 to 0</td>
<td>H'0000 0000</td>
<td>R/W</td>
<td>These bits select multiplexed pin functions as indicated in the table below.</td>
</tr>
</tbody>
</table>

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.
5. Pin Function Controller (PFC)

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Function 1 (Set Value = H0)</th>
<th>Function 2 (Set Value = H1)</th>
<th>Function 3 (Set Value = H2)</th>
<th>Function 4 (Set Value = H3)</th>
<th>Function 5 (Set Value = H4)</th>
</tr>
</thead>
<tbody>
<tr>
<td>sel_eth[0]</td>
<td>+ select pin ETH_CRS_DV for function ETH_CRS_DV + select pin ETH_LINK for function ETH_LINK + select pin ETH_MAGIC for function ETH_MAGIC + select pin ETH_MDC for function ETH_MDC + select pin ETH_MDIQ for function ETH_MDIQ + select pin ETH_REF_CLK for function ETH_REF_CLK + select pin ETH_RXD0 for function ETH_RXD0 + select pin ETH_RXD1 for function ETH_RXD1 + select pin ETH_RX_ER for function ETH_RX_ER + select pin ETH_TXD0 for function ETH_TXD0 + select pin ETH_TXD1 for function ETH_TXD1 + select pin ETH_TX_E for function ETH_TX_E</td>
<td>+ select pin AUDIO_CLKA for function ETH_TXD0_B + select pin AUDIO_CLKB for function ETH_TXD1_B + select pin SSI_SCK1 for function ETH_RXD0_B + select pin SSI_SCK9 for function ETH_MDIQ for function ETH_TXD0 for function ETH_TXD1 for function ETH_RXD1 for function ETH_TXD1 for function ETH_TX_E for function ETH_TX_E</td>
<td>+ select pin V0_VSYNC_N for function I2C0_SCL_C + select pin V0_VSYNC_N for function I2C0_SCL_B + select pin V0_SBI1 for function I2C0_SCL_B + select pin V0_SBI1 for function I2C0_SCL_B</td>
<td>+ select pin D5 for function I2C0_SCL_D + select pin D8 for function I2C0_SCL_D + select pin D11 for function I2C0_SCL_D + select pin D11 for function I2C0_SCL_D</td>
<td>+ select pin HSCIF0_HCTS_N for function I2C0_SCL_E + select pin HSCIF0_HCTS_N for function I2C0_SCL_E + select pin SCI3_TXD for function I2C0_SCL_E + select pin SCI3_TXD for function I2C0_SCL_E</td>
</tr>
<tr>
<td>sel_i2c0[2:0]</td>
<td>+ select pin I2C0_SCL for function I2C0_SCL + select pin I2C0_SDA for function I2C0_SDA</td>
<td>+ select pin AUDIO_CLKA for function I2C0_SCL + select pin AUDIO_CLKB for function I2C0_SDA</td>
<td>+ select pin D11 for function I2C1_SCL_C + select pin D11 for function I2C1_SCL_B + select pin D11 for function I2C1_SCL_B</td>
<td>+ select pin D5 for function I2C0_SCL_D + select pin D8 for function I2C0_SCL_D + select pin D11 for function I2C0_SCL_D + select pin D11 for function I2C0_SCL_D</td>
<td>+ select pin SCI3_TXD for function I2C0_SCL_E + select pin SCI3_TXD for function I2C0_SCL_E</td>
</tr>
<tr>
<td>sel_i2c1[2:0]</td>
<td>+ select pin I2C1_SCL for function I2C1_SCL + select pin I2C1_SDA for function I2C1_SDA</td>
<td>+ select pin D11 for function I2C1_SCL + select pin D11 for function I2C1_SCL + select pin D11 for function I2C1_SCL + select pin D11 for function I2C1_SCL</td>
<td>+ select pin SCI0_HRX for function I2C1_SCL + select pin SCI0_HRX for function I2C1_SCL + select pin SCI0_HRX for function I2C1_SCL + select pin SCI0_HRX for function I2C1_SCL</td>
<td>+ select pin D5 for function I2C0_SCL_D + select pin D8 for function I2C0_SCL_D + select pin D11 for function I2C0_SCL_D + select pin D11 for function I2C0_SCL_D</td>
<td>+ select pin SCI3_TXD for function I2C0_SCL_E + select pin SCI3_TXD for function I2C0_SCL_E</td>
</tr>
<tr>
<td>sel_i2c2[2:0]</td>
<td>+ select pin I2C2_SCL for function I2C2_SCL + select pin I2C2_SDA for function I2C2_SDA</td>
<td>+ select pin D11 for function I2C2_SCL + select pin D11 for function I2C2_SCL + select pin D11 for function I2C2_SCL + select pin D11 for function I2C2_SCL</td>
<td>+ select pin SCI0_HRX for function I2C1_SCL + select pin SCI0_HRX for function I2C1_SCL + select pin SCI0_HRX for function I2C1_SCL + select pin SCI0_HRX for function I2C1_SCL</td>
<td>+ select pin D5 for function I2C0_SCL_D + select pin D8 for function I2C0_SCL_D + select pin D11 for function I2C0_SCL_D + select pin D11 for function I2C0_SCL_D</td>
<td>+ select pin SCI3_TXD for function I2C0_SCL_E + select pin SCI3_TXD for function I2C0_SCL_E</td>
</tr>
<tr>
<td>sel_i2c3[2:0]</td>
<td>+ select pin I2C3_SCL for function I2C3_SCL + select pin I2C3_SDA for function I2C3_SDA</td>
<td>+ select pin D11 for function I2C3_SCL + select pin D11 for function I2C3_SCL + select pin D11 for function I2C3_SCL + select pin D11 for function I2C3_SCL</td>
<td>+ select pin SCI0_HRX for function I2C1_SCL + select pin SCI0_HRX for function I2C1_SCL + select pin SCI0_HRX for function I2C1_SCL + select pin SCI0_HRX for function I2C1_SCL</td>
<td>+ select pin D5 for function I2C0_SCL_D + select pin D8 for function I2C0_SCL_D + select pin D11 for function I2C0_SCL_D + select pin D11 for function I2C0_SCL_D</td>
<td>+ select pin SCI3_TXD for function I2C0_SCL_E + select pin SCI3_TXD for function I2C0_SCL_E</td>
</tr>
<tr>
<td>sel_i2c4[2:0]</td>
<td>+ select pin I2C4_SCL for function I2C4_SCL + select pin I2C4_SDA for function I2C4_SDA</td>
<td>+ select pin MSIO0_RXD for function I2C2_SCL + select pin MSIO0_RXD for function I2C2_SCL + select pin MSIO0_RXD for function I2C2_SCL + select pin MSIO0_RXD for function I2C2_SCL</td>
<td>+ select pin D11 for function I2C1_SCL + select pin D11 for function I2C1_SCL + select pin D11 for function I2C1_SCL + select pin D11 for function I2C1_SCL</td>
<td>+ select pin D5 for function I2C0_SCL_D + select pin D8 for function I2C0_SCL_D + select pin D11 for function I2C0_SCL_D + select pin D11 for function I2C0_SCL_D</td>
<td>+ select pin SCI3_TXD for function I2C0_SCL_E + select pin SCI3_TXD for function I2C0_SCL_E</td>
</tr>
<tr>
<td>sel_i2c5[1]</td>
<td>+ select pin I2C5_SCL for function I2C5_SCL + select pin I2C5_SDA for function I2C5_SDA</td>
<td>+ select pin D11 for function I2C1_SCL + select pin D11 for function I2C1_SCL + select pin D11 for function I2C1_SCL + select pin D11 for function I2C1_SCL</td>
<td>+ select pin D11 for function I2C1_SCL + select pin D11 for function I2C1_SCL + select pin D11 for function I2C1_SCL + select pin D11 for function I2C1_SCL</td>
<td>+ select pin D5 for function I2C0_SCL_D + select pin D8 for function I2C0_SCL_D + select pin D11 for function I2C0_SCL_D + select pin D11 for function I2C0_SCL_D</td>
<td>+ select pin SCI3_TXD for function I2C0_SCL_E + select pin SCI3_TXD for function I2C0_SCL_E</td>
</tr>
</tbody>
</table>

### Legend:
- Setting prohibited
## 5.3.24 Module Select Register 2 (MOD_SEL2)

Function: MOD_SEL2 selects the group for multiple LSI pins with multiplexed pin functions.

Each input or output signal of the IIC, LBS, MSI, RAD, SCIF, TMU, CAN and HSCIF is assigned to two or more groups of pins. Select one of these groups when using these signals. Do not use the module pins in the unselected group; if a module pin in the unselected group is used, correct operation is not guaranteed.

For some modules, however, although the output signals are assigned to two or more groups of pins, there is no bit for selecting the group. Select one of these pins for each output signal through the corresponding peripheral function select register. Also note that each pin can only be used in combination with the other input or output pins of the same group. When ssi8 and ssi7 (in MOD_SEL3 register) are to be used simultaneously, the values of sel_ssi8[0] and sel_ssi7[0] must be the same so that the selected pins belong to the same group. Correct operation is not guaranteed when a pin is used in combination with pins from other groups.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>H'0000 0000</td>
<td>R/W</td>
<td>These bits select multiplexed pin functions as indicated in the table below.</td>
</tr>
</tbody>
</table>

**Note:** To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

### Function 1 (Set Value = H'0)
- **sel_ic0[1:0]**
  - + select pin SCIF2_RXD for function IIC0_SCL + select pin SCIF2_TXD for function IIC0_SDA
- **sel_lbs[0]**
  - + select pin A14 for function DACK1
- **sel_msi[0]**
  - + select pin A10 for function MSIOF1_SCK + select pin A11 for function MSIOF1_SYNC + select pin A12 for function MSIOF1_SS2 + select pin A8 for function MSIOF1_RXD + select pin A9 for function MSIOF1_TXD

### Function 2 (Set Value = H'1)
- **sel_ic0[1:0]**
  - + select pin A10 for function IIC0_SCL_B + select pin A11 for function IIC0_SDA_B
- **sel_scif a4[1]**
  - + select pin A14 for function DACK1_B
- **sel_ssi8[0]**
  - + select pin SSI_SCK for function DACK1

### Function 3 (Set Value = H'2)
- **sel_scif a5[1]**
  - + select pin SSI_RS for function DACK1

### Function 4 (Set Value = H'3)
- **sel_can if0[0]**
  - + select pin SSI_RS for function DACK1

### Function 5 (Set Value = H'4)
- **sel_ssi8[0]**
  - + select pin SSI_RS for function DACK1

---

**Function 1 (Set Value = H'0)**
- **sel_ic0[1:0]**
- **sel_lbs[0]**
- **sel_msi[0]**

**Function 2 (Set Value = H'1)**
- **sel_scif a4[1]**
- **sel_ssi8[0]**

**Function 3 (Set Value = H'2)**
- **sel_scif a5[1]**

**Function 4 (Set Value = H'3)**
- **sel_can if0[0]**

**Function 5 (Set Value = H'4)**
- **sel_ssi8[0]**
### Pin Function Controller (PFC)

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Function 1</th>
<th>Function 2</th>
<th>Function 3</th>
<th>Function 4</th>
<th>Function 5</th>
</tr>
</thead>
<tbody>
<tr>
<td>sel_mua0[0]</td>
<td>+ select pin A14 for function MISOIF2_RXD + select pin A15 for function MISOIF2_TXD + select pin A16 for function MISOIF2_SCK + select pin A17 for function MISOIF2_SYNC + select pin A18 for function MISOIF2_SS1 + select pin A19 for function MISOIF2_SS2</td>
<td>+ select pin ETH_CRS_DV for function MISOIF2_TXD_B + select pin ETH_LINK for function MISOIF2_TXD_B + select pin ETH_MDI0 for function MISOIF2_TXD_B + select pin ETH_RXD0 for function MISOIF2_SYNC_B + select pin ETH_RXD1 for function MISOIF2_SS1_B + select pin ETH_RX_ER for function MISOIF2_SCK_B</td>
<td>+ select pin ADICLK for function ADICLK3_SAMP + select pin ADICLK5_SAMP for function ADICLK5_TXD</td>
<td>+ select pin DU0_DG0 for function ADICLK3_TXD_B + select pin DU0_DG1 for function SCIFA0_TXD_B + select pin DU0_DG2 for function SCIFA0_TXD_C</td>
<td>+ select pin SSI_SDATA2 for function SCIFA0_TXD_D + select pin SSI_WS2 for function SCIFA0_RXD_D</td>
</tr>
<tr>
<td>sel_rad0[0]</td>
<td>+ select pin ETH_CRS_DV for function ADICLK3_SAMP + select pin ADICLK5_SAMP for function ADICLK5_TXD</td>
<td>+ select pin SSI_SCK0129 for function ADIDATA_B + select pin SSI_SDATA34 for function ADICLK3_SAMP_B + select pin SSI_SDATA35 for function ADICLK5_SAMP_B</td>
<td>+ select pin SSI_SCK6 for function SCIFA1_SCK_B + select pin SSI_SDATA6 for function SCIFA1_TXD_B + select pin SSI_W86 for function SCIFA1_RXD_B + select pin SSI_WS34 for function SCIFA1_RXD_C</td>
<td>+ select pin SSI_SDATA2 + select pin SSI_WS2 for function SCIFA1_TXD_B + select pin SSI_WS34 for function SCIFA1_RXD_C</td>
<td>+ select pin SSI_SDATA2 + select pin SSI_WS2 for function SCIFA1_TXD_B + select pin SSI_WS34 for function SCIFA1_RXD_C</td>
</tr>
<tr>
<td>sel_scla0[1:0]</td>
<td>+ select pin A10 for function SCIFA0_RXD_B + select pin A11 for function SCIFA0_TXD</td>
<td>+ select pin SSI_SCK98 for function SCIFA0_RXD_B + select pin SSI_SDATA78 for function SCIFA0_TXD_B + select pin SSI_W88 for function SCIFA0_RXD_B</td>
<td>+ select pin D0 for function SCIFA3_SCK_B + select pin D1 for function SCIFA3_RXD_B + select pin D2 for function SCIFA3_TXD_B + select pin D3 for function SCIFA3_RXD_B</td>
<td>+ select pin SSI_SDATA2 for function SCIFA3_RXD_B + select pin SSI_WS2 for function SCIFA3_RXD_B + select pin SSI_WS34 for function SCIFA3_RXD_C</td>
<td>+ select pin SSI_SDATA2 for function SCIFA3_RXD_B + select pin SSI_WS2 for function SCIFA3_RXD_B + select pin SSI_WS34 for function SCIFA3_RXD_C</td>
</tr>
<tr>
<td>sel_scla2[0]</td>
<td>+ select pin A10 for function SCIFA2_RXD_B + select pin A11 for function SCIFA2_TXD</td>
<td>+ select pin SSI_SCK18 for function SCIFA2_RXD_B + select pin SSI_SDATA18 for function SCIFA2_TXD_B + select pin SSI_W88 for function SCIFA2_RXD_B</td>
<td>+ select pin D0 for function SCIFA3_SCK_B + select pin D1 for function SCIFA3_RXD_B + select pin D2 for function SCIFA3_TXD_B + select pin D3 for function SCIFA3_RXD_B</td>
<td>+ select pin SSI_SDATA2 for function SCIFA3_RXD_B + select pin SSI_WS2 for function SCIFA3_RXD_B + select pin SSI_WS34 for function SCIFA3_RXD_C</td>
<td>+ select pin SSI_SDATA2 for function SCIFA3_RXD_B + select pin SSI_WS2 for function SCIFA3_RXD_B + select pin SSI_WS34 for function SCIFA3_RXD_C</td>
</tr>
<tr>
<td>sel_scla3[0]</td>
<td>+ select pin SSI_SCK5 for function SCIFA1_SCK + select pin SSI_SDATA5 for function SCIFA1_TXD</td>
<td>+ select pin A10 for function SCIFA2_RXD_B + select pin A11 for function SCIFA2_TXD</td>
<td>+ select pin D0 for function SCIFA3_SCK_B + select pin D1 for function SCIFA3_RXD_B + select pin D2 for function SCIFA3_TXD_B + select pin D3 for function SCIFA3_RXD_B</td>
<td>+ select pin A10 for function SCIFA2_RXD_B + select pin A11 for function SCIFA2_TXD</td>
<td>+ select pin SSI_SDATA2 for function SCIFA3_RXD_B + select pin SSI_WS2 for function SCIFA3_RXD_B + select pin SSI_WS34 for function SCIFA3_RXD_C</td>
</tr>
<tr>
<td>sel_scla4[1:0]</td>
<td>+ select pin A10 for function SCIFA4_RXD_B + select pin A11 for function SCIFA4_TXD</td>
<td>+ select pin A10 for function SCIFA2_RXD_B + select pin A11 for function SCIFA2_TXD</td>
<td>+ select pin D0 for function SCIFA3_SCK_B + select pin D1 for function SCIFA3_RXD_B + select pin D2 for function SCIFA3_TXD_B + select pin D3 for function SCIFA3_RXD_B</td>
<td>+ select pin A10 for function SCIFA2_RXD_B + select pin A11 for function SCIFA2_TXD</td>
<td>+ select pin A10 for function SCIFA2_RXD_B + select pin A11 for function SCIFA2_TXD</td>
</tr>
<tr>
<td>sel_scla5[1:0]</td>
<td>+ select pin A10 for function SCIFA5_RXD_B + select pin A11 for function SCIFA5_TXD</td>
<td>+ select pin A10 for function SCIFA4_RXD_B + select pin A11 for function SCIFA4_TXD</td>
<td>+ select pin A10 for function SCIFA5_RXD_B + select pin A11 for function SCIFA5_TXD</td>
<td>+ select pin A10 for function SCIFA4_RXD_B + select pin A11 for function SCIFA4_TXD</td>
<td>+ select pin SSI_WS2 for function SCIFA5_RXD_B + select pin SSI_WS34 for function SCIFA5_RXD_C</td>
</tr>
<tr>
<td>sel_tmu0[0]</td>
<td>+ select pin D7 for function TCLK1 + select pin SSI1_SCK for function TCLK2</td>
<td>+ select pin D13 for function TCLK1 + select pin D8 for function TCLK2</td>
<td>+ select pin D13 for function TCLK1 + select pin D8 for function TCLK2</td>
<td>+ select pin D0 for function TCLK1 + select pin D8 for function TCLK2</td>
<td>+ select pin D0 for function TCLK1 + select pin D8 for function TCLK2</td>
</tr>
<tr>
<td>sel_can0[1:0]</td>
<td>+ select pin SD1 for function CAN0_RX + select pin SD1 for function CAN0_TX</td>
<td>+ select pin ETA_RXD0 for function CAN0_RX + select pin ETA_RXD0 for function CAN0_TX</td>
<td>+ select pin ETA_RXD0 for function CAN0_RX + select pin ETA_RXD0 for function CAN0_TX</td>
<td>+ select pin ETA_RXD0 for function CAN0_RX + select pin ETA_RXD0 for function CAN0_TX</td>
<td>+ select pin ETA_RXD0 for function CAN0_RX + select pin ETA_RXD0 for function CAN0_TX</td>
</tr>
<tr>
<td>sel_can1[1:0]</td>
<td>+ select pin MMC6_D6 for function CAN1_RX + select pin MMC6_D7 for function CAN1_TX</td>
<td>+ select pin ETA_RXD0 for function CAN1_RX + select pin ETA_RXD0 for function CAN1_TX</td>
<td>+ select pin ETA_RXD0 for function CAN1_RX + select pin ETA_RXD0 for function CAN1_TX</td>
<td>+ select pin ETA_RXD0 for function CAN1_RX + select pin ETA_RXD0 for function CAN1_TX</td>
<td>+ select pin ETA_RXD0 for function CAN1_RX + select pin ETA_RXD0 for function CAN1_TX</td>
</tr>
<tr>
<td>sel_hsci0[0]</td>
<td>+ select pin HSCI0_HRX for function HRX0 + select pin HSCI0_HSK0 for function HSK0</td>
<td>+ select pin ETA4 for function HSK0_B + select pin ETA15 for function HTX0</td>
<td>+ select pin ETA4 for function HSK0_B + select pin ETA15 for function HTX0</td>
<td>+ select pin ETA4 for function HSK0_B + select pin ETA15 for function HTX0</td>
<td>+ select pin ETA4 for function HSK0_B + select pin ETA15 for function HTX0</td>
</tr>
</tbody>
</table>
## 5. Pin Function Controller (PFC)

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Function 1 (Set Value = H'0)</th>
<th>Function 2 (Set Value = H'1)</th>
<th>Function 3 (Set Value = H'2)</th>
<th>Function 4 (Set Value = H'3)</th>
<th>Function 5 (Set Value = H'4)</th>
</tr>
</thead>
<tbody>
<tr>
<td>set_hscif1[0]</td>
<td>+ select pin HSCIF1_HCTS_N for function HCTS1_N + select pin HSCIF1_HRTS_N for function HRTS1_N + select pin HSCIF1_HRX for function HRX1 + select pin HSCIF1_HTX for function HTX1</td>
<td>+ select pin SSI_SCK2 for function HTX1_B + select pin SSI_SDATA1 for function HRTS1_N_B + select pin SSI_WS2 for function HCTS1_N_B</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend: – Setting prohibited
5.3.25 Module Select Register 3 (MOD_SEL3)

Function: MOD_SEL3 selects the group for multiple LSI pins with multiplexed pin functions.

Each input or output signal of the SCIF and SSI is assigned to two or more groups of pins. Select one of these groups when using these signals. Do not use the module pins in the unselected group; if a module pin in the unselected group is used, correct operation is not guaranteed.

For some modules, however, although the output signals are assigned to two or more groups of pins, there is no bit for selecting the group. Select one of these pins for each output signal through the corresponding peripheral function select register. Also note that each pin can only be used in combination with the other input or output pins of the same group. When ssi8 and ssi7 (in MOD_SEL3 register) are to be used simultaneously, the values of sel_ssi8[0] and sel_ssi7[0] must be the same so that the selected pins belong to the same group. Correct operation is not guaranteed when a pin is used in combinations with pins from other groups.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31 to 0</td>
<td>H’0000 0000</td>
<td>R/W</td>
<td>These bits select multiplexed pin functions as indicated in the table below.</td>
</tr>
</tbody>
</table>

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Function 1 (Set Value = H’0)</th>
<th>Function 2 (Set Value = H’1)</th>
<th>Function 3 (Set Value = H’2)</th>
<th>Function 4 (Set Value = H’3)</th>
<th>Function 5 (Set Value = H’4)</th>
</tr>
</thead>
<tbody>
<tr>
<td>sel_scf1[0:3]</td>
<td>+ select pin EX_WAIT0 for function SCIF1_CLK + select pin MMC_D6 for function SCIF0_RXD + select pin SCIF0_TXD + select pin SCIF0_SCK for function SCIF0_TXD</td>
<td>+ select pin HSCI0_HSCK for function SCIF1_CLK_B + select pin VIO_VSYNC_N for function SCIF0_RXD_B + select pin VIO_SSI_N for function SCIF0_TXD_B</td>
<td>+ select pin I2C0_SCL for function SCIF0_RXD_C + select pin I2C0_SDA for function SCIF0_TXD_C</td>
<td>+ select pin HSCI0_HCTS_N for function SCIF0_RXD_D + select pin HSCI0_HRTS_N for function SCIF0_TXD_D</td>
<td>+ select pin I2C0_SCL for function SCIF1_CLK_B + select pin VIO_SSI_N for function SCIF1_TXD_B</td>
</tr>
<tr>
<td>sel_scf1[1:0]</td>
<td>+ select pin SCI1_RXD for function SCIF1_RXD + select pin SCI1_SCK for function SCIF1_TXD + select pin SCI1_TXD for function SCIF1_TXD + select pin SCI1_SSI_W1 for function SCIF1_RXD_B</td>
<td>+ select pin SSI_SCK1 for function SCIF1_RXD_B + select pin SSI_SDATA_B for function SCIF1_RXD_B + select pin SSI_WS1 for function SCIF1_TXD_B</td>
<td>+ select pin D10 for function SCIF1_SCL_C + select pin D11 for function SCIF1_RD_C + select pin D12 for function SCIF1_RXD_C + select pin D13 for function SCIF1_TXD_C</td>
<td>+ select pin SCI1_SCL_C for function SCIF1_RXD_C + select pin SCI1_RTS_C for function SCIF1_TXD_C + select pin SCI1_RXD_C for function SCIF1_RXD_C + select pin SCI1_TXD_C for function SCIF1_TXD_C</td>
<td>+ select pin SCI1_SCL_C for function SCIF1_RXD_C + select pin SCI1_RTS_C for function SCIF1_TXD_C + select pin SCI1_RXD_C for function SCIF1_RXD_C + select pin SCI1_TXD_C for function SCIF1_TXD_C</td>
</tr>
<tr>
<td>sel_scf2[2:0]</td>
<td>+ select pin SCI2_RXD for function SCIF2_RXD + select pin SCI2_SCK for function SCIF2_TXD + select pin SCI2_TXD for function SCIF2_RXD + select pin SCI2_SSI_W9 for function SCIF2_RXD_B</td>
<td>+ select pin SSI_SCK9 for function SCIF2_RXD_B + select pin SSI_SDATA9 for function SCIF2_RXD_B + select pin SSI_WS9 for function SCIF2_TXD_B</td>
<td>+ select pin ETH_REF_CLK for function SCIF2_RXD_C + select pin ETH_TXD1 for function SCIF2_RXD_C + select pin ETH_TXD2 for function SCIF2_RXD_C + select pin ETH_TXD3 for function SCIF2_TXD_C</td>
<td>+ select pin SCI1_SCL_C for function SCIF1_RXD_C + select pin SCI1_RTS_C for function SCIF1_TXD_C + select pin SCI1_RXD_C for function SCIF1_RXD_C + select pin SCI1_TXD_C for function SCIF1_TXD_C</td>
<td>+ select pin SCI1_SCL_C for function SCIF1_RXD_C + select pin SCI1_RTS_C for function SCIF1_TXD_C + select pin SCI1_RXD_C for function SCIF1_RXD_C + select pin SCI1_TXD_C for function SCIF1_TXD_C</td>
</tr>
<tr>
<td>sel_scf3[0:0]</td>
<td>+ select pin SCI3_RXD for function SCIF3_RXD + select pin SCI3_SCK for function SCIF3_RXD + select pin SCI3_TXD for function SCIF3_RXD + select pin SCI3_SSI_W6 for function SCIF3_RXD_B</td>
<td>+ select pin ETH_MAGIC for function SCIF3_CLK_B + select pin ETH_MDC for function SCIF3_TXD_B + select pin ETH_TXD0 for function SCIF3_RXD_B</td>
<td>+ select pin ETHERNET_CLK for function SCIF3_CLK_B + select pin ETHERNET_MDC for function SCIF3_TXD_B + select pin ETHERNET_TXD0 for function SCIF3_RXD_B</td>
<td>+ select pin ETH_LINK for function SCIF3_RXD_C + select pin ETHERNET_TXD1 for function SCIF3_RXD_C + select pin ETHERNET_TXD2 for function SCIF3_RXD_C + select pin ETHERNET_TXD3 for function SCIF3_TXD_C</td>
<td>+ select pin A17 for function SCIF3_RXD_E + select pin A18 for function SCIF3_TXD_E</td>
</tr>
<tr>
<td>sel_scf4[2:0]</td>
<td>+ select pin SCI4_RXD for function SCIF4_RXD + select pin SCI4_SCK for function SCIF4_RXD + select pin SCI4_TXD for function SCIF4_RXD + select pin SCI4_SSI_W10 for function SCIF4_RXD_B</td>
<td>+ select pin D5 for function SCIF4_RXD_B + select pin D6 for function SCIF4_TXD_B</td>
<td>+ select pin EX_CS2_N for function SCIF4_RXD_C + select pin SCI4_RXD_C + select pin SCI4_RXD_D + select pin SCI4_TXD_C</td>
<td>+ select pin SCI4_SCL_C for function SCIF4_RXD_C + select pin SCI4_RTS_C for function SCIF4_TXD_C + select pin SCI4_RXD_C for function SCIF4_RXD_C + select pin SCI4_TXD_C for function SCIF4_TXD_C</td>
<td>+ select pin SCI4_SCL_C for function SCIF4_RXD_C + select pin SCI4_RTS_C for function SCIF4_TXD_C + select pin SCI4_RXD_C for function SCIF4_RXD_C + select pin SCI4_TXD_C for function SCIF4_TXD_C</td>
</tr>
</tbody>
</table>
## Pin Function Controller (PFC)

### Bit Name | Function 1 (Set Value = H'0) | Function 2 (Set Value = H'1) | Function 3 (Set Value = H'2) | Function 4 (Set Value = H'3) | Function 5 (Set Value = H'4)
---|---|---|---|---|---
**sel_sci0[0]** | + select pin M890_RXD for function SCIF5_RXD + select pin M890_TXD for function SCIF5_TXD | + select pin D3 for function SCIF5_RXD_B + select pin D4 for function SCIF5_TXD_B | + select pin DUD_DR0 for function SCIF5_RXD_C + select pin DUD_DR1 for function SCIF5_TXD_C | + select pin SSI_WS129 for function SCIF5_RXD_D + select pin SSI_WS129 for function SCIF5_TXD_D |  
**sel_sci1[0]** | + select pin SSI_SCK1 for function SSI_WS1 + select pin SSI_WS1 for function SSI_WS1 | + select pin HSCIF1_HCTS_N for function SSI_SCK1 + select pin HSCIF1_HCTS_N for function SSI_WS1 + select pin SCIF1_SCK for function SSI_WS1 |  
**sel_sci2[0]** | + select pin SSI_SCK2 for function SSI_WS2 + select pin SSI_WS2 for function SSI_WS2 | + select pin SCIF1_RXD for function SSI_SCK2 + select pin SCIF1_RXD for function SSI_WS2 + select pin SCIF2_RXD for function SSI_WS2 |  
**sel_sci4[0]** | + select pin SSI_SCK4 for function SSI_WS4 + select pin SSI_WS4 for function SSI_WS4 | + select pin I2C2_SCL for function SSI_SCK4 + select pin I2C2_SCL for function SSI_WS4 + select pin SCIF3_RXD for function SSI_WS4 |  
**sel_sci5[0]** | + select pin SSI_SCK5 for function SSI_WS5 + select pin SSI_WS5 for function SSI_WS5 | + select pin ETH_REF_CLK for function SSI_SCK5 + select pin ETH_REF_CLK for function SSI_WS5 + select pin ETH_TXD1 for function ETH_TXD0 for function SSI_WS5 |  
**sel_sci6[0]** | + select pin SSI_SCK6 for function SSI_WS6 + select pin SSI_WS6 for function SSI_WS6 | + select pin ETH_MAGIC for function SSI_SCK6 + select pin ETH_MAGIC for function SSI_WS6 + select pin ETH_TXD0 for function ETH_TXD0 for function SSI_WS6 |  
**sel_sci7[0]** | + select pin SSI_SCK7 for function SSI_WS7 + select pin SSI_WS7 for function SSI_WS7 | + select pin HSCIF0_HCTS_N for function SSI_SDATA7 + select pin HSCIF0_HCTS_N for function SSI_WS7 + select pin HSCIF0_HTX for function SSI_WS7 |  
**sel_sci8[0]** | + select pin SSI_SDATA8 for function SSI_SDATA8 + select pin SSI_SDATA8 for function SSI_SDATA8 | + select pin HSCIF0_HRTS_N for function SSI_SDATA8 + select pin HSCIF0_HRTS_N for function SSI_SDATA8 |  
**sel_sci9[0]** | + select pin SSI_WS9 for function SSI_WS9 + select pin SSI_WS9 for function SSI_WS9 | + select pin SCIF2_SCK for function SSI_WS9 + select pin SCIF2_SCK for function SSI_WS9 |  

Legend: - Setting prohibited
### 5.3.26 LSI Pin Pull-Up Control Register 0 (PUPR0)

Function: PUPR0 performs on/off control of the pull-up resistors.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
</table>
| 0   | PUPR0[31:0]  | H'5D60 FFFF   | R/W | Performs individual on/off control of the pull-up/down resistor provided in each signal pin of the LSI.  
 0: Pull-up/down function is disabled.  
 1: Pull-up/down function is enabled. |

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Set Value = 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>PUPR0[31]</td>
<td>A15 is pull up</td>
</tr>
<tr>
<td>PUPR0[30]</td>
<td>A14 is pull up</td>
</tr>
<tr>
<td>PUPR0[29]</td>
<td>A13 is pull up</td>
</tr>
<tr>
<td>PUPR0[28]</td>
<td>A12 is pull up</td>
</tr>
<tr>
<td>PUPR0[27]</td>
<td>A11 is pull up</td>
</tr>
<tr>
<td>PUPR0[26]</td>
<td>A10 is pull up</td>
</tr>
<tr>
<td>PUPR0[25]</td>
<td>A9 is pull up</td>
</tr>
<tr>
<td>PUPR0[24]</td>
<td>A8 is pull up</td>
</tr>
<tr>
<td>PUPR0[23]</td>
<td>A7 is pull up</td>
</tr>
<tr>
<td>PUPR0[22]</td>
<td>A6 is pull up</td>
</tr>
<tr>
<td>PUPR0[21]</td>
<td>A5 is pull up</td>
</tr>
<tr>
<td>PUPR0[20]</td>
<td>A4 is pull up</td>
</tr>
<tr>
<td>PUPR0[19]</td>
<td>A3 is pull up</td>
</tr>
<tr>
<td>PUPR0[18]</td>
<td>A2 is pull up</td>
</tr>
<tr>
<td>PUPR0[17]</td>
<td>A1 is pull up</td>
</tr>
<tr>
<td>PUPR0[16]</td>
<td>A0 is pull up</td>
</tr>
<tr>
<td>PUPR0[15]</td>
<td>D15 is pull up</td>
</tr>
<tr>
<td>PUPR0[14]</td>
<td>D14 is pull up</td>
</tr>
<tr>
<td>PUPR0[13]</td>
<td>D13 is pull up</td>
</tr>
<tr>
<td>PUPR0[12]</td>
<td>D12 is pull up</td>
</tr>
<tr>
<td>PUPR0[11]</td>
<td>D11 is pull up</td>
</tr>
<tr>
<td>PUPR0[10]</td>
<td>D10 is pull up</td>
</tr>
<tr>
<td>PUPR0[9]</td>
<td>D9 is pull up</td>
</tr>
<tr>
<td>PUPR0[8]</td>
<td>D8 is pull up</td>
</tr>
<tr>
<td>PUPR0[7]</td>
<td>D7 is pull up</td>
</tr>
<tr>
<td>Bit Name</td>
<td>Set Value</td>
</tr>
<tr>
<td>----------</td>
<td>-----------</td>
</tr>
<tr>
<td>PUPR0[6]</td>
<td>D6 is pull up</td>
</tr>
<tr>
<td>PUPR0[5]</td>
<td>D5 is pull up</td>
</tr>
<tr>
<td>PUPR0[4]</td>
<td>D4 is pull up</td>
</tr>
<tr>
<td>PUPR0[3]</td>
<td>D3 is pull up</td>
</tr>
<tr>
<td>PUPR0[2]</td>
<td>D2 is pull up</td>
</tr>
<tr>
<td>PUPR0[1]</td>
<td>D1 is pull up</td>
</tr>
<tr>
<td>PUPR0[0]</td>
<td>D0 is pull up</td>
</tr>
</tbody>
</table>
### 5.3.27 LSI Pin Pull-Up Control Register 1 (PUPR1)

Function: PUPR1 performs on/off control of the pull-up resistors.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>PUPR1[31:0]</td>
<td>H'7FD8 3FF3</td>
<td>R/W</td>
<td>Performs individual on/off control of the pull-up/down resistor provided in each signal pin of the LSI.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0: Pull-up/down function is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1: Pull-up/down function is enabled.</td>
</tr>
</tbody>
</table>

Bit Name | Set Value = 1
---|---
PUPR1[31] | -
PUPR1[30] | ACK is pull down
PUPR1[29] | EX_CS5_N is pull up
PUPR1[28] | EX_CS3_N is pull up
PUPR1[27] | EX_CS1_N is pull up
PUPR1[26] | CS1_N_A26 is pull up
PUPR1[25] | TDI is pull up
PUPR1[24] | TMS is pull up
PUPR1[23] | TCK is pull up
PUPR1[22] | TRST_N is pull up
PUPR1[21] | DACK0 is pull up
PUPR1[20] | DREQ0_N is pull up
PUPR1[19] | EX_WAIT0 is pull up
PUPR1[18] | WE1_N is pull up
PUPR1[17] | WE0_N is pull up
PUPR1[16] | RD_WR_N is pull up
PUPR1[15] | RD_N is pull up
PUPR1[14] | BS_N is pull up
PUPR1[13] | EX_CS4_N is pull up
PUPR1[12] | EX_CS2_N is pull up
PUPR1[11] | EX_CS0_N is pull up
PUPR1[10] | CS0_N is pull up
PUPR1[9]  | A25 is pull up
PUPR1[8]  | A24 is pull up
PUPR1[7]  | A23 is pull up
## Pin Function Controller (PFC)

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Set Value = 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>PUPR1[6]</td>
<td>A22 is pull up</td>
</tr>
<tr>
<td>PUPR1[5]</td>
<td>A21 is pull up</td>
</tr>
<tr>
<td>PUPR1[4]</td>
<td>A20 is pull up</td>
</tr>
<tr>
<td>PUPR1[3]</td>
<td>A19 is pull up</td>
</tr>
<tr>
<td>PUPR1[2]</td>
<td>A18 is pull up</td>
</tr>
<tr>
<td>PUPR1[1]</td>
<td>A17 is pull up</td>
</tr>
<tr>
<td>PUPR1[0]</td>
<td>A16 is pull up</td>
</tr>
</tbody>
</table>
### 5.3.28 LSI Pin Pull-Up Control Register 2 (PUPR2)

Function: PUPR2 performs on/off control of the pull-up resistors.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>PUPR2[31:0]</td>
<td>H'27FF FFFF</td>
<td>R/W</td>
<td>Performs individual on/off control of the pull-up/down resistor provided in each signal pin of the LSI.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0: Pull-up/down function is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1: Pull-up/down function is enabled.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Set Value = 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>PUPR2[31]</td>
<td>DU0_CDE is pull up</td>
</tr>
<tr>
<td>PUPR2[30]</td>
<td>DU0_DISP is pull up</td>
</tr>
<tr>
<td>PUPR2[29]</td>
<td>DU0_EXODDF_DU0_ODDF_DISP_CDE is pull up</td>
</tr>
<tr>
<td>PUPR2[28]</td>
<td>DU0_EXVSYNC_DU0_VSYNC is pull up</td>
</tr>
<tr>
<td>PUPR2[27]</td>
<td>DU0_EXHSYNC_DU0_HSYNC is pull up</td>
</tr>
<tr>
<td>PUPR2[26]</td>
<td>DU0_DOTCLKOUT1 is pull up</td>
</tr>
<tr>
<td>PUPR2[25]</td>
<td>DU0_DOTCLKOUT0 is pull up</td>
</tr>
<tr>
<td>PUPR2[24]</td>
<td>DU0_DOTCLKIN is pull up</td>
</tr>
<tr>
<td>PUPR2[23]</td>
<td>DU0_DB7 is pull up</td>
</tr>
<tr>
<td>PUPR2[22]</td>
<td>DU0_DB6 is pull up</td>
</tr>
<tr>
<td>PUPR2[21]</td>
<td>DU0_DB5 is pull up</td>
</tr>
<tr>
<td>PUPR2[20]</td>
<td>DU0_DB4 is pull up</td>
</tr>
<tr>
<td>PUPR2[19]</td>
<td>DU0_DB3 is pull up</td>
</tr>
<tr>
<td>PUPR2[18]</td>
<td>DU0_DB2 is pull up</td>
</tr>
<tr>
<td>PUPR2[17]</td>
<td>DU0_DB1 is pull up</td>
</tr>
<tr>
<td>PUPR2[16]</td>
<td>DU0_DB0 is pull up</td>
</tr>
<tr>
<td>PUPR2[15]</td>
<td>DU0 DG7 is pull up</td>
</tr>
<tr>
<td>PUPR2[14]</td>
<td>DU0 DG6 is pull up</td>
</tr>
<tr>
<td>PUPR2[13]</td>
<td>DU0 DG5 is pull up</td>
</tr>
<tr>
<td>PUPR2[12]</td>
<td>DU0 DG4 is pull up</td>
</tr>
<tr>
<td>PUPR2[11]</td>
<td>DU0 DG3 is pull up</td>
</tr>
<tr>
<td>PUPR2[10]</td>
<td>DU0 DG2 is pull up</td>
</tr>
<tr>
<td>PUPR2[9]</td>
<td>DU0 DG1 is pull up</td>
</tr>
<tr>
<td>PUPR2[8]</td>
<td>DU0 DG0 is pull up</td>
</tr>
<tr>
<td>PUPR2[7]</td>
<td>DU0 DR7 is pull up</td>
</tr>
</tbody>
</table>
Bit Name | Set Value = 1
---|---
PUPR2[6] | DU0_DR6 is pull up
PUPR2[5] | DU0_DR5 is pull up
PUPR2[4] | DU0_DR4 is pull up
PUPR2[3] | DU0_DR3 is pull up
PUPR2[2] | DU0_DR2 is pull up
PUPR2[1] | DU0_DR1 is pull up
PUPR2[0] | DU0_DR0 is pull up
# 5.3.29 LSI Pin Pull-Up Control Register 3 (PUPR3)

Function: PUPR3 performs on/off control of the pull-up resistors.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>PU{PR3[31:0]</td>
<td>H'FFFF FFFF</td>
<td>R/W</td>
<td>Performs individual on/off control of the pull-up/down resistor provided in each signal pin of the LSI.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0: Pull-up function is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1: Pull-up function is enabled.</td>
</tr>
</tbody>
</table>

**Bit Name**

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Set Value = 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>PU{PR3[31]</td>
<td>I2C1_SDA is pull up</td>
</tr>
<tr>
<td>PU{PR3[30]</td>
<td>I2C1_SCL is pull up</td>
</tr>
<tr>
<td>PU{PR3[29]</td>
<td>I2C0_SDA is pull up</td>
</tr>
<tr>
<td>PU{PR3[28]</td>
<td>I2C0_SCL is pull up</td>
</tr>
<tr>
<td>PU{PR3[27]</td>
<td>HSCIF0_HSCK is pull up</td>
</tr>
<tr>
<td>PU{PR3[26]</td>
<td>HSCIF0_HRTS_N is pull up</td>
</tr>
<tr>
<td>PU{PR3[25]</td>
<td>HSCIF0_HCTS_N is pull up</td>
</tr>
<tr>
<td>PU{PR3[24]</td>
<td>HSCIF0_HTX is pull up</td>
</tr>
<tr>
<td>PU{PR3[23]</td>
<td>HSCIF0_HRX is pull up</td>
</tr>
<tr>
<td>PU{PR3[22]</td>
<td>ETH_MDC is pull up</td>
</tr>
<tr>
<td>PU{PR3[21]</td>
<td>ETH_TXD0 is pull up</td>
</tr>
<tr>
<td>PU{PR3[20]</td>
<td>ETH_MAGIC is pull up</td>
</tr>
<tr>
<td>PU{PR3[19]</td>
<td>ETH_TX_EN is pull up</td>
</tr>
<tr>
<td>PU{PR3[18]</td>
<td>ETH_TXD1 is pull up</td>
</tr>
<tr>
<td>PU{PR3[17]</td>
<td>ETH_REF_CLK is pull up</td>
</tr>
<tr>
<td>PU{PR3[16]</td>
<td>ETH_LINK is pull up</td>
</tr>
<tr>
<td>PU{PR3[15]</td>
<td>ETH_RXD1 is pull up</td>
</tr>
<tr>
<td>PU{PR3[14]</td>
<td>ETH_RXD0 is pull up</td>
</tr>
<tr>
<td>PU{PR3[13]</td>
<td>ETH_RX_ER is pull up</td>
</tr>
<tr>
<td>PU{PR3[12]</td>
<td>ETH_CRS_DV is pull up</td>
</tr>
<tr>
<td>PU{PR3[11]</td>
<td>ETH_MDIO is pull up</td>
</tr>
<tr>
<td>PU{PR3[10]</td>
<td>VI0_VSYNC_N is pull up</td>
</tr>
<tr>
<td>PU{PR3[ 9]</td>
<td>VI0_HSYNC_N is pull up</td>
</tr>
<tr>
<td>PU{PR3[ 8]</td>
<td>VI0_FIELD is pull up</td>
</tr>
<tr>
<td>PU{PR3[ 7]</td>
<td>VI0_CLKENB is pull up</td>
</tr>
</tbody>
</table>
### Pin Function Controller (PFC)

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Set Value = 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>PUPR3[6]</td>
<td>VI0_DATA7_VI0_B7 is pull up</td>
</tr>
<tr>
<td>PUPR3[5]</td>
<td>VI0_DATA6_VI0_B6 is pull up</td>
</tr>
<tr>
<td>PUPR3[4]</td>
<td>VI0_DATA5_VI0_B5 is pull up</td>
</tr>
<tr>
<td>PUPR3[3]</td>
<td>VI0_DATA4_VI0_B4 is pull up</td>
</tr>
<tr>
<td>PUPR3[2]</td>
<td>VI0_DATA3_VI0_B3 is pull up</td>
</tr>
<tr>
<td>PUPR3[1]</td>
<td>VI0_DATA2_VI0_B2 is pull up</td>
</tr>
<tr>
<td>PUPR3[0]</td>
<td>VI0_DATA1_VI0_B1 is pull up</td>
</tr>
</tbody>
</table>
### 5.3.30 LSI Pin Pull-Up Control Register 4 (PUPR4)

Function: PUPR4 performs on/off control of the pull-up resistors.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>PUPR4[31]</td>
<td>H'FFFF FFFF</td>
<td>R/W</td>
<td>Performs individual on/off control of the pull-up resistor provided in each signal pin of the LSI.</td>
</tr>
<tr>
<td>30</td>
<td></td>
<td></td>
<td></td>
<td>0: Pull-up function is disabled.</td>
</tr>
<tr>
<td>29</td>
<td></td>
<td></td>
<td></td>
<td>1: Pull-up function is enabled.</td>
</tr>
</tbody>
</table>

**Bit Name**

- PUPR4[31]: SSI_SCK0129 is pull up
- PUPR4[30]: SSI_SDATA7 is pull up
- PUPR4[29]: SSI_WS78 is pull up
- PUPR4[28]: SSI_SCK78 is pull up
- PUPR4[27]: SSI_SDATA6 is pull up
- PUPR4[26]: SSI_WS6 is pull up
- PUPR4[25]: SSI_SCK6 is pull up
- PUPR4[24]: SSI_SDATA5 is pull up
- PUPR4[23]: SSI_WS5 is pull up
- PUPR4[22]: SSI_SCK5 is pull up
- PUPR4[21]: I2C2_SDA is pull up
- PUPR4[20]: I2C2_SCL is pull up
- PUPR4[19]: SCIF3_TXD is pull up
- PUPR4[18]: SCIF3_RXD is pull up
- PUPR4[17]: SCIF3_SCK is pull up
- PUPR4[16]: SCIF2_SCK is pull up
- PUPR4[15]: SCIF2_TXD is pull up
- PUPR4[14]: SCIF2_RXD is pull up
- PUPR4[13]: SCIF1_TXD is pull up
- PUPR4[12]: SCIF1_RXD is pull up
- PUPR4[11]: SCIF1_SCK is pull up
- PUPR4[10]: HSCIF1_HRTS_N is pull up
- PUPR4[9]: HSCIF1_HCTS_N is pull up
- PUPR4[8]: HSCIF1_HSCK is pull up
- PUPR4[7]: HSCIF1_HTX is pull up

**Initial Value**

- R/W: R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W

---

R01UH0544EJ0100 Rev.1.00
Sep 30, 2016

Renesas Engineering Corporation
<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Set Value = 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>PUPR4[6]</td>
<td>HSCIF1_HRX is pull up</td>
</tr>
<tr>
<td>PUPR4[5]</td>
<td>MSIOF0_SS2 is pull up</td>
</tr>
<tr>
<td>PUPR4[4]</td>
<td>MSIOF0_SS1 is pull up</td>
</tr>
<tr>
<td>PUPR4[3]</td>
<td>MSIOF0_SYNC is pull up</td>
</tr>
<tr>
<td>PUPR4[2]</td>
<td>MSIOF0_SCK is pull up</td>
</tr>
<tr>
<td>PUPR4[1]</td>
<td>MSIOF0_TXD is pull up</td>
</tr>
<tr>
<td>PUPR4[0]</td>
<td>MSIOF0_RXD is pull up</td>
</tr>
</tbody>
</table>
## 5.3.31 LSI Pin Pull-Up Control Register 5 (PUPR5)

Function: PUPR5 performs on/off control of the pull-up resistors.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>PUPR5[31]</td>
<td>H'00FF FF1F</td>
<td>R/W</td>
<td>Performs individual on/off control of the pull-up resistor provided in each signal pin of the LSI.</td>
</tr>
<tr>
<td>30</td>
<td>-</td>
<td></td>
<td></td>
<td>0: Pull-up function is disabled.</td>
</tr>
<tr>
<td>29</td>
<td>-</td>
<td></td>
<td></td>
<td>1: Pull-up function is enabled.</td>
</tr>
</tbody>
</table>

### Bit Name

- PUPR5[31]
- PUPR5[30]
- PUPR5[29]
- PUPR5[28]
- PUPR5[27]
- PUPR5[26]
- PUPR5[25]
- PUPR5[24]
- PUPR5[23]
- PUPR5[22]
- PUPR5[21]
- PUPR5[20]
- PUPR5[19]
- PUPR5[18]
- PUPR5[17]
- PUPR5[16]
- PUPR5[15]
- PUPR5[14]
- PUPR5[13]
- PUPR5[12]
- PUPR5[11]
- PUPR5[10]
- PUPR5[9]
- PUPR5[8]
- PUPR5[7]
- PUPR5[6]
- PUPR5[5]
- PUPR5[4]
- PUPR5[3]
- PUPR5[2]
- PUPR5[1]
- PUPR5[0]

- VI0_DATA0_VI0_B0 is pull up
- VI0_CLK is pull up
- AUDIO_CLKOUT is pull up
- AUDIO_CLKC is pull up
- AUDIO_CLKB is pull up
- AUDIO_CLKA is pull up
- SSI_SDATA9 is pull up
- SSI_WS9 is pull up
- SSI_SCK9 is pull up
- SSI_SDATA2 is pull up
- SSI_WS2 is pull up
- SSI_SCK2 is pull up
- SSI_SDATA1 is pull up
- SSI_WS1 is pull up
- SSI_SCK1 is pull up
- SSI_SDATA8 is pull up
- -
### Pin Function Controller (PFC)

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Set Value = 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>PUPR5[6]</td>
<td></td>
</tr>
<tr>
<td>PUPR5[5]</td>
<td></td>
</tr>
<tr>
<td>PUPR5[4]</td>
<td>SSI_SDATA3 is pull up</td>
</tr>
<tr>
<td>PUPR5[3]</td>
<td>SSI_WS34 is pull up</td>
</tr>
<tr>
<td>PUPR5[2]</td>
<td>SSI_SCK34 is pull up</td>
</tr>
<tr>
<td>PUPR5[1]</td>
<td>SSI_SDATA0 is pull up</td>
</tr>
<tr>
<td>PUPR5[0]</td>
<td>SSI_WS0129 is pull up</td>
</tr>
</tbody>
</table>
5.3.32 LSI Pin Pull-Up Control Register 6 (PUPR6)

Function: PUPR6 performs on/off control of the pull-up resistors.

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Set Value = 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>PUPR6[31]</td>
<td>-</td>
</tr>
<tr>
<td>PUPR6[30]</td>
<td>-</td>
</tr>
<tr>
<td>PUPR6[29]</td>
<td>-</td>
</tr>
<tr>
<td>PUPR6[28]</td>
<td>-</td>
</tr>
<tr>
<td>PUPR6[27]</td>
<td>-</td>
</tr>
<tr>
<td>PUPR6[26]</td>
<td>-</td>
</tr>
<tr>
<td>PUPR6[25]</td>
<td>-</td>
</tr>
<tr>
<td>PUPR6[24]</td>
<td>-</td>
</tr>
<tr>
<td>PUPR6[23]</td>
<td>MMC_D7 is pull up</td>
</tr>
<tr>
<td>PUPR6[22]</td>
<td>MMC_D6 is pull up</td>
</tr>
<tr>
<td>PUPR6[21]</td>
<td>MMC_D5 is pull up</td>
</tr>
<tr>
<td>PUPR6[20]</td>
<td>MMC_D4 is pull up</td>
</tr>
<tr>
<td>PUPR6[19]</td>
<td>MMC_D3 is pull up</td>
</tr>
<tr>
<td>PUPR6[18]</td>
<td>MMC_D2 is pull up</td>
</tr>
<tr>
<td>PUPR6[17]</td>
<td>MMC_D1 is pull up</td>
</tr>
<tr>
<td>PUPR6[16]</td>
<td>MMC_D0 is pull up</td>
</tr>
<tr>
<td>PUPR6[15]</td>
<td>MMC_CMD is pull up</td>
</tr>
<tr>
<td>PUPR6[14]</td>
<td>-</td>
</tr>
<tr>
<td>PUPR6[13]</td>
<td>SD1_WP is pull up</td>
</tr>
<tr>
<td>PUPR6[12]</td>
<td>SD1_CD is pull up</td>
</tr>
<tr>
<td>PUPR6[11]</td>
<td>SD1_DATA3 is pull up</td>
</tr>
<tr>
<td>PUPR6[10]</td>
<td>SD1_DATA2 is pull up</td>
</tr>
<tr>
<td>PUPR6[9]</td>
<td>SD1_DATA1 is pull up</td>
</tr>
<tr>
<td>PUPR6[8]</td>
<td>SD1_DATA0 is pull up</td>
</tr>
<tr>
<td>PUPR6[7]</td>
<td>SD1_CMD is pull up</td>
</tr>
</tbody>
</table>
### Pin Function Controller (PFC)

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Set Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>PUPR6[6]</td>
<td>SD0_WP is pull up</td>
</tr>
<tr>
<td>PUPR6[5]</td>
<td>SD0_CD is pull up</td>
</tr>
<tr>
<td>PUPR6[4]</td>
<td>SD0_DATA3 is pull up</td>
</tr>
<tr>
<td>PUPR6[3]</td>
<td>SD0_DATA2 is pull up</td>
</tr>
<tr>
<td>PUPR6[2]</td>
<td>SD0_DATA1 is pull up</td>
</tr>
<tr>
<td>PUPR6[1]</td>
<td>SD0_DATA0 is pull up</td>
</tr>
<tr>
<td>PUPR6[0]</td>
<td>SD0_CMD is pull up</td>
</tr>
</tbody>
</table>
### 5.3.33 SD Control Register 0 (IOCTRL0)

Function: IOCTRL0 controls the driving abilities of pins in use for the MMC and SD0 interfaces.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>drv2_mmcclock</td>
<td>1</td>
<td>R/W</td>
<td>MMC_CLK Setting.</td>
</tr>
<tr>
<td>30</td>
<td>drv1_mmcclock</td>
<td>1</td>
<td>R/W</td>
<td>The value of these bits must be 11.</td>
</tr>
<tr>
<td>29</td>
<td>drv2_mmccmd</td>
<td>1</td>
<td>R/W</td>
<td>MMC_CMD Setting.</td>
</tr>
<tr>
<td>28</td>
<td>drv1_mmccmd</td>
<td>1</td>
<td>R/W</td>
<td>The value of these bits must be 11.</td>
</tr>
<tr>
<td>27</td>
<td>drv2_mmcmd0</td>
<td>1</td>
<td>R/W</td>
<td>MMC_CD0 Setting.</td>
</tr>
<tr>
<td>26</td>
<td>drv1_mmcmd0</td>
<td>1</td>
<td>R/W</td>
<td>The value of these bits must be 11.</td>
</tr>
<tr>
<td>25</td>
<td>drv2_mmcmd1</td>
<td>1</td>
<td>R/W</td>
<td>MMC_CD1 Setting.</td>
</tr>
<tr>
<td>24</td>
<td>drv1_mmcmd1</td>
<td>1</td>
<td>R/W</td>
<td>The value of these bits must be 11.</td>
</tr>
<tr>
<td>23</td>
<td>drv2_mmcmd2</td>
<td>1</td>
<td>R/W</td>
<td>MMC_CD2 Setting.</td>
</tr>
<tr>
<td>22</td>
<td>drv1_mmcmd2</td>
<td>1</td>
<td>R/W</td>
<td>The value of these bits must be 11.</td>
</tr>
<tr>
<td>21</td>
<td>drv2_mmcmd3</td>
<td>1</td>
<td>R/W</td>
<td>MMC_CD3 Setting.</td>
</tr>
<tr>
<td>20</td>
<td>drv1_mmcmd3</td>
<td>1</td>
<td>R/W</td>
<td>The value of these bits must be 11.</td>
</tr>
<tr>
<td>19</td>
<td>drv2_mmcmd4</td>
<td>1</td>
<td>R/W</td>
<td>MMC_CD4 Setting.</td>
</tr>
<tr>
<td>18</td>
<td>drv1_mmcmd4</td>
<td>1</td>
<td>R/W</td>
<td>The value of these bits must be 11.</td>
</tr>
<tr>
<td>17</td>
<td>drv2_mmcmd5</td>
<td>1</td>
<td>R/W</td>
<td>MMC_CD5 Setting.</td>
</tr>
<tr>
<td>16</td>
<td>drv1_mmcmd5</td>
<td>1</td>
<td>R/W</td>
<td>The value of these bits must be 11.</td>
</tr>
<tr>
<td>15</td>
<td>drv2_mmcmd6</td>
<td>1</td>
<td>R/W</td>
<td>MMC_CD6 Setting.</td>
</tr>
<tr>
<td>14</td>
<td>drv1_mmcmd6</td>
<td>1</td>
<td>R/W</td>
<td>The value of these bits must be 11.</td>
</tr>
<tr>
<td>13</td>
<td>drv2_mmcmd7</td>
<td>1</td>
<td>R/W</td>
<td>MMC_CD7 Setting.</td>
</tr>
<tr>
<td>12</td>
<td>drv1_mmcmd7</td>
<td>1</td>
<td>R/W</td>
<td>The value of these bits must be 11.</td>
</tr>
<tr>
<td>11</td>
<td>drv2_sd0cmd</td>
<td>1</td>
<td>R/W</td>
<td>SD0_CD Setting.</td>
</tr>
<tr>
<td>10</td>
<td>drv1_sd0cmd</td>
<td>1</td>
<td>R/W</td>
<td>The value of these bits must be 11.</td>
</tr>
<tr>
<td>9</td>
<td>drv2_sd0clk</td>
<td>1</td>
<td>R/W</td>
<td>SD0_CLK Setting.</td>
</tr>
<tr>
<td>8</td>
<td>drv1_sd0clk</td>
<td>1</td>
<td>R/W</td>
<td>The value of these bits must be 11.</td>
</tr>
<tr>
<td>7</td>
<td>drv2_sd0cmd</td>
<td>1</td>
<td>R/W</td>
<td>SD0_CMD Setting.</td>
</tr>
<tr>
<td>6</td>
<td>drv1_sd0cmd</td>
<td>1</td>
<td>R/W</td>
<td>The value of these bits must be 11.</td>
</tr>
<tr>
<td>5</td>
<td>drv2_sd0dat0</td>
<td>1</td>
<td>R/W</td>
<td>SD0_DATA0 Setting.</td>
</tr>
<tr>
<td>4</td>
<td>drv1_sd0dat0</td>
<td>1</td>
<td>R/W</td>
<td>The value of these bits must be 11.</td>
</tr>
<tr>
<td>3</td>
<td>drv2_sd0dat1</td>
<td>1</td>
<td>R/W</td>
<td>SD0_DATA1 Setting.</td>
</tr>
<tr>
<td>2</td>
<td>drv1_sd0dat1</td>
<td>1</td>
<td>R/W</td>
<td>The value of these bits must be 11.</td>
</tr>
</tbody>
</table>
### Bit Bit Name Initial Value R/W Description

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>drv2_sd0data2</td>
<td>1</td>
<td>R/W</td>
<td>SD0_DATA2 Setting.</td>
</tr>
<tr>
<td>0</td>
<td>drv1_sd0data2</td>
<td>1</td>
<td>R/W</td>
<td>The value of these bits must be 11.</td>
</tr>
</tbody>
</table>

**Note:** To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.
### 5.3.34 SD Control Register 1 (IOCTRL1)

Function: IOCTRL1 controls the driving abilities of pins in use for the SD0 and SD1 interfaces.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>drv2_sd0data3</td>
<td>1</td>
<td>R/W</td>
<td>SD0_DATA3 Setting</td>
</tr>
<tr>
<td>30</td>
<td>drv1_sd0data3</td>
<td>1</td>
<td>R/W</td>
<td>SD0_WP Setting</td>
</tr>
<tr>
<td>29</td>
<td>drv2_sd0wp</td>
<td>1</td>
<td>R/W</td>
<td>The value of these bits must be 11.</td>
</tr>
<tr>
<td>28</td>
<td>drv1_sd0wp</td>
<td>1</td>
<td>R/W</td>
<td>The value of these bits must be 11.</td>
</tr>
<tr>
<td>27</td>
<td>drv2_sd1cmd</td>
<td>1</td>
<td>R/W</td>
<td>SD1_CMD Setting</td>
</tr>
<tr>
<td>26</td>
<td>drv1_sd1cmd</td>
<td>1</td>
<td>R/W</td>
<td>The value of these bits must be 11.</td>
</tr>
<tr>
<td>25</td>
<td>drv2_sd1clk</td>
<td>1</td>
<td>R/W</td>
<td>SD1_CLK Setting</td>
</tr>
<tr>
<td>24</td>
<td>drv1_sd1clk</td>
<td>1</td>
<td>R/W</td>
<td>The value of these bits must be 11.</td>
</tr>
<tr>
<td>23</td>
<td>drv2_sd1data0</td>
<td>1</td>
<td>R/W</td>
<td>SD1_DATA0 Setting</td>
</tr>
<tr>
<td>22</td>
<td>drv1_sd1data0</td>
<td>1</td>
<td>R/W</td>
<td>The value of these bits must be 11.</td>
</tr>
<tr>
<td>21</td>
<td>drv2_sd1data1</td>
<td>1</td>
<td>R/W</td>
<td>SD1_DATA1 Setting</td>
</tr>
<tr>
<td>20</td>
<td>drv1_sd1data1</td>
<td>1</td>
<td>R/W</td>
<td>The value of these bits must be 11.</td>
</tr>
<tr>
<td>19</td>
<td>drv2_sd1data2</td>
<td>1</td>
<td>R/W</td>
<td>SD1_DATA2 Setting</td>
</tr>
<tr>
<td>18</td>
<td>drv1_sd1data2</td>
<td>1</td>
<td>R/W</td>
<td>The value of these bits must be 11.</td>
</tr>
<tr>
<td>17</td>
<td>drv2_sd1data3</td>
<td>1</td>
<td>R/W</td>
<td>SD1_DATA3 Setting</td>
</tr>
<tr>
<td>16</td>
<td>drv1_sd1data3</td>
<td>1</td>
<td>R/W</td>
<td>The value of these bits must be 11.</td>
</tr>
<tr>
<td>15</td>
<td>drv2_sd1data3</td>
<td>1</td>
<td>R/W</td>
<td>SD1_WP Setting</td>
</tr>
<tr>
<td>14</td>
<td>drv1_sd1data3</td>
<td>1</td>
<td>R/W</td>
<td>The value of these bits must be 11.</td>
</tr>
<tr>
<td>13</td>
<td>drv2_sd1data1</td>
<td>1</td>
<td>R/W</td>
<td>The value of these bits must be 11.</td>
</tr>
</tbody>
</table>

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.
### 5.3.35 TDSEL Control Register (IOCTRL2)

Function: IOCTRL2 controls the delay of clock of pins in use for the IRQ, DU and Ethernet interfaces.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>tsd1_a10</td>
<td>0</td>
<td>R/W</td>
<td>A10 Setting.</td>
</tr>
<tr>
<td>30</td>
<td>tsd0_a10</td>
<td>0</td>
<td>R/W</td>
<td>The value of these bits must be 00.</td>
</tr>
<tr>
<td>29</td>
<td>tsd1_a16</td>
<td>0</td>
<td>R/W</td>
<td>A16 Setting.</td>
</tr>
<tr>
<td>28</td>
<td>tsd0_a16</td>
<td>0</td>
<td>R/W</td>
<td>The value of these bits must be 00.</td>
</tr>
<tr>
<td>27</td>
<td>tsd1_audclk2b</td>
<td>0</td>
<td>R/W</td>
<td>AUDIO_CLKB Setting.</td>
</tr>
<tr>
<td>26</td>
<td>tsd0_audclk2b</td>
<td>0</td>
<td>R/W</td>
<td>The value of these bits must be 00.</td>
</tr>
<tr>
<td>25</td>
<td>tsd1_ethrxer</td>
<td>0</td>
<td>R/W</td>
<td>ETH_RX_ER Setting.</td>
</tr>
<tr>
<td>24</td>
<td>tsd0_ethrxer</td>
<td>0</td>
<td>R/W</td>
<td>The value of these bits must be 00.</td>
</tr>
<tr>
<td>23</td>
<td>tsd1_excs3n</td>
<td>0</td>
<td>R/W</td>
<td>EX_CS3_N Setting.</td>
</tr>
<tr>
<td>22</td>
<td>tsd0_excs3n</td>
<td>0</td>
<td>R/W</td>
<td>The value of these bits must be 00.</td>
</tr>
<tr>
<td>21</td>
<td>tsd1_i2c1sda</td>
<td>0</td>
<td>R/W</td>
<td>I2C1_SDA Setting.</td>
</tr>
<tr>
<td>20</td>
<td>tsd0_i2c1sda</td>
<td>0</td>
<td>R/W</td>
<td>The value of these bits must be 00.</td>
</tr>
<tr>
<td>19</td>
<td>tsd1_mmcclk</td>
<td>0</td>
<td>R/W</td>
<td>MMC_CLK Setting.</td>
</tr>
<tr>
<td>18</td>
<td>tsd0_mmcclk</td>
<td>0</td>
<td>R/W</td>
<td>The value of these bits must be 00.</td>
</tr>
<tr>
<td>17</td>
<td>tsd1_msi0f0sck</td>
<td>0</td>
<td>R/W</td>
<td>MSI0F0_SCK Setting.</td>
</tr>
<tr>
<td>16</td>
<td>tsd0_msi0f0sck</td>
<td>0</td>
<td>R/W</td>
<td>The value of these bits must be 00.</td>
</tr>
<tr>
<td>15</td>
<td>tsd1_msi0f0sync</td>
<td>0</td>
<td>R/W</td>
<td>MSI0F0_SYNC Setting.</td>
</tr>
<tr>
<td>14</td>
<td>tsd0_msi0f0sync</td>
<td>0</td>
<td>R/W</td>
<td>The value of these bits must be 00.</td>
</tr>
<tr>
<td>13</td>
<td>tsd1_sd1clck</td>
<td>0</td>
<td>R/W</td>
<td>SD1_CLK Setting.</td>
</tr>
<tr>
<td>12</td>
<td>tsd0_sd0clck</td>
<td>0</td>
<td>R/W</td>
<td>The value of these bits must be 00.</td>
</tr>
<tr>
<td>11</td>
<td>tsd1_sd1clck</td>
<td>0</td>
<td>R/W</td>
<td>SD1_CLK Setting.</td>
</tr>
<tr>
<td>10</td>
<td>tsd0_sd1clck</td>
<td>0</td>
<td>R/W</td>
<td>The value of these bits must be 00.</td>
</tr>
<tr>
<td>9</td>
<td>tsd1_ssisdata0</td>
<td>0</td>
<td>R/W</td>
<td>SSI_SDATA0 Setting.</td>
</tr>
<tr>
<td>8</td>
<td>tsd0_ssisdata0</td>
<td>0</td>
<td>R/W</td>
<td>The value of these bits must be 00.</td>
</tr>
</tbody>
</table>

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.
### 5.3.36 POC Control Register (IOCTRL3)

Function: IOCTRL3 controls the IO voltage of pins in use for the SD interfaces.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>poc_mmcclk (sd2clk)</td>
<td>1</td>
<td>R/W</td>
<td>Selecting IO voltage for the SD2 H'00: 1.8 V (VCCQ_MMC_SD2 = 1.8 V) H'FF: 3.3 V (VCCQ_MMC_SD2 = 3.3 V) Other than above: Setting prohibited Note: H'00 can only be set for the SDHI SDR50/SDR104 mode and the GPIO multiplexed with the SDHI that can be used either 3.3 V or 1.8 V. Note that the MMC IO can only be used with 3.3 V.</td>
</tr>
<tr>
<td>30</td>
<td>poc_mmccmd (sd2cmd)</td>
<td>1</td>
<td>R/W</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>poc_mmcd0 (sd2data0)</td>
<td>1</td>
<td>R/W</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>poc_mmcd1 (sd2data1)</td>
<td>1</td>
<td>R/W</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>poc_mmcd2 (sd2data2)</td>
<td>1</td>
<td>R/W</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>poc_mmcd3 (sd2data3)</td>
<td>1</td>
<td>R/W</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>poc_mmcd4 (sd2cmd)</td>
<td>1</td>
<td>R/W</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>poc_mmcd5 (sd2wp)</td>
<td>1</td>
<td>R/W</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>poc_sd0cmd</td>
<td>1</td>
<td>R/W</td>
<td>Selecting IO voltage for the SD0 H'00: 1.8 V (VCCQ_SD0 = 1.8 V) H'FF: 3.3 V (VCCQ_SD0 = 3.3 V) Other than above: Setting prohibited Note: H'00 can only be set for the SDHI SDR50/SDR104 mode and the GPIO multiplexed with the SDHI that can be used either 3.3 V or 1.8 V.</td>
</tr>
<tr>
<td>22</td>
<td>poc_sd0clk</td>
<td>1</td>
<td>R/W</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>poc_sd0cmd</td>
<td>1</td>
<td>R/W</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>poc_sd0data0</td>
<td>1</td>
<td>R/W</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>poc_sd0data1</td>
<td>1</td>
<td>R/W</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>poc_sd0data2</td>
<td>1</td>
<td>R/W</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>poc_sd0data3</td>
<td>1</td>
<td>R/W</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>poc_sd0wp</td>
<td>1</td>
<td>R/W</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>poc_sd1cmd</td>
<td>1</td>
<td>R/W</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>poc_sd1clk</td>
<td>1</td>
<td>R/W</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>poc_sd1cmd</td>
<td>1</td>
<td>R/W</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>poc_sd1data0</td>
<td>1</td>
<td>R/W</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>poc_sd1data1</td>
<td>1</td>
<td>R/W</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>poc_sd1data2</td>
<td>1</td>
<td>R/W</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>poc_sd1data3</td>
<td>1</td>
<td>R/W</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>poc_sd1wp</td>
<td>1</td>
<td>R/W</td>
<td></td>
</tr>
</tbody>
</table>

Initial values: 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
### Pin Function Controller (PFC)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 to 0</td>
<td>—</td>
<td>All 0</td>
<td>R/W</td>
<td>—</td>
</tr>
</tbody>
</table>

**Notes:**
1. Any pin belongs to the same SD channel must be set to the same IO voltage as VCCQ_(MMC)_SDn. Even though setting different voltage for each pin of the same SD channel, it is impossible to change each pin voltage from the power supply voltage of the VCCQ_(MMC)_SDn.
2. When the VCCQ_(MMC)_SDn power supply voltage is 1.8-V to use the SDHI interface as SDR50/SDR104 mode or the GPIO (multiplexed with SDHI channel n pin) as 1.8-V IO, specify 1.8-V for IOCTRL6, then IO voltage of the SDHI channel n pins and multiplexed other function pins is all 1.8-V. In this condition, never input 3.3-V signal to these pins; if input 3.3-V signal, the LSI may be permanently damaged even though specifying the pin voltage to 3.3-V individually, furthermore, pull-up voltage of the unused pin which belongs to the same SD channel must be 1.8-V.
3. When the VCCQ_(MMC)_SDn power supply voltage is 3.3-V, to use the SDHI interface as default mode, high-speed mode or other module function, specify 3.3-V for IOCTRL3, then IO voltage of the SDHI channel n and multiplexed other function pins is all 3.3-V. In this condition, output level of the pin is 3.3-V and if the external device can only operate with 1.8-V, the external device may be permanently damaged even though specifying the pin voltage to 1.8-V individually.
4. For details of SDn related pin function settings, refer to following section. Section 5.3.8 GPSR 6, 5.3.9 IPSR 0 and 5.3.24 MOD_SEL2 (MMC_D[7:6]).
5. Some of the following module pins are multiplexed with the SDn pins.
   - INT, CAN0, CAN1, MMC, SCIF0, I2C2
     They cannot be used with 1.8-V power supply (VCCQ_(MMC)_SDn) except for the multiplexed GPIO. Use them with 3.3-V power supply and set the corresponding VCCQ_(MMC)_SDn supply voltage to 3.3-V by IOCTRL3.
     For details of multiplexed pins of MMC/SDn, refer to Table 4.1, List of Multiplexed Pin Functions in section 4, Pin Multiplexing.
6. To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.
5.3.37 IICDVFS and TDBG IO cell control register (IOCTRL7)

Function: IOCTRL7 controls the driving abilities of pins in use for the IIC and IICDVFS interfaces. This register is internal use and reserved; the value of this register should not be changed.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Initial Value</th>
<th>R/W</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31 to 13</td>
<td>—</td>
<td>All 0</td>
<td>R/W</td>
<td>—</td>
</tr>
<tr>
<td>12</td>
<td>gpreg_msel03_p[15]</td>
<td>0</td>
<td>R/W</td>
<td>Debug monitor function:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0: Use DU pins for debug monitor function.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1: Use SDHI pins for debug monitor function.</td>
</tr>
<tr>
<td>11 to 8</td>
<td>—</td>
<td>All 0</td>
<td>R/W</td>
<td>—</td>
</tr>
<tr>
<td>7</td>
<td>conta_iicdvfs</td>
<td>0</td>
<td>R/W</td>
<td>Control TOF value of IICDVFS IO cell (TOF: Output fall time from VIH min to VIL max OR from 0.7VPU to 0.3VPU )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0: 0.3VPU</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1: 0.7VPU</td>
</tr>
<tr>
<td>6</td>
<td>contb_iicdvfs</td>
<td>0</td>
<td>R/W</td>
<td>Control VIH/VIL value of IICDVFS IO cell (VIH: High level input voltage ; VIL: Low level input voltage )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0: VIL</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1: VIH</td>
</tr>
<tr>
<td>5 to 0</td>
<td>—</td>
<td>All 0</td>
<td>R/W</td>
<td>—</td>
</tr>
</tbody>
</table>

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.
5.4 Operation

5.4.1 Function Setting for Multiplexed Pins

Setting the LSI multiplexed pin setting mask register (PMMR) is necessary before setting each of the GPIO/peripheral function select registers 0 to 6 (GPSR0 to GPSR6) and peripheral function select registers 0 to 13 (IPSR0 to IPSR13). Specifically, the inverse of the value to be set in the select register must be written to the LSI multiplexed pin setting mask register. Otherwise, the GPIO/peripheral function select registers 0 to 6 (GPSR0 to GPSR6) and peripheral function select registers 0 to 13 (IPSR0 to IPSR13) cannot be set. IPSR0 to IPSR13, MOD_SEL, MOD_SEL2 and MOD_SEL3 registers shall be set before setting GPSR0 to GPSR6 registers in case that they need to be configured. MOD_SEL, MOD_SEL2 and MOD_SEL3 registers can be set either earlier or later than setting IPSR0 to IPSR13 registers.

1. Procedure for changing pin function from GPIO to peripheral function

![Diagram](image1)

Figure 5.1 Procedure for Changing Pin Function from GPIO to Peripheral Function

2. Procedure for changing pin function from peripheral function to GPIO

![Diagram](image2)

Figure 5.2 Procedure for Changing Pin Function from Peripheral function to GPIO
5.4.2 Setting Pull-Up/Down Resistors

The LSI pin pull-up control registers 0 to 6 (PUPR0 to PUPR6) are used to switch the pull-up/down resistors on and off.
Main Revisions and Additions in this Edition

Minor revisions such as corrections of errors in spelling and modifications of wording are not included in the revision history.

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Page</th>
<th>Contents</th>
<th>Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>—</td>
<td>First edition issued</td>
<td></td>
</tr>
</tbody>
</table>