# TK100E10NE

This material is for a technological examination material to aim at the product introduction. The change in the content of the characteristic might be accompanied at the final specification process. The latest specification will be able to be gotten in the brokerage department when the product of an equipment is designed and to get the confirmation.

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (U−MOSⅧ-H)

# TK100E10NE

## ■ E-Bike/UPS/Inverter

Note : This product is designed for E-Bike / UPS / Inverter in China / India market.

- Low drain−source on-resistance : $R_{DS(ON)}$ = 4.3 mΩ (typ.)
- Low leakage current : $I_{DSS}$ = 10 μA (max) ($V_{DS}$ = 100 V)
- Enhancement mode : $V_{th}$ = 2.0~4.0 V ($V_{DS}$ = 10 V, $I_D$ = 1 mA)

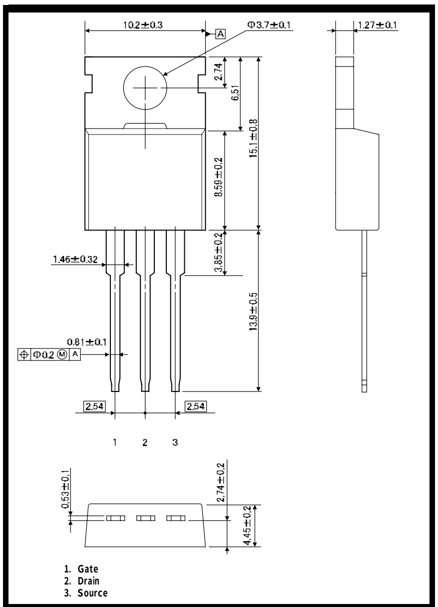
## Absolute Maximum Ratings (Ta = 25°C)

| Characteristics | | Symbol | Rating | Unit |
|---|---|---|---|---|
| Drain−source voltage | | $V_{DSS}$ | 100 | V |
| Drain−gate voltage ($R_{GS}$ = 20 kΩ) | | $V_{DGR}$ | 100 | V |
| Gate−source voltage | | $V_{GSS}$ | ±20 | V |
| Drain current | DC (Note 1) | $I_D$ | 100 | A |
| | DC (Note 1,4) | $I_D$ | 90 | A |
| | Pulse (Note 1) | $I_{DP}$ | 670 | A |
| Drain power dissipation (Tc = 25°C) | | $P_D$ | 230 | W |
| Single pulse avalanche energy (Note 2) | | $E_{AS}$ | 65 | mJ |
| Avalanche current | | $I_{AR}$ | 50 | A |
| Repetitive avalanche energy (Note 3) | | $E_{AR}$ | 23 | mJ |
| Peak diode recovery dv/dt (Note 5) | | dv/dt | 12 | V/ns |
| Channel temperature (Note 4) | | $T_{ch}$ | 175 | °C |
| Storage temperature range (Note 4) | | $T_{stg}$ | −55~175 | °C |

## Thermal Characteristics

| Characteristics | Symbol | Max | Unit |
|---|---|---|---|
| Thermal resistance, channel to case | $R_{th(ch-c)}$ | 0.65 | °C/W |
| Thermal resistance, channel to ambient | $R_{th(ch-a)}$ | 83.3 | °C/W |

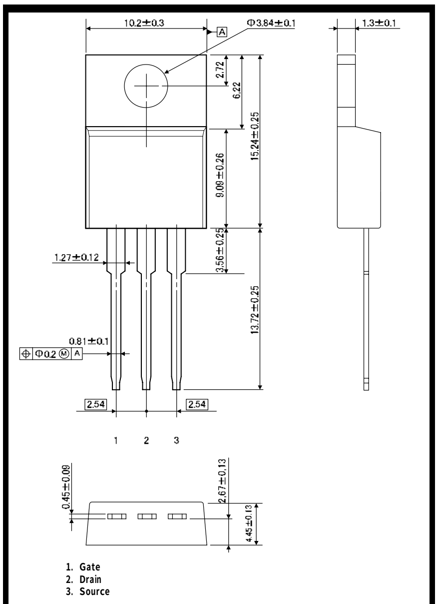
Unit: mm




| | |
|---|---|
| JEDEC | TO-220AB |
| JEITA | SC-46 |
| TOSHIBA | - |

Weight: 1.9 g (typ.)

Unit: mm




| | |
|---|---|
| JEDEC | TO-220AB |
| JEITA | SC-46 |
| TOSHIBA | - |

Weight: 1.9 g (typ.)

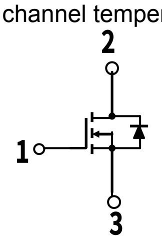
Note 1: Ensure that the channel temperature does not exceed 175°C.

Note 2: $V_{DD}$ = 25 V, $T_{ch}$ = 25°C (initial), L = 42 μH, $R_G$ = 25 Ω, $I_{AR}$ = 50A

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

Note 4: Tc = 100°C

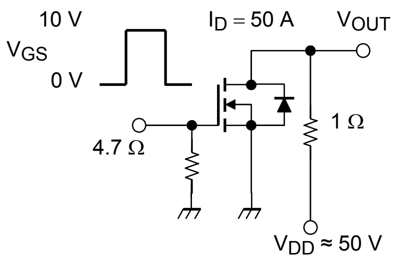
Note 5: $I_{DR}$≦80 A,di/dt≦160 A/μs, Tch≦Tch max.,
$V_{DS}$ peak < $V_{DSS}$




This transistor is an electrostatic-sensitive device.
Please handle with caution.

Note :Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).Thermal Characteristics

## Electrical Characteristics (Ta = 25°C)

| Characteristics | | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| Gate leakage current | | $I_{GSS}$ | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | — | — | ±0.1 | μA |
| Drain cut−off current | | $I_{DSS}$ | $V_{DS}$ = 100 V, $V_{DS}$ = 0 V | — | — | 10 | μA |
| Drain−source breakdown voltage | | $V_{(BR)\ DSS}$ | $I_D$ = 10 mA, $V_{GS}$ = 0 V | 100 | — | — | V |
| | | $V_{(BR)\ DSX}$ | $I_D$ = 10 mA, $V_{GS}$ = -20 V(Note 5) | 65 | — | — | V |
| Gate threshold voltage | | $V_{th}$ | $V_{DS}$ = 10 V, $I_D$ = 1 mA | 2.0 | — | 4.0 | V |
| Drain−source ON resistance | | $R_{DS\ (ON)}$ | $V_{GS}$ = 10 V, $I_D$ = 50 A | — | 4.3 | 5.1 | mΩ |
| Input capacitance | | $C_{iss}$ | $V_{DS}$ = 10 V, $V_{GS}$ = 0 V, f = 1 MHz | — | 5590 | — | pF |
| Reverse transfer capacitance | | $C_{rss}$ | | — | 350 | — | |
| Output capacitance | | $C_{oss}$ | | — | 2680 | — | |
| Switching time | Rise time | $t_r$ |   Duty ≤ 1%, $t_w$ = 10 μs | — | 18 | — | ns |
| | Turn−on time | $t_{on}$ | | — | 44 | — | |
| | Fall time | $t_f$ | | — | 27 | — | |
| | Turn−off time | $t_{off}$ | | — | 86 | — | |
| Total gate charge (Gate−source plus gate−drain) | | $Q_g$ | $V_{DD}$ ≈ 80 V, $V_{GS}$ = 10 V, $I_D$ = 100 A | — | 83 | — | nC |
| Gate−source charge | | $Q_{gs}$ | | — | 63 | — | |
| Gate−drain (“miller”) charge | | $Q_{gd}$ | | — | 20 | — | |

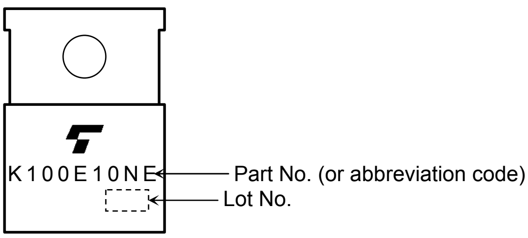
## Source−Drain Ratings and Characteristics (Ta = 25°C)

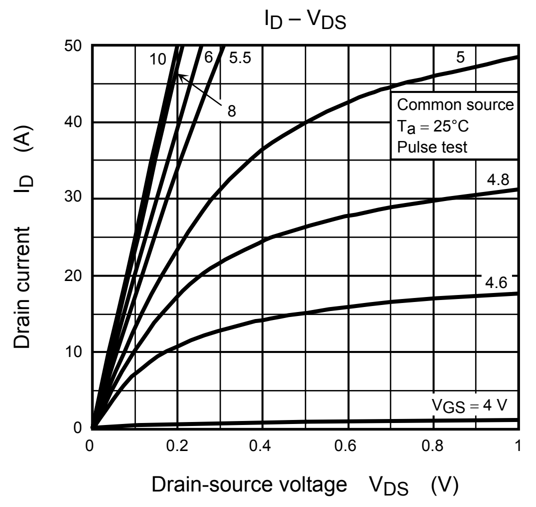
| Characteristics | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Continuous drain reverse current (Note 1) | $I_{DR}$ | — | — | — | 100 | A |
| Pulse drain reverse current (Note 1) | $I_{DRP}$ | — | — | — | 670 | A |
| Forward voltage (diode) | $V_{DSF}$ | $I_{DR}$ = 100 A, $V_{GS}$ = 0 V | — | — | −1.5 | V |
| Reverse recovery time(Note 6) | $t_{rr}$ | $I_{DR}$ = 100 A, $V_{GS}$ = 0 V<br>$dI_{DR}/dt$ = 50 A/μs | — | 88 | — | ns |
| Reverse recovery charge(Note 6) | $Q_{rr}$ | | — | 93 | — | nC |

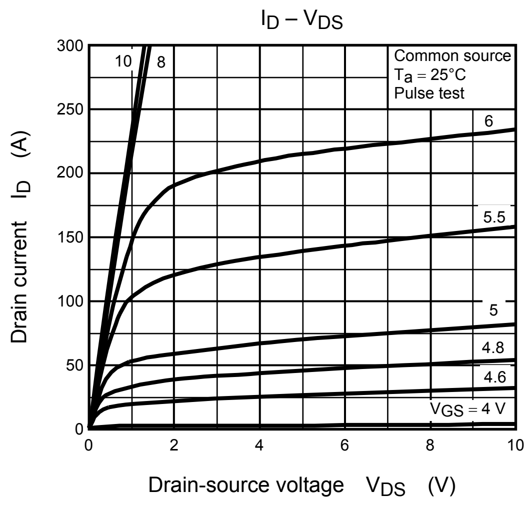
Note 5: If a reverse bias is applied between gate and source, this device enters $V_{(BR)DSX}$ mode.
Note that the drain-source breakdown voltage is lowered in this mode.

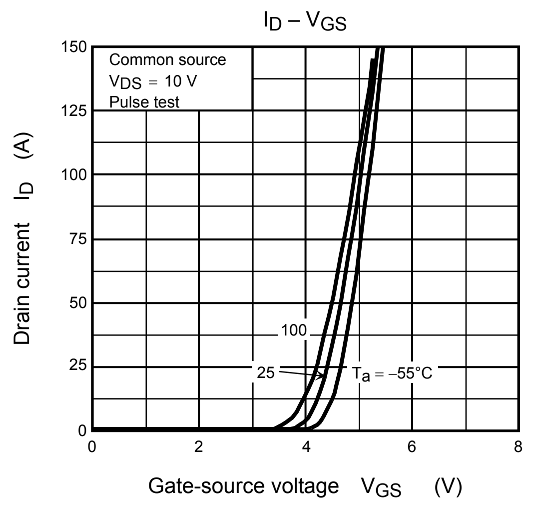
Note 6: Ensure that $V_{DS}$ peak does not exceed $V_{DSS}$.

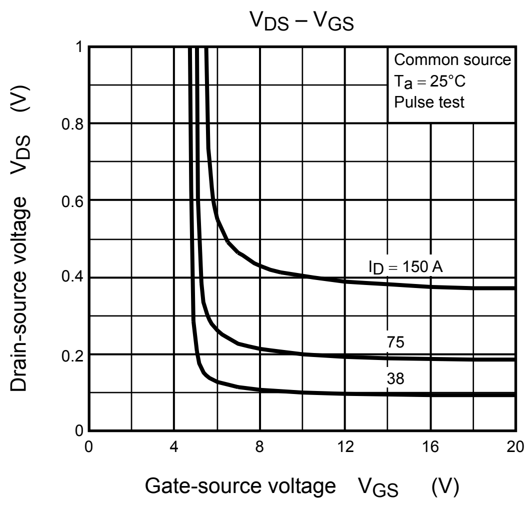
## Marking

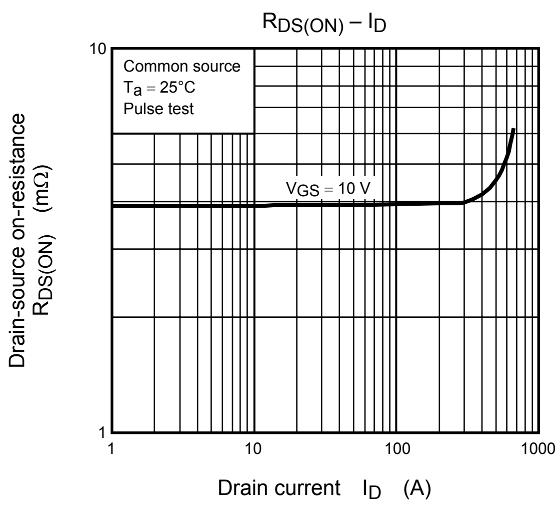


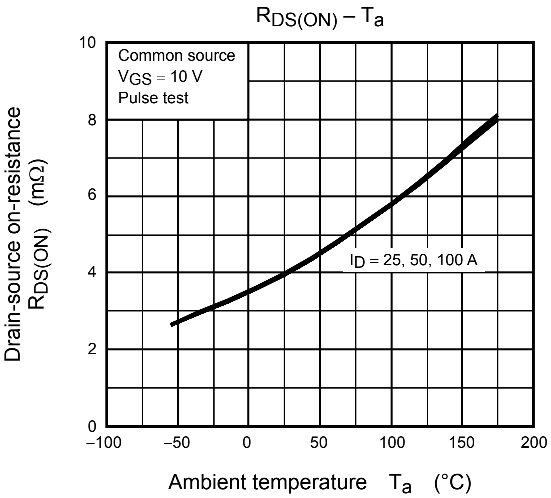

$I_D$ – $V_{DS}$
Common source
Ta = 25°C
Pulse test
10
6
5.5
8
5
4.8
4.6
VGS = 4 V
Drain current ID (A)
Drain-source voltage VDS (V)
0
10
20
30
40
50
0
0.2
0.4
0.6
0.8
1

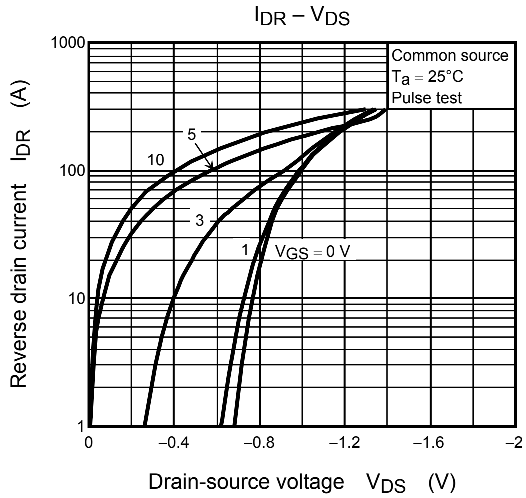

$I_D$ – $V_{DS}$
Common source
Ta = 25°C
Pulse test
10
8
6
5.5
5
4.8
4.6
VGS = 4 V
Drain current ID (A)
Drain-source voltage VDS (V)
0
50
100
150
200
250
300
0
2
4
6
8
10

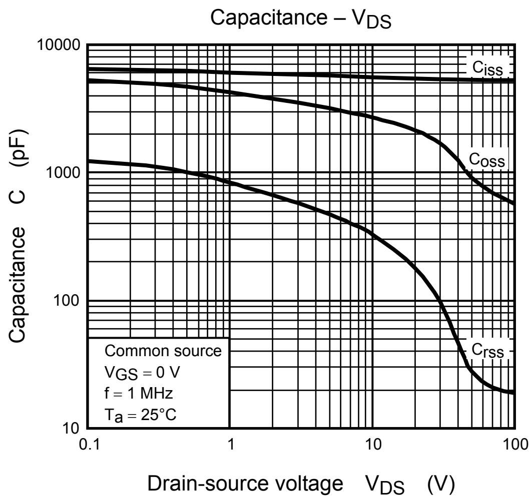

$I_D$ – $V_{GS}$
Common source
VDS = 10 V
Pulse test
100
25
Ta = −55°C
Drain current ID (A)
Gate-source voltage VGS (V)
0
25
50
75
100
125
150
0
2
4
6
8

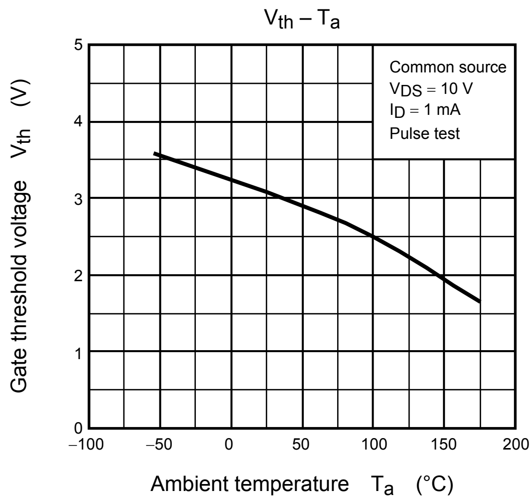

$V_{DS}$ – $V_{GS}$
Common source
Ta = 25°C
Pulse test
ID = 150 A
75
38
Drain-source voltage VDS (V)
Gate-source voltage VGS (V)
0
0.2
0.4
0.6
0.8
1
0
4
8
12
16
20

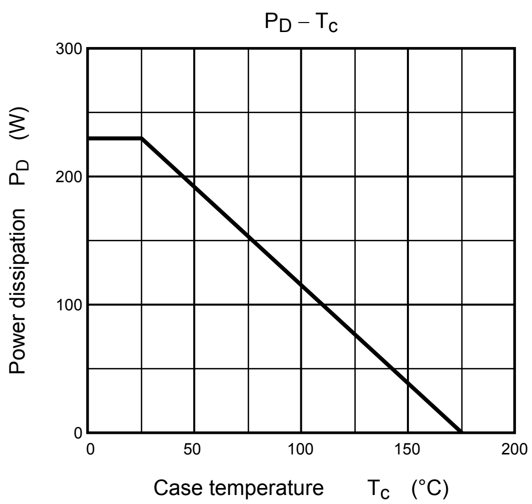

$R_{DS(ON)}$ – $I_D$
Common source
Ta = 25°C
Pulse test
VGS = 10 V
Drain-source on-resistance RDS(ON) (mΩ)
Drain current ID (A)
1
10
1
10
100
1000

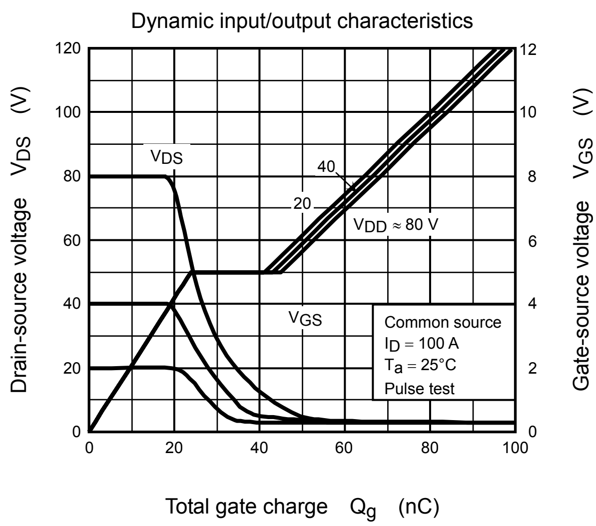

RDS(ON) – Ta
Common source
VGS = 10 V
Pulse test
ID = 25, 50, 100 A
Drain-source on-resistance RDS(ON) (mΩ)
10
8
6
4
2
0
–100
–50
0
50
100
150
200
Ambient temperature Ta (°C)

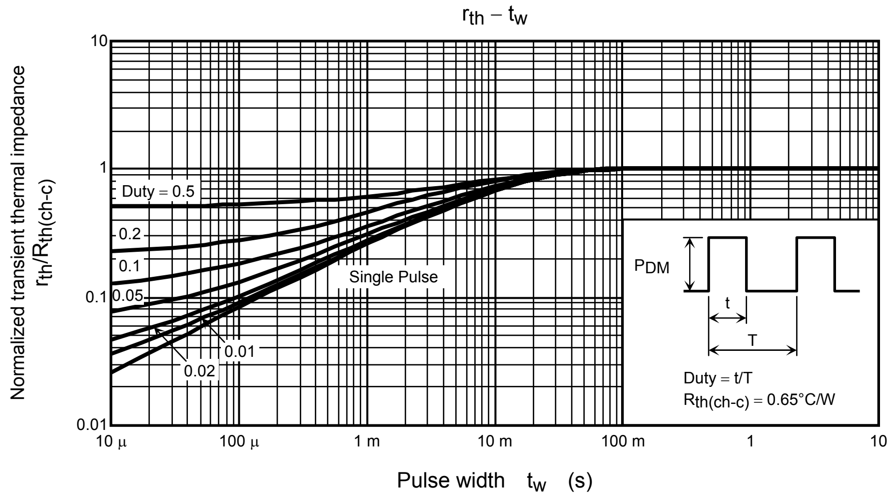

IDR – VDS
Common source
Ta = 25°C
Pulse test
10
5
3
1
VGS = 0 V
Reverse drain current IDR (A)
1000
100
10
1
0
–0.4
–0.8
–1.2
–1.6
–2
Drain-source voltage VDS (V)

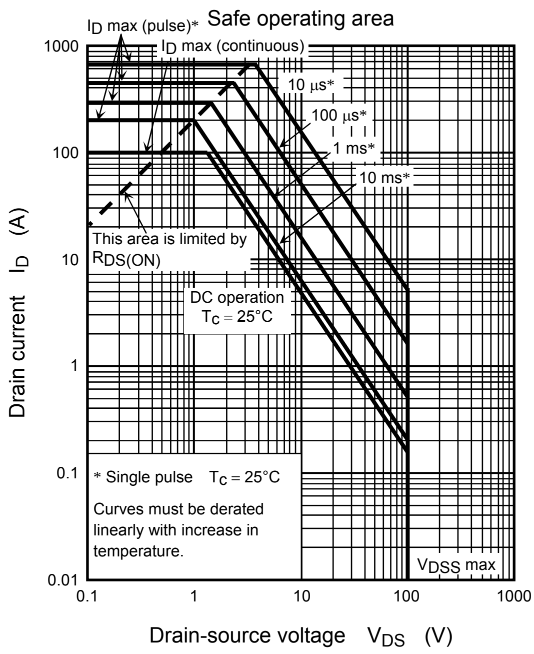

Capacitance – VDS
Ciss
Coss
Crss
Common source
VGS = 0 V
f = 1 MHz
Ta = 25°C
Capacitance C (pF)
10000
1000
100
10
0.1
1
10
100
Drain-source voltage VDS (V)

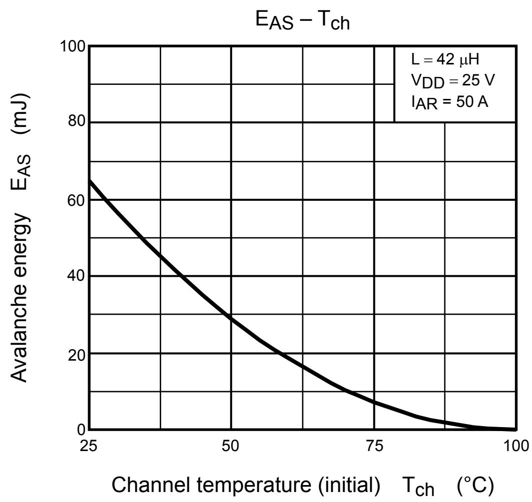

Vth – Ta
Common source
VDS = 10 V
ID = 1 mA
Pulse test
Gate threshold voltage Vth (V)
5
4
3
2
1
0
–100
–50
0
50
100
150
200
Ambient temperature Ta (°C)

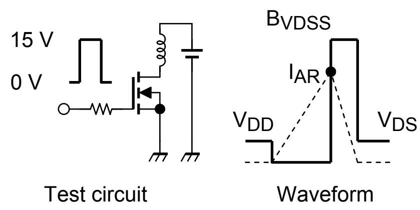

PD – Tc
Power dissipation PD (W)
300
200
100
0
0
50
100
150
200
Case temperature Tc (°C)


Dynamic input/output characteristics
VDS
40
20
VDD ≈ 80 V
VGS
Common source
ID = 100 A
Ta = 25°C
Pulse test
Drain-source voltage VDS (V)
120
100
80
60
40
20
0
Gate-source voltage VGS (V)
12
10
8
6
4
2
0
0
20
40
60
80
100
Total gate charge Qg (nC)




$R_G = 25\ \Omega$
$V_{DD} = 25$ V, $L = 42\ \mu$H

$$E_{AS} = \frac{1}{2} \cdot L \cdot I_{AR}^2 \cdot \left( \frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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