60V 2MHz Synchronous 4-Switch Buck-Boost Controller with Spread Spectrum

FEATURES

- **4-Switch Single Inductor Architecture Allows V_{IN} Above, Below or Equal to V_{OUT}**
- **Up to 95% Efficiency at 2MHz**
- **Proprietary Peak-Buck Peak-Boost Current Mode**
- **Wide V_{IN} Range: 4V to 60V**
- **±1.5% Output Voltage Accuracy: 1V ≤ V_{OUT} ≤ 60V**
- **±3% Input or Output Current Accuracy with Monitor**
- **Spread Spectrum Frequency Modulation for Low EMI**
- High Side PMOS Load Switch Driver
- No Top MOSFET Refresh Noise in Buck or Boost
- Adjustable and Synchronizable: 600kHz to 2MHz
- V_{OUT} Disconnected from V_{IN} During Shutdown
- Available in 28-Lead TSSOP with Exposed Pad and 28-Lead QFN (4mm × 5mm)

APPLICATIONS

- Automotive, Industrial, Telecom Systems
- High Frequency Battery-Powered System

DESCRIPTION

The LT®8390A is a synchronous 4-switch buck-boost DC/DC controller that regulates output voltage, input or output current from an input voltage above, below, or equal to the output voltage. The proprietary peak-buck peak-boost current mode control scheme allows adjustable and synchronizable 600kHz to 2MHz fixed frequency operation, or internal 25% triangle spread spectrum frequency modulation for low EMI. With a 4V to 60V input voltage range, 0V to 60V output voltage capability, and seamless low noise transitions between operation regions, the LT8390A is ideal for voltage regulator, battery and supercapacitor charger applications in automotive, industrial, telecom, and even battery-powered systems.

The LT8390A provides input or output current monitor and power good flag. Fault protection is also provided to detect output short-circuit condition, during which the LT8390A retries, latches off, or keeps running.

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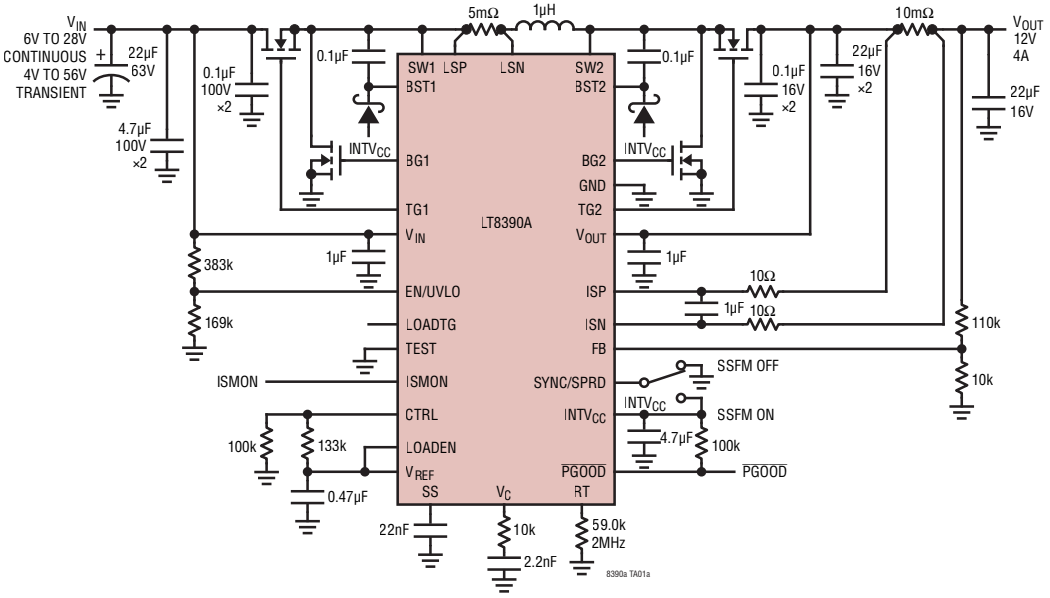
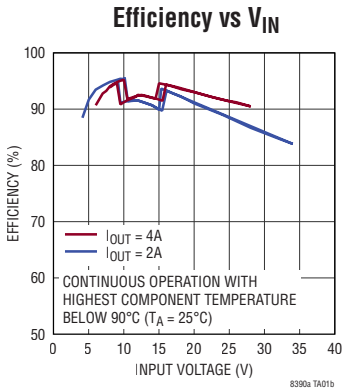
TYPICAL APPLICATION

95% Efficient 48W (12V 4A) 2MHz Buck-Boost Voltage Regulator





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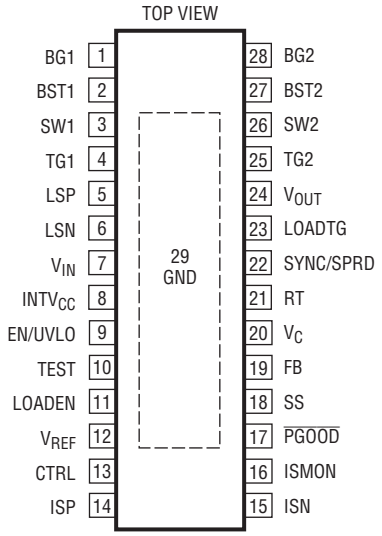
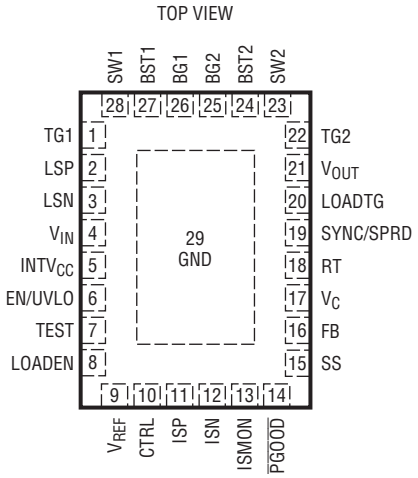
ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{IN}, EN/UVLO, V_{OUT}, ISP, ISN 60V
(ISP-ISN) .....–1V to 1V
BST1, BST2.....66V
SW1, SW2, LSP, LSN ..... –6V to 60V
$INTV_{CC}$, (BST1-SW1), (BST2-SW2).....6V
(BST1-LSP), (BST1-LSN) 6V
FB, LOADEN, SYNC/SPRD, CTRL, $\overline{PGOOD}$.....6V
Operating Junction Temperature Range (Notes 2, 3)
LT8390AE ..... –40°C to 125°C
LT8390AI ..... –40°C to 125°C
LT8390AH..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



FE PACKAGE
28-LEAD PLASTIC TSSOP
θ_{JA} = 30°C/W, θ_{JC} = 5°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN
θ_{JA} = 43°C/W, θ_{JC} = 3.4°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION http://www.linear.com/product/LT8390A#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8390AEFE#PBF	LT8390AEFE#TRPBF	LT8390AFE	28-Lead Plastic TSSOP	–40°C to 125°C
LT8390AIFE#PBF	LT8390AIFE#TRPBF	LT8390AFE	28-Lead Plastic TSSOP	–40°C to 125°C
LT8390AHFE#PBF	LT8390AHFE#TRPBF	LT8390AFE	28-Lead Plastic TSSOP	–40°C to 150°C
LT8390AEUFD#PBF	LT8390AEUFD#TRPBF	8390A	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LT8390AIUFD#PBF	LT8390AIUFD#TRPBF	8390A	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LT8390AHUFD#PBF	LT8390AHUFD#TRPBF	8390A	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, $V_{EN/UVLO}$ = 1.5V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply						
V_{IN} Operating Voltage Range		●	4		60	V
V_{IN} Quiescent Current	$V_{EN/UVLO}$ = 0.3V $V_{EN/UVLO}$ = 1.1V Not Switching			1 270 2.1	2 2.8	µA µA mA
V_{OUT} Voltage Range		●	0		60	V
V_{OUT} Quiescent Current	$V_{EN/UVLO}$ = 0.3V, V_{OUT} = 12V $V_{EN/UVLO}$ = 1.1V, V_{OUT} = 12V Not Switching, V_{OUT} = 12V		 20	0.1 0.1 40	0.5 0.5 60	µA µA µA
Linear Regulators						
$INTV_{CC}$ Regulation Voltage	I_{INTVCC} = 20mA		4.85	5.0	5.15	V
$INTV_{CC}$ Load Regulation	I_{INTVCC} = 0mA to 80mA			1	4	%
$INTV_{CC}$ Line Regulation	I_{INTVCC} = 20mA, V_{IN} = 6V to 60V			1	4	%
$INTV_{CC}$ Current Limit	V_{INTVCC} = 4.5V		110	145	190	mA
$INTV_{CC}$ Dropout Voltage (V_{IN} – $INTV_{CC}$)	I_{INTVCC} = 20mA, V_{IN} = 4V			160		mV
$INTV_{CC}$ Undervoltage Lockout Threshold	Falling		3.44	3.54	3.64	V
$INTV_{CC}$ Undervoltage Lockout Hysteresis				0.24		V
V_{REF} Regulation Voltage	I_{VREF} = 100µA	●	1.97	2.00	2.03	V
V_{REF} Load Regulation	I_{VREF} = 0mA to 1mA			0.4	1	%
V_{REF} Line Regulation	I_{VREF} = 100µA, V_{IN} = 4V to 60V			0.1	0.2	%
V_{REF} Current Limit	V_{REF} = 1.8V		2	2.5	3.2	mA
V_{REF} Undervoltage Lockout Threshold	Falling		1.78	1.84	1.90	V
V_{REF} Undervoltage Lockout Hysteresis				50		mV
Control Inputs/Outputs						
EN/UVLO Shutdown Threshold		●	0.3	0.6	1.0	V
EN/UVLO Enable Threshold	Falling	●	1.196	1.220	1.244	V
EN/UVLO Enable Hysteresis				13		mV
EN/UVLO Hysteresis Current	$V_{EN/UVLO}$ = 0.3V $V_{EN/UVLO}$ = 1.1V $V_{EN/UVLO}$ = 1.3V		–0.1 2.1 –0.1	0 2.5 0	0.1 2.9 0.1	µA µA µA
CTRL Input Bias Current	V_{CTRL} = 0.75V, Current Out of Pin		0	20	50	nA
CTRL Latch-Off Threshold	Falling	●	285	300	315	mV
CTRL Latch-Off Hysteresis				25		mV
Load Switch Driver						
LOADEN Threshold	Rising	●	1.3	1.4	1.5	V
LOADEN Hysteresis				220		mV
Minimum V_{OUT} for LOADTG to be On	V_{LOADEN} = 5V			2.4	3	V
LOADTG On Voltage $V_{(VOUT-LOADTG)}$	V_{OUT} = 12V		4.5	5	5.5	V
LOADTG Off Voltage $V_{(VOUT-LOADTG)}$	V_{OUT} = 12V		–0.1	0	0.1	V
LOADEN to LOADTG Turn On Propagation Delay LOADEN to LOADTG Turn Off Propagation Delay	C_{LOADTG} = 3.3nF to V_{OUT}, 50% to 50% C_{LOADTG} = 3.3nF to V_{OUT}, 50% to 50%			90 40		ns ns
LOADTG Turn On Fall Time LOADTG Turn Off Rise Time	C_{LOADTG} = 3.3nF to V_{OUT}, 10% to 90% C_{LOADTG} = 3.3nF to V_{OUT}, 90% to 10%			300 10		ns ns

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, $V_{EN/UVLO}$ = 1.5V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Error Amplifier						
Full Scale Current Regulation $V_{(ISP-ISN)}$	V_{CTRL} = 2V, V_{ISP} = 12V V_{CTRL} = 2V, V_{ISP} = 0V	● ●	97 97	100 100	103 103	mV mV
1/10th Current Regulation $V_{(ISP-ISN)}$	V_{CTRL} = 0.35V, V_{ISP} = 12V V_{CTRL} = 0.35V, V_{ISP} = 0V	● ●	8 8	10 10	12 12	mV mV
ISMON Monitor Output V_{ISMON}	$V_{(ISP-ISN)}$ = 100mV, V_{ISP} = 12V/0V $V_{(ISP-ISN)}$ = 10mV, V_{ISP} = 12V/0V $V_{(ISP-ISN)}$ = 0mV, V_{ISP} = 12V/0V	● ● ●	1.20 0.30 0.20	1.25 0.35 0.25	1.30 0.40 0.30	V V V
ISP/ISN Input Common Mode Range		●	0		60	V
ISP/ISN Low Side to High Side Switchover Voltage	V_{ISP} = V_{ISN}			1.8		V
ISP/ISN High Side to Low Side Switchover Voltage	V_{ISP} = V_{ISN}			1.7		V
ISP Input Bias Current	V_{LOADEN} = 5V, V_{ISP} = V_{ISN} = 12V V_{LOADEN} = 5V, V_{ISP} = V_{ISN} = 0V $V_{EN/UVLO}$ = 0V, V_{ISP} = V_{ISN} = 12V or 0V			23 –10 0		µA µA µA
ISN Input Bias Current	V_{LOADEN} = 5V, V_{ISP} = V_{ISN} = 12V V_{LOADEN} = 5V, V_{ISP} = V_{ISN} = 0V $V_{EN/UVLO}$ = 0V, V_{ISP} = V_{ISN} = 12V or 0V			23 –10 0		µA µA µA
ISP/ISN Current Regulation Amplifier g_m				2000		µs
FB Regulation Voltage	V_C = 1.2V	●	0.985	1.00	1.015	V
FB Line Regulation	V_{IN} = 4V to 60V			0.2	0.5	%
FB Load Regulation				0.2	0.8	%
FB Voltage Regulation Amplifier g_m				660		µS
FB Input Bias Current	FB in Regulation, Current Out of Pin			10	40	nA
V_C Output Impedance				10		MΩ
V_C Standby Leakage Current	V_C = 1.2V, V_{LOADEN} = 0V		–10	0	10	nA
Current Comparator						
Maximum Current Sense Threshold $V_{(LSP-LSN)}$	Buck, V_{FB} = 0.8V Boost, V_{FB} = 0.8V	● ●	35 40	50 50	65 60	mV mV
LSP Pin Bias Current	V_{LSP} = V_{LSN} = 12V			60		µA
LSN Pin Bias Current	V_{LSP} = V_{LSN} = 12V			60		µA
Fault						
FB Overvoltage Threshold (V_{FB})	Rising	●	1.08	1.1	1.12	V
FB Overvoltage Hysteresis		●	35	50	65	mV
FB Short Threshold (V_{FB})	Falling	●	0.24	0.25	0.26	V
FB Short Hysteresis	Hysteresis	●	35	50	65	mV
ISP/ISN Over Current Threshold $V_{(ISP-ISN)}$	V_{ISP} = 12V			750		mV
$\overline{PGOOD}$ Upper Threshold Offset from V_{FB}	Rising	●	8	10	12	%
$\overline{PGOOD}$ Lower Threshold Offset from V_{FB}	Falling	●	–12	–10	–8	%
$\overline{PGOOD}$ Pull-Down Resistance				100	200	Ω
SS Hard Pull-Down Resistance	$V_{EN/UVLO}$ = 1.1V			100	200	Ω
SS Pull-Up Current	V_{FB} = 0.4V, V_{SS} = 0V		10	12.5	15	µA
SS Pull-Down Current	V_{FB} = 0.1V, V_{SS} = 2V		1	1.25	1.5	µA
SS Fault Latch-Off Threshold				1.7		V
SS Fault Reset Threshold				0.2		V

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, $V_{EN/UVLO}$ = 1.5V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Oscillator						
RT Pin Voltage	R_T = 100kΩ			1.00		V
Switching Frequency	$V_{SYNC/SPRD}$ = 0V, R_T = 226kΩ $V_{SYNC/SPRD}$ = 0V, R_T = 100kΩ $V_{SYNC/SPRD}$ = 0V, R_T = 59.0kΩ	 ●	645 1290 1900	685 1360 2000	725 1430 2100	kHz kHz kHz
SYNC Frequency			600		2100	kHz
SYNC/SPRD Input Bias Current	$V_{SYNC/SPRD}$ = 5V		–0.1	0	0.1	µA
SYNC/SPRD Threshold Voltage			0.4		1.5	V
Highest Spread Spectrum Above Oscillator Frequency	$V_{SYNC/SPRD}$ = 5V		21	23	25	%
Region Transition						
Buck-Boost to Boost (V_{IN}/V_{OUT})			0.73	0.75	0.77	
Boost to Buck-Boost (V_{IN}/V_{OUT})			0.83	0.85	0.87	
Buck to Buck-Boost (V_{IN}/V_{OUT})			1.23	1.25	1.27	
Buck-Boost to Buck (V_{IN}/V_{OUT})			1.31	1.33	1.35	
Peak-Buck to Peak-Boost (V_{IN}/V_{OUT})			0.96	0.98	1.00	
Peak-Boost to Peak-Buck (V_{IN}/V_{OUT})			1.00	1.02	1.04	
NMOS Drivers						
TG1, TG2 Gate Driver On-Resistance Gate Pull-Up Gate Pull-Down	$V_{(BST-SW)}$ = 5V			 2.6 1.4		 Ω Ω
BG1, BG2 Gate Driver On-Resistance Gate Pull-Up Gate Pull-Down	V_{INTVCC} = 5V			 3.2 1.2		 Ω Ω
TG1, TG2 Rise Time TG1, TG2 Fall Time	C_L = 3.3nF, 10% to 90% C_L = 3.3nF, 90% to 10%			25 20		ns ns
BG1, BG2 Rise Time BG1, BG2 Fall Time	C_L = 3.3nF, 10% to 90% C_L = 3.3nF, 90% to 10%			25 20		ns ns
TG Off to BG On Delay	C_L = 3.3nF			25		ns
BG Off to TG On Delay	C_L = 3.3nF			25		ns
TG1 Minimum Duty Cycle in Buck Region	Peak-Buck Current Mode			10		%
TG1 Maximum Duty Cycle in Buck Region	Peak-Buck Current Mode			90		%
TG1 Fixed Duty Cycle in Buck-Boost Region	Peak-Boost Current Mode			80		%
BG2 Fixed Duty Cycle in Buck-Boost Region	Peak-Buck Current Mode			20		%
BG2 Minimum Duty Cycle in Boost Region	Peak-Boost Current Mode			10		%
BG2 Maximum Duty Cycle in Boost Region	Peak-Boost Current Mode			90		%

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT8390AE is guaranteed to meet performance specifications from 0°C to 125°C operating junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT8390AI is guaranteed over the –40°C to 125°C operating junction temperature range. The LT8390AH is guaranteed over the –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 3: The LT8390A includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability.

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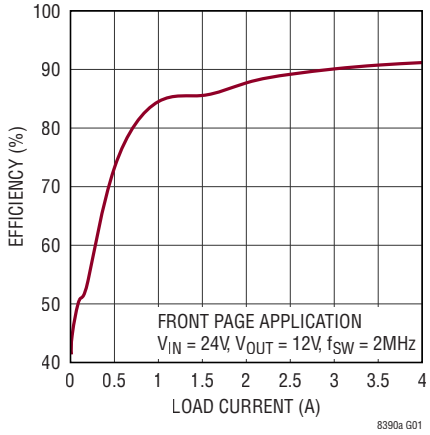
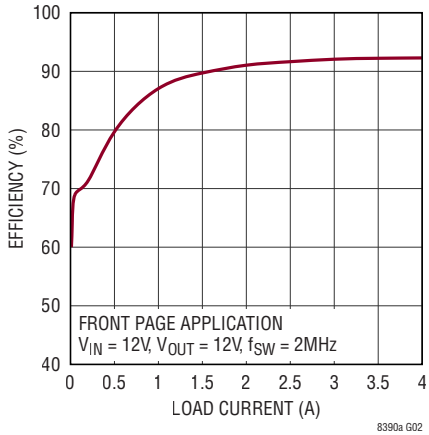
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

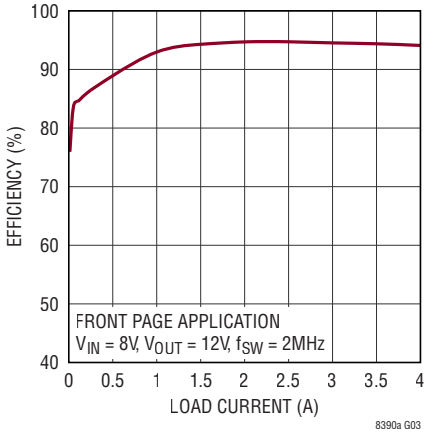
Efficiency vs Load Current (Buck Region)



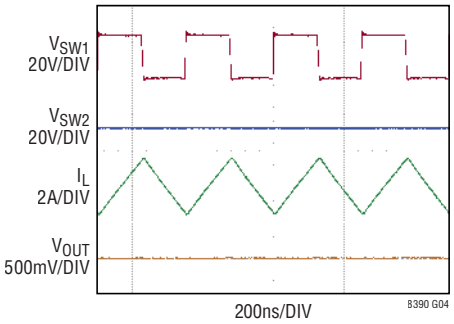
Efficiency vs Load Current (Buck-Boost Region)



Efficiency vs Load Current (Boost Region)

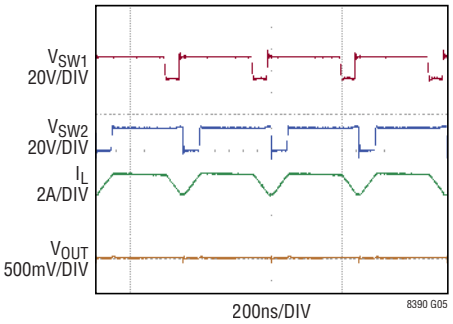


Switching Waveforms (Buck Region)



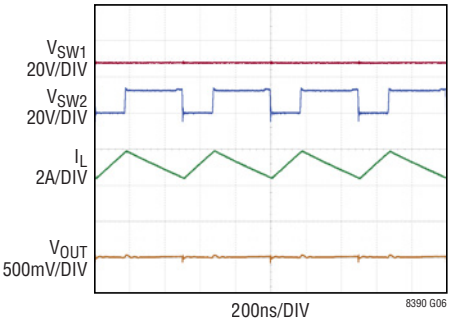
FRONT PAGE APPLICATION
V_{IN} = 24V, I_{OUT} = 2A

Switching Waveforms (Buck-Boost Region)



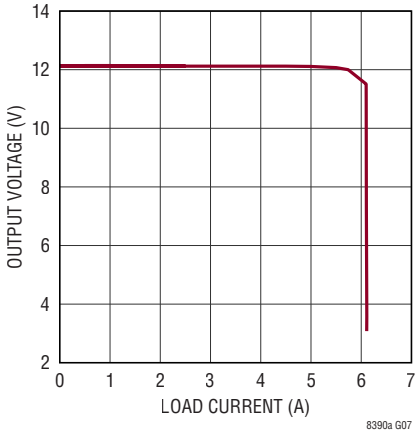
FRONT PAGE APPLICATION
V_{IN} = 12V, I_{OUT} = 2A

Switching Waveforms (Boost Region)

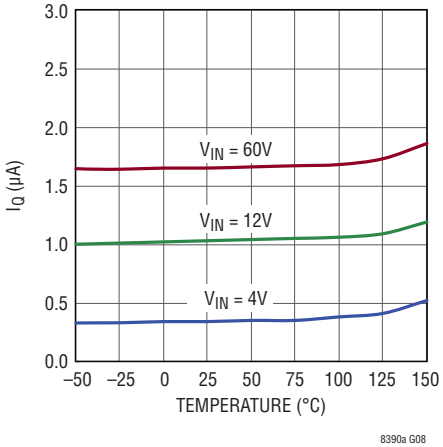


FRONT PAGE APPLICATION
V_{IN} = 8V, I_{OUT} = 2A

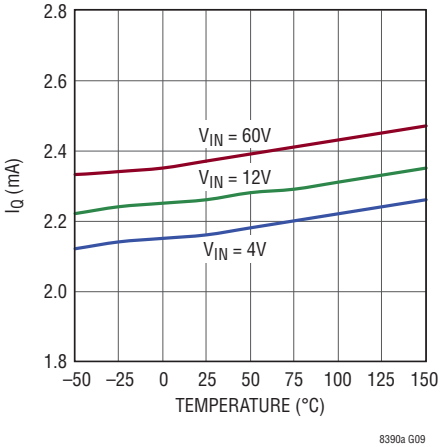
V_{OUT} vs I_{OUT} (CV/CC)



V_{IN} Shutdown Current



V_{IN} Quiescent Current



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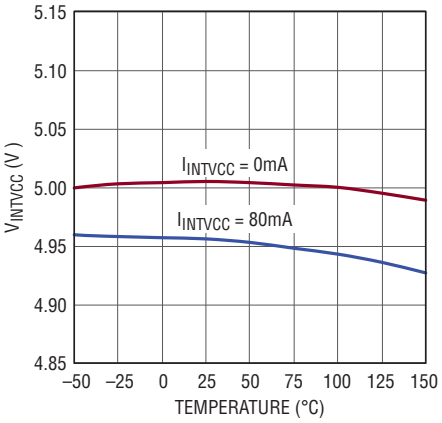
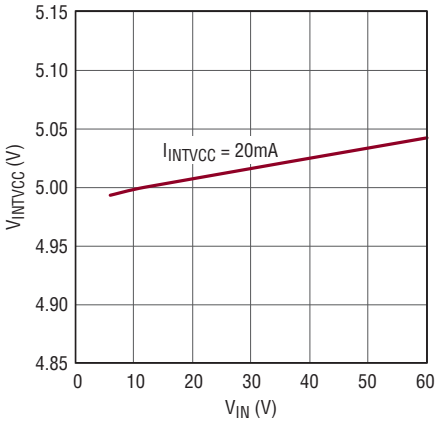
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

$INTV_{CC}$ Voltage vs Temperature



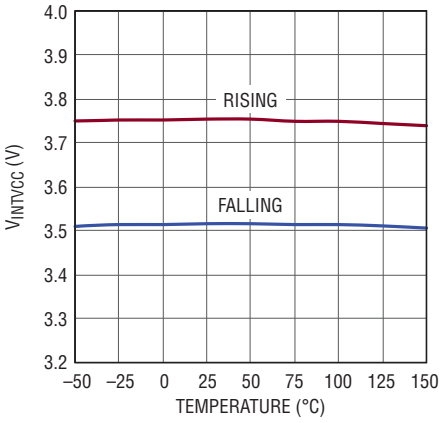
8390a G10

$INTV_{CC}$ Voltage vs V_{IN}



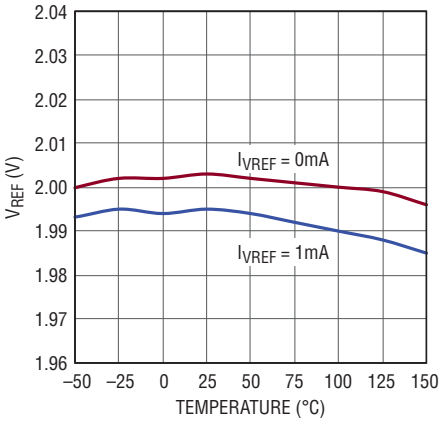
8390a G11

$INTV_{CC}$ UVLO Threshold



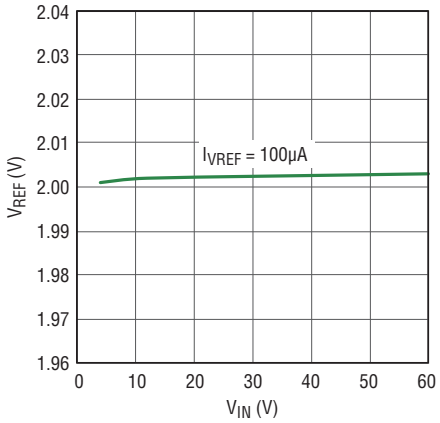
8390a G12

V_{REF} Voltage vs Temperature



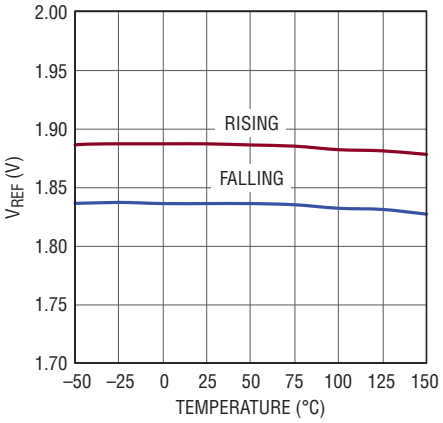
8390a G13

V_{REF} Voltage vs V_{IN}



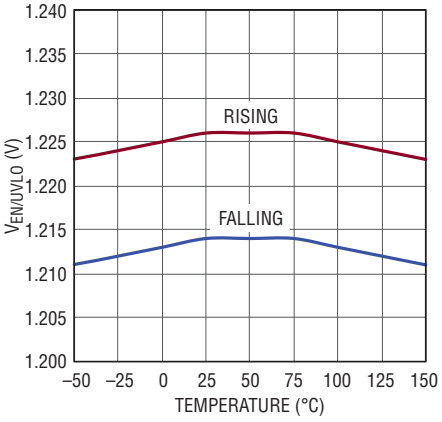
8390a G14

V_{REF} UVLO Threshold



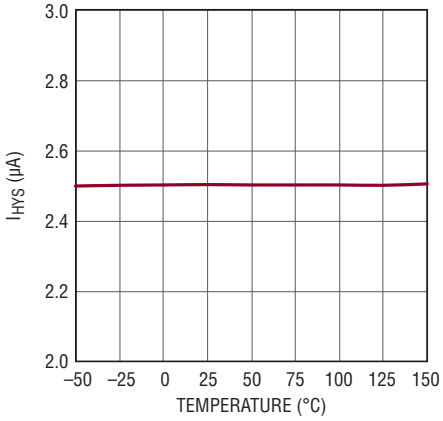
8390a G15

EN/UVLO Enable Threshold



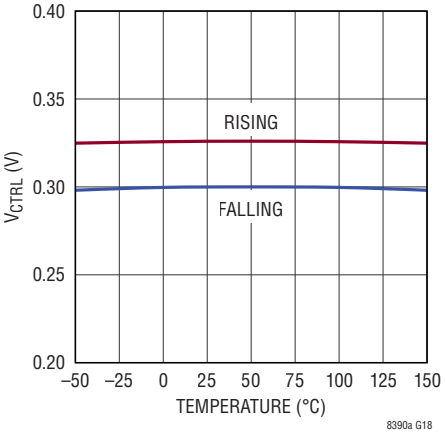
8390a G16

EN/UVLO Hysteresis Current



8390a G17

CTRL Latch-Off Threshold



8390a G18

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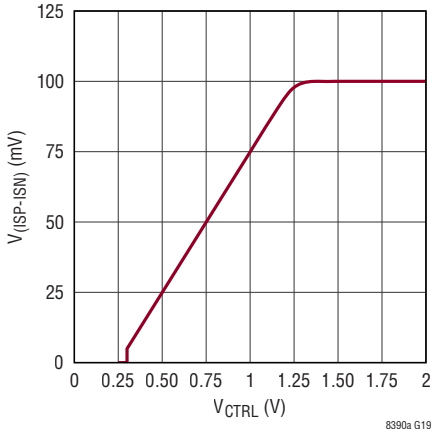
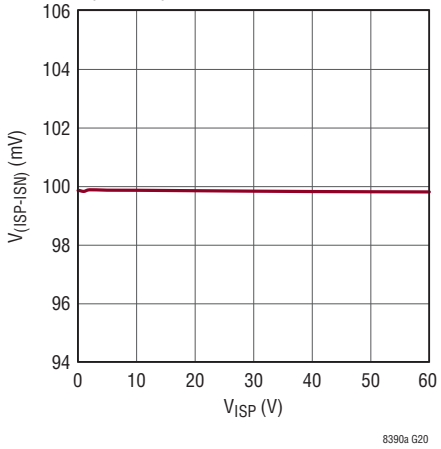
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

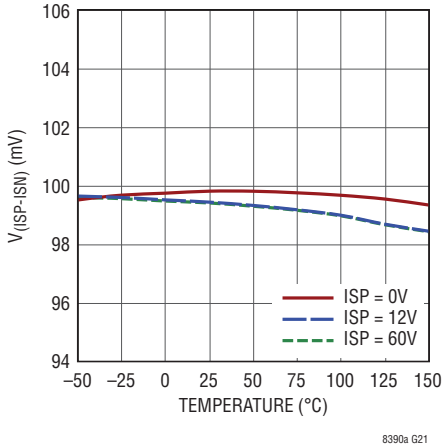
$V_{(ISP-ISN)}$ Regulation vs V_{CTRL}



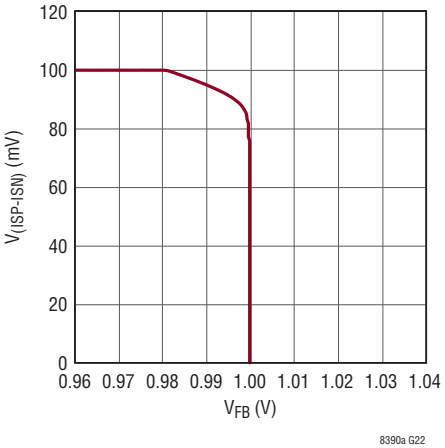
$V_{(ISP-ISN)}$ Regulation vs V_{ISP}



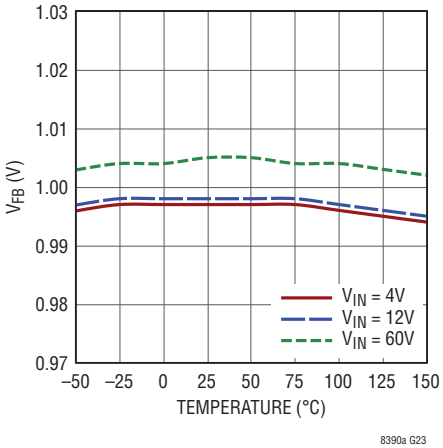
$V_{(ISP-ISN)}$ Regulation vs Temperature



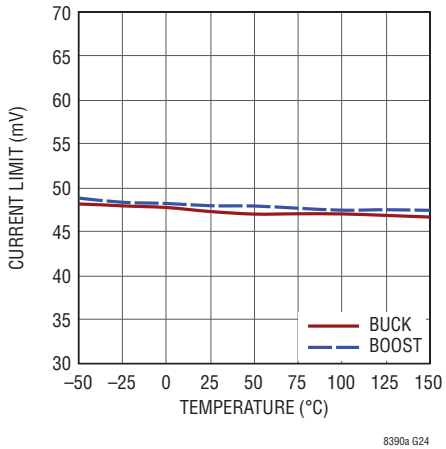
$V_{(ISP-ISN)}$ Regulation vs V_{FB}



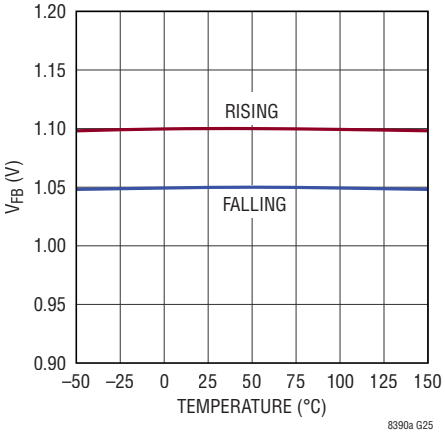
FB Regulation vs Temperature



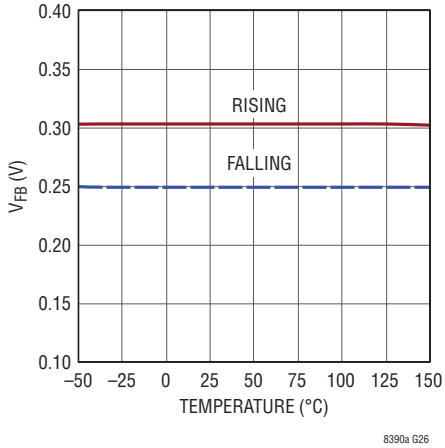
Maximum Current Sense vs Temperature



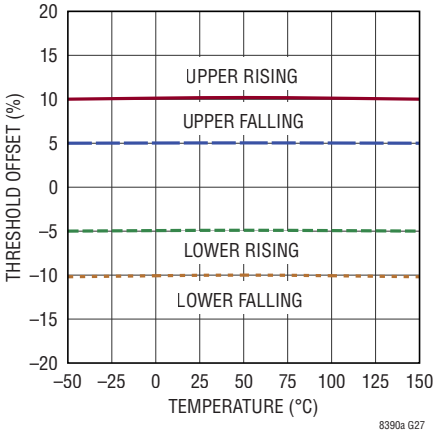
FB Overvoltage Threshold



FB Short Threshold



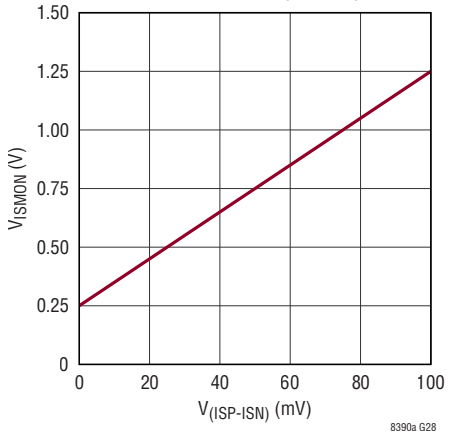
$\overline{PGOOD}$ Thresholds



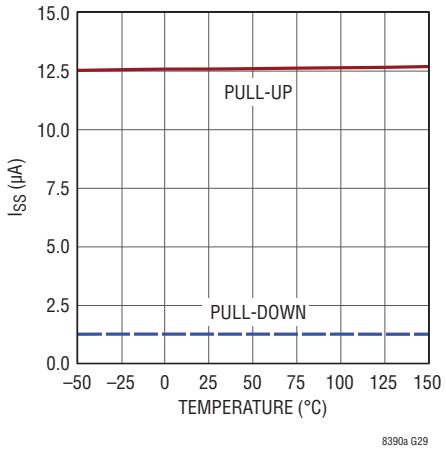
Downloaded from Arrow.com.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

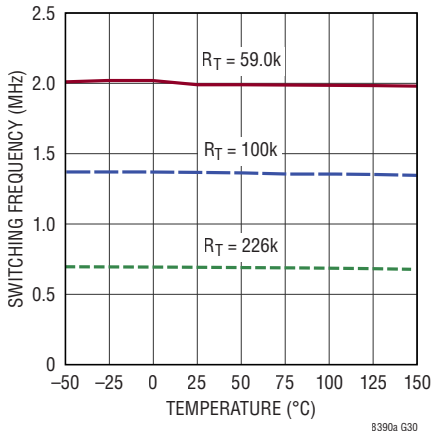
ISMON Voltage vs $V_{(ISP-ISN)}$



SS Current vs Temperature



Oscillator Frequency vs Temperature



PIN FUNCTIONS

BG1: Buck Side Bottom Gate Drive. Drives the gate of buck side bottom N-channel MOSFET with a voltage swing from ground to $INTV_{CC}$.

BST1: Buck Side Bootstrap Floating Driver Supply. The BST1 pin has an integrated bootstrap Schottky diode from the $INTV_{CC}$ pin and requires an external bootstrap capacitor to the SW1 pin. The BST1 pin swings from a diode voltage drop below $INTV_{CC}$ to (V_{IN} + $INTV_{CC}$).

SW1: Buck Side Switch Node. The SW1 pin swings from a Schottky diode voltage drop below ground up to V_{IN}.

TG1: Buck Side Top Gate Drive. Drives the gate of buck side top N-channel MOSFET with a voltage swing from SW1 to BST1.

LSP: Positive Terminal of the Buck Side Inductor Current Sense Resistor (R_{SENSE}). Ensure accurate current sense with Kelvin connection.

LSN: Negative Terminal of the Buck Side Inductor Current Sense Resistor (R_{SENSE}). Ensure accurate current sense with Kelvin connection.

V_{IN}: Input Supply. The V_{IN} pin must be tied to the power input to determine the buck, buck-boost, or boost operation regions. Locally bypass this pin to ground with a minimum 1µF ceramic capacitor.

$INTV_{CC}$: Internal 5V Linear Regulator Output. The $INTV_{CC}$ linear regulator is supplied from the V_{IN} pin, and powers the internal control circuitry and gate drivers. Locally bypass this pin to ground with a minimum 4.7µF ceramic capacitor.

EN/UVLO: Enable and Undervoltage Lockout. Force the pin below 0.3V to shut down the part and reduce V_{IN} quiescent current below 2µA. Force the pin above 1.233V for normal operation. The accurate 1.220V falling threshold can be used to program an undervoltage lockout (UVLO) threshold with a resistor divider from V_{IN} to ground. An accurate 2.5µA pull-down current allows the programming of V_{IN} UVLO hysteresis. If neither function is used, tie this pin directly to V_{IN}.

TEST: Factory Test. This pin is used for testing purpose only and must be directly connected to ground for the part to operate properly.

LOADEN: Load Switch Enable Input. The LOADEN pin is used to control the ON/OFF of the high side PMOS load switch. If the load switch control is not used, tie this pin to V_{REF} or $INTV_{CC}$. Forcing the pin low turns off TG1 and TG2, turns on BG1 and BG2, disconnects the V_C pin from all internal loads, and turns off LOADTG.

V_{REF}: Voltage Reference Output. The V_{REF} pin provides an accurate 2V reference capable of supplying 1mA current. Locally bypass this pin to ground with a 0.47µF ceramic capacitor.

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PIN FUNCTIONS

CTRL: Control Input for ISP/ISN Current Sense Threshold. The CTRL pin is used to program the ISP/ISN current limit:

$$I_{IS(MAX)} = \frac{Min(V_{CTRL} - 0.25V, 1V)}{10 \bullet R_{IS}}$$

The V_{CTRL} can be set by an external voltage reference or a resistor divider from V_{REF} to ground. For $0.3V \le V_{CTRL} \le 1.15V$, the current sense threshold linearly goes up from 5mV to 90mV. For $V_{CTRL} \ge 1.35V$, the current sense threshold is constant at 100mV full scale value. For $1.15V \le V_{CTRL} \le 1.35V$, the current sense threshold smoothly transitions from the linear function of V_{CTRL} to the 100mV constant value. Tie CTRL to V_{REF} for the 100mV full scale threshold. Force the pin below 0.3V to stop switching.

ISP: Positive Terminal of the ISP/ISN Current Sense Resistor (R_{IS}). Ensure accurate current sense with Kelvin connection.

ISN: Negative Terminal of the ISP/ISN Current Sense Resistor (R_{IS}). Ensure accurate current sense with Kelvin connection.

ISMON: ISP/ISN Current Sense Monitor Output. The ISMON pin generates a voltage that is equal to ten times $V_{(ISP-ISN)}$ plus 0.25V offset voltage. For parallel applications, tie the master LT8390A ISMON pin to the slave LT8390A CTRL pin.

$\overline{PGOOD}$: Power Good Open Drain Output. The $\overline{PGOOD}$ pin is pulled low when the FB pin is within ±10% of the final regulation voltage. To function, the pin requires an external pull-up resistor.

SS: Soft-Start Timer Setting. The SS pin is used to set soft-start timer by connecting a capacitor to ground. An internal 12.5µA pull-up current charging the external SS capacitor gradually ramps up FB regulation voltage. A 22nF capacitor is recommended on this pin. Any UVLO or thermal shutdown immediately pulls SS pin to ground and stops switching. Using a single resistor from SS to V_{REF}, the LT8390A can be set in three different fault protection modes during output short-circuit condition: hiccup (no resistor), latch-off (499kΩ), and keep-running (100kΩ). See more details in the Application Information section.

FB: Voltage Loop Feedback Input. The FB pin is used for constant-voltage regulation and output fault protection. The internal error amplifier with its output V_C regulates V_{FB} to 1.00V through the DC/DC converter. During output short-circuit ($V_{FB} < 0.25V$) condition, the part gets into one fault mode per customer setting. During an overvoltage ($V_{FB} > 1.1V$) condition, the part turns off all TG1, BG1, TG2, BG2, and LOADTG.

V_C: Error Amplifier Output to Set Inductor Current Comparator Threshold. The V_C pin is used to compensate the control loop with an external RC network. During LOADEN low state, the V_C pin is disconnected from all internal loads to store its voltage information.

RT: Switching Frequency Setting. Connect a resistor from this pin to ground to set the internal oscillator frequency from 600kHz to 2MHz.

SYNC/SPRD: Switching Frequency Synchronization or Spread Spectrum. Ground this pin for switching at internal oscillator frequency. Apply a clock signal for external frequency synchronization. Tie to $INTV_{CC}$ for 25% triangle spread spectrum above internal oscillator frequency.

LOADTG: High Side PMOS Load Switch Top Gate Drive. A buffered and inverted version of the LOADEN input signal, the LOADTG pin drives an external high side PMOS load switch with a voltage swing from the higher voltage of (V_{OUT}-5V) and 1.2V to V_{OUT}. Leave this pin unconnected if not used.

V_{OUT}: Output Supply. The V_{OUT} pin must be tied to the power output to determine the buck, buck-boost, or boost operation regions. The V_{OUT} pin also serves as positive rail for the LOADTG drive. Locally bypass this pin to ground with a minimum 1µF ceramic capacitor.

TG2: Boost Side Top Gate Drive. Drives the gate of boost side top N-Channel MOSFET with a voltage swing from SW2 to BST2.

SW2: Boost Side Switch Node. The SW2 pin swings from a Schottky diode voltage drop below ground to V_{OUT}.

BST2: Boost Side Bootstrap Floating Driver Supply. The BST2 pin has an integrated bootstrap Schottky diode from the $INTV_{CC}$ pin and requires an external bootstrap capacitor to the SW2 pin. The BST2 pin swings from a diode voltage drop below $INTV_{CC}$ to (V_{OUT} + $INTV_{CC}$).

BG2: Boost Side Bottom Gate Drive. Drives the gate of boost side bottom N-channel MOSFET with a voltage swing from ground to $INTV_{CC}$.

GND (Exposed Pad): Ground. Solder the exposed pad directly to the ground plane.

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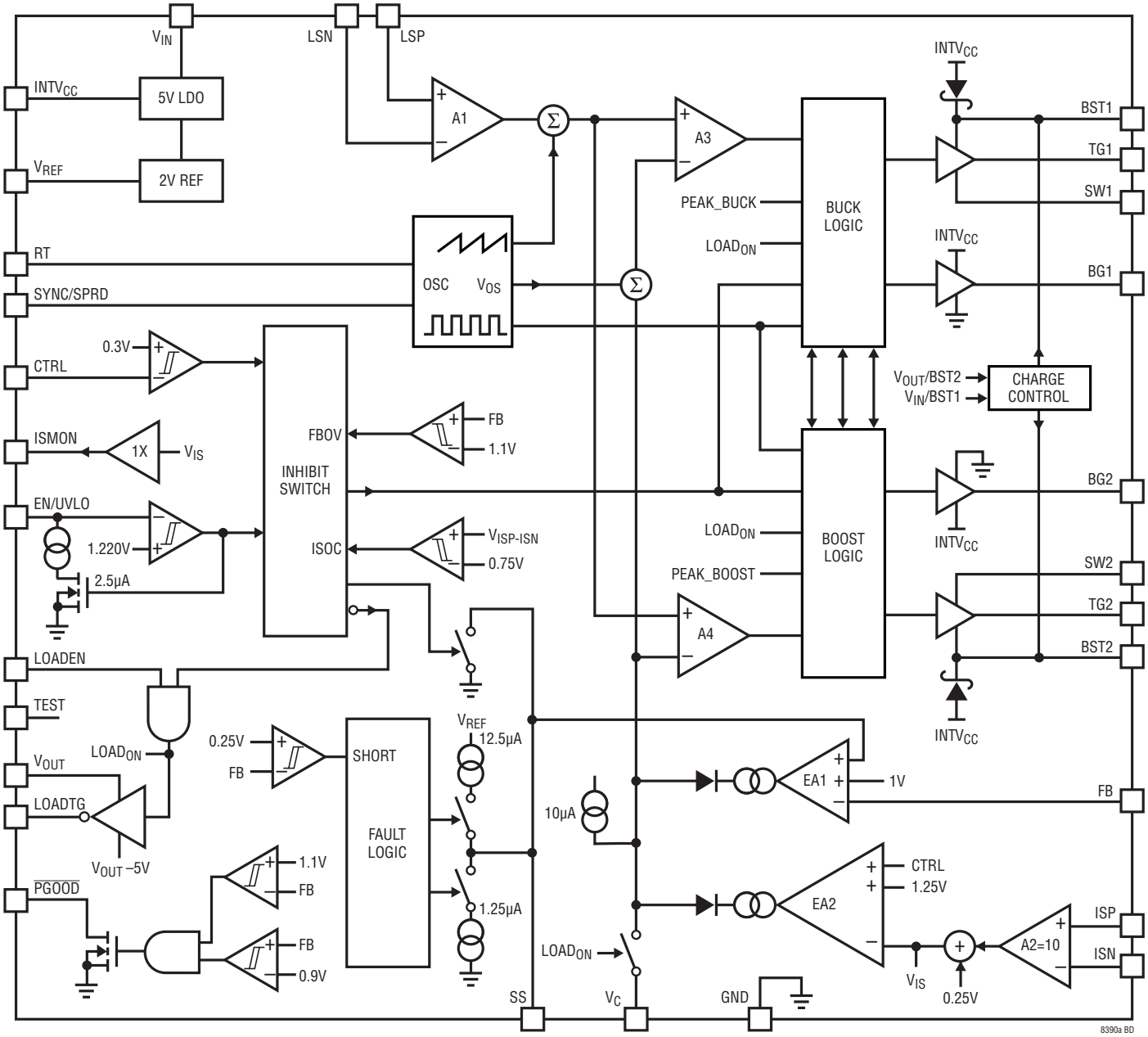
BLOCK DIAGRAM



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OPERATION

The LT8390A is a current mode DC/DC controller that can regulate output voltage, input or output current from input voltage above, below, or equal to the output voltage. The LTC proprietary peak-buck peak-boost current mode control scheme uses a single inductor current sense resistor and provides smooth transition between buck region, buck-boost region, and boost region. Its operation is best understood by referring to the Block Diagram.

Power Switch Control

Figure 1 shows a simplified diagram of how the four power switches A, B, C, and D are connected to the inductor L, the current sense resistor R_{SENSE}, power input V_{IN}, power output V_{OUT}, and ground. The current sense resistor R_{SENSE} connected to the LSP and LSN pins provides inductor current information for both peak current mode control and reverse current detection in buck region, buck-boost region, and boost region. Figure 2 shows the current mode control as a function of V_{IN}/V_{OUT} ratio and Figure 3 shows the operation region as a function of V_{IN}/V_{OUT} ratio. The power switches are properly controlled to smoothly transition between modes and regions. Hysteresis is added to prevent chattering between modes and regions.

There are total four states: (1) peak-buck current mode control in buck region, (2) peak-buck current mode control in buck-boost region, (3) peak-boost current mode control in buck-boost region, and (4) peak-boost current mode control in boost region. The following sections give detailed description for each state with waveforms, in which the shoot-through protection dead time between switches A and B, between switches C and D are ignored for simplification.

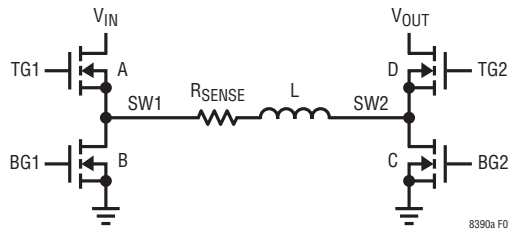

Figure 1. Simplified Diagram of the Power Switches

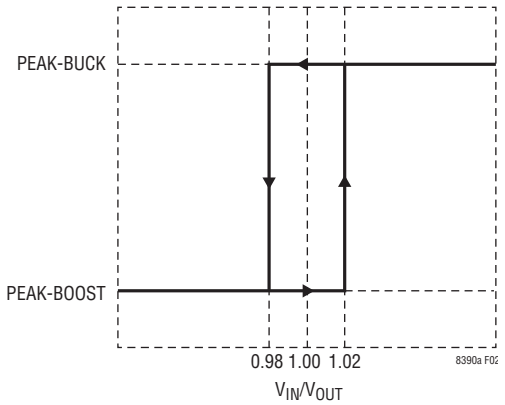

Figure 2. Current Mode vs V_{IN}/V_{OUT} Ratio

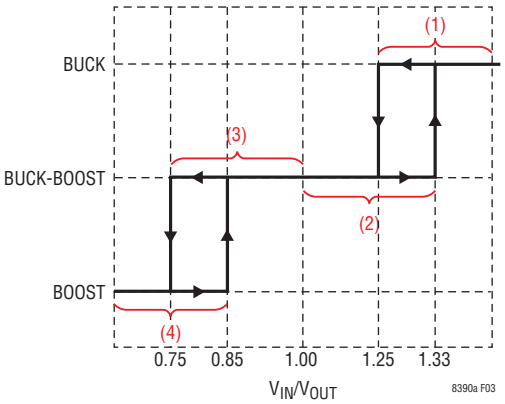

Figure 3. Operation Region vs V_{IN}/V_{OUT} Ratio

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OPERATION

(1) Peak-Buck in Buck Region (V_{IN} >> V_{OUT})

When V_{IN} is much higher than V_{OUT}, the LT8390A uses peak-buck current mode control in buck region (Figure 4). Switch C is always off and switch D is always on. At the beginning of every cycle, switch A is turned on and the inductor current ramps up. When the inductor current hits the peak buck current threshold commanded by V_C voltage at buck current comparator A3 during (A+D) phase, switch A is turned off and switch B is turned on for the rest of the cycle. Switches A and B will alternate, behaving like a typical synchronous buck regulator.

(2) Peak-Buck in Buck-Boost Region (V_{IN} ~> V_{OUT})

When V_{IN} is slightly higher than V_{OUT}, the LT8390A uses peak-buck current mode control in buck-boost region (Figure 5). Switch C is always turned on for the beginning 20% cycle and switch D is always turned on for the remaining 80% cycle. At the beginning of every cycle, switches A and C are turned on and the inductor current ramps up. After 20% cycle, switch C is turned off and switch D is turned on, and the inductor keeps ramping up. When the inductor current hits the peak buck current threshold commanded by V_C voltage at buck current comparator A3 during (A+D) phase, switch A is turned off and switch B is turned on for the rest of the cycle.

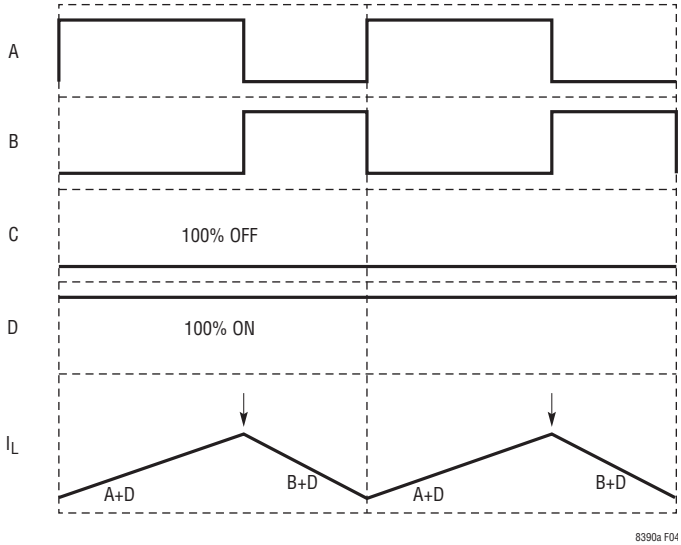

Figure 4. Peak-Buck in Buck Region (V_{IN} >> V_{OUT})

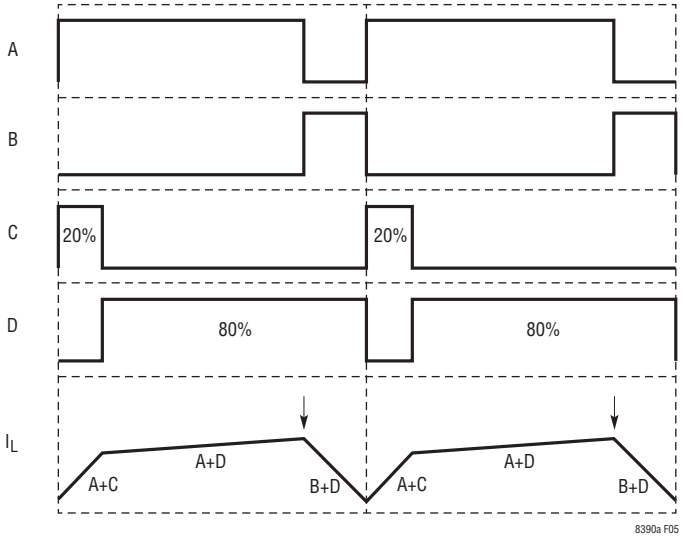

Figure 5. Peak-Buck in Buck-Boost Region (V_{IN} ~> V_{OUT})

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OPERATION

(3) Peak-Boost in Buck-Boost Region (V_{IN} <~ V_{OUT})

When V_{IN} is slightly lower than V_{OUT}, the LT8390A uses peak-boost current mode control in buck-boost region (Figure 6). Switch A is always turned on for the beginning 80% cycle and switch B is always turned on for the remaining 20% cycle. At the beginning of every cycle, switches A and C are turned on and the inductor current ramps up. When the inductor current hits the peak boost current threshold commanded by V_C voltage at boost current comparator A4 during (A+C) phase, switch C is turned off and switch D is turned on for the rest of the cycle. After 80% cycle, switch A is turned off and switch B is turned on for the rest of the cycle.

(4) Peak-Boost in Boost Region (V_{IN} << V_{OUT})

When V_{IN} is much lower than V_{OUT}, the LT8390A uses peak-boost current mode control in boost region (Figure 7). Switch A is always on and switch B is always off. At the beginning of every cycle, switch C is turned on and the inductor current ramps up. When the inductor current hits the peak boost current threshold commanded by V_C voltage at boost current comparator A4 during (A+C) phase, switch C is turned off and switch D is turned on for the rest of the cycle. Switches C and D will alternate, behaving like a typical synchronous boost regulator.

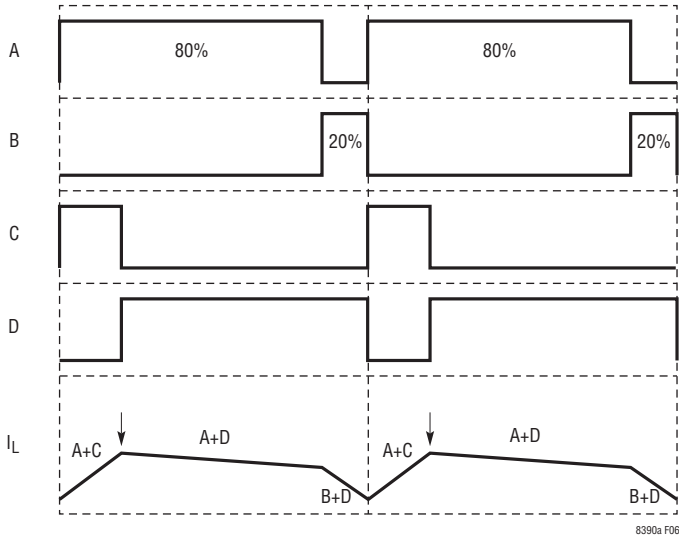

Figure 6. Peak-Boost in Buck-Boost Region (V_{IN} <~ V_{OUT})

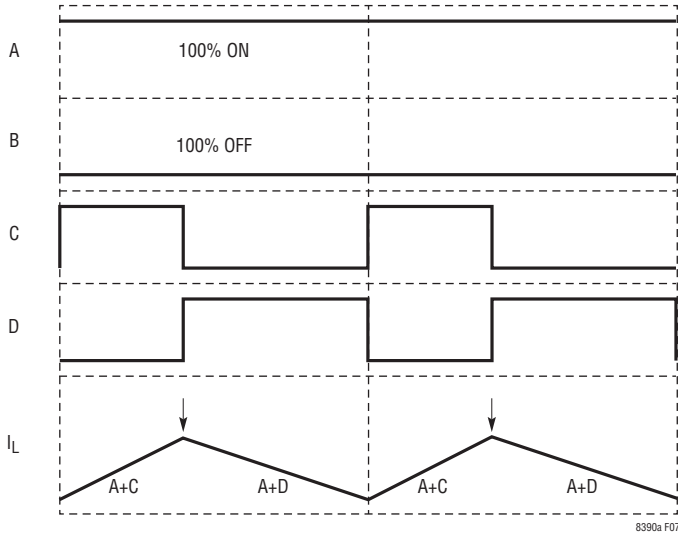

Figure 7. Peak-Boost in Boost Region (V_{IN} << V_{OUT})

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OPERATION

Main Control Loop

The LT8390A is a fixed frequency current mode controller. The inductor current is sensed through the inductor sense resistor between the LSP and LSN pins. The current sense voltage is gained up by amplifier A1 and added to a slope compensation ramp signal from the internal oscillator. The summing signal is then fed into the positive terminals of the buck current comparator A3 and boost current comparator A4. The negative terminals of A3 and A4 are controlled by the voltage on the V_C pin, which is the diode-OR of error amplifiers EA1 and EA2.

Depending on the state of the peak-buck peak-boost current mode control, either the buck logic or the boost logic is controlling the four power switches so that either the FB voltage is regulated to 1V or the current sense voltage between the ISP and ISN pins is regulated by the CTRL pin during normal operation. The gains of EA1 and EA2 have been balanced to ensure smooth transition between constant-voltage and constant-current operation with the same compensation network.

Light Load Current Operation

At light load, the LT8390A runs either at full switching frequency discontinuous conduction mode or pulse-skipping mode, where the switches are held off for multiple cycles (i.e., skipping pulses) to maintain the regulation and improve the efficiency. Both the buck and boost reverse current sense thresholds are set to 1mV (typical) so that no reverse inductor current is allowed. Such no reverse inductor current from the output to the input is highly desired in certain applications.

In the buck region, switch B is turned off whenever the buck reverse current threshold is triggered during (B+D) phase. In the boost region, switch D is turned off whenever the boost reverse current threshold is triggered during (A+D) phase. In the buck-boost region, switch D is turned off whenever the boost reverse current threshold is triggered during (A+D) phase, and both switches B and D are turned off whenever the buck reverse current threshold is triggered during (B+D) phase.

Internal Charge Path

Each of the two top MOSFET drivers is biased from its floating bootstrap capacitor, which is normally re-charged by $INTV_{CC}$ through both the external and internal bootstrap diodes when the top MOSFET is turned off. When the LT8390A operates exclusively in the buck or boost regions, one of the top MOSFETs is constantly on. An internal charge path, from V_{OUT} and BST2 to BST1 or from V_{IN} and BST1 to BST2, charges the bootstrap capacitor to 4.6V so that the top MOSFET can be kept on.

Shutdown and Power-On-Reset

The LT8390A enters shutdown mode and drains less than 2μA quiescent current when the EN/UVLO pin is below its shutdown threshold (0.3V minimum). Once the EN/UVLO pin is above its shutdown threshold (1V maximum), the LT8390A wakes up startup circuitry, generates bandgap reference, and powers up the internal $INTV_{CC}$ LDO. The $INTV_{CC}$ LDO supplies the internal control circuitry and gate drivers. Now the LT8390A enters undervoltage lockout (UVLO) mode with a hysteresis current (2.5μA typical) pulled into the EN/UVLO pin. When the $INTV_{CC}$ pin is charged above its rising UVLO threshold (3.78V typical), the EN/UVLO pin passes its rising enable threshold (1.233V typical), and the junction temperature is less than its thermal shutdown (165°C typical), the LT8390A enters enable mode, in which the EN/UVLO hysteresis current is turned off and the voltage reference V_{REF} is being charged up from ground. From the time of entering enable mode to the time of V_{REF} passing its rising UVLO threshold (1.89V typical), the LT8390A is going through a power-on-reset (POR), waking up the entire internal control circuitry and settling to the right initial conditions. After the POR, the LT8390A is ready and waiting for the signals on the CTRL and LOADEN pins to start switching.

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OPERATION

Start-Up and Fault Protection

Figure 8 shows the start-up and fault sequence for the LT8390A. During the POR state, the SS pin is hard pulled down with a 100Ω to ground. In a pre-biased condition, the SS pin has to be pulled below 0.2V to enter the INIT state, where the LT8390A wait 10µs so that the SS pin can be fully discharged to ground. After the 10µs, the LT8390A enters the UP/PRE state when the LOADON signal goes high. The LOADON high signal happens when CTRL pin is above its rising latch-off thresholds (0.325V typical) and the LOADEN is high.

During the UP/PRE state, the SS pin is charged up by a 12.5µA pull-up current while the switching is disabled and the LOADTG is turned off. Once the SS pin is charged above 0.25V, the LT8390A enters the UP/TRY state, where the LOADTG is turned on first while the switching is still disabled. If an excessive current flowing through the current sense resistor triggers the ISP/ISN over current (ISOC) signal, it will reset the LT8390A back into the POR state. After 10µs in the UP/TRY state without triggering the ISOC signal, the LT8390A enters the UP/RUN state.

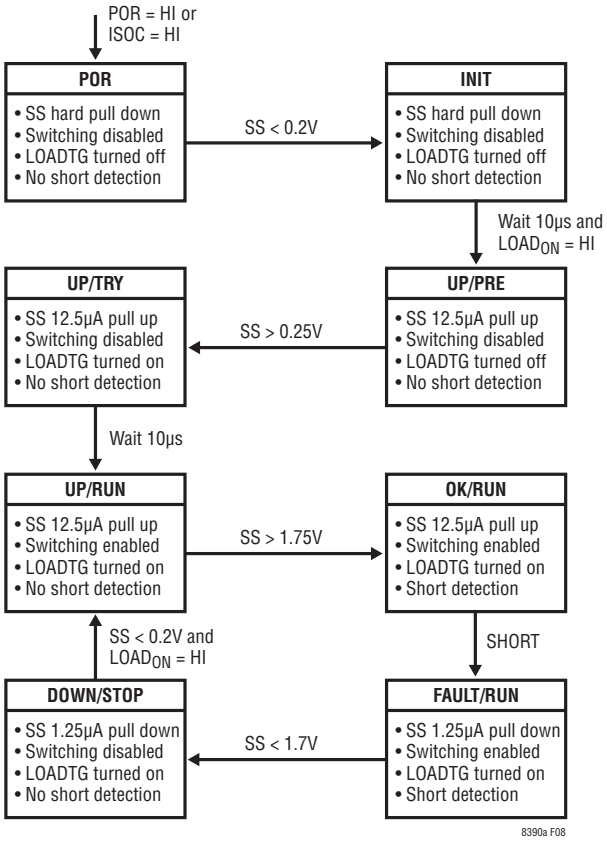

Figure 8. Start-Up and Fault Sequence

During the UP/RUN state, the switching is enabled and the start-up of the output voltage V_{OUT} is controlled by the voltage on the SS pin. When the SS pin voltage is less than 1V, the LT8390A regulates the FB pin voltage to the SS pin voltage instead of the 1V reference. This allows the SS pin to be used to program soft-start by connecting an external capacitor from the SS pin to GND. The internal 12.5µA pull-up current charges up the capacitor, creating a voltage ramp on the SS pin. As the SS pin voltage rises linearly from 0.25V to 1V (and beyond), the output voltage V_{OUT} rises smoothly to its final regulation voltage.

Once the SS pin is charged above 1.75V, the LT8390A enters the OK/RUN state, where the output short detection is activated. The output short means V_{FB} < 0.25V. When the output short happens, the LT8390A enters the FAULT/RUN state, where a 1.25µA pull-down current slowly discharges the SS pin with the other conditions the same as the OK/RUN state. Once the SS pin is discharged below 1.7V, the LT8390A enters the DOWN/STOP state, where the switching is disabled and the short detection is deactivated with the previous fault latched. Once the SS pin is discharged below 0.2V and the LOADON signal is still high, the LT8390A goes back to the UP/RUN state.

In an output short condition, the LT8390A can be set to hiccup, latch-off, or keep-running fault protection mode with a resistor between the SS and V_{REF} pins. Without any resistor, the LT8390A will hiccup between 0.2V and 1.75V and go around the UP/RUN, OK/RUN, FAULT/RUN, and DOWN/STOP states until the fault condition is cleared. With a 499kΩ resistor, the LT8390A will latch off until the EN/UVLO is toggled. With a 100kΩ resistor, the LT8390A will keep running regardless of the fault.

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APPLICATIONS INFORMATION

The front page shows a typical LT8390A application circuit. This Applications Information section serves as a guideline of selecting external components for typical applications. The examples and equations in this section assume continuous conduction mode unless otherwise specified.

Switching Frequency Selection

The LT8390A uses a constant frequency control scheme between 600kHz and 2MHz. Selection of the switching frequency is a tradeoff between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET switching losses, but requires larger inductor and capacitor values. For high power applications, consider operating at lower frequencies to minimize MOSFET heating from switching losses. For low power applications, consider operating at higher frequencies to minimize the total solution size.

In addition, the specific application also plays an important role in switching frequency selection. In a noise-sensitive system, the switching frequency is usually selected to keep the switching noise out of a sensitive frequency band.

Switching Frequency Setting

The switching frequency of the LT8390A can be set by the internal oscillator. With the SYNC/SPRD pin pulled to ground, the switching frequency is set by a resistor from the RT pin to ground. Table 1 shows R_T resistor values for common switching frequencies.

Table 1. Switching Frequency vs R_T Value (1% Resistor)

f_{OSC} (MHz)	R_T (k)
0.6	267
0.8	191
1.0	147
1.2	118
1.4	97.6
1.6	82.5
1.8	66.5
2.0	59.0

Spread Spectrum Frequency Modulation

Switching regulators can be particularly troublesome for applications where electromagnetic interference (EMI) is a concern. To improve the EMI performance, the LT8390A implements a triangle spread spectrum frequency modulation scheme. With the SYNC/SPRD pin tied to $INTV_{CC}$, the LT8390A starts to spread its switching frequency 25% above the internal oscillator frequency. Figure 9 and Figure 10 show the noise spectrum of the front page application when spread spectrum enabled.

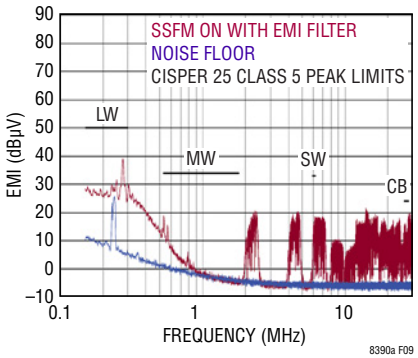

Figure 9. Average Conducted EMI

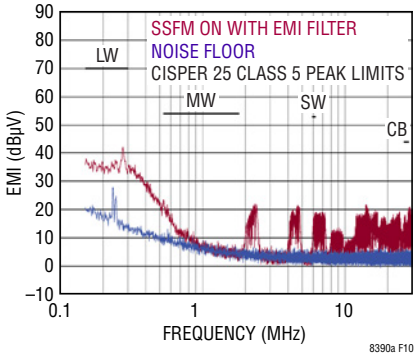

Figure 10. Peak Conducted EMI

Frequency Synchronization

The LT8390A switching frequency can be synchronized to an external clock using the SYNC/SPRD pin. Driving the SYNC/SPRD with a 50% duty cycle waveform is always a good choice, otherwise maintain the duty cycle between 10% and 90%. Due to the use of a phase-locked loop (PLL) inside, there is no restriction between the synchronization frequency and the internal oscillator frequency. The rising edge of the synchronization clock represents the beginning of a switching cycle, turning on switches A and C, or switches A and D.

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Inductor Selection

The switching frequency and inductor selection are interrelated in that higher switching frequencies allow the use of smaller inductor and capacitor values. The inductor value has a direct effect on ripple current. The highest current ripple $\Delta I_L\%$ happens in the buck region at $V_{IN(MAX)}$, and the lowest current ripple $\Delta I_L\%$ happens in the boost region at $V_{IN(MIN)}$. For any given ripple allowance set by customers, the minimum inductance can be calculated as:

$$L_{BUCK} > \frac{V_{OUT} \bullet \left(V_{IN(MAX)} - V_{OUT}\right)}{f \bullet I_{OUT(MAX)} \bullet \Delta I_L\% \bullet V_{IN(MAX)}}$$

$$L_{BOOST} > \frac{V_{IN(MIN)}^2 \bullet \left(V_{OUT} - V_{IN(MIN)}\right)}{f \bullet I_{OUT(MAX)} \bullet \Delta I_L\% \bullet V_{OUT}^2}$$

where:

$$\Delta I_L\% = \frac{\Delta I_L}{I_{L(AVG)}}$$

f is switching frequency

$V_{IN(MIN)}$ is minimum input voltage

$V_{IN(MAX)}$ is maximum input voltage

V_{OUT} is output voltage

$I_{OUT(MAX)}$ is maximum output current

Slope compensation provides stability in constant frequency current mode control by preventing subharmonic oscillations at certain duty cycles. The minimum inductance required for stability when duty cycles are larger than 50% can be calculated as:

$$L > \frac{10 \bullet V_{OUT} \bullet R_{SENSE}}{f}$$

For high efficiency, choose an inductor with low core loss, such as ferrite. Also, the inductor should have low DC resistance to reduce the I^2R losses, and must be able to handle the peak inductor current without saturating. To minimize radiated noise, use a shielded inductor.

R_{SENSE} Selection and Maximum Output Current

R_{SENSE} is chosen based on the required output current. The duty cycle independent maximum current sense thresholds (50mV in peak-buck and 50mV in peak-boost) set the maximum inductor peak current in buck region, buck-boost region, and boost region.

In boost region, the lowest maximum average load current happens at $V_{IN(MIN)}$ and can be calculated as:

$$I_{OUT(MAX_BOOST)} = \left(\frac{50mV}{R_{SENSE}} - \frac{\Delta I_{L(BOOST)}}{2}\right) \bullet \frac{V_{IN(MIN)}}{V_{OUT}}$$

where $\Delta I_{L(BOOST)}$ is peak-to-peak inductor ripple current in boost region and can be calculated as:

$$\Delta I_{L(BOOST)} = \frac{V_{IN(MIN)} \bullet \left(V_{OUT} - V_{IN(MIN)}\right)}{f \bullet L \bullet V_{OUT}}$$

In buck region, the lowest maximum average load current happens at $V_{IN(MAX)}$ and can be calculated as:

$$I_{OUT(MAX_BUCK)} = \left(\frac{50mV}{R_{SENSE}} - \frac{\Delta I_{L(BUCK)}}{2}\right)$$

where $\Delta I_{L(BUCK)}$ is peak-to-peak inductor ripple current in buck region and can be calculated as:

$$\Delta I_{L(BUCK)} = \frac{V_{OUT} \bullet \left(V_{IN(MAX)} - V_{OUT}\right)}{f \bullet L \bullet V_{IN(MAX)}}$$

The maximum current sense R_{SENSE} in boost region is:

$$R_{SENSE(BOOST)} = \frac{2 \bullet 50mV \bullet V_{IN(MIN)}}{2 \bullet I_{OUT(MAX)} \bullet V_{OUT} + \Delta I_{L(BOOST)} \bullet V_{IN(MIN)}}$$

The maximum current sense R_{SENSE} in buck region is

$$R_{SENSE(BUCK)} = \frac{2 \bullet 50mV}{2 \bullet I_{OUT(MAX)} + \Delta I_{L(BUCK)}}$$

The final R_{SENSE} value should be lower than the calculated R_{SENSE} in both buck and boost regions. A 20% to 30% margin is usually recommended. Always choose a low ESL current sense resistor.

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Power MOSFET Selection

The LT8390A requires four external N-channel power MOSFETs, two for the top switches (switches A and D shown in Figure 1) and two for the bottom switches (switches B and C shown in Figure 1). Important parameters for the power MOSFETs are the breakdown voltage $V_{BR(DSS)}$, threshold voltage $V_{GS(TH)}$, on-resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS} and maximum current $I_{DS(MAX)}$.

To achieve 2MHz operation, the power MOSFET selection is critical. With typical 25ns shoot-through protection deadtime, high performance power MOSFETs with low Q_g and low $R_{DS(ON)}$ must be used.

Since the gate drive voltage is set by the 5V $INTV_{CC}$ supply, logic-level threshold MOSFETs must be used in LT8390A applications. Switching four MOSFETs at higher frequency like 2MHz, the substantial gate charge current from $INTV_{CC}$ can be estimated as:

$$I_{INTVCC} = f \bullet \left(Q_{gA} + Q_{gB} + Q_{gC} + Q_{gD}\right)$$

where:

f is the switching frequency

Q_{gA}, Q_{gB}, Q_{gC}, Q_{gD} are the total gate charges of MOSFETs A, B, C, D

Make sure the total required $INTV_{CC}$ current not exceeding the $INTV_{CC}$ current limit in the datasheet. Typically, MOSFETs with less than 10nC Q_g are recommended.

The LT8390A uses the V_{IN}/V_{OUT} ratio to transition between modes and regions. Bigger IR drop in the power path caused by improper MOSFET and inductor selection may prevent the LT8390A from smooth transition. To ensure smooth transitions between buck, buck-boost, and boost modes of operation, choose low $R_{DS(ON)}$ MOSFETs and low DCR inductor to satisfy:

$$I_{OUT(MAX)} \le \frac{0.025 \bullet V_{OUT}}{R_{A,B} + R_{C,D} + R_{SENSE} + R_L}$$

where:

$R_{A,B}$ is the maximum $R_{DS(ON)}$ of MOSFETs A or B at 25°C

$R_{C,D}$ is the maximum $R_{DS(ON)}$ of MOSFETs C or D at 25°C

R_L is the maximum DCR resistor of inductor at 25°C

The $R_{DS(ON)}$ and DCR increase at higher junction temperatures and the process variation have been included in the calculation above.

In order to select the power MOSFETs, the power dissipated by the device must be known. For switch A, the maximum power dissipation happens in boost region, when it remains on all the time. Its maximum power dissipation at maximum output current is given by:

$$P_{A(BOOST)} = \left(\frac{I_{OUT(MAX)} \bullet V_{OUT}}{V_{IN}}\right)^2 \bullet \rho_T \bullet R_{DS(ON)}$$

where ρ_T is a normalization factor (unity at 25°C) accounting for the significant variation in on-resistance with temperature, typically 0.4%/°C as shown in Figure 11. For a maximum junction temperature of 125°C, using a value of ρ_T = 1.5 is reasonable.

Switch B operates in buck region as the synchronous rectifier. Its power dissipation at maximum output current is given by:

$$P_{B(BUCK)} = \frac{V_{IN} - V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX)}^2 \bullet \rho_T \bullet R_{DS(ON)}$$

Switch C operates in boost region as the control switch. Its power dissipation at maximum current is given by:

$$P_{C(BOOST)} = \frac{(V_{OUT} - V_{IN}) \bullet V_{OUT}}{V_{IN}^2} \bullet I_{OUT(MAX)}^2 \bullet \rho_T \bullet R_{DS(ON)} + k \bullet V_{OUT}^3 \bullet \frac{I_{OUT(MAX)}}{V_{IN}} \bullet C_{RSS} \bullet f$$

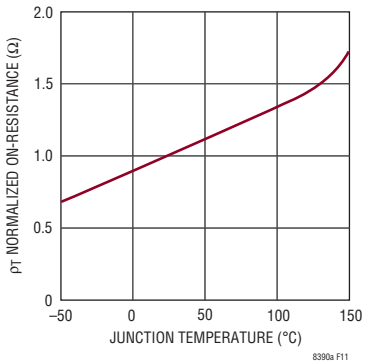

Figure 11. Normalized $R_{DS(ON)}$ vs Temperature

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where C_{RSS} is usually specified by the MOSFET manufacturers. The constant k, which accounts for the loss caused by reverse recovery current, is inversely proportional to the gate drive current and has an empirical value of 1.7.

For switch D, the maximum power dissipation happens in boost region, when its duty cycle is higher than 50%. Its maximum power dissipation at maximum output current is given by:

$$P_{D(BOOST)} = \frac{V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX)}^{2} \bullet \rho_T \bullet R_{DS(ON)}$$

For the same output voltage and current, switch A has the highest power dissipation and switch B has the lowest power dissipation unless a short occurs at the output.

From a known power dissipated in the power MOSFET, its junction temperature can be obtained using the following formula:

$$T_J = T_A + P \bullet R_{TH(JA)}$$

The junction-to-ambient thermal resistance $R_{TH(JA)}$ includes the junction-to-case thermal resistance $R_{TH(JC)}$ and the case-to-ambient thermal resistance $R_{TH(CA)}$. This value of T_J can then be compared to the original, assumed value used in the iterative calculation process.

Optional Schottky Diode (D_B, D_D) Selection

The optional Schottky diodes D_B (in parallel with switch B) and D_D (in parallel with switch D) conduct during the dead time between the conduction of the power MOSFET switches. They are intended to prevent the body diode of synchronous switches B and D from turning on and storing charge during the dead time. In particular, D_B significantly reduces reverse recovery current between switch B turn-off and switch A turn-on, and D_D significantly reduces reverse recovery current between switch D turn-off and switch C turn-on. They improve converter efficiency and reduce switch voltage stress. In order for the diode to be effective, the inductance between it and the synchronous switch must be as small as possible, mandating that these components be placed adjacently.

C_{IN} and C_{OUT} Selection

Input and output capacitance is necessary to suppress voltage ripple caused by discontinuous current moving in and out the regulator. A parallel combination of capacitors is typically used to achieve high capacitance and low equivalent series resistance (ESR). Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Capacitors with low ESR and high ripple current ratings, such as OS-CON and POSCAP are also available.

Ceramic capacitors should be placed near the regula-tor input and output to suppress high frequency switching spikes. Ceramic capacitors, of at least 1µF, should also be placed from V_{IN} to GND and V_{OUT} to GND as close to the LT8390A pins as possible. Due to their excellent low ESR characteristics, ceramic capacitors can significantly reduce input ripple voltage and help reduce power loss in the higher ESR bulk capacitors. X5R or X7R dielectrics are preferred, as these materials retain their capacitance over wide voltage and temperature ranges. Many ceramic capacitors, particularly 0805 or 0603 case sizes, have greatly reduced capacitance at the desired operating voltage.

Input Capacitance C_{IN}: Discontinuous input current is highest in the buck region due to the switch A toggling on and off. Make sure that the C_{IN} capacitor network has low enough ESR and is sized to handle the maximum RMS current. In buck region, the input RMS current is given by:

$$I_{RMS} \approx I_{OUT(MAX)} \bullet \frac{V_{OUT}}{V_{IN}} \bullet \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

The formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT(MAX)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief.

Output Capacitance C_{OUT}: Discontinuous current shifts from the input to the output in the boost region. Make sure that the C_{OUT} capacitor network is capable of reducing the output voltage ripple. The effects of ESR and the bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage. The maximum steady state ripple due to charging and discharging the bulk capacitance is given by:

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$$\Delta V_{CAP(BOOST)} = \frac{I_{OUT(MAX)} \bullet \left(V_{OUT} - V_{IN(MIN)}\right)}{C_{OUT} \bullet V_{OUT} \bullet f}$$

$$\Delta V_{CAP(BUCK)} = \frac{V_{OUT} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)}{8 \bullet L \bullet f^2 \bullet C_{OUT}}$$

The maximum steady ripple due to the voltage drop across the ESR is given by:

$$\Delta V_{ESR(BOOST)} = \frac{V_{OUT} \bullet I_{OUT(MAX)}}{V_{IN(MIN)}} \bullet ESR$$

$$\Delta V_{ESR(BUCK)} = \frac{V_{OUT} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)}{L \bullet f} \bullet ESR$$

$INTV_{CC}$ Regulator

An internal P-channel low dropout regulator produces 5V at the $INTV_{CC}$ pin from the V_{IN} supply pin. The $INTV_{CC}$ powers internal circuitry and gate drivers in the LT8390A. The $INTV_{CC}$ regulator can supply a peak current of 145mA and must be bypassed to ground with a minimum of 4.7µF ceramic capacitor. Good local bypass is necessary to supply the high transient current required by MOSFET gate drivers.

Higher input voltage applications with large MOSFETs being driven at higher switching frequencies may cause the maximum junction temperature rating for the LT8390A to be exceeded. The system supply current is normally dominated by the gate charge current. Additional external loading of the $INTV_{CC}$ also needs to be taken into account for the power dissipation calculation. The total LT8390A power dissipation in this case is $V_{IN} \bullet I_{INTVCC}$, and overall efficiency is lowered. The junction temperature can be estimated by using the equation:

$$T_J = T_A + P_D \bullet \theta_{JA}$$

where θ_{JA} (in °C/W) is the package thermal resistance.

To prevent maximum junction temperature from being exceeded, the input supply current must be checked operating in continuous mode at maximum V_{IN}.

Top Gate MOSFET Driver Supply (C_{BST1}, C_{BST2})

The top MOSFET drivers, TG1 and TG2, are driven between their respective SW and BST pin voltages. The boost voltages are biased from floating bootstrap capacitors C_{BST1} and C_{BST2}, which are normally recharged through both the external and internal bootstrap diodes when the respective top MOSFET is turned off. External bootstrap diodes are recommended because the internal bootstrap diodes are not always strong enough to refresh top MOSFETs at 2MHz. Both capacitors are charged to the same voltage as the $INTV_{CC}$ voltage. The bootstrap capacitors C_{BST1} and C_{BST2}, need to store about 100 times the gate charge required by the top switches A and D. In most applications, a 0.1µF to 0.47µF, X5R or X7R dielectric capacitor is adequate.

Programming V_{IN} UVLO

A resistor divider from V_{IN} to the EN/UVLO pin implements V_{IN} undervoltage lockout (UVLO). The EN/UVLO enable falling threshold is set at 1.220V with 13mV hysteresis. In addition, the EN/UVLO pin sinks 2.5µA when the voltage on the pin is below 1.220V. This current provides user programmable hysteresis based on the value of R1. The programmable UVLO thresholds are:

$$V_{IN(UVLO+)} = 1.233V \bullet \frac{R1+R2}{R2} + 2.5\mu A \bullet R1$$

$$V_{IN(UVLO-)} = 1.220V \bullet \frac{R1+R2}{R2}$$

Figure 12 shows the implementation of external shut-down control while still using the UVLO function. The NMOS grounds the EN/UVLO pin when turned on, and puts the LT8390A in shutdown with quiescent current less than 2µA.

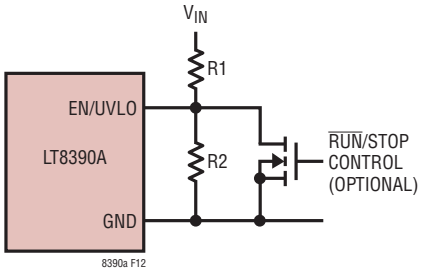

Figure 12. V_{IN} Undervoltage Lockout (UVLO)

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APPLICATIONS INFORMATION

Programming Input or Output Current Limit

The input or output current limit can be programmed by placing an appropriate value current sense resistor, R_{IS}, in the input or output power path. The voltage drop across R_{IS} is (Kelvin) sensed by the ISP and ISN pins. The CTRL pin should be tied to a voltage higher than 1.35V to get the full-scale 100mV (typical) threshold across the sense resistor. The CTRL pin can be used to reduce the current threshold to zero, although relative accuracy decreases with the decreasing sense threshold. When the CTRL pin voltage is between 0.3V and 1.15V, the current limit is:

$$I_{IS(MAX)} = \frac{V_{CTRL} - 0.25V}{10 \bullet R_{IS}}$$

When V_{CTRL} is between 1.15V and 1.35V the current limit varies with V_{CTRL}, but departs from the equation above by an increasing amount as V_{CTRL} increases. Ultimately, when V_{CTRL} is larger than 1.35V, the current limit no longer varies. The typical $V_{(ISP-ISN)}$ threshold vs V_{CTRL} is listed in Table 2.

Table 2. $V_{(ISP-ISN)}$ Threshold vs V_{CTRL}

V_{CTRL} (V)	$V_{(ISP-ISN)}$ (mV)
1.15	90
1.20	94.5
1.25	98
1.30	99.5
1.35	100

When V_{CTRL} is larger than 1.35V, the current threshold is regulated to:

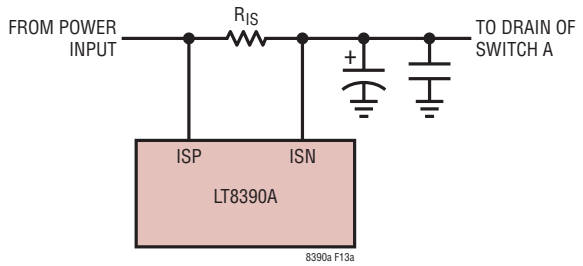
$$I_{IS(MAX)} = \frac{100mV}{R_{IS}}$$

The CTRL pin should not be left open (tie to V_{REF} if not used). The CTRL pin can also be used in conjunction with a thermistor to provide overtemperature protection for the output load, or with a resistor divider to V_{IN} to reduce output power and switching current when V_{IN} is low.

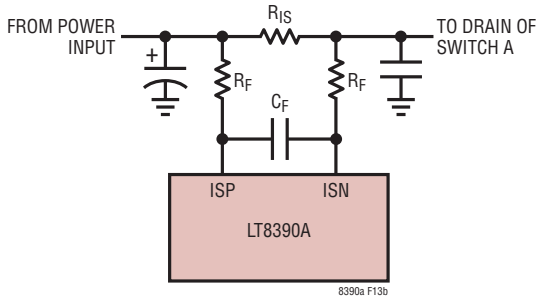
The presence of a time varying differential voltage ripple signal across the ISP and ISN pins at the switching frequency is expected. If the current sense resistor R_{IS} is placed between power input and input bulk capacitor (Figure 13a), or between output bulk capacitor and system output (Figure 14a), a filter is typically not necessary. If the R_{IS} is placed between input bulk capacitor and input decoupling capacitor (Figure 13b), or between output decoupling capacitor and output bulk capacitor (Figure 14b), a low pass filter formed by R_F and C_F is recommended to reduce the current ripple and stabilize the current loop. Since the bias currents of the ISP and ISN pins are matched, no offset is introduced by R_F. If input or output current limit is not used, the ISP and ISN pins should be shorted to V_{IN}, V_{OUT}, or ground.

ISMON Current Monitor

The ISMON pin provides a buffered monitor output of the current flowing through the ISP/ISN current sense resistor, R_{IS}. The V_{ISMON} voltage is calculated as $V_{(ISP-ISN)} \bullet 10 + 0.25V$. Since the ISMON pin has the same 0.25V offset as the CTRL pin, the master LT8390A ISMON pin can be directly tied to the slave LT8390A CTRL pin for equal current sharing in parallel applications.



(13a)



(13b)

Figure 13. Programming Input Current Limit

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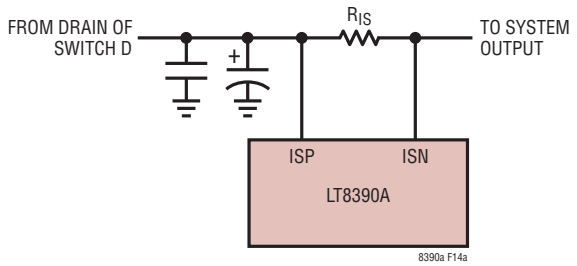
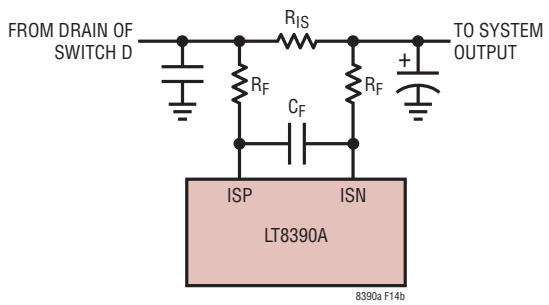


(14a)



(14b)

Figure 14. Programming Output Current Limit

Load Switch Control

The LOADEN and LOADTG pins provide high side PMOS load switch control. The LOADEN pin accepts a logic level ON/OFF signal and then drives the LOADTG pin to turn on or off the high side PMOS load switch, thereby connecting or disconnecting the LT8390A power output from the system output. When the LOADEN pin is forced low, the LT8390A turns off TG1 and TG2, turns on BG1 and BG2, disconnects the V_C pin from all internal loads, and turns off LOADTG. The LOADEN pin should not be left open (tie to $INTV_{CC}$ or V_{REF} if not used).

High Side PMOS Load Switch Selection

A high side PMOS load switch is recommended in some LT8390A applications requiring load switch control. The high side PMOS load switch is typically selected for drain-source voltage V_{DS}, gate-source threshold voltage $V_{GS(TH)}$, and continuous drain current I_D. For proper operations, V_{DS} rating should exceed the output regulation voltage set by the FB pin, the absolute value of $V_{GS(TH)}$ should be less than 3V, and I_D rating should be above $I_{OUT(MAX)}$.

Programming Output Voltage and Thresholds

The LT8390A has a voltage feedback pin FB that can be used to program a constant-voltage output. The output voltage can be set by selecting the values of R3 and R4 (Figure 15) according to the following equation:

$$V_{OUT} = 1V \bullet \frac{R3+R4}{R4}$$

In addition, the FB pin also sets output overvoltage threshold, output power good thresholds, and output short threshold. For an application with small output capacitors, the output voltage may overshoot a lot during

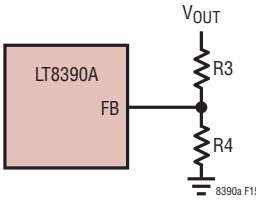


Figure 15. Feedback Resistor Connection

load transient event. Once the FB pin hits its overvoltage threshold 1.1V, the LT8390A stops switching by turning off TG1, BG1, TG2, and BG2, and also turns off LOADTG to disconnect the output load for protection. The output overvoltage threshold can be set as:

$$V_{OUT(OVP)} = 1.1V \bullet \frac{R3+R4}{R4}$$

To provide the output short-circuit detection and protection, the output short falling threshold can be set as:

$$V_{OUT(SHORT)} = 0.25V \bullet \frac{R3+R4}{R4}$$

Power GOOD ($\overline{PGOOD}$) Pin

The LT8390A provides an open-drain status pin, $\overline{PGOOD}$, which is pulled low when V_{FB} is within ±10% of the 1.00V regulation voltage. The $\overline{PGOOD}$ pin is allowed to be pulled up by an external resistor to $INTV_{CC}$ or an external voltage source of up to 6V.

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Soft-Start and Short-Circuit Protection

As shown in Figure 8 and explained in the Operation section, the SS pin can be used to program the output voltage soft-start by connecting an external capacitor from the SS pin to ground. The internal 12.5µA pull-up current charges up the capacitor, creating a voltage ramp on the SS pin. As the SS pin voltage rises linearly from 0.25V to 1V (and beyond), the output voltage rises smoothly into its final voltage regulation. The soft-start time can be calculated as:

$$t_{SS} = 1V \bullet \frac{C_{SS}}{12.5\mu A}$$

Make sure the C_{SS} is at least five to ten times larger than the compensation capacitor on the V_C pin for a well-controlled output voltage soft-start. A 22nF ceramic capacitor is a good starting point.

The SS pin is also used as a fault timer. Once an output short-circuit fault is detected, a 1.25µA pull-down current source is activated. Using a single resistor from the SS pin to the V_{REF} pin, the LT8390A can be set to three different fault protection modes: hiccup (no resistor), latch-off (499k), and keep-running (100k).

With a 100k resistor in keep-running mode, the LT8390A continues switching normally and regulates the current into ground. With a 499k resistor in latch-off mode, the LT8390A stops switching until the EN/UVLO pin is pulled low and high to restart. With no resistor in hiccup mode, the LT8390A enters low duty cycle auto-retry operation. The 1.25µA pull-down current discharges the SS pin to 0.2V and then 12.5µA pull-up current charges the SS pin up. If the output short-circuit condition has not been removed when the SS pin reaches 1.75V, the 1.25µA pull-down current turns on again, initiating a new hiccup cycle. This will continue until the fault is removed. Once the output short-circuit condition is removed, the output will have a smooth short-circuit recovery due to soft-start.

Loop Compensation

The LT8390A uses an internal transconductance error amplifier, the output of which, V_C, compensates the control loop. The external inductor, output capacitor, and the compensation resistor and capacitor determine the loop stability.

The inductor and output capacitor are chosen based on performance, size and cost. The compensation resistor and capacitor on the V_C pin are set to optimize control loop response and stability. For a typical voltage regulator application, a 2.2nF compensation capacitor on the V_C pin is adequate, and a series resistor should always be used to increase the slew rate on the V_C pin to maintain tighter output voltage regulation during fast transients on the input supply of the converter.

Efficiency Considerations

The power efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Although all dissipative elements in circuits produce losses, four main sources account for most of the losses in LT8390A circuits:

1. DC I^2R losses. These arise from the resistances of the MOSFETs, sensing resistor, inductor and PC board traces and cause the efficiency to drop at high output currents.
2. Transition loss. This loss arises from the brief amount of time switch A or switch C spends in the saturated region during switch node transitions. It depends upon the input voltage, load current, driver strength and MOSFET capacitance, among other factors.
3. $INTV_{CC}$ current. This is the sum of the MOSFET driver and control currents.
4. C_{IN} and C_{OUT} loss. The input capacitor has the difficult job of filtering the large RMS input current to the regulator in buck region. The output capacitor has the difficult job of filtering the large RMS output current in boost region. Both C_{IN} and C_{OUT} are required to have low ESR to minimize the AC I^2R loss and sufficient capacitance to prevent the RMS current from causing additional upstream losses in fuses or batteries.

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APPLICATIONS INFORMATION

5. Other losses. Schottky diode D_B and D_D are responsible for conduction losses during dead time and light load conduction periods. Inductor core loss occurs predominately at light loads. Switch A causes reverse recovery current loss in buck region, and switch C causes reverse recovery current loss in boost region.

   When making adjustments to improve efficiency, the input current is the best indicator of changes in efficiency. If you make a change and the input current decreases, then the efficiency has increased. If there is no change in the input current, then there is no change in efficiency.

PC Board Layout Checklist

The basic PC board layout requires a dedicated ground plane layer. Also, for high current, a multilayer board provides heat sinking for power components.

- The ground plane layer should not have any traces and it should be as close as possible to the layer with power MOSFETs.
- Place C_{IN}, switch A, switch B and D_B in one compact area. Place C_{OUT}, switch C, switch D and D_D in one compact area.
- Use immediate vias to connect the components to the ground plane. Use several large vias for each power component.
- Use planes for V_{IN} and V_{OUT} to maintain good voltage filtering and to keep power losses low.
- Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. Connect the copper areas to any DC net (V_{IN} or GND).
- Separate the signal and power grounds. All small-signal components should return to the exposed GND pad from the bottom, which is then tied to the power GND close to the sources of switch B and switch C.
- Place switch A and switch C as close to the controller as possible, keeping the PGND, BG and SW traces short.
- Keep the high dV/dT SW1, SW2, BST1, BST2, TG1 and TG2 nodes away from sensitive small-signal nodes.
- The path formed by switch A, switch B, D_B and the C_{IN} capacitor should have short leads and PCB trace lengths. The path formed by switch C, switch D, D_D and the C_{OUT} capacitor also should have short leads and PCB trace lengths.
- The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor.
- Connect the top driver bootstrap capacitor C_{BST1} closely to the BST1 and SW1 pins. Connect the top driver bootstrap capacitor C_{BST2} closely to the BST2 and SW2 pins.
- Connect the input capacitors C_{IN} and output capacitors C_{OUT} closely to the power MOSFETs. These capacitors carry the MOSFET AC current.
- Route LSP and LSN traces together with minimum PCB trace spacing. Avoid sense lines pass through noisy areas, such as switch nodes. The filter capacitor between LSP and LSN should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the R_{SENSE} resistor. Low ESL sense resistor is recommended.
- Connect the V_C pin compensation network close to the IC, between V_C and the signal ground. The capacitor helps to filter the effects of PCB noise and output voltage ripple voltage from the compensation loop.
- Connect the $INTV_{CC}$ bypass capacitor, C_{INTVCC}, close to the IC, between the $INTV_{CC}$ and the power ground. This capacitor carries the MOSFET drivers' current peaks.

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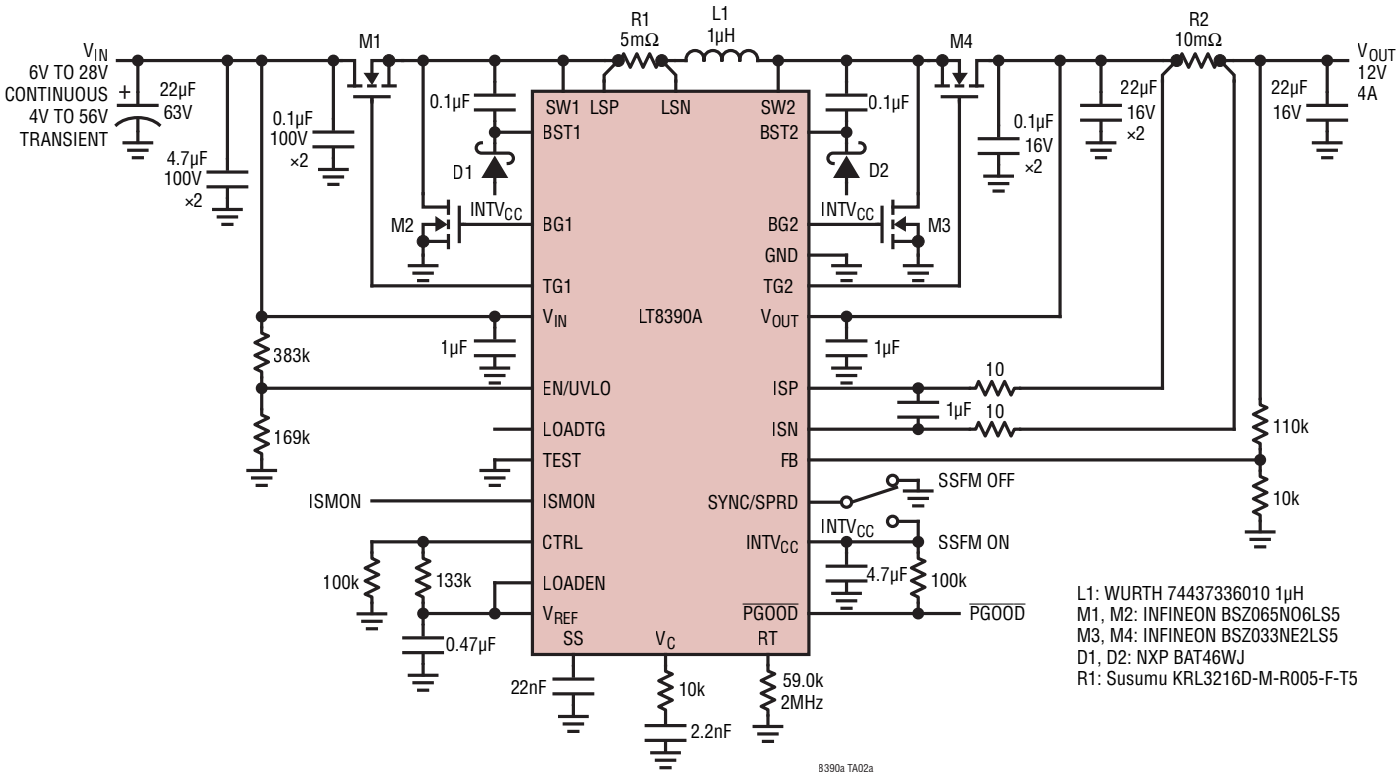
TYPICAL APPLICATIONS

95% Efficient 48W (12V 4A) 2MHz Buck-Boost Voltage Regulator



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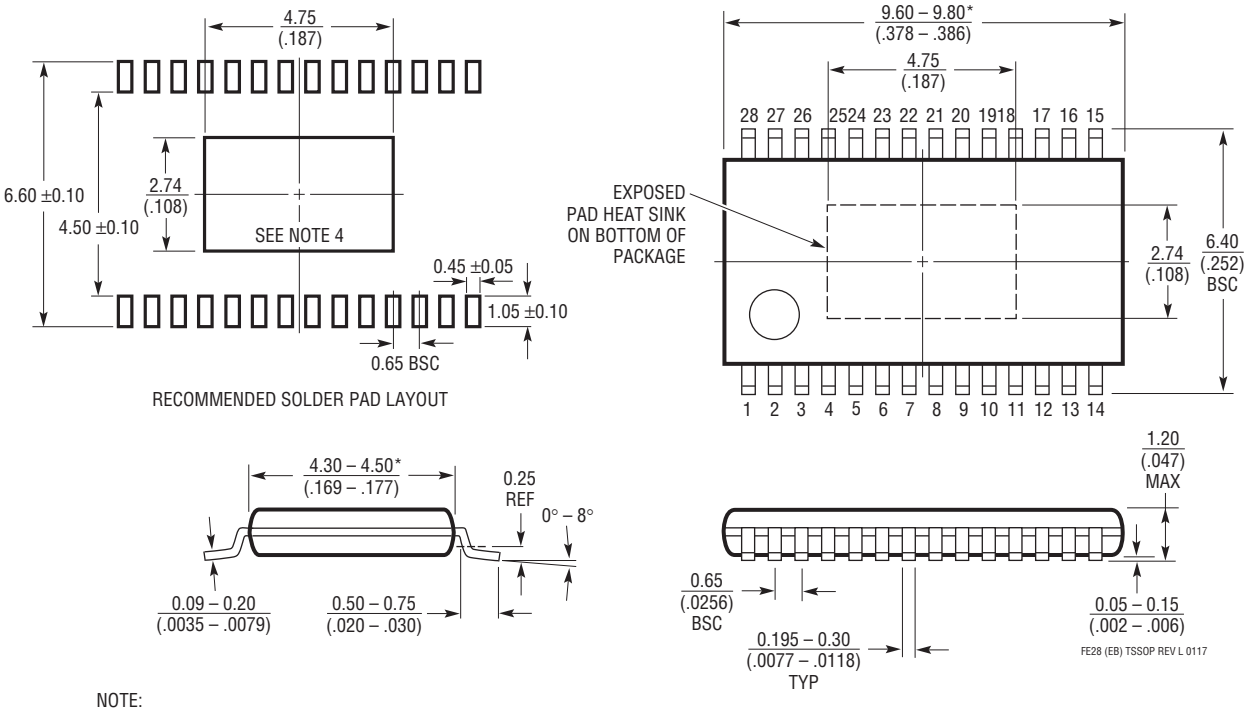
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT8390A#packaging for the most recent package drawings.

FE Package
28-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev L)
Exposed Pad Variation EB



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

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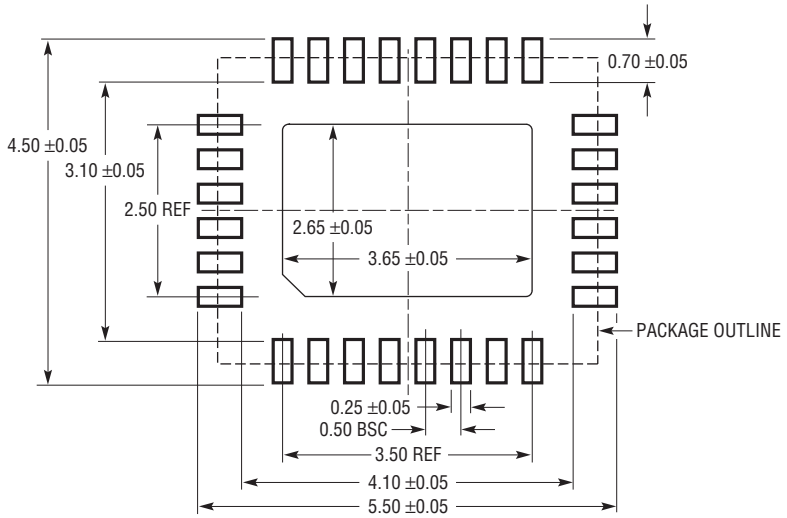
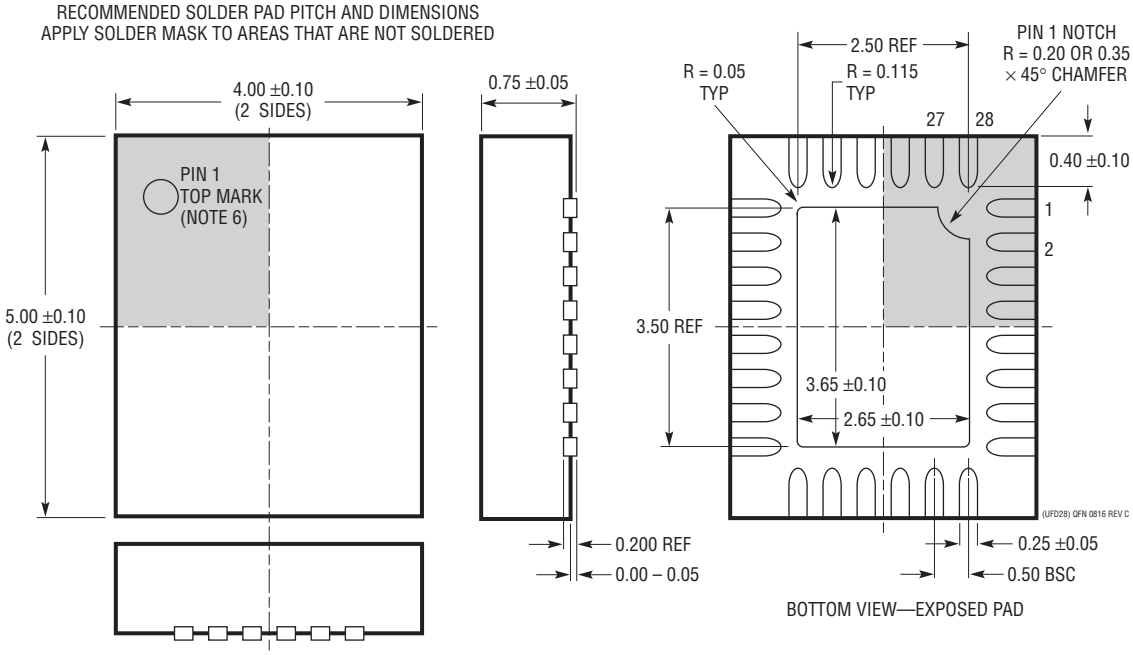
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT8390A#packaging for the most recent package drawings.

UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGHD-3).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

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REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	09/17	Added H-Grade Temperature Option	2, 5
		Clarified Block Diagram	11
		Clarified Sense Resistors descriptiion in Route LSP and LSN traces bullet	25

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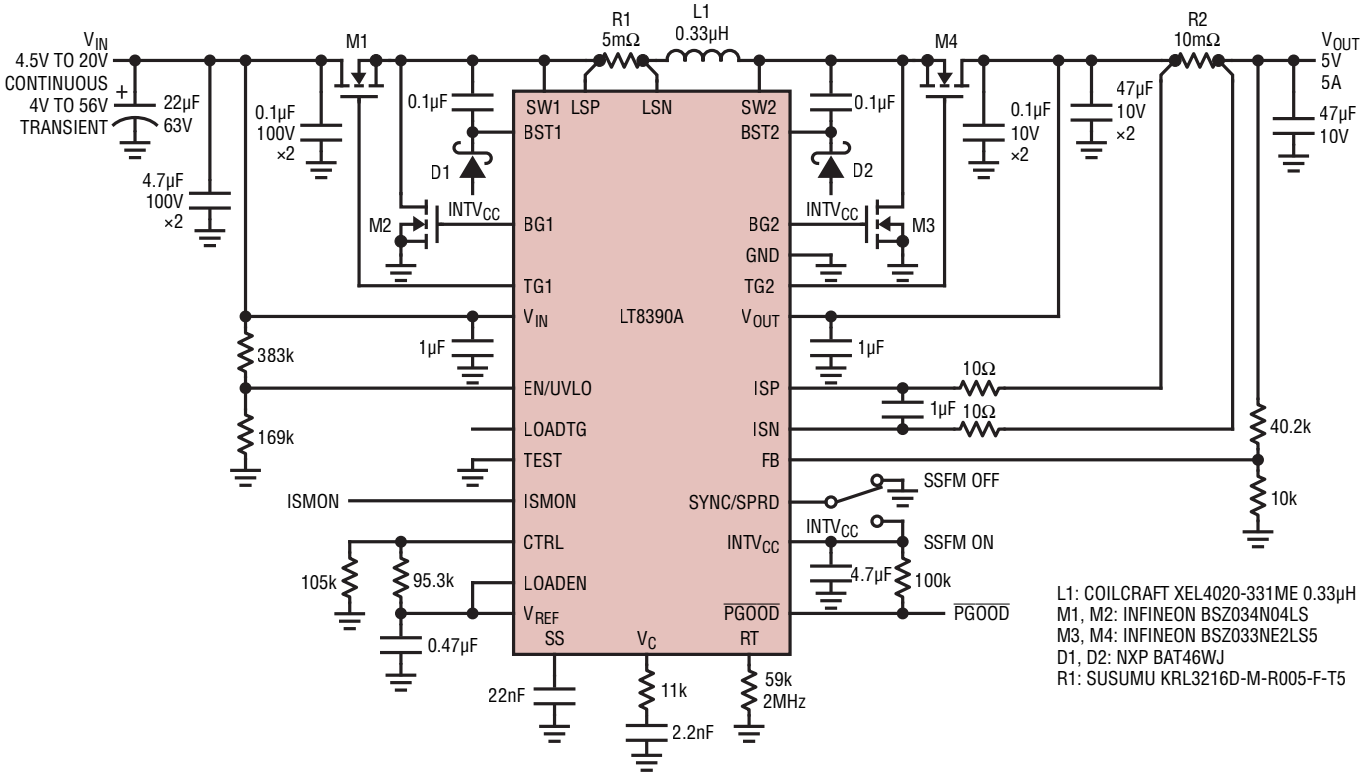
TYPICAL APPLICATION

25W (5V 5A) 2MHz Buck-Boost Voltage Regulator



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT8390	60V Synchronous 4-Switch Buck-Boost Controller with Spread Spectrum	V_{IN}: 4V to 60V, V_{OUT}: 0V to 60V, ±1.5% Voltage Accuracy, ±3% Current Accuracy, TSSOP-28 and 4mm × 5mm QFN-28
LT8391	60V Synchronous 4-Switch Buck-Boost LED Controller with Spread Spectrum	V_{IN}: 4V to 60V, V_{OUT}: 0V to 60V, ±1.5% Voltage Accuracy, ±3% Current Accuracy, TSSOP-28 and 4mm × 5mm QFN-28
LT8391A	60V Synchronous 2MHz 4-Switch Buck-Boost LED Controller with Spread Spectrum	V_{IN}: 4V to 60V, V_{OUT}: 0V to 60V, ±1.5% Voltage Accuracy, ±3% Current Accuracy, TSSOP-28 and 4mm × 5mm QFN-28
LT3790	60V Synchronous 4-Switch Buck-Boost Controller	V_{IN}: 4.7V to 60V, V_{OUT}: 1.2V to 60V, Regulates V_{OUT}, I_{OUT}, I_{IN}, TSSOP-38
LT8705	80V V_{IN} and V_{OUT} Synchronous 4-Switch Buck-Boost DC/DC Controller	V_{IN}: 2.8V to 80V, V_{OUT}: 1.3V to 80V, Regulates V_{OUT}, I_{OUT}, V_{IN}, I_{IN}, 5mm × 7mm QFN-38 and Modified TSSOP-38 for High Voltage
LTC®3789	High Efficiency Synchronous 4-Switch Buck-Boost Controller	V_{IN}: 4V to 38V, V_{OUT}: 0.8V to 38V, Regulates V_{OUT}, I_{OUT} or I_{IN}, 5mm × 5mm QFN-32 and SSOP-24
LTC3780	High Efficiency Synchronous 4-Switch Buck-Boost Controller	V_{IN}: 4V to 36V, V_{OUT}: 0.8V to 30V, Regulates V_{OUT}, 4mm × 5mm QFN-28 and SSOP-28
LT3763	60V High Current Step-Down LED Driver Controller	V_{IN}: 6V to 60V, 4mm × 4mm QFN-20 and TSSOP-20
LT3757/LT3757A	Boost, Flyback, SEPIC and Inverting Controller	V_{IN}: 2.9V to 40V, Positive or Negative V_{OUT}, 3mm × 3mm DFN-10, MSOP-10
LT3758	High Input Voltage, Boost, Flyback, SEPIC and Inverting Controller	V_{IN}: 5.5V to 100V, Positive or Negative V_{OUT}, 3mm × 3mm DFN-10, MSOP-10
LT8710	Synchronous SEPIC/Inverting/Boost Controller with Output Current Control	V_{IN}: 4.5V to 80V, Rail-to-Rail Output Current Monitor and Control, TSSOP-28

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