Features

- Four independent clock channels
- Frequency and Phase Sync over Packet Networks
  - Frequency accuracy performance for WCDMA-FDD, GSM, LTE-FDD and femtocell applications
  - Frequency performance for ITU-T G.823 and G.824 synchronization interface, as well as G.8261 PNT PEC and CES interfaces
  - Phase Synchronization performance for WCDMA-TDD, Mobile WiMAX, TD-SCDMA and CDMA2000 applications
- Client holdover and reference switching between multiple Servers
- Physical Layer Equipment Clocks Synchronization
  - ITU-T G.8262 for SyncE EEC option 1 & 2
  - ITU-T G.813 for SONET/SDH SEC option 1 & 2
- Telcordia GR-1244 & GR-253 Stratum 3 & SMC
- Support for G.781 SETS

Ordering Information

ZL30362GDG2 144 Pin LBGA Trays
Pb Free Tin/Silver/Copper
-40°C to +85°C
Package size: 13 x 13 mm

- Any input clock rate from 1 Hz to 750 MHz
- Automatic hitless reference switching and digital holdover on reference fail
- Flexible two-stage architecture translates between arbitrary data, line coding and FEC rates
- Digital PLLs programmable bandwidth from 0.1 MHz up to 1 kHz
- Programmable synthesizers
  - Any output clock rate from 1 Hz to 750 MHz
  - Output jitter below 0.61 ps rms
- Operates from a single crystal resonator or clock oscillator
- Field configurable via SPI/i2C interface

Figure 1 - Functional Block Diagram
Detailed Features

General

• Four independent clock channels
• Operates from a single crystal resonator or clock oscillator
• Configurable its SPI/I2C interface

Time Synchronization Algorithm

• External algorithm controls software digital PLL to adjust frequency & phase alignment
• Frequency, Phase and Time Synchronization over IP, MPLS and Ethernet Packet Networks
• Frequency accuracy performance for WCDMA-FDD, GSM, LTE-FDD and femtocell applications, with target performance less than ± 15 ppb.
• Frequency performance for ITU-T G.823 and G.824 synchronization interface, as well as G.8261 PNT EEC, PNT PEC and CES interface specifications.
• Phase Synchronization performance for WCDMA-TDD, Mobile WiMAX, TD-SCDMA and CDMA2000 applications with target performance less than ± 1 µs phase alignment.
• Time Synchronization for UTC-traceability and GPS replacement.
• Client reference switching between multiple Servers
• Client holdover when Server packet connectivity is lost

Electrical Clock Inputs

• Nine input references configurable as single ended or differential and two single ended input references
• Synchronize to any clock rate from 1 Hz to 750 MHz on differential inputs
• Synchronize to any clock rate from 1 Hz to 177.75 MHz on single-ended inputs
• Any input reference can be fed with sync (frame pulse) or clock.
• Synchronize to sync pulse and sync pulse/clock pair.
• Flexible input reference monitoring automatically disqualifies references based on frequency and phase irregularities
  • LOS
  • Single cycle monitor
  • Precise frequency monitor
  • Coarse frequency monitor
  • Guard soak timer
• Per input clock delay compensation

Electrical Clock Engine

• Digital PLLs filter jitter from 0.1 mHz up to 1 kHz
• Flexible two-stage architecture translates between arbitrary data rates, line coding rates and FEC rates
• Internal state machine automatically controls mode of operation (free-run, locked, holdover)
• Automatic hitless reference switching and digital holdover on reference fail
  • Physical-to-physical reference switching
• Physical-to-packet reference switching
• Packet-to-physical reference switching
• Packet-to-packet reference switching
• Support for wide variety of Equipment Clock specifications
  • SyncE
    • ITU-T G.8262 option 1 EEC (Europe/China)
    • ITU-T G.8262 option 2 (USA)
  • SONET/SDH
    • ITU-T G.813 option 1 SEC (Europe/China)
    • ITU-T G.813 option 2 (USA)
    • ANSI T1.105/Telcordia GR-253 Stratum 3 for SONET
    • Telcordia GR-253 SMC
  • PDH
    • ITU-T G.812 Type I SSU
    • ITU-T G.812 Type III, ANSI T1.101/Telcordia GR-1244 Stratum 3E, including phase build out
    • ANSI T1.101/Telcordia GR-1244 Stratum 3
    • ANSI T1.101/Telcordia GR-1244 Stratum 4E/4
• Selectable phase slope limiting
• Holdover better than 1 ppb (when using < 0.1 Hz filter)
• Supports ITU-T G.823, G.824 and G.8261 for 2048 kbit/s and 1544 kbit/s interfaces
• Supports G.781 SETS

Electrical Clock Generation
• Four programmable synthesizers
• Eight LVPECL outputs
  • Two LVPECL outputs per synthesizer
  • Generate any clock rate from 1 Hz to 750 MHz
  • Maximum jitter below 0.61 ps RMS
  • Meets OC-192, STM-64, 1 GbE & 10 GbE interface jitter requirements
• Eight LVCMOS outputs
  • Two LVCMOS outputs per synthesizer
  • Generate any clock rate from 1 Hz to 177.75 MHz
  • Maximum jitter below 1 ps rms
• Programmable output advancement/delay to accommodate trace delays or compensate for system routing paths
• Outputs may be disabled to save power

API Software
• Interfaces to 1588-capable PHY and switches with integrated timestamping
• Abstraction layer for independence from OS and CPU, from embedded SoC to home-grown
• Fits into centralized, highly integrated pizza box architectures as well as distributed architectures with multiple line cards and timing cards
Applications

- ITU-T G.8262 System Timing Cards which support 1 GbE and 10 GbE interfaces
- Telcordia GR-253 Carrier Grade SONET/SDH Stratum 3 System Timing Cards
- System Timing Cards which supports ITU-T G.781 SETS (SDH Equipment Timing Source)
- Integrated basestation reference clock for air interface for GSM, WCDMA, LTE and WiMAX macro, micro or femtocells
- Mobile Backhaul NID, edge router or access aggregation node
- EPON/GE-PON & GPON OLT
- EPON/GE-PON & GPON ONU/OLT
- DSLAM and RT-DSLAM
- 10 Gigabit line cards
- Synchronous Ethernet, 10 GBASE-R and 10 GBASE-W
- SONET/SDH, Fibre Channel, XAUI