FSA4480

USB Type-C Analog Audio Switch with Protection Function

FSA4480 is a high performance USB Type−C port multimedia switch which supports analog audio headsets. FSA4480 allows the sharing of a common USB Type−C port to pass USB2.0 signal, analog audio, sideband use wires and analog microphone signal. FSA4480 also supports high voltage on SBU port and USB port on USB Type−C receptacle side.

Features

- Power Supply: VCC, 2.7 V to 5.5 V
- USB High Speed (480 Mbps) Switch:
  - SDD21 −3dB bandwidth: 950 MHz
  - 3 Ω RON Typical
- Audio Switch
  - Negative Rail Capability: −3 V to +3 V
  - THD+N = −110 dB; 1 VRMS, f = 20 Hz ~ 20 kHz, 32 W Load
  - 1 Ω RON Typical
- High Voltage Protection
  - 20 V DC Tolerance on Connector Side Pins
  - Over Voltage Protection: VTH = 5 V (Typ)
- OMTP and CTIA Pinout Support
- Support Audio Sense Path
- 25−Ball WLCSP Package (2.24 mm x 2.28 mm)

Applications

- Mobile Phone, Tablet, Notebook PC, Media Player

Figure 1. Application Block Diagram
PIN CONFIGURATION

Figure 2. Pin Assignment (Top Through View)

A

B

C

D

E

1  2  3  4  5

SBU1_H  SBU2  SBU1  ENN  VCC

SBU2_H  AGND  AGND  ADDR  GND

MIC  DET  INT  L  R

GSBU1  CC_IN  SCL  DN_L  DP_R

GSBU2  SENSE  SDA  DN  DP
<table>
<thead>
<tr>
<th>No.</th>
<th>Pin</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>A5</td>
<td>VCC</td>
<td>Power Supply (2.7 to 5.5 V)</td>
</tr>
<tr>
<td>2</td>
<td>B5</td>
<td>GND</td>
<td>Chip ground</td>
</tr>
<tr>
<td>3</td>
<td>D5</td>
<td>DP_R</td>
<td>USB/Audio Common Connector</td>
</tr>
<tr>
<td>4</td>
<td>D4</td>
<td>DN_L</td>
<td>USB/Audio Common Connector</td>
</tr>
<tr>
<td>5</td>
<td>E5</td>
<td>DP</td>
<td>USB Data (Differential +)</td>
</tr>
<tr>
<td>6</td>
<td>E4</td>
<td>DN</td>
<td>USB Data (Differential –)</td>
</tr>
<tr>
<td>7</td>
<td>C5</td>
<td>R</td>
<td>Audio – Right Channel</td>
</tr>
<tr>
<td>8</td>
<td>C4</td>
<td>L</td>
<td>Audio – Left Channel</td>
</tr>
<tr>
<td>9</td>
<td>A3</td>
<td>SBU1</td>
<td>Sideband use wire 1</td>
</tr>
<tr>
<td>10</td>
<td>A2</td>
<td>SBU2</td>
<td>Sideband use wire 2</td>
</tr>
<tr>
<td>11</td>
<td>C1</td>
<td>MIC</td>
<td>Microphone signal</td>
</tr>
<tr>
<td>12</td>
<td>B2</td>
<td>AGND</td>
<td>Audio signal ground</td>
</tr>
<tr>
<td>13</td>
<td>B3</td>
<td>AGND</td>
<td>Audio signal ground</td>
</tr>
<tr>
<td>14</td>
<td>E2</td>
<td>SENSE</td>
<td>Audio ground reference output</td>
</tr>
<tr>
<td>15</td>
<td>C3</td>
<td>INT</td>
<td>I^2C Interrupt output, active low (open drain)</td>
</tr>
<tr>
<td>16</td>
<td>D2</td>
<td>CC_IN</td>
<td>Audio accessory attachment detection input</td>
</tr>
<tr>
<td>17</td>
<td>D1</td>
<td>GSBU1</td>
<td>Audio sense path 1 to headset jack GND</td>
</tr>
<tr>
<td>18</td>
<td>E1</td>
<td>GSBU2</td>
<td>Audio sense path 2 to headset jack GND</td>
</tr>
<tr>
<td>19</td>
<td>C2</td>
<td>DET</td>
<td>Push–pull output. When CC_IN &gt; 1.5 V, DET is low and CC_IN &lt; 1.2 V, DET is high</td>
</tr>
<tr>
<td>20</td>
<td>D3</td>
<td>SCL</td>
<td>I^2C clock</td>
</tr>
<tr>
<td>21</td>
<td>E3</td>
<td>SDA</td>
<td>I^2C data</td>
</tr>
<tr>
<td>22</td>
<td>B1</td>
<td>SBU2_H</td>
<td>Host Side Sideband Use Wire 2</td>
</tr>
<tr>
<td>23</td>
<td>A1</td>
<td>SBU1_H</td>
<td>Host Side Sideband Use Wire 1</td>
</tr>
<tr>
<td>24</td>
<td>A4</td>
<td>ENN</td>
<td>Chip Enable, active low, internal pull–down by 470 kΩ</td>
</tr>
<tr>
<td>25</td>
<td>B4</td>
<td>ADDR</td>
<td>I^2C slave address pin</td>
</tr>
</tbody>
</table>
### Table 2. ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>Supply Voltage from VCC</td>
<td>−0.5</td>
<td>6.5</td>
<td>V</td>
</tr>
<tr>
<td>$V_{CC_IN}$</td>
<td>$V_{CC_IN}$, to GND</td>
<td>−0.5</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>$V_{SW_C}$</td>
<td>$V_{DP_R}$ to GND, $V_{DN_L}$ to GND</td>
<td>−3.5</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>$V_{SW_USB}$</td>
<td>$V_{DP}$ to GND, $V_{DN}$ to GND</td>
<td>−0.5</td>
<td>6.5</td>
<td>V</td>
</tr>
<tr>
<td>$V_{SW_Audio}$</td>
<td>$V_{L}$ to GND, $V_{R}$ to GND</td>
<td>−0.5</td>
<td>6.5</td>
<td>V</td>
</tr>
<tr>
<td>$V_{V_SBU/GSBU}$</td>
<td>$V_{SBU1}$ to GND, $V_{SBU2}$ to GND, $V_{GSBU1}$ to GND, $V_{GSBU1}$ to GND</td>
<td>−0.5</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>$V_{V_SBU_H}$</td>
<td>$V_{SBU1_H}$ to GND, $V_{SBU2_H}$ to GND</td>
<td>−0.5</td>
<td>6.5</td>
<td>V</td>
</tr>
<tr>
<td>$V_{I/O}$</td>
<td>SENSE, MIC, DET, INT, to GND</td>
<td>−0.5</td>
<td>6.5</td>
<td>V</td>
</tr>
<tr>
<td>$V_{CNTRL}$</td>
<td>Control Input Voltage SDA, SCL, ENN, ADDR</td>
<td>−0.5</td>
<td>6.5</td>
<td>V</td>
</tr>
<tr>
<td>$I_{SW_Audio}$</td>
<td>Switch I/O Current, Audio Path</td>
<td>−250</td>
<td>250</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{SW_USB}$</td>
<td>Switch I/O Current, USB Path</td>
<td>−</td>
<td>100</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{SW_MIC}$</td>
<td>Switch I/O Current, MIC to SBU1 or SBU2</td>
<td>−</td>
<td>50</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{SW_SBU}$</td>
<td>Switch I/O Current, SBUx to SBUx H</td>
<td>−</td>
<td>50</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{SW_SENSE}$</td>
<td>Switch I/O Current, SENSE to GSBU1 or GSBU2</td>
<td>−</td>
<td>100</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{SW_AGND}$</td>
<td>Switch I/O Current, AGND to SBU1 or SBU2</td>
<td>−</td>
<td>500</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{IK}$</td>
<td>DC Input Diode Current</td>
<td>−50</td>
<td>−</td>
<td>mA</td>
</tr>
<tr>
<td>ESD</td>
<td>Human Body Model, ANSI/ESDA/JEDEC JS−001−2012 Connector side and power pins: VCC, SBU1, SBU2, DP_R, DN_L, GSBU1, GSBU2, CC_IN</td>
<td>4</td>
<td>−</td>
<td>kV</td>
</tr>
<tr>
<td>ESD</td>
<td>Human Body Model, ANSI/ESDA/JEDEC JS−001−2012 Host side pins: the rest pins</td>
<td>2</td>
<td>−</td>
<td>kV</td>
</tr>
<tr>
<td>ESD</td>
<td>Charged Device Model, JEDEC: JESD22−C101</td>
<td>1</td>
<td>−</td>
<td>kV</td>
</tr>
<tr>
<td>$T_{A}$</td>
<td>Absolute Maximum Operating Temperature</td>
<td>−40</td>
<td>85</td>
<td>°C</td>
</tr>
<tr>
<td>$T_{STG}$</td>
<td>Storage Temperature</td>
<td>−65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
### Table 3. RECOMMENDED OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>POWER</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>Supply Voltage</td>
<td>2.7</td>
<td>–</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td><strong>USB SWITCH</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VSW_USB</td>
<td>VDP to GND, VDN to GND, VDP_R to GND, VDN_L to GND</td>
<td>0</td>
<td>–</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td><strong>AUDIO SWITCH</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VSW_Audio</td>
<td>VDP_R to GND, VDN_L to GND, VL to GND, VR to GND</td>
<td>–3.6</td>
<td>–</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td><strong>MIC SWITCH</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VSBU_MIC</td>
<td>VSBU1 to GND, VSBU2 to GND, VMIC to GND</td>
<td>0</td>
<td>–</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td><strong>SENSE SWITCH</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VGSBU_SEN</td>
<td>VGSBU1 to GND, VGSBU2 to GND, VSENSE to GND</td>
<td>0</td>
<td>–</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td><strong>SBU TO SBUX_H SWITCH</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VGSBU</td>
<td>VSBU1 to GND, VSBU2 to GND, VSBU1_H to GND, VSBU2_H to GND</td>
<td>0</td>
<td>–</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td><strong>CC_IN PIN</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCC_IN</td>
<td>VCC_IN, to GND</td>
<td>0</td>
<td>–</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td><strong>CONTROL VOLTAGE (ENN/SDA/SCL)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIH</td>
<td>Input Voltage High</td>
<td>1.3</td>
<td>–</td>
<td>VCC</td>
<td>V</td>
</tr>
<tr>
<td>VIL</td>
<td>Input Voltage Low</td>
<td>–</td>
<td>–</td>
<td>0.5</td>
<td>V</td>
</tr>
<tr>
<td><strong>OPERATING TEMPERATURE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TA</td>
<td>Ambient Operating Temperature</td>
<td>–40</td>
<td>25</td>
<td>+85</td>
<td>°C</td>
</tr>
</tbody>
</table>

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
Table 4. DC ELECTRICAL CHARACTERISTICS
(VCC = 2.7 V to 5.5 V, VCC (Typ.) = 3.3 V, TA = −40°C to 85°C, and TA (Typ.) = 25°C, unless otherwise specified.)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Power</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICC</td>
<td>Supply Current</td>
<td>USB switches on, SBUx to SBUx_H switches on</td>
<td>VCC: 2.7 V to 5.5 V</td>
<td>–</td>
<td>–</td>
<td>65</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Audio switches on, MIC switch on and Audio GND switch on</td>
<td>–</td>
<td>–</td>
<td>60</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>ICCZ</td>
<td>Quiescent Current</td>
<td>ENN = L, 04H'b7 = 0</td>
<td>–</td>
<td>–</td>
<td>5</td>
<td>µA</td>
<td></td>
</tr>
</tbody>
</table>

**USB/AUDIO COMMON PINS: DP/R, DN_L**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Power</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>IOZ</td>
<td>Off Leakage Current of DP_R and DN_L</td>
<td>DN_L, DP_R = −3 V to 3.6 V</td>
<td>VCC: 2.7 V to 5.5 V</td>
<td>−3.0</td>
<td>–</td>
<td>3.0</td>
<td>µA</td>
</tr>
<tr>
<td>IOFF</td>
<td>Power–Off Leakage Current of DP_R and DN_L</td>
<td>DN_L, DP_R = 0 V to 3.6 V</td>
<td>Power off</td>
<td>–3.0</td>
<td>–</td>
<td>3.0</td>
<td>µA</td>
</tr>
<tr>
<td>VOV_TRIP</td>
<td>Input OVP Lockout</td>
<td>Rising edge</td>
<td>VCC: 2.7 V to 5.5 V</td>
<td>4.5</td>
<td>5</td>
<td>5.3</td>
<td>V</td>
</tr>
<tr>
<td>VOV_HYS</td>
<td>Input OVP Hysteresis</td>
<td>–</td>
<td>0.3</td>
<td>–</td>
<td>V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**AUDIO SWITCH**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Power</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>ION</td>
<td>On Leakage Current of Audio Switch</td>
<td>DN_L, DP_R = −3 V to 3.0 V, DP, DN, R, L = Float</td>
<td>VCC: 2.7 V to 5.5 V</td>
<td>−2.5</td>
<td>–</td>
<td>2.5</td>
<td>µA</td>
</tr>
<tr>
<td>IOFF</td>
<td>Power–Off Leakage Current of L and R</td>
<td>L, R = 0 V to 3 V; DP_R, DN_L = Float</td>
<td>Power off</td>
<td>−1.0</td>
<td>–</td>
<td>1.0</td>
<td>µA</td>
</tr>
<tr>
<td>RON</td>
<td>Switch On Resistance</td>
<td>ISW = 100 mA, VSW = −3 V to 3 V</td>
<td>VCC: 2.7 V to 5.5 V</td>
<td>–</td>
<td>1</td>
<td>–</td>
<td>Ω</td>
</tr>
<tr>
<td>RSHUNT</td>
<td>Pull Down Resistor on R/L Pin when Audio Switch is Off</td>
<td>L = R = 3 V</td>
<td>6</td>
<td>10</td>
<td>14</td>
<td>kΩ</td>
<td></td>
</tr>
</tbody>
</table>

**USB SWITCH**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Power</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>ION</td>
<td>On Leakage Current of USB Switch</td>
<td>DN_L, DP_R = 0 V to 3.6 V, DP, DN, R, L = Float</td>
<td>VCC: 2.7 V to 5.5 V</td>
<td>−3.0</td>
<td>–</td>
<td>3.0</td>
<td>µA</td>
</tr>
<tr>
<td>IOZ</td>
<td>Off Leakage Current of DP and DN</td>
<td>DN, DP = 0 V to 3.6 V</td>
<td>–3.0</td>
<td>–</td>
<td>3.0</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>IOFF</td>
<td>Power–Off Leakage Current of DP and DN</td>
<td>DN, DP = 0 V to 3.6 V</td>
<td>Power off</td>
<td>−3.0</td>
<td>–</td>
<td>3.0</td>
<td>µA</td>
</tr>
<tr>
<td>RON_USB</td>
<td>USB Switch On Resistance</td>
<td>ISW = 8 mA, VSW = 0.4 V</td>
<td>VCC: 2.7 V to 5.5 V</td>
<td>–</td>
<td>3</td>
<td>–</td>
<td>Ω</td>
</tr>
</tbody>
</table>

**SENSE SWITCH**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Power</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>ION</td>
<td>Sense Path Leakage Current</td>
<td>GSBUX = 0 V to 1 V, SENSE is floating</td>
<td>VCC: 2.7 V to 5.5 V</td>
<td>−2.0</td>
<td>–</td>
<td>2.0</td>
<td>µA</td>
</tr>
<tr>
<td>RON</td>
<td>SENSE Switch On Resistance</td>
<td>IOUT = 100 mA, VSW = 1 V</td>
<td>VCC: 2.7 V to 5.5 V</td>
<td>–</td>
<td>300</td>
<td>–</td>
<td>mΩ</td>
</tr>
<tr>
<td>IOZ</td>
<td>Off Leakage Current of SENSE</td>
<td>Sense = 0 V to 1.0 V</td>
<td>–2.0</td>
<td>–</td>
<td>2.0</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Off Leakage Current of GSBUX</td>
<td>GSBUX = 0 V to 1.0 V</td>
<td>–2.0</td>
<td>–</td>
<td>2.0</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>GSBUX = 1 V to 3.6 V</td>
<td>GSBUX = 1 V to 3.6 V</td>
<td>−3.0</td>
<td>–</td>
<td>3.0</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>IOFF</td>
<td>Power–Off Leakage Current of SENSE</td>
<td>Sense = 0 V to 1.0 V</td>
<td>Power off</td>
<td>−2.0</td>
<td>–</td>
<td>2.0</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>Power–Off Leakage Current of GSBUX</td>
<td>GSBUX = 0 V to 3.6 V</td>
<td>Power off</td>
<td>−3.0</td>
<td>–</td>
<td>3.0</td>
<td>µA</td>
</tr>
</tbody>
</table>
Table 4. DC ELECTRICAL CHARACTERISTICS (continued)
(VCC = 2.7 V to 5.5 V, VCC (Typ.) = 3.3 V, TA = −40°C to 85°C, and TA (Typ.) = 25°C, unless otherwise specified.)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Power Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SENSE SWITCH</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VOV_TRIP</td>
<td>Input OVP Lockout on GSBUx</td>
<td>Rising edge</td>
<td>VCC: 2.7 V to 5.5 V</td>
<td>4.5</td>
<td>5</td>
<td>5.3</td>
<td>V</td>
</tr>
<tr>
<td>VOV_HYS</td>
<td>Input OVP Hysteresis of GSBUx</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>SBUX PINS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IOZ</td>
<td>Off Leakage Current of SBUx</td>
<td>SBUx = 0 V to 3.6 V</td>
<td>VCC: 2.7 V to 5.5 V</td>
<td>−3.0</td>
<td>−</td>
<td>3.0</td>
<td>μA</td>
</tr>
<tr>
<td>IOFF</td>
<td>Power−Off Leakage Current Port SBUx</td>
<td>SBUx = 0 V to 3.6 V</td>
<td>Power off</td>
<td>−3.0</td>
<td>−</td>
<td>3.0</td>
<td>μA</td>
</tr>
<tr>
<td>VOV_TRIP</td>
<td>Input OVP Lockout</td>
<td>Rising edge</td>
<td>VCC: 2.7 V to 5.5 V</td>
<td>4.5</td>
<td>5</td>
<td>5.3</td>
<td>V</td>
</tr>
<tr>
<td>VOV_HYS</td>
<td>Input OVP Hysteresis</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td><strong>MIC SWITCH</strong></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IOON</td>
<td>On Leakage Current of MIC Switch</td>
<td>SBUx = 0 V to 3.6 V, MIC is floating</td>
<td>VCC: 2.7 V to 5.5 V</td>
<td>−3.0</td>
<td>−</td>
<td>3.0</td>
<td>μA</td>
</tr>
<tr>
<td>IOZ</td>
<td>Off Leakage Current of MIC</td>
<td>MIC = 0 V to 3.6 V</td>
<td></td>
<td>−1.0</td>
<td>−</td>
<td>1.0</td>
<td>μA</td>
</tr>
<tr>
<td>IOFF</td>
<td>Power Off Leakage Current of MIC</td>
<td>MIC = 0 V to 3.6 V</td>
<td>Power off</td>
<td>−1.0</td>
<td>−</td>
<td>1.0</td>
<td>μA</td>
</tr>
<tr>
<td>RON</td>
<td>MIC Switch On Resistance</td>
<td>VSW = 3.6 V, Isw = 30 mA</td>
<td>VCC: 2.7 V to 5.5 V</td>
<td>−</td>
<td>3</td>
<td>−</td>
<td>Ω</td>
</tr>
<tr>
<td><strong>SBUX_H SWITCH</strong></td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>IOON</td>
<td>On Leakage Current of SBUx_H Switch</td>
<td>SBUx = 0 V to 3.6 V, SBUx_H is floating</td>
<td>VCC: 2.7 V to 5.5 V</td>
<td>−3.0</td>
<td>−</td>
<td>3.0</td>
<td>μA</td>
</tr>
<tr>
<td>IOZ</td>
<td>Off Leakage of SBUx_H</td>
<td>SBUx_H =0 V to 3.6 V</td>
<td></td>
<td>−1</td>
<td>−</td>
<td>1</td>
<td>μA</td>
</tr>
<tr>
<td>IOFF</td>
<td>Power Off Leakage Current of SBUx_H</td>
<td>SBUx_H = 0 V to 3.6 V</td>
<td>Power off</td>
<td>−1.0</td>
<td>−</td>
<td>1.0</td>
<td>μA</td>
</tr>
<tr>
<td>RON</td>
<td>SBUx_H Switch On Resistance</td>
<td>VSW = 0 V to 3.6 V, Isw = 30 mA</td>
<td>VCC: 2.7 V to 5.5 V</td>
<td>−</td>
<td>3</td>
<td>−</td>
<td>Ω</td>
</tr>
<tr>
<td><strong>AUDIO GROUND SWITCH: PIN: AGND TO SBUX</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RON</td>
<td>AGND Switch On Resistance</td>
<td>ISOURCE = 100 mA on SBUx</td>
<td>VCC: 2.7 V to 5.5 V</td>
<td>−</td>
<td>50</td>
<td>90</td>
<td>mΩ</td>
</tr>
<tr>
<td><strong>CC_IN PIN</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VTH_L</td>
<td>Input Low Threshold</td>
<td>VCC: 2.7 V to 5.5 V</td>
<td></td>
<td>−</td>
<td>1.2</td>
<td>−</td>
<td>V</td>
</tr>
<tr>
<td>VTH_H</td>
<td>Input High Threshold</td>
<td></td>
<td></td>
<td>−</td>
<td>1.5</td>
<td>−</td>
<td>V</td>
</tr>
<tr>
<td>IN</td>
<td>Input Leakage of CC_IN</td>
<td>CC_IN = 0 V to 5.5 V</td>
<td></td>
<td>−</td>
<td>−</td>
<td>1.0</td>
<td>μA</td>
</tr>
<tr>
<td><strong>INT, DET PINS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VOH</td>
<td>Output High for DET</td>
<td>Io = −2 mA</td>
<td>VCC: 2.7 V to 5.5 V</td>
<td>1.5</td>
<td>1.8</td>
<td>2</td>
<td>V</td>
</tr>
<tr>
<td>VDL</td>
<td>Output Low for DET and INT</td>
<td>Io = 2 mA</td>
<td></td>
<td>−</td>
<td>−</td>
<td>0.4</td>
<td>V</td>
</tr>
</tbody>
</table>

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Table 4. DC ELECTRICAL CHARACTERISTICS (continued)

(VCC = 2.7 V to 5.5 V, VCC (Typ.) = 3.3 V, TA = −40°C to 85°C, and T(A) (Typ.) = 25°C, unless otherwise specified.)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Power</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADDR PIN</td>
<td>VTH</td>
<td>Input voltage High</td>
<td>VCC: 2.7 V to 5.5 V</td>
<td>1.3</td>
<td>−</td>
<td>−</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>VIL</td>
<td>Input voltage Low</td>
<td>−</td>
<td>−</td>
<td>0.45</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>IN</td>
<td>Control Input Leakage</td>
<td>ADDR = 0 V to VCC</td>
<td>−1</td>
<td>−</td>
<td>1</td>
<td>μA</td>
</tr>
<tr>
<td>ENN PIN</td>
<td>VTH</td>
<td>Input Voltage High</td>
<td>VCC: 2.7 V to 5.5 V</td>
<td>1.3</td>
<td>−</td>
<td>−</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>VIL</td>
<td>Input Voltage Low</td>
<td>−</td>
<td>−</td>
<td>0.45</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>RP DL</td>
<td>Internal Pull Down Resistor</td>
<td>−</td>
<td>470</td>
<td>−</td>
<td>kΩ</td>
<td></td>
</tr>
<tr>
<td>SDS, SCL PINS</td>
<td>VIL2C</td>
<td>Low-Level Input Voltage</td>
<td>VCC: 2.7 V to 5.5 V</td>
<td>−</td>
<td>−</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>VHI2C</td>
<td>High-Level Input Voltage</td>
<td>−</td>
<td>−</td>
<td>1.2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>I2C</td>
<td>Input Current of SDA and SCL Pins</td>
<td>SCL/SDA = 0 V to 3.6 V</td>
<td>−2</td>
<td>−</td>
<td>2</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td>VOLS DA</td>
<td>Low-Level Output Voltage</td>
<td>IOL = 2 mA</td>
<td>−</td>
<td>−</td>
<td>0.3</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>IOLS DA</td>
<td>Low-Level Output Current</td>
<td>VOLS DA = 0.2 V</td>
<td>10</td>
<td>−</td>
<td>−</td>
<td>mA</td>
</tr>
</tbody>
</table>

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
Table 5. AC ELECTRICAL CHARACTERISTICS  
(VCC = 2.7 V to 5.5 V, VCC (Typ.) = 3.3 V, TA = −40°C to 85°C, and TA (Typ.) = 25°C, unless otherwise specified.)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Power</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>AUDIO SWITCH</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{\text{delay}} )</td>
<td>Audio Switch Turn On Delay Time</td>
<td>DP.R = DN.L = 1 V, ( R_L = 32 , \Omega )</td>
<td></td>
<td>−65</td>
<td>−</td>
<td>−</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>( t_{\text{rise}} )</td>
<td>Audio Switch Turn On Rising Time</td>
<td>(Note 1)  DP.R = DN.L = 1 V, ( R_L = 32 , \Omega )</td>
<td></td>
<td>−240</td>
<td>−</td>
<td>−</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>( t_{\text{OFF}} )</td>
<td>Audio Switch Turn Off Time</td>
<td>DP.R = DN.L = 1 V, ( R_L = 32 , \Omega )</td>
<td></td>
<td>−15</td>
<td>−</td>
<td>−</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>( X_{\text{TALK}} )</td>
<td>Cross Talk (Adjacent)</td>
<td>( f = 1 , \text{kHz}, , R_L = 50 , \Omega, , V_{SW} = 1 , \text{V}_{\text{RMS}} )</td>
<td></td>
<td>−100</td>
<td>−</td>
<td>−</td>
<td>dB</td>
</tr>
<tr>
<td><strong>BW</strong></td>
<td>−3 dB Bandwidth</td>
<td>( R_L = 50 , \Omega )</td>
<td></td>
<td>−600</td>
<td>−</td>
<td>−</td>
<td>MHz</td>
</tr>
<tr>
<td><strong>OIRR</strong></td>
<td>Off Isolation</td>
<td>F = 1 kHz, ( R_L = 50 , \Omega, , \text{CL} = 0 , \text{pF}, , V_{SW} = 1 , \text{V}_{\text{RMS}} )</td>
<td></td>
<td>−100</td>
<td>−</td>
<td>−</td>
<td>dB</td>
</tr>
<tr>
<td><strong>THD+N</strong></td>
<td>Total Harmonic Distortion + Noise</td>
<td>Performance with A−weighting Filter ( R_L = 600 , \Omega, , f = 20 , \text{Hz−20 kHz}, , V_{SW} = 2 , \text{V}_{\text{RMS}} )</td>
<td></td>
<td>−110</td>
<td>−</td>
<td>−</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( R_L = 32 , \Omega, , f = 20 , \text{Hz−20 kHz}, , V_{SW} = 1 , \text{V}_{\text{RMS}} )</td>
<td></td>
<td>−110</td>
<td>−</td>
<td>−</td>
<td>dB</td>
</tr>
<tr>
<td><strong>THD+N</strong></td>
<td></td>
<td>( R_L = 16 , \Omega, , f = 20 , \text{Hz−20 kHz}, , V_{SW} = 0.5 , \text{V}_{\text{RMS}} )</td>
<td></td>
<td>−108</td>
<td>−</td>
<td>−</td>
<td>dB</td>
</tr>
<tr>
<td><strong>USB SWITCH</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{\text{ON}} )</td>
<td>USB Switch Turn−on Time</td>
<td>DP.R = DN.L = 1.5 V, ( R_L = 50 , \Omega )</td>
<td></td>
<td>−60</td>
<td>−</td>
<td>−</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>( t_{\text{OFF}} )</td>
<td>USB Switch Turn −off Time</td>
<td>DP.R = DN.L = 1.5 V, ( R_L = 50 , \Omega )</td>
<td></td>
<td>−15</td>
<td>−</td>
<td>−</td>
<td>( \mu s )</td>
</tr>
<tr>
<td><strong>BW</strong></td>
<td>−3 dB Bandwidth</td>
<td>( R_L = 50 , \Omega )</td>
<td></td>
<td>−850</td>
<td>−</td>
<td>−</td>
<td>MHz</td>
</tr>
<tr>
<td><strong>OIRR</strong></td>
<td>Off Isolation between DP, DN and Common Node Pins</td>
<td>f = 1 kHz, ( R_L = 50 , \Omega, , \text{Cl} = 0 , \text{pF}, , V_{SW} = 1 , \text{V}_{\text{RMS}} )</td>
<td></td>
<td>−100</td>
<td>−</td>
<td>−</td>
<td>dB</td>
</tr>
<tr>
<td>( t_{\text{OVP}} )</td>
<td>DP.R and DN.L pins OVP Response Time</td>
<td>Vsw = 3.5 V to 5.5 V</td>
<td></td>
<td>1</td>
<td>1.5</td>
<td>−</td>
<td>( \mu s )</td>
</tr>
<tr>
<td><strong>MIC/AUDIO GROUND SWITCH</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{\text{delay} _\text{MIC}} )</td>
<td>MIC Switch Turn On Delay Time</td>
<td>SBUx = 1 V, ( R_L = 50 , \Omega )</td>
<td></td>
<td>−100</td>
<td>−</td>
<td>−</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>( t_{\text{rise} _\text{MIC}} )</td>
<td>MIC Switch Turn On Rising Time</td>
<td>(Note 1) SBUx = 1 V, ( R_L = 50 , \Omega )</td>
<td></td>
<td>−250</td>
<td>−</td>
<td>−</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>( t_{\text{delay} _\text{AGND}} )</td>
<td>AGND Switch Turn On Time</td>
<td>SBUx pulled up to 0.5 V by 16 ( \Omega, , \text{AGND connect to GND} )</td>
<td></td>
<td>−100</td>
<td>−</td>
<td>−</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>( t_{\text{rise} _\text{AGND}} )</td>
<td>AGND Switch Turn On Rising Time</td>
<td>(Note 1) SBUx pulled up to 0.5 V by 16 ( \Omega, , \text{AGND connect to GND} )</td>
<td></td>
<td>−1500</td>
<td>−</td>
<td>−</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>( t_{\text{OFF} _\text{MIC}} )</td>
<td>MIC Switch Turn Off Time</td>
<td>SBUx = 2.5 V, ( R_L = 50 , \Omega )</td>
<td></td>
<td>−15</td>
<td>−</td>
<td>−</td>
<td>−</td>
</tr>
<tr>
<td>( t_{\text{OFF} _\text{Audio GND}} )</td>
<td>AGND Switch Turn Off Time</td>
<td>SBUx: Isource = 10 mA, clamp to 2.5 V</td>
<td></td>
<td>−15</td>
<td>−</td>
<td>−</td>
<td>−</td>
</tr>
<tr>
<td><strong>BW</strong></td>
<td>MIC Switch Bandwidth</td>
<td>( R_L = 50 , \Omega )</td>
<td></td>
<td>−50</td>
<td>−</td>
<td>−</td>
<td>MHz</td>
</tr>
</tbody>
</table>
### Table 5. AC ELECTRICAL CHARACTERISTICS (continued)

(V\(\text{CC} = 2.7\) V to 5.5 V, V\(\text{CC}\) (Typ.) = 3.3 V, T\(\text{A}\) = −40°C to 85°C, and T\(\text{A}\) (Typ.) = 25°C, unless otherwise specified.)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Power</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>i\text{ON}</td>
<td>SBUx_H Switch Turn On Time</td>
<td>SBUx = 2.5 V, R(L) = 50 Ω</td>
<td>V(\text{CC}) = 3.3 V</td>
<td>−35</td>
<td>−</td>
<td>−</td>
<td>μs</td>
</tr>
<tr>
<td>i\text{OFF}</td>
<td>SBUx_H Switch Turn Off Time</td>
<td></td>
<td></td>
<td>−15</td>
<td>−</td>
<td>−</td>
<td></td>
</tr>
<tr>
<td>BW</td>
<td>Bandwidth</td>
<td>R(L) = 50 Ω</td>
<td></td>
<td>−</td>
<td>50</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>i\text{OVP}</td>
<td>SBUx Pins OVP Response Time</td>
<td>V(\text{sw}) = 3.5 V to 5.5 V</td>
<td></td>
<td>−0.5</td>
<td>1</td>
<td></td>
<td>μs</td>
</tr>
</tbody>
</table>

**SENSE SWITCH**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Power</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>t\text{delay}</td>
<td>Sense Switch Turn On Delay Time</td>
<td>GSBUx = 1 V, R(L) = 50 Ω</td>
<td>V(\text{CC}) = 3.3 V</td>
<td>−65</td>
<td>−</td>
<td>−</td>
<td>μs</td>
</tr>
<tr>
<td>t\text{rise}</td>
<td>Sense Switch Turn On Rising Time</td>
<td></td>
<td></td>
<td>−260</td>
<td>−</td>
<td>−</td>
<td>μs</td>
</tr>
<tr>
<td>t\text{OFF}</td>
<td>Sense Switch Turn Off Time</td>
<td></td>
<td></td>
<td>−15</td>
<td>−</td>
<td>−</td>
<td>μs</td>
</tr>
<tr>
<td>i\text{OVP}</td>
<td>GSBUx Pins OVP Response Time</td>
<td>V(\text{SW}): 3.5 V to 5.5 V</td>
<td></td>
<td>−0.7</td>
<td>1.5</td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>BW</td>
<td>Bandwidth</td>
<td>R(L) = 50 Ω</td>
<td></td>
<td>−</td>
<td>150</td>
<td>−</td>
<td>MHz</td>
</tr>
</tbody>
</table>

**DET DELAY**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Power</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>t\text{DELAY_DET}</td>
<td>DET Response Delay</td>
<td>Transition from 0 to 1.8 V</td>
<td>V(\text{CC}) = 3.3 V</td>
<td>−1</td>
<td>−</td>
<td>−</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Transition from 1.8 to 0 V</td>
<td></td>
<td>−5</td>
<td>−</td>
<td>−</td>
<td></td>
</tr>
</tbody>
</table>

1. Turn on timing can be controlled by I\(\text{C}\) register.
Table 6. I²C SPECIFICATION
(VCC = 2.7 V to 5.5, VCC (Typ.) = 3.3 V, TA = −40°C to 85°C, TA (Typ.) = 25°C, unless otherwise specified)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Fast Mode</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>fSCL</td>
<td>I²C_SCL Clock Frequency</td>
<td></td>
<td>400</td>
<td>kHz</td>
</tr>
<tr>
<td>tHD; STA</td>
<td>Hold Time (Repeated) START Condition</td>
<td>0.6</td>
<td>ns</td>
<td>μs</td>
</tr>
<tr>
<td>tLOW</td>
<td>Low Period of I²C_SCL Clock</td>
<td>1.3</td>
<td>ns</td>
<td>μs</td>
</tr>
<tr>
<td>tHIGH</td>
<td>High Period of I²C_SCL Clock</td>
<td>0.6</td>
<td>ns</td>
<td>μs</td>
</tr>
<tr>
<td>tSU; STA</td>
<td>Set-up Time for Repeated START Condition</td>
<td>0.6</td>
<td>ns</td>
<td>μs</td>
</tr>
<tr>
<td>tHD; DAT</td>
<td>Data Hold Time (Note 2)</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>tSU; DAT</td>
<td>Data Set-up Time (Note 3)</td>
<td>100</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tR</td>
<td>Rise Time of I²C_SDA and I²C_SCL Signals (Note 3)</td>
<td>20 + 0.1C₀</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tF</td>
<td>Fall Time of I²C_SDA and I²C_SCL Signals (Note 3)</td>
<td>20 + 0.1C₀</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tSU; STO</td>
<td>Set-up Time for STOP Condition</td>
<td>0.6</td>
<td>ns</td>
<td>μs</td>
</tr>
<tr>
<td>tBUF</td>
<td>Bus–Free Time between STOP and START Conditions</td>
<td>1.3</td>
<td>ns</td>
<td>μs</td>
</tr>
<tr>
<td>tSP</td>
<td>Pulse Width of Spikes that Must Be Suppressed by the Input Filter</td>
<td>0</td>
<td>50</td>
<td>ns</td>
</tr>
</tbody>
</table>

2. Guaranteed by design, not production tested.
3. A fast–mode I²C–bus device can be used in a standard–mode I²C–bus system, but the requirement tSU;DAT ≥ ±250 ns must be met. This is automatically the case if the device does not stretch the LOW period of the I²C_SCL signal. If such a device does stretch the LOW period of the I²C_SCL signal, it must output the next data bit to the I²C_SDA line \( t_{R \max} + t_{SU;DAT} = 1000 + 250 = 1250 \) ns (according to the standard–mode I²C bus specification) before the I²C_SCL line is released.

![Figure 3. Definition of Timing for Full-Speed Mode Devices on the I²C Bus](https://www.onsemi.com)
Table 7. CAPACITANCE
(VCC= 2.7 V to 5.5 V, VCC (Typ.) = 3.3 V, TA = −40°C to 85°C, and TA (Typ.) = 25°C)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_{ON_USB/Audio}</td>
<td>On Capacitance (6)</td>
<td>f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias</td>
<td>VCC = 3.3 V</td>
</tr>
<tr>
<td>C_{OFF_USB/Audio}</td>
<td>Off Capacitance (6)</td>
<td>f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias</td>
<td>9</td>
</tr>
<tr>
<td>C_{OFF_USB}</td>
<td>Off Capacitance (Non–Common Ports) (6)</td>
<td>f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias</td>
<td>7.5</td>
</tr>
<tr>
<td>C_{ON_SENSE_SW}</td>
<td>On Capacitance – (Common Ports) (6)</td>
<td>f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias</td>
<td>3</td>
</tr>
<tr>
<td>C_{OFF_SENSE_SW}</td>
<td>Off Capacitance – (Common Ports) (6)</td>
<td>f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias</td>
<td>55</td>
</tr>
<tr>
<td>C_{ON_MIC_SW}</td>
<td>On Capacitance – (Common Ports) (6)</td>
<td>f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias</td>
<td>88</td>
</tr>
<tr>
<td>C_{OFF_MIC_SW}</td>
<td>Off Capacitance – (Common Ports) (6)</td>
<td>f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias</td>
<td>170</td>
</tr>
<tr>
<td>C_{ON_AGGND_SW}</td>
<td>On Capacitance – (Common Ports) (6)</td>
<td>f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias</td>
<td>125</td>
</tr>
<tr>
<td>C_{ON_SBUX_H_SW}</td>
<td>On Capacitance – (Common Ports) (6)</td>
<td>f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias</td>
<td>160</td>
</tr>
<tr>
<td>C_{CNTRL}</td>
<td>Control Input Pin Capacitance (6)</td>
<td>f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias</td>
<td>ENN</td>
</tr>
</tbody>
</table>

Table 8. REGISTER MAPS

<table>
<thead>
<tr>
<th>ADDR</th>
<th>Register Name</th>
<th>Type</th>
<th>Reset Value</th>
<th>BIT7</th>
<th>BIT6</th>
<th>BIT5</th>
<th>BIT4</th>
<th>BIT3</th>
<th>BIT2</th>
<th>BIT1</th>
<th>BIT0</th>
</tr>
</thead>
<tbody>
<tr>
<td>00H</td>
<td>Device ID</td>
<td>R</td>
<td>0x09</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>01H</td>
<td>OVP Interrupt Mask</td>
<td>R/W</td>
<td>0x00</td>
<td>Reserved</td>
<td>Mask OVP interrupt</td>
<td>Mask OVP /DP_R</td>
<td>Mask OVP /DN_L</td>
<td>Mask OVP /SBU1</td>
<td>Mask OVP /SBU2</td>
<td>Mask OVP /GSBU1</td>
<td>Mask OVP /GSBU2</td>
</tr>
<tr>
<td>02H</td>
<td>OVP interrupt flag</td>
<td>R/C</td>
<td>0x00</td>
<td>Reserved</td>
<td>DP_R</td>
<td>DN_L</td>
<td>SBU1</td>
<td>SBU2</td>
<td>GSBU</td>
<td>GSBU2</td>
<td></td>
</tr>
<tr>
<td>03H</td>
<td>OVP status</td>
<td>R</td>
<td>0x00</td>
<td>Reserved</td>
<td>OVP/DP_R</td>
<td>OVP/DN_L</td>
<td>OVP/SBU1</td>
<td>OVP/DBU1</td>
<td>OVP/GSBU1</td>
<td>OVP/GSBU2</td>
<td></td>
</tr>
<tr>
<td>04H</td>
<td>Switch settings Enable</td>
<td>R/W</td>
<td>0x08</td>
<td>Device control</td>
<td>SBU1_H to SBUX</td>
<td>SBU2_H to SBUX</td>
<td>SBU1_L to DN or L</td>
<td>SBU2_L to DN or L</td>
<td>Sense to GSBU1</td>
<td>Sense to GSBU2</td>
<td>Audio Ground to SBUX</td>
</tr>
<tr>
<td>05H</td>
<td>Switch select</td>
<td>R/W</td>
<td>0x18</td>
<td>Reserved</td>
<td>SBU1_H to SBUX</td>
<td>SBU2_H to SBUX</td>
<td>SBU1_L to DN or L</td>
<td>SBU2_L to DN or L</td>
<td>Sense to GSBU1</td>
<td>Sense to GSBU2</td>
<td>Audio Ground to SBUX</td>
</tr>
<tr>
<td>06H</td>
<td>Switch Status0</td>
<td>R</td>
<td>0x00</td>
<td>Reserved</td>
<td>Sense Switch Status</td>
<td>DP_R Switch Status</td>
<td>DN_L Switch Status</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>07H</td>
<td>Switch Status1</td>
<td>R</td>
<td>0x00</td>
<td>Reserved</td>
<td>SBU2 Switch Status</td>
<td>SBU1 Switch Status</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>08H</td>
<td>Audio Switch Left Channel turn on Control</td>
<td>R/W</td>
<td>0x01</td>
<td>Audio switch left channel slow control [7:0]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>09H</td>
<td>Audio Switch Right Channel turn on Control</td>
<td>R/W</td>
<td>0x01</td>
<td>Audio switch right channel slow control [7:0]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0AH</td>
<td>MIC switch turn on control</td>
<td>R/W</td>
<td>0x01</td>
<td>MIC switch right channel slow control [7:0]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0BH</td>
<td>Sense switch turn on control</td>
<td>R/W</td>
<td>0x01</td>
<td>Sense switch right channel slow control [7:0]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0CH</td>
<td>Audio Ground Switch turn on Control</td>
<td>R/W</td>
<td>0x01</td>
<td>Audio ground switch right channel slow control [7:0]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Table 8. REGISTER MAPS

| ADDR | Register Name | Type | Reset Value | BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|------|---------------|------|-------------|------|------|------|------|------|------|------|------|------|
| 0DH  | Timing Delay between R switch enable and L switch enable | R/W  | 0x00        |      |      |      |      |      |      |      |      |      |
| 0EH  | Timing Delay between MIC switch enable and L switch enable | R/W  | 0x00        |      |      |      |      |      |      |      |      |      |
| 0FH  | Timing Delay between Sense switch enable and L switch enable | R/W  | 0x00        |      |      |      |      |      |      |      |      |      |
| 10H  | Timing Delay between Audio ground switch enable and L switch enable | R/W  | 0x00        |      |      |      |      |      |      |      |      |      |
| 11H  | Audio accessory status | R    | 0x02        |      |      |      |      |      |      |      |      |      |
| 12H  | Function enable | R/W  | 0x08        |      |      |      |      |      |      |      |      |      |
| 13H  | RES detection pin setting | R/W  | 0x00        |      |      |      |      |      |      |      |      |      |
| 14H  | RES detection value | R    | 0xFF        |      |      |      |      |      |      |      |      |      |
| 15H  | RES detection interrupt threshold | R/W  | 0x16        |      |      |      |      |      |      |      |      |      |
| 16H  | RES detection interval | R/W  | 0x00        |      |      |      |      |      |      |      |      |      |
| 17H  | Audio jack Status | RO   | 0x01        |      |      |      |      |      |      |      |      |      |
| 18H  | Detection interrupt | R/C  | 0x00        |      |      |      |      |      |      |      |      |      |
| 19H  | Detection interrupt Mask | R/W  | 0x00        |      |      |      |      |      |      |      |      |      |
| 1AH  | Audio detection RGE1 | RO   | 0xFF        |      |      |      |      |      |      |      |      |      |
| 1BH  | Audio detection RGE2 | RO   | 0xFF        |      |      |      |      |      |      |      |      |      |
| 1CH  | MIC Threshold DATA0 | R/W  | 0x20        |      |      |      |      |      |      |      |      |      |
| 1DH  | MIC Threshold DATA1 | R/W  | 0xFF        |      |      |      |      |      |      |      |      |      |
| 1EH  | I2C Reset | W/C  | 0x00        |      |      |      |      |      |      |      |      |      |
| 1FH  | Current Source Setting | R/W  | 0x07        |      |      |      |      |      |      |      |      |      |

### Table 9. I2C SLAVE ADDRESS

<table>
<thead>
<tr>
<th>ADDR</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADDR = L</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>R/W</td>
</tr>
<tr>
<td>ADDR = H</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>R/W</td>
</tr>
</tbody>
</table>
### DEVICE ID
Address: 00h  
Reset Value: 8'b 0000_1001  
Type: Read  

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:6</td>
<td>Vendor ID</td>
<td>2</td>
<td>Vendor ID</td>
</tr>
<tr>
<td>5:3</td>
<td>Version ID</td>
<td>3</td>
<td>Device Version ID</td>
</tr>
<tr>
<td>2:0</td>
<td>Revision ID</td>
<td>3</td>
<td>Revision History ID</td>
</tr>
</tbody>
</table>

### OVP INTERRUPT MASK
Address: 01h  
Reset Value: 8'b 0000_0000  
Type: Read/Write  

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Reserved</td>
<td>1</td>
<td>Do Not Use</td>
</tr>
<tr>
<td>6</td>
<td>OVP Interrupt mask control</td>
<td>1</td>
<td>OVP Interrupt function Enable/Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Controlled by [5:0] bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Mask all connector side pins OVP interrupt</td>
</tr>
<tr>
<td>5</td>
<td>DP_R OVP Interrupt mask control</td>
<td>1</td>
<td>0: Do not mask OVP interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Mask OVP interrupt</td>
</tr>
<tr>
<td>4</td>
<td>DN_L OVP Interrupt mask control</td>
<td>1</td>
<td>0: Do not mask OVP interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Mask OVP interrupt</td>
</tr>
<tr>
<td>3</td>
<td>SBU1 OVP Interrupt mask control</td>
<td>1</td>
<td>0: Do not mask OVP interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Mask OVP interrupt</td>
</tr>
<tr>
<td>2</td>
<td>SBU2 OVP Interrupt mask control</td>
<td>1</td>
<td>0: Do not mask OVP interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Mask OVP interrupt</td>
</tr>
<tr>
<td>1</td>
<td>GSBU1 OVP Interrupt mask control</td>
<td>1</td>
<td>0: Do not mask OVP interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Mask OVP interrupt</td>
</tr>
<tr>
<td>0</td>
<td>GSBU2 OVP Interrupt mask control</td>
<td>1</td>
<td>0: Do not mask OVP interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Mask OVP interrupt</td>
</tr>
</tbody>
</table>

### OVP INTERRUPT FLAG
Address: 02h  
Reset Value: 8'b 0000_0000  
Type: Read Clear  

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7:6]</td>
<td>Reserved</td>
<td>2</td>
<td>Do Not Use</td>
</tr>
<tr>
<td>5</td>
<td>DP_R OVP</td>
<td>1</td>
<td>0: OVP event has not occurred</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: OVP event has occurred</td>
</tr>
<tr>
<td>4</td>
<td>DN_L OVP</td>
<td>1</td>
<td>0: OVP event has not occurred</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: OVP event has occurred</td>
</tr>
<tr>
<td>3</td>
<td>SBU1 OVP</td>
<td>1</td>
<td>0: OVP event has not occurred</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: OVP event has occurred</td>
</tr>
<tr>
<td>2</td>
<td>SBU2 OVP</td>
<td>1</td>
<td>0: OVP event has not occurred</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: OVP event has occurred</td>
</tr>
<tr>
<td>1</td>
<td>GSBU1 OVP</td>
<td>1</td>
<td>0: OVP event has not occurred</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: OVP event has occurred</td>
</tr>
<tr>
<td>0</td>
<td>GSBU2 OVP</td>
<td>1</td>
<td>0: OVP event has not occurred</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: OVP event has occurred</td>
</tr>
</tbody>
</table>
### OVP STATUS

Address: 03h  
Reset Value: 8'b 0000_0000  
Type: Read

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7:6]</td>
<td>Reserved</td>
<td>2</td>
<td>Do Not Use</td>
</tr>
<tr>
<td>5</td>
<td>OVP on DP_R PIN</td>
<td>1</td>
<td>0: OVP event has not occurred</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: OVP event has occurred</td>
</tr>
<tr>
<td>4</td>
<td>OVP on DN_L PIN</td>
<td>1</td>
<td>0: OVP event has not occurred</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: OVP event has occurred</td>
</tr>
<tr>
<td>3</td>
<td>OVP on SBU1 PIN</td>
<td>1</td>
<td>0: OVP event has not occurred</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: OVP event has occurred</td>
</tr>
<tr>
<td>2</td>
<td>OVP on SBU2 PIN</td>
<td>1</td>
<td>0: OVP event has not occurred</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: OVP event has occurred</td>
</tr>
<tr>
<td>1</td>
<td>OVP on GSBU1 PIN</td>
<td>1</td>
<td>0: OVP event has not occurred</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: OVP event has occurred</td>
</tr>
<tr>
<td>0</td>
<td>OVP on GSBU2 PIN</td>
<td>1</td>
<td>0: OVP event has not occurred</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: OVP event has occurred</td>
</tr>
</tbody>
</table>

### SWITCHING SETTING ENABLE

Address: 04h  
Reset Value: 8'b 1001_1000  
Type: Read/Write

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
</table>
| 7    | Device Enable                     | 1    | 0: Device Disable; L, R pull down by 10 k and other switch nodes will be high−Z for positive input.  
|      |                                   |      | 1: Device Enable.  
|      |                                   |      | Device Enable = 1 Device enable = 0 Device Disable  
|      |                                   |      | 0 Device Enable  
|      |                                   |      | Device Disable = 0 Device Disable  
| 6    | SBU1_H to SBUx switches           | 1    | 0: Switch Disable; SBU1_H will be high−Z for positive input  
|      |                                   |      | 1: Switch Enable  
| 5    | SBU2_H to SBUx switches           | 1    | 0: Switch Disable; SBU2_H will be high−Z for positive input  
|      |                                   |      | 1: Switch Enable  
| 4    | DN_L to DN or L switches          | 1    | 0: Switch Disable; DN_L,DN will be high−Z for positive input. L pull down by 10 kohm  
|      |                                   |      | 1: Switch Enable  
| 3    | DP_R to DP or R switches          | 1    | 0: Switch Disable; DP_R,DP will be high−Z for positive input. R pull down by 10 kohm  
|      |                                   |      | 1: Switch Enable  
| 2    | Sense to GSBUx switches           | 1    | 0: Switch Disable; Sense,GSBU1 and GSBU2 will be high−Z for positive input  
|      |                                   |      | 1: Switch Enable  
| 1    | MIC to SBUx switches              | 1    | 0: Switch Disable; MIC will be high−Z for positive input.  
|      |                                   |      | 1: Switch Enable  
| 0    | AGND to SBUx switches             | 1    | 0: Switch Disable; AGND will be high−Z for positive input.  
|      |                                   |      | 1: Switch Enable  

---

[Downloaded from Arrow.com](https://www.onsemi.com)
### SWITCH SELECT
Address: 05h  
Reset Value: 8'b 0001_1000  
Type: Read/Write

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Reserved</td>
<td>1</td>
<td>Do Not Use</td>
</tr>
</tbody>
</table>
| 6    | SBU1_H switches             | 1    | 0: SBU1_H to SBU1 switch ON  
1: SBU1_H to SBU2 switch ON                                   |
| 5    | SBU2_H switches             | 1    | 0: SBU2_H to SBU2 switch ON  
1: SBU2_H to SBU1 switch ON                                   |
| 4    | DN_L to DN or L switches    | 1    | 0: DN_L to L switch ON  
1: DN_L to DN switch ON                                   |
| 3    | DP_R to DP or R switches    | 1    | 0: DP_R to R switch ON  
1: DP_R to DP switch ON                                   |
| 2    | Sense to GSBUx switches     | 1    | 0: Sense to GSBU1 switch ON  
1: Sense to GSBU2 switch ON                                   |
| 1    | MIC to SBUx switches        | 1    | 0: MIC to SBU2 switch ON  
1: MIC to SBU1 switch ON                                   |
| 0    | AGND to SBUx switches       | 1    | 0: AGND to SBU1 switch ON  
1: AGND to SBU2 switch ON                                   |

### SWITCH STATUS0
Address: 06h  
Reset Value: 8'b 0000_0000  
Type: Read Only

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7:6]</td>
<td>Reserved</td>
<td>2</td>
<td>Do not use</td>
</tr>
</tbody>
</table>
| [5:2]     | Sense Switch Status   | 2    | 00: Sense switch is Open/Not Connected  
01: Sense connected to GSBU1  
10: Sense connected to GSBU2  
11: Not Valid |
| [3:2]     | DP_R Switch Status    | 2    | 00: DP_R Switch Open/Not Connected  
01: DP_R connected to DP  
10: DP_R connected to R  
11: Not Valid |
| [1:0]     | DN_L switch Status    | 2    | 00: DN_L Switch Open/Not Connected  
01: DN_L connected to DN  
10: DN_L connected to L  
11: Not Valid |
### SWITCH STATUS1
Address: 07h  
Reset Value: 8'b 0000_0000  
Type: Read Only

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7:6]</td>
<td>Reserved</td>
<td>2</td>
<td>Do not use</td>
</tr>
</tbody>
</table>
| [5:3]  | SBU2 Switch Status | 3    | 000: SBU2 switch is Open/Not Connected  
001: SBU2 connected to MIC  
010: SBU2 connected to AGND  
011: SBU2 connected to SBU1_H  
100: SBU2 connected to SBU2_H  
101: SBU2 connected both SBU1_H and SBU2_H  
110…111: Do not use |
| [2:0]  | SBU1 Switch Status | 3    | 000: SBU1 switch is Open/Not Connected  
001: SBU1 connected to MIC  
010: SBU1 connected to AGND  
011: SBU1 connected to SBU1_H  
100: SBU1 connected to SBU2_H  
101: SBU1 connected both SBU1_H and SBU2_H  
110…111: Do not use |

### AUDIO SWITCH LEFT CHANNEL SLOW TURN–ON
Address: 08h  
Reset Value: 8'b 0000_0001  
Type: Read/Write

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7:0]</td>
<td>Switch turn on rising time setting</td>
<td>8</td>
<td>11111111: 25600 μS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>...</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00000000: 200 μS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00000000: 100 μS</td>
</tr>
</tbody>
</table>

### AUDIO SWITCH RIGHT CHANNEL SLOW TURN–ON
Address: 09h  
Reset Value: 8'b 0000_0001  
Type: Read/Write

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7:0]</td>
<td>Switch turn on rising time setting</td>
<td>8</td>
<td>11111111: 25600 μS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>...</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00000001: 200 μS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00000000: 100 μS</td>
</tr>
</tbody>
</table>

### MIC SWITCH SLOW TURN–ON
Address: 0Ah  
Reset Value: 8'b 0000_0001  
Type: Read/Write

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7:0]</td>
<td>Switch turn on rising time setting</td>
<td>8</td>
<td>11111111: 25700 μS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>...</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00000010: 350 μS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00000011: 250 μS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00000000: Not Valid</td>
</tr>
</tbody>
</table>
SENSE SWITCH SLOW TURN-ON
Address: 0Bh
Reset Value: 8'b 0000_0001
Type: Read/Write

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7:0]</td>
<td>Switch turn on rising time setting</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11111111: 25600 µS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>...</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00000001: 200 µS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00000000: 100 µS</td>
</tr>
</tbody>
</table>

AUDIO GROUND SWITCH SLOW TURN-ON
Address: 0Ch
Reset Value: 8'b 0000_0001
Type: Read/Write

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7:0]</td>
<td>Switch turn on rising time setting</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11111111: 179000 µS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>...</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00000001: 1400 µS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00000000: 700 µS</td>
</tr>
</tbody>
</table>

TIMING DELAY BETWEEN R SWITCH ENABLE AND L SWITCH ENABLE
Address: 0Dh
Reset Value: 8'b 0000_0000
Type: Read/Write

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7:0]</td>
<td>Delay timing setting</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11111111: 25500 µS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11111110: 25400 µS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>...</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00000001: 100 µS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00000000: 0 µS</td>
</tr>
</tbody>
</table>

TIMING DELAY BETWEEN MIC SWITCH ENABLE AND L SWITCH ENABLE
Address: 0Eh
Reset Value: 8'b 0000_0000
Type: Read/Write

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7:0]</td>
<td>Delay timing setting</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11111111: 25500 µS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11111110: 25400 µS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>...</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00000001: 100 µS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00000000: 0 µS</td>
</tr>
</tbody>
</table>
## TIMING DELAY BETWEEN SENSE SWITCH ENABLE AND L SWITCH ENABLE

Address: 0Fh  
Reset Value: 8'b 0000_0000  
Type: Read/Write

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7:0]</td>
<td>Delay timing setting</td>
<td>8</td>
<td>11111111: 25500 μS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11111110: 25400 μS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>...</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00000001: 100 μS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00000000: 0 μS</td>
</tr>
</tbody>
</table>

## TIMING DELAY BETWEEN AUDIO GROUND SWITCH ENABLE AND L SWITCH ENABLE

Address: 10h  
Reset Value: 8'b 0000_0000  
Type: Read/Write

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7:0]</td>
<td>Delay timing setting</td>
<td>8</td>
<td>11111111: 25500 μS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11111110: 25400 μS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>...</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00000001: 100 μS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00000000: 0 μS</td>
</tr>
</tbody>
</table>

## AUDIO ACCESSORY STATUS

Address: 11h  
Reset Value: 8'b 0000_0010  
Type: Read

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7:2]</td>
<td>Reserved</td>
<td>6</td>
<td>Do not use</td>
</tr>
<tr>
<td>1</td>
<td>CC_IN</td>
<td>1</td>
<td>0: CC_IN &lt; 1.2 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: CC_IN &gt; 1.5 V</td>
</tr>
<tr>
<td>0</td>
<td>DET</td>
<td>1</td>
<td>0: DET output is low</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: DET is output is high</td>
</tr>
</tbody>
</table>
FUNCTION ENABLE
Address: 12h
Reset Value: 8'b 0000_1000
Type: Read/Write

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Reserved</td>
<td>1</td>
<td>Do not use</td>
</tr>
</tbody>
</table>
| 6    | DET I/O Control                   | 1    | 1: DET pin is in Open/Drain Configuration
                                      |      | 0: DET pin is in Push/Pull Configuration                                     |
| 5    | RES detection range setting       | 1    | 1: 10k to 2560 k                                                          |
                                      |      | 0: 1k to 256 k                                                             |
| 4    | GPIO control enable               | 1    | 1: enable                                                                   |
                                      |      | 0: disable                                                                  |
| 3    | Slow turn on control enable       | 1    | 1: enable                                                                   |
                                      |      | 0: disable                                                                  |
| 2    | MIC auto break out control enable | 1    | 1: enable                                                                   |
                                      |      | 0: disable                                                                  |
| 1    | RES detection enable              | 1    | 1: enable; will be changed to ‘0’ after low resistance detection
                                      |      | 0: disable                                                                  |
| 0    | Audio jack detection and          | 1    | 1: enable; will be changed to ‘0’ after audio jack detection and configuration
                                      |      | 0: disable                                                                  |

When GPIO control mode (manual switch control) is enable. ‘Switch control’ register is changed to read only. It will reflect switch status. I²C slave address is

RES DETECTION PIN SETTING
Address: 13h
Reset Value: 8'b 0000_0000
Type: Read

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7:3]</td>
<td>Reserved</td>
<td>5</td>
<td>Do not use</td>
</tr>
</tbody>
</table>
| [2:0]| Pin selection | 3 | 000: CC_IN
                                      |      | 001: DP/R
                                      |      | 010: DN_L
                                      |      | 011: SBU1
                                      |      | 100: SBU2
                                      |      | 101: Do not use
                                      |      | ...                                |
                                      |      | 111: Do not use                     |

If RES detection pin is enable before setting PIN selection it will always do the CC_IN first. Recommend user to select the pin first before setting the RES detection pin enable.

RES VALUE
Address: 14h
Reset Value: 8'b 1111_1111
Type: Read

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
</table>
| [7:0]| Detected resistance value | 8    | 0000_0000 : R < 1 k
                                      |      | ...                        |
                                      |      | 1111_1111: R > 300 K
# RES DETECTION THRESHOLD

Address: 15h  
Reset Value: 8'b 0001_0110  
Type: Read

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7:0]</td>
<td>RES detection threshold</td>
<td>8</td>
<td>Selection by 1 KΩ per step if Reg 12h [5] = 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Selection by 10 KΩ per step if Reg 12h [5] = 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Default Value = 22 KΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0000_0000: 1 KΩ /10 KΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>...</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1111_1111: 256 KΩ /2560 KΩ</td>
</tr>
</tbody>
</table>

# RES DETECTION INTERVAL

Address: 16h  
Reset Value: 8'b 0000_0000  
Type: Read

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7:2]</td>
<td>Reserved</td>
<td>6</td>
<td>Do not use</td>
</tr>
<tr>
<td>[1:0]</td>
<td>RES detection interval</td>
<td>2</td>
<td>00: Single</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: 100 mS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: 1 S</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: 10 S</td>
</tr>
</tbody>
</table>

# AUDIO JACK STATUS

Address: 17h  
Reset Value: 8'b 0000_0001  
Type: Read

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7:3]</td>
<td>Reserved</td>
<td>4</td>
<td>Do not use</td>
</tr>
<tr>
<td>3</td>
<td>4pole</td>
<td>1</td>
<td>1: 4 Pole SBU2 to MIC, SBU1 to audio ground</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: others</td>
</tr>
<tr>
<td>2</td>
<td>4pole</td>
<td>1</td>
<td>1: 4 Pole SBU1 to MIC, SBU2 to audio ground</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: others</td>
</tr>
<tr>
<td>1</td>
<td>3 pole</td>
<td>1</td>
<td>1: 3 pole</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: others</td>
</tr>
<tr>
<td>0</td>
<td>No audio accessory</td>
<td>1</td>
<td>1: No audio accessory</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Audio accessory attached</td>
</tr>
</tbody>
</table>

# RES DETECTION /AUDIO JACK DETECTION INTERRUPT FLAG

Address: 18h  
Reset Value: 8'b 0000_0000  
Type: Read Clear

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7:3]</td>
<td>Reserved</td>
<td>5</td>
<td>Do Not Use</td>
</tr>
<tr>
<td>2</td>
<td>Audio jack detection and configuration</td>
<td>1</td>
<td>0: Audio jack detection and configuration has not occurred</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Audio jack detection and configuration has occurred</td>
</tr>
<tr>
<td>1</td>
<td>Low resistance occurred</td>
<td>1</td>
<td>0: Low resistance has not occurred</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Low resistance has occurred</td>
</tr>
<tr>
<td>0</td>
<td>Low resistance detection</td>
<td>1</td>
<td>0: Low resistance has not occurred</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Low resistance has occurred</td>
</tr>
</tbody>
</table>
### RES / AUDIO JACK DETECTION INTERRUPT MASK
Address: 19h
Reset Value: 8'b 0000_0000
Type: Read

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7:3]</td>
<td>Reserved</td>
<td>5</td>
<td>Do Not Use</td>
</tr>
<tr>
<td>2</td>
<td>Audio jack detection and configuration</td>
<td>1</td>
<td>1: Mask Audio jack detection and configuration has occurred interrupt</td>
</tr>
<tr>
<td>1</td>
<td>Low resistance occurred</td>
<td>1</td>
<td>1: Low resistance has occurred interrupt</td>
</tr>
<tr>
<td>0</td>
<td>Low resistance detection</td>
<td>1</td>
<td>1: Low resistance detection has occurred interrupt</td>
</tr>
</tbody>
</table>

### AUDIO JACK DETECTION REG1 VALUE
Address: 1Ah
Reset Value: 8'b 1111_1111
Type: Read

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7:0]</td>
<td>Audio jack detection value</td>
<td>8</td>
<td>Resistance between SBU1 to SBU2</td>
</tr>
</tbody>
</table>

### AUDIO JACK DETECTION REG2 VALUE
Address: 1Bh
Reset Value: 8'b 1111_1111
Type: Read

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7:0]</td>
<td>Audio jack detection value</td>
<td>8</td>
<td>Resistance between SBU2 to SBU1</td>
</tr>
</tbody>
</table>

### MIC DETECTION THRESHOLD DATA0
Address: 1Ch
Reset Value: 8'b 0010_0000
Type: Read/Write

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7:0]</td>
<td>MIC detection threshold DATA0</td>
<td>8</td>
<td>MIC detection threshold DATA0</td>
</tr>
</tbody>
</table>

### MIC DETECTION THRESHOLD DATA1
Address: 1Dh
Reset Value: 8'b 1111_1111
Type: Read/Write

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7:0]</td>
<td>MIC detection threshold DATA1</td>
<td>8</td>
<td>MIC detection threshold DATA1</td>
</tr>
</tbody>
</table>

### I2C RESET
Address: 1Eh
Reset Value: 8'b 0000_0000
Type: W/C

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7:1]</td>
<td>Reserved</td>
<td>7</td>
<td>Reserved</td>
</tr>
<tr>
<td>0</td>
<td>I2C reset</td>
<td>1</td>
<td>0: default</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: I2C reset</td>
</tr>
</tbody>
</table>
### CURRENT SOURCE SETTING
Address: 1Fh  
Reset Value: 8'b 0000_0111  
Type: Write

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7:4]</td>
<td>Reserved</td>
<td>4</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| [3:0]  | Current Source Setting    | 4    | 1111: 1500 μA  
|        |                            |      | 0111: 700 μA  
|        |                            |      | 0001: 100 μA  
|        |                            |      | 0000: invalid                       |
**APPLICATION INFORMATION**

**Over−Voltage Protection**
FSA4480 features over−voltage protection (OVP) on receptacle side pins that switches off the internal signal routing path if the input voltage exceeds the OVP threshold.

If OVP is occurred, interrupt signal can be send by INT signal and FLAG data will provide information that which pin had OVP event.

<table>
<thead>
<tr>
<th>Condition</th>
<th>Device Disable</th>
<th>Device Enable</th>
</tr>
</thead>
<tbody>
<tr>
<td>CC_IN &lt; V_{TH_L}</td>
<td>DET = 0</td>
<td>DET = 1</td>
</tr>
<tr>
<td>CC_IN &gt; V_{TH_H}</td>
<td>DET = 0</td>
<td>DET = 0</td>
</tr>
</tbody>
</table>

**Headset Detection**
FSA4480 integrates headset unplug detection function by detecting the CC_IN voltage. The function is always active when device is enabling. DET will be high when CC_IN is low (CC_IN < 1.2 V). When CC_IN = High (CC_IN > 1.5 V), DET will be released to low.

**Audio Ground Detection and Configuration**
The function is active when control bit 0x12h bit[0] = 1 and R, L AGND switches are set to be on status. For type−C interface analog headset, the audio ground could be SBU1 pin or SBU2 pin. The function will provide autonomous detection and configuration to route MIC and audio ground signal accordingly.

**MIC Switch Auto−off Function**
The function is active during control bit 0x12h bit[2] = 1. When CC_IN is high (CC_IN > 1.5 V) and L,R, Audio ground switches are under on status, MIC switch will be off and receptacle side pin will be connected to ground for 50 μS first. Then it shows high−Z status under MIC switch is set on status.

**Audio Jack detection and configuration Start**

- REG2>= DATA1 and REG1>=DATA1
  - Hold current setting
  - MIC to SBU2, Audio ground to SBU1, Sense to GSBU1 send INT

- REG2>=REG1>DATA0 && REG1<DATA1 or REG2>DATA0>REG1
  - MIC to SBU2, Audio ground to SBU1, Sense to GSBU1 send INT

- REG1>REG2>DATA0 && REG2<DATA1 or REG1>DATA0>RGE2
  - MIC to SBU1, Audio ground to SBU2, Sense to GSBU2 send INT

- DATA0>=REG2 and DATA1>=REG1
  - Audio ground to SBU1, Sense to GSBU1, SBU2 switch open

**During detection and configuration, the R, L, Sense, MIC and Audio ground switch will be off. After detection and configuration, R and L switches will turn on according to switch configuration and timing setting. MIC, Sense and Audio ground will turn on according to detection results and timing control setting.**
**Resistance Detection**

The function is active during control bit 0x12h bit[1] = 1. It will monitor the resistance between receptacle side pins and ground. During resistance detection, the switch which is monitored will be off. The detection result will be saved in the resistance flag register. The measurement could be from 1 kΩ to 2.56 MΩ which is controlled by internal register. The detection interval can be set at 100 ms, 1 s or 10 s by register 0x16h.

**Manual Switch Control**

The function is active during control bit 0x12h bit[4] = 1 and 0x04h = FF. It will provide manual control for device. During this configuration, ADDR and INT pins will be set as logic control input.

**MANUAL SWITCH CONTROL**

(The function is active during control bit 0x12h bit[4] = 1 and 0x04h = FF. It will provide manual control for device. During this configuration, ADDR and INT pins will be set as logic control input.)

<table>
<thead>
<tr>
<th>Power</th>
<th>ENN</th>
<th>ADDR</th>
<th>INT</th>
<th>SENSE Switch</th>
<th>Headset Detection</th>
<th>USB Switch</th>
<th>Audio Switch</th>
<th>MIC/ Audio GND Switch</th>
<th>SBU by Pass Switch</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFF</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>ON</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>ON</td>
<td>L</td>
<td>0</td>
<td>0</td>
<td>OFF</td>
<td>OFF</td>
<td>ON: DP_R to DP DN_L to DN</td>
<td>OFF</td>
<td>ON: SBU1 to SBU1_H SBU2 to SBU2_H</td>
<td></td>
</tr>
<tr>
<td>ON</td>
<td>L</td>
<td>0</td>
<td>1</td>
<td>OFF</td>
<td>OFF</td>
<td>ON: DP_R to DP DN_L to DN</td>
<td>OFF</td>
<td>ON: SBU1 to SBU2_H SBU2 to SBU1_H</td>
<td></td>
</tr>
<tr>
<td>ON</td>
<td>L</td>
<td>1</td>
<td>0</td>
<td>ON: GSBU2 to SESNE</td>
<td>ON</td>
<td>OFF</td>
<td>ON: SBU1 to MIC SBU2 to Audio GND</td>
<td>OFF</td>
<td></td>
</tr>
<tr>
<td>ON</td>
<td>L</td>
<td>1</td>
<td>1</td>
<td>ON: GSBU1 to SESNE</td>
<td>ON</td>
<td>OFF</td>
<td>ON: SBU2 to MIC SBU1 to Audio GND</td>
<td>OFF</td>
<td></td>
</tr>
</tbody>
</table>
I²C INTERFACE

The FSA4480 includes a full I²C slave controller. The I²C slave fully complies with the I²C specification version 2.1 requirements. This block is designed for fast mode, 400 kHz, signals. Examples of an I²C write and read sequence are shown below figures respectively.

**Figure 6. I²C Write Example**

```
     8bits     8bits     8bits
    S | Slave Address | WR | A | Register Address K | A | Write Data | A | Write Data K+1 | A | Write Data K+2 | A | Write Data K+N−1 | A | P |
```

NOTE:  Single Byte read is initiated by Master with P immediately following first data byte.

**Figure 7. I²C Read Example**

```
     8bits     8bits     8bits     8bits
    S | Slave Address | WR | A | Register Address K | A | Slave Address | RD | A | Read Data K | A | Read Data K+1 | A | Read Data K+N−1 | NA | P |
```

NOTE:  If Register is not specified Master will begin read from current register. In this case only sequence showing in Red bracket is needed.

```
     From Master to Slave     From Slave to Master
    S     Start Condition     A     Acknowledge (SDA Low)     NA     NOT Acknowledge (SDA High)     RD     Read =1     WR     Write = 0     P     Stop Condition
```

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Figure 8. On Resistance

Figure 9. Off Leakage (I\text{Oz})

Figure 10. On Leakage

Figure 11. Power Off Leakage (I\text{off})

Figure 12. Test Circuit Load

Figure 13. Turn On/Off Waveforms under Manual Mode
Figure 14. Bandwidth

Figure 15. Channel Off Isolation

Figure 16. Adjacent Channel Crosstalk

Figure 17. Channel Off Capacitance

Figure 18. Channel On Capacitance

Figure 19. Total Harmonic Distortion (THD + N)

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Top Mark</th>
<th>Package</th>
<th>D</th>
<th>E</th>
<th>X</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>FSA4480UCX</td>
<td>6D</td>
<td>25–Ball WLCSP</td>
<td>2.24mm</td>
<td>2.28mm</td>
<td>0.32mm</td>
<td>0.34mm</td>
</tr>
</tbody>
</table>

R_L and C_L are function of application environment (see AC/DC Tables)
C_L includes test fixture and stray capacitance

RS and RT are function of application environment (see AC/DC Tables)
CROSSTALK = 20 Log (VOUT/VIN)

Capacitance Meter

F = 1 MHz

VSEL = 0 or VDD

RL and CL are function of application environment (see AC/DC Tables)
C_L includes test fixture and stray capacitance

VSEL = 0 or VDD

VOUT

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## PACKAGE DIMENSIONS

**WLCSP25 2.24x2.28x0.586**  
**CASE 567UZ**  
**ISSUE A**

### NOTES:

1. **DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.**
2. **CONTROLLING DIMENSION: MILLIMETERS**
3. **DATUM C APPLIES TO THE SPHERICAL CROWN OF THE SOLDER BALLS**

<table>
<thead>
<tr>
<th>DIM</th>
<th>MIN.</th>
<th>NOM.</th>
<th>MAX.</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0.547</td>
<td>0.586</td>
<td>0.625</td>
</tr>
<tr>
<td>A1</td>
<td>0.178</td>
<td>0.208</td>
<td>0.238</td>
</tr>
<tr>
<td>A2</td>
<td>0.360</td>
<td>0.378</td>
<td>0.396</td>
</tr>
<tr>
<td>b</td>
<td>0.24</td>
<td>0.26</td>
<td>0.28</td>
</tr>
<tr>
<td>D</td>
<td>2.250</td>
<td>2.280</td>
<td>2.310</td>
</tr>
<tr>
<td>E</td>
<td>2.210</td>
<td>2.240</td>
<td>2.270</td>
</tr>
<tr>
<td>e</td>
<td>0.40</td>
<td>BSC</td>
<td></td>
</tr>
<tr>
<td>x</td>
<td>0.325</td>
<td>0.340</td>
<td>0.355</td>
</tr>
<tr>
<td>y</td>
<td>0.305</td>
<td>0.320</td>
<td>0.335</td>
</tr>
</tbody>
</table>

---

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