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MAX30009

Low-Power, High-Performance Bioimpedance Analog Front-End

General Description

The MAX30009 is a complete Bioimpedance (BioZ) Analog Front-End (AFE) solution for wearable applications. It offers high performance for fitness, wellness, and clinical applications, and ultra-low power for long battery life. The BioZ receive channel has Electrostatic Discharge (ESD) protection, Electromagnetic Interference (EMI) filtering, internal lead-biasing, DC leads-off detection, DRVN lead-off detection, and ultra-low power lead-on detection during standby mode. The BioZ receive channel also has high input impedance, low noise, high Common-Mode Rejection Ratio (CMRR), programmable gain, various low-pass and high-pass filter options, and two high resolution analog-to-digital converters for simultaneous I and Q acquisition.

The BioZ transmit channel has a sine-wave current generator to drive AC currents into the body with a wide frequency range of 16Hz to 806kHz and a wide magnitude range of $16nA_{RMS}$ to $1.28mA_{RMS}$. The transmit channel can also operate in the sine-wave voltage and H-bridge modes. The flexible input/output MUX allows for both bipolar and tetrapolar measurements with multiple sets of electrodes.

For measurements requiring high absolute impedance accuracy such as Bioimpedance Analysis/Spectroscopy (BIA/BIS) and Automated External Defibrillator (AED) body impedance, the MAX30009 offers several calibration options. An external precision resistor can be connected to the four-wire calibration port for the highest accuracy. Internal trimmed resistors also provide high accuracy.

The PLL-based timing subsystem allows for a wide range of fine-tuned stimulus and sampling frequencies, and can be synchronized with other Analog Devices biosensors for simultaneous data collection.

The MAX30009 is available in a 2.03mm x 2.03mm, 25-bump Wafer-Level Package (WLP), operating over the -40ºC to +85ºC temperature range.

Applications

- Wearable Fitness, Wellness, and Medical Devices
- Multifrequency Body Composition Analyzers
- Non-Invasive Hemodynamic Monitors
- Automatic External Defibrillators
- Optimized Performance to Accurately Detect:
  - Respiration Rate
  - Galvanic Skin Response/Electrodermal Activity
  - Bioimpedance Spectroscopy
  - Body Composition and Fluid Analysis
  - Impedance Cardiography and Plethysmography

Benefits and Features

BIOZ

- Complete High-Performance BioZ AFE
- Simultaneous I and Q Measurement Capability
- Four-Electrode (Tetrapolar) and Two-Electrode (Bipolar) Configurations
- Ultra-Low Power Operation
  - 250 µW at 1.8V AVDD
- High-Resolution, 20-Bit Sigma Delta Analog-to-Digital Converters (ADCs)
- Wide Range of Sample Rates from 16sps to 4ksps
- Flexible and Programmable Input/Output MUX
- Low-Noise, High-Resolution Receive Channel
  - 17 Bits Effective Resolution with $1.1\mu V_{P-P}$ Noise
- High Input Impedance > 1GΩ for Extremely Low Common to Differential-Mode Conversion
- Programmable Sine-Wave Stimulus
- Low Frequency, Low Current Options for Galvanic Skin Response (GSR)/Electrodermal Activity (EDA) Starting from 16Hz and $16nA_{RMS}$
- Wide Range of Bioelectrical Impedance Analysis/Spectroscopy (BIA/BIS) Frequencies from 1kHz to 806kHz
- High Currents at High Frequencies for Impedance Cardiography (ICG) Applications (e.g.,$1.28mA_{RMS}$ at 100kHz) with Lockout for Lower Frequencies for Conformance with 60601-1
- High Input AC Dynamic Range of $>1000mV_{P-P}$
- 4-Pin In-Situ Calibration Port (4-Wire Precision Resistor) Enables High-Quality Absolute Impedance Measurements
- DC Leads-Off Detect Capability
- Ultra-Low Power Lead-On Detection with Interrupt for System Wake-Up.
  - Lead-On Detect Current: 0.7µA (typ)

SYSTEM

- Shutdown Current of 0.6µA (Typ)
- 256 Word FIFO
- Flexible PLL-Based Timing Subsystem with Internal or External Clock Source
- PLL can be Synchronized with Adjacent Biosensor AFEs (such as the MAX86176 Photoplethsymography (PPG)/Electrocardiography (ECG) AFE)
- Configurable Interrupts Reduce µC Wake-Up Time and Save Power
- High-Speed Serial Peripheral Interface (SPI) and I^2C Digital Interface

Ordering Information appears at end of data sheet.

19-101213; Rev 1; 2/22

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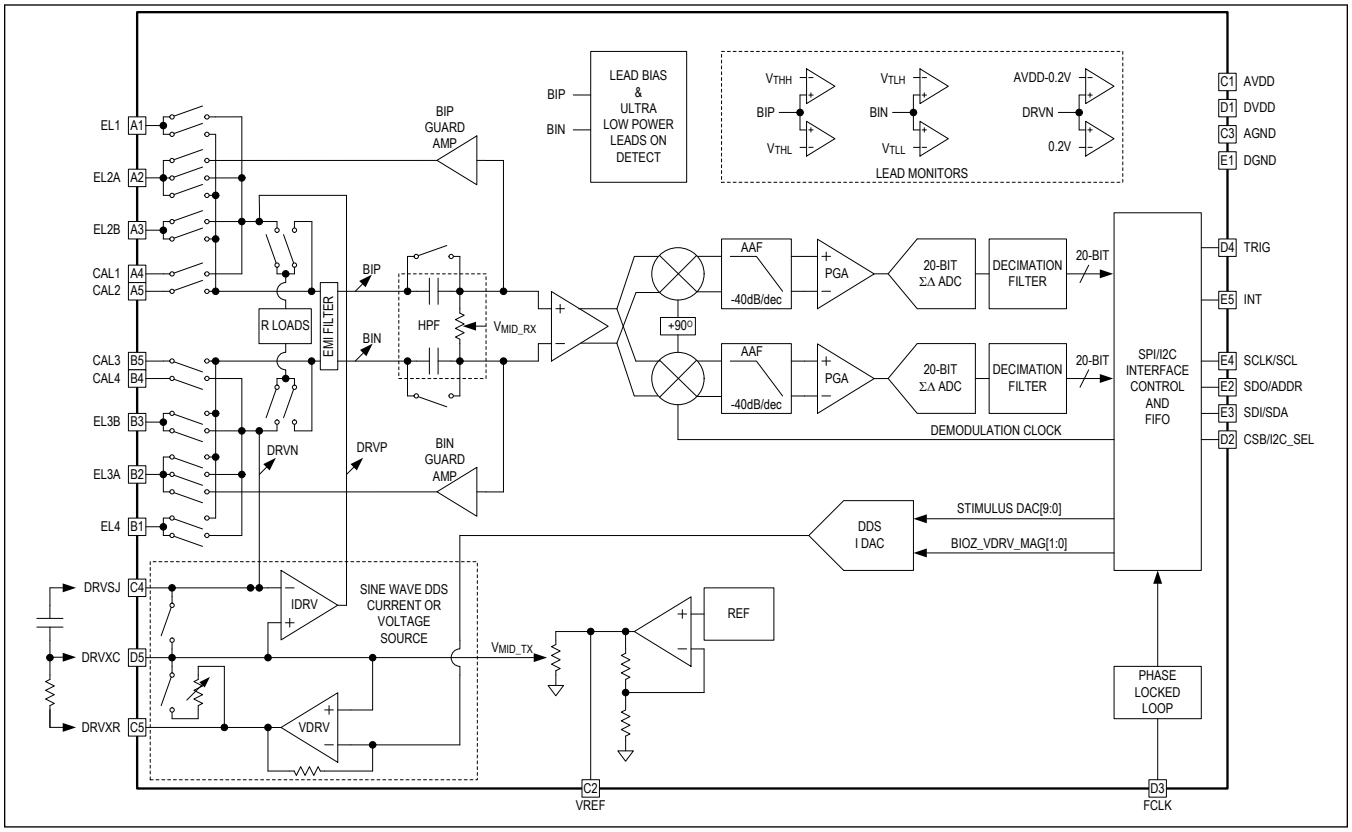
Simplified Block Diagram



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Absolute Maximum Ratings

AVDD to AGND ..... -0.3V to +2.2V
DVDD to DGND ..... -0.3V to +2.2V
AVDD to DVDD ..... -0.3V to +0.3V
DGND to AGND ..... -0.3V to +0.3V
SDI/SDA, SCLK/SCL, CSB/I2C_SEL to DGND .... -0.3V to +5.5V
SDO/ADDR to DGND ..... -0.3V to +2.2V
INT, TRIG to DGND ..... -0.3V to +5.5V

All Other Pins to AGND ..... -0.3V to +2.2V
Maximum Current into Any Pin ..... ±50mA
Operating Temperature Range ..... -40ºC to +85ºC
Junction Temperature ..... +150ºC
Storage Temperature Range ..... -65ºC to +150ºC
Lead Temperature (Soldering, 10sec) ..... +300ºC
Soldering Temperature (Reflow) ..... +260ºC

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

WLP

Package Code	N252C2+1
Outline Number	21-100494
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	52.43°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(AVDD = 1.8V, DVDD = 1.8V, FCLK = 32.768Hz, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted, *Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BIOZ Characteristics / Receive Path						
ADC Resolution				20		bits
ENOB		BIOZ_ADC_OSR = 128		16.3		bits
		BIOZ_ADC_OSR = 8		9.6		
ADC Sample Rate		Programmable, see *Timing Subsystem*		16 to 4546		sps
Phase Measurement Accuracy at 50kHz		Cole Impedance (324Ω || (232Ω + 22nF)) load at 50kHz after calibration, TA = +25°C. (*Note 2*, *Note 3*)	-0.15		+0.15	deg
		Cole Impedance (800Ω || (2500Ω + 1nF)) load at 50kHz after calibration, TA = +25°C. (*Note 2*, *Note 3*)	-0.1		+0.1	
Phase Measurement Accuracy at 16Hz		453kΩ in series with 22nF load at 16Hz after calibration (*Note 2*), T_A = +25°C. BIOZ_DC_RESTORE feedback resistance enabled in parallel with the load.		±1		deg

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Electrical Characteristics (continued)

(AVDD = 1.8V, DVDD = 1.8V, FCLK = 32.768Hz, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted, *Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Phase Measurement Accuracy at 500kHz		316Ω in series with 1nF load at 500kHz after calibration (*Note 2*), T_A = +25°C.		±1		deg
Phase Measurement Drift		Drift of impedance phase at 50kHz after calibration (*Note 2*), drift relative to T_A = +25°C.		±0.003		deg/°C
Magnitude Measurement Accuracy at 50kHz		Cole Impedance (324Ω || (232Ω + 22nF)) load at 50kHz after calibration, TA = +25°C. (*Note 2*, *Note 3*)	-0.1		+0.1	%
		Cole Impedance (800Ω || (2500Ω + 1nF)) load at 50kHz after calibration, TA = +25°C. (*Note 2*, *Note 3*)	-0.1		+0.1	
Magnitude Measurement Accuracy at 16Hz		453kΩ in series with 22nF load at 16Hz after calibration (*Note 2*), T_A = +25°C. BIOZ_DC_RESTORE feedback resistance enabled in parallel with the load.		±1		%
Magnitude Measurement Accuracy at 500kHz		316Ω in series with 1nF load at 500kHz after calibration (*Note 2*), T_A = +25°C.		±1		%
Magnitude Measurement Drift		Drift of impedance magnitude at 50kHz after calibration (*Note 2*), drift relative to T_A = +25°C		±0.017		%/°C
Impedance Repeatability		R_{BODY} = 100kΩ, conditions for GSR (*Note 4*)		2.53		Ω_{RMS}
		R_{BODY} = 680Ω, conditions for respiration (*Note 4*)		8.94		$m\Omega_{RMS}$
		R_{BODY} = 25Ω, conditions for ICG/AED body impedance (*Note 4*)		0.80		
DC Power Supply Rejection	PSRR	I_{DRV} = 64μA_{RMS}, F_BIOZ = 1kHz, BIOZ_GAIN = 10V/V, R_{BODY} = 1kΩ, V_{AVDD} = V_{DVDD} = 1.7V to 2.0V		900	7000	LSB/V
		V_{DRV} = 100mV_{P-P}, F_BIOZ = 64Hz, BIOZ_GAIN = 10V/V, V_{AVDD} = V_{DVDD} = 1.7V to 2.0V		150	1800	
Channel Gain		Selected by BIOZ_GAIN		1 to 10		V/V
I vs. Q Channel Gain Matching		3σ with Cole Impedance (324Ω || 232Ω-22nF) load at 50kHz after calibration, TA = +25°C. (*Note 2*)		0.2		%
AC Differential Input Signal		Shift from small-signal gain < 0.6%, BIOZ_GAIN = 1V/V, f_{IN} = 1kHz			1000	mV_{P-P}
Input Referred Voltage Noise (BIP, BIN)		Integrated Noise BW = 0.05 to 100Hz, Gain = 10x, Current Drive Off, BIN = BIP = VCM		1.0		μV_{RMS}
Input Referred Current Noise		DRVP and DRVN Disconnected, BIOZ_GAIN = 10V/V, F_BIOZ = 65.5kHz, SR_BIOZ = 256sps, BIOZ_DLPF = 64Hz, 200MΩ Lead Bias, BIOZ_AHPF = 5kHz		300		$fA/\sqrt{Hz}$

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Electrical Characteristics (continued)

(AVDD = 1.8V, DVDD = 1.8V, FCLK = 32.768Hz, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted, *Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Referred Offset Voltage		R_{BODY} = 0Ω, BIOZ_GAIN = 10V/V, BIOZ_AHPF = Bypass, Demodulation Disabled	-6		+6	mV
Differential Input Impedance		Lead bias disabled, BIOZ_AHPF = 100Hz		48		MΩ
		Lead bias disabled, BIOZ_AHPF = bypass		10GΩ//2 pF		
Common-Mode Input Impedance		Lead bias disabled, BIOZ_AHPF = bypass		3GΩ/2pF		
Input Analog High-Pass Filter		Programmable, see Register Map.		100 to 10,000		Hz
Input Analog High-Pass Filter Variation			-50		+100	%
Input Analog High-Pass Filter Resistor		BIOZ_AHPF[3:0] = 1000	14	24	36	MΩ
		BIOZ_AHPF[3:0] = 1001	7	12	18	
		BIOZ_AHPF[3:0] = 1010	2.6	4.8	7	
		BIOZ_AHPF[3:0] = 1011	1.3	2.4	3.3	
		BIOZ_AHPF[3:0] = 1100	0.75	1.1	1.5	
		BIOZ_AHPF[3:0] = 1101 or 1110	0.3	0.47	0.65	
Input Analog High-Pass Filter Bias Voltage	V_{MID_RX}		0.79	0.81	0.83	V
Input Leakage Current		BIP, BIN = V_{AVDD} - 0.2V or AGND + 0.2V, TA = +25°C	-3	0.1	+3	nA
I/Q Gain Matching		1kHz input, I/Q correlated with same phase, T_A = +25°C, 1σ		0.2		%
BIOZ Characteristics / Transmit Path						
DDS Sine-Wave Resolution				10		bits
Current-Drive Amplitude Resolution		See BIOZ_VDRV_MAG[1:0] and BIOZ_IDRV_RGE[1:0]		4		bits
Current-Drive Range 0		BIOZ_IDRV_RGE[1:0] = 0x0, sine-wave drive with amplitude = 16nA_{RMS}, 32nA_{RMS}, 80nA_{RMS}, 160nA_{RMS}	16		160	nA_{RMS}
Current-Drive Range 1		BIOZ_IDRV_RGE[1:0] = 0x1, sine-wave drive with amplitude = 320nA_{RMS}, 640nA_{RMS}, 1.6µA_{RMS}, 3.2µA_{RMS}	0.32		3.2	µA_{RMS}
Current-Drive Range 2		BIOZ_IDRV_RGE[1:0] = 0x2, sine-wave drive with amplitude = 6.4µA_{RMS}, 12.8µA_{RMS}, 32µA_{RMS}, 64µA_{RMS}	6.4		64	µA_{RMS}
Current-Drive Range 3		BIOZ_IDRV_RGE[1:0] = 0x3, sine-wave with amplitude = 128µA_{RMS}, 256µA_{RMS}, 640µA_{RMS}, 1.28mA_{RMS}	0.128		1.28	mA_{RMS}
Short-Circuit Current		BIOZ_DRV_MODE[1:0] = Voltage Mode, DRVP, DRVN shorted to AVDD, AGND	0.8	1.5	3	mA
		BIOZ_DRV_MODE[1:0] = H-Bridge Mode, DRVP, DRVN shorted to AVDD, AGND	2.0	3.5	6.0	

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Electrical Characteristics (continued)

(AVDD = 1.8V, DVDD = 1.8V, FCLK = 32.768Hz, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted, *Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current-Drive Accuracy		I_{DRV} ≥ $32nA_{RMS}$	-6		+6	%
		I_{DRV} = $16nA_{RMS}$	-10		+10	
Current-Drive Total Harmonic Distortion (THD)		I_{DRV} = $64\mu A_{RMS}$, f_{STIM} = 50kHz, R_{BODY} = 1kΩ. Include odd harmonics h3, h5, and h7.		0.07	0.3	%
Current-Drive Temperature Coefficient				128		ppm/°C
Current-Drive Power Supply Rejection		I_{DRV} = 64µA, DC test mode		0.1		%/V
Compliance Voltage		BIOZ_DRV_MODE[1:0] = current mode, current accuracy ±1%	0.2		V_{AVDD} - 0.2	V
Compliance Monitor Thresholds		EN_DRV_OOR = 1	0.27		V_{AVDD} - 0.35	V
Drive Frequency Range		See BIOZ_FREQ_DIV[3:0]		0.016 to 500		kHz
Drive Common-Mode Voltage	V_{MID_TX}	Voltage at DRVSJ in current mode	0.79	0.81	0.83	V
BIOZ Characteristics / Digital Filter						
Output Digital Low-Pass Filter		BIOZ_DLPF[2:0] = 0x1		0.005 x SR_BIOZ		Hz
		BIOZ_DLPF[2:0] = 0x2		0.02 x SR_BIOZ		
		BIOZ_DLPF[2:0] = 0x3		0.08 x SR_BIOZ		
		BIOZ_DLPF[2:0] ≥ 0x4		0.25 x SR_BIOZ		
Output Digital High-Pass Filter		BIOZ_DHPF[1:0] = 0x1		0.00025 x SR_BIOZ		Hz
		BIOZ_DHPF[1:0] ≥ 0x2		0.002 x SR_BIOZ		
BIOZ I/O Mux / DC Leads Off						
Full-Scale Current		Selected by LOFF_IMAG[2:0]		5.5, 11.3, 22.5, 55, 110		nA
Full-Scale Current Accuracy		LOFF_IMAG = 110nA	-40		+40	%
Comparator Threshold	V_{THH}, V_{THL}	Selectable by DC_LOFF_THRESH[3:0]	V_{MID} ±200		V_{MID} ±695	mV

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Electrical Characteristics (continued)

(AVDD = 1.8V, DVDD = 1.8V, FCLK = 32.768Hz, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted, *Note 1*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Comparator Threshold Accuracy		LOFF_THRESH = V_{MID_RX} ± 425mV		-5		+5	%
Full-Scale Electrode Resistance		LOFF_IMAG = 100nA, LOFF_THRESH = V_{MID_RX} ± 210mV			4		MΩ
		LOFF_IMAG = 10nA, LOFF_THRESH = V_{MID_RX} ± 660mV			100		
BIOZ I/O Mux / Lead Bias							
Lead Bias Impedance		Lead bias enabled.	RBIAS_VALUE = 0x0		50		MΩ
			RBIAS_VALUE = 0x1		100		
			RBIAS_VALUE = 0x2		200		
Lead Bias Voltage		Lead bias enabled		0.76	0.81	0.84	V
BIOZ I/O Mux / Internal Resisitive Loads							
Internal BIA Resistive Load Nominal Value	R_{VAL}	Selected by BMUX_RSEL			280, 600, 900, 5100		Ω
Internal GSR Resistive Load Nominal Value	R_{GSR}	Selected by BMUX_GSR_RSEL			25.7, 101, 505,100 0		kΩ
Timing Subsystem							
PLL Lock Time		Change in FCLK to FREQ_LOCK asserted, MDIV = 0x328			2	5	ms
FCLK Input Frequency		Must match CLK_FREQ_SEL			32.0 or 32.768		kHz
Maximum FCLK Rise Time (10% to 90%)	t_{RISE}	T_A = +25°C, V_{IN} = 0V or 1.8V, C_{LOAD} = 15pF			100		ns
Maximum FCLK Fall Time (90% to 10%)	t_{FALL}	T_A = +25°C, V_{IN} = 0V or 1.8V, C_{LOAD} = 15pF			100		ns
PLL External Reference Jitter		Cycle-to-cycle period, PLL_LOCK_WNDW = 0			3		ns_{RMS}
Internal FCLK	$FCLK_{INT}$	CLK_FREQ_SEL = 32.0kHz	T_A = 25°C	-1	±0.4	+1	%
			T_A = -40°C to +85°C	-2.5	±0.4	+2.5	
	$FLCK_{INT}$	CLK_FREQ_SEL = 32.768kHz	T_A = 25°C	-1	±0.4	+1	
			T_A = -40°C to +85°C	-2.5	±0.4	+2.5	
Internal Reference							
Reference Output Voltage	V_{REF}	TA = +25°C		0.985	1	1.015	V
Reference Temperature Coefficient	TC_{REF}				42		ppm/°C

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Electrical Characteristics (continued)

(AVDD = 1.8V, DVDD = 1.8V, FCLK = 32.768Hz, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted, *Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BIA Supply Current						
V_{AVDD} Supply Voltage	V_{AVDD}	Verified during Power-Supply Rejection Ratio (PSRR) tests	1.7	1.8	2.0	V
V_{DVDD} Supply Voltage	V_{DVDD}	Verified during Power-Supply Rejection Ratio (PSRR) tests	1.7	1.8	2.0	V
BIA Supply Current (BIA/BIS Example at 1KHz)	I_{AVDD} + I_{DVDD}	PLL_CLK = 16.384MHz, F_BIOZ = 1kHz (KDIV = 64, M = 500, FCLK = 32768Hz, BIOZ_DAC_OSR = 256); BIOZ_DRV_MODE = current; BIOZ_INA_MODE = low power; BIOZ_GAIN = 10V/V; SR_BIOZ = 62.5sps (NDIV = 512, BIOZ_ADC_OSR = 512); I_{MAG} = 32µA; I and Q ADCs enabled; Digital filters bypassed		926		µA
BIA Supply Current (BIA/BIS Example at 50KHz)	I_{AVDD} + I_{DVDD}	PLL_CLK = 25.591808MHz, F_BIOZ = 49.984kHz (KDIV = 2, M = 781, FCLK = 32768Hz, BIOZ_DAC_OSR = 256); BIOZ_DRV_MODE = current; BIOZ_INA_MODE = low noise; BIOZ_GAIN = 10V/V; SR_BIOZ = 48.8125sps (NDIV = 1024, BIOZ_ADC_OSR = 512); I_{MAG} = 32µA; I and Q ADCs enabled; Digital filters bypassed		1222	2700	µA
BIA Supply Current (BIA/BIS Example at 100KHz)	I_{AVDD} + I_{DVDD}	PLL_CLK = 25.591808MHz, F_BIOZ = 99.968kHz (KDIV=2, M = 781, FCLK = 32768Hz, BIOZ_DAC_OSR = 128); BIOZ_DRV_MODE = current; BIOZ_INA_MODE = low noise; BIOZ_GAIN = 10V/V; SR_BIOZ = 48.8125sps (NDIV = 1024, BIOZ_ADC_OSR = 512); I_{MAG} = 32µA; I and Q ADCs enabled; Digital filters bypassed		1227		µA
BIA Supply Current (BIA/BIS Example at 250KHz)	I_{AVDD} + I_{DVDD}	PLL_CLK = 15.990784MHz, F_BIOZ = 249.856kHz (KDIV = 1, M = 488, FCLK = 32768Hz, BIOZ_DAC_OSR = 64); BIOZ_DRV_MODE = current; BIOZ_INA_MODE = low noise; BIOZ_GAIN = 10V/V; SR_BIOZ = 61sps (NDIV = 512, BIOZ_ADC_OSR = 512); I_{MAG} = 32µA; I and Q ADCs enabled; Digital filters bypassed		1148	2700	µA
BIA Supply Current (BIA/BIS Example at 500KHz)	I_{AVDD} + I_{DVDD}	PLL_CLK = 15.990784MHz, F_BIOZ = 499.712kHz (KDIV = 1, M = 488, FCLK = 32768Hz, BIOZ_DAC_OSR = 32); BIOZ_DRV_MODE = current; BIOZ_INA_MODE = low noise; BIOZ_GAIN = 10V/V; SR_BIOZ = 61sps (NDIV = 512, BIOZ_ADC_OSR = 512); I_{MAG} = 32µA; I and Q ADCs enabled; Digital filters bypassed		1192		µA

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Electrical Characteristics (continued)

(AVDD = 1.8V, DVDD = 1.8V, FCLK = 32.768Hz, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted, *Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BIA Supply Current (Respiration Current Drive Example)	I_{AVDD} + I_{DVDD}	PLL_CLK = 16.384MHz, F_BIOZ = 32kHz (KDIV = 2, M = 500, FCLK = 32768HZ, BIOZ_DAC_OSR = 256); BIOZ_DRV_MODE = current; BIOZ_INA_MODE = low power; BIOZ_GAIN = 10V/V; SR_BIOZ = 62.5sps (NDIV = 512, BIOZ_ADC_OSR = 512); I_{MAG} = 32µA; In-phase ADC only; BIOZ_DHPF = bypass, BIOZ_DLPF = 0.08 x SR_BIOZ		943	2300	µA
BIA Supply Current (Respiration H-Bridge Example)	I_{AVDD} + I_{DVDD}	PLL_CLK = 16.384MHz, F_BIOZ = 32kHz (KDIV = 2, M = 500, FCLK = 32768Hz, BIOZ_DAC_OSR = 256); BIOZ_DRV_MODE = current; BIOZ_INA_MODE = low power; BIOZ_GAIN = 10V/V; SR_BIOZ = 62.5sps (NDIV = 512, BIOZ_ADC_OSR = 512); No load; In-phase ADC only; BIOZ_DHPF = bypass, BIOZ_DLPF = 0.08 x SR_BIOZ		328		µA
BIA Supply Current (ICG Example)	I_{AVDD} + I_{DVDD}	PLL_CLK = 25.591808MHz, F_BIOZ = 99.968kHz (KDIV = 1, M = 781, FCLK = 32768Hz, BIOZ_DAC_OSR = 256); BIOZ_DRV_MODE = current; BIOZ_INA_MODE = low noise; BIOZ_GAIN = 10V/V; SR_BIOZ = 97.625sps (NDIV = 1024, BIOZ_ADC_OSR = 256); I_{MAG} = 1.28mA; In-phase ADC only; BIOZ_DHPF = 0.002 x SR_BIOZ, BIOZ_DLPF = 0.25 x SR_BIOZ		2280		µA
BIA Supply Current (GSR/EDA Example)	I_{AVDD} + I_{DVDD}	PLL_CLK = 14.024704MHz, F_BIOZ = 53.5Hz (KDIV = 1024, M = 428, FCLK = 32768Hz, BIOZ_DAC_OSR = 256); BIOZ_DRV_MODE = current; BIOZ_INA_MODE = low power; BIOZ_GAIN = 1V/V; SR_BIOZ = 53.5sps (NDIV = 512, BIOZ_ADC_OSR = 512); I_{MAG} = 320nA; In-phase ADC only; Digital filters bypassed		353	680	µA
Shutdown Current	I_{AVDD} + I_{DVDD}	T_A = +25°C		1.0	3	µA
		-40°C < T_A < +85°C			25	
Digital I/O Characteristics						
Input Voltage Low	V_{IL}	SDI/SDA, SCLK/SCL, TRIG, CSB/ I2C_SEL, FCLK			0.4	V
Input Voltage High	V_{IH}	SDI/SDA, SCLK/SCL, TRIG, CSB/ I2C_SEL, FCLK	1.4			V
Input Hysteresis	V_{HYS}	SDI/SDA, SCLK/SCL, TRIG, CSB/ I2C_SEL, FCLK		430		mV
Input Capacitance	C_{IN}	SDI/SDA, SCLK/SCL, TRIG, CSB/ I2C_SEL, FCLK		10		pF

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Electrical Characteristics (continued)

(AVDD = 1.8V, DVDD = 1.8V, FCLK = 32.768Hz, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted, *Note 1*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Leakage Current	I_{IN}	SDI/SDA, SCLK/ SCL, TRIG, CSB/ I2C_SEL, FCLK	T_A = +25°C, V_{IN} = 0V or 1.8V	-0.1	0.01	+0.1	µA
Output Voltage Low	V_{OL}	SDO/ADDR, INT	I_{SINK} = 4mA			0.4	V
Output Voltage High	V_{OH}	SDO/ADDR, INT	I_{SOURCE} = 4mA	V_{DVDD} - 0.4			V
Open-Drain Output Voltage Low	V_{OL_OD}	INT_OCFG = 0x0	I_{SINK} = 4mA			0.4	V
I²C Timing Characteristics (*Note 3*)							
I²C Write Address		SDO/ADDR = 0			D0		Hex
		SDO/ADDR = 1			D2		
I²C Read Address		SDO/ADDR = 0			D1		Hex
		SDO/ADDR = 1			D3		
Serial Clock Frequency	f_{SCL}			0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}			1.3			µs
Hold Time START and Repeat START Condition	$t_{HD,STA}$			0.6			µs
SCL Pulse-Width Low	t_{LOW}			1.3			µs
SCL Pulse-Width High	t_{HIGH}			0.6			µs
Setup Time for a Repeated START Condition	$t_{SU,STA}$			0.6			µs
Data Hold Time	$t_{HD,DAT}$			0		900	ns
Data Setup Time	$t_{SU,DAT}$			100			ns
Setup Time for STOP Condition	$t_{SU,STO}$			0.6			µs
Pulse-Width of Suppressed Spike	t_{SP}			0		50	ns
Bus Capacitance	C_B					400	pF
SDA and SCL Receiving Rise Time	t_R	C_B = bus capacitance in pF		20 + 0.1 x C_B		300	ns
SDA and SCL Receiving Fall Time	t_F	C_B = bus capacitance in pF		20 + 0.1 x C_B		300	ns
SDA Transmitting Fall Time	t_{TF}	C_B = bus capacitance in pF		20 + 0.1 x C_B		300	ns
SPI Timing Characteristics (*Note 3*)							
SCLK Frequency	f_{SCLK}			0.1		24	MHz
SCLK Period	t_{CP}			40			ns
SCLK Pulse-Width High	t_{CH}			18			ns
SCLK Pulse-Width Low	t_{CL}			18			ns

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Electrical Characteristics (continued)

(AVDD = 1.8V, DVDD = 1.8V, FCLK = 32.768Hz, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted, *Note 1*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CSB Fall to SCLK Rise Setup Time	t_{CSS0}	Applies to first SCLK rising edge after CSB goes low.		20			ns
CSB Fall to SCLK Rise Hold Time	t_{CSH0}	Applies to inactive rising edge preceding first rising edge.		5			ns
Last SCLK Rise to CSB Rise	t_{CSH1}	Applies to last SCLK rising edge in a transaction.		20			ns
Last SCLK Rise to Next CSB Fall	t_{CSF}	Applies to last SCLK rising edge to next CSB falling edge (new transaction).		60			ns
CSB Pulse-Width High	t_{CSPW}			40			ns
SDI to SCLK Rise Setup Time	t_{DS}			5			ns
SDI to SCLK Rise Hold Time	t_{DH}			5			ns
SCLK Fall to SDO Transition	t_{DOT}	C_{LOAD} = 30pF				15	ns
CSB Fall to SDO Enabled	t_{DOE}	C_{LOAD} = 0pF		10			ns
CSB Rise to SDO Hi-Z	t_{DOZ}	Disable Time				5	ns
TRIG Pulse-Width	t_{TRIG}			1 x t_{FCLK}			s
ESD PROTECTION							
E1, E2A, E2B, C1, C2, C3, C4, E3A, E3B, E4		IEC61000-4-2	Contact Discharge	±8			kV
			Air Discharge	±6			

Note 1: Limits are 100% tested at TA = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. All register settings use default values, unless otherwise noted in specific EC conditions.

Note 2: Overall accuracy must include calibration resistor accuracy and overall calibration accuracy. Calibration uses an external 32.768kHz, 2.5nsRMS jitter, ±5ppm TC oscillator with a 680Ω external calibration resistor. The calibration resistor and Cole impedance are measured to within 0.05% magnitude and 0.1° phase accuracy using a calibrated Zurich Instruments MFIA.

Note 3: Guaranteed by design and characterization. Not tested in production.

Note 4: a. BIOZ_DRV_MODE = 0x0, IDRV = 160nARMS, F_BIOZ = 16Hz, SR_BIOZ = 16sps, BIOZ_GAIN = 10V/V, BIOZ_DLPF = 0x4, BIOZ_AHPF = 24MΩ with external 47nF BIP and BIN capacitors. Effective signal band = DC to 4Hz.
b. BIOZ_DRV_MODE = 0x0, IDRV = 32µARMS, F_BIOZ = 32kHz, SR_BIOZ = 31.25sps, BIOZ_GAIN = 10V/V, BIOZ_DLPF = 0x3, BIOZ_AHPF = 2kHz. Effective signal band = DC to 2.5Hz.
c. BIOZ_DRV_MODE = 0x0, IDRV = 1.28mARMS, F_BIOZ = 64kHz, SR_BIOZ = 250sps, BIOZ_GAIN = 10V/V, BIOZ_AHPF = 5kHz. Effective signal band = DC to 62.5Hz.

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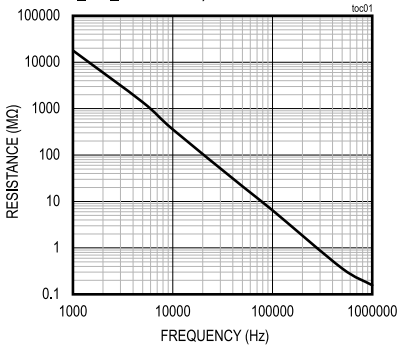
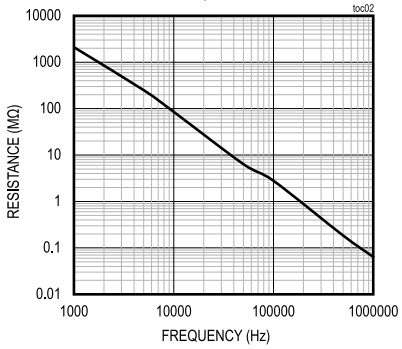
Typical Operating Characteristics

(V_{DVDD} = V_{AVDD} = +1.8V, T_A = +25°C, unless otherwise noted.)

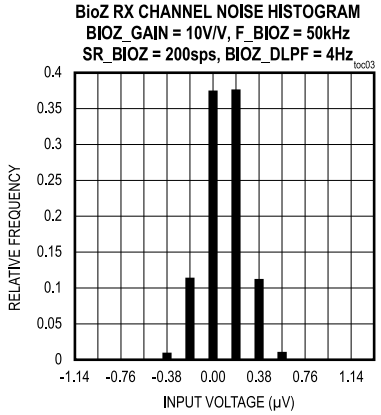
BioZ RX CHANNEL DIFFERENTIAL INPUT RESISTANCE
EN_INT_INLOAD = 1, LEAD BIAS DISABLED



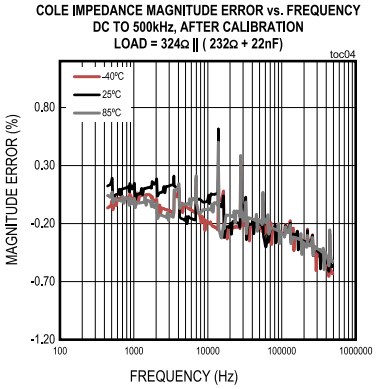
BioZ RX CHANNEL COMMON MODE INPUT RESISTANCE
EN_INT_INLOAD = 1, LEAD BIAS DISABLED



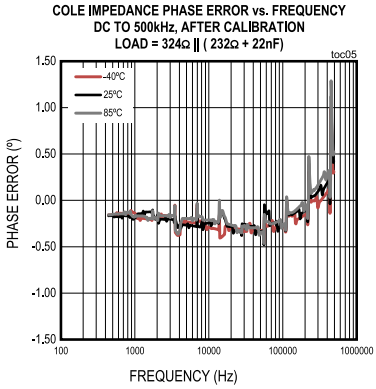
BioZ RX CHANNEL NOISE HISTOGRAM
BIOZ_GAIN = 10V/V, F_BIOZ = 50kHz
SR_BIOZ = 200sps, BIOZ_DLPF = 4Hz



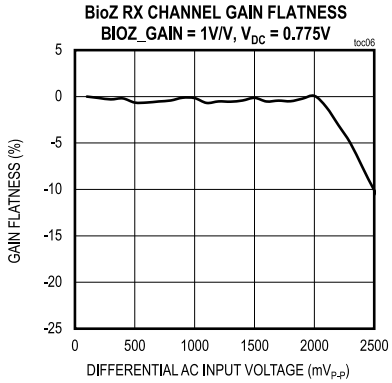
COLE IMPEDANCE MAGNITUDE ERROR vs. FREQUENCY
DC TO 500kHz, AFTER CALIBRATION
LOAD = 324Ω || (232Ω + 22nF)



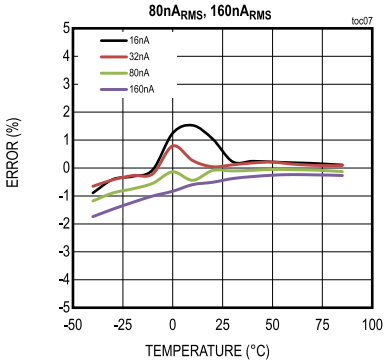
COLE IMPEDANCE PHASE ERROR vs. FREQUENCY
DC TO 500kHz, AFTER CALIBRATION
LOAD = 324Ω || (232Ω + 22nF)



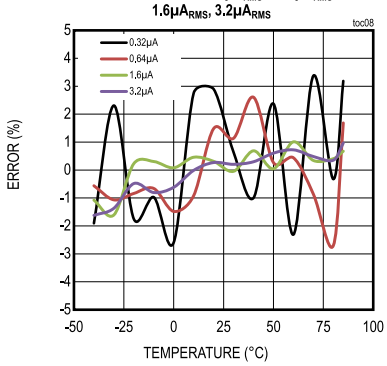
BioZ RX CHANNEL GAIN FLATNESS
BIOZ_GAIN = 1V/V, V_{DC} = 0.775V



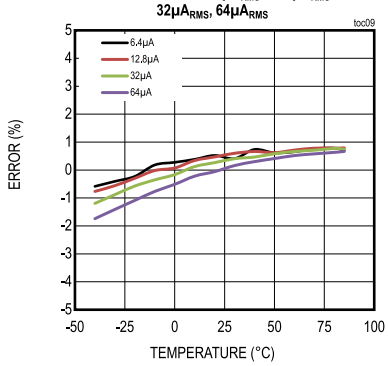
BIOZ DRIVE CURRENT ERROR vs. TEMPERATURE
BIOZ CURRENT = 16nA_{RMS}, 32nA_{RMS},
80nA_{RMS}, 160nA_{RMS}



BIOZ DRIVE CURRENT ERROR vs. TEMPERATURE
BIOZ CURRENT = 0.32$µA_{RMS}$, 0.64$µA_{RMS}$,
1.6$µA_{RMS}$, 3.2$µA_{RMS}$



BIOZ DRIVE CURRENT ERROR vs. TEMPERATURE
BIOZ CURRENT = 6.4$µA_{RMS}$, 12.8$µA_{RMS}$,
32$µA_{RMS}$, 64$µA_{RMS}$



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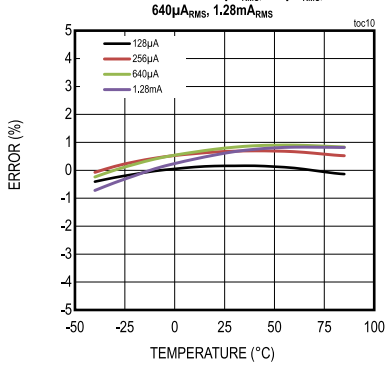
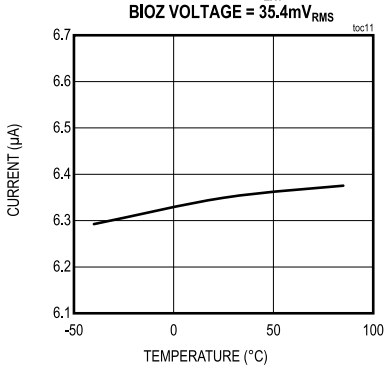
Typical Operating Characteristics (continued)

(V_{DVDD} = V_{AVDD} = +1.8V, T_A = +25°C, unless otherwise noted.)

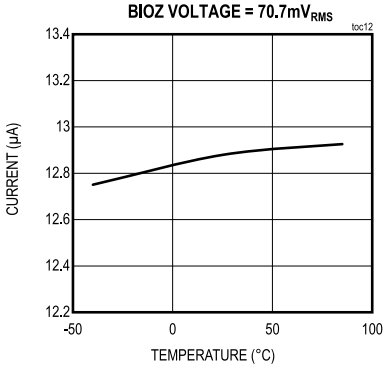
BIOZ DRIVE CURRENT ERROR vs. TEMPERATURE
BIOZ CURRENT = 128μA$_{RMS}$, 256μA$_{RMS}$, 640μA$_{RMS}$, 1.28mA$_{RMS}$



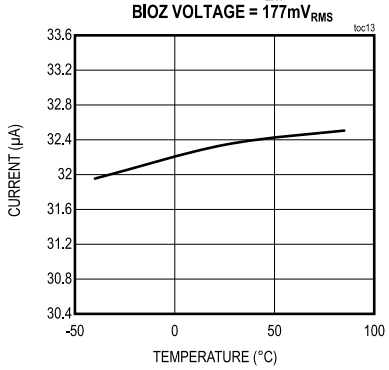
BIOZ DRIVE CURRENT vs. TEMPERATURE
BIOZ_EXT_RES = 1, R_{EXT} = 5.525kΩ
BIOZ VOLTAGE = 35.4mV$_{RMS}$



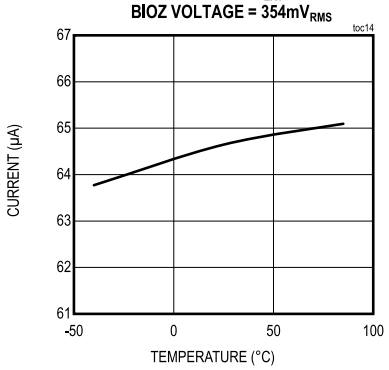
BIOZ DRIVE CURRENT vs. TEMPERATURE
BIOZ_EXT_RES = 1, R_{EXT} = 5.525kΩ
BIOZ VOLTAGE = 70.7mV$_{RMS}$



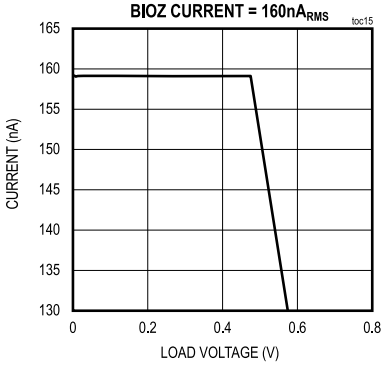
BIOZ DRIVE CURRENT vs. TEMPERATURE
BIOZ_EXT_RES = 1, R_{EXT} = 5.525kΩ
BIOZ VOLTAGE = 177mV$_{RMS}$



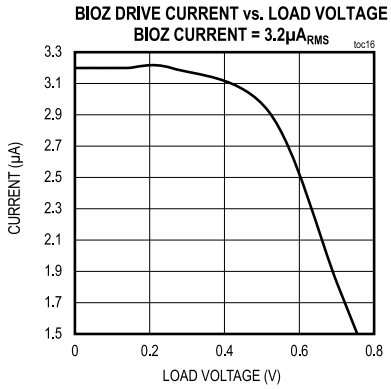
BIOZ DRIVE CURRENT vs. TEMPERATURE
BIOZ_EXT_RES = 1, R_{EXT} = 5.525kΩ
BIOZ VOLTAGE = 354mV$_{RMS}$



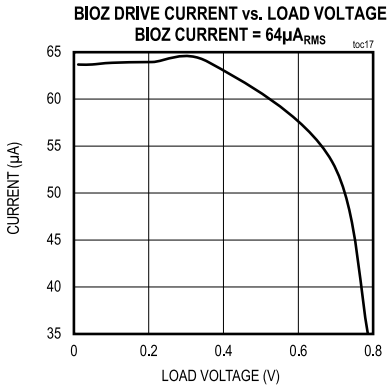
BIOZ DRIVE CURRENT vs. LOAD VOLTAGE
BIOZ CURRENT = 160nA$_{RMS}$



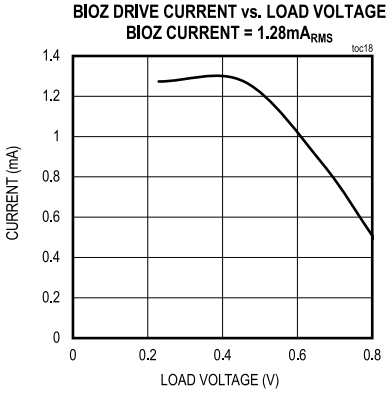
BIOZ DRIVE CURRENT vs. LOAD VOLTAGE
BIOZ CURRENT = 3.2μA$_{RMS}$



BIOZ DRIVE CURRENT vs. LOAD VOLTAGE
BIOZ CURRENT = 64μA$_{RMS}$



BIOZ DRIVE CURRENT vs. LOAD VOLTAGE
BIOZ CURRENT = 1.28mA$_{RMS}$



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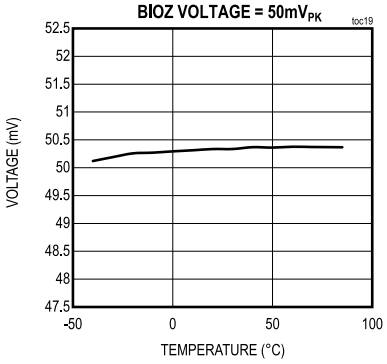
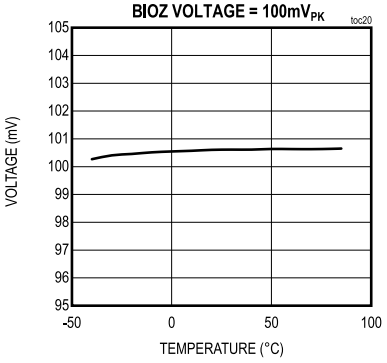
Typical Operating Characteristics (continued)

(V_{DVDD} = V_{AVDD} = +1.8V, T_A = +25°C, unless otherwise noted.)

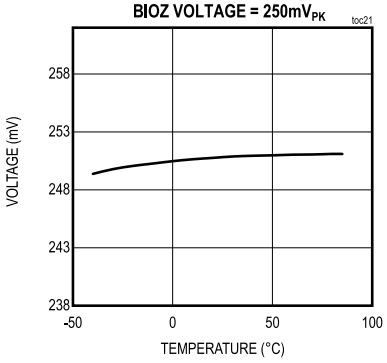
BIOZ DRIVE VOLTAGE vs. TEMPERATURE
BIOZ VOLTAGE = 50mV$_{PK}$



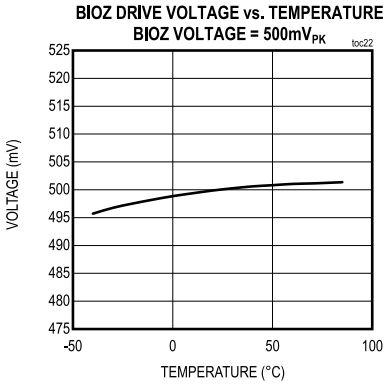
BIOZ DRIVE VOLTAGE vs. TEMPERATURE
BIOZ VOLTAGE = 100mV$_{PK}$



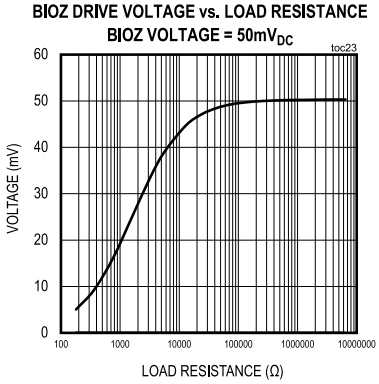
BIOZ DRIVE VOLTAGE vs. TEMPERATURE
BIOZ VOLTAGE = 250mV$_{PK}$



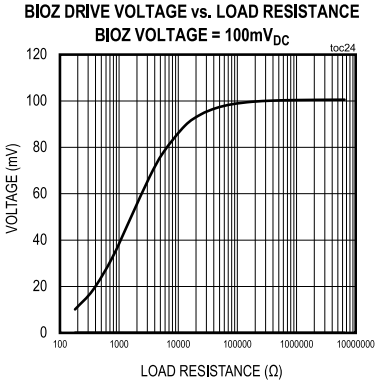
BIOZ DRIVE VOLTAGE vs. TEMPERATURE
BIOZ VOLTAGE = 500mV$_{PK}$



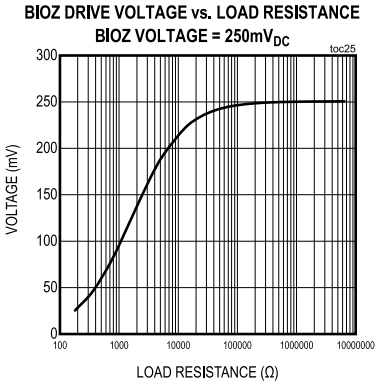
BIOZ DRIVE VOLTAGE vs. LOAD RESISTANCE
BIOZ VOLTAGE = 50mV$_{DC}$



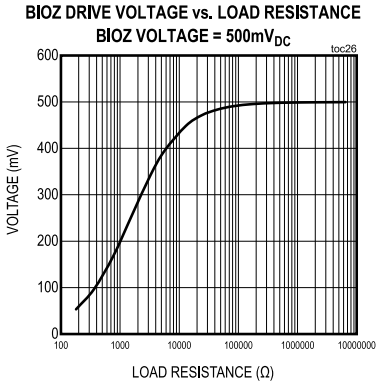
BIOZ DRIVE VOLTAGE vs. LOAD RESISTANCE
BIOZ VOLTAGE = 100mV$_{DC}$



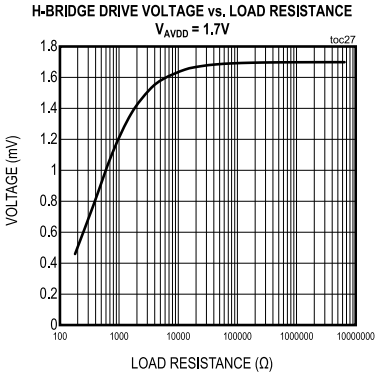
BIOZ DRIVE VOLTAGE vs. LOAD RESISTANCE
BIOZ VOLTAGE = 250mV$_{DC}$



BIOZ DRIVE VOLTAGE vs. LOAD RESISTANCE
BIOZ VOLTAGE = 500mV$_{DC}$



H-BRIDGE DRIVE VOLTAGE vs. LOAD RESISTANCE
V_{AVDD} = 1.7V



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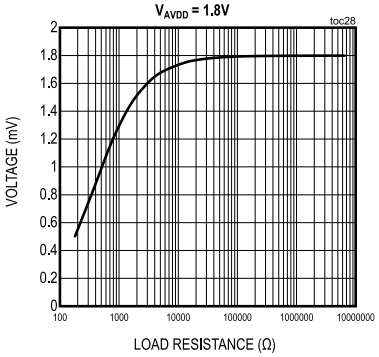
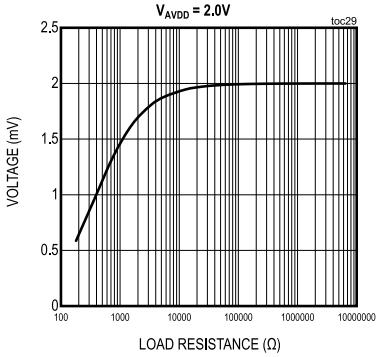
Typical Operating Characteristics (continued)

(V_{DVDD} = V_{AVDD} = +1.8V, T_A = +25°C, unless otherwise noted.)

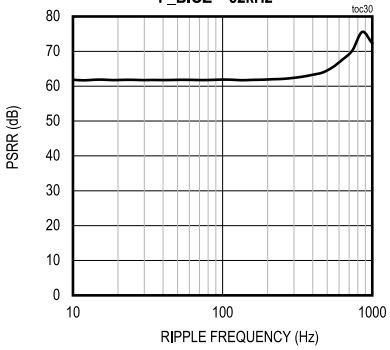
H-BRIDGE DRIVE VOLTAGE vs. LOAD RESISTANCE
V_{AVDD} = 1.8V



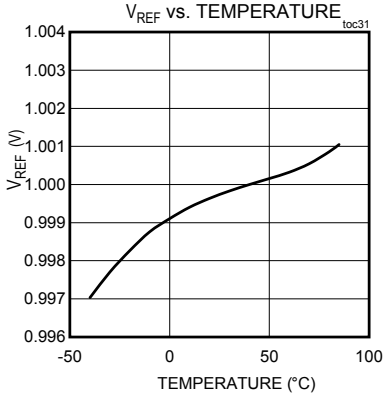
H-BRIDGE DRIVE VOLTAGE vs. LOAD RESISTANCE
V_{AVDD} = 2.0V



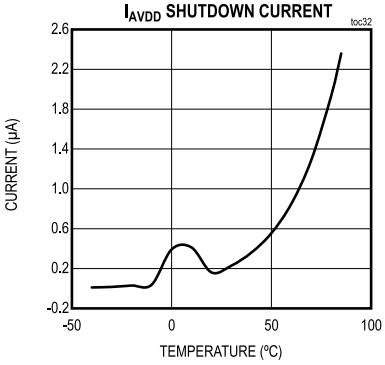
BIOZ MEASUREMENT PSRR
CONDITIONS FOR BIA
F_BIOZ = 32kHz



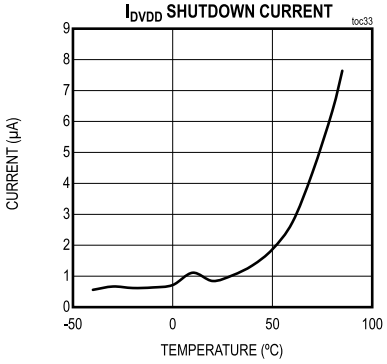
V_{REF} vs. TEMPERATURE



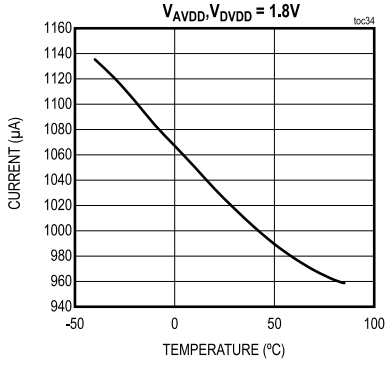
I_{AVDD} SHUTDOWN CURRENT



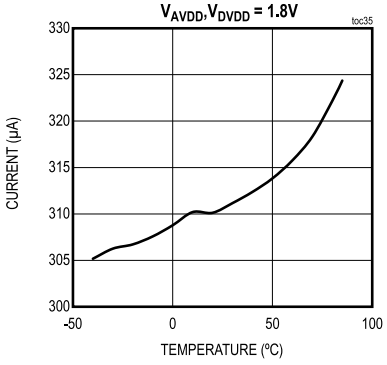
I_{DVDD} SHUTDOWN CURRENT



AVERAGE (I_{AVDD}+I_{DVDD}) SUPPLY CURRENT
RESPIRATION WITH CURRENT DRIVE
V_{AVDD},V_{DVDD} = 1.8V



AVERAGE (I_{AVDD}+I_{DVDD}) SUPPLY CURRENT
RESPIRATION WITH H-BRIDGE DRIVE
V_{AVDD},V_{DVDD} = 1.8V



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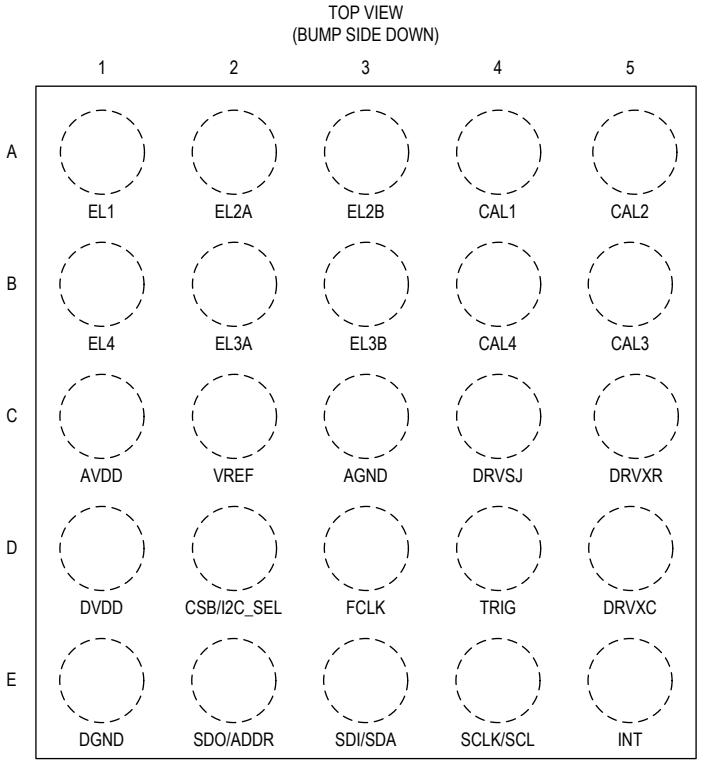
Pin Configuration

WLP



25 WLP (5x5)
2.03mm x 2.03mm, 0.4mm PITCH

Pin Description

PIN	NAME	FUNCTION
Power		
C1	AVDD	Analog Core Supply Voltage. Bypass to AGND with a 0.1µF and a 10µF X5R 0603 capacitor or equivalent effective capacitance.
D1	DVDD	Digital Core Supply Voltage. Bypass to DGND with a 0.1µF and a 10µF X5R 0603 capacitor or equivalent effective capacitance.
C3	AGND	Analog Power and Reference Ground. Connect to the PCB ground plane.
E1	DGND	Digital Ground for both Digital Core and I/O Pad Drivers. Recommended to connect to AGND plane.
Electrode Connections		
A1	EL1	Electrode 1 Connection. EL1 is normally connected to the DRVP current generator output, but can be switched to the receive channel's BIP input under program control.
A2	EL2A	Electrode 2A Connection. EL2A or EL2B are normally connected to the receive channel's BIP input, but can be switched to connect to the DRVP current generator output under program control. Two EL2 inputs are provided to use the device for both GSR/EDA applications that require an external AC-coupling capacitor and BIA/BIS applications that use the internal AHPF, and thus do not require an external AC-coupling capacitor.
A3	EL2B	Electrode 2B Connection. See description for EL2A.

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Pin Description (continued)

PIN	NAME	FUNCTION
B1	EL4	Electrode 4 Connection. EL4 is normally connected to the DRVN current generator output, but can be switched to the receive channel's BIN input under program control.
B2	EL3A	Electrode 3A Connection. EL3A or EL3B are normally connected to the receive channel's BIN input, but can be switched to connect to the DRVN current generator output under program control. Two EL3 inputs are provided to use the device for both GSR/EDA applications that require an external AC-coupling capacitor and BIA/BIS applications that use the internal AHPF, and thus do not require an external AC-coupling capacitor.
B3	EL3B	Electrode 3B Connection. See description for EL3A.
Calibration Support		
A4	CAL1	Calibration Port 1. Connects the internal DRVP node to an external reference resistor when calibration is enabled.
A5	CAL2	Calibration Port 2. Connects the internal BIP node to an external reference resistor when calibration is enabled.
B5	CAL3	Calibration Port 3. Connects the internal BIN node to an external reference resistor when calibration is enabled.
B4	CAL4	Calibration Port 4. Connects the internal DRVN node to an external reference resistor when calibration is enabled.
PLL		
D3	FCLK	External Clock Input. Connect to a 32.0kHz or 32.768kHz external clock source (optional). When not used, it can be left unconnected.
Control Interface		
E4	SCLK/SCL	SPI Clock in SPI Mode or I^2C Clock in I^2C Mode.
E3	SDI/SDA	SPI Data Input in SPI Mode or I^2C Data Input and Output in I^2C Mode.
E2	SDO/ADDR	SPI Data Output in SPI Mode or I^2C Address Select in I^2C Mode. Do not leave unconnected.
D2	CSB/ I2C_SEL	Active-Low Chip Select Input in SPI Mode. Pull high or connect to DVDD to select I^2C Mode. Do not leave unconnected.
E5	INT	Interrupt Output. INT is a programmable active-high/active-low status output. It can be used to interrupt an external device. When not used, it can be left unconnected.
D4	TRIG	PLL Synchronization Input. When not used, connect to DGND.
Reference		
C2	V_{REF}	ADC Reference Buffer Output. Connect a 1µF X5R ceramic capacitor between V_{REF} and AGND.
C4	DRVSJ	Drive Summing Junction Connection. Virtual AC ground in current mode.
C5	DRVXR	Drive Amplifier External Resistor. Connect a precision resistor between DRVXR and DRVXC if setting the BioZ drive current externally. Leave unconnected if using internal current settings.
D5	DRVXC	Drive Amplifier External Capacitor. Connect a 47nF capacitor between DRVXC and DRVSJ to AC-couple the V_{DRV} and I_{DRV} amplifiers in sine-wave current-drive applications. Otherwise, short DRVXC to DRVSJ.

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Detailed Description

The MAX30009 is a complete, integrated data acquisition system ideal for respiration, Galvanic Skin Response (GSR) and Electrodermal Activity (EDA), Bioimpedance Analysis/Spectroscopy (BIA/BIS), Impedance Cardiography (ICG), and numerous other applications. It is designed for the demanding requirements of medical, mobile, and wearable devices, and requires minimal external hardware components for integration.

The BioZ transmit channel has an independent current stimulus circuit to provide injected body currents. The stimulus current generation circuit can be supplied in a four-electrode (tetrapolar) as well as two-electrode (bipolar) manner. This injected current is programmable and available over a wide frequency range (16Hz to 806kHz) and a wide range of stimulus current magnitudes (16nA_{RMS}, up to 1.28mA_{RMS} maximum). These ranges support Galvanic Skin Response (GSR) and Electrodermal Activity (EDA) measurements, Bioimpedance Analysis/Spectroscopy (BIA/BIS) applications, and Impedance Cardiography (ICG) measurements such as cardiac output and stroke volume, or Impedance Plethysmography (IPG) measurements.

The BioZ receive channel also has high input impedance, low noise, high Common-Mode Rejection Ratio (CMRR), programmable gain, various low-pass and high-pass filter options, two high-resolution analog-to-digital converters, and simultaneous I and Q measurement capability to provide resistance and reactance measurements for BIA/BIS applications. It also includes DC lead-off detection, drive lead-off detection, ultra-low-power lead-on detection during standby mode, and extensive calibration features and programmable resistive loads for built-in self-test. Soft power-up sequencing ensures no large transients are injected into the electrodes.

The MAX30009 provides a calibration port for a four-wire external precision reference resistance to use during calibration. This calibration is required when using the MAX30009 for bioimpedance measurements needing absolute accuracy such as BIA/BIS or Automated External Defibrillator (AED) body-impedance. The four-wire calibration port can also be used to support multiple calibration resistances. Alternatively, there are trimmed load resistors internal to the device that can be used for calibration, but they are not as accurate as using an external reference resistor.

The MAX30009 is fully adjustable through software registers and the digital output data is stored in a 256-word FIFO. The FIFO allows the MAX30009 to be connected to a microcontroller or processor on a shared I^2C or Serial Peripheral Interface (SPI) bus. The MAX30009 operates in fully autonomous mode for low-power battery applications. The MAX30009 operates on a 1.8V main supply voltage, and can be configured for low-power consumption, enabling long battery life.

Timing Subsystem

The MAX30009 timing subsystem is shown in Figure 1, which includes all the register bits and formulas needed for setting the BioZ sample rate and stimulus frequency. REF_CLK is sourced either from an external oscillator on the FCLK or from the internal slow oscillator clock INT_FCLK, depending on the REF_CLK_SEL[6](0x1D) setting. The MAX30009 timing system offers a great deal of flexibility. However, certain considerations must be taken into account when configuring the timing system. The following sections describe these considerations in detail.

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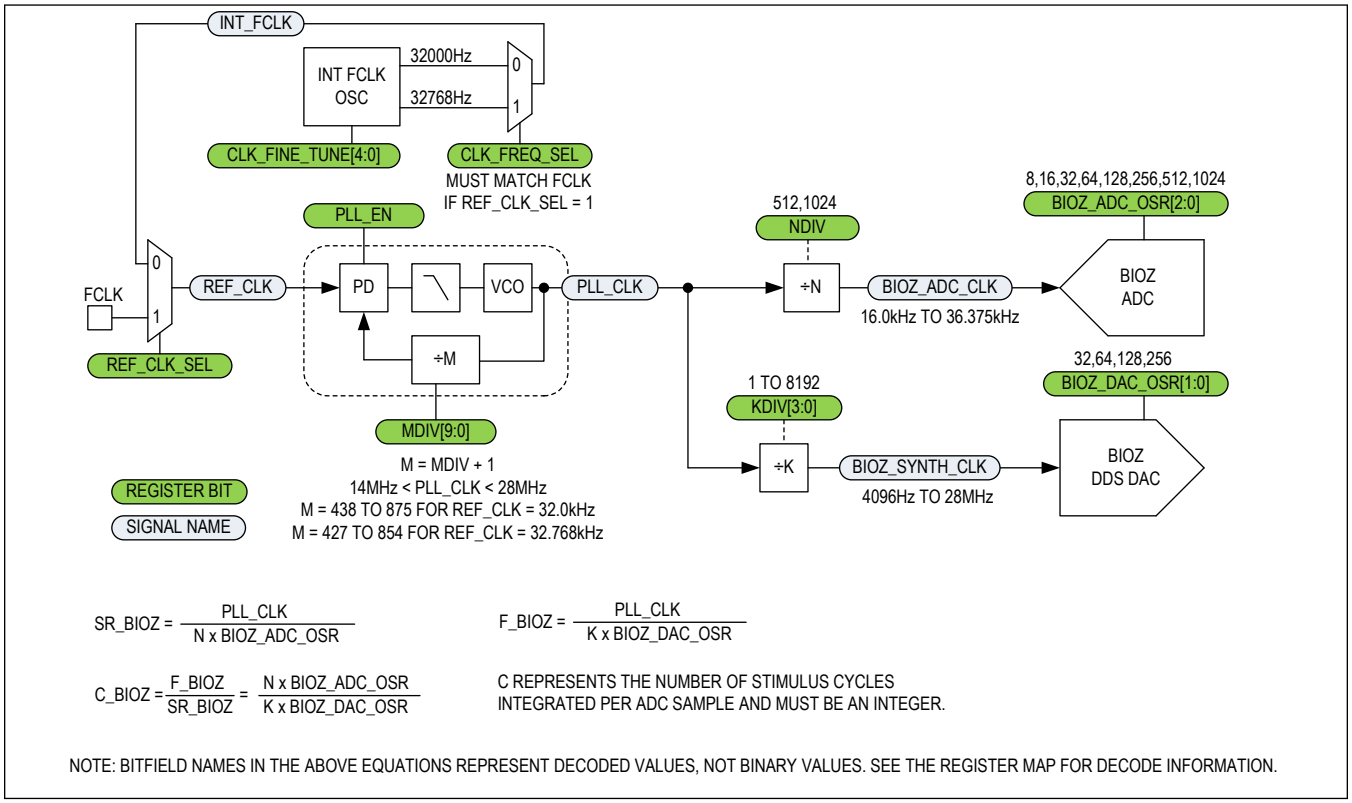

Figure 1. Timing Subsystem

Clock Sources

The MAX30009 timing system incorporates two internal slow oscillators, 32.0kHz and 32.768kHz, and the oscillator with the desired frequency can be selected by setting CLK_FREQ_SEL[5](0x1D). If REF_CLK_SEL[6](0x1D) = 0, the internal slow oscillator selected by CLK_FREQ_SEL provides the reference clock to the PLL circuit used as the time base for the BioZ channel. If REF_CLK_SEL = 1, the oscillator on the FCLK (either 32.0kHz or 32.768kHz) becomes the source of REF_CLK. Even when using the external oscillator on FCLK, the CLK_FREQ_SEL must be set according to the frequency of the external clock source. Use a low-jitter external oscillator with < 347ppm of frequency accuracy to meet IEC60601-2-47 timing accuracy compliance. The FCLK source must be an active-drive clock, not only a crystal.

The two internal slow oscillators, 32.0kHz and 32.768kHz in MAX30009, are factory trimmed and exhibit a drift with temperature (primary cause of drift) of less than ±1% over the temperature range of 0°C to +50°C. If this level of stability is inadequate, then the MAX30009 offers a fine adjust register CLK_FINE_TUNE[4:0](0x1D), which can be used in combination with a highly stable crystal based Real-Time Clock (RTC) oscillator in the host microcontroller to trim out the drift of the on-chip slow oscillator. By counting the time between the MAX30009 generated interrupts using the microcontroller-based RTC, it is possible to compute the error in the slow oscillator frequency and trim it to within ±0.1% (typ) of the microcontroller-based RTC. Using this approach, it is possible to achieve accuracy near that of a crystal oscillator as the phase noise of the MAX30009 slow oscillator is low and the drift is primarily due to temperature.

Phase-Locked Loop (PLL) and PLL Synchronization

The MAX30009 timing subsystem in Figure 1 allows the use of an internal PLL synchronized to either an internal or external clock source used by the BioZ channel.

The PLL generates an output clock (PLL_CLK) that operates over a 14MHz to 28MHz frequency range. The frequency of PLL_CLK is selected by the frequency of REF_CLK and the M divider value, which is set in MDIV[9:0](0x18, 0x19),

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where M = MDIV + 1.

The 10-bit MDIV register field must be set such that the PLL output frequency (PLL_CLK) is between 14MHz and 28MHz. For a reference clock of 32.768kHz, this means a valid MDIV range is 426 to 853 (M = 427 to 854). For a reference clock of 32.0kHz, this means a valid MDIV range of 437 to 874 (M = 438 to 875).

Soft-reset using RESET[0](0x11) is not allowed when PLL is enabled (PLL_EN[0](0x18) = 1). The BioZ reference must be enabled (BIOZ_BG_EN[2](0x20) = 1) before PLL_EN is set to 1, and can take up to 6ms to settle.

Sequence of Operation When PLL is Used

When enabling or disabling PLL, the proper sequence of operations must be followed. This section describes the recommended sequence of operations for various scenarios when PLL is used.

Enabling and Disabling the PLL

The following sequence is recommended when enabling and disabling the PLL.

- Disable BioZ, if enabled.
- Enable PLL by setting PLL_EN to 1.
- Wait for PLL to lock using either the FREQ_LOCK[3](0x02) or PHASE_LOCK[2](0x02) status bits.
- Enable BioZ I and Q, as needed.
- Disable BioZ when data collection is done.
- Disable PLL by setting PLL_EN to 0.

Entering and Exiting Shutdown

The following sequence is recommended when putting the device into a shutdown state and to exit it.

- Disable BioZ, if enabled.
- Disable PLL by setting PLL_EN to 0, if enabled.
- Set SHDN to 1, to enter the shutdown mode.
- ...
- Set SHDN to 0 to enter the normal mode.
- Enable PLL by setting PLL_EN to 1.
- Enable BioZ I and Q as needed.
- ...

Soft-Reset Sequence

The following sequence is required when resetting the device using the RESET bit. Failure to follow this sequence may result in registers becoming unresponsive until a power-on reset is performed.

- Set BIOZ_BG_EN = 1.
- Set SHDN = 0.
- Set REF_CLK_SEL = 0.
- Set PLL_EN = 0.
- Wait for 1ms.
- Set RESET = 1 to reset all registers.
- Enable PLL by setting PLL_EN to 1.
- ...

PLL Synchronization

The MAX30009 provides a PLL synchronization feature for use with multiple MAX30009, MAX86176, MAX30005, or MAX86178 AFEs in a system. This allows the PLLs of the multiple AFEs to remain synchronized and output synchronized samples. PLL synchronization uses either the TRIG pin or the broadcast feature. Both options are discussed as following.

PLL Synchronization Using the TRIG Pin

When the TRIG pin is used for PLL synchronization, one AFE is set up to act as a master and initiates the PLL and timing subsystem synchronization process, while the other(s) act(s) as a slave(s). Alternatively, all the AFEs together act as slaves and the microcontroller acts as the master of this process. In either case, all AFEs should use the same

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external reference clock for the PLLs, and all the PLLs must be enabled and locked before generating a timing system reset pulse. The timing, when using the MAX30009 in a master configuration (MASTER[7](0x11) = 1), is shown in Figure 2. When acting as a master, TIMING_SYS_RESET[7](0x10) is set to 1. TIMING_SYS_RESET is a self-clearing bit and resets to 0 on the second rising edge of FCLK after it is asserted. Once the bit is cleared, the MAX30009 sends out a timing system reset pulse on the TRIG output after an internal time delay. On the first FCLK rising edge after the TRIG pin is pulled high by the timing system reset pulse, the N-divider of the master (if the AFE is the master) restarts its count at 0.

The timing, when using the MAX30009 in a slave configuration (MASTER[7](0x11) = 0), is shown in Figure 3. In this mode, MAX30009 receives a timing system reset pulse on the TRIG pin. After the TRIG input is pulled high, the timing system reset signal is latched by the slave on the first falling edge of FCLK, as shown in Figure 3. On the first FCLK rising edge after the timing system reset pulse is latched on the TRIG input, the N-divider of the slave AFE device restarts its count at 0. As the FCLK input to multiple devices uses the same clock source, the PLLs of all the devices in the system are synchronized automatically.

This is the recommended sequence for synchronizing PLLs on multiple devices using the TRIG pin:

- Disable BioZ by setting BIOZ_BG_EN[2](0x20), BIOZ_Q_EN[1](0x20), and BIOZ_I_EN[0](0x20) to 0, if enabled.
- Reset the part and flush the FIFO by setting SHDN[1](0x11) to 1.
- Then set SHDN = 0 on all the parts.
- Wait for 6ms.
- Program the configuration registers for BioZ as needed:
  - To synchronize multiple devices, the BioZ sample rate should be the same on all devices.
  - The broadcast feature can be used to program the common registers.
- Program FIFO_A_FULL[7:0](0x0D) as desired, and A_FULL_EN[7](0x80) = 1 on the master device.
- Enable PLL by setting PLL_EN[0](0x18) to 1 on all the parts (using the broadcast feature or separately).
- Wait for PLL to lock on all the devices.
- Enable BioZ by setting BIOZ_BG_EN to 1, and BIOZ_Q_EN and BIOZ_I_EN as needed.
- Set TIMING_SYS_RESET to 1 on the master device. All the devices reset their N-dividers, and restart their state machines within the current clock cycle.
- Disable BioZ when data collection is done.
- Disable PLL by setting PLL_EN to 0.

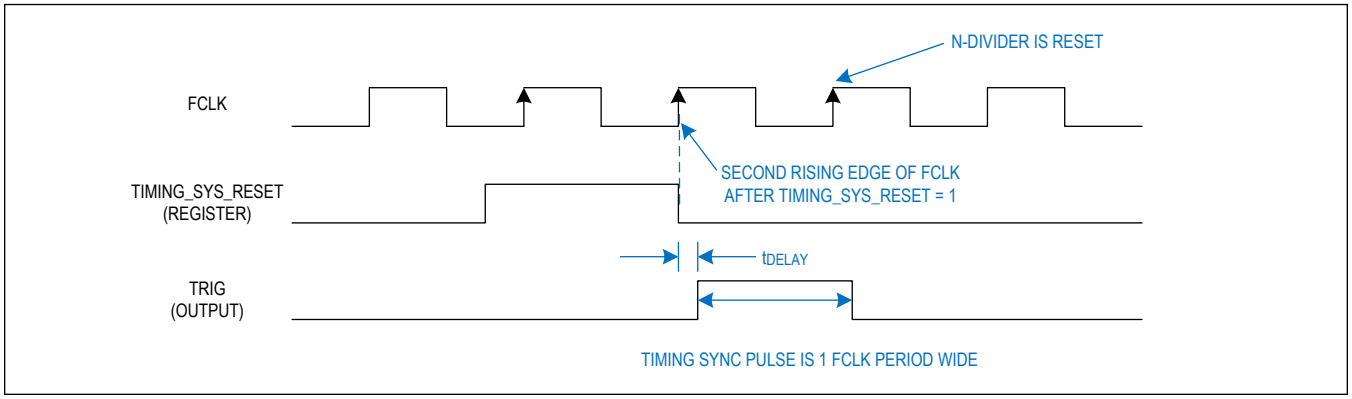

Figure 2. Timing System Synchronization with MAX30009 as a Master

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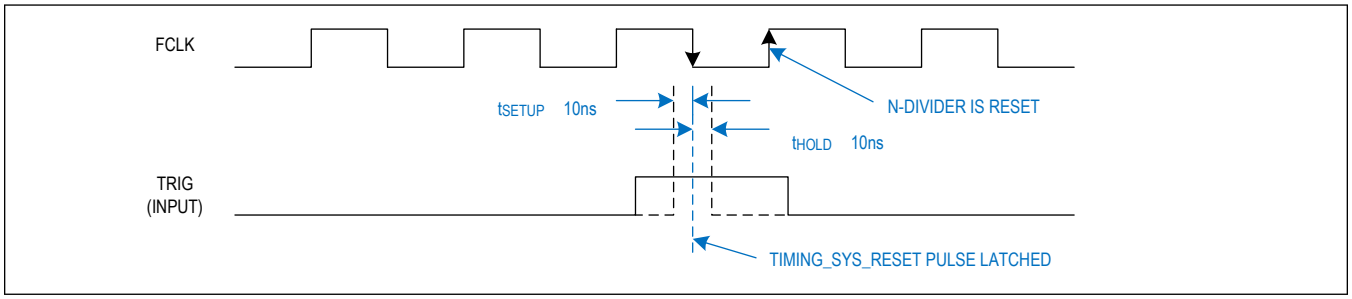

Figure 3. Timing System Synchronization with MAX30009 as a Slave

PLL Synchronization Using the Broadcast Command

PLLs on multiple AFEs can be synchronized using the broadcast feature if the TIMING_SYS_RESET[7](0x10) bit is at the same address in all the devices, and if all the PLLs use the same external reference clock for their PLLs.

Using the I²C Serial Interface:

Set I2C_BCAST_EN to 1, and I2C_BCAST_ADDR to the upper 7 bits of the broadcast address chosen for the system on all the AFEs with PLLs to be synchronized. Using this address as the Slave Address, write 1 to the TIMING_SYS_RESET bit.

Using the Serial Peripheral Interface (**SPI):**

Write 1 to the TIMING_SYS_RESET bits of all the AFEs in a single transaction by asserting their CSB inputs at the same time.

The internal timing reset pulse resets the BioZ N-divider in all the AFEs at the same time on the third rising edge of the FCLK after TIMING_SYS_RESET bit is set to 1; thus, synchronizing all the PLLs.

This is the recommended sequence for synchronizing PLLs on multiple MAX30009 devices using the broadcast feature:

- Disable BioZ by setting BIOZ_BG_EN[2](0x20), BIOZ_Q_EN[1](0x20), and BIOZ_I_EN[0](0x20) to 0, if enabled.
- Reset the part and flush the FIFO by setting SHDN[1](0x11) to 1.
- Then set SHDN = 0 on all the parts.
- Wait for 6ms.
- Program the configuration registers for BioZ as needed:
  - To synchronize multiple devices, the BioZ sample rate should be the same on all the parts.
  - The broadcast feature can be used to program the common registers.
- Program FIFO_A_FULL[7:0](0x0D) as desired, and A_FULL_EN1[7](0x80) = 1 on one of the parts, which becomes the primary part (other parts are secondary parts).
- Enable PLL by setting PLL_EN[0](0x18) to 1 on all the devices (using the broadcast feature or separately).
- Wait for PLL to lock on all devices.
- Enable BioZ by setting BIOZ_BG_EN to 1, and BIOZ_Q_EN and BIOZ_I_EN as needed using the broadcast feature.
- Using the broadcast feature, set TIMING_SYS_RESET to 1 on all the devices.
  - All the devices reset the N-divider, and restart the state machines within the current clock cycle.
- Disable BioZ when data collection is done.

  Note: TIMING_SYS_RESET can be set to 1 before or after enabling BioZ.
- Disable PLL by setting PLL_EN to 0.

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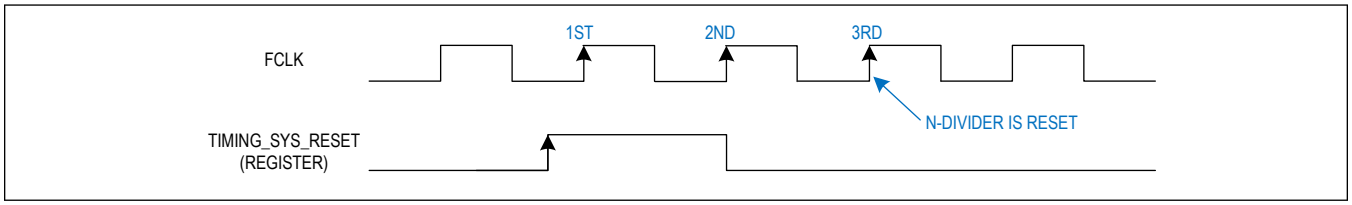

Figure 4. Timing System Synchronization for MAX30009 Using the Broadcast Feature

BioZ Sample Rate and Stimulus Frequency

To make a BioZ measurement, set the following parameters, and then BIOZ_Q_EN[1](0x20) and BIOZ_I_EN[0](0x20) as needed.

The BioZ sample rate and stimulus frequencies depend on the state of the following fields:

- MDIV[9:0](0x17, 0x18)
- NDIV[7](0x17)
- KDIV[4:1](0x17)
- BIOZ_ADC_OSR[5:3](0x20)
- BIOZ_DAC_OSR[7:6](0x20)
- CLK_FREQ_SEL[5](0x1A)
- REF_CLK_SEL[6](0x1A)

The BioZ sample rate is calculated as follows.

- $SR_BIOZ = \frac{PLL_CLK}{NDIV x BIOZ_ADC_OSR}$
- $BIOZ_ADC_CLK = \frac{PLL_CLK}{NDIV}$ (must be between 16.0kHz and 36.375kHz)
- PLL_CLK = *M*xREF_CLK (must be between 14MHz and 28MHz)

REF_CLK is either 32.0kHz or 32.768kHz depending on the state of the CLK_FREQ_SEL and REF_CLK_SEL bits, and M = MDIV +1.

The BioZ stimulus frequency is set by the following equation.

- $F_BIOZ = \frac{PLL_CLK}{KDIV x BIOZ_DAC_OSR}$
- $BIOZ_SYNTH_CLK = \frac{PLL_CLK}{KDIV}$ (must be between 4096Hz and 28MHz)

The ratio of F_BIOZ to SR_BIOZ must be an integer, so that each BioZ sample is integrated over a given number of stimulus cycles. This ratio, C_BIOZ, is calculated by the following equation.

- $C_BIOZ = \frac{F_BIOZ}{SR_BIOZ} = \frac{NDIV x BIOZ_ADC_OSR}{KDIV x BIOZ_DAC_OSR}$

The procedure for setting the BioZ timing parameters is as follows:

First decide the target stimulus frequency (F_BIOZ) for the BioZ measurement.

If F_BIOZ < 54,668Hz:

1. Set BIOZ_DAC_OSR = 256.
2. Set KDIV to get PLL_CLK in range.
3. Calculate MDIV + 1 = ROUND(PLL_CLK / REF_CLK).
4. Set NDIV to get BIOZ_ADC_CLK in range.
5. Set BIOZ_ADC_OSR so that C is an integer.
6. If F_BIOZ = BIOZ_ADC_CLK / 8, set BIOZ_CH_FSEL = 1, otherwise set to 0.
7. If F_BIOZ = BIOZ_ADC_CLK / 2, set BIOZ_INA_CHOP_EN = 0, otherwise set to 1.

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If F_BIOZ > 54,668Hz:

1. Set KDIV = 1.
2. Set BIOZ_DAC_OSR to get PLL_CLK in range.
3. Calculate MDIV + 1 = ROUND(PLL_CLK / REF_CLK).
4. Set NDIV to get BIOZ_ADC_CLK in range.
5. Set BIOZ_ADC_OSR so that C is an integer.
6. Set BIOZ_CH_FSEL = 0.
7. Set BIOZ_INA_CHOP_EN = 1.

Examples are shown in Table 1 and Table 2

Table 1. Example Calculations of BioZ Configuration Parameters for F_BIOZ < 54688Hz

STEP	APPLICATION	EX1	EX2	EX3	EX4	EX5
	EDA/GSR	X	X	X		
	BIA/BIS			X	X	X
	RESP					X
	ICG					
	CLK_REF	32,768	32,768	32,768	32,768	32,768
Target	F_BIOZ	8	100	1,000	10,000	40,000
Step 1	BIOZ_DAC_OSR[2:0]	256	256	256	256	256
Target	BIOZ_SYNTH_CLK	2,048	25,600	256,000	2,560,000	10,240,000
Step 2	KDIV[3:0]	8192	1024	64	8	2
Target	PLL_CLK	16,777,216	26,214,400	16,384,000	20,480,000	20,480,000
Step 3	MDIV[9:0] + 1	512	800	500	625	625
Step 4	NDIV[3:0]	1024	1024	512	1024	1024
Target	BIOZ_ADC_CLK	16,384	25,600	32,000	20,000	20,000
Step 5	BIOZ_ADC_OSR[2:0]	1024	512	128	128	128
	C	0.5	2	4	64	256
Actual	PLL_CLK	16,777,216	26,208,000	16,384,000	20,480,000	20,480,000
Actual	BIOZ_ADC_CLK	16,384	25,600	32,000	20,000	20,000
Actual	BIOZ_SYNTH_CLK	2,048	25,600	256,000	2,560,000	10,240,000
Actual	SR_BIOZ	16	50	250	156.25	156.25
Actual	F_BIOZ	8	100	1,000	10,000	40,000
Actual	Error	0.00%	0.00%	0.00%	0.00%	0.00%

Table 2. Example Calculations of BioZ Configuration Parameters for F_BIOZ > 54688Hz

STEP	APPLICATION	EX1	EX2	EX3	EX4	EX5
	EDA/GSR					
	BIA/BIS	X	X	X	X	X

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Table 2. Example Calculations of BioZ Configuration Parameters for F_BIOZ > 54688Hz (continued)

STEP	APPLICATION	EX1	EX2	EX3	EX4	EX5
	RESP	X	X	X		
	ICG	X	X	X		
	CLK_REF	32,768	32,768	32,768	32,768	32,768
Target	F_BIOZ	54688	100000	150,000	250,000	500,000
Step 1	KDIV[3:0]	1	1	1	1	1
Target	BIOZ_DAC_OSR[2:0]	256	256	128	64	32
Step 2	BIOZ_SYNTH_CLK	14000128	25600000	19200000	16000000	16000000
Target	PLL_CLK	14,000,128	25,600,000	19,200,000	16,000,000	16,000,000
Step 3	MDIV[9:0] + 1	427	781	586	488	488
Step 4	NDIV[3:0]	512	1024	1024	512	512
Target	BIOZ_ADC_CLK	27,344	25,000	18,750	31,250	31,250
Step 5	BIOZ_ADC_OSR[2:0]	128	128	128	256	256
	C	427	512	1024	2048	4096
Actual	PLL_CLK	13,991,936	25,591,808	19,202,048	15,990,784	15.990,784
Actual	BIOZ_ADC_CLK	27,328	24,992	18,752	31,232	31,232
Actual	BIOZ_SYNTH_CLK	13,991,936	25,591,808	19,202,048	15,990,784	15,990,784
Actual	SR_BIOZ	213.5	195.25	146.5	122.0	122
Actual	F_BIOZ	54,656	99,968	150,016	249,856	499,712
Actual	Error	-0.06%	-0.03%	0.01%	-0.06%	-0.06%

Some common stimulus frequencies are shown in Table 3 for REF_CLK frequencies of 32.768kHz. In the BioZ receive channel, the demodulation is done at the same frequency as the stimulus.

Table 3. Common BioZ Stimulus Frequencies and Sample Rates with REF_CLK = 32.768kHz

REF_CLK (Hz)	M (MDIV + 1)	PLL_CLK (Hz)	KDIV	BIOZ_ DAC_OSR	F_BIOZ (Hz)	NDIV	BIOZ_ ADC_OSR	INTEGRATION CYCLES	SR_BIOZ (sps)
32768	790	25886720	1	32	808960	1024	128	4096	197.50
32768	706	23134208	1	32	722944	1024	128	4096	176.50
32768	634	20774912	1	32	649216	1024	128	4096	158.50
32768	568	18612224	1	32	581632	512	128	2048	284.00
32768	488	15990784	1	32	499712	512	128	2048	244.00
32768	458	15007744	1	32	468992	512	128	2048	229.00
32768	822	26935296	1	64	420864	1024	128	2048	205.50
32768	738	24182784	1	64	377856	1024	128	2048	184.50
32768	662	21692416	1	64	338944	1024	128	2048	165.50
32768	594	19464192	1	64	304128	1024	128	2048	148.50
32768	533	17465344	1	64	272896	512	128	1024	266.50
32768	488	15990784	1	64	249856	512	128	1024	244.00

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Table 3. Common BioZ Stimulus Frequencies and Sample Rates with REF_CLK = 32.768kHz (continued)

REF_CLK (Hz)	M (MDIV + 1)	PLL_CLK (Hz)	KDIV	BIOZ_ DAC_OSR	F_BIOZ (Hz)	NDIV	BIOZ_ ADC_OSR	INTEGRATION CYCLES	SR_BIOZ (sps)
32768	479	15695872	1	64	245248	512	128	1024	239.50
32768	430	14090240	1	64	220160	512	128	1024	215.00
32768	781	25591808	1	128	199936	1024	128	1024	195.25
32768	691	22642688	1	128	176896	1024	128	1024	172.75
32768	621	20348928	1	128	158976	1024	128	1024	155.25
32768	559	18317312	1	128	143104	512	128	512	279.50
32768	512	16777216	1	128	131072	512	128	512	256.00
32768	449	14712832	1	128	114944	512	128	512	224.50
32768	781	25591808	1	256	99968	1024	128	512	195.25
32768	727	23822336	1	256	93056	1024	128	512	181.75
32768	648	21233664	1	256	82944	1024	128	512	162.00
32768	641	21004288	1	256	82048	1024	128	512	160.25
32768	586	19202048	1	256	75008	1024	128	512	146.50
32768	523	17137664	1	256	66944	512	128	256	261.50
32768	469	15368192	1	256	60032	512	128	256	234.50
32768	844	27656192	2	256	54016	1024	128	256	211.00
32768	781	25591808	2	256	49984	1024	128	256	195.25
32768	672	22020096	2	256	43008	1024	128	256	168.00
32768	641	21004288	2	256	41024	1024	128	256	160.25
32768	609	19955712	2	256	38976	1024	256	512	76.13
32768	547	17924096	2	256	35008	512	256	256	136.75
32768	484	15859712	2	256	30976	512	256	256	121.00
32768	438	14352384	2	256	28032	512	256	256	109.50
32768	781	25591808	4	256	24992	1024	256	256	97.63
32768	719	23560192	4	256	23008	1024	256	256	89.88
32768	625	20480000	4	256	20000	1024	256	256	78.13
32768	563	18448384	4	256	18016	512	256	128	140.75
32768	500	16384000	4	256	16000	512	256	128	125.00
32768	469	15368192	4	256	15008	512	256	128	117.25
32768	438	14352384	4	256	14016	512	256	128	109.50
32768	813	26640384	8	256	13008	1024	256	128	101.63
32768	750	24576000	8	256	12000	1024	256	128	93.75
32768	688	22544384	8	256	11008	1024	256	128	86.00
32768	625	20480000	8	256	10000	1024	256	128	78.13
32768	563	18448384	8	256	9008	1024	256	128	70.38
32768	500	16384000	8	256	8000	512	256	64	125.00

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Table 3. Common BioZ Stimulus Frequencies and Sample Rates with REF_CLK = 32.768kHz (continued)

REF_CLK (Hz)	M (MDIV + 1)	PLL_CLK (Hz)	KDIV	BIOZ_ DAC_OSR	F_BIOZ (Hz)	NDIV	BIOZ_ ADC_OSR	INTEGRATION CYCLES	SR_BIOZ (sps)
32768	438	14352384	8	256	7008	512	256	64	109.50
32768	750	24576000	16	256	6000	1024	256	64	93.75
32768	625	20480000	16	256	5000	1024	256	64	78.13
32768	500	16384000	16	256	4000	512	256	32	125.00
32768	500	16384000	32	256	2000	512	512	32	62.50
32768	500	16384000	64	256	1000	512	1024	32	31.25
32768	500	16384000	128	256	500	512	1024	16	31.25
32768	500	16384000	256	256	250	512	1024	8	31.25
32768	500	16384000	512	256	125	512	1024	4	31.25
32768	512	16777216	1024	256	64	512	1024	2	32
32768	512	16777216	2048	256	32	512	1024	1	32
32768	512	16777216	4096	256	16	1024	1024	1	16

FIFO Description

The FIFO holds a maximum of 256 samples, and supports BioZ samples of both phases and timing markers. Each sample in the FIFO is three bytes wide, and contains the tag and data. The tag embedded in the FIFO_DATA[23:20] is used to identify the source of each sample data. Table 4 shows the format of the FIFO data along with the associated tags.

Table 4. FIFO Data Format

DATA TYPE	TAG[3:0]				DATA[19:0]																			
BIT	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BioZ In Phase ADC Data	0	0	0	1	BIOZ_ IN_PHASE[19:0]																			
BioZ Quadrature Phase ADC Data	0	0	1	0	BIOZ_QUAD_PHASE[19:0]																			
Marker	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
Invalid Data	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

BioZ Tags:

The BioZ In-Phase and Quad-Phase ADC Measurements have 4-bit tags and 20-bit sample data. Note that if the BioZ channel is disabled while a sample is being pushed to the FIFO, the FIFO contains an extra sample containing the value 0x004000, which should be ignored. This can be avoided by disabling the BioZ channel immediately after a FIFO_DATA_RDY or A_FULL interrupt.

Other Tags:

Markers are 24 bits long and can be used to insert a timing marker into the FIFO data stream. A marker is inserted by setting FIFO_MARK[5](0x0E), which is a self-clearing bit. An attempt to read an empty FIFO sample returns the INVALID_DATA tag.

BioZ

The BioZ system in [[BioZ System Block Diagram]] primarily consists of a transmit (TX) channel, a receive (RX) channel, and an input/output MUX. The BioZ system supports calibration using internal or external calibration resistors, enabling

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0.1% accuracy in the I and Q channels. The flexible I/O MUX, lead-on and lead-off detection, adjustable amplifier bias, and lead bias allow for flexible hardware designs capable of multiple measurement types with low power consumption. The stimulus frequency and sample rate are determined by the timing subsystem (see the *Timing Subsystem* section).

The BioZ channel can measure impedances across multiple application areas with a wide range of frequencies and magnitudes, as shown in Figure 6. Each type of stimulus can operate over frequencies between 16Hz and 806kHz.

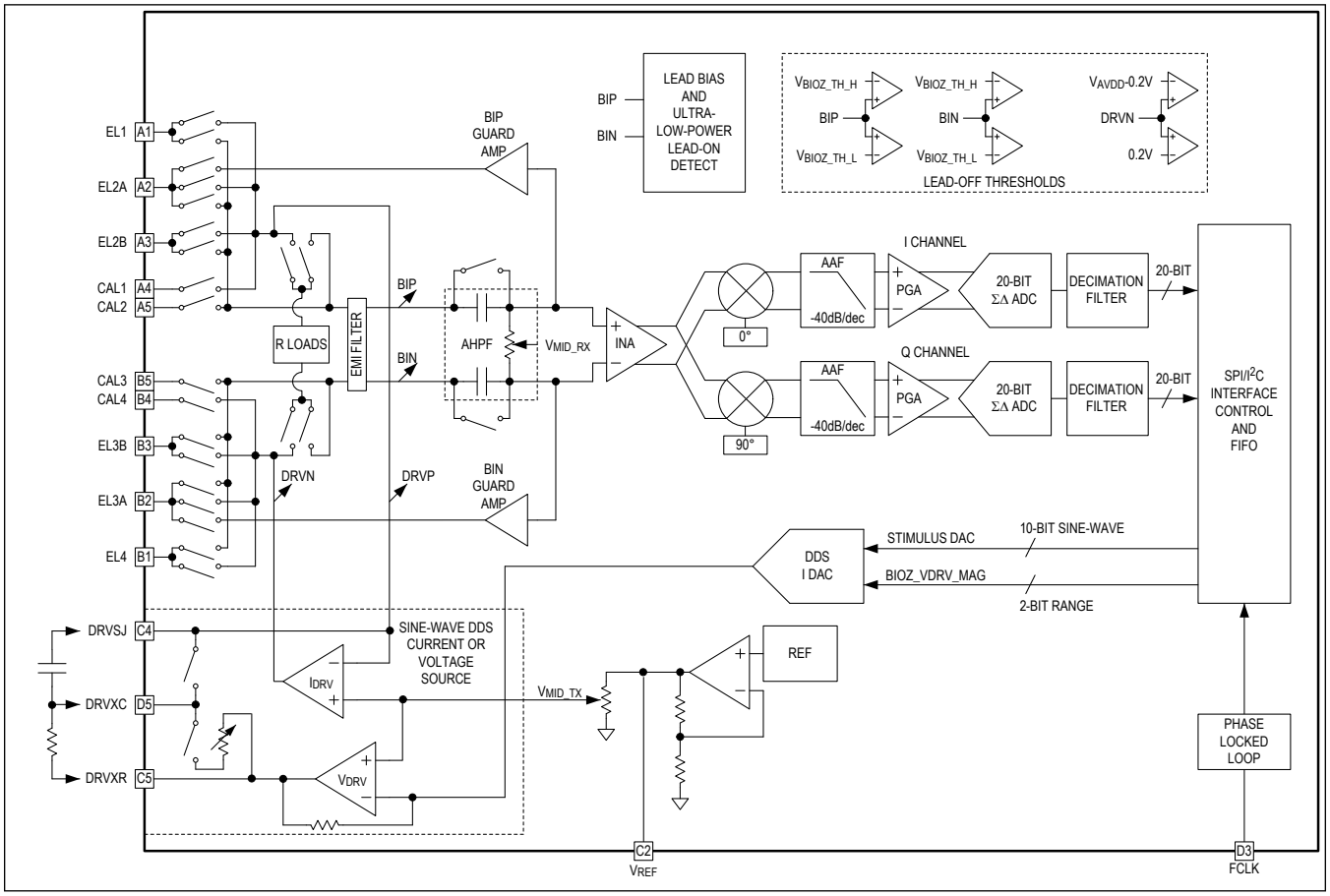

Figure 5. BioZ System Block Diagram

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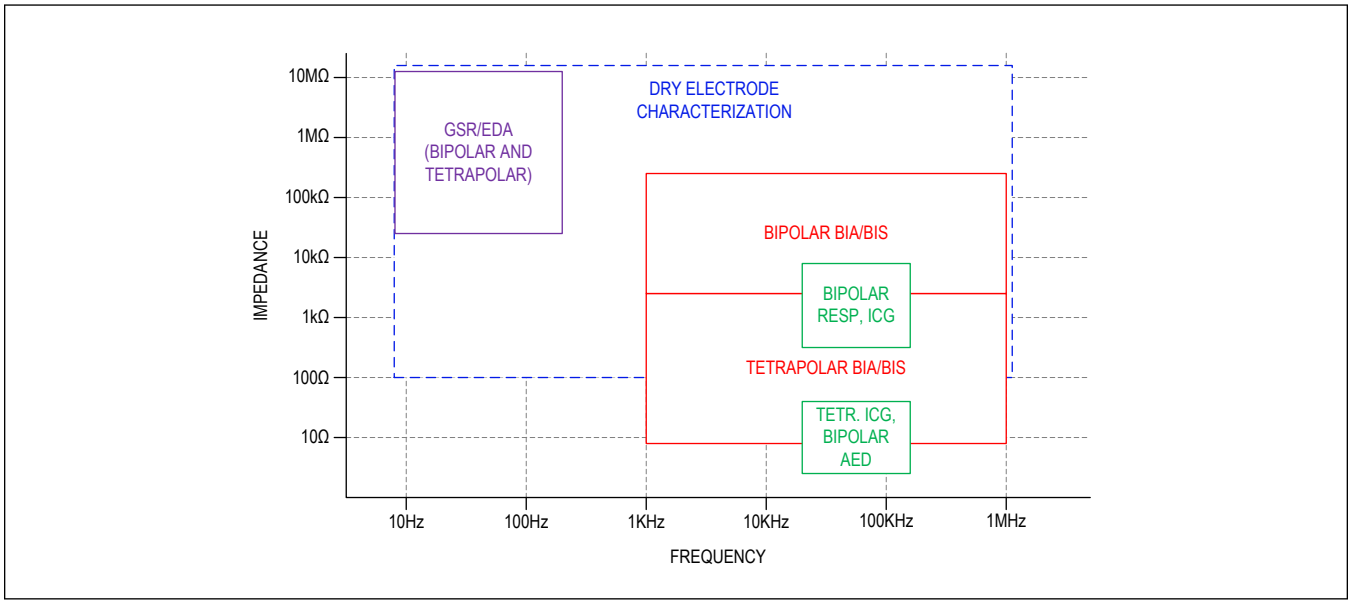

Figure 6. BioZ Typical Application Areas

BioZ Start-up and Shutdown

To power on the BioZ subsystem, set BIOZ_BG_EN[2](0x20) to 1, which enables the bandgap reference, V_{REF}. After a start-up time of approximately 200ms, BioZ measurements can be initiated by selecting in-phase (I) in BIOZ_I_EN[0](0x20) and quadrature (Q) in BIOZ_Q_EN[1](0x20). BioZ data begins within 2ms of enabling the measurement.

When the measurement is finished, the BioZ subsystem can be shut down by writing BIOZ_BG_EN, BIOZ_I_EN, and BIOZ_Q_EN to 0. Alternatively, if another measurement is set to follow shortly after, setting BIOZ_DRV_MODE[1:0](0x22) to 0x3 can place the BioZ TX channel into standby mode, while BIOZ_BG_EN, BIOZ_I_EN, and BIOZ_Q_EN remain set to their active values. Standby mode disables the stimulus but maintains the DC bias of the drive electrodes, preventing any settling time associated with charging the electrode and body capacitance during the next measurement. In standby mode, the receive channel stops sampling and enters low-power mode unless BIOZ_STBYON[4](0x28) is set. Setting BIOZ_STBYON = 1 can further reduce settling time during the next measurement by maintaining the receive channel in an active state.

BioZ Transmit Channel

The MAX30009 can generate three types of stimuli: a sine-wave current, a sine-wave voltage, and an H-bridge voltage square wave. Each of these modes are described in the following sections. The stimulus generator can be put into a low-power standby mode by setting BIOZ_DRV_MODE[1:0](0x22) to 0x3. In this mode, the DDS circuit remains active, but the BIOZ_DRV_RESET switch is closed, driving DRVN to V_{MID_TX}. The amplifiers are put into a low-power state to reduce power consumption, and the H-bridge driver is disabled.

Sine-Wave Current Stimulus

To select the sine-wave current mode, set BIOZ_DRV_MODE[1:0](0x22) to 0x0. When generating a sine-wave current stimulus, the AC current is injected into the body using electrodes assigned to the DRVP and DRVN (drive) functions with the bioimpedance sensed differentially through the electrodes assigned to the BIP and BIN (bioimpedance receive) functions. Two-electrode and four-electrode configurations are supported for typical wet or dry electrode impedances. Figure 7 shows the stimulus signal path with a four-electrode configuration. A sine-wave current stimulus is generated by a Direct Digital Synthesis (DDS) circuit with the help of a 10-bit current DAC (I DAC). The V_{DRV} amplifier converts this sine-wave current into a sine-wave voltage. One of four range resistors should be selected using

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BIOZ_IDRV_RGE[3:2](0x22). The current range can alternatively be set with an external resistor by enabling BIOZ_EXT_RES[7](0x22). The sine-wave voltage appears on one side of this resistor and the other side is held at V_{MID_TX} by the operation of the I_{DRV} amplifier, thus creating the sine-wave current stimulus in the I_{DRV} amplifier feedback loop. This current flows through the range resistor, electrodes, and body impedance, then back into the I_{DRV} amplifier output terminal.

A blocking capacitor (C_{EXT}) connected between the DRVXC and DRVSJ pins is required to avoid the DC current from being driven through the body. A 47nF capacitor is recommended for all applications.

Both amplifiers in the signal chain have adjustable range and bandwidth to optimize power consumption for the required performance. BIOZ_AMP_RGE[3:2](0x25) sets the amplifier range, and BIOZ_AMP_BW[1:0](0x25) sets the gain-bandwidth product. When using the MAX30009 for Impedance Cardiography (ICG) and Bioimpedance Analysis (BIA), set the BIOZ_AMP_RGE and BIOZ_AMP_BW to higher values. It is generally acceptable to leave these settings at the lowest value for other applications.

When selecting a stimulus current magnitude, there are several restrictions to follow. The stimulus current is set by a combination of BIOZ_IDRV_RGE[3:2](0x22) and BIOZ_VDRV_MAG[5:4](0x22), and Table 5 shows the stimulus current options available for MAX30009.

1. To ensure patient safety, some current amplitude and frequency combinations are not allowed (see Table 5). If an off-limits setting is selected, the BIOZ_VDRV_MAG and BIOZ_IDRV_RGE fields are automatically overwritten to the highest allowed value based on the frequency settings. It is the responsibility of the end application device manufacturer to ensure the MAX30009 is programmed properly and in conformance with *IEC60601-1 Medical electrical equipment – Part 1: General requirements for basic safety and essential performance* with regards to patient auxiliary current limitations.
2. When using stimulus currents greater than $640\mu A_{RMS}$, EL1 and EL4 must be used for DRVP and DRVN, respectively. Electrode pins EL2A, EL2B, EL3A, and EL3B are not designed to support currents above $640\mu A_{RMS}$. Assigning the wrong pins does not damage the MAX30009, but switch resistance is higher and degrades measurement accuracy.
3. The current amplitude should be chosen to not exceed $1000mV_{P-P}$ at the BIP and BIN pins based on the network impedance at the current injection frequency.

Table 5. Stimulus Current Options

STEP	BIOZ_IDRV_RGE	RANGE RESISTOR	BIOZ_VDRV_MAG	RMS CURRENT	FREQUENCY RANGE (Hz)	RECOMMENDED BIOZ_AMP_RGE
1	1 (0x0)	552.5kΩ	low (0x0)	16nA	All frequencies	Low
2	1 (0x0)	552.5kΩ	low mid (0x1)	32nA	All frequencies	Low
3	1 (0x0)	552.5kΩ	high mid (0x2)	80nA	All frequencies	Low
4	1 (0x0)	552.5kΩ	high (0x3)	160nA	All frequencies	Medium-Low
5	2 (0x1)	110.5kΩ	low (0x0)	320nA	All frequencies	Medium-Low
6	2 (0x1)	110.5kΩ	low mid (0x1)	640nA	All frequencies	Medium-Low
7	2 (0x1)	110.5kΩ	high mid (0x2)	1.6µA	All frequencies	Medium-Low
8	2 (0x1)	110.5kΩ	high (0x3)	3.2µA	All frequencies	Medium-Low
9	3 (0x2)	5.525kΩ	low (0x0)	6.4µA	All frequencies	Medium-Low
10	3 (0x2)	5.525kΩ	low mid (0x1)	12.8µA	All frequencies	Medium-High
11	3 (0x2)	5.525kΩ	high mid (0x2)	32µA	All frequencies	Medium-High
12	3 (0x2)	5.525kΩ	high (0x3)	64µA	All frequencies	Medium-High
13	4 (0x3)	276.25Ω	low (0x0)	128µA	≥ 512	High
14	4 (0x3)	276.25Ω	low mid (0x1)	256µA	≥ 2048	High
15	4 (0x3)	276.25Ω	high mid (0x2)	640µA	≥ 8192	High
16	4 (0x3)	276.25Ω	high (0x3)	1.28mA	≥ 16384	High

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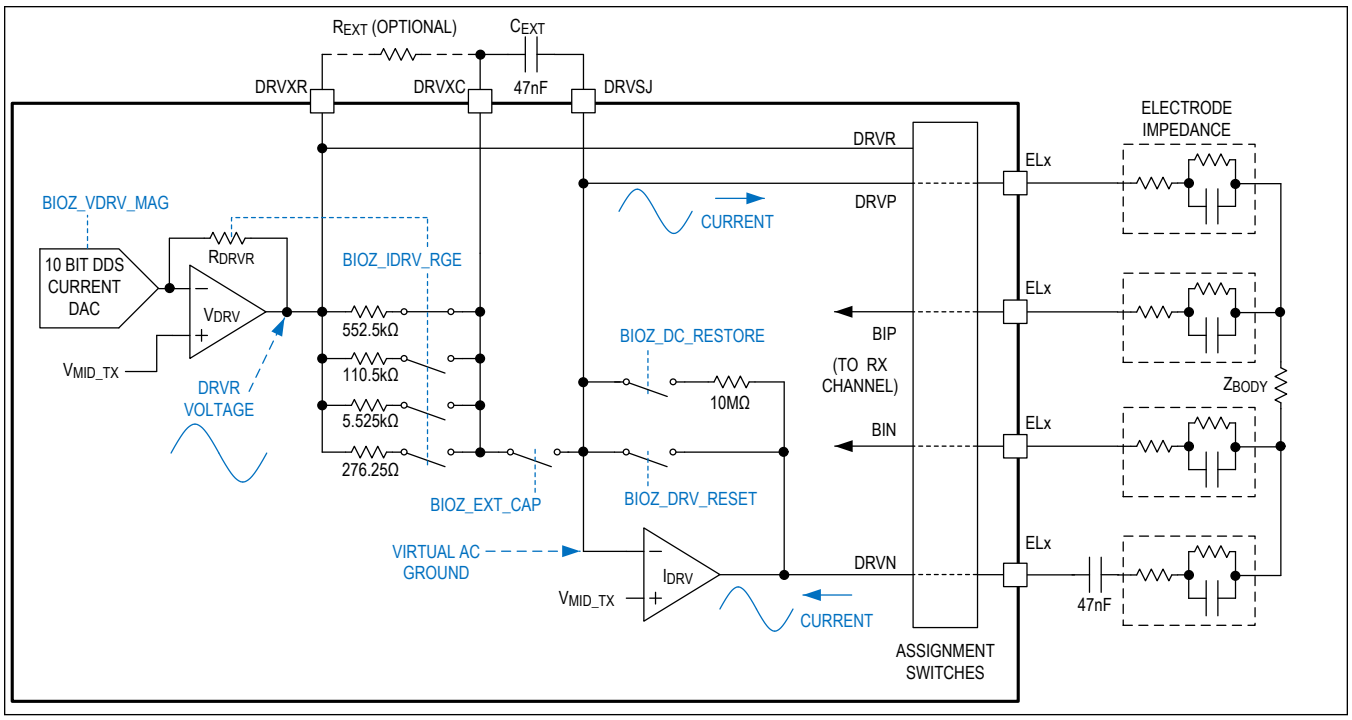

Figure 7. Bioimpedance Stimulus Generator — Sine-Wave Current Mode

Sine-Wave Voltage Stimulus

To select the sine-wave voltage mode, set BIOZ_DRV_MODE[1:0](0x22) to 0x1. Figure 8 shows the stimulus signal path for a four-electrode configuration. The voltage output from the V_{DRV} amplifier, available on the DRVXR node, is applied directly to the EL1 electrode with a switch within the MAX30009 I/O MUX. In this mode of operation, a switch is closed around the I_{DRV} amplifier so that the amplifier becomes a voltage follower and drives the EL4 node to V_{MID_TX}. In this mode, external resistors on the EL1 and EL4 nodes are used to limit the patient current to V_{RMS} / (2 x R_{SERIES}), where V_{RMS} is the voltage output amplitude out of the V_{DRV} amplifier set by BIOZ_VDRV_MAG[5:4](0x22). When using this voltage stimulus mode, EL1 must be selected for DRVP, and EL4 must be selected for DRVN. Electrode pins EL2A, EL2B, EL3A, and EL3B are not available for voltage mode stimulation.

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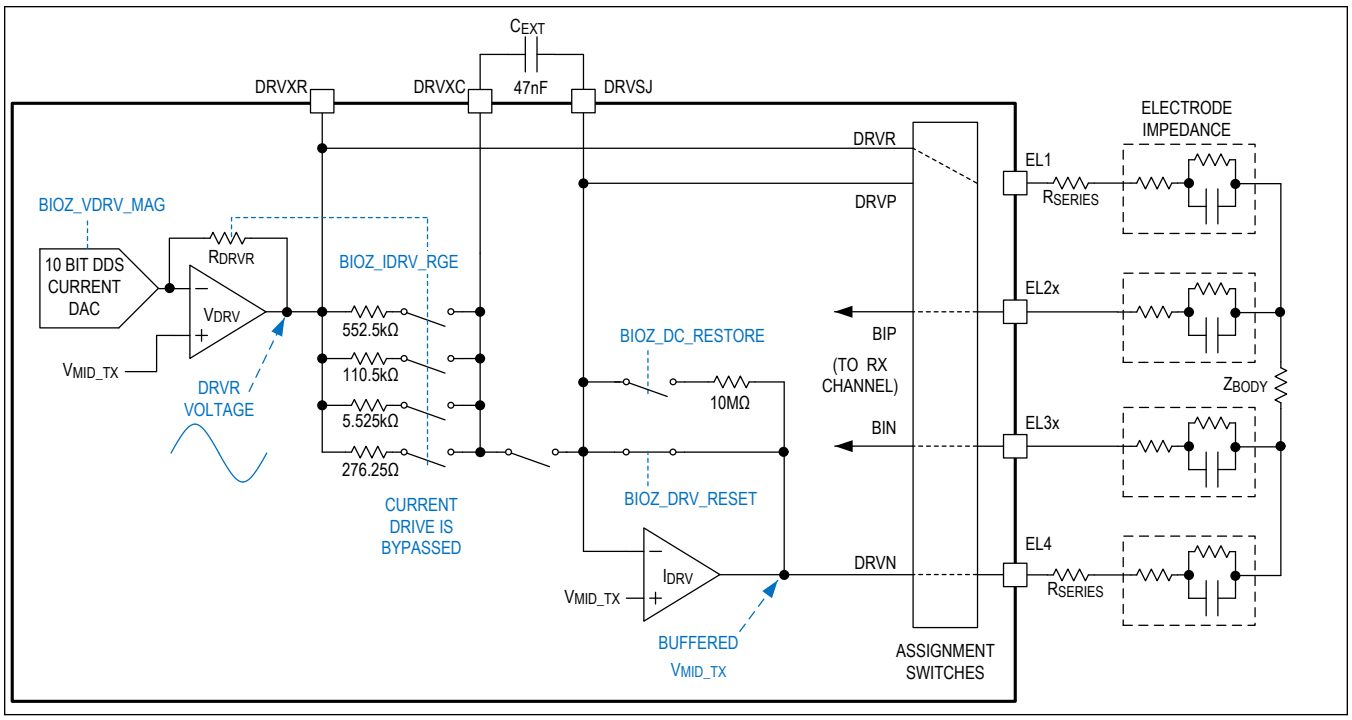

Figure 8. Bioimpedance Stimulus Generator — Sine-Wave Voltage Mode

Square-Wave Voltage (H-Bridge) Stimulus

To select the H-bridge square-wave voltage stimulus mode, set BIOZ_DRV_MODE[1:0](0x22) to 0x2. Figure 9 shows the signal path for H-bridge mode. An H-bridge is used to alternately switch AVDD and then AGND onto EL1, and AGND and then AVDD onto EL4. In this case, the DDS circuit and I_{DRV} amplifier are disabled, and the range resistor switches are all opened. When using this mode of operation, there must be series precision resistors in both the EL1 and EL4 paths to limit the current to V_{AVDD} / (2 x R_{SERIES}). The current from the H-bridge flows through R_{SERIES_EL1}, a first electrode impedance, body impedance with its variable component, a second electrode impedance, and R_{SERIES_EL4}. The applied patient current is set by selecting the appropriate R_{SERIES} resistance value. The two R_{SERIES} resistors and the body form an impedance divider, and the portion of the AC voltage signal across the body impedance is sensed by the bioimpedance AFE receive channel with the inputs selected from EL2A, EL2B, EL3A, and EL4B. DRVP must be assigned to EL1 and DRVN must be assigned to EL4.

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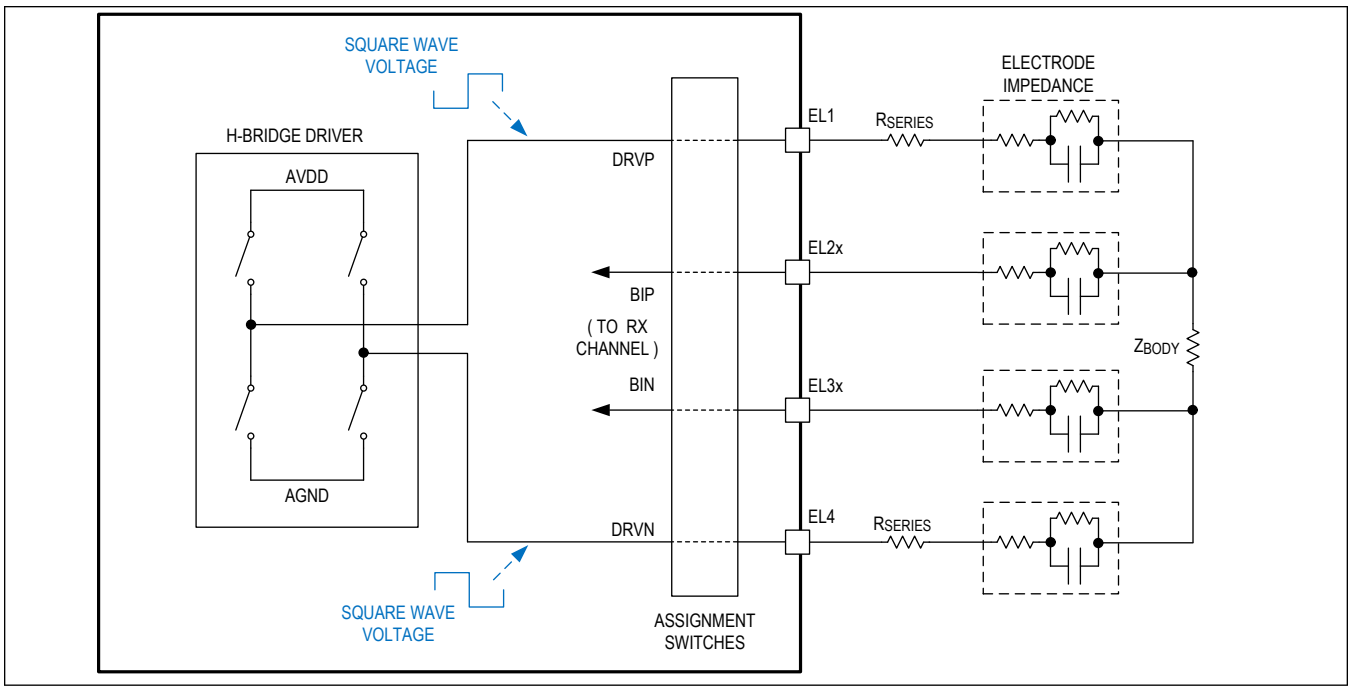

Figure 9. Bioimpedance Stimulus Generator — H-Bridge Square-Wave Voltage Mode

BioZ Receive Channel

Figure 10 illustrates the BioZ receive channel block diagram. The channel comprises an input MUX, a bypassable and programmable analog high-pass filter, an instrumentation amplifier with programmable gain, two demodulators, two anti-alias filters, two programmable gain amplifiers, and two Analog-to-Digital Converters (ADCs). The input MUX includes several features such as Electrostatic Discharge (ESD) protection, Electromagnetic Interference (EMI) filtering, programmable electrode assignment switches, lead biasing, DC lead-off detection, and ultra-low power lead-on detection.

The MAX30009 BioZ receive channel Instrumentation Amplifier (INA) provides low-noise amplification of the differential signal, rejects differential DC voltage due to the analog high-pass filter, rejects common-mode interference such as AC mains interference, and provides high input impedance to guarantee high Common-Mode Rejection Ratio (CMRR) even in the presence of severe electrode impedance mismatch. The total channel gain can be set to 1V/V, 2V/V, 5V/V, or 10V/V, and is set by BIOZ_GAIN[1:0](0x24), which affects both the INA gain and PGA gain. The demodulators multiply the received signal by square waves with the same frequency (F_BIOZ) to down-convert the measurement frequency to DC. The phase of the demodulator f_{DEMOD} signal is 0° for the I channel and 90° for the Q channel. Following the PGA amplifiers are two-pole, active low-pass Anti-Aliasing Filters (AAFs) with a 600Hz -3dB frequency that provide approximately 57dB of attenuation at half the sigma-delta ADC input sampling rate (BIOZ_ADC_CLK). After the AAFs are 20-bit sigma-delta ADCs. The effective bits of the ADC depend on the value of BIOZ_ADC_OSR[5:3](0x20) with higher oversampling ratios resulting in more effective bits (see the Electrical Characteristics section).

When AC-coupling the BioZ receive channel or using the internal analog High-Pass Filter (HPF), the AC differential range is > $1000mV_{P-P}$ with an INA gain of 1V/V. When DC-coupling the bioimpedance receive channel, the usable common-mode range of the bioimpedance receive channel is 0.5V to V_{AVDD} - 0.75V. Internal lead biasing is used to achieve these requirements (see the *BioZ Lead Bias* section).

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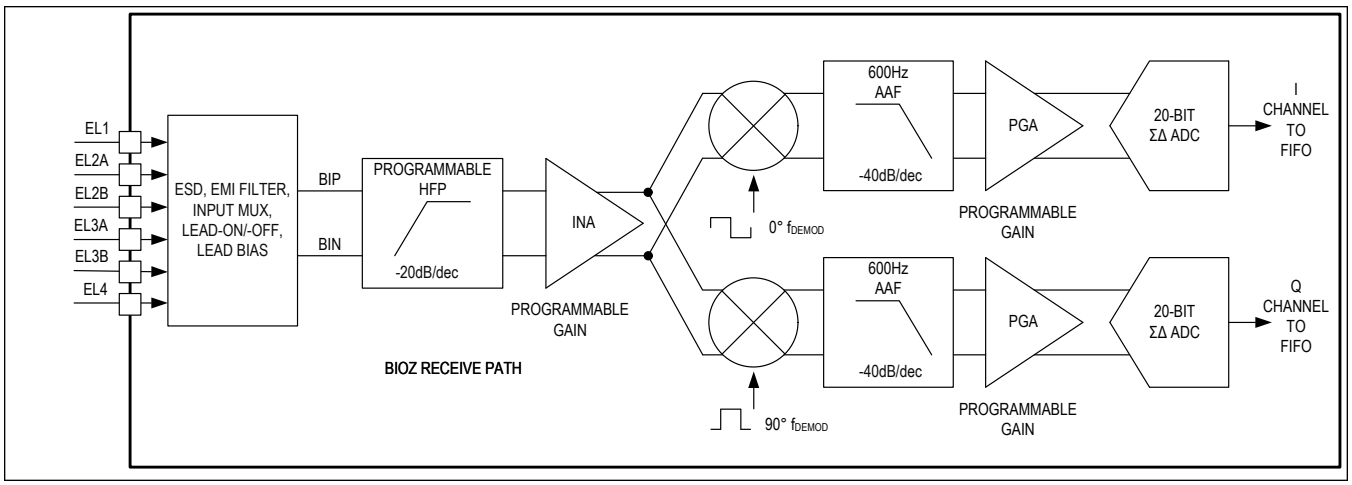

Figure 10. BioZ Receive Channel

BioZ Decimation and Digital Filters

The decimation filter is used along with the sigma-delta modulator within the ADC to reduce the sample rate of the BIOZ_ADC_CLK to a smaller programmable output rate (SR_BIOZ). The decimation filter has a SINC3 response with a corner frequency at approximately 0.26 x SR_BIOZ. The decimation filter is followed by a programmable digital filter to implement High-Pass Filter (HPF) and Low-Pass Filter (LPF) selections.

The programmable digital high-pass filter scales with the ADC clock rate and can be set to either 0.00025 x SR_BIOZ, 0.002 x SR_BIOZ, or bypassed by setting BIOZ_DHPF[7:6](0x21). Similarly, the programmable digital low-pass filter scales with the ADC clock rate and can be set to 0.005 x SR_BIOZ, 0.02 x SR_BIOZ, 0.08 x SR_BIOZ, 0.25 x SR_BIOZ, or bypassed using BIOZ_LPF[5:3](0x21).

Converting Digitized BioZ Samples to Voltage and Impedance

BioZ channel samples are recorded in 20-bit left-justified 2's complement format. These samples represent the voltage at the ADC, which has passed through the INA, demodulator, PGA, and AAF. The INA and PGA apply a combined gain of 1V/V, 2V/V, 5V/V, or 10V/V as set by BIOZ_GAIN[1:0](0x24). The demodulator multiplies the incoming sine-wave or square-wave by a square-wave with the same frequency as F_BIOZ. The AAF is a two-pole low-pass filter with a 600Hz corner frequency. The decimation filter in the ADC has a bandwidth of approximately 0.26 x SR_BIOZ.

When performing absolute impedance measurements for applications such as BIA/BIS and GSR/EDA, the DC component of the demodulated voltage represents the measured impedance. When F_BIOZ >> 600Hz or when SR_BIOZ << F_BIOZ, the harmonics resulting from the square-wave demodulation can be ignored, and the digitized samples represent the DC component of the demodulated voltage. For sine-wave stimulation, the square-wave demodulation applies a scaling factor of 2 / π to the DC component, as shown in Figure 11.

The DC component of the demodulated voltage is converted by the ADC, and represents load impedance in current-stimulus mode according to the following equation.

Sine-Wave Stimulus: $Z_{BIOZ}(\Omega) = ADC_COUNT \times V_{REF_ECG} / (2^{19} \times BIOZ_GAIN \times 2 / \pi \times I_{MAG})$

where,

ADC_COUNT = ADC counts in signed magnitude format

V_{REF_ECG} = 1V (typ, see the Electrical Characteristics section)

BIOZ_GAIN = Options1V/V, 2V/V, 5V/V, and 10V/V.

I_{MAG} = Stimulus current in A_{PK} set by BIOZ_VDRV_MAG[5:4](0x22) and BIOZ_IDRV_RGE[3:2](0x22).

The input-referred voltage amplitude can likewise be calculated with the following equations.

Sine-Wave Stimulus: $V_{BIOZ}(V_{PK}) = ADC_COUNT \times V_{REF_ECG} / (2^{19} \times BIOZ_GAIN \times 2 / \pi)$

Square-Wave Stimulus: $V_{BIOZ}(V_{PK}) = ADC_COUNT \times V_{REF_ECG} / (2^{19} \times BIOZ_GAIN)$

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For voltage stimulus modes, the impedance can be calculated from an impedance divider with the series resistors.

For respiration and ICG applications, the signal of interest is contained in the time-varying impedance signal. So, the DC component is not as important. The respiration signal band is typically 0.05Hz to 4Hz, and the ICG signal band is typically DC to 64Hz. For these applications, the BioZ sample rate and digital filters can be adjusted to select the signal band of interest, considering the decimation filter 0x26 x SR_BIOZ bandwidth. The above impedance or voltage calculations can be performed for these applications, but these conversions are not strictly necessary.

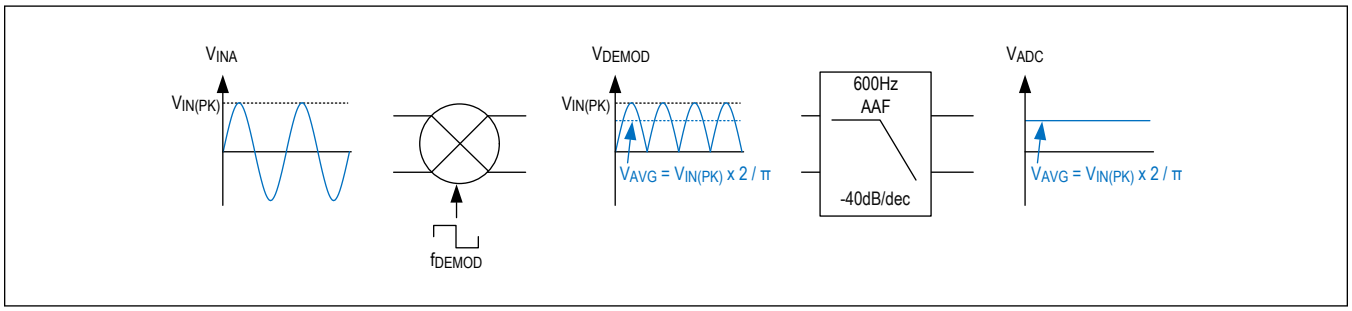

Figure 11. Square-Wave Demodulation for a Sine-Wave Stimulus (INA and PGA Gain Not Shown)

BioZ Noise Measurements

Table 6 shows the input referred voltage noise of the BioZ receive channel measured with the inputs shorted and the frequency settings shown in Table 7 and BIOZ_AHPF[7:4](0x24) = 5kHz.

Table 6. BioZ Receive Channel Input-Referred Noise, 256sps

BIOZ_GAIN (V/V)	BIOZ_DLPF (Hz)	NOISE (μV_{RMS})	NOISE (μV_{P-P})	SNR (dB)	ENOB
1	bypass	16.89	75.28	86.4	14.1
	1.28	0.71	2.43	114.0	18.6
	5.12	1.40	9.71	108.0	17.7
	20.48	5.32	30.36	96.5	15.7
	64	15.53	65.57	87.1	14.2
2	bypass	8.40	40.68	92.5	15.1
	1.28	0.39	1.82	119.2	19.5
	5.12	0.74	4.86	113.6	18.6
	20.48	2.64	15.79	102.5	16.7
	64	7.72	33.39	93.2	15.2
5	bypass	3.32	15.06	92.6	15.1
	1.28	0.14	0.73	119.8	19.6
	5.12	0.33	2.19	112.6	18.4
	20.48	1.02	5.83	102.8	16.8
	64	3.09	13.36	93.2	15.2

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Table 6. BioZ Receive Channel Input-Referred Noise, 256sps (continued)

BIOZ_GAIN (V/V)	BIOZ_DLPF (Hz)	NOISE (μV_{RMS})	NOISE (μV_{P-P})	SNR (dB)	ENOB
10	bypass	1.70	8.01	92.4	15.1
	1.28	0.09	0.49	118.2	19.3
	5.12	0.19	1.21	111.6	18.2
	20.48	0.53	3.28	102.5	16.7
	64	1.57	7.77	93.1	15.2

Note: SNR = $20\log\left(\frac{V_{IN(RMS)}}{V_{N(RMS)}}\right)$, ENOB =(SNR -1.76)/6.02

Note: $V_{IN(P-P)}$ = ($2V_{P-P}$ / BIOZ_GAIN) or $1V_{P-P}$, whichever is smaller. This represents the maximum signal of the receive channel: $V_{IN(RMS)} = \frac{V_{IN(P-P)}}{2\sqrt{2}}$

Table 7. Input-Referred Noise Frequency Settings

REF_CLK (Hz)	M	PLL_CLK (Hz)	BIOZ_KDIV	BIOZ_DAC_OSR	F_BIOZ (Hz)	BIOZ_NDIV	ADC_OSR	INTEGRATION CYCLES	ADC_SR (sps)	BIOZ_AHPF (kHz)
32768	512	16,777,216	2	128	65536	512	128	256	256	5

BioZ Input/Output MUX

The BioZ input/output MUX shown in Figure 12 has many helpful circuits to support BioZ applications. For the electrodes assigned to the receive channel, this circuitry contains integrated ESD and EMI protection, DC lead-off detect current sources, lead-biasing, programmable resistor loads, as well as a programmable HPF. The electrodes assigned to provide the stimulus have ESD protection and compliance monitors. The input/output MUX assigns physical electrodes to the available BioZ channel functions. For example, EL1 can be assigned to DRVP (positive drive), EL2B to BIP (positive input), EL3B to BIN (negative input), and EL4 to DRVN (negative drive). The EL2 and EL3 electrode inputs have A and B pins, allowing one board to support both GSR/EDA and BIA/BIS in the same application. In this case, the A inputs should be used for GSR/EDA and need external AC coupling capacitors, and the B inputs should be used for BIA/BIS and do not need external capacitors. The MUX also has four-wire calibration port (CAL1 to CAL4) for in-situ calibration to one or more precision external resistors with more details shown in Figure 17.

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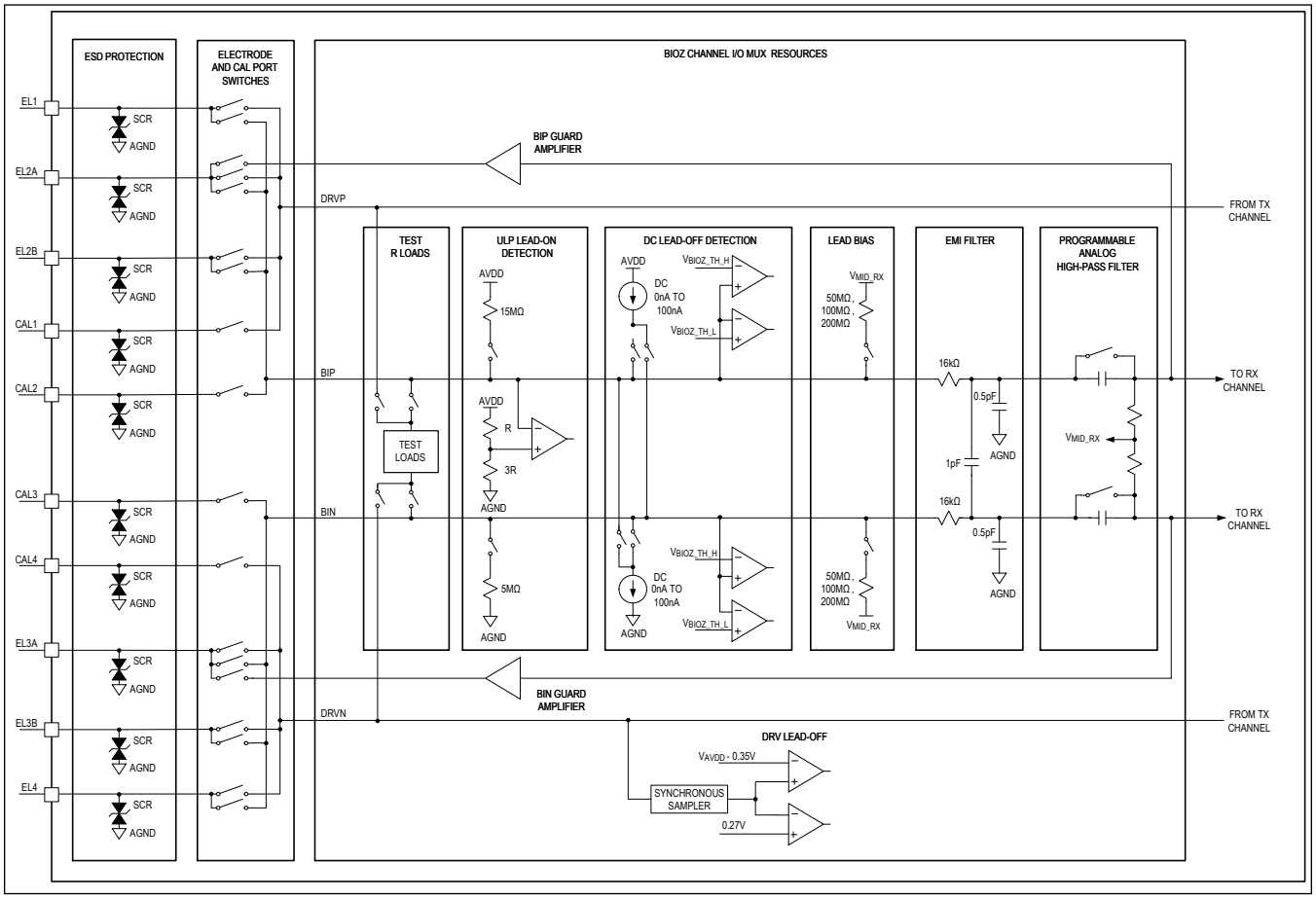

Figure 12. BioZ Input/Output MUX

BioZ EMI Filtering and ESD Protection

The EMI filter on the BIP and BIN internal inputs consists of 16kΩ resistors connected to BIP and BIN, followed by a 1pF differential-mode capacitor and 0.5pF common-mode capacitors. These form a single-pole, low-pass, differential- and common-mode filter with the differential mode pole located at approximately 4MHz and the common-mode pole located at approximately 20MHz. Additional external EMI filters are not recommended for applications with dry electrodes to maintain high input impedance, which helps mitigate the impact of electrode impedance mismatch. With lower input impedance, the electrode impedance mismatch translates into increased conversion of common-mode voltage to differential-mode voltage. Applications with wet electrodes can use external EMI filters with high-precision components to minimize electrode impedance mismatch. In this case, the differential-mode pole can be set as low as the desired signal bandwidth, and the common-mode pole is set at least a decade below the AM radio band (535kHz).

Pins EL1, EL2A,EL2B, CAL1, CAL2, CAL3, CAL4, EL3B, EL3A, and EL4 meet the following ESD standards:

- ±8kV using the Contact Discharge method specified in IEC61000-4-2 ESD.
- ±6kV using the Air-Gap Discharge method specified in IEC61000-4-2 ESD.

BioZ Lead Bias

The MAX30009 limits the BIP and BIN DC input range to 0.5V to V_{AVDD} - 0.75V. This range can be maintained either through external or internal lead biasing.

Internal DC lead biasing consists of 50MΩ, 100MΩ, or 200MΩ selectable resistors from BIP and BIN to V_{MID_RX} that

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bias the MAX30009 to the proper potential relative to the body in battery-powered systems. By matching the voltage of V_{MID_RX} to the body, lead bias ensures the common-mode input voltage of BIP and BIN are within the DC input range of the BioZ receive channel. Lead bias is only effective when the MAX30009 system has high galvanic isolation from earth ground. See BIOZ_RBIAS_VALUE[3:2](0x58) to select a resistance value, and EN_RBIAS_BIP[1](0x58) and EN_RBIAS_BIN[0](0x58) to enable lead bias.

Programmable BioZ Resistor Load

The programmable resistive load allows a built-in self-test of the current generator and BioZ receive channel. See Figure 13 for implementation details. For BIA/BIS applications, there is a selection of low-impedance loads to choose from: 280Ω, 600Ω, 900Ω, and 5.1kΩ. For GSR/EDA applications, there is a selection of high-impedance loads to choose from: 25.7kΩ, 101kΩ, 505kΩ, and 1MΩ.

See register fields BMUX_RSEL[7:6](0x41), BMUX_BIST_EN[5](0x41), BMUX_GSR_RSEL[7:6](0x42), and GSR_LOAD_EN[5](0x42) to set the resistor value.

The BIA/BIA resistive loads can also be used as internal calibration resistors. See BIST_R_ERROR[7:0](0x44) for details.

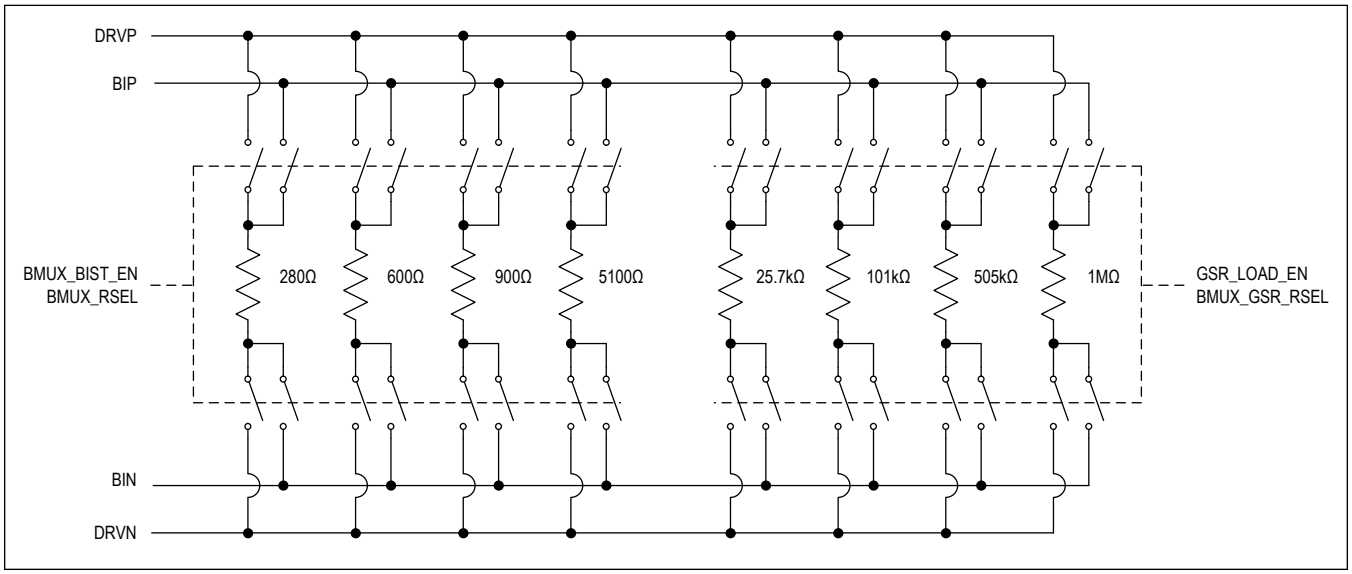

Figure 13. Programmable Resistor Load

BioZ Lead-Off Detection

The MAX30009 has three techniques to determine if there is one or more electrode lead-off condition(s). Lead-off is a term to indicate that one or more electrodes used during the bioimpedance measurements has/have become open. In other words, the electrode-tissue interface impedance is too high and the bioimpedance measurement might become unreliable. These three lead-off techniques are DC lead-off, DRV lead-off, and programmable thresholds (AC lead-off) circuit. The relevant techniques depend on the electrode configuration (bipolar or tetrapolar) and which electrode is off. The first two techniques use circuits contained within the I/O MUX circuitry and the final technique is accomplished using digital circuitry after the receive channel ADC.

There is also an Ultra-Low-Power (ULP) lead-on detect circuit only to wake up the microcontroller controlling the MAX30009. This circuit should never be used while making bioimpedance measurements and should not be confused with the lead-off circuit functionality.

The DC lead-off detection circuit provides matched source and sink currents injected into the BIP and BIN electrodes. This current, when the electrodes are connected properly, flows through a first electrode-tissue interface, through the body, and then through a second electrode-tissue interface. This current flow develops a differential voltage across the two input pins. If one or both electrode-tissue interfaces have a poor connection with the body, then this current path has

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much higher impedance and this voltage is large. If the electrodes are properly connected, then this voltage is small. The DC lead-off circuitry provides two sets of dual comparators to test if the differential voltage is too high.

This feature is enabled by EN_LOFF_DET[6](0x50), and the stimulus current magnitude (5nA to 100nA) is set by LOFF_IMAG[2:0](0x50). The current magnitude should be chosen to match the expected acceptable maximum impedance of the specific electrodes used in the application.

When using DC lead-off detection, the microcontroller and user can be alerted if the viability of the electrode tissue interface electrodes is compromised by dual comparators, indicating if BIP or BIN voltages exceed either a programmable high-limit or low-limit. The dual comparators can be used to generate a hardware interrupt if the DC lead-off voltage exceeds the threshold (i.e., a minimum continuous violation) for an interval exceeding either 115ms or 140ms, depending on the setting of FCLK before asserting one of the DC_LOFF interrupt flags. The comparator threshold is controlled by BIOZ_LOFF_THRESH[3:0](0x51). See Figure 14 for an example of the threshold and timing behavior.

For applications without external AC-coupling capacitors, the DC lead-off detection is applied directly to the BIP and BIN electrodes, as shown in Figure 15. However, when external AC-coupling capacitors are used, such as in GSR/EDA applications, DC lead-off detection must be applied externally. In this case, BIP and BIN must be assigned to EL2A and EL3A, and DC lead-off detection is applied externally through EL2B and EL3B. To enable this feature, EL2B and EL3B must be connected outside the AC-coupling capacitors, as shown in Figure 15, and EN_EXT_LOFF[5](0x50) must be enabled in addition to EN_LOFF_DET.

The DRV lead-off circuit checks the BioZ current stimulus path to determine if or not the DRVP and DRVN connections are in place when using a tetrapolar electrode configuration. In this case, one or both the DRVP and DRVN electrodes are compromised and are not reliably connected to the body. When the impedance between the DRVP and DRVN electrodes becomes too high, the magnitude of this amplifier output signal starts to approach one or both rails (AVDD or AGND), getting very close to amplifier saturation. When the DRV lead-off circuit is enabled, a sample-and-hold circuit followed by a dual-comparator samples the I_{DRV} amplifier output signal and determines if it is outside 0.27V and V_{AVDD} - 0.35V. If it is, the comparator trips and a DRV lead-off condition is flagged. To turn on the DRV lead-off circuit, set EN_DRV_OOR[4](0x50) to 1. An out-of-range condition must be exceeded for either 125ms or 128ms, depending on CLK_FREQ_SEL[5](0x1A), before the DRV_OOR status bit is asserted.

The BioZ threshold (AC lead-off) detection circuit monitors the output of the BioZ ADC with programmable high or low thresholds, and is enabled by EN_BIOZ_THRESH[0](0x21). The thresholds are set by BIOZ_LO_THRESH[7:0](0x26) and BIOZ_HI_THRESH[7:](0x27). If the digitized output remains over BIOZ_HI_THRESH or under BIOZ_LO_THRESH for longer than 128ms, then the BIOZ_OVER[6](0x01) or BIOZ_UNDR[5](0x01) is asserted. This behavior is described graphically in Figure 16.

Table 8 shows the lead-off techniques suitable for each electrode configuration and lead-off condition. The internal HPF is suitable for stimulus frequencies above 1kHz, and external capacitors are need for stimulus frequencies under 1kHz.

Table 8. BioZ Lead-Off Cases

CONFIGURATION	CONDITION	DRVP	DRVN	BIP	BIN	MEASURED SIGNAL	LEAD-OFF TECHNIQUES
Bipolar, internal HPF	DRVP/BIP off	DDS sine	large signal	DDS sine	large signal	large	DC Lead-Off, DRVN Lead-Off, AC Lead-Off (Over)
Bipolar, internal HPF	DRVP/BIN off	DDS sine	large signal	DDS sine	large signal	large	DC Lead-Off, DRVN Lead-Off, AC Lead-Off (Over)
Bipolar, external capacitors	DRVP/BIP off	DDS sine	large signal	DDS sine	large signal	large	DRVN Lead-Off, AC Lead-Off (Over)
Bipolar, external capacitors	DRVN/BIN off	DDS sine	large signal	DDS sine	large signal	large	DRVN Lead-Off, AC Lead-Off (Over)
Tetrapolar, internal HPF	DRVP off	DDS sine	large signal	large signal	large signal	indeterminant	DRVN Lead-Off
Tetrapolar, internal HPF	DRVN off	DDS sine	railed	railed	railed	railed	DRVN Lead-Off, AC Lead-Off (Over)
Tetrapolar, internal HPF	BIP off	V_{MID_TX}	normal	V_{MID_RX}	normal	1/2 of normal size	DC Lead-Off, AC Lead-Off (Under)

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Table 8. BioZ Lead-Off Cases (continued)

CONFIGURATION	CONDITION	DRVP	DRVN	BIP	BIN	MEASURED SIGNAL	LEAD-OFF TECHNIQUES
Tetrapolar, internal HPF	BIN off	V_{MID_TX}	normal	V_{MID_RX}	V_{MID_RX}	near DC	DC Lead-Off, AC Lead-Off (Under)
Tetrapolar, internal HPF	BIP and BIN off	V_{MID_TX}	normal	V_{MID_RX}	V_{MID_RX}	near DC	DC Lead-Off, AC Lead-Off (Under)
Tetrapolar, internal HPF	DRVP and BIP off	DDS sine	large signal	V_{MID_RX}	large signal	large	DC Lead-Off, DRVN Lead-Off, AC Lead-Off (Over)
Tetrapolar, internal HPF	DRVP and BIN off	DDS sine	large signal	DDS sine	V_{MID_RX}	DDS sine magnitude	DC Lead-Off, DRVN Lead-Off
Tetrapolar, internal HPF	DRVN and BIP off	DDS sine	large signal	V_{MID_RX}	large signal	large	DC Lead-Off, DRVN Lead-Off, AC Lead-Off (Over)
Tetrapolar, internal HPF	DRVN and BIN off	DDS sine	large signal	DDS sine	V_{MID_RX}	DDS sine magnitude	DC Lead-Off, DRVN Lead-Off
Tetrapolar, external capacitors	DRVP off	DDS sine	large signal	large signal	DDS sine	large	DRVN Lead-Off, AC Lead-Off (Over)
Tetrapolar, external capacitors	DRVN off	DDS sine	large signal	large signal	large signal	indeterminant	AC Lead-Off (Over)
Tetrapolar, external capacitors	BIP off	V_{MID_TX}	normal	V_{MID_RX}	normal	DDS sine magnitude	DC Lead-Off
Tetrapolar, external capacitors	BIN off	V_{MID_TX}	normal	normal	V_{MID_RX}	DDS sine magnitude	DC Lead-Off
Tetrapolar, external capacitors	BIP and BIN off	V_{MID_TX}	normal	V_{MID_RX}	V_{MID_RX}	near DC	DC Lead-Off, AC Lead-Off (Under)
Tetrapolar, external capacitors	DRVP and BIP off	DDS sine	large signal	V_{MID_RX}	large signal	large	DC Lead-Off, DRVN Lead-Off, AC Lead-Off (Over)
Tetrapolar, external capacitors	DRVP and BIN off	DDS sine	large signal	large signal	V_{MID_RX}	large	DC Lead-Off, DRVN Lead-Off, AC Lead-Off (Over)
Tetrapolar, external capacitors	DRVN and BIP off	DDS sine	large signal	V_{MID_RX}	DDS sine	DDS sine magnitude	DC Lead-Off
Tetrapolar, external capacitors	DRVN and BIN off	DDS sine	large signal	DDS sine	V_{MID_RX}	DDS sine magnitude	DC Lead-Off

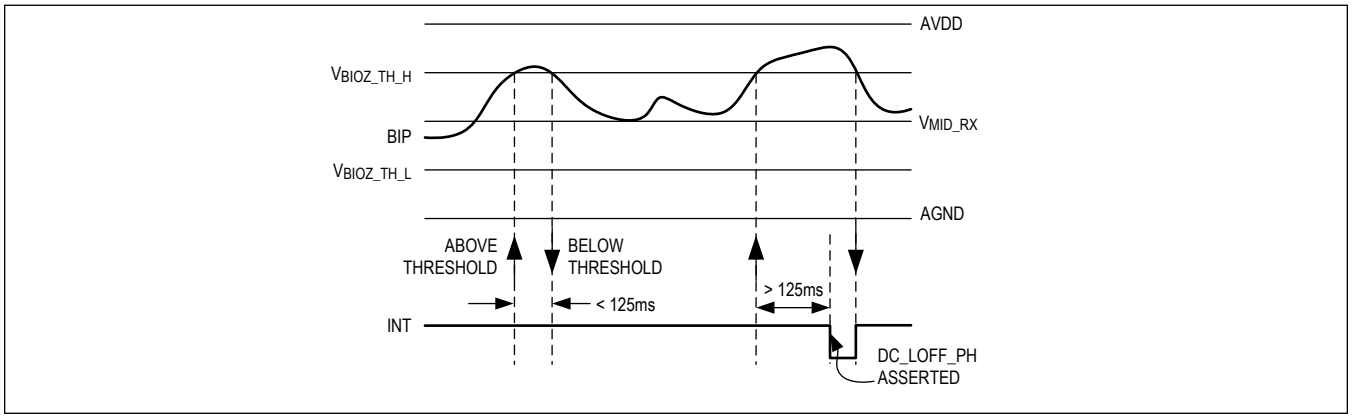

Figure 14. BioZ DC Lead-Off Behavior

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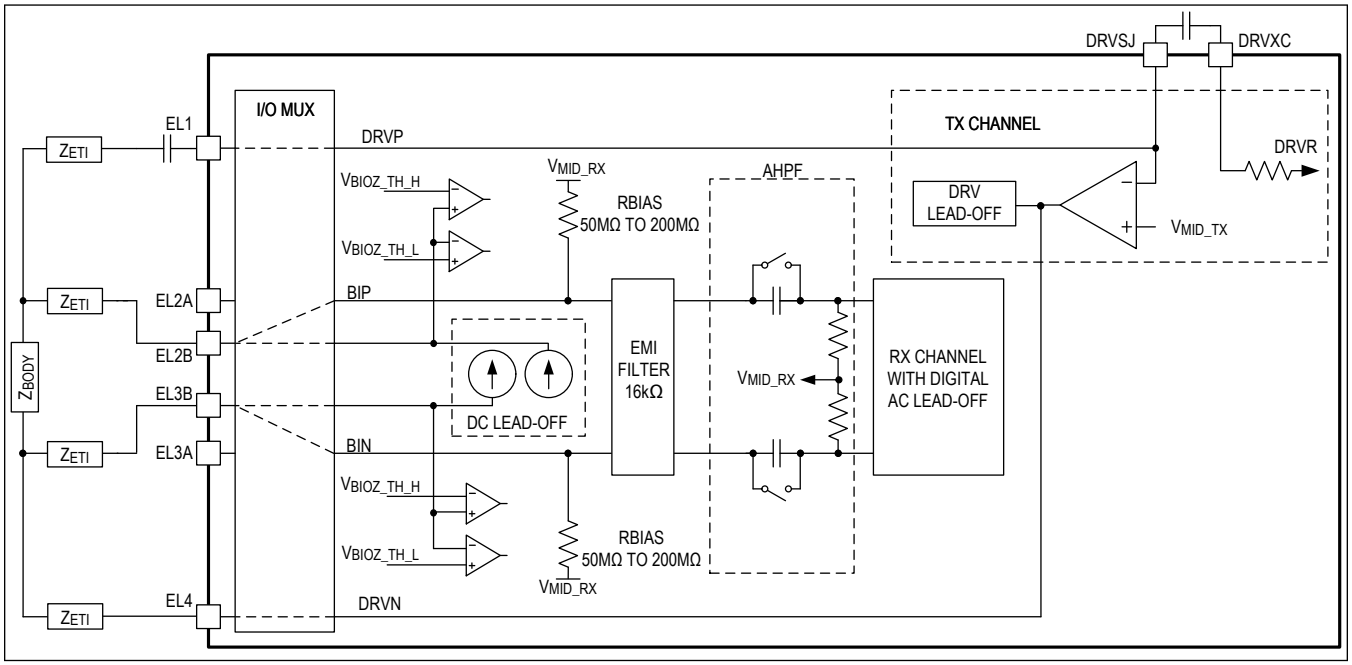

Figure 15. BioZ DC Lead-Off Detection with Internal Sense

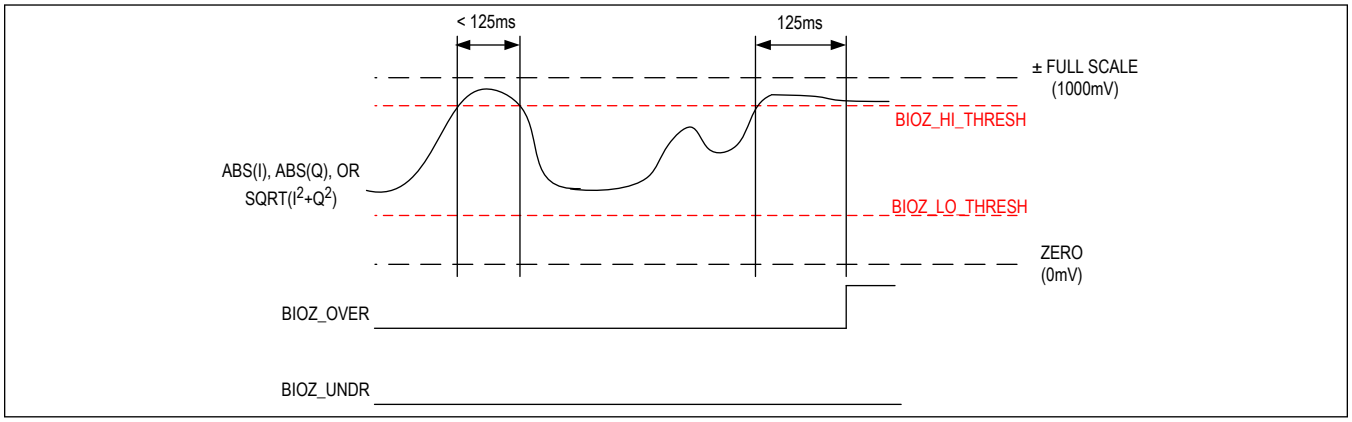

Figure 16. BioZ Threshold Behavior

BioZ Ultra-Low-Power (ULP) Lead-On Detection

The MAX30009 features an Ultra-Low-Power (ULP) lead-on detection circuit for the BioZ input electrodes. The BioZ channel must be disabled (BIOZ_I_EN[0](0x20) and BIOZ_Q_EN[1](0x20) = 0) when ULP lead-on detection is enabled.

The ULP lead-on detect circuit operates by pulling BIN low with a pulldown resistance of 5MΩ (typ) and pulling BIP high with a pullup resistance of 15MΩ (typ). A low-power comparator determines if BIP is pulled below 0.75 x AVDD (typ), and asserts the LON[7](0x01) status bit if BIP remains below the threshold for at least 128ms. This circuit is shown in Figure 12. Because this circuit relies on DC current flowing through the electrodes, it does not work when external AC-coupling capacitors are used on the pins assigned to BIP and BIN.

There are several conditions that can pull BIP below the threshold and trigger a lead-on status:

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- The total impedance between BIP and BIN is below 40MΩ (typ) due to both electrodes contacting the body.
- The total impedance between BIP and AGND is below 45MΩ (typ) due to the the BIP electrode contacting a body that is coupled to AGND. For example, if the MAX30009 system is coupled to earth ground through a power or data cable, and the body is also coupled to earth ground, then a low-impedance path can pull the BIP electrode low.
- The BIP electrode is contacting the body and has a large half-cell potential. The half-cell potential can push the BIP voltage below the threshold.

If the LON interrupt is enabled by LON_EN1[7](0x81), an interrupt is generated to alert the host microcontroller of the lead-on condition. This interrupt allows the microcontroller to sleep when the system is not in use, and only wake up when the device electrodes are touched. Upon receiving an interrupt and waking up, the microcontroller should read the LON status register to determine if a lead-on condition occurred. Because of the bit's clear-on-read behavior, read the status register a second time to determine if the lead-on condition persists.

BioZ Calibration

The MAX30009 can be calibrated, and can achieve impedance magnitude errors of 0.1% and impedance phase errors of 0.1°. The calibration can be performed at the factory by applying a precision resistor to the device electrodes, or on-board by connecting a precision resistor to the CALx pins. To achieve 0.1% accuracy, the calibration resistor(s) must have 0.05% tolerance, or be measured by an external reference with 0.05% accuracy. If using an on-board calibration, the reference resistor (R_{CAL}) should have a low temperature coefficient and should be connected to the calibration port, as shown in Figure 17. To connect the on-board R_{CAL}, assert MUX_EN[1](0x41) and CAL_EN[0](0x41).

The calibration consists of measuring the I and Q offsets, and magnitude and phase coefficients at each measurement frequency, according to the following steps. Registers not mentioned in the following steps should be set to the values intended for use during measurement.

1. Set the synthesis frequency to the desired frequency.
2. Measure the I and Q offsets:
    1. Set the stimulus current magnitude to the minimum $16nA_{RMS}$ by setting BIOZ_VDRV_MAG[5:4](0x22) and BIOZ_IDRV_RGE[3:2](0x22) to 0x0.
    2. Enable BIOZ_DRV_RESET[5](0x25) to apply a short circuit across the load.
    3. Set BIOZ_I_EN[0](0x20) and BIOZ_Q_EN[1](0x20) to 1 to enable measurement.
    4. Record data until the impedance signal is settled, and then record the average impedance in Ω (I_offset [Ω], Q_offset[Ω]). Settling time varies with sample rate, filter selections, and other settings.
    5. Note: I_offset and Q_offset should be calculated using the intended measurement current magnitude, not the minimum $16nA_{RMS}$.
3. Measure the calibration resistor with both channels set to in-phase:
    1. Set the stimulus current to the desired value by adjusting BIOZ_VDRV_MAG[5:4](0x22) and BIOZ_IDRV_RGE[3:2](0x22).
    2. Disable BIOZ_DRV_RESET[5](0x25).
    3. Set BIOZ_Q_CLK_PHASE[3](0x28) to 1, which shifts the Q-channel's demodulation clock to in-phase.
    4. Set BIOZ_I_EN[0](0x20) and BIOZ_Q_EN[1](0x20) to 1 to enable measurement.
    5. Record data until the impedance signal is settled, and then record the average impedance in Ω (I_rcal_in [Ω], Q_rcal_in [Ω]).
4. Measure the calibration resistor with both channels set to quadrature-phase:
    1. Set BIOZ_Q_CLK_PHASE[3](0x28) to 0.
    2. Set BIOZ_I_CLK_PHASE[2](0x28) to 1, which shifts the I-channel's demodulation clock to quadrature phase.
    3. Set BIOZ_I_EN[0](0x20) and BIOZ_Q_EN[1](0x20) to 1 to enable measurement.
    4. Record data until the impedance signal is settled, and then record the average impedance in Ω (I_rcal_quad [Ω], Q_rcal_quad [Ω]).
5. Subtract the offsets from the resistor measurements:
    1. I_cal_in [Ω] = I_rcal_in - I_offset
    2. Q_cal_in [Ω] = Q_rcal_in - Q_offset
    3. I_cal_quad [Ω] = I_rcal_quad - I_offset
    4. Q_cal_quad [Ω] = Q_rcal_quad - Q_offset
6. Calculate the calibration magnitude and phase delay coefficients for each channel:

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1. $I_coef = \sqrt{(I_cal_in^2 + I_cal_quad^2)} / R_{CAL}$
2. $Q_coef = \sqrt{(Q_cal_in^2 + Q_cal_quad^2)} / R_{CAL}$
3. I_phase_coef [°] = arctan(I_cal_quad / I_cal_in) x 180° / π
4. Q_phase_coef [°] = arctan(-Q_cal_quad / -Q_cal_in) x 180° / π

To apply the calibration coefficients to a measured impedance, follow these steps.

1. Measure I and Q load impedances (I_load [Ω] and Q_load [Ω]).
2. Subtract the offsets from the load impedances:
   1. I_load_offset [Ω] = I_load - I_offset
   2. Q_load_offset [Ω] = Q_load - Q_offset
3. Apply I and Q coefficients to correct magnitude and phase delay of each channel:
   1. I_cal_real [Ω] = (I_load_offset / I_coef) x cos(I_phase_coef x π / 180)
   2. I_cal_imag [Ω] = (I_load_offset / I_coef) x sin(I_phase_coef x π / 180)
   3. Q_cal_real [Ω] = (Q_load_offset / Q_coef) x sin(Q_phase_coef x π / 180)
   4. Q_cal_imag [Ω] = (Q_load_offset / Q_coef) x cos(Q_phase_coef x π / 180)
4. Calculate the corrected load impedance:
   1. Load_real [Ω] = I_cal_real - Q_cal_real
   2. Load_imag [Ω] = I_cal_imag + Q_cal_imag
   3. $Load_mag [\Omega] = \sqrt{(Load_real^2 + Load_imag^2)}$
   4. Load_angle [°] = arctan(Load_imag / Load_real) x 180 / π

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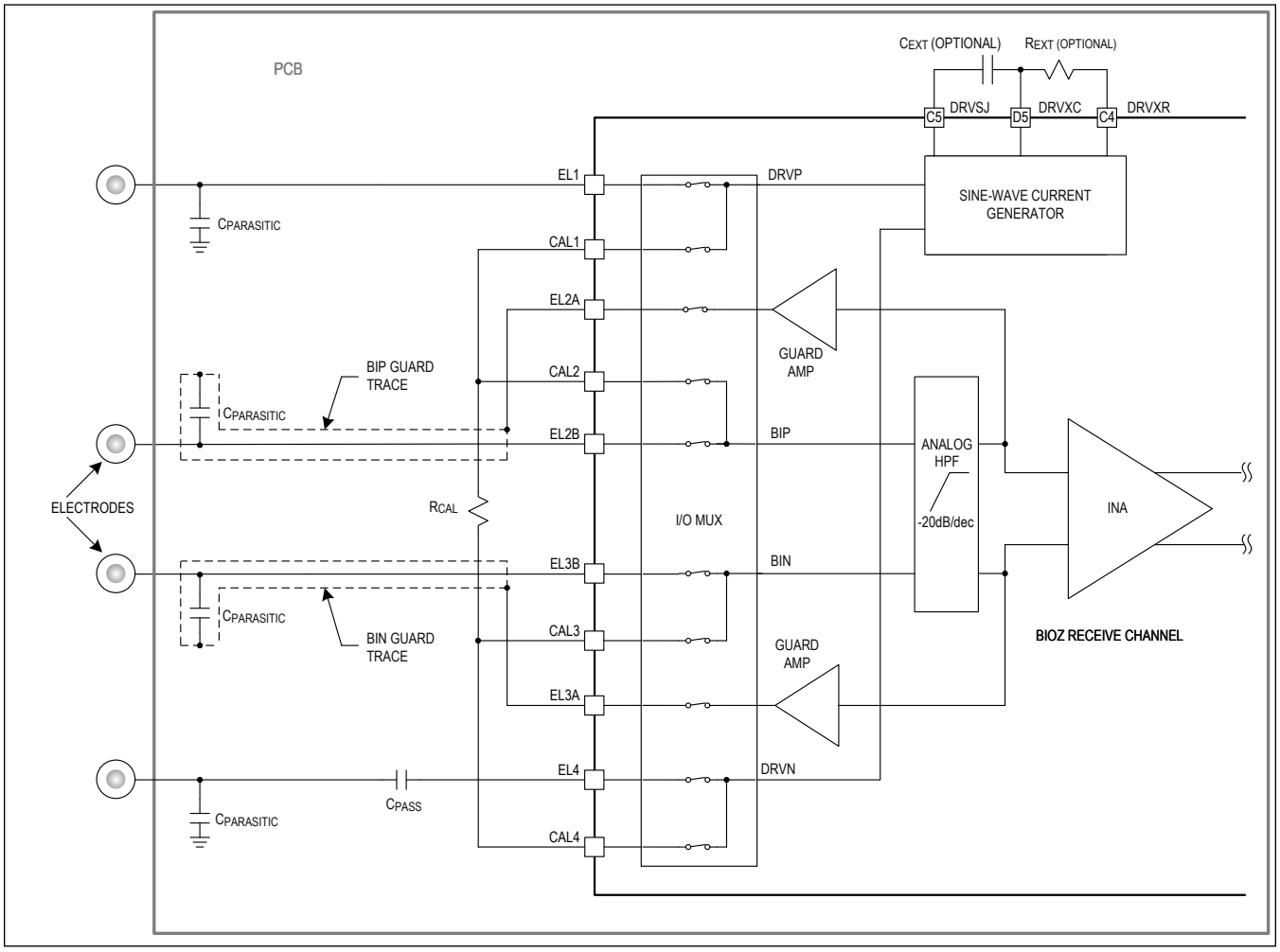

Figure 17. Calibration Port Connections

Improving Accuracy of BIA/BIS Measurements

The parasitic capacitance on the pins assigned to DRVP and DRVN can be calibrated using the procedure described above. However, the parasitic capacitances on the pins assigned to BIP and BIN are more difficult to manage. The MAX30009 has two features to minimize the effect of these receive-channel parasitic capacitances.

First, it is important to realize that differences in BIP and BIN electrode tissue interface impedances working against these parasitic BIP and BIN capacitances can create phase accuracy issues. For instance, if the two PCB traces used to route BIP and BIN to the MAX30009 are carefully managed so that their parasitic capacitances are nearly equal, but the BIP electrode has a higher electrode tissue interface impedance than the BIN electrode. In such a case, the BIP side has more phase lag than the BIN side, creating a potential source of inaccuracy.

This problem can be mitigated with driven guard amplifiers, and BIP and BIN guard traces. The BIP and BIN-driven guard amplifiers can be enabled using EN_EXT_INLOAD[1](0x42). The outputs of the BIP and BIN guard amplifiers are offered at pins EL2A and EL3A, respectively. Guard traces remove the effect of the parasitic PCB capacitances by driving a guard signal, that moves at the same frequency, amplitude, and phase as the input signal of interest. These guard signal routes can be used to surround the BIP and BIN nets, usually parallel to the nets and on both sides. As there is no AC voltage drop across these parasitic capacitances, there are no associated AC currents needed to charge or discharge

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them.

To help mitigate the effects of parasitic capacitances within the MAX30009 itself, assert the EN_INT_INLOAD[0](0x42), which enables an inverse capacitive load on each input.

Digital Interface

The MAX30009 supports I2C interface and Serial Peripheral Interface (SPI). The CSB/I2C_SEL pin selects the interface being used at a time. When the I2C_SEL pin is high using an external pullup resistor, the interface is in the I2C mode and idles looking for a start condition on the SCL and SDA pins, while the SPI is held in a reset state. When the CSB/I2C_SEL pin is low, the I2C interface is disabled and SPI is activated. The following sections describe the timings and protocols for both interfaces.

Serial Peripheral Interface (SPI)

The SPI on the MAX30009 is SPI-/QSPI-/microwire-/DSP-compatible consisting of a Serial Data Input (SDI), Serial Data Output (SDO), Serial Clock Line (SCLK), and Chip Select (CSB). In SPI mode, the SDI/SDA pin operates as SDI and the SCLK/SCL pin operates as SCLK. The timing of the SPI is shown in Figure 18. Data is strobed on the SCLK rising edge while clocked out on the SCLK falling edge. All single-word SPI read and write operations are done in a 3-byte, 24-clock-cycle SPI instruction framed by a CSB low interval. The content of the SPI operation consists of a one-byte register address (A[7:0]) followed by a one-byte command word, which defines the transaction as write or read, followed by a single-byte data word either written to or read from the register location provided in the first byte.

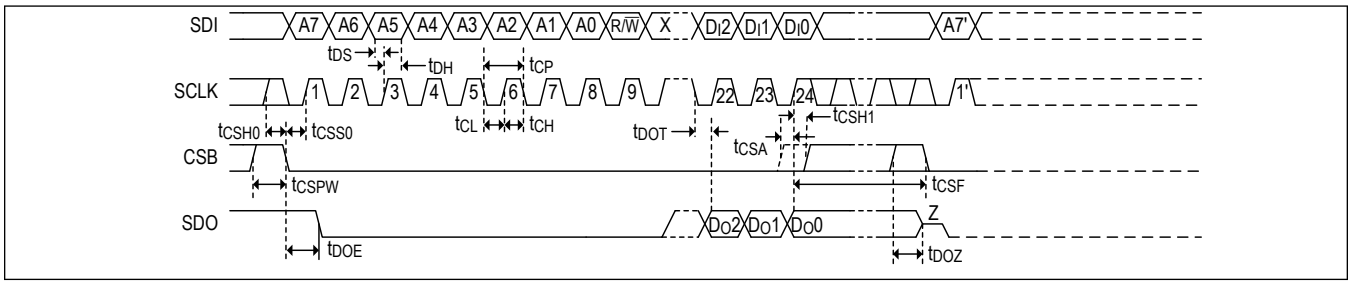

Figure 18. Detailed SPI Timing Diagram

Single-Word SPI Register Read and Write Transactions

SPI write mode operations for MAX30009 are executed on the 24th SCLK rising edge using the first three bytes of data available. In write mode, any data supplied after the 24th SCLK rising edge is ignored, as shown in Figure 19. Subsequent writes require CSB to deassert high and then assert low for the next write command. A rising CSB edge preceding the 24th rising edge of SCLK by t_{CSA}, as shown in Figure 18, results in the transaction being aborted.

Read mode operations access the requested data on the 16th SCLK rising edge, and present the MSB of the requested data on the following SCLK falling edge, allowing the microcontroller to latch the data MSB on the 17th SCLK rising edge, as shown in Figure 20. Configuration and status registers are available using normal-mode read-back sequences. FIFO reads must be done with a burst mode FIFO read (see the SPI Burst Mode Read Transaction section). In a normal read sequence, any SCLK rising edges after the 24th SCLK rising edge are ignored and if more than 24 SCLK rising edges are provided, the device reads back zeros.

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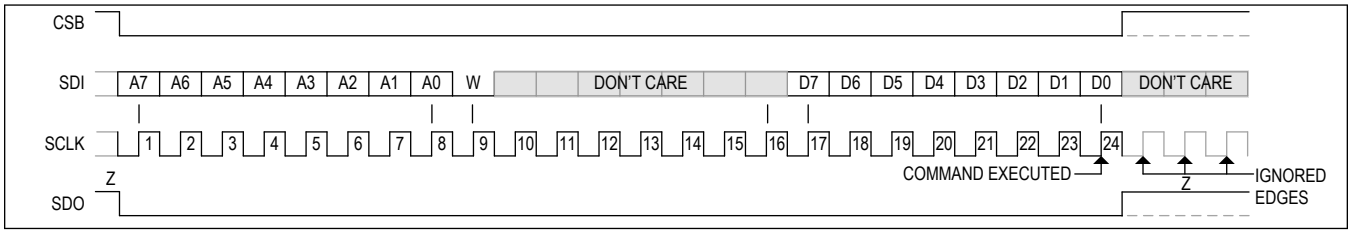

Figure 19. SPI Write Transaction

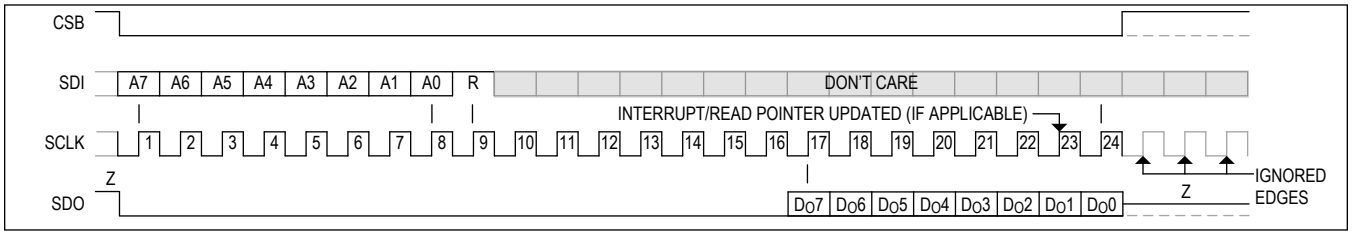

Figure 20. SPI Read Transaction

SPI Burst-Mode Read Transaction

The MAX30009 has a FIFO burst-read mode to increase data transfer efficiency. The first 16 SCLK cycles operate exactly as described for the normal read mode, where the first byte is the register address and the second is the read command. The subsequent SCLKs consist of FIFO data, 24 SCLKs per word. All words in the FIFO should be read with a single FIFO burst-read command.

Each FIFO sample consists of three bytes per sample, and thus requires 24 SCLKs per sample to read out. The first byte (SCLK 17 to 24) consists of a tag indicating the data type of the subsequent bits as well as the MSBs of the data. The next two bytes (SCLK 24 to 40) consist of data. For example, Figure 21 shows a FIFO burst read consisting of three PPG samples in FIFO, labeled A through C, each with a 4-bit tag and 20-bit data. The number of words in the FIFO depends on the FIFO configuration. See the FIFO Description section for more details about the FIFO configuration and readout.

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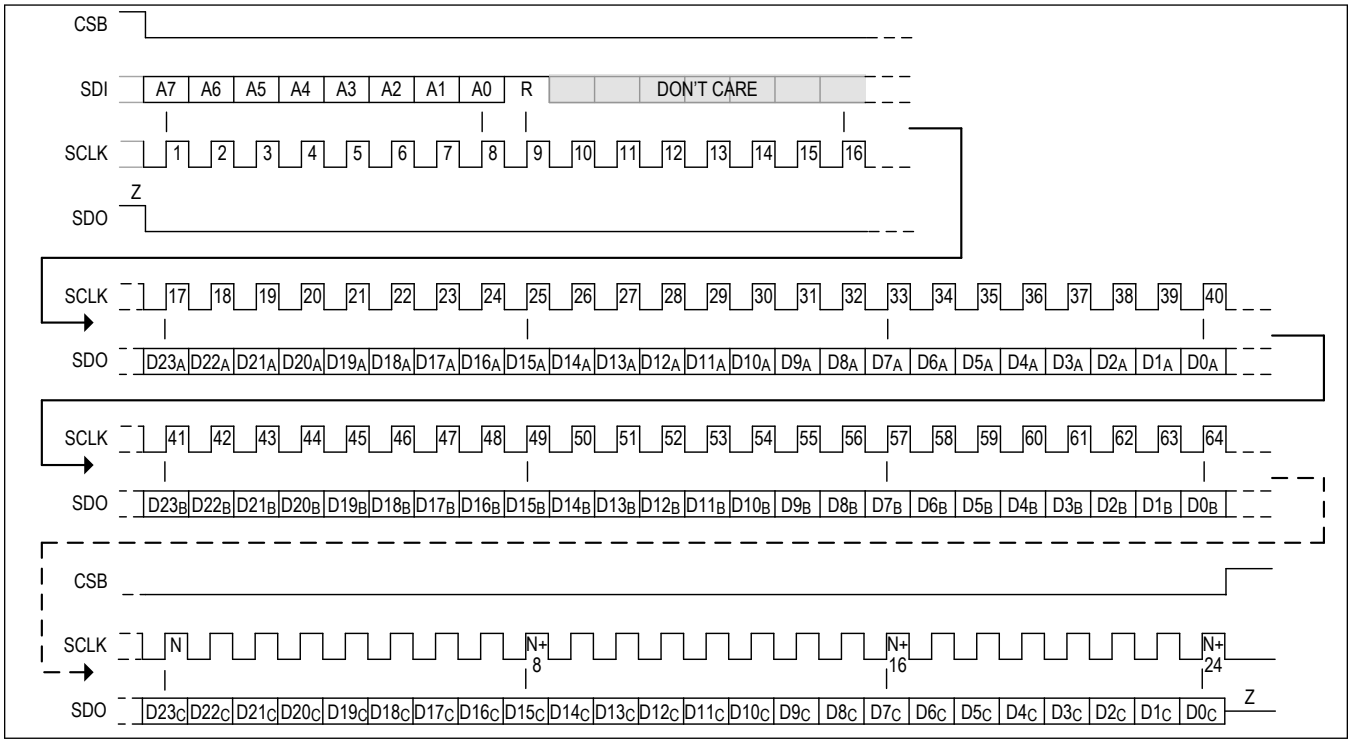

Figure 21. SPI FIFO Burst Mode Read Transaction

I²C-/SMBus-Compatible Serial Interface

The I²C interface on the MAX30009 is an I²C-/SMBus-compatible, two-wire serial interface consisting of an SDA and a SCL. In the I²C mode, the SDI/SDA pin operates as SDA and the SCLK/SCL pin operates as SCL. These two pins are used for the communication between the MAX30009 and the master at clock rates up to 400kHz. Figure 22 shows the two-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. The master device writes data to the MAX30009 by transmitting the proper slave address, followed by the register address, and then the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition, and a STOP (P) condition. Each word transmitted to the MAX30009 is 8-bits long and is followed by an acknowledge clock pulse. A master reading data from the MAX30009 transmits the proper slave address, followed by a series of nine SCL pulses. The MAX30009 transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START (S) or REPEATED START (Sr) condition, a not acknowledge (NACK), and a STOP (P) condition. SDA operates as both an input and open-drain output. A pullup resistor is required on SDA. SCL operates only as an input. A pullup resistor is required on SCL if there are multiple masters on the bus, or if the single master has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs from high-voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

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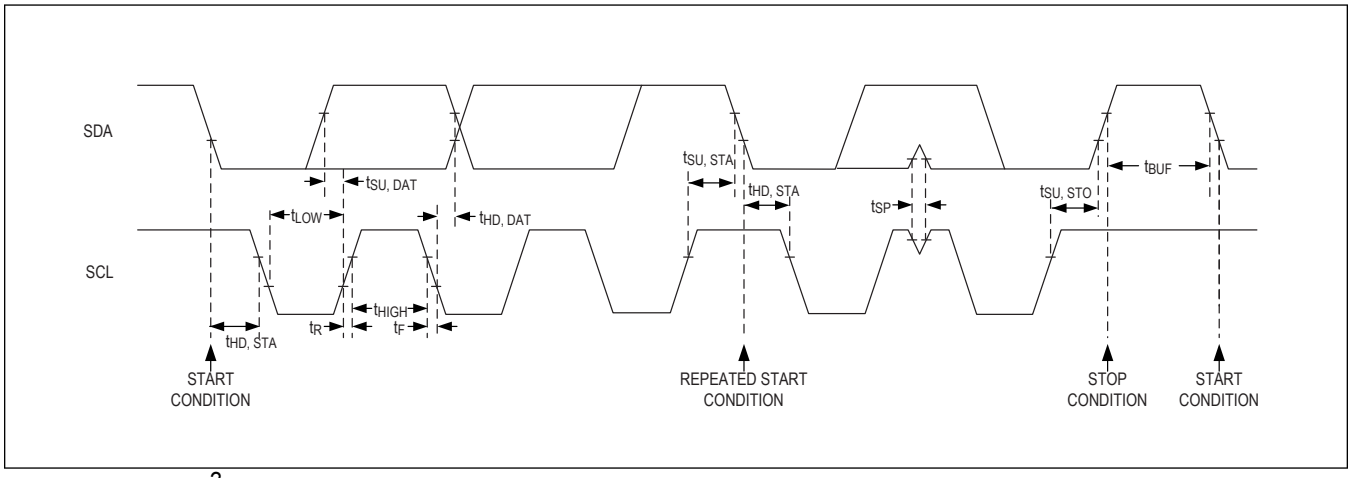

Figure 22. Detailed I^2C Timing Diagram

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section).

START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition, which indicates the beginning of a transmission to the MAX30009. A START condition is a high-to-low transition on SDA while SCL is high, as shown in Figure 23. The master terminates transmission, and frees the bus, by issuing a STOP condition. A STOP condition is a low-to-high transition on SDA while SCL is high, as shown in Figure 23. The bus remains active if a REPEATED START condition is generated instead of a STOP condition. A REPEATED START condition is the same as a START condition (high-to-low transition with SCL high), but it is sent after a START condition.

The MAX30009 recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

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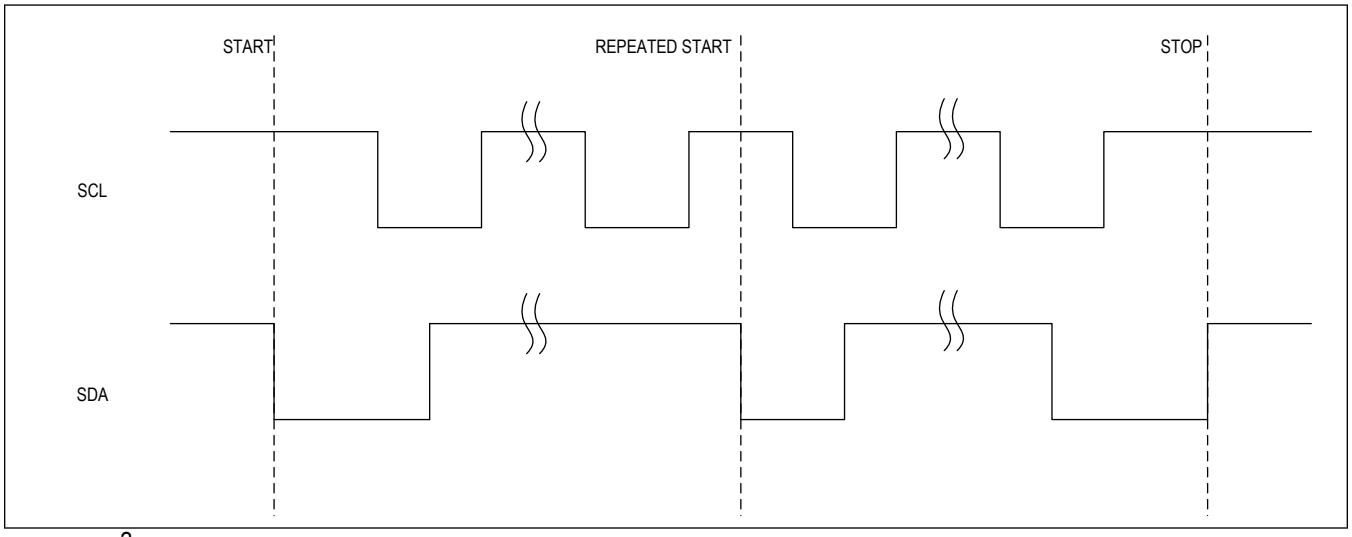

Figure 23. I²C START, STOP, and REPEATED START Conditions

I²C Slave Address

In the I²C mode, the SDO/ADDR pin acts as the device address selector pin. The I²C slave address has two values, selected by SDO/ADDR when the I2C_SEL pin is pulled high. When ADDR is pulled low, either by a pulldown resistor or by the host controller, the slave address is 0xD0 (write) and 0xD1 (read), or 0b1101000 + R/$\overline{W}$. When ADDR is pulled high, the slave address is 0xD2 (write) and 0xD3 (read), or 0b1101001 + R/$\overline{W}$.

Table 9. I²C Addresses for MAX30009

ADDR PIN	WRITE ADDRESS	READ ADDRESS
Low	0xD0	0xD1
High	0xD2	0xD3

Acknowledge Bit

The acknowledge bit (ACK) is a clocked 9th bit that the MAX30009 uses to handshake-receipt each byte of data when in write mode, as shown in Figure 24. The MAX30009 pulls down SDA during the entire master-generated 9th clock pulse if the previous byte is successfully received. Monitoring ACK detects unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault occurred. For an unsuccessful data transfer, the bus master retries communication. The master pulls down SDA during the 9th clock cycle to acknowledge the receipt of data when the MAX30009 is in the read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not-acknowledge is sent when the master reads the final byte of data from the MAX30009, followed by a STOP condition.

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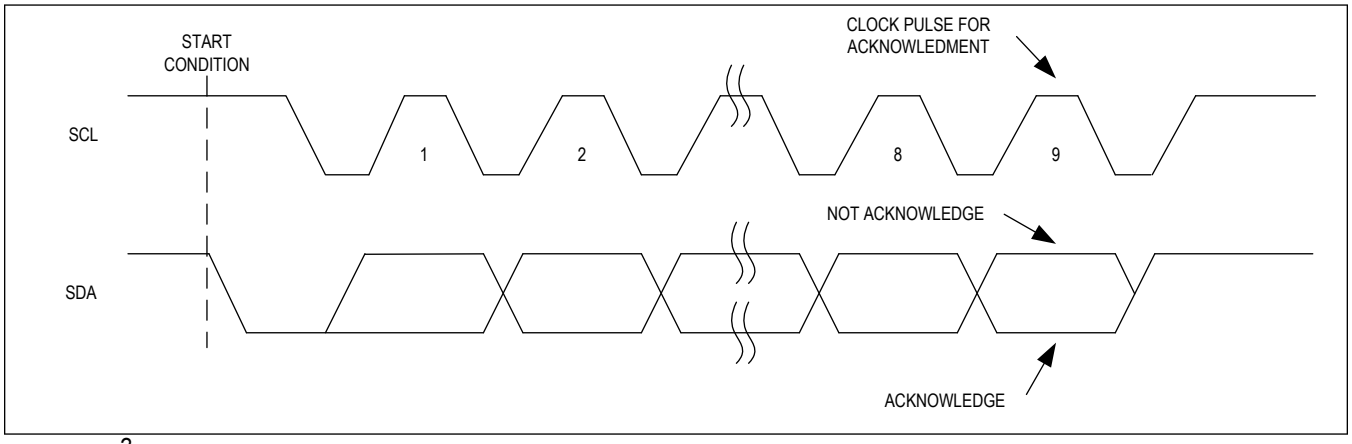

Figure 24. I²C Acknowledge Bit

I²C Write Data Format

A write to the MAX30009 includes the transmission of a START condition, the slave address with the R/$\overline{W}$ bit set to 0, one byte of data to configure the internal register-address pointer, one or more bytes of data, and a STOP condition. Figure 25 illustrates the proper frame format for writing one byte of data to the MAX30009. Figure 26 illustrates the frame format to write multiple bytes of data to the MAX30009.

The slave address with the R/$\overline{W}$ bit set to 0 indicates the master intends to write data to the MAX30009. The device acknowledges receipt of the address byte during the master-generated 9th-SCL pulse.

The second byte transmitted from the master configures the internal register-address pointer of the MAX30009. The pointer tells the device where to write the next byte of data. An acknowledge pulse is sent by the MAX30009 upon receipt of the address-pointer data.

The third byte sent to the MAX30009 contains the data to be written to the pointed register. An acknowledge pulse from the MAX30009 signals receipt of the data byte. The address pointer auto-increments to the next register address after each received data byte. This auto-increment feature allows a master to write to sequential registers within one continuous frame. The master signals the end of transmission by issuing a STOP condition. The auto-increment feature is disabled when there is an attempt to write to the FIFO data register (0x0C).

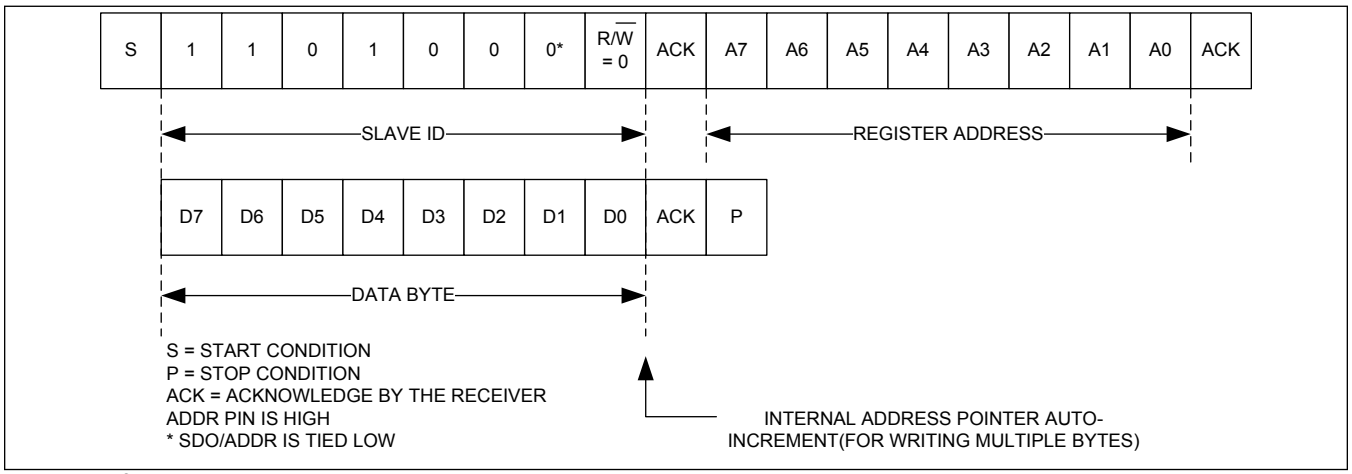

Figure 25. I²C Single-Byte Write Transaction

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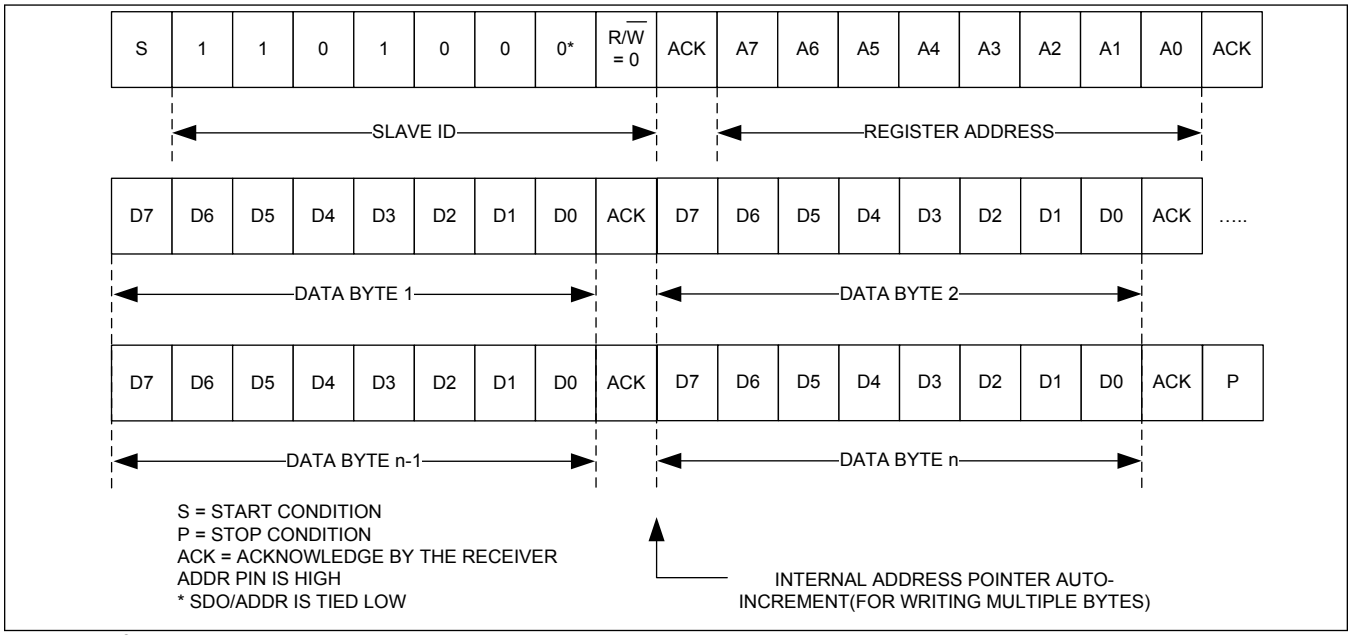

Figure 26. I²C Multibyte Write Transaction

I²C Read Data Format

A read from the MAX30009 includes sending the slave address with the R/$\overline{W}$ bit set to 1 to initiate a read operation. The MAX30009 acknowledges receipt of the slave address by pulling SDA low during the 9th SCL clock pulse. A START command followed by a read command resets the address pointer to register 0x00.

The first byte transmitted from the MAX30009 is the content of register 0x00. Transmitted data is valid on the rising edge of SCL. The address pointer auto-increments after each read data byte. This auto-increment feature allows all registers to be read sequentially within one continuous frame. The auto-increment feature is disabled when there is an attempt to read from the FIFO Data register (0x0C). A STOP condition can be issued after any number of read data bytes. If a STOP condition is issued followed by another read operation, the first data byte to be read is from register 0x00.

The address pointer can be preset to a specific register before a read command is issued. The master presets the address pointer by first sending the MAX30009 slave address with the R/$\overline{W}$ bit set to 0, followed by the register address. A REPEATED START condition is then sent, followed by the slave address with the R/$\overline{W}$ bit set to 1. The MAX30009 then transmits the content of the specified register. The address pointer auto-increments after transmitting the first byte.

The master acknowledges receipt of each read byte during the acknowledge clock pulse. The master must acknowledge all correctly received bytes except the last byte. The final byte must be followed by a not acknowledge from the master and then a STOP condition. Figure 27 illustrates the frame format for reading one byte from the MAX30009. Figure 28 illustrates the frame format for reading multiple bytes from the MAX30009.

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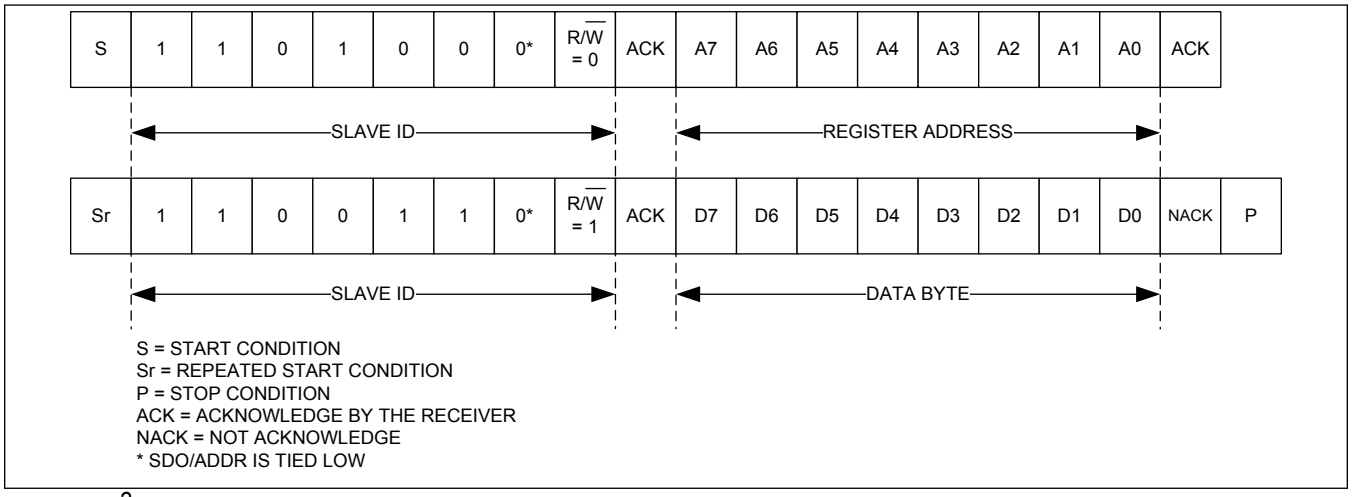

Figure 27. I²C Single-Byte Read Transaction

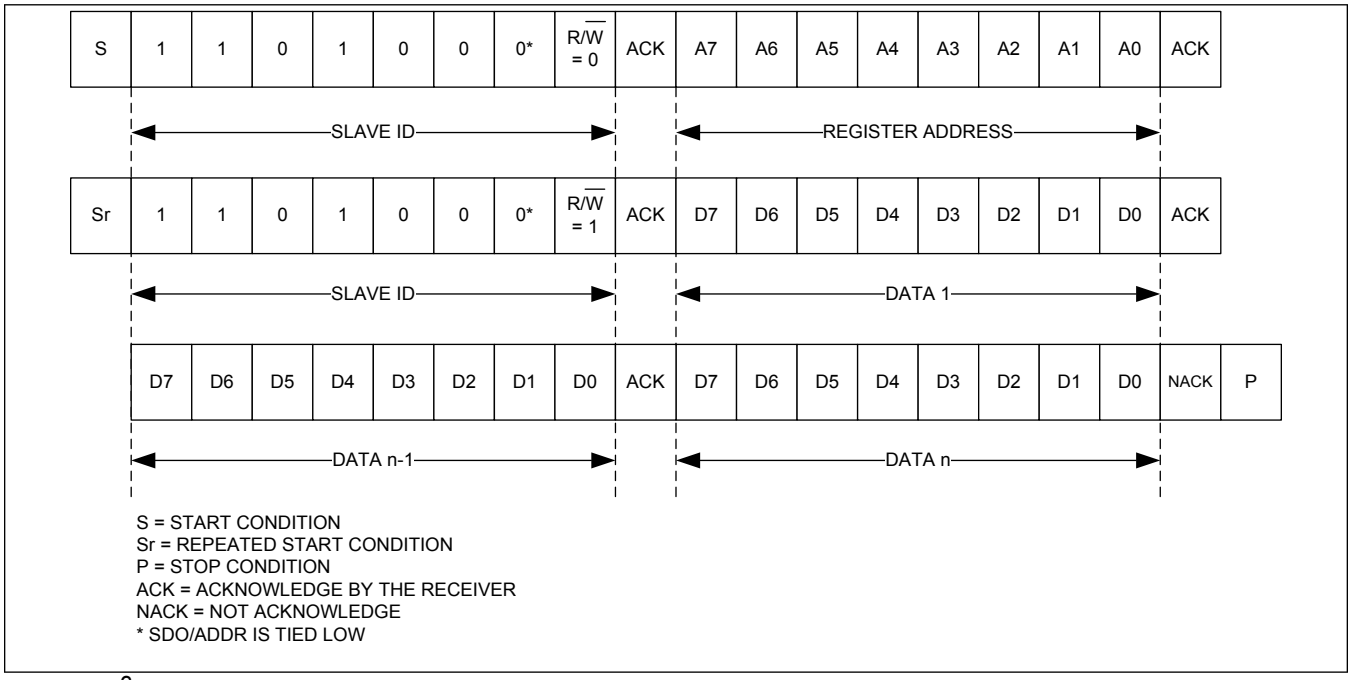

Figure 28. I²C Multibyte Read Transaction

I²C Broadcast

The MAX30009 provides a feature of I²C broadcast write transactions to multiple devices simultaneously using the I²C serial interface. The host microcontroller uses the address programmed in I2C_BCAST_ADDR[7:1](0x14) to send a write command to multiple devices and the slave devices respond with an ACK. To use the broadcast feature, I2C_BCAST_EN[0[(0x14) must be set to 1.

This feature is especially useful for:

1. Synchronizing PLLs on multiple devices using the TIMING_SYS_RESET[7](0x10) bit; thereby, avoiding any external

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connections.

2. Programming the same configuration to multiple devices at the same time.

Read transactions in broadcast mode are not supported. If a host sends out a read command using the I^2C broadcast address, the device responds with a NACK.

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Register Map

User Register Map

ADDRESS	NAME	MSB							LSB
Status									
0x00	Status 1[7:0]	A_FULL	–	FIFO_DATA_RDY	FREQ_UNLOCK	FREQ_LOCK	PHASE_UNLOCK	PHASE_LOCK	PWR_RDY
0x01	Status 2[7:0]	LON	BIOZ_OVER	BIOZ_UNDR	DRV_OOR	DC_LOFF_PH	DC_LOFF_PL	DC_LOFF_NH	DC_LOFF_NL
FIFO									
0x08	FIFO Write Pointer[7:0]	FIFO_WR_PTR[7:0]							
0x09	FIFO Read Pointer[7:0]	FIFO_RD_PTR[7:0]							
0x0A	FIFO Counter 1[7:0]	FIFO_DATA_COUNT[8]	OVF_COUNTER[6:0]						
0x0B	FIFO Counter 2[7:0]	FIFO_DATA_COUNT[7:0]							
0x0C	FIFO Data Register[7:0]	FIFO_DATA[7:0]							
0x0D	FIFO Configuration 1[7:0]	FIFO_A_FULL[7:0]							
0x0E	FIFO Configuration 2[7:0]	–	–	FIFO_MARK	FLUSH_FIFO	FIFO_STAT_CLR	A_FULL_TYPE	FIFO_RO	–
System Control									
0x10	System Sync[7:0]	TIMING_SYS_RESET	–	–	–	–	–	–	–
0x11	System Configuration 1[7:0]	MASTER	DISABLE_I2C	–	–	–	–	SHDN	RESET
0x12	Pin Functional Configuration[7:0]	–	–	–	–	INT_FCFG[1:0]		–	TRIG_ICFG
0x13	Output Pin Configuration[7:0]	–	–	–	–	INT_OCFG[1:0]		TRIG_OCFG[1:0]	
0x14	I2C Broadcast Address[7:0]	I2C_BCAST_ADDR[6:0]							I2C_BCAST_EN
PLL									
0x17	PLL Configuration 1[7:0]	MDIV[9:8]		NDIV	KDIV[3:0]				PLL_EN
0x18	PLL Configuration 2[7:0]	MDIV[7:0]							
0x19	PLL Configuration 3[7:0]	–	–	–	–	–	–	–	PLL_LOCK_WNDW
0x1A	PLL Configuration 4[7:0]	–	REF_CLK_SEL	CLK_FREQ_SEL	CLK_FINE_TUNE[4:0]				
BioZ Setup									
0x20	BioZ Configuration 1[7:0]	BIOZ_DAC_OSR[1:0]		BIOZ_ADC_OSR[2:0]			BIOZ_BG_EN	BIOZ_Q_EN	BIOZ_I_EN
0x21	BioZ Configuration 2[7:0]	BIOZ_DHPF[1:0]		BIOZ_DLPF[2:0]			BIOZ_CMP[1:0]		EN_BIOZ_THRESH

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ADDRESS	NAME	MSB							LSB
0x22	BioZ Configuration 3[7:0]	BIOZ_EXT_RES	LOFF_RAPID	BIOZ_VDRV_MAG[1:0]		BIOZ_IDRV_RGE[1:0]		BIOZ_DRV_MODE[1:0]	
0x23	BioZ Configuration 4[7:0]	–	–	–	–	–	–	BIOZ_FAST_MANUAL	BIOZ_FAST_START_EN
0x24	BioZ Configuration 5[7:0]	BIOZ_AHPF[3:0]				BIOZ_INA_MODE	BIOZ_DM_DIS	BIOZ_GAIN[1:0]	
0x25	BioZ Configuration 6[7:0]	BIOZ_EXT_CAP	BIOZ_DC_RESTORE	BIOZ_DRV_RESET	BIOZ_DAC_RESET	BIOZ_AMP_RGE[1:0]		BIOZ_AMP_BW[1:0]	
0x26	BIOZ Low Threshold[7:0]	BIOZ_LO_THRESH[7:0]							
0x27	BIOZ High Threshold[7:0]	BIOZ_HI_THRESH[7:0]							
0x28	BioZ Configuration 7[7:0]	–	–	–	BIOZ_STBYON	BIOZ_Q_CLK_PHASE	BIOZ_I_CLK_PHASE	BIOZ_INA_CHOP_EN	BIOZ_CH_FSEL
BioZ Calibration									
0x41	BioZ Mux Configuration 1[7:0]	BMUX_RSEL[1:0]		BMUX_BIST_EN	–	–	CONNECT_CAL_ONLY	MUX_EN	CAL_EN
0x42	BioZ Mux Configuration 2[7:0]	BMUX_GSR_RSEL[1:0]		GSR_LOAD_EN	–	–	–	EN_EXT_INLOAD	EN_INT_INLOAD
0x43	BioZ Mux Configuration 3[7:0]	BIP_ASSIGN[1:0]		BIN_ASSIGN[1:0]		DRVP_ASSIGN[1:0]		DRVN_ASSIGN[1:0]	
0x44	BioZ Mux Configuration 4[7:0]	BIST_R_ERR[7:0]							
DC Leads Setup									
0x50	DC Leads Configuration[7:0]	EN_LON_DET	EN_LOFF_DET	EN_EXT_LOFF	EN_DRV_OOR	LOFF_IPOL	LOFF_IMAG[2:0]		
0x51	DC Lead Detect Threshold[7:0]	–	–	–	–	LOFF_THRESH[3:0]			
Lead Bias									
0x58	Lead Bias Configuration 1[7:0]	–	–	–	–	RBIAS_VALUE[1:0]		EN_RBIAS_BIP	EN_RBIAS_BIN
Interrupt Enables									
0x80	Interrupt Enable 1[7:0]	A_FULL_EN	–	FIFO_DATA_RDY_EN	FREQ_UNLOCK_EN	FREQ_LOCK_EN	PHASE_UNLOCK_EN	PHASE_LOCK_EN	–
0x81	Interrupt Enable 2[7:0]	LON_EN	BIOZ_OVER_EN	BIOZ_UNDR_EN	DRV_OOR_EN	DC_LOFF_PH_EN	DC_LOFF_PL_EN	DC_LOFF_NH_EN	DC_LOFF_NL_EN
Part ID									
0xFF	Part ID[7:0]	PART_ID[7:0]							

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Register Details

Status 1 (0x00)

BIT	7	6	5	4	3	2	1	0
Field	A_FULL	–	FIFO_DATA_RDY	FREQ_UNLOCK	FREQ_LOCK	PHASE_UNLOCK	PHASE_LOCK	PWR_RDY
Reset	0	–	0	0	0b0	0	0	1
Access Type	Read Only	–	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

A_FULL

A_FULL is set to 1 when the FIFO reaches the threshold programmed in the FIFO_A_FULL[7:0](0x0D). This is a read-only bit and is cleared when the Status 1 Register is read. It is also cleared when the FIFO Data Register(0x0C) is read if FIFO_STAT_CLR[3](0x0E) = 1.

A_FULL	DECODE
0	Normal operation
1	Indicates the FIFO buffer reached the threshold set by FIFO_A_FULL[7:0](0x0D).

FIFO_DATA_RDY

FIFO_DATA_RDY bit is set to 1 when new data is available in the FIFO. This is a read-only bit and is cleared by reading the Status 1 register. It is also cleared by reading the FIFO Data Register(0x0C) if FIFO_STAT_CLR[3](0x0E) = 1.

FIFO_DATA_RDY	DECODE
0	Normal operation
1	New data is available in the FIFO

FREQ_UNLOCK

FREQ_UNLOCK is set to 1 when the PLL loses the frequency lock. This is a read-only bit and is cleared by reading the Status 1 register. If the frequency unlock state persists, the FREQ_UNLOCK bit is set again.

FREQ_UNLOCK	DECODE
0	The PLL is frequency locked.
1	The PLL is frequency unlocked.

FREQ_LOCK

FREQ_LOCK bit is set to 1 when the PLL frequency gets locked. This is a read-only bit and is cleared by reading the Status 1 register. If the PLL remains locked, the FREQ_LOCK bit continues to be asserted.

PHASE_UNLOCK

PHASE_UNLOCK is set to 1 when the PLL phase is locked and then loses its phase lock. This is a read-only bit and cleared by reading the Status 1 register. If the PLL remains phase unlocked, the PHASE_UNLOCK bit is set again.

PHASE_UNLOCK	DECODE
0	The PLL is phase locked.
1	The PLL is phase unlocked.

PHASE_LOCK

PHASE_LOCK is set to 1 when the PLL achieves phase lock. This is a read-only bit and cleared by reading the Status 1

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register. If the PLL remains in phase lock, the PHASE_LOCK bit is set again.

PHASE_LOCK	DECODE
0	The PLL is phase unlocked.
1	The PLL is phase locked.

PWR_RDY

PWR_RDY is set to 1 when V_{DVDD} goes below the Undervoltage Lockout (UVLO) threshold, which is nominally 1.3V. If this condition occurs, all registers are reset to their POR state. This bit is not triggered by a soft-reset. This is a read-only bit and is cleared when Status 1 register is read, or by setting SHDN[1](0x11) bit to 1.

PWR_RDY is a non-maskable interrupt, so it gets asserted on INT.

Value	Decode
0	Normal operation
1	Indicates that V_{DVDD} goes below the UVLO threshold.

Status 2 (0x01)

BIT	7	6	5	4	3	2	1	0
Field	LON	BIOZ_OVER	BIOZ_UNDR	DRV_OOR	DC_LOFF_PH	DC_LOFF_PL	DC_LOFF_NH	DC_LOFF_NL
Reset	0	0	0	0	0	0	0	0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

LON

LON is set to 1 when a BioZ lead-on condition is detected. This is a read-only bit and is cleared by reading the Status 2 register. If the

BioZ lead-on condition persists, the LON bit is set again.

For the LON status bit to work when PLL is not enabled, set REF_CLK_SEL to 0 to enable the on-chip oscillator.

LON	DECODE
0	BioZ lead-on condition is not detected.
1	BioZ lead-on condition is detected.

BIOZ_OVER

BIOZ_OVER is set to 1 when the absolute value of the BioZ ADC reading exceeds the BioZ high threshold set by register BIOZ_HI_THRESH[7:0](0x27) for more than 128ms if CLK_FREQ_SEL = 0, or 125ms if CLK_FREQ_SEL = 1. This bit is cleared when the Status 2 register is read. If the BIOZ_OVER condition persists at the end of next BioZ sample, the bit is set to 1 again.

This status bit is recommended for use in two-electrode and four-electrode BioZ Lead-Off detection.

BIOZ_OVER	DECODE
0	Normal operation
1	BIOZ_HI_THRESH is exceeded.

BIOZ_UNDR

BIOZ_UNDR is set to 1 when the absolute value of the BioZ ADC reading is below the BIOZ Low Threshold set by register BIOZ_LO_THRESH[7:0](0x26) for more than 128ms if CLK_FREQ_SEL = 0, or 125ms if CLK_FREQ_SEL = 1. This bit is cleared when the Status 2 register is read. If the BIOZ_UNDR condition persists at the end of the next BioZ

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sample, the bit is set to 1 again.

This status bit is recommended for use in four-electrode BioZ Lead-Off detection.

BIOZ_UNDER	DECODE
0	Normal operation
1	BIOZ_LO_THRESH is exceeded.

DRV_OOR

DRV_OOR is set to 1 when the BioZ DRVN voltage peaks are out of range (< 0.2V or > (V_{AVDD} - 0.2V)) for more than 128ms if CLK_FREQ_SEL = 0, or 125ms if CLK_FREQ_SEL = 1.

This bit is cleared when the Status 2 register is read. If the BioZ drive out-of-range condition persists, this bit continues to remain asserted.

DRV_OOR	DECODE
0	Normal operation
1	DRVN is out of range.

DC_LOFF_PH

DC_LOFF_PH is set to 1 when the BIP voltage is greater than $V_{BIOZ_TH_H}$ for more than 128ms if CLK_FREQ_SEL = 0, or 125ms if CLK_FREQ_SEL = 1.

$V_{BIOZ_TH_H}$ is set by LOFF_THRESH[3:0](0x51).

This is a read-only bit and it is cleared by reading the Status 2 register. If the lead-off condition for DC_LOFF_PH persists, this bit is set again.

DC_LOFF_PH	DECODE
0	Normal operation
1	The BIP voltage is greater than $V_{BIOZ_TH_H}$.

DC_LOFF_PL

DC_LOFF_PL is set to 1 when the BIP voltage is less than $V_{BIOZ_TH_L}$ for more than 128ms if CLK_FREQ_SEL = 0, or125ms if CLK_FREQ_SEL = 1.

$V_{BIOZ_TH_L}$ is set by LOFF_THRESH[3:0](0x51).

This is a read-only bit and it is cleared by reading the Status 2 register. If the lead-off condition for DC_LOFF_PL persists, this bit is set again.

DC_LOFF_PL	DECODE
0	Normal operation
1	The BIP voltage is lower than $V_{BIOZ_TH_L}$.

DC_LOFF_NH

DC_LOFF_NH is set to 1 when the BIN voltage is greater than $V_{BIOZ_TH_H}$ for more than 128ms if CLK_FREQ_SEL = 0, or 125ms if CLK_FREQ_SEL = 1.

$V_{BIOZ_TH_H}$ is set by LOFF_THRESH[3:0](0x51).

This is a read-only bit and it is cleared by reading the Status 2 register. If the lead-off condition for DC_LOFF_NH persists, this bit is set again.

DC_LOFF_NH	DECODE
0	Normal operation
1	The BIN voltage is higher than $V_{BIOZ_TH_H}$.

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DC_LOFF_NL

DC_LOFF_NL is set to 1 when the BIN voltage is less than $V_{BIOZ_TH_L}$ for more than 128ms if CLK_FREQ_SEL = 0, or 125ms if CLK_FREQ_SEL = 1.

$V_{BIOZ_TH_L}$ is set by LOFF_THRESH[3:0](0x51).

This is a read-only bit and it is cleared by reading the Status 2 register. If the lead-off condition for DC_LOFF_NL persists, this bit is set again.

DC_LOFF_NL	DECODE
0	Normal operation
1	The BIN voltage is lower than $V_{BIOZ_TH_L}$.

FIFO Write Pointer (0x08)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_WR_PTR[7:0]							
Reset	0x00							
Access Type	Read Only							

FIFO_WR_PTR

FIFO_WR_PTR points to the FIFO location where the next sample is written. This pointer advances for each sample pushed on to the circular FIFO. The write pointer wraps around to count 0x00 as the next FIFO location after count 0xFF.

FIFO Read Pointer (0x09)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_RD_PTR[7:0]							
Reset	0x00							
Access Type	Write, Read, Dual							

FIFO_RD_PTR

FIFO_RD_PTR points to the FIFO location from which the next sample is to be read through the serial interface. This pointer advances each time a sample is read from the circular FIFO. If the PLL is enabled, the read pointer can also be written to. This allows rereading (or retrying) samples from the FIFO. However, writing to FIFO_RD_PTR can have adverse effects if it results in the FIFO being almost full. The read pointer wraps around to count 0x00 after count 0xFF.

If the PLL is disabled, writing to FIFO_RD_PTR register is not allowed.

FIFO Counter 1 (0x0A)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_DATA_COUNT[8]	OVF_COUNTER[6:0]						
Reset	0	0x00						
Access Type	Read Only	Read Only						

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FIFO_DATA_COUNT

FIFO_DATA_COUNT[8](0x0A) is a read-only bit that holds the most significant bit of the number of items available in the FIFO for the host to read. The lower 8 bits are in the FIFO_DATA_COUNT[7:0](0x0B) register. FIFO_DATA_COUNT[8:0] increments when a new item is pushed to the FIFO, and decrements when the host reads an item from the FIFO.

FIFO_DATA_COUNT[8:0] is useful for debug.

OVF_COUNTER

The overflow counter OVF_COUNTER logs the number of samples lost if the FIFO is not read in a timely fashion. When the FIFO is full, any new sample results in either new or old sample getting lost depending on the FIFO_RO[1](0x0E) setting.

This is a read-only register. When a complete sample is read from FIFO and the read pointer advances, the OVF_COUNTER is reset to zero. It should be read immediately before reading the FIFO to check if an overflow condition occurred. This counter saturates at count value 0x7F.

FIFO Counter 2 (0x0B)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_DATA_COUNT[7:0]							
Reset	0x00							
Access Type	Read Only							

FIFO_DATA_COUNT

FIFO_DATA_COUNT[7:0] is a read-only register that holds the lower 8 bits of the number of items available in the FIFO for the host to read.

See the FIFO_DATA_COUNT[8](0x0A) description for details.

FIFO Data Register (0x0C)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_DATA[7:0]							
Reset	0xFF							
Access Type	Read Only							

FIFO_DATA

FIFO_DATA is used to get data from the FIFO using burst reads only. When burst reading from this register, the register address pointer does not auto-increment, and the FIFO_RD_PTR[7:0](0x09) advances to provide subsequent samples. Each sample is three bytes. So, burst reading three bytes in the FIFO_DATA register through the serial interface advances the FIFO_RD_PTR by one count. The format and data type of the data stored in the FIFO is determined by the tag associated with the data. For details and examples of various data types in some use cases, see the FIFO Description section. This is a read-only register.

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FIFO Configuration 1 (0x0D)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_A_FULL[7:0]							
Reset	0x7F							
Access Type	Write, Read							

FIFO_A_FULL

FIFO_A_FULL sets the high-water mark for the FIFO and determines when status bit A_FULL[7](0x00) is asserted. The A_FULL bit is asserted when the FIFO holds (256 - FIFO_A_FULL) samples. For example, if set to 0x0F, A_FULL is asserted when there are 15 empty spaces left (241 samples in FIFO). If A_FULL_EN[7](0x80), then A_FULL being asserted results in an interrupt on the INT pin. This condition should prompt the processor to read samples from the FIFO before it fills and overflows. The A_FULL bit is cleared and the interrupt is deasserted when the Status 1 register (0x00) is read.

FIFO_A_FULL	Free Spaces Before Interrupt is Asserted	Number of Samples in FIFO
0x00	0	256
0x01	1	255
0x02	2	254
0x03	3	253
----	----	----
0xFE	254	2
0xFF	255	1

FIFO Configuration 2 (0x0E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	FIFO_MARK	FLUSH_FIFO	FIFO_STAT_CLR	A_FULL_TYPE	FIFO_RO	–
Reset	–	–	0	0	1	0	1	–
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–

FIFO_MARK

When the FIFO_MARK is set to 1, a marker tag is pushed to the FIFO. FIFO_MARK is a self-clearing bit. The marker tag is useful for differentiating the data in the FIFO before and after the tag.

See the FIFO Description section for the marker tag information.

FLUSH_FIFO

When the FLUSH_FIFO bit is set to 1, the FIFO is flushed, and FIFO_WR_PTR[7:0](0x08), FIFO_RD_PTR[7:0](0x09), FIFO_DATA_COUNT[8:0](0x0A, 0x0B), and OVF_COUNTER[6:0](0x0A) are reset to zero. The contents of the FIFO are lost. FLUSH_FIFO is a self-clearing bit.

FIFO_STAT_CLR

FIFO_STAT_CLR determines if a FIFO_DATA[7:0](0x0C) register read clears the status bits A_FULL[7](0x00) and FIFO_DATA_RDY[5](0x00), and their corresponding interrupts.

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FIFO_STAT_CLR	DECODE
0	A_FULL and FIFO_DATA_RDY status and interrupts do not get cleared by a FIFO_DATA[7:0](0x0C) register read. They get cleared by a Status 1 register read.
1	A_FULL and FIFO_DATA_RDY status and interrupts get cleared by a FIFO_DATA[7:0](0x0C) register read or a Status 1 register read.

A_FULL_TYPE

A_FULL_TYPE defines the behavior of status bit A_FULL[7](0x00) and its corresponding interrupt. When A_FULL_TYPE is set to 0, A_FULL is asserted every time the FIFO almost-full condition is detected. When A_FULL_TYPE is set to 1, A_FULL is asserted only for any new almost-full condition.

A_FULL_TYPE	DECODE
0	A_FULL interrupt gets asserted when the almost full condition is detected. It is cleared by a Status 1 register read, but reasserts for every sample if the almost-full condition persists.
1	A_FULL interrupt gets asserted when the almost-full condition is detected. The interrupt gets cleared by a Status 1 register read, and does not reassert until the FIFO is read and then a new almost-full condition is detected.

FIFO_RO

FIFO_RO controls the behavior of the FIFO when the FIFO becomes completely filled with data. Push to FIFO is enabled when FIFO is full if FIFO_RO is set to 1 and old samples are lost. Both FIFO Write Pointer (0x08) and FIFO Read Pointer (0x09) increment for each sample after the FIFO is full. If FIFO_RO is set to 0, new samples are lost and the FIFO is not updated. FIFO Write Pointer and FIFO Read Pointer do not increment until a sample is read from the FIFO.

FIFO_RO	DECODE
0	The FIFO stops on full.
1	The FIFO automatically rolls over on full.

System Sync (0x10)

BIT	7	6	5	4	3	2	1	0
Field	TIMING_SYS_RESET	–	–	–	–	–	–	–
Reset	0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

TIMING_SYS_RESET

TIMING_SYS_RESET bit works together with the MASTER bit to synchronize the timing sub systems of multiple AFEs.

Writing a one to the TIMING_SYS_RESET bits resets the NDIV divider. This should only be done when BIOZ_BG_EN[2](0x20), BIOZ_I_EN[0](0x20) and BIOZ_Q_EN[1](0x20) are set to 0. TIMING_SYS_RESET is ignored when BIOZ_BG_EN, BIOZ_I_EN or BIOZ_Q_EN are set to 1.

If MASTER = 1, then a sync pulse also appears on the TRIG pin.

If MASTER = 0, writing 1 to the TIMING_SYS_RESET bit has no effect, but any sync pulse on the TRIG pin resets the NDIV divider.

TIMING_SYS_RESET is a self-clearing bit.

Value	Enumeration	Decode
0x0		Normal Mode
0x1		Master Slave Mode

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System Configuration 1 (0x11)

BIT	7	6	5	4	3	2	1	0
Field	MASTER	DISABLE_I2C	–	–	–	–	SHDN	RESET
Reset	0b0	0	–	–	–	–	0	0
Access Type	Write, Read	Write, Read	–	–	–	–	Write, Read	Write, Read

MASTER

The MASTER bit works together with the TIMING_SYS_RESET bit to synchronize the timing sub systems of mulitple AFEs.

When set to 1b'1, this bit causes this device to behave as a master. If MASTER is set to 1'b0, the device is a slave for timing subsystem synchronization.

See TIMING_SYS_RESET for more information.

Value	Enumeration	Decode
0x0		Slave Mode. TRIG pin configured as input by TRIG_ICFG
0x1		Master Mode. TRIG configured as ouput by TRIG_OCFG<1:0>

DISABLE_I2C

When DISABLE_I2C is set to 0 (default), the part uses the I^2C interface or SPI depending on the state of the CSB/I2C_SEL pin. When DISABLE_I2C is set to 1, the part uses the SPI.

For SPI, set this DISABLE_I2C to 1 during initialization after power-up. See the Digital Interface section for more information.

DISABLE_I2C	DECODE
0	CSB/I2C_SEL pin selects interface
1	Part uses SPI interface only

SHDN

Setting SHDN to 1 puts the MAX30009 into shutdown mode. While in shutdown mode, all configuration registers retain their values and write/read operations function normally. All interrupts are cleared to zero in this mode. Also, in this mode, the oscillator is shut down and the part draws minimum current. If this bit is asserted during an active conversion, then the conversion is aborted. Set SHDN to 0 to put the part back in normal mode. See the Shutdown Sequence section for more details.

SHDN	DECODE
0	Normal mode
1	Shutdown mode

RESET

The RESET bit is used to force a power-on-reset sequence. The sequence in Soft-Reset Sequence must be followed when asserting this bit, or registers may become unresponsive until a power-on reset is performed. This is a self-clearing bit and resets to 0 after the reset sequence is completed.

Value	Enumeration	Decode
0	NORMAL	The part is in normal operation. No action is taken.
1	RESET	The MAX30009 undergoes a forced power-on-reset sequence. All configuration, threshold, and data registers are reset to their power-on-state. This bit then automatically becomes ‘0’ after the reset sequence is completed.

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Pin Functional Configuration (0x12)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	INT_FCFG[1:0]		–	TRIG_ICFG
Reset	–	–	–	–	0x1		–	0
Access Type	–	–	–	–	Write, Read		–	Write, Read

INT_FCFG

INT_FCFG controls the function and behavior of the INT pin.

INT_FCFG	DECODE
0x0	Disabled
0x1	INT is enabled and is cleared upon reading of any status register or FIFO.
0x2	INT is enabled and is self-clearing after 30µs to 60µs (depending on PLL_CLK).
0x3	INT is enabled and is self-clearing after 240µs to 480µs (depending on PLL_CLK).

TRIG_ICFG

TRIG_ICFG bit sets the input active edge of the TRIG pin.

TRIG_ICFG	DECODE
0	The TRIG pin active edge is falling.
1	The TRIG pin active edge is rising.

Output Pin Configuration (0x13)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	INT_OCFG[1:0]		TRIG_OCFG[1:0]	
Reset	–	–	–	–	0x0		0x0	
Access Type	–	–	–	–	Write, Read		Write, Read	

INT_OCFG

INT_OCFG[1:0] selects the output drive type for the INT pin.

INT_OCFG	INT OUTPUT DRIVE TYPE
0x0	Open-drain, active-low output.
0x1	Active drive to DVDD and DGND; the active level is a high output.
0x2	Active drive to DVDD and DGND; the active level is a low output.
0x3	Do not use.

TRIG_OCFG

TRIG_OCFG selects the output drive type for the TRIG pin.

TRIG_OCFG	TRIG OUTPUT DRIVE TYPE
0x0	Open-drain, active-low output.
0x1	Active drive to DVDD and DGND; the active level is a high output.
0x2	Active drive to DVDD and DGND; the active level is a low output.
0x3	Do not use.

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I2C Broadcast Address (0x14)

BIT	7	6	5	4	3	2	1	0
Field	I2C_BCAST_ADDR[6:0]							I2C_BCAST_EN
Reset	0x00							0
Access Type	Write, Read							Write, Read

I2C_BCAST_ADDR

I2C_BCAST_ADDR is used to define the upper 7 bits of the I2C address in I2C broadcast mode (I2C_BCAST_EN = 1) when writing to multiple devices simultaneously using the I2C serial interface. I2C_BCAST_ADDR is ignored in SPI mode.

See the I2C Broadcast section for more details.

I2C_BCAST_EN

I2C_BCAST_EN enables write transactions to multiple devices using the broadcast address programmed in I2C_BCAST_ADDR in I2C mode. I2C read transactions are not supported when I2C_BCAST_ADDR is used.

Note that for devices using SPI, broadcast write transactions can be achieved by driving the CSB pins low on multiple devices at the same time.

I2C_BCAST_EN	DECODE
0	Normal mode. I2C transactions are for one device only.
1	I2C broadcast mode. Write transactions to multiple devices are enabled.

PLL Configuration 1 (0x17)

BIT	7	6	5	4	3	2	1	0
Field	MDIV[9:8]		NDIV	KDIV[3:0]				PLL_EN
Reset	0x1		0	0x0				0
Access Type	Write, Read, Dual		Write, Read	Write, Read				Write, Read

MDIV

MDIV[9:0] multiplies the REF_CLK by MDIV + 1 to set the frequency of the PLL. MDIV[9:8] are the 2 MSBs of MDIV[9:0]. The lower 8 bits are in MDIV[7:0](0x18).

MDIV must be set such that PLL_CLK is between 14.0MHz and 28.0MHz.

For information on how to set MDIV[9:0], see the Timing Subsystem section.

NDIV

NDIV divides down the PLL clock as shown in the following table and sets the clock for the BioZ ADC.

For information on how to set BIOZ_NDIV, see the Timing Subsystem section.

NDIV	BioZ N-Divider
0	512
1	1024

KDIV

KDIV divides down the PLL clock as shown in the following table and sets the clock for the DDS DAC.

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For information on how to set KDIV, see the Timing Subsystem section.

KDIV	BIOZ K DIVIDER
0x0	1
0x1	2
0x2	4
0x3	8
0x4	16
0x5	32
0x6	64
0x7	128
0x8	256
0x9	512
0xA	1024
0xB	2048
0xC	4096
0xD	8192
0xE	8192
0xF	8192

PLL_EN

PLL_EN enables the internal PLL, which multiplies the reference clock to a frequency between 14MHz and 28MHz. For details on the PLL, see the Timing Subsystem section. PLL_EN must be set to 1 before enabling BioZ measurements.

PLL_EN	DECODE
0	PLL is disabled
1	PLL is enabled

PLL Configuration 2 (0x18)

BIT	7	6	5	4	3	2	1	0
Field	MDIV[7:0]							
Reset	0xBB							
Access Type	Write, Read, Dual							

MDIV

MDIV[7:0] are the 8 LSBs of MDIV[9:0].

See MDIV[9:8](0x17) register for details.

PLL Configuration 3 (0x19)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	PLL_LOCK_WNDW
Reset	–	–	–	–	–	–	–	0
Access Type	–	–	–	–	–	–	–	Write, Read

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PLL_LOCK_WNDW

PLL_LOCK_WNDW selects the time window for the PLL phase lock detector. The PLL lock detector compares the rising edges of FCLK and the output of the M divider, and determines the PLL to be locked if the difference between the two is less than PLL_LOCK_WNDW. Setting PLL_LOCK_WNDW = 1 helps to avoid false PHASE_UNLOCK interrupts when the FCLK reference has high jitter.

PLL_LOCK_WNDW	PLL PHASE LOCK WINDOW
0	1 PLL clock period
1	2 PLL clock periods (recommended when using high-jitter FCLK input)

PLL Configuration 4 (0x1A)

BIT	7	6	5	4	3	2	1	0
Field	–	REF_CLK_SEL	CLK_FREQ_SEL	CLK_FINE_TUNE[4:0]				
Reset	–	0	0	0x00				
Access Type	–	Write, Read	Write, Read	Write, Read				

REF_CLK_SEL

REF_CLK_SEL	DECODE
0	Internal 32.0kHz or 32.768kHz oscillator used for REF_CLK
1	External oscillator used for REF_CLK

CLK_FREQ_SEL

CLK_FREQ_SEL selects the PLL reference-clock frequency. When using the internal oscillator (REF_CLK_SEL = 0), this bit sets the frequency of the internal oscillator. When using an external clock on the FCLK pin (REF_CLK_SEL = 1), this bit must match the frequency of the external clock. This bit sets the internal timing durations according to the clock frequency.

CLK_FREQ_SEL	DECODE
0	PLL reference clock is 32.0kHz
1	PLL reference clock is 32.768kHz

CLK_FINE_TUNE

CLK_FINE_TUNE is used to fine-tune the internal slow oscillator. This is accomplished by measuring the time between interrupts using a microcontroller, crystal-based real-time oscillator as a reference, and computing the error in the time between interrupts. CLK_FINE_TUNE is a 2's complement code with a resolution of 0.2% per LSB. The total range is +3.0% to -3.2% around the factory trimmed value.

CLK_FINE_TUNE	SHIFT IN FREQUENCY (%)	CLK_FINE_TUNE	SHIFT IN FREQUENCY(%)
0x00	0.0	0x10	-3.2
0x01	0.2	0x11	-3.0
0x02	0.4	0x12	-2.8
0x03	0.6	0x13	-2.6
0x04	0.8	0x14	-2.4
0x05	1.0	0x15	-2.2
0x06	1.2	0x16	-2.0
0x07	1.4	0x17	-1.8
0x08	1.6	0x18	-1.6

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CLK_FINE_TUNE	SHIFT IN FREQUENCY (%)	CLK_FINE_TUNE	SHIFT IN FREQUENCY(%)
0x09	1.8	0x19	-1.4
0x0A	2.0	0x1A	-1.2
0x0B	2.2	0x1B	-1.0
0x0C	2.4	0x1C	-0.8
0x0D	2.6	0x1D	-0.6
0x0E	2.8	0x1E	-0.4
0x0F	3.0	0x1F	-0.2

BioZ Configuration 1 (0x20)

BIT	7	6	5	4	3	2	1	0
Field	BIOZ_DAC_OSR[1:0]		BIOZ_ADC_OSR[2:0]			BIOZ_BG_EN	BIOZ_Q_EN	BIOZ_I_EN
Reset	0x0		0x0			0	0	0
Access Type	Write, Read		Write, Read			Write, Read	Write, Read	Write, Read

BIOZ_DAC_OSR

BIOZ_DAC_OSR[1:0] sets the over sample ratio of the BioZ DDS DAC. For information on how to set BIOZ_DAC_OSR[1:0], see Timing Subsystem.

BIOZ_DAC_OSR	DAC OVER SAMPLING RATIO
0x0	32
0x1	64
0x2	128
0x3	256

BIOZ_ADC_OSR

BIOZ_ADC_OSR[2:0] sets the over sample ratio of the BioZ I and Q ADCs. For information on how to set BIOZ_ADC_OSR[2:0], see Timing Subsystem.

BIOZ_ADC_OSR	ADC OVER SAMPLING RATIO
0x0	8
0x1	16
0x2	32
0x3	64
0x4	128
0x5	256
0x6	512
0x7	1024

BIOZ_BG_EN

BIOZ_BG_EN enables the BioZ bandgap bias required for all functions except the ULP LON. The bias power-up time is approximately 13ms and should be kept on between subsequent measurements.

BIOZ_BG_EN	DECODE
0	BioZ bandgap bias disabled

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1	BioZ bandgap bias enabled

BIOZ_Q_EN

BIOZ_Q_EN enables the bioimpedance drive and receive channels for the quadrature-phase (Q) component when set to 1. When set to 0, the Q receive channel is disabled.

BIOZ_I_EN

BIOZ_I_EN enables the bioimpedance drive and receive channels for the in-phase (I) component when set to 1. When set to 0, the I receive channel is disabled.

BioZ Configuration 2 (0x21)

BIT	7	6	5	4	3	2	1	0
Field	BIOZ_DHPF[1:0]		BIOZ_DLPF[2:0]			BIOZ_CMP[1:0]		EN_BIOZ_THRESH
Reset	0x0		0x0			0x0		0
Access Type	Write, Read		Write, Read			Write, Read		Write, Read

BIOZ_DHPF

BIOZ_DHPF sets the BioZ channel digital high-pass filter cutoff frequency.

BIOZ_DHPF[1:0]	CUTOFF FREQUENCY (Hz)
0x0	Bypass
0x1	0.00025 x SR_BIOZ
0x2	0.002 x SR_BIOZ
0x3	0.002 x SR_BIOZ

BIOZ_DLPF

BIOZ_DLPF sets the BioZ channel digital low-pass filter cutoff frequency.

BIOZ_DLPF[2:0]	CUTOFF FREQUENCY (Hz)
0x0	Bypass
0x1	0.005 x SR_BIOZ
0x2	0.02 x SR_BIOZ
0x3	0.08 x SR_BIOZ
0x4 to 0x7	0.25 x SR_BIOZ

BIOZ_CMP

BIOZ_CMP selects which component of the BioZ measurement is used to compare with the thresholds programmed at BIOZ_HI_THRESH[7:0](0x27) and BIOZ_LO_THRESH[7:0](0x26).

If only one of I and Q channels is enabled, the disabled channel data is zero, and the magnitude of Z is same as the magnitude of the enabled channel data.

BIOZ_CMP[1:0]	COMPONENT
0x0	Magnitude of In-phase component, I only
0x2	Magnitude of Quadrature-phase component, Q only
0x2	Magnitude of Z, where Z = SQRT(I^2 + Q^2)
0x3	Reserved. Do not use

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EN_BIOZ_THRESH

When EN_BIOZ_THRESH bit is set to 1, the BioZ data I, Q, or Z (see BIOZ_CMP[2:1](0x21)) is compared with the thresholds programmed in the BIOZ_HI_THRESH[7:0](0x27) and BIOZ_LO_THRESH[7:0](0x26) registers. The BioZ high threshold can be used for AC lead-off detection in two-electrode systems, and the BioZ low threshold can be used for AC lead-off detection in four-electrode systems. The status is reflected in BIOZ_OVER[6](0x01) and BIOZ_UNDR[5](0x01).

When EN_BIOZ_THRESH is set to 0, threshold detection is disabled.

BioZ Configuration 3 (0x22)

BIT	7	6	5	4	3	2	1	0
Field	BIOZ_EXT_RES	LOFF_RAPID	BIOZ_VDRV_MAG[1:0]		BIOZ_IDRV_RGE[1:0]		BIOZ_DRV_MODE[1:0]	
Reset	0	0	0x0		0x0		0x0	
Access Type	Write, Read	Write, Read	Write, Read, Dual		Write, Read, Dual		Write, Read	

BIOZ_EXT_RES

BIOZ_EXT_RES selects the external R_{EXT} resistor or the internal range settings resistors.

When BIOZ_EXT_RES is set to 0, the internal range resistors are used and the current magnitude is set by both BIOZ_VDRV_MAG[5:4](0x22) and BIOZ_IDRV_RGE[3:2](0x22). BIOZ_VDRV_MAG and BIOZ_IDRV_RGE can be automatically overwritten depending on the stimulus frequency according to patient safety requirements. Note that R_{EXT} is not disconnected, so the DRVXR pin should be unconnected. If DRVXR is connected, R_{EXT} is connected in parallel with the internal range resistor, which results in a larger current magnitude.

When BIOZ_EXT_RES is set to 1, BIOZ_VDRV_MAG and the value of R_{EXT} set the current magnitude. BIOZ_VDRV_MAG is not automatically overwritten.

Value	Enumeration	Decode
0x0		Normal, no ext-res
0x1		Use external res

LOFF_RAPID

LOFF_RAPID bypasses the approximately 128ms window delay for DC lead-off detection. The delay is beneficial in most cases to ignore unintended voltage spikes caused by line noise or electrode movement.

LOFF_RAPID	DECODE
0	A lead off condition must be sustained for approximately 128ms to trigger a DC lead-off status.
1	A lead-off condition immediately triggers a DC lead off status.

BIOZ_VDRV_MAG

In voltage drive mode, BIOZ_VDRV_MAG sets the voltage amplitude at DRVR, which is connected to EL1. BIOZ_IDRV_RGE is ignored.

In current drive mode, BIOZ_VDRV_MAG and BIOZ_IDRV_RGE set the current magnitude. See BIOZ_IDRV_RGE for details.

BIOZ_VDRV_MAG[1:0]	VOLTAGE MAGNITUDE (mV_{PK})	VOLTAGE MAGNITUDE (mV_{RMS})
0x0	50	35.4
0x1	100	70.7

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BIOZ_VDRV_MAG[1:0]	VOLTAGE MAGNITUDE (mV_{PK})	VOLTAGE MAGNITUDE (mV_{RMS})
0x2	250	177
0x3	500	354

BIOZ_IDRV_RGE

BIOZ_IDRV_RGE[1:0] sets the value of the internal current-range resistor, which determines the current magnitude when BIOZ_EXT_RES = 0.

BIOZ_IDRV_RGE[1:0]	INTERNAL RANGE RESISTOR VALUE
0x0	552.5kΩ (V_{DRV} resistor reduced by 4x)
0x1	110.5kΩ
0x2	5.525kΩ
0x3	276.25Ω

When BIOZ_EXT_RES = 1, the external resistor connected between DRVXR and DRVXC determines the drive current amplitude: Drive Current (A_{PK}) = DRVR (V_{PK}) / R_{EXT}.

BIOZ_VDRV_MAG and BIOZ_IDRV_RGE together select the magnitude of the stimulus current. When BIOZ_IDRV_RGE = 0x0, the drive voltage at DRVR is reduced by a factor of four to support smaller current magnitudes.

BIOZ_IDRV_RGE[1:0]	BIOZ_VDRV_MAG[1:0]	AMPLITUDE OF V_{DRVR} (mV_{PK})	AMPLITUDE OF V_{DRVR} (mV_{RMS})	AMPLITUDE OF CURRENT (PEAK)	AMPLITUDE OF CURRENT (RMS)
0x0	0x0	12.5	8.8	23nA	16nA
0x0	0x1	25	17.7	45nA	32nA
0x0	0x2	62.5	44.2	113nA	80nA
0x0	0x3	125	88.4	226nA	160nA
0x1	0x0	50	35.4	452nA	320nA
0x1	0x1	100	70.7	905nA	640nA
0x1	0x2	250	177	2.262µA	1.6µA
0x1	0x3	500	354	4.525µA	3.2µA
0x2	0x0	50	35.4	9.05µA	6.4µA
0x2	0x1	100	70.7	18.10µA	12.8µA
0x2	0x2	250	177	45.25µA	32µA
0x2	0x3	500	354	90.50µA	64µA
0x3	0x0	50	35.4	181µA	128µA
0x3	0x1	100	70.7	362µA	256µA
0x3	0x2	250	177	905µA	640µA
0x3	0x3	500	354	1.81mA	1.28mA

BIOZ_DRV_MODE

BIOZ_DRV_MODE selects the stimulus type of the BioZ transmit channel.

BIOZ_DRV_MODE[1:0]	DRIVE TYPE
0x0	Current Drive. A sine-wave current is driven into the body through selectable electrode pins.
0x1	Voltage Drive. A sine-wave voltage is applied to EL1 while EL4 is driven to V_{MID_TX}.
0x2	H-Bridge Drive. EL1 and EL4 are alternately switched between AVDD and AGND.

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BIOZ_DRV_MODE[1:0]	DRIVE TYPE
0x3	Standby. The transmit channel is reset and held in a low-power state, driving the electrodes to V_{MID_TX}.

BioZ Configuration 4 (0x23)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	BIOZ_FAST_MANUAL	BIOZ_FAST_START_EN
Reset	–	–	–	–	–	–	0	0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BIOZ_FAST_MANUAL

Together with BIOZ_FAST_START_EN, BIOZ_FAST_MANUAL is used to turn on the fast-start mode manually. The fast-start mode is kept until the register BIOZ_FAST_MANUAL is set back to 0. See BIOZ_FAST_START_EN.

BIOZ_FAST_START_EN

BIOZ_FAST_START_EN enables the fast-start mode, which connects the BIP and BIN inputs to V_{MID_RX} through 10kΩ resistors after enabling the I or Q channel. This quickly establishes a DC bias on the input electrodes.

Normally, the fast-start mode is turned on at the very beginning when BioZ is enabled. The turn-on time is about ~200ms, which is automatically set.

However, the fast mode can also be kept manually by programming the value of register BIOZ_FAST_MANUAL.

Three cases are listed as follows:

1. When BIOZ_FAST_START_EN is set to 0, fast-start is disabled.
2. When BIOZ_FAST_START_EN is set to 1 and BIOZ_FAST_MANUAL is set to 0, fast-start is enabled automatically for 200ms at the very beginning when BIOZ_E_EN or BIOZ_Q_EN are enabled.
3. When BIOZ_FAST_START_EN is set to 1 and BIOZ_FAST_MANUAL is set to 1, fast-start is kept enabled until BIOZ_FAST_MANUAL is set to 0.

BIOZ_FAST_START_EN	BIOZ_FAST_MANUAL	DECODE
0	x	Fast start is disabled
1	0	Fast start is enabled for approximately 200ms after BioZ is enabled.
1	1	Fast start is enabled until BIOZ_FAST_MANUAL is set to 0.

BioZ Configuration 5 (0x24)

BIT	7	6	5	4	3	2	1	0
Field	BIOZ_AHPF[3:0]				BIOZ_INA_MODE	BIOZ_DM_DIS	BIOZ_GAIN[1:0]	
Reset	0x0				0	0	0x0	
Access Type	Write, Read				Write, Read	Write, Read	Write, Read	

BIOZ_AHPF

BIOZ_AHPF sets the corner frequency of the internal analog high-pass filter, or sets the filter resistance when using external capacitors on BIP and BIN. The resistance is center tapped with the midpoint connected to V_{MID_RX}. When using external capacitors, the analog HPF corner frequency is set by the series capacitance and the selected common-mode resistance according to the following equation:

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- $f_{-3dB} = 1/(2 \times \pi \times R_{AHPF} \times C_{SERIES})$

where C_{SERIES} is the series combination of the external capacitors on BIP and BIN:

- $C_{SERIES} = (C_{BIP} \times C_{BIN}) / (C_{BIP} + C_{BIN})$

BIOZ_AHPF[3:0]	DECODE
0x0	100Hz
0x1	200Hz
0x2	500Hz
0x3	1,000Hz
0x4	2,000Hz
0x5	5,000Hz
0x6	10,000Hz
0x7	Resistor opened, internal capacitors shorted (AHPF bypassed)
0x8	42.4MΩ, internal capacitors shorted
0x9	21.2MΩ, internal capacitors shorted
0xA	8.4MΩ, internal capacitors shorted
0xB	4.2MΩ, internal capacitors shorted
0xC	2.2MΩ, internal capacitors shorted
0xD	848kΩ, internal capacitors shorted
0xE	848kΩ, internal capacitors shorted
0xF	Resistor opened, internal capacitor shorted (AHPF bypassed)

BIOZ_INA_MODE

BIOZ_INA_MODE sets BioZ receive channel's Instrumentation Amplifier (INA) power mode.

BIOZ_INA_MODE	DECODE
0	BioZ INA is in high power mode (low noise mode)
1	BioZ INA is in low power mode

BIOZ_DM_DIS

BIOZ_DM_DIS disables the BioZ receive channel demodulators to allow a direct conversion of the differential input voltage across BIP and BIN.

BIOZ_DM_DIS	DECODE
0	BioZ demodulation clock enabled
1	BioZ demodulation clock disabled

BIOZ_GAIN

BIOZ_GAIN sets the combined gain of the BioZ receive channel's INA and PGAs.

BIOZ_GAIN[1:0]	TOTAL GAIN (V/V)	INA GAIN (V/V)	PGA GAIN (V/V)
0x0	1	1	1
0x1	2	2	1
0x2	5	2	2.5
0x3	10	2	5

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BioZ Configuration 6 (0x25)

BIT	7	6	5	4	3	2	1	0
Field	BIOZ_EXT_CAP	BIOZ_DC_RESTORE	BIOZ_DRV_RESET	BIOZ_DAC_RESET	BIOZ_AMP_RGE[1:0]		BIOZ_AMP_BW[1:0]	
Reset	1	0	0	0	0x0		0x0	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read	

BIOZ_EXT_CAP

BIOZ_EXT_CAP selects the external capacitor C_{EXT} connected between DRVXC and DRVSJ, which AC-couples the stimulus current in the current mode, thus preventing DC current from passing into the patient stimulus electrodes. When not using an external capacitor, short DRVXC and DRVSJ.

BIOZ_EXT_CAP	DECODE
0	No external capacitor used. The internal switch shorts the DRVXC and DRVSJ pins together with a drain to source resistance of approximately 100Ω.
1	External capacitor used. The internal switch is open, and AC current is coupled through the external capacitor.

BIOZ_DC_RESTORE

BIOZ_DC_RESTORE closes the DC_RESTORE switch in the current-generator amplifier circuit, which applies a feedback resistance of approximately 10MΩ

to the current-drive amplifier. This maintains the DC bias of the drive electrodes during a lead-off event, which reduces the amplifier setting time when the lead is reconnected.

When using external AC-coupling capacitors on the pins assigned to DRVP or DRVN, set DC_RESTORE to 1 to absorb any DC offset currents and prevent amplifier saturation.

BIOZ_DC_RESTORE	DECODE
0	DC_RESTORE switch is open. No feedback resistance is applied to the current drive amplifier.
1	DC_RESTORE switch is closed. A 10MΩ feedback resistance is applied to the current-drive amplifier.

BIOZ_DRV_RESET

BIOZ_DRV_RESET places the BioZ transmit channel in a reset state by disabling the DDS DAC and closing the RESET switch of the current-drive amplifier. This shorts the feedback network of the amplifier, configuring it as a unity gain buffer and driving both drive electrodes to V_{MID_TX}.

BIOZ_DRV_RESET	DECODE
0	Normal Operation. The RESET switch is open.
1	Reset Condition. The DDC DAC is disabled and the RESET switch is closed, shorting the current drive amplifier feedback.

BIOZ_DAC_RESET

BIOZ_DAC_RESET forces the DDS DAC output to zero. The human body load is driven by the reference voltage V_{MID_TX}, and the AC current going through the human body load is zero.

BIOZ_AMP_RGE

BIOZ_AMP_RGE selects the output stage option for the voltage-drive amplifier and current-drive amplifier within the BioZ transmit channel. Higher strength is recommended for higher output current loading. Higher settings increase supply-current consumption.

Match these settings with the BIOZ_IDRV_RGE setting.

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BIOZ_AMP_RGE[1:0]	BIOZ AMPLIFIER RANGE
0x0	Low
0x1	Medium-Low
0x2	Medium-High
0x3	High

BIOZ_AMP_BW

BIOZ_DRV_BW sets the gain bandwidth of the voltage-drive amplifier and current-drive amplifier within the BioZ transmit channel. Higher bandwidth is recommended for high-frequency applications including Bioimpedance Analysis and Impedance Cardiography. Low bandwidth is recommended for low-frequency applications including Galvanic Skin Response to reduce power consumption.

BIOZ_AMP_BW[1:0]	BIOZ AMPLIFIER BANDWIDTH
0x0	Low
0x1	Medium-Low
0x2	Medium-High
0x3	High

BIOZ Low Threshold (0x26)

BIT	7	6	5	4	3	2	1	0
Field	BIOZ_LO_THRESH[7:0]							
Reset	0x00							
Access Type	Write, Read							

BIOZ_LO_THRESH

BIOZ_LO_THRESH sets the BioZ under-range threshold.

If the BioZ measurement selected by BIOZ_CMP is within the symmetric thresholds defined by ±32 x BIOZ_LO_THRESH for longer than approximately 128ms, the BIOZ_UNDR status bit is asserted.

BIOZ High Threshold (0x27)

BIT	7	6	5	4	3	2	1	0
Field	BIOZ_HI_THRESH[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BIOZ_HI_THRESH

BIOZ_HI_THRESH sets the BioZ over-range threshold.

If the BioZ measurement selected by BIOZ_CMP is outside of the symmetric thresholds defined by ±2048 x BIOZ_HI_THRESH for longer than approximately 128ms, the BIOZ_OVER status bit is asserted.

The default value (BIOZ_HI_THRESH= 0xFF) corresponds to a BioZ output upper threshold of 0x7F800, or about 99.6% of the full-scale range.

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BioZ Configuration 7 (0x28)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	BIOZ_STBYON	BIOZ_Q_CLK_PHASE	BIOZ_I_CLK_PHASE	BIOZ_INA_CHOP_EN	BIOZ_CH_FSEL
Reset	–	–	–	0	0	0	0	0
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BIOZ_STBYON

BIOZ_STBYON selects the BioZ receive channel's behavior when the transmit channel is in standby mode (BIOZ_DRV_MODE = 0x3). When in standby mode, the transmit channel does not generate a stimulus. So, the receive channel can be powered down in most cases.

BIOZ_STBYON	RECEIVE CHANNEL BEHAVIOR IN STANDBY MODE
0	Disabled. The receive channel's amplifiers, demodulators, and ADCs are disabled.
1	Enabled. The BioZ receive channel's amplifiers, demodulators, and ADCs remain enabled.

BIOZ_Q_CLK_PHASE

BIOZ_Q_CLK_PHASE controls the phase of the Q channel's demodulator. Changing the phase of the demodulator can be used to compare the I and Q channel gains.

BIOZ_Q_CLK_PHASE	DECODE
0	Normal Operation. The Q channel demodulator's clock is in quadrature phase to the stimulus signal.
1	I Phase. The Q channel demodulator's clock is in phase with the stimulus signal.

BIOZ_I_CLK_PHASE

BIOZ_I_CLK_PHASE controls the phase of the I channel's demodulator. Changing the phase of the demodulator can be used to compare the I and Q channel gains.

BIOZ_I_CLK_PHASE	DECODE
0	Normal Operation. The I channel demodulator's clock is in phase to the stimulus signal.
1	Q Phase. The I channel demodulator's clock is in quadrature phase with the stimulus signal.

BIOZ_INA_CHOP_EN

BIOZ_INA_CHOP_EN enables chopping in the BioZ receive channel's instrumentation amplifier. The chopping frequency is BIOZ_ADC_CLK / 2. INA chopping is recommended except when F_BIOZ = BIOZ_ADC_CLK / 2.

BIOZ_INA_CHOP_EN	DECODE
0	BIOZ_ADC_CLK / 2 chopping disabled
1	BIOZ_ADC_CLK / 2 chopping enabled

BIOZ_CH_FSEL

BIOZ_CH_FSEL selects the chopping frequency of the BioZ receive channel PGA and AAF.

Set to 1 if the F_BIOZ is equal to BIOZ_ADC_CLK

/ 8. Otherwise, set to 0.Note: The synthesis frequency must not equal the PGA chopping frequency or the correlator does not work. Use BIOZ_CH_FSEL to ensure they are not equal.

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BIOZ_CH_FSEL	DECODE
0	BioZ PGA chopping frequency is $f_{BIOZ_ADC_CLK}$ / 8
1	BioZ PGA chopping frequency is $f_{BIOZ_ADC_CLK}$ / 4

BioZ Mux Configuration 1 (0x41)

BIT	7	6	5	4	3	2	1	0
Field	BMUX_RSEL[1:0]		BMUX_BIST_EN	–	–	CONNECT_CAL_ONLY	MUX_EN	CAL_EN
Reset	0x0		0	–	–	0	0	0
Access Type	Write, Read		Write, Read	–	–	Write, Read	Write, Read	Write, Read

BMUX_RSEL

BMUX_RSEL selects the value of the resistive calibration load applied across DRVP/BIP and DRVN/BIN for non-GSR applications. This load is only applied when BMUX_BIST_EN = 1. The resistor error is measured during factory test, and the error value is saved in BIST_R_ERR[7:0](0x44).

BMUX_RSEL[1:0]	CALIBRATION RESISTANCE (Ω)
0x0	5100
0x1	900
0x2	600
0x3	280

BMUX_BIST_EN

BMUX_BIST_EN enables the built-in self-test resistor between DRVP/BIP and DRVN/BIN for non-GSR applications. To avoid external interference, disable both MUX_EN and CAL_EN when using BMUX_BIST_EN. The resistive value is selected by BMUX_RSEL.

BMUX_BIST_EN	DECODE
0	Disabled. The internal resistive load is disconnected.
1	Enabled. The internal resistive load is connected between DRVP and BIP, and DRVN and BIN.

CONNECT_CAL_ONLY

When both MUX_EN and CAL_EN are set to 1, enabling CONNECT_CAL_ONLY connects only the CAL1 to CAL4 pins, and disconnects the ELx pins. See MUX_EN for details.

CAL	CONNECT_CAL_ONLY	Use Case
0	0	EL1-EL4 connected only
0	1	EL1-EL4 connected only
1	0	CAL + EL1-EL4 connected
1	1	CAL connected only

MUX_EN

MUX_EN enables the BioZ input/output MUX connections to the ELx pins and/or CALx pins selected by DRVP_ASSIGN, DRVN_ASSIGN, BIP_ASSIGN, BIN_ASSIGN, CAL_EN, and CONNECT_CAL_ONLY.

MUX_EN	CAL_EN	CONNECT_CAL_ONLY	DECODE
0	X	X	MUX Disabled. All ELx and CALx pins are disconnected.

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MUX_EN	CAL_EN	CONNECT_CAL_ONLY	DECODE
1	0	X	ELx pins are connected according to BIP_ASSIGN, BIN_ASSIGN, DRVP_ASSIGN, and DRVN_ASSIGN. CALx pins are disconnected.
1	1	0	ELx pins are connected according to BIP_ASSIGN, BIN_ASSIGN, DRVP_ASSIGN, and DRVN_ASSIGN. CALx pins are also connected.
1	1	1	ELx pins are disconnected. CALx pins are connected only.

CAL_EN

CAL_EN connects the calibration pins (CAL1 to CAL4) of the BioZ input/output MUX to measure the external calibration resistor when MUX_EN = 1. See MUX_EN for details.

CAL_EN	DECODE
0	Calibration pins are disconnected.
1	Calibration pins are connected. CAL1 = DRVP, CAL2 = BIP, CAL3 = BIN, and CAL4 = DRVN. Electrode pins E1, E2A, E2B, E3A, E3B, and E4 are disconnected.

BioZ Mux Configuration 2 (0x42)

BIT	7	6	5	4	3	2	1	0
Field	BMUX_GSR_RSEL[1:0]		GSR_LOAD_EN	–	–	–	EN_EXT_INLOAD	EN_INT_INLOAD
Reset	0x0		0	–	–	–	0	0
Access Type	Write, Read		Write, Read	–	–	–	Write, Read	Write, Read

BMUX_GSR_RSEL

BMUX_GSR_RSEL selects the value of the resistive calibration load applied across DRVP/BIP and DRVN/BIN for GSR applications. This load is only applied when GSR_LOAD_EN = 1.

BMUX_GSR_RSEL[1:0]	LOAD RESISTANCE (kΩ)
0x0	25.7
0x1	101
0x2	505
0x3	1000

GSR_LOAD_EN

GSR_LOAD_EN enables the built in GSR load resistor between DRVP/BIP and DRVN/BIN. To avoid external interference, disable both MUX_EN and CAL_EN when using GSR_LOAD_EN. The resistive value is selected by BMUX_GSR_RSEL.

GSR_LOAD_EN	DECODE
0	Disabled. The internal resistive load is disconnected.
1	Enabled. The internal resistive load is connected between DRVP and BIP, and DRVN and BIN.

EN_EXT_INLOAD

EN_EXT_INLOAD enables the external guard-trace-drive circuit, which outputs the buffered voltage from BIP and BIN onto the EL2A and EL3A pins.

EN_EXT_INLOAD	DECODE
0	External guard-drive circuit disabled.
1	External guard-drive circuit enabled.

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EN_INT_INLOAD

EN_INT_INLOAD enables the circuit that compensates for input capacitive loading on BIN and BIP.

EN_INT_INLOAD	DECODE
0	Input capacitive loading compensation circuit disabled.
1	Input capacitive loading compensation circuit enabled.

BioZ Mux Configuration 3 (0x43)

BIT	7	6	5	4	3	2	1	0
Field	BIP_ASSIGN[1:0]		BIN_ASSIGN[1:0]		DRVP_ASSIGN[1:0]		DRVN_ASSIGN[1:0]	
Reset	0x0		0x0		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BIP_ASSIGN

BIP_ASSIGN selects the electrode pin used for the BioZ positive input (BIP) when MUX_EN = 1. When CAL_EN = 1, this selection is ignored and the electrode pins are disconnected.

BIP_ASSIGN[1:0]	ASSIGNED ELECTRODE PIN
0x0	EL1
0x1	EL2A
0x2	EL2B
0x3	Do not use.

BIN_ASSIGN

BIN_ASSIGN selects the electrode pin used for the BioZ negative input (BIN) when MUX_EN = 1. When CAL_EN = 1, this selection is ignored and the electrode pins are disconnected.

BIN_ASSIGN[1:0]	ASSIGNED ELECTRODE PIN
0x0	EL4
0x1	EL3A
0x2	EL3B
0x3	Do not use.

DRVP_ASSIGN

DRVP_ASSIGN selects the electrode pin used for the BioZ positive drive (DRVP) in the current mode when MUX_EN = 1. When CAL_EN = 1, this selection is ignored and the electrode pins are disconnected.

In voltage or H-bridge mode, the BioZ positive drive only connects to EL1.

The EL1 MUX switch has lower on-resistance than EL2A and EL2B. So, assign DRVP to EL1 when using currents or 64µA or greater.

BIOZ_DRV_MODE[1:0]	DRVP_ASSIGN[1:0]	ASSIGNED ELECTRODE PIN
0x0 or 0x3	0x0	EL1 (low resistance)
0x0 or 0x3	0x1	EL2A
0x0 or 0x3	0x2	EL2B
0x0 or 0x3	0x3	Do not use.
0x1	X	EL1
0x2	X	EL1

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DRVN_ASSIGN

DRVN_ASSIGN selects the electrode pin used for the BioZ negative drive (DRVN) in the current mode when MUX_EN = 1. When CAL_EN = 1, this selection is ignored and the electrode pins are disconnected.

In voltage or H-bridge mode, the BioZ negative drive only connects to EL4.

The EL4 MUX switch has lower on-resistance than EL3A and EL3B. So, assign DRVN to EL4 when using currents or 64µA or greater.

BIOZ_DRV_MODE[1:0]	DRVN_ASSIGN[1:0]	ASSIGNED ELECTRODE PIN
0x0 or 0x3	0x0	EL4 (low resistance)
0x0 or 0x3	0x1	EL3A
0x0 or 0x3	0x2	EL3B
0x0 or 0x3	0x3	Do not use.
0x1	X	EL4
0x2	X	EL4

BioZ Mux Configuration 4 (0x44)

BIT	7	6	5	4	3	2	1	0
Field	BIST_R_ERR[7:0]							
Reset	0x00							
Access Type	Read Only							

BIST_R_ERR

The on-chip Built-In Self-Test (BIST) resistors are available to calibrate the BioZ channel magnitude/phase error. 5.1kΩ, 900Ω, 600Ω, or 280Ω of resistors can be chosen by BMUX_RSEL. Due to process variations, the actual resistances vary by up to ±25%. During factory test, the actual resistance of the 600Ω resistor is measured with an accuracy of ±1.5%, and the error stored in the BIST_R_ERR field. The actual resistance (to within ±1.5%) can be calculated with the following equation, where BIST_R_ERR is a 2's complement representation. The other values (5.1kΩ, 900Ω, and 280Ω) are process-matched to the 600Ω resistor with approximately 2% precision.

$R_{ACTUAL} = R_{NOMINAL}$ x (1 + BIST_R_ERR / 512)

For example, when BIST_R_ERR = 64 and BMUX_RSEL = 0x2, R_{ACTUAL} = 600Ω x (1 + 64 / 512) = 675Ω ±1.5%.

BIST_R_ERR is a read-only register.

DC Leads Configuration (0x50)

BIT	7	6	5	4	3	2	1	0
Field	EN_LON_DET	EN_LOFF_DET	EN_EXT_LOFF	EN_DRV_OOR	LOFF_IPOL	LOFF_IMAG[2:0]		
Reset	0	0	0	0	0	0x0		
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		

EN_LON_DET

EN_LOT_DET enables Ultra-Low-Power (ULP) DC lead-on detection on the BIP and BIN inputs. ULP mode only functions when BioZ is not enabled (BIOZ_I_EN = BIOZ_Q_EN = 0).

EN_LON_DET	DECODE
0	ULP lead-on detection is disabled.

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EN_LON_DET	DECODE
1	ULP lead-on detection is enabled.

EN_LOFF_DET

EN_LOFF_DET enables DC lead-off detection on the BIP and BIN inputs, and only functions when BioZ is enabled (BIOZ_I_EN or BIOZ_Q_EN = 1). When enabled, the lead-off status is reported by the DC_LOFF_PH, DC_LOFF_PL, DC_LOFF_NH, and DC_LOFF_NL status bits and interrupts.

EN_LOFF_DET	DECODE
0	BioZ DC lead-off detection is disabled.
1	BioZ DC lead-off detection is enabled.

EN_EXT_LOFF

EN_EXT_LOFF enables DC lead-off detection on the EL2B and EL3B pins when the EL2A and EL3A pins are being used as AC-coupled BioZ inputs. EL2B and EL3B must be connected externally to the electrode side of the AC-coupling capacitors for this feature to function.

EN_EXT_LOFF	DECODE
0	DC lead-off detection is applied to the internal BIP and BIN nodes.
1	DC lead-off detection is applied externally through EL2B and EL3B for AC-coupled applications.

EN_DRV_OOR

EN_DRV_OOR enables the voltage monitor on DRVN to detect drive electrode lead-off conditions. If the total impedance between DRVP and DRVN is high, due to either the DRVP or DRVN electrode being disconnected, the AC voltage at DRVN is large, and triggers a DRV_OOR status and interrupt.

EN_DRV_OOR	DECODE
0	Drive voltage out-of-range detection is disabled.
1	Drive voltage out-of-range detection is enabled.

LOFF_IPOL

LOFF_IPOL sets the polarity of the matched DC current sources used for DC lead-off detection.

LOFF_IPOL	LEAD-OFF CURRENT POLARITY
0	Non-inverted. BIP sources current, BIN sinks current.
1	Inverted. BIP sinks current, BIN sources current.

LOFF_IMAG

LOFF_IMAG selects the DC lead-off current amplitude.

LOFF_IMAG[2:0]	DC CURRENT MAGNITUDE (nA)
0x0	0 (Current sources disabled)
0x1	5
0x2	10
0x3	20
0x4	50
0x5	100
0x6	100
0x7	100

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DC Lead Detect Threshold (0x51)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	LOFF_THRESH[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

LOFF_THRESH

LOFF_THRESH selects the voltage threshold for the DC lead-off window comparators, which are centered at V_{MID_RX}. If the voltage of either BIP or BIN goes above the high threshold or below the low threshold for approximately 128ms, the corresponding DC_LOFF status bit is set to 1 in register 0x01. If LOFF_RAPID = 1, the 128ms delay is bypassed and the status asserts immediately.

LOFF_THRESH[3:0]	DC LEAD-OFF THRESHOLD
0x0	V_{MID_RX} ± 215mV
0x1	V_{MID_RX} ± 245mV
0x2	V_{MID_RX} ± 275mV
0x3	V_{MID_RX} ± 305mV
0x4	V_{MID_RX} ± 335mV
0x5	V_{MID_RX} ± 365mV
0x6	V_{MID_RX} ± 395mV
0x7	V_{MID_RX} ± 425mV
0x8	V_{MID_RX} ± 455mV
0x9	V_{MID_RX} ± 485mV
0xA	V_{MID_RX} ± 515mV
0xB	V_{MID_RX} ± 545mV
0xC	V_{MID_RX} ± 575mV
0xD	V_{MID_RX} ± 605mV
0xE	V_{MID_RX} ± 635mV
0xF	V_{MID_RX} ± 665mV

Lead Bias Configuration 1 (0x58)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	RBIAS_VALUE[1:0]		EN_RBIAS_BIP	EN_RBIAS_BIN
Reset	–	–	–	–	0x0		0	0
Access Type	–	–	–	–	Write, Read		Write, Read	Write, Read

RBIAS_VALUE

RBIAS_VALUE selects the BioZ input lead bias resistance, which is between BIP and V_{MID_RX} (EN_RBIAS_BIP = 1), and BIN and V_{MID_RX} (EN_RBIAS_BIN = 1).

RBIAS_VALUE[1:0]	BIAS RESISTANCE (MΩ)
0x0	50
0x1	100

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0x2	200
0x3	Do not use.

EN_RBIAS_BIP

EN_RBIAS_BIP enables lead bias on BIP. The resistor connecting BIP to V_{MID_RX} is selected in RBIAS_VALUE.

EN_RBIAS_BIP	DECODE
0	BIP is not resistively connected to V_{MID_RX}.
1	BIP is connected to V_{MID_RX} through a resistor (selected by RBIAS_VALUE).

EN_RBIAS_BIN

EN_RBIAS_BIN enables lead bias on BIN. The resistor connecting BIN to V_{MID_RX} is selected in RBIAS_VALUE.

EN_RBIAS_BIN	DECODE
0	BIN is not resistively connected to V_{MID_RX}.
1	BIN is connected to V_{MID_RX} through a resistor (selected by RBIAS_VALUE).

Interrupt Enable 1 (0x80)

BIT	7	6	5	4	3	2	1	0
Field	A_FULL_EN	–	FIFO_DATA_RDY_EN	FREQ_UNLOCK_EN	FREQ_LOCK_EN	PHASE_UNLOCK_EN	PHASE_LOCK_EN	–
Reset	0	–	0	0	0	0	0	–
Access Type	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–

A_FULL_EN

Enables the A_FULL[7](0x00) status bit to be output to the INT output pin.

FIFO_DATA_RDY_EN

Enables the FIFO_DATA_RDY[5](0x00) status bit to be output to the INT output pin.

FREQ_UNLOCK_EN

Enables the FREQ_UNLOCK[4](0x00) status bit to be output to the INT output pin.

FREQ_LOCK_EN

Enables the FREQ_LOCK[3](0x00) status bit to be output to the INT output pin.

PHASE_UNLOCK_EN

Enables the PHASE_UNLOCK[2](0x00) status bit to be output to the INT output pin.

PHASE_LOCK_EN

Enables the PHASE_LOCK[1](0x00) status bit to be output to the INT output pin.

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Interrupt Enable 2 (0x81)

BIT	7	6	5	4	3	2	1	0
Field	LON_EN	BIOZ_OVER_EN	BIOZ_UNDR_EN	DRV_OOR_EN	DC_LOFF_PH_EN	DC_LOFF_PL_EN	DC_LOFF_NH_EN	DC_LOFF_NL_EN
Reset	0	0	0	0	0	0	0	0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

LON_EN

Enables the LON[7](0x01) status bit to be output to the INT output pin.

BIOZ_OVER_EN

Enables the BIOZ_OVER[6](0x01) status bit to be output to the INT output pin.

BIOZ_UNDR_EN

Enables the BIOZ_UNDR[5](0x01) status bit to be output to the INT output pin.

DRV_OOR_EN

Enables the DRV_OOR[4](0x01) status bit to be output to the INT output pin.

DC_LOFF_PH_EN

Enables the DC_LOFF_PH[3](0x01) status bit to be output to the INT output pin.

DC_LOFF_PL_EN

Enables the DC_LOFF_PL[2](0x01) status bit to be output to the INT output pin.

DC_LOFF_NH_EN

Enables the DC_LOFF_NH[1](0x01) status bit to be output to the INT output pin.

DC_LOFF_NL_EN

Enables the DC_LOFF_NL[0](0x01) status bit to be output to the INT output pin.

Part ID (0xFF)

BIT	7	6	5	4	3	2	1	0
Field	PART_ID[7:0]							
Reset	0x42							
Access Type	Read Only							

PART_ID

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Applications Information

Patient Safety

Whenever applying a voltage or current to a human body, patient safety must be the top priority. According to IEC 60601-1, the maximum allowable AC patient auxiliary current under normal condition is 100µA at low frequencies such as 50Hz or 60Hz. As frequency increases, the allowable current also increases. The end application designers are always responsible to ensure patient safety, and the MAX30009 does not guarantee that stimulus signals comply with IEC 60601-1.

To facilitate patient safety in the current-drive mode, the MAX30009 limits the drive current setting according to the stimulus frequency as shown in Table 10. If the host controller writes a value outside of the allowed range to either the frequency divider or the current magnitude register fields, BIOZ_VDRV_MAG[5:4](0x22) and BIOZ_IDRV_RGE[3:2](0x22) are automatically overwritten to the maximum allowed setting. To enable high-frequency, high-current stimulus, the host controller must first set f_{STIM} and then set I_{MAG}. If the application uses the optional R_{EXT} to set the current magnitude, this lockout feature does not apply.

Table 10. Allowed Current Magnitudes vs. Frequency

FREQUENCY RANGE (Hz)	MAXIMUM CURRENT (µA)
<512	64
≥512	128
≥2048	256
≥8192	640
≥16384	1280

In the voltage or H-bridge drive mode, the MAX30009 does not limit the patient current, and compliance must be achieved with external current-limiting resistors between the drive electrodes, and the EL1 and EL4 pins. Choose the resistance to limit the current to V_{MAG} / (2 x R_{SERIES}) if the electrode and body impedances are very small. In the H-bridge mode, V_{MAG} is equal to AVDD.

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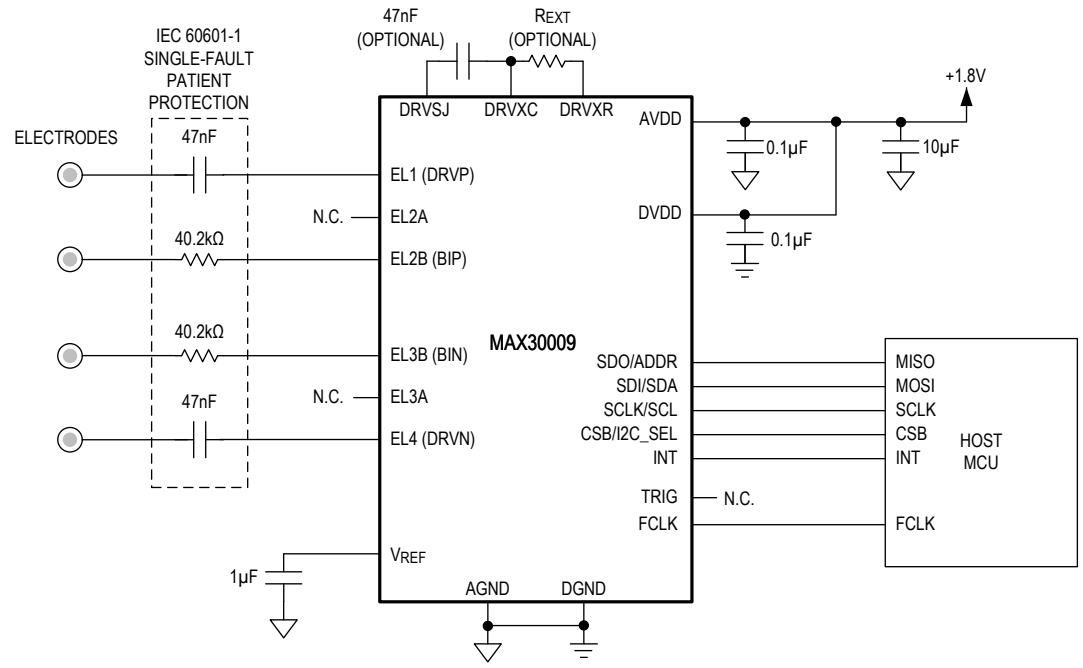
Typical Application Circuits

4-Electrode Device Supporting BIA/BIS, Respiration, or ICG



NOTES:

- FOR IEC 60601-1 SINGLE FAULT PATIENT SAFETY COMPLIANCE, EACH ELECTRODE PIN SHOULD HAVE A SERIES RESISTOR OR CAPACITOR TO LIMIT DC CURRENT INTO THE ELECTRODE IN THE CASE OF A SHORT OF THE ELx PIN TO A NEARBY POWER SUPPLY VOLTAGE OR GND. TO LIMIT THE DC CURRENT TO 50µA, THE SERIES RESISTANCE SHOULD BE ≥ (V_{SUPPLY} / 50µA), WHERE V_{SUPPLY} IS THE HIGHEST NEARBY VOLTAGE.
- THE DIGITAL INTERFACE IS SHOWN IN SPI CONFIGURATION. I^2C CONFIGURATION CAN BE SELECTED BY TYING CSB/I2C_SEL HIGH, TYING SDO/ADDR LOW OR HIGH, AND ADDING PULLUP RESISTORS TO SDI/SDA AND SCLK/SCL.
- THE INT OUTPUT IS SHOWN IN PUSH-PULL CONFIGURATION, WHICH IS PROGRAMMED BY INT_OCFG[3:2](0X13). FOR OPEN-DRAIN CONFIGURATION, ADD A PULLUP RESISTOR.

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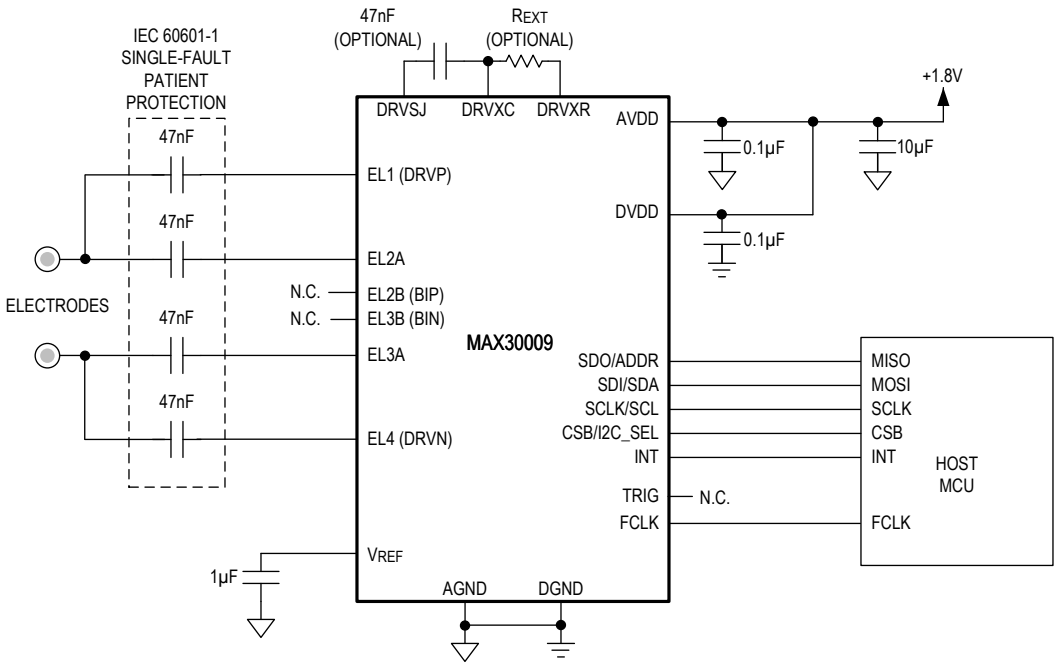
Typical Application Circuits (continued)

2-Electrode Device Supporting GSR/EDA



NOTES:

- FOR IEC 60601-1 SINGLE FAULT PATIENT SAFETY COMPLIANCE, EACH ELECTRODE PIN SHOULD HAVE A SERIES RESISTOR OR CAPACITOR TO LIMIT DC CURRENT INTO THE ELECTRODE IN THE CASE OF A SHORT OF THE ELx PIN TO A NEARBY POWER SUPPLY VOLTAGE OR GND. TO LIMIT THE DC CURRENT TO 50µA, THE SERIES RESISTANCE SHOULD BE ≥ (V_{SUPPLY} / 50µA), WHERE V_{SUPPLY} IS THE HIGHEST NEARBY VOLTAGE.
- THE DIGITAL INTERFACE IS SHOWN IN SPI CONFIGURATION. I^2C CONFIGURATION CAN BE SELECTED BY TYING CSB/I2C_SEL HIGH, TYING SDO/ADDR LOW OR HIGH, AND ADDING PULLUP RESISTORS TO SDI/SDA AND SCLK/SCL.
- THE INT OUTPUT IS SHOWN IN PUSH-PULL CONFIGURATION, WHICH IS PROGRAMMED BY INT_OCFG[3:2](0X13). FOR OPEN-DRAIN CONFIGURATION, ADD A PULLUP RESISTOR.

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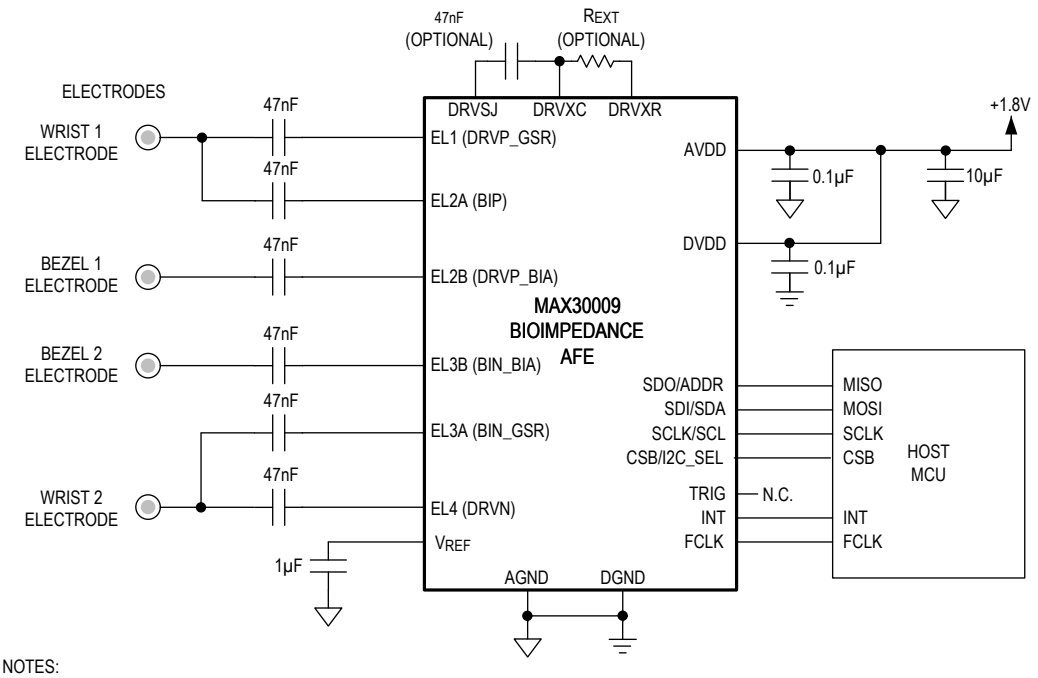
Typical Application Circuits (continued)

4-Electrode Wrist Device Supporting BIA and GSR



NOTES:

- FOR IEC 60601-1 SINGLE FAULT PATIENT SAFETY COMPLIANCE, EACH ELECTRODE PIN SHOULD HAVE A SERIES RESISTOR OR CAPACITOR TO LIMIT DC CURRENT INTO THE ELECTRODE IN THE CASE OF A SHORT OF THE ELx PIN TO A NEARBY POWER SUPPLY VOLTAGE OR GND. TO LIMIT THE DC CURRENT TO 50µA, THE SERIES RESISTANCE SHOULD BE ≥ (V_{SUPPLY} / 50µA), WHERE V_{SUPPLY} IS THE HIGHEST NEARBY VOLTAGE.
- THE DIGITAL INTERFACE IS SHOWN IN SPI CONFIGURATION. I^2C CONFIGURATION CAN BE SELECTED BY TYING CSB/I2C_SEL HIGH, TYING SDO/ADDR LOW OR HIGH, AND ADDING PULLUP RESISTORS TO SDI/SDA AND SCLK/SCL.
- THE INT OUTPUT IS SHOWN IN PUSH-PULL CONFIGURATION, WHICH IS PROGRAMMED BY INT_OCFG[3:2](0X13). FOR OPEN-DRAIN CONFIGURATION, ADD A PULLUP RESISTOR.

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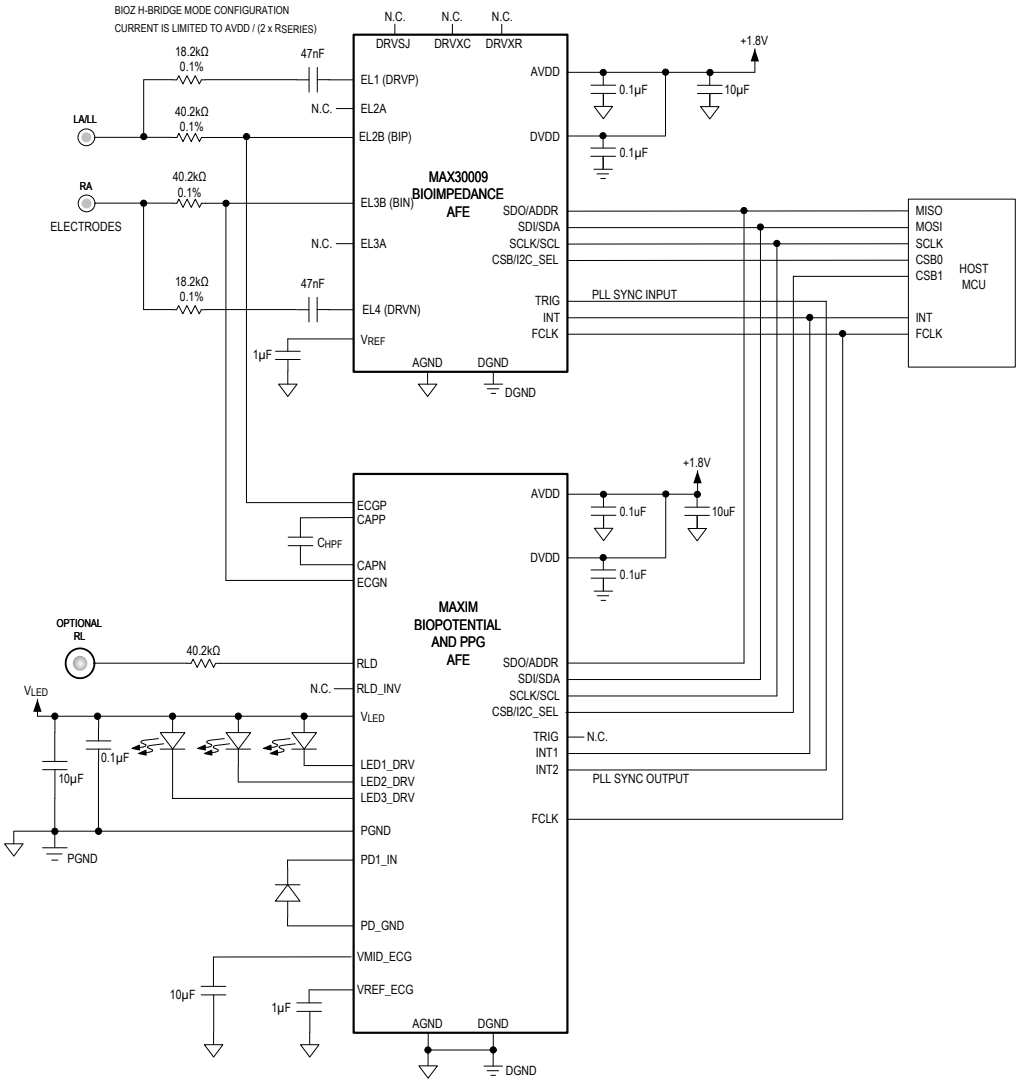
Typical Application Circuits (continued)

2-Electrode Chest Device Supporting Respiration with ECG and PPG



NOTES:

- FOR IEC 60601-1 SINGLE FAULT PATIENT SAFETY COMPLIANCE, EACH ELECTRODE PIN SHOULD HAVE A SERIES RESISTOR OR CAPACITOR TO LIMIT DC CURRENT INTO THE ELECTRODE IN THE CASE OF A SHORT OF THE ELx PIN TO A NEARBY POWER SUPPLY VOLTAGE OR GND. TO LIMIT THE DC CURRENT TO 50µA, THE SERIES RESISTANCE SHOULD BE ≥ (V_{SUPPLY} / 50µA), WHERE V_{SUPPLY} IS THE HIGHEST NEARBY VOLTAGE.
- THE DIGITAL INTERFACE IS SHOWN IN SPI CONFIGURATION. TO AVOID FALSE I^2C START CONDITIONS ON THE SHARED BUS, SET DISABLE_I2C[6](0X11) = 1. I^2C CONFIGURATION CAN BE SELECTED BY TYING CSB/I2C_SEL HIGH, TYING SDO/ADDR LOW OR HIGH, AND ADDING PULLUP RESISTORS TO SDI/SDA AND SCLK/SCL.
- THE INT OUTPUT IS SHOWN IN PUSH-PULL CONFIGURATION, WHICH IS PROGRAMMED BY INT_OCFG[3:2](0X13). FOR OPEN-DRAIN CONFIGURATION, ADD A PULLUP RESISTOR.

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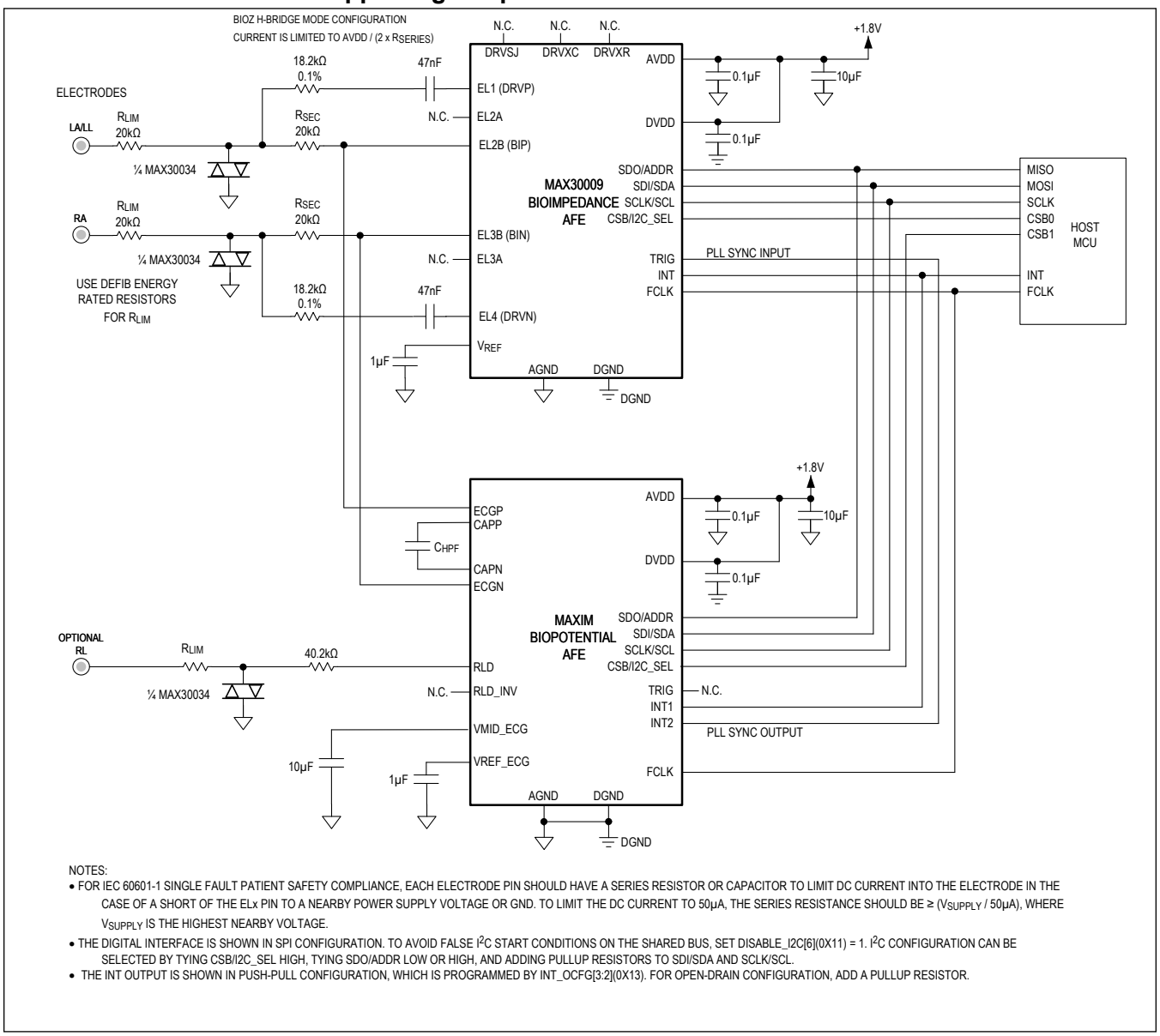
Typical Application Circuits (continued)

2-Electrode Chest Device Supporting Respiration with ECG and Defibrillation Protection



NOTES:

- FOR IEC 60601-1 SINGLE FAULT PATIENT SAFETY COMPLIANCE, EACH ELECTRODE PIN SHOULD HAVE A SERIES RESISTOR OR CAPACITOR TO LIMIT DC CURRENT INTO THE ELECTRODE IN THE CASE OF A SHORT OF THE ELx PIN TO A NEARBY POWER SUPPLY VOLTAGE OR GND. TO LIMIT THE DC CURRENT TO 50µA, THE SERIES RESISTANCE SHOULD BE ≥ (V_{SUPPLY} / 50µA), WHERE V_{SUPPLY} IS THE HIGHEST NEARBY VOLTAGE.
- THE DIGITAL INTERFACE IS SHOWN IN SPI CONFIGURATION. TO AVOID FALSE I^2C START CONDITIONS ON THE SHARED BUS, SET DISABLE_I2C[6](0X11) = 1. I^2C CONFIGURATION CAN BE SELECTED BY TYING CSB/I2C_SEL HIGH, TYING SDO/ADDR LOW OR HIGH, AND ADDING PULLUP RESISTORS TO SDI/SDA AND SCLK/SCL.
- THE INT OUTPUT IS SHOWN IN PUSH-PULL CONFIGURATION, WHICH IS PROGRAMMED BY INT_OCFG[3:2](0X13). FOR OPEN-DRAIN CONFIGURATION, ADD A PULLUP RESISTOR.

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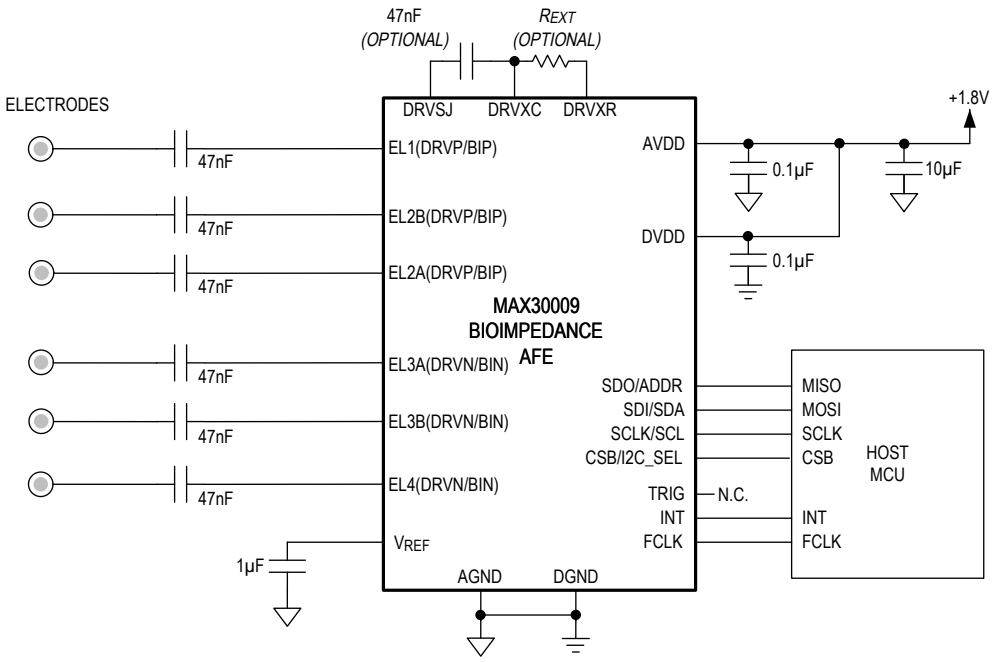
Typical Application Circuits (continued)

6-Electrode Device Supporting Multiple Measurement Vectors



NOTES:

- FOR IEC 60601-1 SINGLE FAULT PATIENT SAFETY COMPLIANCE, EACH ELECTRODE PIN SHOULD HAVE A SERIES RESISTOR OR CAPACITOR TO LIMIT DC CURRENT INTO THE ELECTRODE IN THE CASE OF A SHORT OF THE ELx PIN TO A NEARBY POWER SUPPLY VOLTAGE OR GND. TO LIMIT THE DC CURRENT TO 50µA, THE SERIES RESISTANCE SHOULD BE ≥ (V_{SUPPLY} / 50µA), WHERE V_{SUPPLY} IS THE HIGHEST NEARBY VOLTAGE.
- THE DIGITAL INTERFACE IS SHOWN IN SPI CONFIGURATION. I^2C CONFIGURATION CAN BE SELECTED BY TYING CSB/I2C_SEL HIGH, TYING SDO/ADDR LOW OR HIGH, AND ADDING PULLUP RESISTORS TO SDI/SDA AND SCLK/SCL.
- THE INT OUTPUT IS SHOWN IN PUSH-PULL CONFIGURATION, WHICH IS PROGRAMMED BY INT_OCFG[3:2](0X13). FOR OPEN-DRAIN CONFIGURATION, ADD A PULLUP RESISTOR.

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX30009ENA+	-40°C to +85°C	25 WLP
MAX30009ENA+T	-40°C to +85°C	25 WLP

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/21	Initial release	—
1	2/22	Updated *General Description*, *Simplified Block Diagram*, *I^2C Timing Characteristics*, *Pin Configuration*	1, 2, 14, 20

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