FlexCore® ARM7EJ-S™ 32-bit Processor Core with Java™ acceleration

OVERVIEW

LSI Logic offers FlexCore® ARM7EJ-S™ processor cores available on both our G*flx*™ 0.11 micron (drawn) and G12™ 0.18 micron (drawn) high performance process technologies, and configured to individual customer needs.

By choosing a FlexCore ARM7EJ-S processor core from LSI Logic, system-on-chip (SoC) designers can define their specific needs for target process technology, target ASIC libraries (high performance, high density or low leakage) and the number of metal routing layers required. Once the customer has decided on the optimal processor configuration, a design simulation model can be provided within a week, and complete CoreWare® deliverables within four weeks.

The ARM7EJ-S macrocell, licensed from ARM Limited, is an enhanced performance version of the extremely popular ARM7TDMI 32-bit RISC processor core family, delivering new levels of performance, functionality and flexibility to cost sensitive SoC applications requiring a compact but powerful processor. The high performance 32-bit RISC core includes Jazelle™ technology from ARM® for Java acceleration and also an enhanced 16 x 32-bit multiplier. The ARM7EJ-S core supports the ARMv5TEJ instruction set including 16-bit fixed point DSP instructions to enhance performance of many signal processing algorithms and applications. The ARMv5TEJ instruction set also includes the 16-bit Thumb instruction set and Java bytecode execution.

LSI Logic is a leading supplier of the most complex ASIC SoC solutions, with over 20 years in the industry and more than 20,000 ASIC designs behind us. Our extensive CoreWare® intellectual property (IP) offering includes a full range of ARM, MIPS® and ZSP™ DSP cores, a broad range of peripherals and application specific IP, reference designs, platforms, rapid prototyping support, and comprehensive design integration support.

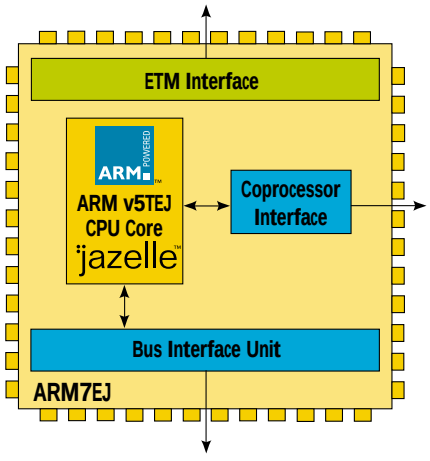
ASIC library	Process Technology (microns)	Max Clock Frequency (MHz)	Power Dissipation (mW/MHz) [2]
Gflx P (High performance)	0.11 drawn	167	0.25
Gflx D (High Density)	0.11 drawn	133	0.2
G12 P (High Performance)	0.18 drawn	125	1.0
G12 D (High Density)	0.18 drawn	100	0.55
G12 L (Low Leakage)	0.18 drawn	75	0.26

Example ARM7EJ-S FlexCore performance figures

FEATURES AND BENEFITS

- Up to 167 MHz performance available on LSI Logic's G*flx* 0.11 micron (drawn) process technology [1]
- Power dissipation as low as 0.2 mW/MHz (on G*flx* D process) [2]
- Available on both G*flx*™ 0.11 micron (drawn) and G12™ 0.18 micron (drawn) high performance process technologies
- High performance, low power, and high density versions available
- 32-bit processor core implementing the ARM, Thumb, DSP, and Java ISAs (v5TEJ)
- Small die size
- High code density
- Wide range of development tools available
- EmbeddedICE-RT logic for real-time debug

Notes:
[1] Worst case conditions
[2] Estimated



ARM7EJ-S Processor Core

FlexCore® ARM7EJ-S 32-bit Processor Core

FUNCTIONALITY

Performance

The ARM7EJ-S has a 5-stage pipeline to make it the highest performance member of the ARM7TDMI family, and delivers up to 175 MHz on LSI Logic's high performance G*flx* 0.11 micron (drawn) process technology. The ARM7EJ-S architecture is rated at 1.0 MIPS/MHz (Dhrystone 2.1). LSI Logic's FlexCore ARM7EJ-S processor cores include an AMBA 2.0 AHB bus interface as standard. The core is also available with a native ARM bus interface.

ARM's commitment to instruction set compatibility ensures that products designed with the ARM7EJ-S core have a clear roadmap to higher performance and optimal cost.

Thumb®

All ARM processors are native 32-bit designs, but also incorporate the 16-bit Thumb instruction set, which enables software to be coded as shorter 16-bit instructions. This provides typical memory savings of up to 35% over the equivalent 32-code, while retaining all the benefits of a 32-bit system such as access to a full 32-bit address space.

DSP Extensions

Many systems need the flexibility of a microcontroller combined with the data-processing capability of a DSP which historically has forced designers to compromise performance or cost, or adopt multiprocessor strategies. The inclusion of DSP instruction set extensions in the ARM7EJ-S offers enhanced 16-bit and 32-bit arithmetic capabilities, providing improved performance and flexibility.

Jazelle™ Technology

ARM's Jazelle technology provides Java acceleration to deliver significantly higher performance than a software-based Java Virtual Machine (JVM). The Jazelle technology-enabled core uses 87% less energy per CaffieneMark® than an equivalent non-accelerated core. This functionality provides platform developers the freedom to run Java code alongside established operating systems (OS) and applications, on a single processor.

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