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CY7C1020CV26

512-Kbit (32 K × 16) Static RAM

Features

- Temperature range
  - Automotive: –40 °C to 125 °C
- High speed
  - t_{AA} = 15 ns
- Optimized voltage range: 2.5 V to 2.7 V
- Automatic power down when deselected
- Independent control of upper and lower bits
- CMOS for optimum speed and power
- Package offered: 44-pin TSOP II

Functional Description

The CY7C1020CV26 is a high performance CMOS static RAM organized as 32,768 words by 16 bits. This device has an automatic power down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs LOW. If byte low enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_1 through I/O_8), is written into the location specified on the address pins (A_0 through A_{14}). If byte high enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_9 through I/O_{16}) is written into the location specified on the address pins (A_0 through A_{14}).

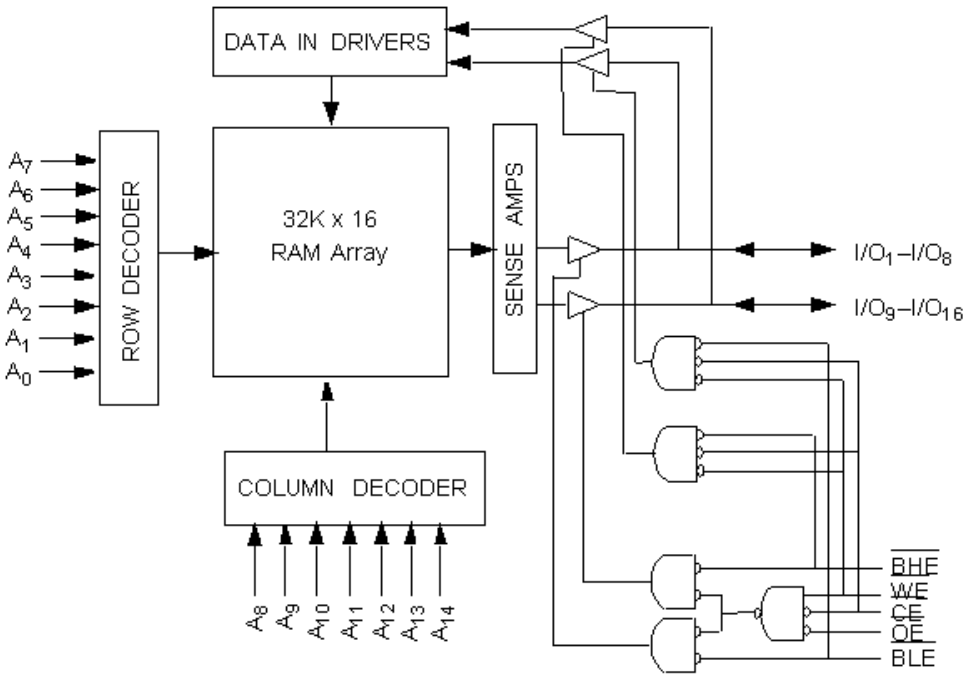
Reading from the device is accomplished by taking chip enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the write enable ($\overline{WE}$) HIGH. If byte low enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appears on I/O_1 to I/O_8. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O_9 to I/O_{16}. See the Truth Table on page 11 for a complete description of read and write modes.

The input/output pins (I/O_1 through I/O_{16}) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

The CY7C1020CV26 is available in a standard 44-pin TSOP Type II.

For a complete list of related documentation, click here.

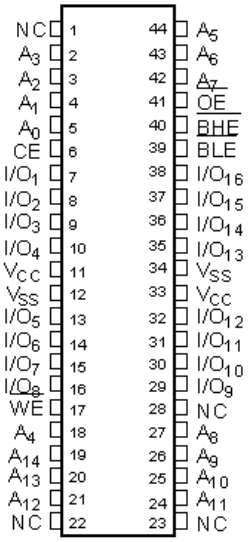
Logic Block Diagram



Contents

Pin Configuration

Figure 1. 44-pin TSOP II pinout (Top View)



Selection Guide

Description	CY7C1020CV26-15	Unit
Maximum access time	15	ns
Maximum operating current	100	mA
Maximum CMOS standby current	5	mA

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage on V_{CC} to relative GND[1] .....–0.5 V to +4.6 V

DC voltage applied to outputs in High-Z State[1] .....–0.5 V to V_{CC}+0.5 V

DC input voltage[1] .....–0.5 V to V_{CC}+0.5 V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage (per MIL-STD-883, Method 3015) .....> 2001 V

Latch up current .....> 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Automotive	–40 °C to +125 °C	2.5 V to 2.7 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	CY7C1020CV26		Unit
			Min	Max	
V_{OH}	Output HIGH voltage	V_{CC} = Minimum, I_{OH} = –1.0 mA	2.3	–	V
V_{OL}	Output LOW voltage	V_{CC} = Minimum, I_{OL} = 1.0 mA	–	0.4	V
V_{IH}	Input HIGH voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW voltage[1]		–0.3	0.8	V
I_{IX}	Input load current	GND ≤ V_I ≤ V_{CC}	–5	+5	µA
I_{OZ}	Output leakage current	GND ≤ V_I ≤ V_{CC}, Output Disabled	–5	+5	µA
I_{OS}[2]	Output short circuit current	V_{CC} = Maximum, V_{OUT} = GND	–	–300	mA
I_{CC}	V_{CC} operating supply current	V_{CC} = Maximum, I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	–	100	mA
I_{SB1}	Automatic CE power-down Current – TTL Inputs	Maximum V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	–	40	mA
I_{SB2}	Automatic CE power-down Current – CMOS Inputs	Maximum V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3 V, V_{IN} ≥ V_{CC} – 0.3 V, or V_{IN} ≤ 0.3 V, f = 0	–	5	mA

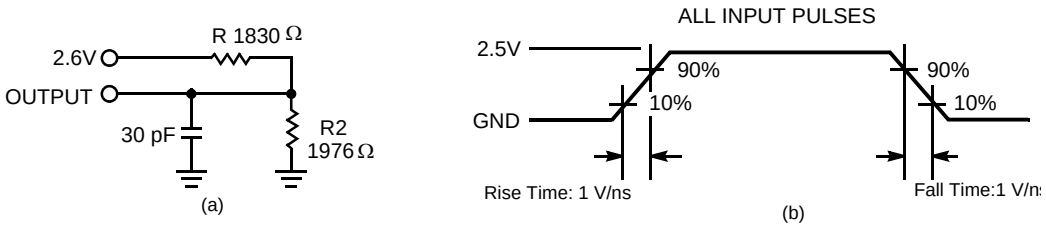
Notes
1. VIL (min.) = –2.0V for pulse durations of less than 20 ns.
2. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

Capacitance

Parameter [3]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 2.6 V	8	pF
C_{OUT}	Output capacitance		8	pF

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms [4]



Notes
3. Tested initially and after any design or process changes that may affect these parameters.
4. Test conditions assume signal transition time of 1V/ns or less, timing reference levels of 1.3 V, input pulse levels of 0 to 2.5 V and transmission line loads as in (a) of Figure 2.

AC Switching Characteristics

Over the Operating Range

Parameter	Description	CY7C1020CV26		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	15	–	ns
t_{AA}	Address to data valid	–	15	ns
t_{OHA}	Data hold from address change	3	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	15	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	7	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z[5]	0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z[5, 6]	–	7	ns
t_{LZCE}	$\overline{CE}$ LOW to low Z[5]	3	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to high Z[5, 6]	–	7	ns
t_{PU}[7]	$\overline{CE}$ LOW to power-up	0	–	ns
t_{PD}[7]	$\overline{CE}$ HIGH to power-down	–	15	ns
t_{DBE}	Byte enable to data valid	–	7	ns
t_{LZBE}	Byte enable to low Z	0	–	ns
t_{HZBE}	Byte disable to high Z	–	7	ns
Write Cycle[8, 9]				
t_{WC}	Write cycle time	15	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	10	–	ns
t_{AW}	Address setup to write end	10	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	10	–	ns
t_{SD}	Data setup to write end	8	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[5]	3	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5, 6]	–	4	ns
t_{BW}	Byte enable to end of write	10	–	ns

Notes

5. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
6. t_{HZOE}, t_{HZBE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in (b) of Figure 2 on page 5. Transition is measured ±500 mV from steady-state voltage.
7. This parameter is guaranteed by design and is not tested.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW, $\overline{WE}$ LOW and $\overline{BHE}$ / $\overline{BLE}$ LOW. $\overline{CE}$, $\overline{WE}$ and $\overline{BHE}$ / $\overline{BLE}$ must be LOW to initiate a write, and the transition of these signals can terminate the write. The input data setup and hold timing should be referenced to the leading edge of the signal that terminates the write.
9. The minimum write pulse width for WRITE Cycle No.3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 3. Read Cycle No. 1 [10, 11]

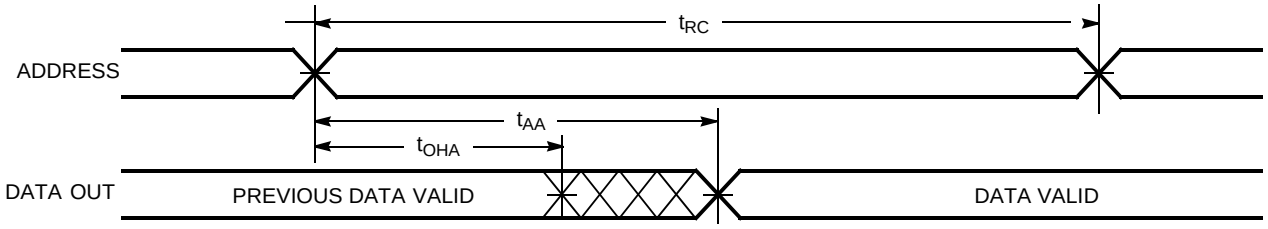
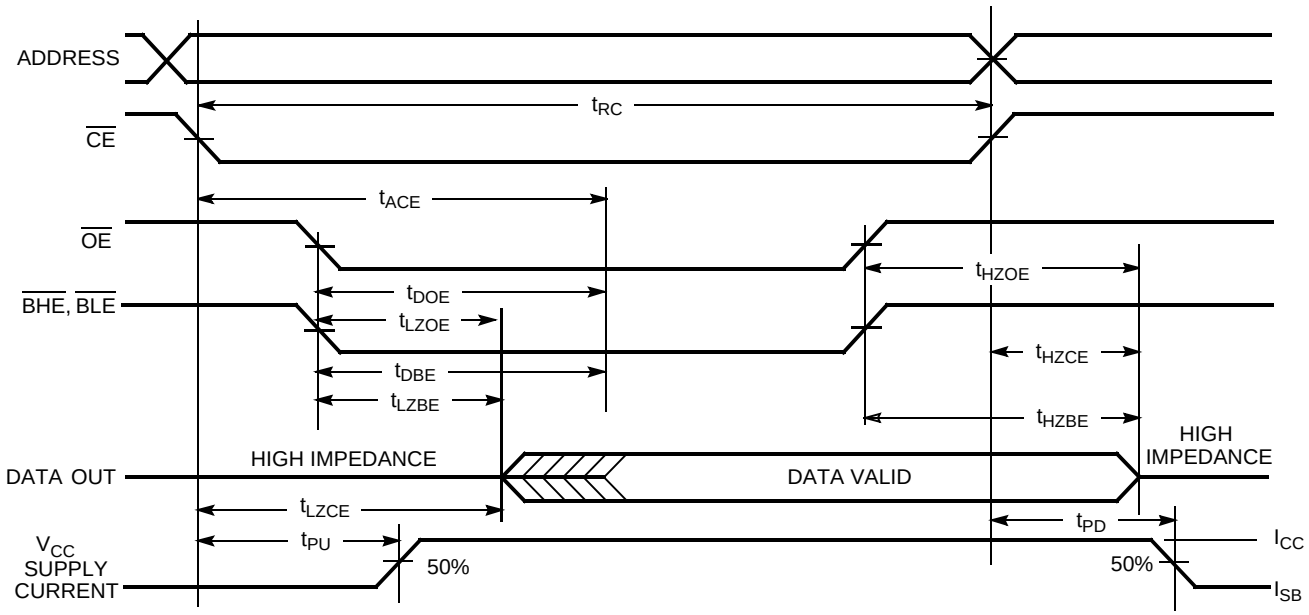


Figure 4. Read Cycle No. 2 ($\overline{OE}$ Controlled) [11, 12]



Notes
10. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$ and/or $\overline{BHE} = V_{IL}$.
11. $\overline{WE}$ is HIGH for read cycle.
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Figure 5. Write Cycle No. 1 ($\overline{CE}$ Controlled) [13, 14]

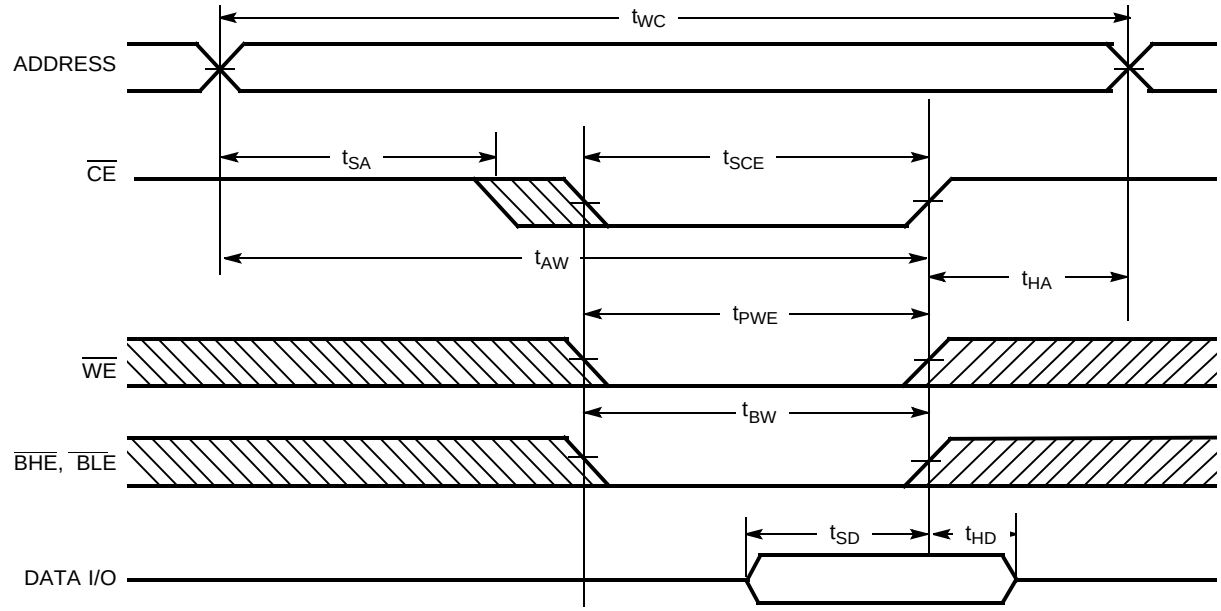
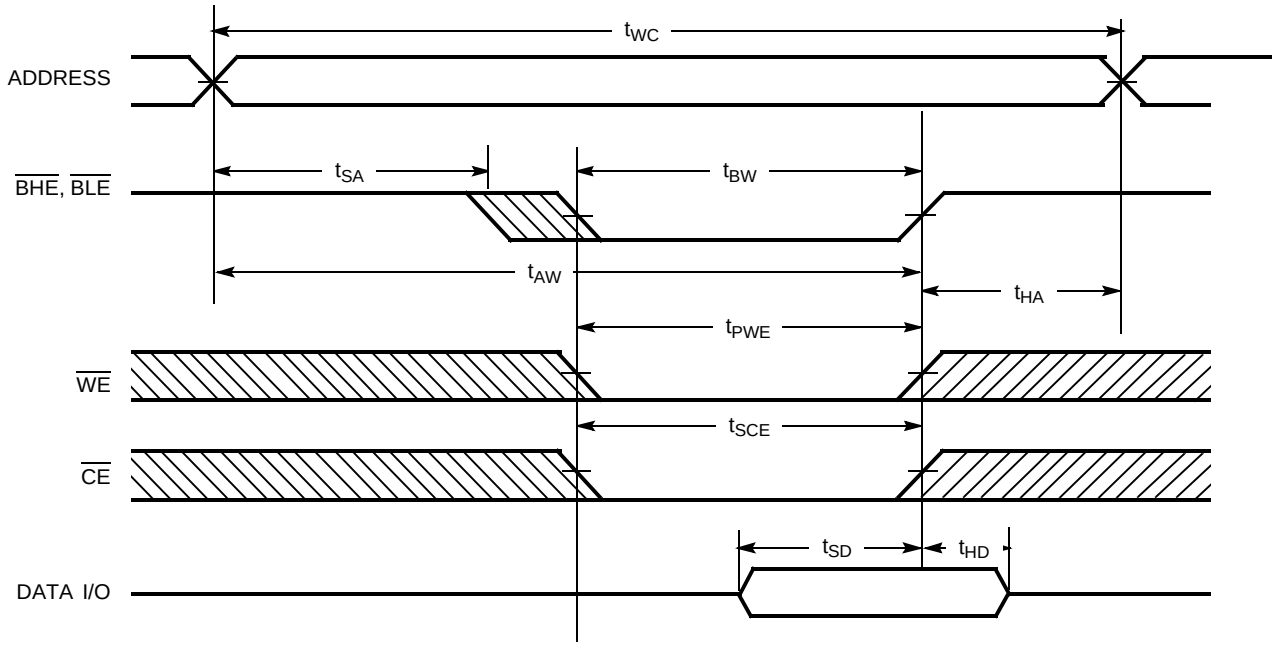


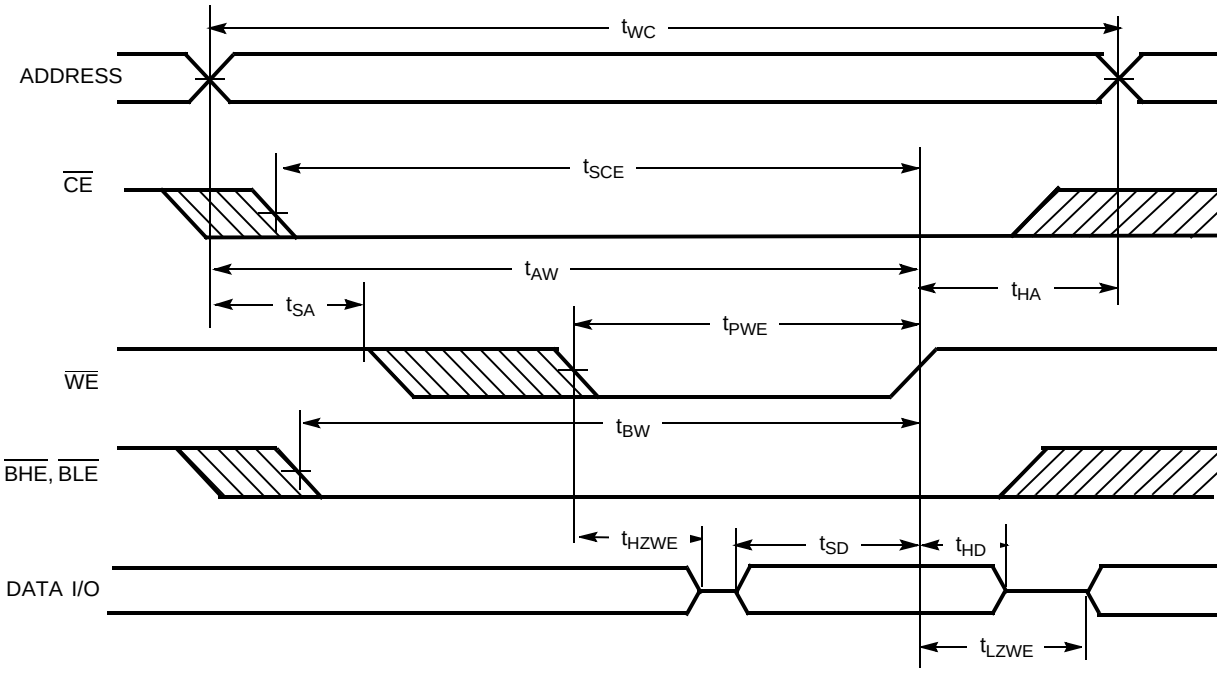
Figure 6. Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled)



Notes
13. Data I/O is high impedance if $\overline{OE}$ or $\overline{BHE}$ and $\overline{BLE}$ = V_{IH}.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high impedance state.

Switching Waveforms (continued)

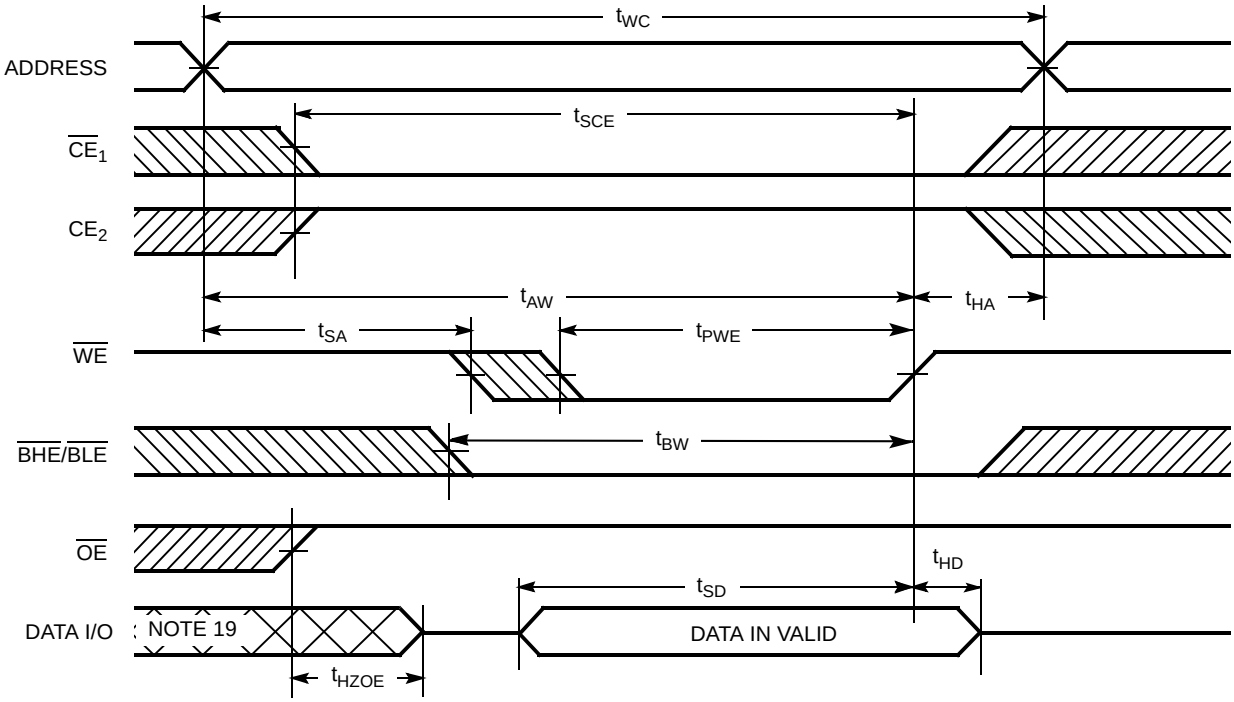
Figure 7. Write Cycle No. 3 (WE Controlled, OE LOW) [15]



Note
15. The minimum write pulse width for WRITE Cycle No.3 (WE Controlled, OE LOW) should be sum of t_{HZWE} and t_{SD}.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 4 ($\overline{WE}$ Controlled) [16, 17, 18]



Notes

16. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE_1} = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$ or both $= V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
17. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
18. If $\overline{CE_1}$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
19. During this period the I/Os are in output state. Do not apply input signals.

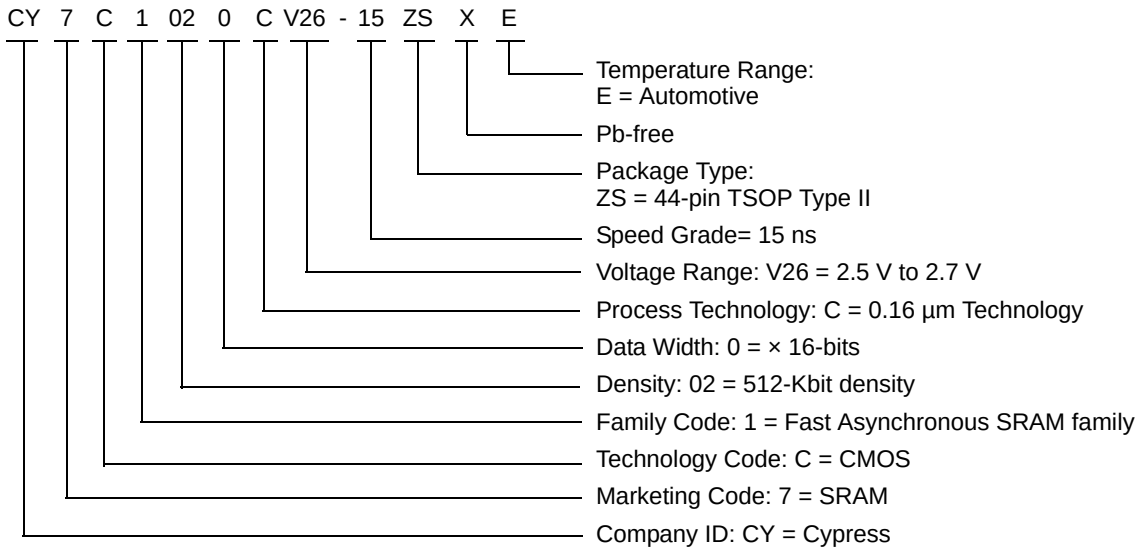
Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O_1–I/O_8	I/O_9–I/O_{16}	Mode	Power
H	X	X	X	X	High Z	High Z	Power-Down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read – All bits	Active (I_{CC})
			L	H	Data Out	High Z	Read – Lower bits only	Active (I_{CC})
			H	L	High Z	Data Out	Read – Upper bits only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write – All bits	Active (I_{CC})
			L	H	Data In	High Z	Write – Lower bits only	Active (I_{CC})
			H	L	High Z	Data In	Write – Upper bits only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})
L	X	X	H	H	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

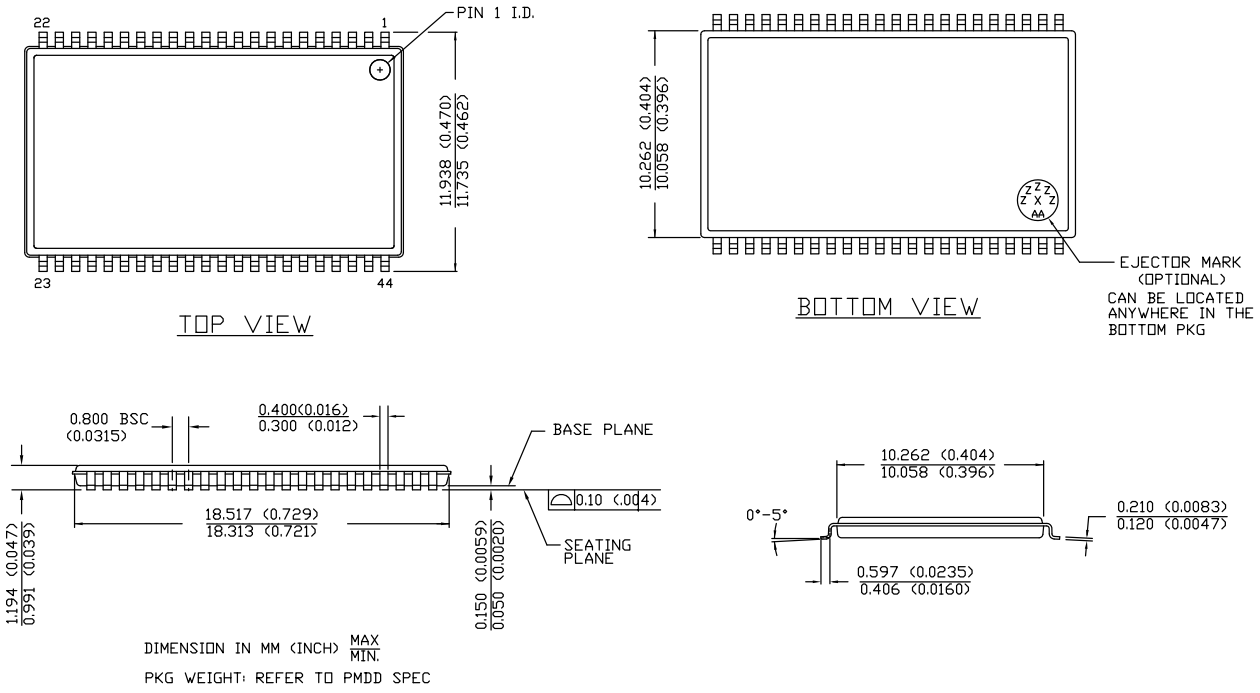
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C1020CV26-15ZSXE	Z44	44-pin TSOP Type II (Pb-free)	Automotive

Ordering Code Definitions



Package Diagrams

Figure 9. 44-pin TSOP Z44-II Package Outline, 51-85087



51-85087 *E

Acronyms

Acronym	Description
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mm	millimeter
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt

Document History Page

Document Title: CY7C1020CV26, 512-Kbit (32 K × 16) Static RAM Document Number: 38-05406				
Rev.	**ECN NO.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	128060	07/30/03	EJH	Customized data sheet to meet special requirements for CG5988AF Automotive temperature range: –40°C / +125°C
*A	352999	See ECN	SYT	Updated Document Title (to include the mention of '512Kb'). Removed 'CG5988AF' from the Datasheet. Updated Features (for better structure).
*B	2903127	04/01/2010	VIVG	Updated Package Diagrams. Added Sales, Solutions, and Legal Information. Updated to new template.
*C	3109992	12/14/2010	AJU	Added Ordering Code Definitions.
*D	3346414	08/16/2011	RAME	Updated Ordering Code Definitions.
*E	4499482	09/11/2014	MEMJ	Updated AC Switching Characteristics: Updated Note 7. Added Note 9 and referred the same note in "Write Cycle". Updated Switching Waveforms: Added Note 15 and referred the same note in Figure 7. Updated Package Diagrams: spec 51-85087 – Changed revision from *C to *E. Updated to new template. Completing Sunset Review.
*F	4573200	11/18/2014	MEMJ	Updated Functional Description: Added "For a complete list of related documentation, click here." at the end.
*G	4919066	09/14/2015	VINI	Updated Switching Waveforms: Added Figure 8. Added Note 16, 17, 18, 19 and referred the same notes in Figure 8. Added Acronyms and Units of Measure. Updated to new template. Completing Sunset Review.

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