

DDR5 SDRAM UDIMM Addendum

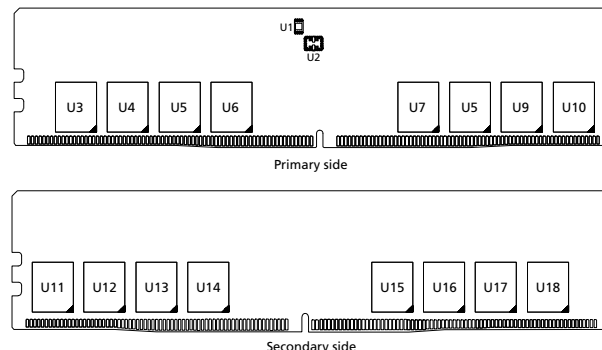
MTC16C2085S1UC – 32GB 16Gb Die Revision A

Features

Information provided here is in addition to or supersedes information provided in the Micron DDR5 UDIMM Core data sheet.

- DDR5 functionality and operations supported as defined in the component data sheet
- Features and specifications defined in the Micron DDR5 UDIMM core data sheet
- 288-pin, DDR5 unbuffered dual in-line memory module (DDR5 UDIMM)
- Fast data transfer rate: PC5-4800, PC5-5600
- 32GB (4 Gig x 64)
- Dual-rank
- 32 internal banks; 8 groups of 4 banks each

Figure 1: 288-Pin DDR5 UDIMM (R/C-A0)



Options

- Operating temperature
 - Commercial ($0^{\circ}\text{C} \leq T_{\text{OPER}} \leq 95^{\circ}\text{C}$)
- Frequency/CAS latency
 - 0.416ns @ CL = 40 (DDR5-4800)
 - 0.357ns @ CL = 46 (DDR5-5600)

Marking

C
48B
56B

Table 1: Addressing

Parameter	32GB
Row address ¹	64K (R0-R15)
Column address ¹	1K (C0-C9)
Device bank group address ¹	8 (BG0-BG2)
Device bank address per bank group ¹	4 (BA0-BA1)
Device configuration	16Gb (2Gb x 8), 32 banks
Module rank address	2 (CS0_n, CS1_n)

Notes: 1. These parameters represent the logical address state of the CA bus for different commands. Refer to the command truth table in the component data sheet.



32GB (x64, DR) 288-Pin DDR5 UDIMM Features

Table 2: Part Numbers and Timing Parameters – 32GB Modules

Base device: MT60B2G8,¹ 16Gb DDR5 SDRAM Die Revision A

Part Number	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-nRCD-nRP)
MTC16C2085S1UC48BA1	32GB	4Gb x 64	38.4 GB/s	0.416ns/4800 MT/s	40-39-39
MTC16C2085S1UC56BA1	32GB	4Gb x 64	44.8 GB/s	0.357ns/5600 MT/s	46-45-45

Notes: 1. The data sheet for the base device can be found on [micron.com](https://www.micron.com).

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DQ Map

Table 3: Component-to-Module DQ Map

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U3	0	3A	156	U4	0	11A	166
	1	2A	154		1	8A	20
	2	1A	11		2	10A	164
	3	0A	9		3	9A	22
	4	7A	162		4	15A	173
	5	4A	16		5	12A	26
	6	5A	18		6	13A	28
	7	6A	160		7	14A	171
U5	0	23A	183	U6	0	29A	49
	1	20A	37		1	28A	47
	2	22A	181		2	31A	194
	3	21A	39		3	30A	192
	4	19A	177		4	27A	187
	5	16A	30		5	24A	41
	6	18A	175		6	25A	43
	7	17A	32		7	26A	185
U7	0	3B	248	U8	0	10B	256
	1	0B	101		1	8B	112
	2	2B	246		2	11B	258
	3	1B	103		3	9B	114
	4	7B	254		4	15B	265
	5	4B	108		5	12B	118
	6	5B	110		6	13B	120
	7	6B	252		7	14B	263
U9	0	18B	267	U10	0	29B	141
	1	17B	124		1	28B	139
	2	19B	269		2	31B	286
	3	16B	122		3	30B	284
	4	23B	275		4	27B	279
	5	20B	129		5	24B	133
	6	21B	131		6	26B	277
	7	22B	273		7	25B	135

Table 3: Component-to-Module DQ Map (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U11	0	28B	139	U12	0	17B	124
	1	29B	141		1	18B	267
	2	30B	284		2	16B	122
	3	31B	286		3	19B	269
	4	24B	133		4	20B	129
	5	27B	279		5	23B	275
	6	25B	135		6	22B	273
	7	26B	277		7	21B	131
U13	0	8B	112	U14	0	0B	101
	1	10B	256		1	3B	248
	2	9B	114		2	1B	103
	3	11B	258		3	2B	246
	4	12B	118		4	4B	108
	5	15B	265		5	7B	254
	6	14B	263		6	6B	252
	7	13B	120		7	5B	110
U15	0	28A	47	U16	0	20A	37
	1	29A	49		1	23A	183
	2	30A	192		2	21A	39
	3	31A	194		3	22A	181
	4	24A	41		4	16A	30
	5	27A	187		5	19A	177
	6	26A	185		6	17A	32
	7	25A	43		7	18A	175
U17	0	8A	20	U18	0	2A	154
	1	11A	166		1	3A	156
	2	9A	22		2	0A	9
	3	10A	164		3	1A	11
	4	12A	26		4	4A	16
	5	15A	173		5	7A	162
	6	14A	171		6	6A	160
	7	13A	28		7	5A	18

I_{DD} Specifications

Table 4: DDR5 I_{DD} Specifications and Conditions – 32GB (Die Revision A)

Module I_{DD} is based on PMIC VIN_BULK 5V input current and typical operating range of temperature. Each I_{DD} parameter includes PMIC efficiency and all DRAM current on all supplies (V_{DD}, V_{DDQ}, and V_{PP}).

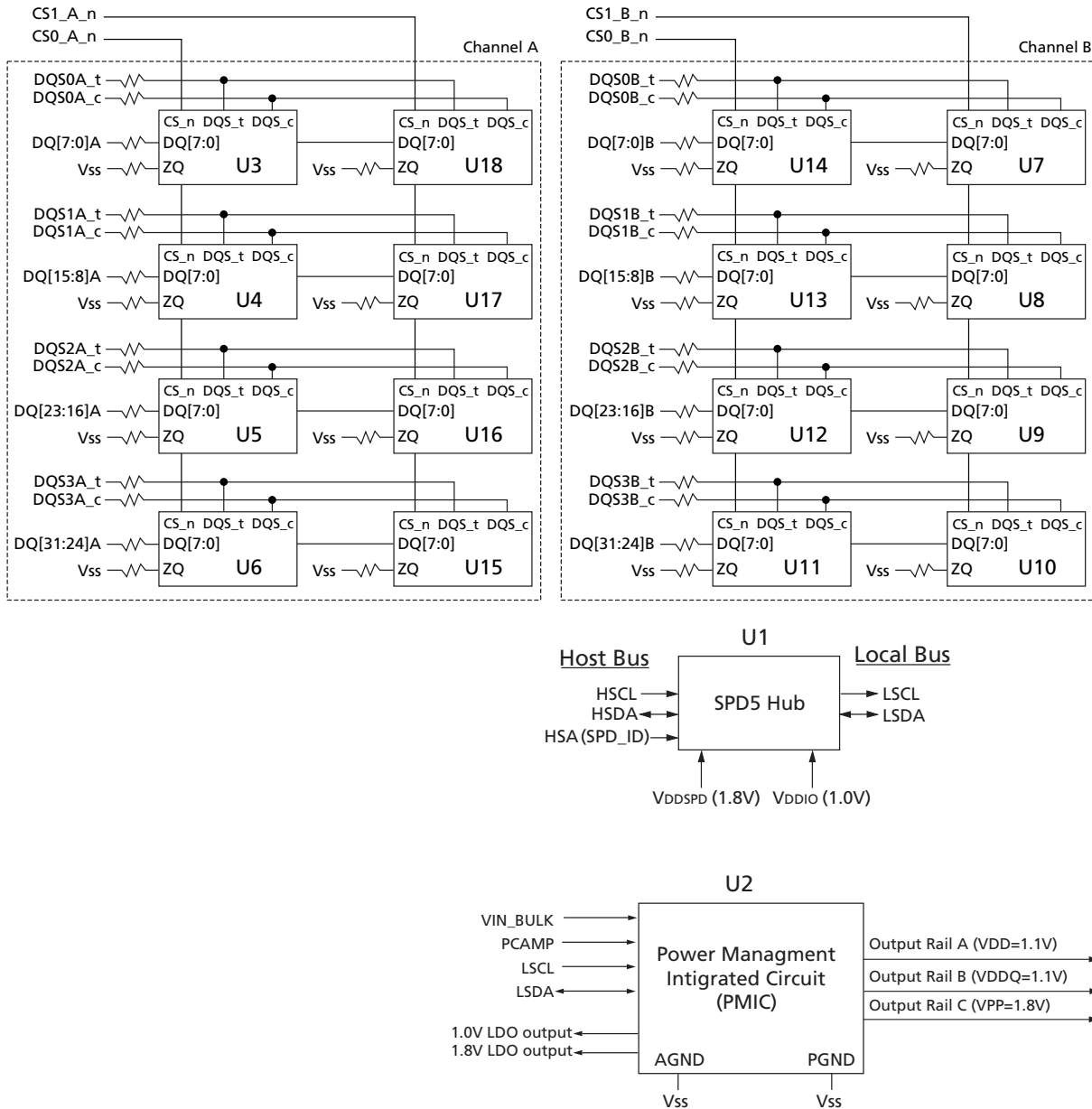
Parameter	Symbol	4800	5600	Units
Operating one bank ACTIVATE-PRECHARGE current	I _{DD0} ¹	247	TBD	mA
Operating four bank ACTIVATE-PRECHARGE current	I _{DD0F} ¹	328	TBD	mA
Precharge standby current	I _{DD2N} ²	219	TBD	mA
Precharge standby non-target command	I _{DD2NT} ¹	370	TBD	mA
Precharge power-down current	I _{DD2P} ²	187	TBD	mA
Active standby current	I _{DD3N} ²	249	TBD	mA
Active power-down current	I _{DD3P} ²	221	TBD	mA
Operating burst read current	I _{DD4R} ¹	757	TBD	mA
Operating burst write current	I _{DD4W} ¹	993	TBD	mA
Operating burst write with write CRC current	I _{DD4WC} ¹	907	TBD	mA
Burst refresh (normal refresh mode) current	I _{DD5B} ¹	550	TBD	mA
Burst refresh (fine granularity refresh mode) current	I _{DD5F} ¹	373	TBD	mA
Burst refresh (same bank refresh mode) current	I _{DD5C} ¹	290	TBD	mA
Self refresh current	I _{DD6N} ²	119	TBD	mA
Operating bank interleave read current	I _{DD7} ¹	825	TBD	mA
Maximum power saving deep power down mode current	I _{DD8} ²	86	TBD	mA

Notes: 1. One module rank in this I_{DD}/I_{DDQ}/I_{PP} condition, the other rank in I_{DD2N}/I_{DDQ2N}/I_{PP2N}.

2. Both ranks in this I_{DD}/I_{DDQ}/I_{PP} condition.

Functional Block Diagram

Figure 2: Functional Block Diagram



- Notes:
1. The ZQ ball on each DDR5 component is connected to an external $240\Omega \pm 1\%$ resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.
 2. Functional block diagram is for reference only.



Revision History

Rev. F – 10/2021

- Add 5600 speed, IDDs are TBD
- Remove Micron Confidential marking

Rev. E – 08/2021

- Production Release

Rev. D – 02/2021

- Preliminary Release

Rev. C – 01/2021

- Preliminary Release

Rev. B – 06/2020

- Preliminary Release

Rev. A – 06/2020

- Preliminary Release

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