

IRHNM597110, IRHNMC597110

PD-97179D

Radiation Hardened Power MOSFET Surface Mount (SMD-0.2) 100V, 3.1A, P-channel, R5 Technology

Features

- Single event effect (SEE) hardened
- Low total gate charge
- Simple drive requirements
- Hermetically sealed
- Surface mount
- Ceramic package
- Light weight
- ESD rating: Class 1A per MIL-STD-750, Method 1020

Potential Applications

- DC-DC converter
- Motor drives

Product Validation

Qualified according to MIL-PRF-19500 for space applications

Description

IR HiRel R5 technology provides high performance power MOSFETs for space applications. These devices have been characterized for Single Event Effects (SEE) with useful performance up to an LET of 80MeV·cm²/mg. The combination of low $R_{DS(on)}$ and low gate charge reduces the power losses in switching applications such as DC-DC converters and motor control. These devices retain all of the well-established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parameters switching and temperature stability of electrical parameters.

Ordering Information

Table 1 Ordering options

Part number	Package	Screening Level	TID Level
IRHNM597110	SMD-0.2	COTS	100 krad(Si)
JANSR2N7506U8	SMD-0.2	JANS	100 krad(Si)
IRHNMC597110	SMD-0.2 ceramic lid	COTS	100 krad(Si)
JANSR2N7506U8C	SMD-0.2 ceramic lid	JANS	100 krad(Si)
IRHNM593110	SMD-0.2	COTS	300 krad(Si)
JANSF2N7506U8C	SMD-0.2	JANS	300 krad(Si)
IRHNMC593110	SMD-0.2 ceramic lid	COTS	300 krad(Si)
JANSF2N7506U8C	SMD-0.2 ceramic lid	JANS	300 krad(Si)

Product Summary

- BV_{DSS} : -100V
- I_D : -3.1A
- $R_{DS(on), max}$: 1.2Ω
- $Q_{G, max}$: 11nC
- REF: MIL-PRF-19500/749

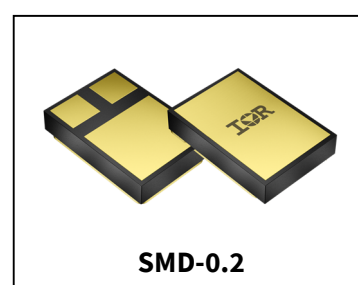


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Absolute Maximum Ratings

1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings (Pre-Irradiation)

Symbol	Parameter	Value	Unit
$I_{D1} @ V_{GS} = -12V, T_C = 25^{\circ}C$	Continuous Drain Current	-3.1	A
$I_{D2} @ V_{GS} = -12V, T_C = 100^{\circ}C$	Continuous Drain Current	-2.0	A
$I_{DM} @ T_C = 25^{\circ}C$	Pulsed Drain Current ¹	-12.4	A
$P_D @ T_C = 25^{\circ}C$	Maximum Power Dissipation	23	W
	Linear Derating Factor	0.18	W/ $^{\circ}C$
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ²	28	mJ
I_{AR}	Avalanche Current ¹	-3.1	A
E_{AR}	Repetitive Avalanche Energy ¹	2.3	mJ
dv/dt	Peak Diode Reverse Recovery ³	-21	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	$^{\circ}C$
	Lead Temperature	300 (for 5s)	
	Weight	0.25 (Typical)	

¹ Repetitive Rating; Pulse width limited by maximum junction temperature.² $V_{DD} = -50V$, starting $T_J = 25^{\circ}C$, $L = 5.8mH$, Peak $I_L = -3.1A$, $V_{GS} = -12V$ ³ $I_{SD} \leq -3.1A$, $di/dt \leq 544A/\mu s$, $V_{DD} \leq -100V$, $T_J \leq 150^{\circ}C$

Device Characteristics

2 Device Characteristics

2.1 Electrical Characteristics (Pre-Irradiation)

Table 3 Static and Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-100	—	—	V	$V_{GS} = 0V, I_D = -1.0mA$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.13	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = -1mA$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	1.2	Ω	$V_{GS} = 12V, I_{D2} = -2.0A^1$
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{DS} = V_{GS}, I_D = -1.0mA$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	4.88	—	mV/ $^\circ\text{C}$	
G_{fs}	Forward Transconductance	1.9	—	—	S	$V_{DS} = -15V, I_{D2} = -2.0A^1$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	-10	μA	$V_{DS} = -80V, V_{GS} = 0V$
		—	—	-25		$V_{DS} = -80V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	$V_{GS} = -20V$
	Gate-to-Source Leakage Reverse	—	—	100		$V_{GS} = 20V$
Q_G	Total Gate Charge	—	—	11	nC	$I_{D1} = -3.1A$
Q_{GS}	Gate-to-Source Charge	—	—	5.0		$V_{DS} = -50V$
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	4.0		$V_{GS} = -12V$
$t_{d(on)}$	Turn-On Delay Time	—	—	18	ns	$I_{D1} = -3.1A^{**}$ $V_{DD} = -50V$ $R_G = 7.5\Omega$ $V_{GS} = -12V$
t_r	Rise Time	—	—	26		
$t_{d(off)}$	Turn-Off Delay Time	—	—	24		
t_f	Fall Time	—	—	85		
$L_s + L_D$	Total Inductance	—	6.8	—	nH	Measured from center of Drain pad to center of Source pad
C_{iss}	Input Capacitance	—	379	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	98	—		$V_{DS} = -25V$
C_{rss}	Reverse Transfer Capacitance	—	9.5	—		$f = 100KHz$
R_G	Gate Resistance	—	24	—	Ω	$f = 1.0MHz$, open drain

** Switching speed maximum limits are based on manufacturing test equipment and capability.

¹ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$

Device Characteristics

2.2 Source-Drain Diode Ratings and Characteristics (Pre-Irradiation)

Table 4 Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-3.1	A	
I _{SM}	Pulsed Source Current (Body Diode) ¹	—	—	-12.4	A	
V _{SD}	Diode Forward Voltage	—	—	-5.0	V	T _J = 25°C, I _S = -3.1A, V _{GS} = 0V ²
t _{rr}	Reverse Recovery Time	—	—	100	ns	T _J = 25°C, I _F = -3.1A, V _{DD} ≤ -50V di/dt = -100A/μs ²
Q _{rr}	Reverse Recovery Charge	—	271	—	nC	
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

2.3 Thermal Characteristics

Table 5 Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-Case	—	—	5.4	$^\circ\text{C}/\text{W}$

2.4 Radiation Characteristics

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 3 and 4) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

2.4.1 Electrical Characteristics — Post Total Dose Irradiation

Table 6 Electrical Characteristics @ $T_J = 25^\circ\text{C}$, Post Total Dose Irradiation ^{3, 4}

Symbol	Parameter	100 krad (Si) ⁵		300 krad (Si) ⁶		Unit	Test Conditions
		Min.	Max.	Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	-100	—	-100	—	V	$V_{GS} = 0\text{V}$, $I_D = -1.0\text{mA}$
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	-4.0	-2.0	-4.0	V	$V_{DS} = V_{GS}$, $I_D = -1.0\text{mA}$
I_{GSS}	Gate-to-Source Leakage Forward	—	-100	—	-100	nA	$V_{GS} = -20\text{V}$
	Gate-to-Source Leakage Reverse	—	100	—	100		$V_{GS} = 20\text{V}$
I_{DSS}	Zero Gate Voltage Drain Current	—	-10	—	-10	μA	$V_{DS} = -80\text{V}$, $V_{GS} = 0\text{V}$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (TO-3) ²	—	0.916	—	0.936	Ω	$V_{GS} = -12\text{V}$, $I_{D2} = -2.0\text{A}$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (SMD-0.2) ²	—	1.2	—	1.2	Ω	$V_{GS} = -12\text{V}$, $I_{D2} = -2.0\text{A}$
V_{SD}	Diode Forward Voltage	—	-5.0	—	-5.0	V	$V_{GS} = 0\text{V}$, $I_F = -3.1\text{A}$

¹ Repetitive Rating; Pulse width limited by maximum junction temperature.

² Pulse width $\leq 300 \mu\text{s}$; Duty Cycle $\leq 2\%$

³ Total Dose Irradiation with V_{GS} Bias. $V_{GS} = -12\text{V}$ applied and $V_{DS} = 0$ during irradiation per MIL-STD-750, Method 1019, condition A.

⁴ Total Dose Irradiation with V_{DS} Bias. $V_{DS} = -80\text{V}$ applied and $V_{GS} = 0$ during irradiation per MIL-STD-750, Method 1019, condition A.

⁵ Part numbers IRHNM597110 (JANSR2N7506U8)

⁶ Part numbers IRHNM593110 (JANSF2N7506U8)

IRHNM597110, IRHNMC597110

Radiation Hardened Power MOSFET Surface-Mount (SMD-0.2)

Device Characteristics

2.4.2 Single Event Effects — Safe Operating Area

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. 1 and Table 7.

Table 7 Worst Case Single Event Effects Safe Operating Area

LET (MeV·cm ² /mg)	Energy (MeV)	Range (μm)	V _{DS} (V)				
			V _{GS} = 0V	V _{GS} = 5V	V _{GS} = 10V	V _{GS} = 15V	V _{GS} = 20V
38 ± 5%	270 ± 7.5%	35 ± 7.5%	-100	-100	-100	-100	-100
61 ± 5%	330 ± 7.5%	30 ± 7.5%	-100	-100	-100	-100	-25
84 ± 5%	350 ± 7.5%	28 ± 7.5%	-100	-100	-100	-30	—

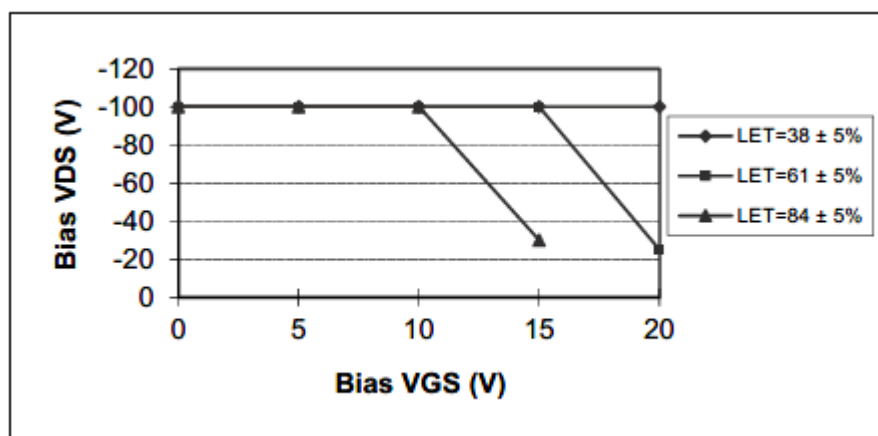


Figure 1 Worst Case Single Event Effect, Safe Operating Area

3

Electrical Characteristics Curves (Pre-irradiation)

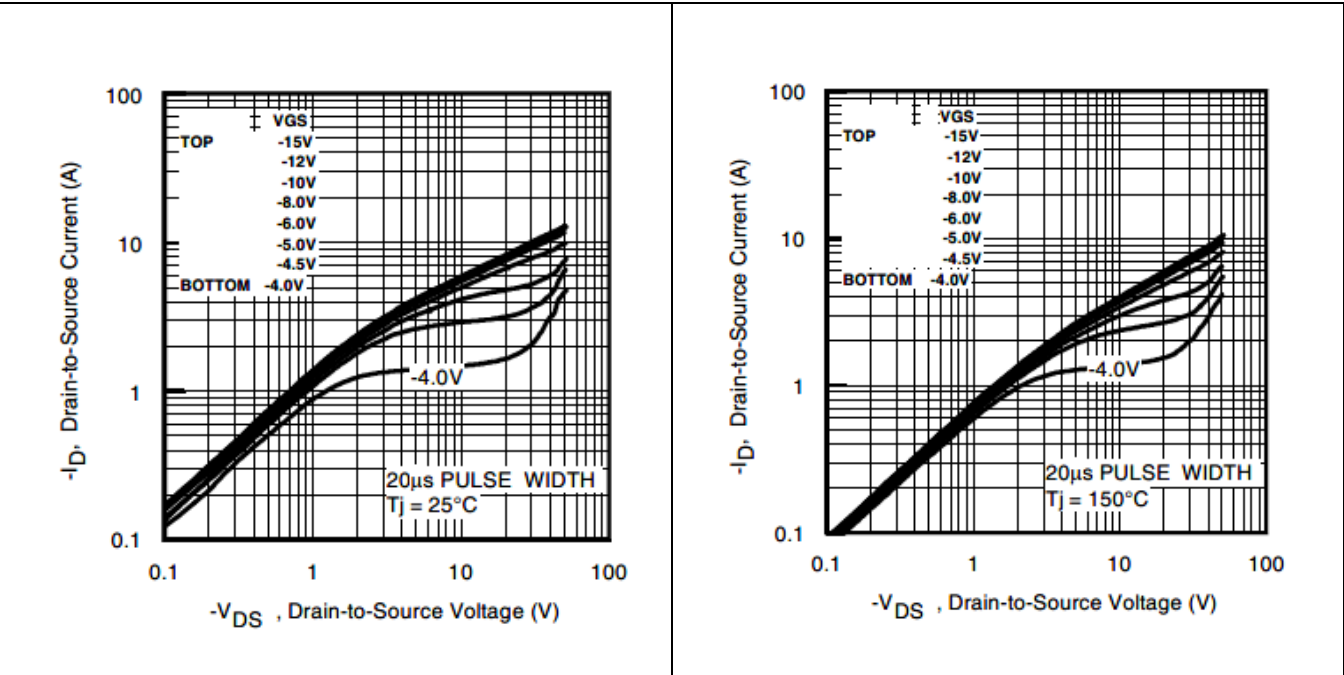


Figure 2 Typical Output Characteristics

Figure 3 Typical Output Characteristics

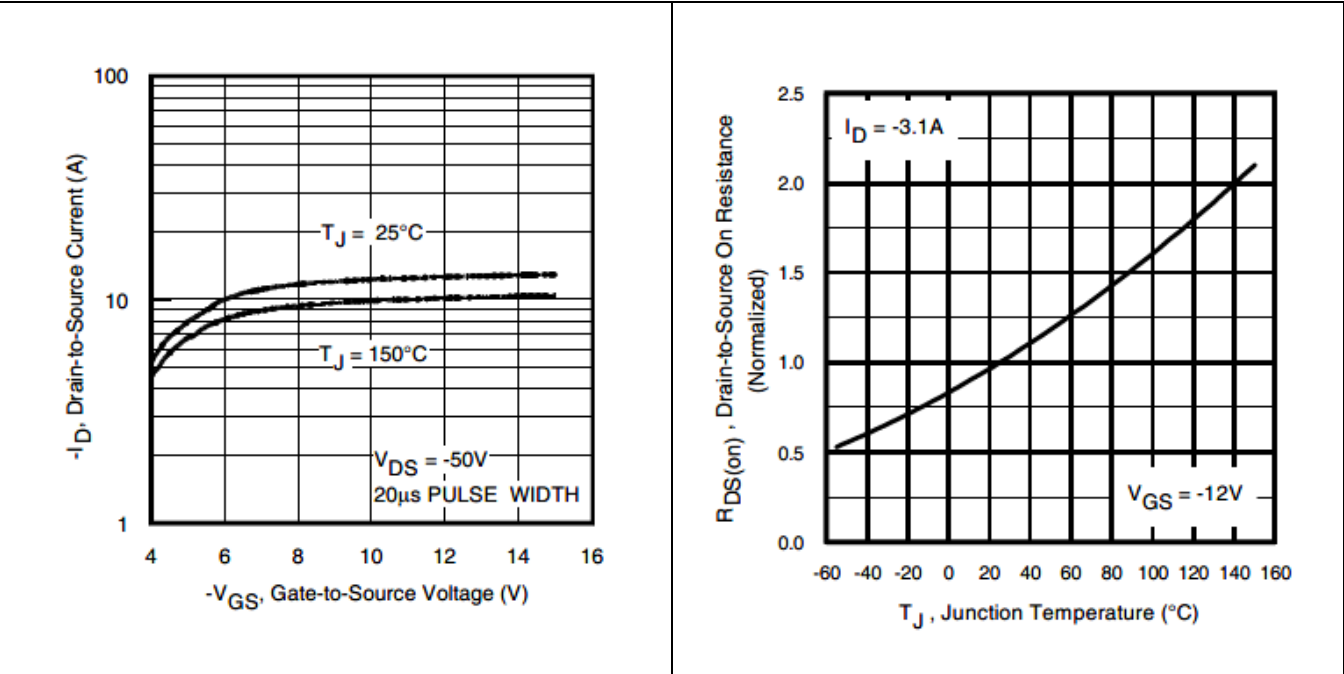


Figure 4 Typical Transfer Characteristics

Figure 5 Normalized On-Resistance Vs. Temperature

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Radiation Hardened Power MOSFET Surface-Mount (SMD-0.2)

Electrical Characteristics Curves (Pre-irradiation)

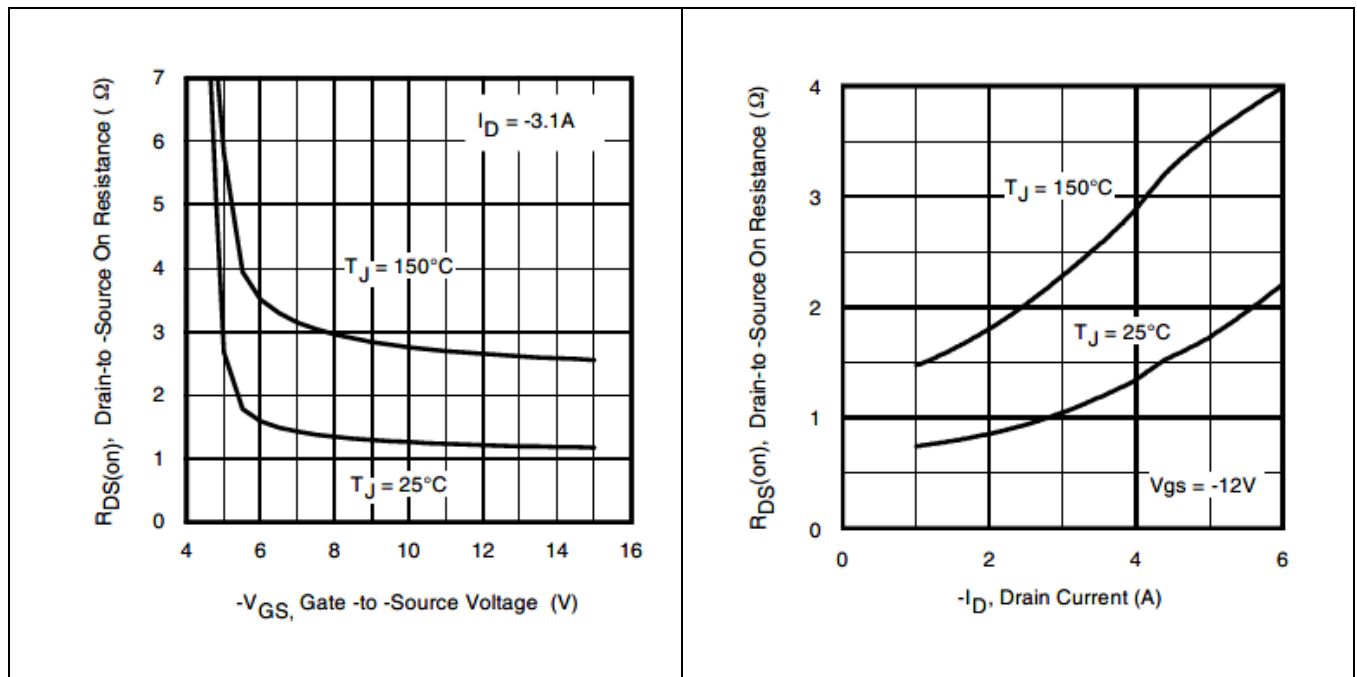


Figure 6 Typical On-Resistance Vs. Gate Voltage

Figure 7 Typical On-Resistance Vs. Drain Current

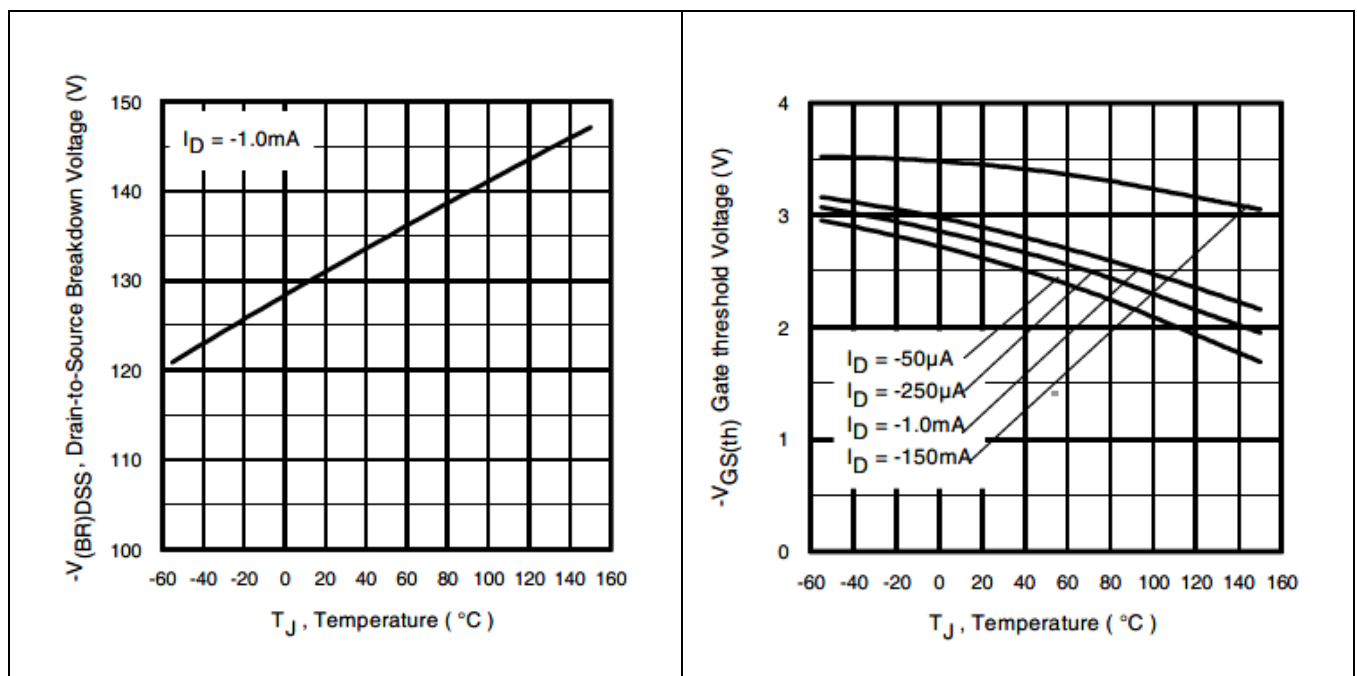


Figure 8 Typical Drain-to-Source Breakdown Voltage Vs. Temperature

Figure 9 Typical Threshold Voltage Vs. Temperature

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Radiation Hardened Power MOSFET Surface-Mount (SMD-0.2)

Electrical Characteristics Curves (Pre-irradiation)

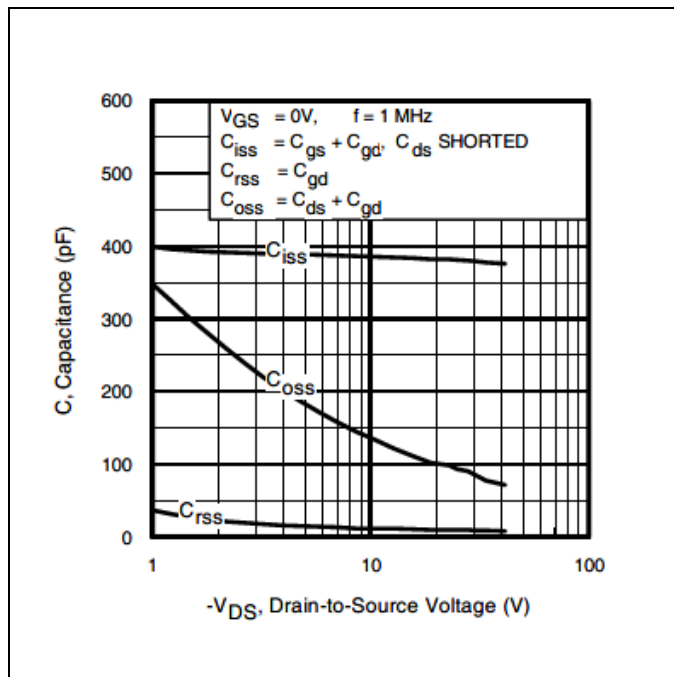


Figure 10 Typical Capacitance Vs. Drain-to-Source Voltage

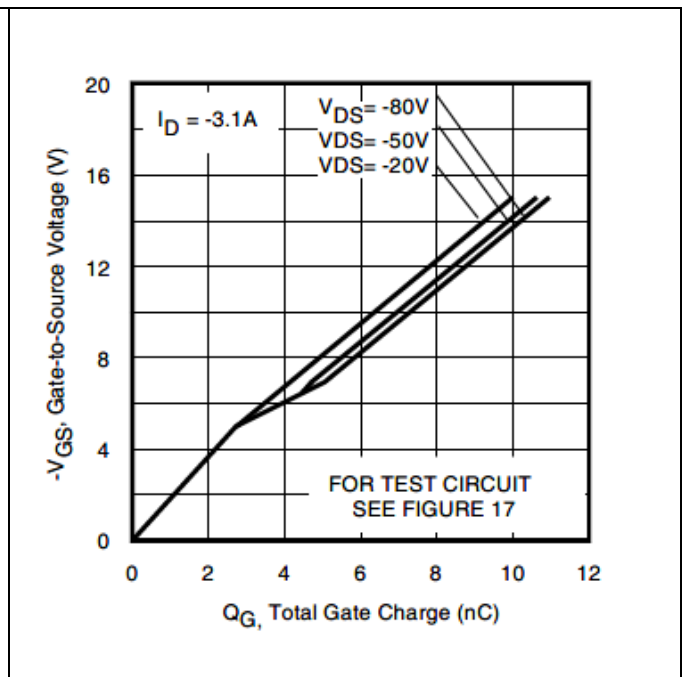


Figure 11 Gate-to-Source Voltage Vs. Typical Gate Charge

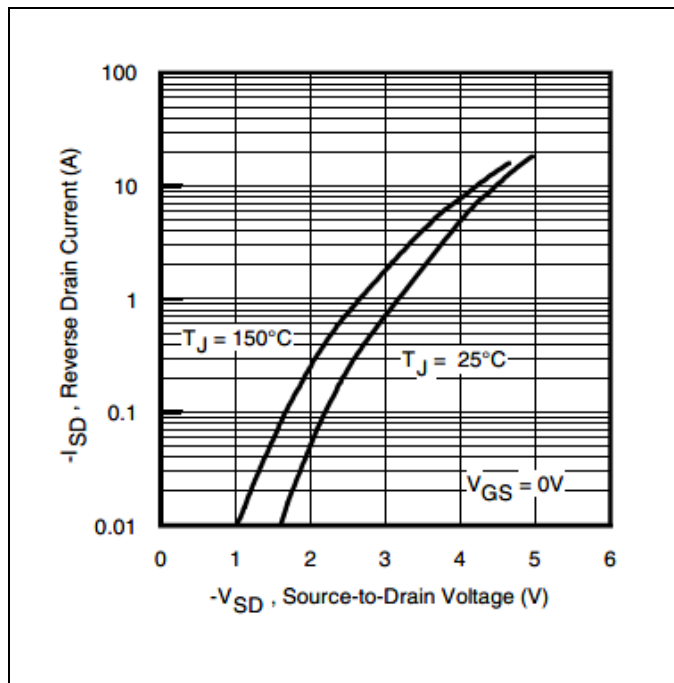


Figure 12 Typical Source-Drain Current Vs. Diode Forward Voltage

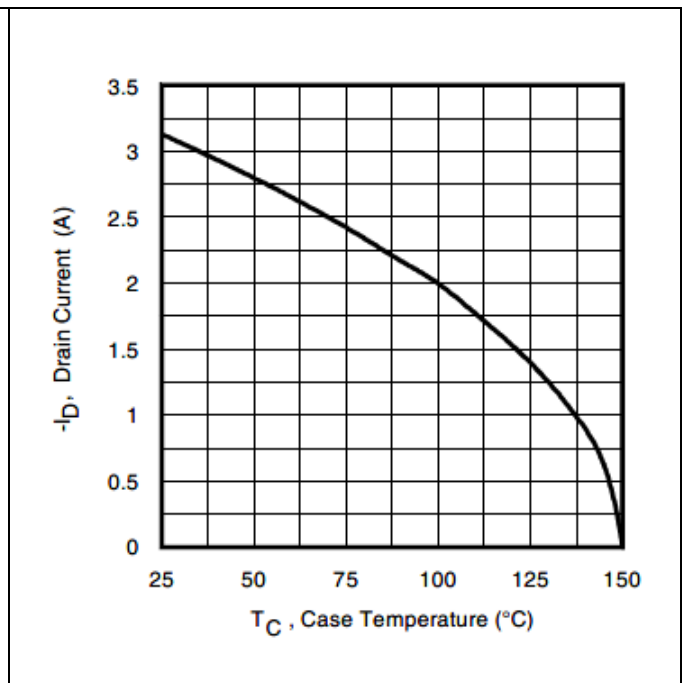


Figure 13 Maximum Drain Current Vs. Case Temperature

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Radiation Hardened Power MOSFET Surface-Mount (SMD-0.2)

Electrical Characteristics Curves (Pre-irradiation)

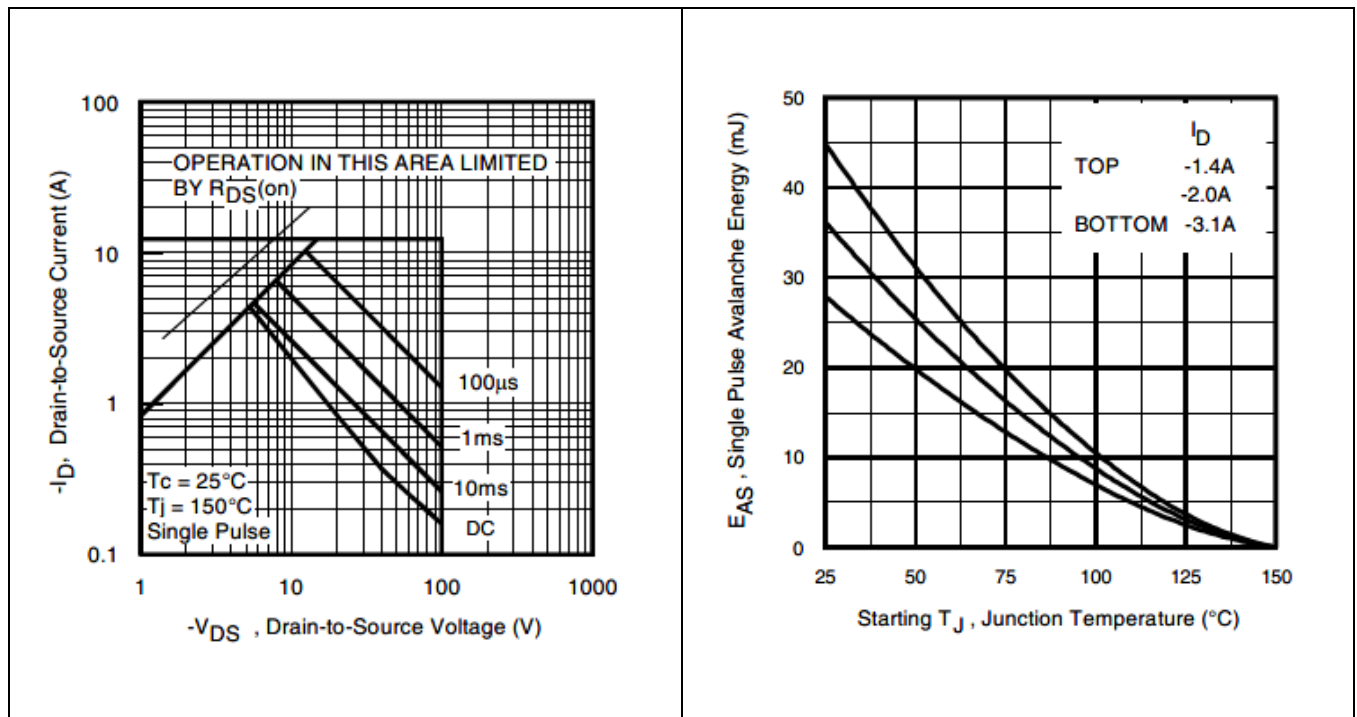


Figure 14 Maximum Safe Operating Area

Figure 15 Maximum Avalanche Energy Vs. Junction Temperature

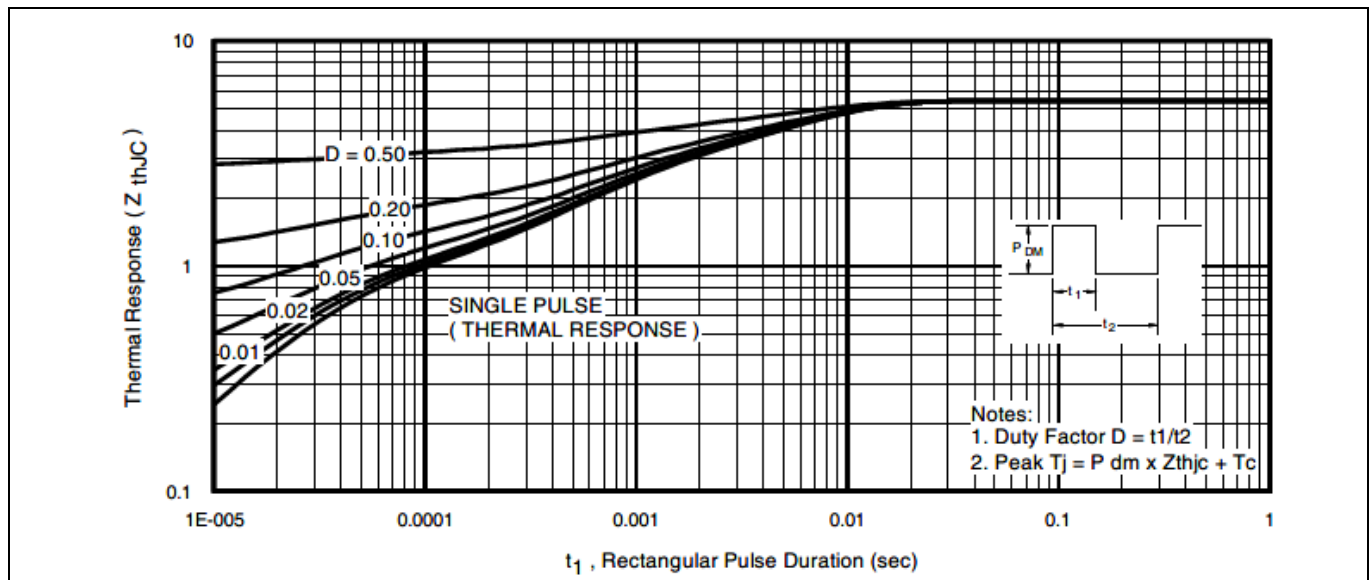


Figure 16 Maximum Effective Transient Thermal Impedance, Junction-to-Case

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Radiation Hardened Power MOSFET Surface-Mount (SMD-0.2)

Test Circuits (Pre-irradiation)

4 Test Circuits (Pre-irradiation)

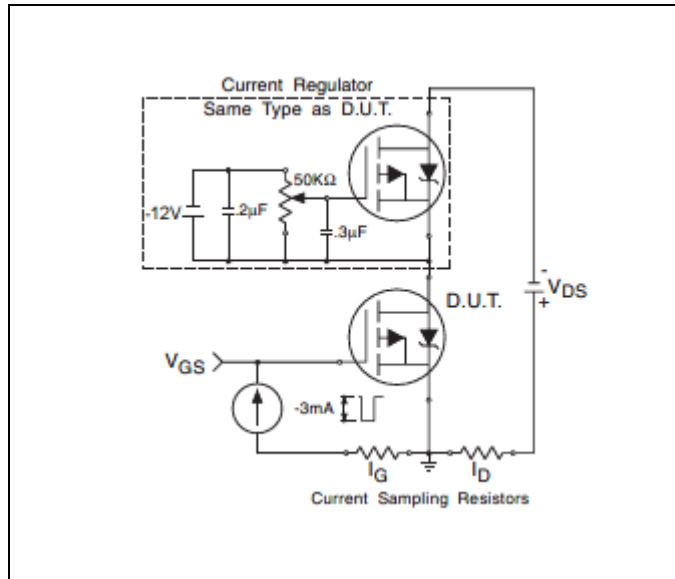


Figure 17 Gate Charge Test Circuit

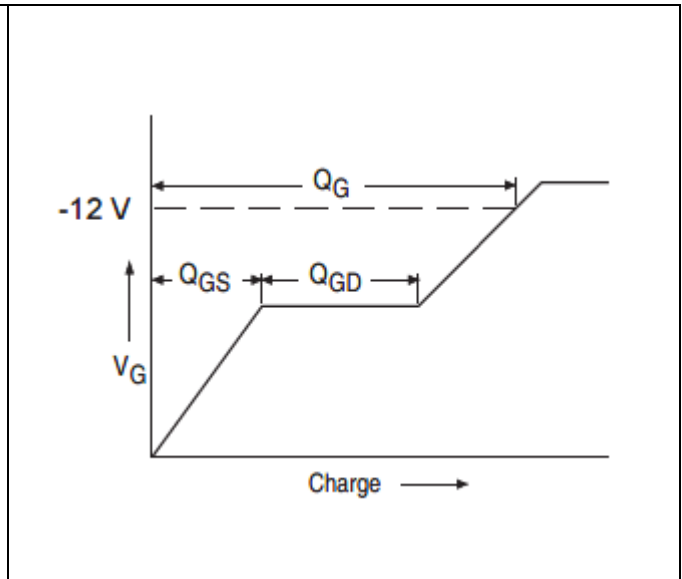


Figure 18 Gate Charge Waveform

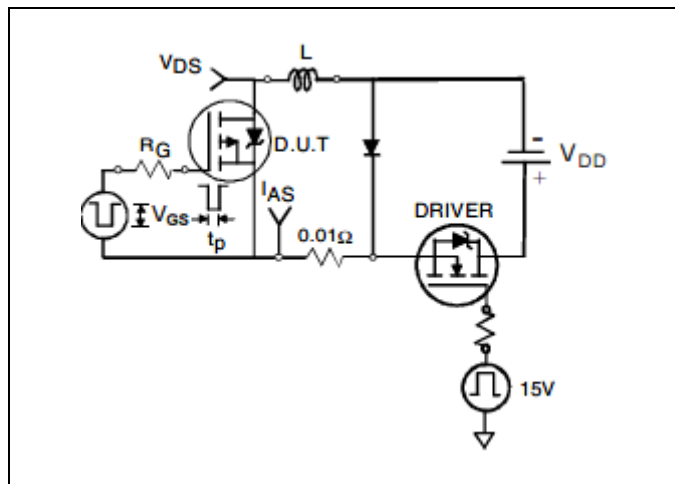


Figure 19 Unclamped Inductive Test Circuit

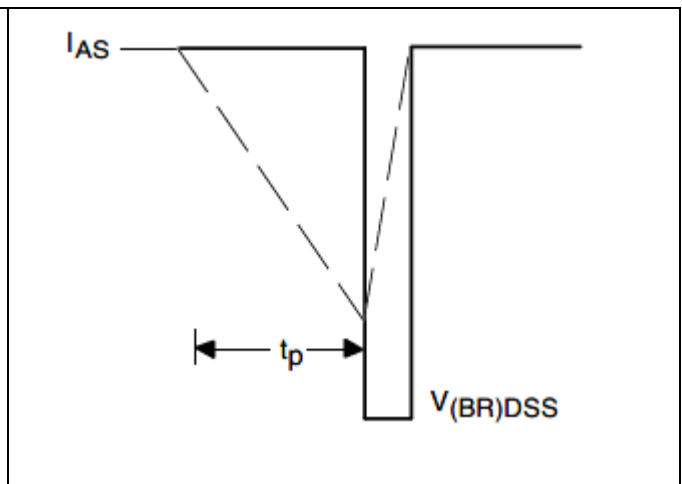


Figure 20 Unclamped Inductive Waveform

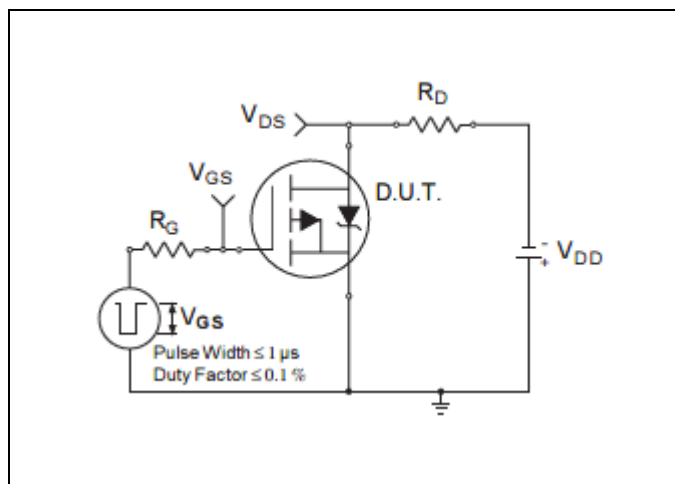


Figure 21 Switching Time Test Circuit

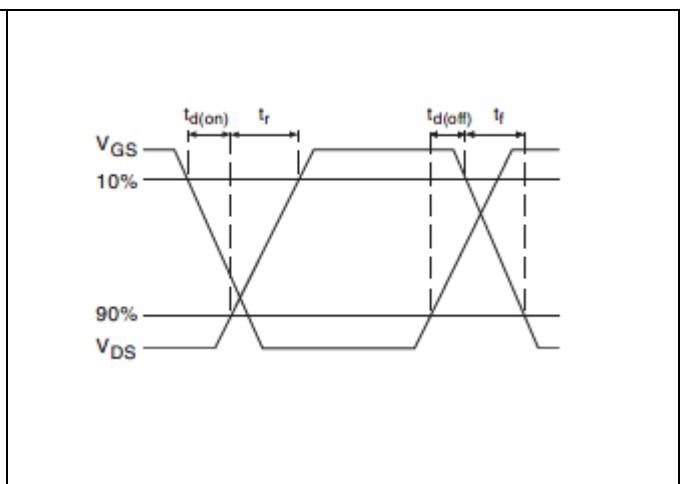


Figure 22 Switching Time Waveforms

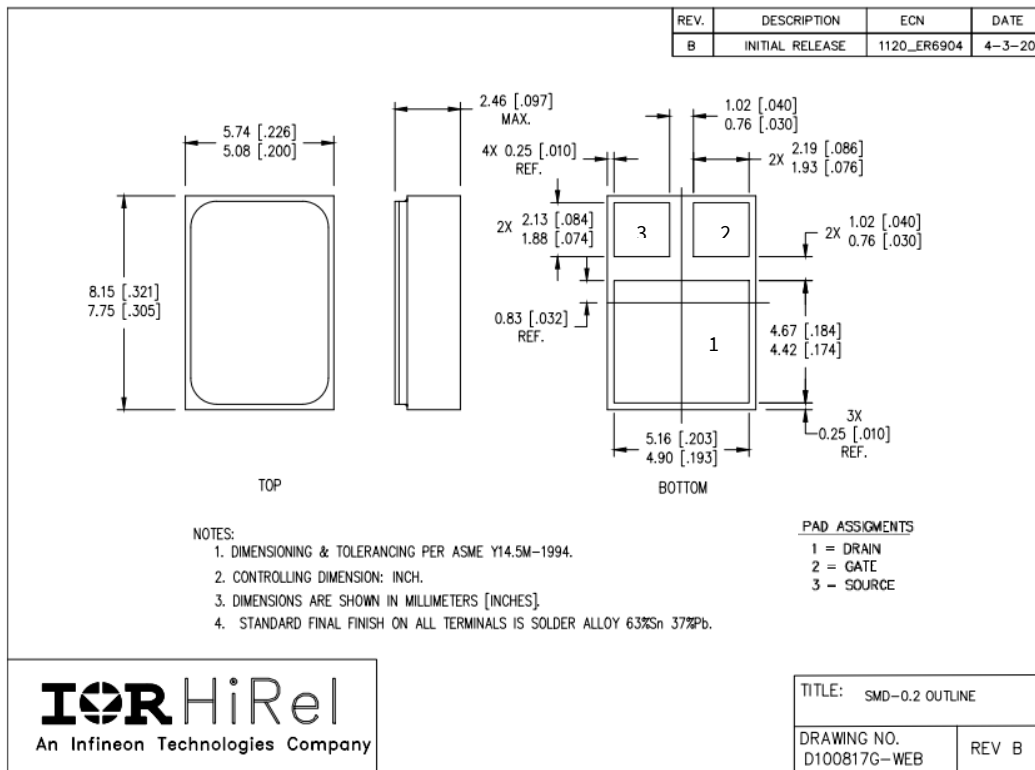
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Radiation Hardened Power MOSFET Surface-Mount (SMD-0.2)

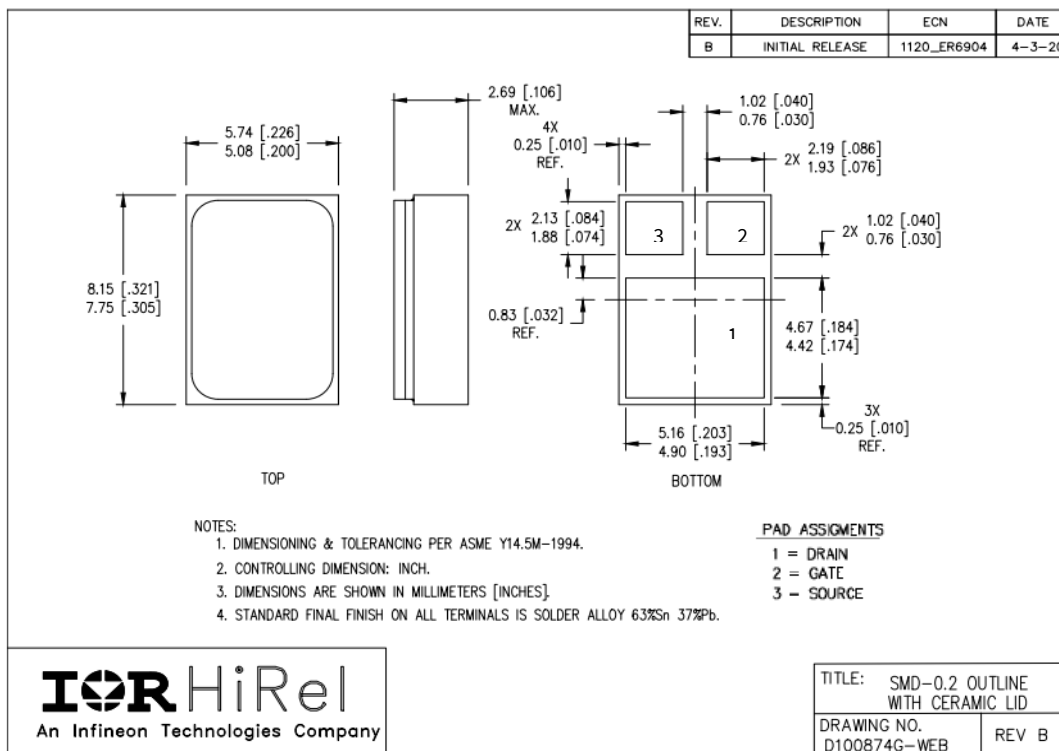
Package Outline

5 Package Outline

Note: For the most updated package outline, please see the website: [SMD-0.2 \(Metal Lid\)](#)



Note: For the most updated package outline, please see the website: [SMD-0.2 \(Ceramic Lid\)](#)



Revision history**Revision history**

Document version	Date of release	Description of changes
	12/13/2007	Datasheet (PD-97179)
Rev A	12/20/2007	Updated case outline
Rev B	09/03/2010	Updated based on ECN-17186
Rev C	09/30/2019	Updated based on ECN-1120_07435
Rev D	06/30/2022	Updated based on ECN-1120_09060

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