General Features

- Operational from 9.9 Gbps to 11.32 Gbps
- Built-In Self Test (BIST) with Error Counter
- On-chip High-Frequency PLLs for Clock Recovery and Clock Generation
- 16-bit LVDS Parallel Data Path
- TX and RX Lock Detect Indicators
- Reference Loop Timing Modes
- Line and Diagnostic Loopback Mode for Faulty Node Identification
- -40°C to 85°C Industrial Temperature Range
- Supports MDIO, I2C and SPI serial interface
- Complies with applicable OIF SFI-4 Phase 1, Telcordia/ ITU-T, 300-pin MSA, IEEE 802.3ae and XFP MSA Standards
- 2000 V ESD rating, 1500 V on high speed inputs
- 15 x 15 mm, 0.8 mm pitch package with RoHS compliant lead free option.
- 1.1 W typical
- JTAG support

Transmitter Features

- Reference Clock Frequency Selection: Divide by 16, 64 or 66 of the TX rate; for example (644.53 MHz, 161.13 MHz or 156.25 MHz) for 10GE TX rate
- Internal, Self-Initializing FIFO to Decouple Transmit Clocks
- Programmable TSD Output Differential Swing
- 10 G Transmitter Serial Clock Output
- Duo Binary Encoding
- Transmitter De-Emphasis

Receiver Features

- LOS/RSSI
- ISI compensation. Tolerates additional 350 ps/nm of chromatic dispersion with an OSNR penalty of 1.0dB over a traditional demux
- Tolerates up to 34” of Standard FR-4 Material
- Adaptive Post-Amplifier Offset Adjust
- Phase Adjust of -0.11 to +0.085 UI
- Reference Clock Frequency Selection: Divide by 16, 64 or 66 of the RX rate; for example (644.53 MHz, 161.13 MHz or 156.25 MHz) for 10GE RX rate
- Capability to Interface with Single-Ended or Differential TIAs (Center Tap Option)
- Input Sensitivity of 10 mV p-p (one wire or two wire) at 10^{-12} BER

Applications

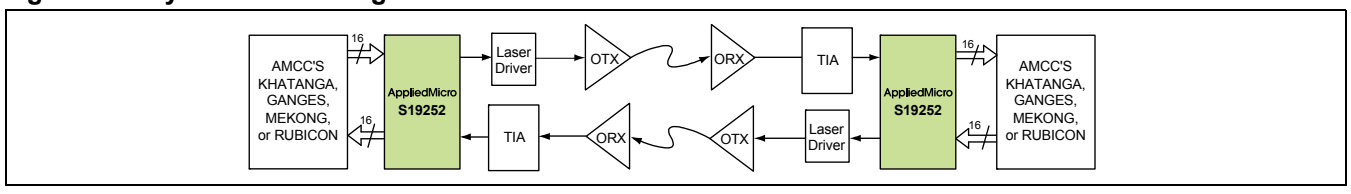
- SONET/SDH and 10GbE-Based Transmission Systems & Modules
- Section Repeaters
- Add Drop Multiplexers (ADM)
- Broad-Band Cross-Connects
- Fiber Optic Test Equipment

General Description

The S19252 MUX/DeMux chip is a fully integrated serialization/de-serialization SONET STS-192/ 10 GB Ethernet/Fiber Channel transceiver with Electronic Dispersion Compensation (EDC). This device can be used to compensate channel impairments caused by Single Mode Fiber (SMF) and copper medium. The chip performs all necessary parallel-to-serial and serial-to-parallel functions in conformance with SONET/SDH, 10 Gigabit Ethernet (10 GbE) and 10 Gigabit Fibre Channel (10 G FC) transmission standards. Figure 1, shows a typical network application. The other application block diagrams are shown in Figures 2, 3 and 4.

On-chip clock synthesis PLL components are contained in the S19252 chip, allowing the use of a slower external transmit clock reference. The chip can be used with 155.52 MHz or 622.08 MHz (or equivalent FEC/10 GbE/10 G FC rates) reference clocks, in support of existing system clocking schemes. The low-jitter LVDS interface guarantees compliance with the bit-error rate requirements of the Telcordia and ITU-T standards.

Figure 1: System Block Diagram



Data Sheet Type

NOTICE: THIS IS A "RELEASED" SPECIFICATION

This document is a **RELEASED** specification for a device under development by AppliedMicro:

- Specifications in this document are not guaranteed to be the latest and are subject to change.
- This data sheet may be superseded by a future revision. Always confirm with AppliedMicro that you are using the latest version.
- Please consult and register for documentation updates from AppliedMicro's external website via the AppliedMicro's MyProduct subscription updates page: https://www.AppliedMicro.com/MyAMCC/jsp/secure/alertSubscriptions/my_product_list.jsp.

Data Sheet Type	Definition
CONCEPT	Concept Specifications are made available for products ideas that are being marketed to obtain customer feedback.
ADVANCE	Advance Specifications are made available for products that are in the engineering development cycle. General samples are not yet available for these products and the specifications, including pin lists and functional descriptions, may change at any time WITHOUT NOTICE.
PRELIMINARY	Preliminary Specifications are made available for products that have been released for general sampling by AppliedMicro (known as Sample Release (SR)). The SR milestone indicates that device samples and evaluation kits may made available upon request. Preliminary device characterization and evaluation has also been completed by AppliedMicro. Known device errata's will be published and dispositioned upon SR. Device specifications may still change WITHOUT NOTICE.
RELEASED	Released Specifications are made available for products that have passed AppliedMicro's Production and Qualification Testing. Although Released Specifications are expected to never change, occasional clean-up changes may be made throughout the remaining product life cycle.

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S19252 Overview

The S19252 transceiver incorporates SONET/SDH/10 GbE/10 G Fibre Channel serialization and deserialization functions. This chip can be used to implement the front end of SONET/10 GbE/10 G Fibre Channel equipment, which consists primarily of the serial transmit interface and the serial receive interface. The chip includes parallel-to-serial, and serial-to-parallel conversion and system timing.

The sequence of operations is as follows:

Transmitter Operations:

1. 16-bit parallel input
2. Parallel-to-serial conversion
3. Serial data output
4. At rate transmitter clock output

Receiver Operations:

1. Serial input to limiting post-amp
2. Inter Symbol Interference (ISI) compensation
3. Threshold adjustment
4. Clock and Data recovery
5. Phase adjustment for improved BER
6. Serial-to-parallel conversion
7. 16-bit parallel data and clock output

Figure 2: Mid-Plane Application Block Diagram

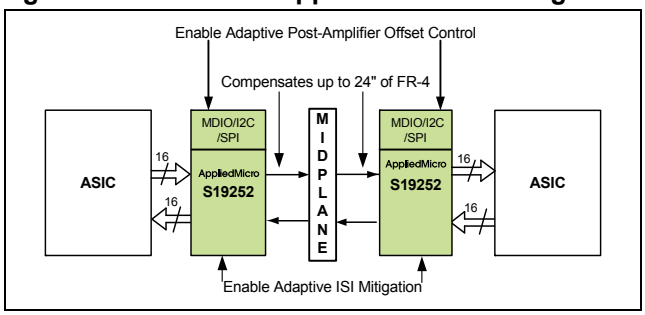


Figure 3: XFP Application Block Diagram

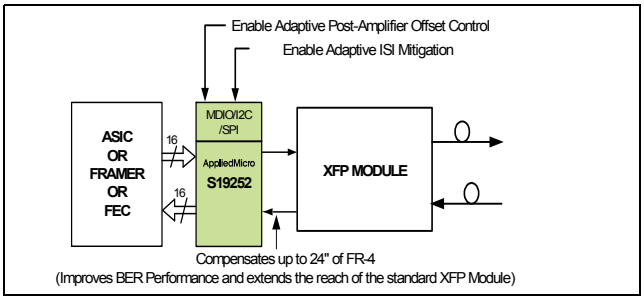
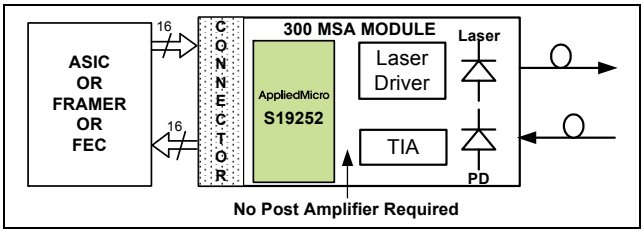


Figure 4: 300 MSA Application Block Diagram



Suggested Interface Devices

AppliedMicro	GANGES II (S19202CBI20)	STS-192 POS/ATM SONET/SDH Mapper
AppliedMicro	RUBICON (S19227)	OC-192/48/12/3 DW/FEC/PM and ASYNC Mapper Device with Strong FEC
AppliedMicro	MEKONG (S19204)	STS-192 Pointer Processor
AppliedMicro	KHATANGA (S19205)	STS-192c SONET/SDH Framer/ Mapper with Integrated MAC

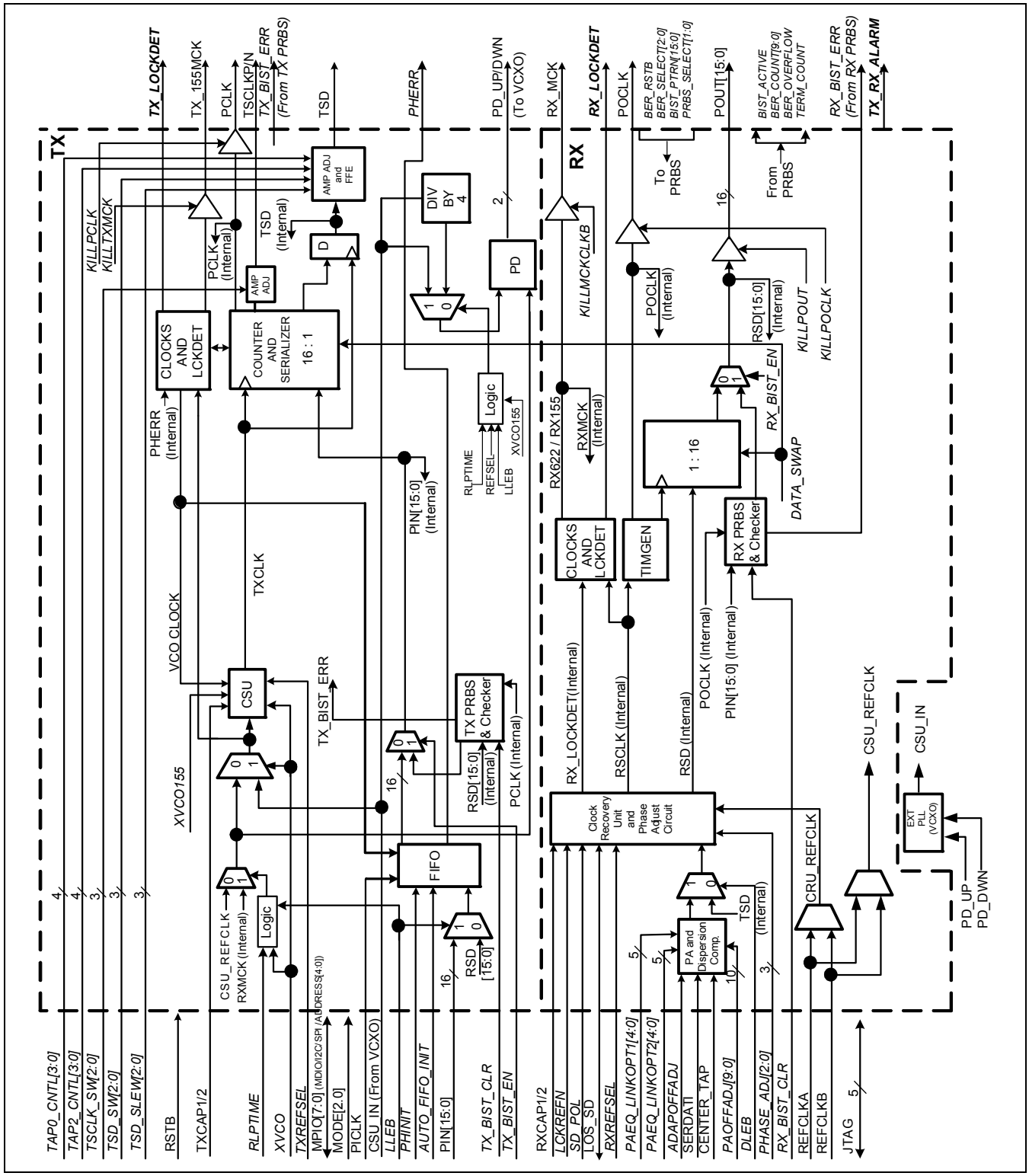
Standards Compliance List

Standard	Revision	Date
300 Pin MSA for 10G Transponders	Edition 4	August 14, 2002
GR-253-CORE SONET Jitter Specifications	Issue 4.0	December 2005
IEEE Draft P802.3ae/	-	August 30, 2002
XFP MSA (XFI Electrical- High Speed outputs)	Rev 4.0	April 13, 2004
SFF-8431 [1] (SFP+ Host Serdes)	Rev 1.3	February 16, 2007
Fibre Channel Physical Interfaces (FC-PI-2)	Rev 4.1	March 24, 2004
OIF SFI4 Phase 1 [2] Parallel Interface	Rev 1.0	September 26, 2000

1. See SFP+ Jitter Performance, Table 28 for transmitter conditional compliance.
2. See LVDS Characteristics, Table 35 for Input Level conditional compliance.

Standard Compliance only relates to applicable sections pertaining to this product type.

Figure 5: Transceiver Functional Block Diagram



Normal Font – External Pin Access Only
Italics Font – Serial Bus Register Access Only
Italics and Bold Font – External Pin And Serial Bus Register Access

Transmit Input Pin Description

Parallel Input Data (PINP/N[15:0]) – External Pin

PINP/N[15:0] is the LVDS parallel data input bus which is multiplexed 16:1 and transmitted serially at STS-192/10 GbE/10G FC rates. This data is aligned with the Parallel Input Clock (PICLKP/N). Bit 15 is the Most Significant Bit (MSB). This bus is typically connected to a framer, mapper or digital wrapper (e.g. GANGES, or RUBICON). These inputs are internally terminated 100 Ω line-to-line and are either internally biased for AC coupling or DC level shifted for DC coupling. See LVDS_INPUT_AC_EN control description.

Parallel Input Clock (PICLKP/N) – External Pin

PICLKP/N is the LVDS 622.08 MHz (or equivalent FEC/10 GbE/10G FC Rate) input clock to which the Parallel Input Data (PINP/N[15:0]) is aligned. PICLKP/N is a delayed version of the PCLK. This clock is used to clock the data into the S19252 FIFO. These inputs are internally terminated 100 Ω line-to-line and are either internally biased for AC coupling or DC level shifted for DC coupling. See LVDS_INPUT_AC_EN control description.

LVDS Input AC Enable (LVDS_INPUT_AC_EN) – Register

The LVDS_INPUT_AC_EN is an active high input which selects between AC or DC coupling for the PINP/N[15:0] and PICLKP/N (LVDS) inputs. When active (default), the LVDS inputs will provide bias for AC coupled inputs. When disabled the LVDS inputs will provide DC level shifting for DC coupled inputs.

TX Ref. Select (TXREFA_NOTB) – Register

The TXREFA_NOTB is the active high input which selects between REFCLKAP/N or REFCLKBP/N reference clock input. When the TXREFA_NOTB is active (default), the REFCLKAP/N is selected to be the input for the TX Reference Frequency for the Clock Synthesis Unit (CSU). If the TXREFA_NOTB is inactive, the REFCLKBP/N is used as the reference clock source for the CSU. See Table 1. This input is only accessible through the serial bus registers.

Table 1: Transmit Reference Source Select

TXREFA_NOTB	Reference Clock Source
1	REFCLKAP/N
0	REFCLKBP/N

SONET Rate Select (SONET_RATESEL) – Register

SONET Rate Select. When active, the device is operating at SONET rate. When inactive, it is operating at either 10 G FC or GbE rate.

GbE Rate Select (GBE_RATESEL) – Register

GbE Rate Select. When active, the device is operating at 10 GbE or FC rate. The signal is only functional when SONET_RATESEL is inactive.

TX Ref. Rate Select (TXREFSEL) – Register

The TX Reference Rate Select (TXREFSEL) input selects between a 155.52 MHz or 622.08 MHz (or equivalent FEC/10 GbE/10G FC rate) reference clock. When SONET_RATESEL is inactive, and GBE_RATESEL is active, 10 GE reference (156.25 MHz) or FC reference (159.375 MHz) is used. When the SONET_RATESEL is active, and TXREFSEL is inactive, the common reference 155 MHz clock is used; if TXREFSEL is set active, then 622 MHz is used. See Table 2, Transmit Reference Rate Select for the CSU. These inputs are only accessible through the serial bus registers.

Table 2: Transmit Reference Rate Select

TX REF SEL	SONET_ RATE SEL	GBE_ RATE SEL	Reference Clock (MHz) and Rate Multiplier
X	0	1	(10GE) 156.25 or (FC) 159.375 (or equiv. FEC rate) x66
0	1	X	155 (or equiv. FEC rate) x64
1	1	X	622 (or equiv. FEC rate) x16

Note that the source of TXREFCLK is either REFCLKA or REFCLKB. The default is REFCLKAP/N.

CSU Ref. Clock (REFCLKAP/N) – External Pin

The differential CML Reference Clock (REFCLKAP/N by default) input is used to drive the clock synthesizer Phase Lock Loop (PLL). See Table 3, *Reference Frequency (CSU REFCLK) for the Clock Synthesis Unit* and for the recommended FEC rates. The REFCLKAP/N input may go into the Phase Detector (PD) block shown in Figure 5. The output of the PD block (PD_UP/PD_DOWN) can be fed into an External filter and Voltage Controlled Oscillator (VCO) to clean up the REFCLKAP/N for improved jitter generation. The output of the external VCO is fed into the CSU_IN input. The CSU_IN will act as the reference clock for the CSU block if XVCO select input is active. Table 3 summarizes the increased CSU_REFCLK rates required for FEC/10GbE/10G FC operation. The S19252 incorporates the bandwidth expansion requirements needed for the FEC applications that provide up to eight bytes of correction for a 255 byte block. Increased CSU REFCLK frequency is required for bandwidth expansion due to code words and Frame Synchronization Byte (FSB). This input is internally biased and terminated and must be AC coupled.

External Voltage Controlled Oscillator (XVCO) – Register

The XVCO is the active high control input that selects CSU_IN as the reference clock for the CSU block. When active, the CSU_IN (output of the external VCO) input is used as the reference clock for the CSU for improved jitter generation. When inactive and in the normal mode, the CSU_REFCLK is directly used as the reference clock for the CSU block. This input is only accessible through the serial bus register.

Transmitter Reset (TX_RSTB) – Register

The active low Transmitter Reset (TX_RSTB) signal, when asserted low, will reset the CSU and associated logic. Use this reset after all Transmitter CSU and REFCLK control changes. When this bit is high (default) the CSU will function normal. This input is only accessible through the serial bus register.

External Voltage Controlled Oscillator 155 MHz (XVCO155) – Register

The XVCO155 is the active high control for selecting either a 622 MHz (or equiv. FEC/10 GbE/10 GFC) or 155 MHz (or equiv. FEC/10 GbE/10 GFC) external VCO Frequency. When this bit is low (default), the XVCO operates at 622 MHz. When this bit is high, the XVCO operates at 155 MHz. This input is only accessible through the serial bus register.

Kill Transmitter 155MCK Clock Output (KILLTXMCK) – Register

The active high Kill Transmitter 155MCK clock output (KILLTXMCK) signal, when asserted high, will force the TX_155MCK clock output to a logic state determined by the CLKSTOP_VAL. When this bit is low (default) the TX_155MCK will function normal. This input is only accessible through the serial bus register.

Kill Transmitter PCLK Output Clock (KILLPCLK) – Register

The active high Kill Transmitter PCLK output clock (KILLPCLK) signal, when asserted high, will force the PCLK clock output to a logic state determined by the CLKSTOP_VAL. When this bit is low (default) the PCLK will function normal. This input is only accessible through the serial bus register.

Kill Transmit Serial Data Output (KILLTXDATB) – Register

The active low Kill Transmitter Serial Data output (KILLTXDATB) signal, when asserted low, will force the TSD data output pins to a logic state determined by the TSD_SQ_POL. When this bit is high (default) the TSD output will function normal. This input is only accessible through the serial bus register.

Table 3: Reference Frequency (CSU REFCLK) for the Clock Synthesis Unit

TXREF SEL	SONET_ RATE SEL	GBE_ RATE SEL	Mode Description	REFCLK Multiplier / Rate Expansion	Serial Data Output Frequency (Gbps) [1]	Required CSU REFCLK Frequency (MHz) [2]
0	1	X	STS-192, 0 bytes	64 / 0%	9.95328	155.52
0	1	X	STS-192, Reed Soloman - 255/238	64 / 7.14%	10.664	166.63
0	1	X	STS-192, Reed Soloman - 255/237	64 / 7.59%	10.709	167.33
0	1	X	10 Gigabit Ethernet	64 / 0%	10.000	156.25
0	0	1	10 Gigabit Ethernet 64/66B Encoded	66 / 3.125%	10.3125	156.25
0	1	X	10 Gigabit Ethernet 64/66B Encoded	64 / 3.125%	10.3125	161.13
0	1	X	10 Gigabit Ethernet 64/66B Encoded - 255/238	64 / 7.14%	11.0491	172.642
0	1	X	10 Gigabit Ethernet 64/66B Encoded - 255/237	64 / 7.59%	11.0957	173.37
0	0	1	10 G Fibre Channel	66 / 0%	10.51875	159.375
0	1	X	10 G Fibre Channel	64 / 0%	10.51875	164.355
0	1	X	10 G Fibre Channel, Reed Soloman- 255/238	64 / 7.14%	11.27	176.096
0	1	X	10 G Fibre Channel, Reed Soloman- 255/237	64 / 7.59%	11.3176	176.838
1	1	X	STS-192, 0 bytes	16 / 0%	9.95328	622.08
1	1	X	STS-192, Reed Soloman - 255/238	16 / 7.14%	10.664	666.514
1	1	X	STS-192, Reed Soloman - 255/237	16 / 7.59%	10.709	669.327

1. Refer to CSU and CRU VCO Specifications in Table 28 for CSU VCO frequency range selection.
2. All Serial Data Rates shown for divide by 64 REFCLKs could also use divide by 16 REFCLKS by setting TXREFSEL to 1.

The BOLD CELLS denote the default state

Clock Synthesizer Input (CSU_INP/N) – External Pin

The clock synthesizer input is the differential REFCLK CML input to the internal CSU. This input is typically driven from an external VCO, which is controlled by an external loop filter and the internal phase detector output (PD_UP, PD_DWN). CSU_IN will be used as the reference clock for the CSU block when XVCO control input is active. The S19252 should have low jitter generation when CSU_IN is used as the reference clock in conjunction with the internal phase detector output. The CSU_IN jitter generation will be as good as one could expect from a clean external CSU_REFCLK. See Figure 20 and 21 for details. This input is internally biased and terminated and must be AC coupled.

Case 1. XVCO Select Input is Inactive – In this mode, the external VCO is bypassed. The output of the internal phase detector (PD block shown in Figure 5) is not used. The TXREFSEL input selects either the 155.52 MHz or 622.08 MHz reference frequency (CSU REFCLK input) for SONET/SDH applications. Accordingly, the CSU operates in the 155.52 MHz or 622.08 MHz CSU REFCLK mode. **Case 2. XVCO Select Input is Active** – In this mode, the external VCO is used. The output of the phase detector block (PD_UP/DWN) is fed into the external filter/VCO. The output of the external VCO is fed into the CSU_IN input. Setting the XVCO155 control register to a logic high will select a 155.52 MHz external VCO otherwise the external VCO would be 622.08 MHz with XVCO155=0 (default).

TXREFSEL input should be programmed to logic low when CSU REFCLK = 155.52 MHz. This enables the CSU_IN divide by four (622.08 MHz Divide by four = 155.52 MHz) to go into one of the Phase Detector (PD) inputs. The 155.52 MHz CSU_REFCLK directly goes into the second PD input. TXREFSEL should be programmed to logic high when CSU REFCLK = 622.08 MHz. This would enable the CSU_IN (622.08 MHz output of the external VCO) directly into one of the Phase Detector (PD) inputs. The 622.08 MHz CSU REFCLK goes directly into the second Phase Detector (PD) input. See Table 4, *Reference Frequency with External VCO Selected*. Note that XVCO mode is not supported when GBE_RATSEL=1. This input is only accessible through the serial bus register.

TX Loop Filter (TXCAP1, TXCAP2) – External Pin

The transmit clock synthesizer unit external loop filter capacitor and resistors are connected to these pins. These devices should be surrounded by a ground shield. The component values are as stated in Table 38, *Transmit and Receive External Loop Filter Components*.

Phase Initialization (PHINIT) – Register

The active high Phase Initialization (PHINIT) input is an asynchronous input that initializes the internal phase adjust circuit for the transmitter FIFO. When active, this input will align the PICLK and the internally generated PCLK. When AUTO_FIFO_INIT is not enabled, PHINIT must be asserted if the PHERR signal is active which indicates potential internal setup/hold timing violations. See *Figure 28*, *FIFO Initialization*. This input is only accessible through the serial bus register.

Table 4: Reference Frequency with External VCO Selected

XVCO	XVCO155	SONET_RATSEL	TXREFSEL	CSU REFCLK	CSU_IN Frequency	CSU Mode
1	0	1	1	622.08 MHz	622.08 MHz	622.08 MHz
1	0	1	0	155.52 MHz	622.08 MHz	622.08 MHz
1	1	1	0	155.52 MHz	155.52 MHz	155.52 MHz
1	1	1	1	622.08 MHz	155.52 MHz	155.52 MHz

The BOLD CELLS denote the default state

Automatic FIFO Initialization (AUTO_FIFO_INIT) – Register

This active high control input internally connects the transmit FIFO signals (PHERR output and PHINIT input) and automatically initializes the FIFO in case of a PCLK/PICLK set-up or hold time violation. This input is only accessible through the serial bus register.

Transmit Built-In Self Test Enable (TX_BIST_EN) – Register

This active high input enables the transmit built-in self test mode. For normal system operation, TX_BIST_EN should be programmed to logic low. The S19252 goes in the BIST mode when TX_BIST_EN is programmed to logic high. Once the TX_BIST_EN is programmed to logic high, the PRBS generator will start sending the PRBS/user defined pattern (see Table 13 for details). The checker will be activated but will not start checking for the valid data pattern until RX_LOCKDET is active. This function is accessible through the serial bus register. Note - While TX BIST is enabled the parallel input bus will not provide a TX_DATA_SWAP even if TX_DATA_SWAP is enabled.

Transmit Built-In Self Test Clear (TX_BIST_CLR) – Register

This active high level sensitive input clears the transmit built-in self test error (TX_BIST_ERR). For normal system operation, TX_BIST_CLR should be programmed to logic low. The TX_BIST_ERR flag can be cleared by asserting the TX_BIST_CLR in the BIST mode or by resetting (RSTB) the S19252. TX_BIST_CLR is an active high level sensitive input. In order for the transmit checker to clear the TX_BIST_ERR flag, TX_BIST_CLR must be asserted high. This input is only accessible through the serial bus register.

Parallel Input Data Bus Swap (TX_DATA_SWAP) – Register

This input reverses the order of the parallel input data bus (PINP/N[15:0]). This makes routing easier with configurations requiring Data Bus bit order reversal.

AppliedMicro recommends that DATA_SWAP input be programmed to logic low (Default) when S19252 is used with the 300-pin MSA connector. The S19252 should be placed on the top side of the module when used with the 300-pin MSA connector. See Table 22 for details. This input is only accessible through the serial bus register. TX BIST results are invalid while TX_DATA_SWAP is enabled.

Transmit Output Pin Description

Transmit Serial Data (TSDP/N) – External Pin

The differential High Speed CML Transmit Serial Data (TSDP/N) output is the serialized version of the incoming parallel data stream. This output is typically used to drive the laser driver.

Parallel Clock (PCLKP/N) – External Pin

The LVDS Parallel Clock (PCLKP/N) output is a 622.08 MHz (or equivalent FEC/10 GbE/10 GFC rates) internally generated clock output used to coordinate parallel data transfers with upstream logic. The PCLKP/N is directly derived from the CSU REFCLKP/N in the normal operating mode. PCLK is the divided-down version of the internal TXCLK. PCLK is used to clock data out of the upstream devices (framer/mapper). PCLK is also used internally to clock data from the FIFO into the parallel-to-serial shift register. See Table 35 for LVDS termination.

155.52 MHz Clock Output (TX_155MCKP/N) – External Pin

The LVDS 155.52 MHz Clock Output (or equivalent FEC/10 Gigabit Ethernet rate) TX_155MCKP/N pin is an internally generated clock output used to drive the reference clock input of the receive section of the S19252 in the normal mode of operation. The TX_155MCKP/N cannot be used as the reference clock for the receive section of the S19252 in the RLPTIME. See Table 35 for LVDS termination.

Transmit Lock Detect (TX_LOCKDET) – Register and External Pin

The active high transmit Lock Detect is an LVCMOS output. This asynchronous output will be active high once the internal PLL has locked to the clock provided on the CSU REFCLK input. The TX_LOCKDET output goes active (high) when the PCLK is within 500 ppm from the CSU REFCLK. This output can be accessed through the serial bus register and through an external LVCMOS pin.

Phase Error (PHERR) – Register

Phase Error is an active high output. To prevent errors caused by short set-up or hold times between the PICLK and internally generated PCLK, the timing generator circuitry monitors the phase relationship between the two clock domains. The Phase Error (PHERR) signal will be asserted high at the start of the PCLK cycle for which there may be setup/hold timing violations between the PICLK and internal byte clock (PCLK) timing domains. Since PHINIT will initialize the FIFO if a high level is held for at least 50 ns, the FIFO will be initialized if PHERR is connected to PHINIT on the serial bus. This output is only accessible through the serial bus register.

Phase Detector Output (PD_UP, PD_DWN) – External Pin

These Phase Detector CML signals are the output of an internal phase detector which may be used to reduce jitter from an incoming CSU REFCLK or from an internally recovered clock used in loopback modes. This output is typically used to drive an external loop filter, which in turn controls a VCO that has its output feeding the CSU_IN input. The internal phase detector, with the loop filter and VCO, form a PLL which may be used to remove jitter from CSU_REFCLK or internal POCLK.

Transmit Built-In Self Test Error (TX_BIST_ERR) – Register

Active high transmit built-in self test error (TX_BIST_ERR) signal indicates a bit error in the transmit built-in self test loop. After the transmit checker is initialized, it will compare the parallel data output with the calculated pattern. If the parallel data output does not match the calculated pattern, the TX_BIST_ERR flag will be set active. The TX_BIST_ERR flag can be cleared by asserting TX_BIST_CLR in the TX_BIST_EN mode or by resetting (RSTB) the S19252. The TX_BIST_ERR can also be cleared with a rising edge of TX_BIST_EN. This output is only accessible through the serial bus register.

Receive Input Pin Description

Serial Data In (SERDATIP/N) – External Pin

The Serial Data In (SERDATIP/N) pins are the differential high Speed CML inputs. They receive inputs from an optics module or other upstream logic device. The S19252 extracts the clock from the SERDATIP/N inputs and provides a recovered clock (internal RSCLK) with re-timed parallel data. See Figure 28 for the SERDATIP/N termination scheme. The SERDATIP/N is internally terminated 100 Ω line-to-line (50 Ω + 50 Ω with center tap capacitor). The two 50 Ω resistors are center-tapped with a 25 pF capacitor for use in single-ended applications. The SERDATIP/N inputs must be AC coupled. These pins are internally biased and terminated 100 Ω line-to-line.

SERDATIP/N Internal Termination (CENTER_TAP) – External Pin

The SERDATIP/N is internally terminated with two 50 Ω resistors in series. The two 50 Ω resistors are center-tapped with an internal 25 pF capacitor to Ground. The input to the capacitor can be directly accessed through the CENTER_TAP pin. This input should be connected to an external broadband 0.01 μF capacitor to ground if driven single-ended or differential. This termination scheme enables the S19252 to be driven in the single-ended mode and offers better common mode noise rejection. See Figure 32 for the SERDATIP/N termination scheme.

Receive Loop Filter (RXCAP1, RXCAP2) – External Pin

The CRU external loop filter capacitor and resistors are connected to the RXCAP1 and RXCAP2 pins. These devices should be surrounded by a ground shield. Component values should be as stated in Table 41, *Transmit and Receive External Loop Filter Components*.

Receiver Reset (RX_RSTB) – Register

The active low Receiver Reset (RX_RSTB) signal, when asserted low, will reset the PA/CRU and associated logic. Use this reset after all Receiver VCO and REFCLK control changes. When this bit is high (default) the PA and CRU will function normal. This input is only accessible through the serial bus register.

Lock-to-Reference (LCKREFN) – Register

The active low Lock-to-Reference (LCKREFN) input register, when asserted low, will force the PLL to lock to the Reference Clock defined by the RXREFSEL and de-assert RX_LOCKDET. The POCLKP/N will lock to the reference clock in this mode. When the LCKREFN is inactive (high), the POCLKP/N will lock to the valid incoming serial data (SERDATIP/N). This input should be programmed to logic high for normal operation. This input is only accessible through the serial bus register.

LOS/Signal Detect (LOS_SD) – External Pin

This is a dual-purpose pin that can be either an input or output pin, the I/O function is controlled by setting LOS_SDC bit via serial bus. When the LOS_SDC is set to '0', this pin will be a Signal Detect input pin. The default of this pin is a Signal-Detect input pin.

The Signal-Detect is an active high or active low LVCMOS single-ended input to be driven by the external optical receiver module to indicate the presence of received optical power. Signal Detect active level (high or low) is programmed by the SD_POL.

As an output pin, by setting the LOS_SDC to '1' and the RX_LOS_CNTL to '1', this pin will act as a Loss-of-Signal (LOS) output pin. When the SD_POL is set to '1', the LOS_SD will be active high.

When a loss-of-light condition occurs, a de-asserted Signal-Detect (LOS_SD) input pin or an asserted Loss-of-Signal (LOS_SD) output pin will cause the internal PLL to be locked to the CRU reference input signal and if, the squelch function is enabled (default), the SERDATIP/N (and POUT[15:0]) will be forced to a Logic '0' state.

Signal Detect Polarity (SD_POL) – Register

The signal detect polarity is an input signal that will set the LOS_SD input as either active high or active low. Setting this pin low will set the LOS_SD input as active low. Setting this pin high will set the LOS_SD input as active high. This input is only accessible through the serial bus register.

RX Ref. Select (RXREFA_NOTB) – Register

The RX Reference Select (RXREFA_NOTB) input selects between REFCLKAP/N or REFCLKBP/N reference clock input. When the RXREFA_NOTB is set low (default), the REFCLKBP/N is selected to be the input for the Receiver Reference Frequency for the Clock Data Recover Unit (CRU). When this bit is set high, the REFCLKAP/N is used as the CRU reference frequency input. This input is only accessible through the serial bus registers.

Table 5: Receive Reference Source Select

RXREFA_NOTB	Reference Clock Source
1	REFCLKAP/N
0	REFCLKBP/N (Default)

Receive Reference Rate Select (RXREFSEL) – Register

This is the receive reference rate select input. When SONET_RATESEL is low, and GBE_RATESEL is high denotes that the 10 GE reference (156.25 MHz) or FC reference (159.375 MHz) is used. When SONET_RATESEL is high, the RXREFSEL low indicates that the 155 MHz clock is used; and while high 622 MHz clock is used. See Table 6. This input is only accessible through the serial bus register.

Table 6: Receive Reference Rate Select

RX REF SEL	SONET_ RATE SEL	GBE_ RATE SEL	Reference Clock (MHz) and Rate Multiplier
X	0	1	(10GE) 156.25 or (FC) 159.375 (or equiv. FEC rate) x66
0	1	X	155 (or equiv. FEC rate) x64
1	1	X	622 (or equiv. FEC rate) x16

Note that the source of RXREFCLK is either REFCLKA or REFCLKB. The default is REFCLKBP/N.

CRU Reference Clock (REFCLKAP/N) – External Pin

The differential REFCLK CML 155.52 MHz (or equivalent FEC/10 Gigabit Ethernet Rate) reference clock (CRU REFCLKP/N) input is used to establish the initial operating frequency of the Phase Lock Loop (PLL). This input can also be driven by the 155MCKP/N output from the transmit section of S19252. Table 7 summarizes the settings and increased CRU REFCLK rates required for the FEC operation. The S19252 incorporates the bandwidth expansion requirements needed for FEC/10 GB Ethernet applications that provide up to eight bytes of correction per 255 byte block. Increased CRU_REFCLK frequency is required for bandwidth expansion due to code words and Frame Synchronization Byte (FSB). This input is internally biased and terminated 100 Ω line-to-line and must be AC coupled.

Table 7: Reference Frequency (CRU REFCLK) for the Clock and Data Recovery Unit

RXREF SEL	SONET_ RATE SEL	GBE_ RATE SEL	Mode Description	REFCLK Multiplier / Rate Expansion	Serial Data Input Frequency (Gbps) [1]	Required CRU REFCLK Frequency (MHz) [2]
0	1	X	STS-192, 0 bytes	64 / 0%	9.95328	155.52
0	1	X	STS-192, Reed Soloman - 255/238	64 / 7.14%	10.664	166.63
0	1	X	STS-192, Reed Soloman - 255/237	64 / 7.59%	10.709	167.33
0	1	X	10 Gigabit Ethernet	64 / 0%	10.000	156.25
0	0	1	10 Gigabit Ethernet 64/66B Encoded	66 / 3.125%	10.3125	156.25
0	1	X	10 Gigabit Ethernet 64/66B Encoded	64 / 3.125%	10.3125	161.13
0	1	X	10 Gigabit Ethernet 64/66B Encoded - 255/238	64 / 7.14%	11.0491	172.642
0	1	X	10 Gigabit Ethernet 64/66B Encoded - 255/237	64 / 7.59%	11.0957	173.37
0	0	1	10 G Fibre Channel	66 / 0%	10.51875	159.375
0	1	X	10 G Fibre Channel	64 / 0%	10.51875	164.355
0	1	X	10 G Fibre Channel, Reed Soloman- 255/238	64 / 7.14%	11.27	176.096
0	1	X	10 G Fibre Channel, Reed Soloman- 255/237	64 / 7.59%	11.3176	176.838
1	1	X	STS-192, 0 bytes	16 / 0%	9.95328	622.08
1	1	X	STS-192, Reed Soloman - 255/238	16 / 7.14%	10.664	666.514
1	1	X	STS-192, Reed Soloman - 255/237	16 / 7.59%	10.709	669.327

1. Refer to CSU and CRU VCO Specifications in Table 28 for CRU VCO frequency range selection.
2. All Serial Data Rates shown for divide by 64 REFCLKs could also use divide by 16 REFCLKS by setting RXREFSEL to 1.

Kill Parallel Output Clock (KILLPOCLK) – Register

The active high Kill Parallel Output Clock (KILLPOCLK) signal, when asserted high, will force the POCLK output to a state specified by the CLKSTOP_VAL register bit. This input may be programmed to logic '0' for normal operation. This input is only accessible through the serial bus register.

Kill Parallel Output Data (KILLPOUTB) – Register

The active low Kill Parallel Output Data (KILLPOUTB) signal, when asserted low, will force the POUT[15:0] output to a logic '0' state. This input may be programmed to logic '1' for normal operation. This input is only accessible through the serial bus register.

Kill Parallel Output MCK Clock (KILLRXMCK) – Register

The active high Kill Parallel Output 622MCK Clock (KILLRXMCK) signal, when asserted high, will force the 622MCK output to a state specified by the CLKSTOP_VAL register bit. This input may be programmed to logic '0' for normal operation. This input is only accessible through the serial bus register.

Receive Built-In Self Test Enable (RX_BIST_EN) – Register

This active high input enables the receive built-in self test mode. For normal system operation, RX_BIST_EN should be programmed to logic '0'. The S19252 goes in the BIST mode when RX_BIST_EN is programmed to logic high. Once the RX_BIST_EN is programmed to logic high, the PRBS generator will start sending the PRBS/user defined pattern (see Table 13 for details) through the parallel outputs, and the checker will be activated but will not start checking for the valid data pattern until TX_LOCKDET is active. This input is only accessible through the serial bus register. *Note* - While RX BIST is enabled the parallel output bus will not provide a RX_DATA_SWAP even if RX_DATA_SWAP is enabled.

Receive Built-In Self Test Clear (RX_BIST_CLR) – Register

This active high level sensitive input clears the receive Built-In Self Test Error (RX_BIST_ERR). For normal system operation, RX_BIST_CLR should be programmed to logic '0'. The RX_BIST_ERR flag can be cleared by asserting RX_BIST_CLR in the BIST mode or by resetting (RSTB) the S19252. RX_BIST_CLR is an active high level sensitive input. In order for the receive checker to clear the RX_BIST_ERR flag, the RX_BIST_CLR must be asserted high. This input is only accessible through the serial bus register.

LOS Threshold Assert (LOS_VTH_AST [7:0]) – Register

The LOS Threshold Assert (LOS_VTH_AST[7:0]) inputs control the LOS assert threshold for the high speed serial input. The 8-bit control register set the LOS assert voltage where the Loss of signal condition is declared. These inputs are only accessible through the serial bus registers

LOS Threshold De-Assert (LOS_VTH_DST [7:0]) – Register

The LOS Threshold De-Assert (LOS_VTH_DST[7:0]) inputs control the LOS de-assert threshold for the high speed serial input. The 8-bit control register set the LOS de-assert voltage where the Loss of signal condition is declared. These inputs are only accessible through the serial bus registers

Phase Adjust (PHASE_ADJ[2:0]) – Register

The Phase Adjust (PHASE_ADJ[2:0]) inputs control the phase offset between the high speed recovered data and clock for improved bit error rate and link budgets. These registers are not adaptively controlled. See Table 8 for details of the phase adjust settings. These inputs are only accessible through the serial bus registers.

Table 8: Phase Adjust Control

Phase Adjust Input (PHASE_ADJ)			
2	**1**	**0**	**Phase Adjustment**
0	0	0	+8.5 ps
0	0	1	+5.5 ps
0	1	0	+2.5 ps
0	**1**	**1**	**0 ps**
1	0	0	-2.5 ps
1	0	1	-5.2 ps
1	1	0	-8.0 ps
1	1	1	-11.0 ps

The BOLD CELLS denote the device default state. The PHASE_ADJ inputs is recommended to be set to “010” state for optimal performance.

Post Amplifier Offset Adjust (PAOFFADJ[9:0]) and Adaptive Post Amplifier Offset Adjust Enable (ADAPOFFADJ) – Registers

The Post-Amp Offset Adjust (PAOFFADJ[9:0]) inputs may be used to compensate for input data signal duty cycle distortion or asymmetrical noise (for example EDFA noise). The PAOFFADJ[9:8] control the step resolution (Δ) of the post-amp offset change. PAOFFADJ[7:0] control the post-amp offset adjustment settings (number of steps = 2^8 = 256). The positive portion of the differential data signal may be relatively offset from the negative by ±78 mV/±39 mV/±28 mV/ ±19 mV with a resolution (Δ) of 0.6 mV/0.3 mV/ 0.22 mV/0.15 mV respectively. See Table 9 for details of the post-amp offset adjust settings.

The ADAPOFFADJ is an active high input that enables the adaptive setting of the offset adjust to enhance the bit error rate. Upon start up with ADAPOFFADJ active, the default value gets loaded onto the PAOFFADJ[9:8] registers. The feedback control loop in the S19252 will find the setting for offset adjustment that yields the best possible bit error rate. When ADAPOFFADJ is disabled, PAOFFADJ[9:0] must be externally controlled to achieve the best possible bit error rate. See Table 10 for details of the adaptive post-amp offset adjust settings.These inputs are only accessible through the serial bus registers.

Table 9: Post-Amplifier Offset Adjust

PAOFFADJ[9:8] Settings for Resolution/Range		
PAOFFADJ9	**PAOFFADJ8**	**Resolution= Δ/± Range**
0	0	0.6mV/±78mV
0	1	0.3mV/±39mV
1	**0**	**0.22mV/±28mV**
1	1	0.15mV/±19mV

PAOFFADJ[7:0] Settings for Offset Adjustment									
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	α	**SERDATIP-SERDATIN =**
0	0	0	0	0	0	0	0	0	-128 * Δ mV
0	0	0	0	0	0	0	1	1	-127 * Δ mV
0	0	0	0	0	0	1	0	2	-126 * Δ mV
0	0	0	0	0	0	1	1	3	-125 * Δ mV
X	X	X	X	X	X	X	X	α	(-128+α)* Δ mV
1	1	1	1	1	1	1	0	254	126 * Δ mV
1	1	1	1	1	1	1	1	255	127 * Δ mV

The BOLD CELLS denote the default state. The default state settings for PAOFFADJ[7:0] may vary from one device to another.

Table 10: Adaptive Post-Amplifier Offset Adjust

ADAPOFFADJ	Adaptive Offset Adjust Control
0	Inactive. (PAOFFADJ[9:0] must be externally controlled for offset adjustment)
1	Active (Set the resolution through PAOFFADJ[9:8]. PAOFFADJ[7:0] are adaptively controlled to enhance BER)

The BOLD CELLS denote the default state

Parallel Output Data Bus Swap (RX_DATA_SWAP) – Register

This input reverses the order of the parallel output data bus (POUTP/N[15:0]). This makes routing easier with configurations requiring Data Bus bit order reversal.

AppliedMicro recommends that DATA_SWAP input be programmed to logic low (Default) when S19252 is used with the 300-pin MSA connector. The S19252 should be placed on the top side of the module when used with the 300-pin MSA connector. See Table 22 for details. This input is only accessible through the serial bus register. While RX BIST is enabled the parallel output bus will not provide a RX_DATA_SWAP even if RX_DATA_SWAP is enabled.

Receive Output Pin Description

Parallel Output Clock (POCLKP/N) – External Pin

The LVDS Parallel Output Clock (POCLKP/N) output is an internally regenerated clock which is used to transfer demultiplexed data from an internal holding register to the output register, which drives the parallel output data bus POUTP/N [15:0]. This clock is synchronized with the parallel output data. According to OIF99.102.5, section 9.0 for an SFI4 phase 1 I/O, the clock edges should align to the data edges in order to simplify the driver macro design for the SERDES and framers (to do this invert the POCLKP/N by swapping the P and N pins). As is the rising edge of the POCLKP/N is instead centered with the output data valid window (POUTP/N[15:0]). This simplifies the board design, as delaying the clock on the board is not required. See Table 35 for LVDS termination.

Parallel Output Data (POUTP/N[15:0]) – External Pin

The Parallel Output Data (POUTP/N[15:0]) LVDS outputs are re-timed data that are output from the demultiplexer at a rate of 622.08 Mbps (or equivalent FEC/10 Gigabit Ethernet rate). Bit 15 is the most significant bit and is the first received bit. The data is re-timed and synchronized to the Parallel Output Clock (POCLKP/N). This bus is typically connected to a framer, mapper or digital wrapper (e.g. AppliedMicro's KHATANGA, GANGES or RUBICON). See Table 35 for LVDS termination.

Receive Lock Detect (RX_LOCKDET) – Register and External Pin

Active high LVCMOS Lock Detect (RX_LOCKDET) signal indicates a valid incoming data stream. When inactive (low), it indicates that the incoming data stream has failed the frequency test as dictated by the PLL or that LCKREFN has been asserted low or LOS_SD has been de-asserted for negated Signal-Detect input or asserted for Loss-of-Signal output. This test is used to determine if the serial input data is valid. When RX_LOCKDET is active, the PLL is locked to the data stream. This output can be accessed through the serial bus register and external LVCMOS pin.

Recovered 622.08/155.52 MHz Clock (RX_MCKP/N) – External Pin

The LVDS 622.08/155 MHz Clock (or equivalent FEC/10 Gigabit Ethernet rate) (RX_MCKP/N) is the clock which is recovered from the input data stream. When RX622SEL is asserted, RXMCK is 622 MHz. When the RX622SEL is de-asserted, RXMCK is 155 MHz. This clock may be used to drive the reference clock input of the transmit side (CSU REFCLK) of the S19252. See Table 35 for LVDS termination.

Receive Built-In Self Test Error (RX_BIST_ERR) – Register

The active high receive Built-In Self Test Error (RX_BIST_ERR) signal indicates a bit error in the receive built-in self test loop. After the receive checker is initialized, it will compare the parallel data input with the calculated pattern. If the parallel data input does not match the calculated pattern, the RX_BIST_ERR flag will be set active. The RX_BIST_ERR flag can be cleared by asserting RX_BIST_CLR in the RX_BIST_EN mode or by resetting (RSTB) the S19252. The RX_BIST_ERR can also be cleared with a rising edge of RX_BIST_EN. This output is only accessible through the serial bus register.

Common Input Pin Description

Reset (RSTB) – External Pin

This active low LVCMOS Reset (RSTB) input asynchronously resets the device. All clocks, including PCLK, are disabled during reset. For normal system operation, $V_{DD\_3.3V}$ should be connected to RSTB input. This input should be active for 100 ns to accurately reset the device. This input can be accessed through the external LVCMOS input pin.

Diagnostic Loopback Enable (DLEB) – Register

The DLEB is an active low input that selects the diagnostic loopback mode. In this mode, the Transmitter Data (TSD) is routed internally from the transmitter to the receiver. When DLEB mode is enabled, the received parallel data from the framer/mapper transmit path is routed back to the receive parallel data path of the framer/mapper. This mode allows the digital side of the node to be isolated from the rest of the network. The received serial data, SERDATIP/N, will not be passed on to the framer/mapper. The network, however, will receive the aligned high-speed data TSD, when DLEB mode is active. This input is accessible through the serial bus register.

Line Loopback Enable (LLEB) – Register

This active low input selects line loopback mode. In this mode, the internal receiver data (RSD[15:0]) is routed internally from the receiver to the transmitter. When the LLEB is enabled, the parallel output data RSD[15:0] (internal signal) is routed to the parallel input data path PIN[15:0]. The parallel data outputs POUT[15:0] and parallel output clock POCLK are accessible in the LLEB mode.

Case 1. XVCO select input is active. When LLEB and XVCO inputs are active, the internal POCLK acts as the timing source for the CSU block. In this case, the recovered POCLK is fed into the phase detector block. The output of the phase detector block is fed into the external loop filter and VCO. The output of the external VCO is fed into the CSU_IN input, which would be selected as the reference clock for the CSU block. The jitter transfer specification, as defined in GR-253-CORE, is met in this mode.

Case 2. XVCO select input is inactive. When LLEB input is active and XVCO input is inactive, the internal recovered serial clock (RSCLK) acts as the timing source for the CSU block. In this case, the output of the phase detector block is not used. The jitter transfer specification, as defined in GR-253-CORE, is not met in this mode.

This mode allows the network to be isolated from the digital side of the node (framer/mapper gets bypassed).

See Table 11, *Line Loopback Enable Mode*. This input is only accessible through the serial bus register.

Table 11: Line Loopback Enable Mode

LLEB	XVCO	Mode of Operation/ Clock Source
0	0	Line Loopback Active. Internal RSCLK will be the timing source for the transmitter while XVCO input is inactive.
0	1	Line Loopback Active. POCLK (Output of the external XVCO that is fed into the CSU_IN input) will be the timing source for the transmitter while XVCO input is active.
1	**X**	**Line Loopback inactive.**

The BOLD CELLS denote the default state

Reference Loop Timing (RLPTIME) – Register

This active high input selects the reference loop timing mode. In this mode, the transmitter CSU utilizes the receiver POCLK instead of the transmitter external reference clock (CSU_REFCLK). High-speed data flows into the receiver section of the transceiver and is deserialized and aligned before being transmitted to the framer/mapper. The transmitted POCLK provides the timing for the receive section of the framer/mapper. Since some framer/mappers operate with a fixed-size internal FIFO, the framer/mapper transmit section will have to be synchronized with its receive section to avoid over/under flowing of the internal FIFO. In RLPTIME mode, the transmit clock, or PCLK, is generated from the outbound POCLK with the use of the transceiver's internal clock synthesizer unit.

XVCO select input should be programmed to logic high in the RLPTIME mode. The external VCO should be used in the RLPTIME mode.

In the RLPTIME mode, the internal POCLK is fed into the phase detector block. The output of the phase detector block is fed into the external VCO. The output of the external VCO then goes into the CSU_IN input which acts as the reference clock for the internal clock synthesizer circuit (CSU block in Figure 5). The jitter transfer specification, as defined in GR-253-CORE, is met in this mode. See Table 12, *Reference and Loopback Enable*, for details. This input is only accessible through the serial bus register.

Table 12: Reference and Loopback Enable

DLEB	LLEB	RLPTIME	XVCO	Mode/ Timing Source
0	0	X	X	Not a Valid Mode
X	0	1	X	Not a Valid Mode
0	X	1	X	Not a Valid Mode
0	1	0	0	DLEB
0	1	0	1	DLEB/XVCO with TXREFCLK
1	0	0	0	LLEB with CSU timed to RSD recovered clock
1	0	0	1	LLEB + XVCO timed to RSD recovered clock
1	**1**	**0**	**0**	**Normal Mode**
1	1	0	1	Normal Mode/XVCO with TXREFCLK
1	1	1	1	Normal Mode/XVCO timed to RSD recovered clock
1	1	1	0	Normal Mode/RLPTIME timed to RSD recovered clock

The BOLD CELLS denote the default state

User Defined BIST Pattern (BIST_PTRN[15:0]) – Register

This is a user defined pattern which is output from the transmit or the receive pattern generator. This pattern is loaded on the rising edge of TX_BIST_EN or RX_BIST_EN. The user defined pattern can be selected by proper setting of the PRBS_SEL[1:0]. This input is only accessible through the serial bus register.

Pattern Select (PRBS_SELECT[1:0]) – Register

The pattern select bits select between the different PRBS patterns and the user defined pattern. See Table 13 for details. This input is only accessible through the serial bus register.

Table 13: PRBS Pattern Select

PRBS_SELECT 1	PRBS_SELECT 0	PRBS Pattern
0	0	User Defined
0	1	PRBS 7
1	0	PRBS 23
1	**1**	**PRBS 31**

The BOLD CELLS denote the default state

Bit Error Rate Range Select (BER_SELECT[2:0]) – Register

The bit error rate range select bits selects the appropriate bit error rate range for reporting the bit error rate. See Table 14 for details. This input is only accessible through the serial bus register.

Table 14: Bit Error Rate Range Select

BER_SELECT			Bit Error Rate Exponent/ Terminal Count
0	0	0	BER_COUNT[11:0] * 10^{-6} Terminal Count = 10^{6}
0	0	1	BER_COUNT[11:0] * 10^{-7} Terminal Count = 10^{7}
0	1	0	BER_COUNT[11:0] * 10^{-8} Terminal Count = 10^{8}

Table 14: Bit Error Rate Range Select (Continued)

BER_SELECT			Bit Error Rate Exponent/ Terminal Count
0	0	0	BER_COUNT[11:0] * 10^{-6} Terminal Count = 10^{6}
0	1	1	BER_COUNT[11:0] * 10^{-9} Terminal Count = 10^{9}
1	**0**	**0**	**BER_COUNT[11:0] * 10^{-10} Terminal Count = 10^{10}**
1	0	1	BER_COUNT[11:0] * 10^{-11} Terminal Count = 10^{10}
1	1	X	BER_COUNT[11:0] * 10^{-12} Terminal Count = 10^{12}

The BOLD CELLS denote the default state

Bit Error Rate Reset (BER_RSTB) – Register

This input selects whether the BER_COUNT[11:0] is reset after each terminal count. When active (high), BER_COUNT[11:0] is not reset after each terminal count (transition on TERM_COUNT), but instead continues to accrue errors. This input is only accessible through the serial bus register.

Clock Stop Value (CLKSTOP_VAL) – Register

The Clock Stop Value (CLKSTOP_VAL) register bit, specifies the steady state value when a clock is “killed” or disabled. A high value disables the killed clock to a high steady state, a low value disables the killed clock to a low steady state value. This input is only accessible by serial bus control.

Common Output Pin Description

Transmit and Receive Alarm (TX_RX_ALARM) – Register and External Pin

The active high LVCMOS transmit and receive alarm (TX_RX_ALARM) signal indicates an active alarm on the transmit or the receive output. This output is an electrical “OR” of all the transmit and receive alarms [(“NOT” TX_LOCKDET) “OR” (PHERR) “OR” (“NOT” RX_LOCKDET)]. This output can be accessed through the serial bus register and through an external LVCMOS pin.

Built In Self Test Active (BIST_ACTIVE) – Register

This output indicates that the BIST checker is active and is progressively checking data. This signal monitors the RX checker when the RX_BIST_EN is active and TX checker when TX_BIST_EN is active. This output is only accessible through the serial bus register.

Bit Error Rate Count (BER_COUNT[11:0]) – Register

This output holds the bit error rate being received by the checker with the exponent being determined by the BER_SELECT[2:0] input. This signal monitors the RX checker count when the RX_BIST_EN is active and TX checker count when TX_BIST_EN is active. This output is only accessible through the serial bus register.

Bit Error Rate Overflow (BER_OVERFLOW) – Register

This output indicates that the BER_COUNT[11:0] has overflowed and bit error rate range select (BER_SELECT[2:0]) needs to be changed. This signal is active high and is latched high. This signal monitors the RX checker count when the RX_BIST_EN is active and TX checker count when TX_BIST_EN is active. This output is only accessible through the serial bus register.

Terminal Count Monitor (TERM_COUNT) – Register

This output monitors for the terminal count of the PRBS checker. The terminal count is set by the BER_SELECT[2:0] register. See Table 14 for details. Each transition of this signal indicates that the terminal count has been reached. This signal is initially set low upon RSTB or when TX_BIST_EN/RX_BIST_EN are activated. The TERM_COUNT makes a low to high transition when the first terminal count is reached. A transition on TERM_COUNT will set the BER_COUNT[11:0] register to zero depending upon the BER_RSTB setting. When BER_RSTB is active (high), BER_COUNT[11:0] is not reset after each terminal count, but instead continues to accrue errors. This output is only accessible through the serial bus register.

Transmitter Functional Description

MUX Operation

The S19252 performs the serializing stage in the processing of a transmit SONET STS-192/10 Gigabit Ethernet bit serial data stream. It converts the 16-bit parallel data stream to bit serial format from 9.953 Gbps to 11.3 Gbps. The rate will depend upon the CSU_REFCLK frequency used. A high-frequency bit clock is generated from a 155.52 or 622.08 MHz (or equivalent FEC/10 Gigabit Ethernet rate) frequency reference by using a clock synthesizer consisting of an on-chip phase-lock loop circuit with a divider, VCO and loop filter.

Clock Synthesizer

The clock synthesizer shown in the block diagram in Figure 5, is a monolithic PLL that generates the serial output clock frequency locked to the input Reference Clock (CSU_REFCLKP/N).

The CSU_REFCLKP/N input must be generated from a crystal oscillator which has a frequency accuracy that meets the value stated in Table 27 in order for the Transmit Serial Data (TSDP/N) frequency to have the accuracy required for operation in a SONET/10 Gigabit Ethernet system. The CSU_REFCLK must also meet the phase noise requirements shown in Figures 18 and 20 in order to meet the jitter generation specifications as defined in GR-253-CORE. Lower accuracy crystal oscillators may be used in applications less demanding than the SONET/SDH.

The on-chip PLL consists of; a phase detector, which compares the phase relationship between the VCO output and the CSU_REFCLK input, a loop filter, which converts the phase detector output into a smooth DC voltage, and a VCO, whose frequency is varied by this voltage.

The loop filter generates a VCO control voltage based on the average DC level of the phase discriminator output pulses. A single external clean-up capacitor is utilized as part of the loop filter. The loop filter's corner frequency is optimized to minimize output phase jitter.

Loop Timing

In Reference Loop Timing mode (RLPTIME), the Parallel Clock (POCLK) from the receiver is used as the reference clock to the transmitter. In this mode, the CSU_REFCLKP/N input is not used. The TX_155MCK is generated from the POCLK in this operating mode. When operating the S19252 in RLPTIME mode, the TX_155MCK output should not be used as the backup reference clock (CRU_REFCLK) for the clock recovery unit. When performing loopback testing (DLEB), the S19252 must not be in RLPTIME mode.

The XVCO input should be programmed to logic high in the RLPTIME mode. The external VCO is recommended to be used in the RLPTIME mode. The internal POCLK will be fed into the external tracking filter (filter and VCO) for cleanup in the RLPTIME mode. The output of the external VCO (which is fed into the CSU_IN input) will be used as the reference clock for the CSU.

If the external VCO is not used in RLPTIME mode the jitter present from the CRU received data will be passed through to the transmitter.

Line Loopback

The line loopback circuitry selects the source of the data that is output on the TSD. When the Line Loopback Enable (LLEB) input is inactive (high), it selects data and clock from the parallel-to-serial converter block. When LLEB is active (low), it forces the output data multiplexer to select the data from the RSD (internal) input, and a receive-to-transmit loopback can be established at the serial data rate. The parallel data outputs POUT[15:0] and parallel output clock POCLK are accessible in the LLEB mode.

Timing Generator

The timing generator function, shown in the block diagram in Figure 5, *Transceiver Functional Block Diagram*, provides a 16-bit parallel rate clock output.

The PCLK output is a 16-bit parallel clock. For STS-192, the PCLK frequency is 622.08 MHz. PCLK is intended for use as a 16-bit parallel speed clock for upstream multiplexing and overhead processing circuits. Using PCLK for upstream circuits will ensure a stable frequency and phase relationship between the data coming into and leaving the S19252 device.

In the parallel-to-serial conversion process, the incoming data is passed from the PICLK clock timing domain to the internally generated PCLK clock timing domain.

The timing generator also produces a feedback reference clock to the clock synthesizer. A counter divides the synthesized clock down to the same frequency as the Transmit Reference Clock (CSU_REFCLK). The PLL in the clock synthesizer maintains the stability of the synthesized clock by comparing the phase of the feedback clock with that of the CSU_REFCLK. The modulus of the counter is a function of the reference clock frequency.

FIFO

A FIFO is added to decouple the internal and external parallel clocks. The internally generated divide-by-16 clock (PCLK) is used to clock out data from the FIFO. PHINIT and TX_LOCKDET are used to center or reset the FIFO. The PHINIT and TX_LOCKDET signals will center the Figure 28 FIFO once they have been asserted (high). (See Figure 28, *FIFO Initialization*). This is in order to ensure that PICLK is stable. This scheme allows the user to have an infinite PCLK-to-PICLK delay through the ASIC. Once the FIFO is centered, the PCLK-to-PICLK delay can have a maximum drift as specified in Table 36, *Transmitter Timing Characteristics*.

The FIFO shown in Figure 5, *Transceiver Functional Block Diagram*, is comprised of two sets of registers. The 622.08 MHz (or equivalent FEC/10 Gigabit Ethernet rate) clocks in the data from the PINP/N[15:0] bus to the first register of the FIFO. A second register is a parallel loadable shift register which takes its parallel input from the first register.

An internally generated PCLK clock, which is phase aligned to the transmit serial clock, activates the parallel data transfer between registers. This 16-bit data is fed into the parallel-to-serial converter.

FIFO Initialization

The FIFO can be initialized in one of the following three ways:

1. During power up, once the PLL has locked to the reference clock provided on the CSU_REFCLK pins, the TX_LOCKDET will go active and initialize the FIFO.
2. When RSTB goes active, the entire transmitter is reset. This causes the PLL to go out of lock, thus the TX_LOCKDET goes inactive. When the PLL reacquires the lock, the TX_LOCKDET goes active and initializes the FIFO. Note that PCLK is held in reset when RSTB is active.
3. When AUTO_FIFO_INIT is not enabled, the user can also initialize the FIFO by raising PHINIT input.

During normal running operation, the incoming data is passed from the PICLK timing domain to the internally generated divide-by-16 clock timing domain. Although the frequency of PICLK and the internally generated clock (PCLK) are the same, their phase relationship is arbitrary. To prevent errors caused by short setup or hold times between the two timing domains, the FIFO circuitry monitors the phase relationship between PICLK and the internally generated clock. When a potential setup or hold time violation is detected, Phase Error (PHERR) goes high. If the condition persists, PHERR will remain high. When AUTO_FIFO_INIT is not enabled, if PHERR conditions occur, PHINIT should be activated to recenter the FIFO. If AUTO_FIFO_INIT is enabled, PHERR is connected to PHINIT internally. Then, the FIFO is centered automatically. PHERR will go inactive when the realignment is complete or the drift has fallen to a level within the specified maximum of 2 ns. (See Figure 28 *FIFO Initialization*.)

Parallel-to-Serial Converter

The parallel-to-serial converter shown in Figure 5, *Transmitter Functional Block Diagram*, is comprised of staged registers and 2:1 multiplexers. The 16-bit wide data output from the FIFO is presented to the first register/2:1 multiplexer and converted from 16 bits to 8 bits wide. This procedure is repeated to convert to 4, 2 and finally 1-bit wide serial data.

Duo-Binary Encoding

The S19252 has a built-in duobinary encoder. Duobinary coding is a means of controlling ISI by adding the input with the previous data bit. Pre-coding increases duobinary coding's performance by summing (modulo-2) the previous pre-coded input with the current input prior to the final summing operation. The duo-binary precoder is implemented on the parallel side to save power. This function is controlled by setting the DUO_BINARY_EN register bit through the serial interface.

Transmit Built-In Self Test Mode

The S19252 circuitry includes a PRBS generator and a checker. The transmit built-in self test allows for the verification of the serial data path, CRU, CSU and most of the other blocks in the S19252. The S19252 goes in the transmit BIST mode when TX_BIST_EN is programmed to logic high.

Once the S19252 is in the transmit BIST mode, the PRBS generator will start sending the pattern through the parallel input data path. The pattern can be a PRBS pattern or a user defined pattern depending upon the PRBS_SELECT[1:0] settings. See Table 13 for details.

The user defined pattern can be loaded through the BIST_PTRN[15:0] register. There are two modes of transmit BIST operation:

1. Normal operation with DLEB disabled
2. Normal operation with DLEB enabled

When the diagnostic loopback mode is not active, the serial output data (TSDP/N) must be looped back into the serial input (SERDATIP/N) for the transmit PRBS checker to work with the transmit PRBS generator. If the diagnostic loopback mode is enabled, the TSDP/N outputs will be internally looped back into the SERDATIP/N inputs.

Once the TX_BIST_EN input is programmed to logic high, the transmit PRBS checker will be activated but will not start checking for the valid data pattern until RX_LOCKDET is active. This will ensure that valid data is being passed through the receive channel. Once the RX_LOCKDET is active, the checker will begin its initialization phase for 15 CRU_REFCLK cycles. The transmit checker reads the parallel data output and figures out the next PRBS pattern in the initialization phase. After the checker is initialized, it will compare the parallel data output with the calculated pattern. If the parallel data output does not match the calculated pattern, the TX_BIST_ERR flag will be set active and the number of errors will start accumulating on the BER_COUNT[11:0] register. The bit error rate range can be selected with the appropriate setting of the BER_SELECT[2:0]. See Table 14 for details of setting the range for bit error rate.

The TX_BIST_ERR flag can be cleared by asserting TX_BIST_CLR in the TX_BIST_EN mode or by resetting (RSTB) the S19252. Once the TX_BIST_CLR signal has been received by the checker, it will go back to the initialization phase. TX_BIST_CLR is an active high level sensitive input. In order for the checker to clear the TX_BIST_ERR flag, the TX_BIST_CLR must be asserted high.

Also the BER_RSTB input register resets the BER_COUNT[11:0] after each terminal count. BER_RSTB is a active high input. When active BER_COUNT[11:0] is not reset after each terminal count, but instead continues to accrue errors. When inactive, BER_COUNT[11:0] is reset to zero error value after each terminal count. The TERM_COUNT output monitors for the terminal count of the PRBS checker. The terminal count is set by the BER_SELECT[2:0] register. See Table 14 for details. Each transition of TERM_COUNT signal indicates that the terminal count has been reached. This signal is initially set low upon RSTB or when TX_BIST_EN/RX_BIST_EN are activated. The TERM_COUNT makes a low to high transition when the first terminal count is reached. A transition on TERM_COUNT will set the BER_COUNT[11:0] register to zero depending upon the BER_RSTB setting. When BER_RSTB is active (high), BER_COUNT[11:0] is not reset after each terminal count, but instead continues to accrue errors.

The BER_OVERFLOW output will indicate if the BER_COUNT[11:0] has overflowed. When the BER_OVERFLOW goes active, the bit error rate range select (BER_SELECT[2:0]) needs to be changed. This signal is active high and is latched high. This signal monitors the RX checker count when the RX_BIST_EN is active and TX checker count when TX_BIST_EN is active.

Receiver Functional Description

The S19252 transceiver chip provides the first stage of the digital processing of a receive SONET STS-192/10 Gigabit Ethernet bit-serial stream. It converts the 9.953 Gbps bit-serial data stream into a 622.08 Mbps 16-bit parallel data format (or equivalent FEC/10 Gigabit Ethernet rates).

Post-Amp

The S19252 limiting Post-Amp takes the differential serial data from the SERDATIP/N pins and provides 36 dB small-signal gain. The input to the Post Amp can be either AC or DC coupled. There is an offset voltage adjustment (PAOFFADJ[9:0]) for DC coupling in order to facilitate duty cycle distortion correction.

Clock Recovery

Clock recovery, as shown in the block diagram in Figure 5, *Transceiver Functional Block Diagram*, generates a clock that is the same frequency as the incoming data bit rate at the serial data input. The clock is phase aligned by a PLL so that it samples the data in the center of the data eye pattern.

The Clock Recovery Unit (CRU) extracts a synchronous signal from the serial data input using a frequency and Phase Lock Loop (PLL). The PLL consists of a Voltage Controlled Oscillator (VCO), Phase/Frequency Detectors (PFD), and a loop filter.

The frequency detector ensures predictable lock conditions. It is used during acquisition and serves as a means to pull the VCO into the range of the data rate where the phase detector is capable of acquiring lock.

The phase detector used in the CRU is designed to give minimum static phase error of the PLL. When a transition has occurred, the value of the sample in the vicinity of the transition indicates whether the VCO clock leads or lags the incoming data, and the phase detector produces a binary output accordingly.

When a loss of signal condition exists, the PLL locks onto the receiver's internal reference clock (CRU_REFCLK) to provide a steady output clock. There are two pins (RXCAP1 and RXCAP2) to connect the external capacitor and resistors in order to adjust the PLL loop performance.

The phase relationship between the edge transitions of the data and those of the generated clock are compared by a phase/frequency discriminator. Output pulses from the discriminator indicate the required direction of phase corrections. These pulses are smoothed by an integrating loop filter. The output of the loop filter controls the frequency of the Voltage Controlled Oscillator (VCO), which generates the recovered clock.

Frequency stability without incoming data is guaranteed by an alternate reference input (CRU_REFCLK) onto which the PLL locks when data is lost. If the frequency of the incoming signal varies by a value greater than that stated in Table 27, with respect to CRU_REFCLKP/N, the PLL will be declared out of lock, and the PLL will lock to the reference clock. The assertion of Loss-of-Signal (LOS_SD) output or de-assertion of Signal-Detect (LOS_SD) input will also cause an out-of-lock condition.

The loop filter transfer function is optimized in order to enable the PLL to track the jitter yet tolerate the minimum transition density expected in a received SONET or 10 Gigabit Ethernet data signal.

The total loop dynamics of the clock recovery PLL yield a jitter tolerance which exceeds the minimum tolerance proposed for SONET equipment by the Telecordia standard.

Receive Lock Detect

The S19252 contains a lock detect circuit that monitors the integrity of the serial data inputs. If the received serial data fails the frequency test, the PLL will be forced to lock to the local reference clock. This will maintain the correct frequency of the recovered clock output under loss-of-signal or loss-of-lock conditions. If the recovered clock frequency deviates from the local reference clock frequency by more than the typical value stated in Table 27, *Performance Specifications*, the PLL will be declared out of lock. The lock detect circuit will poll the input data stream in an attempt to reacquire lock to data. If the recovered clock frequency is determined to be within the typical value stated in Table 27, *Performance Specifications*, the PLL will be declared in lock and the lock detect output will go active. An inactive LOS_SD input will also cause an out-of-lock condition. The receive lock detect output should not be used as a frequency discriminator for out of band signals.

Serial-to-Parallel Converter

The serial-to-parallel converter consists of three 16-bit registers. The first is a serial-in, parallel-out shift register, which performs serial-to-parallel conversion. The second is a 16-bit internal holding register, which transfers data from the serial-to-parallel register on byte boundaries. On the falling edge of the POCLK, the data in the holding register is transferred to an output holding register which drives POUTP/N[15:0].

Diagnostic Loopback

When the Diagnostic Loopback Enable (DLEB) input is low, a loopback from the transmitter to the receiver at the serial data rate can be set up for diagnostic purposes. The differential serial output data from the transmitter is routed to the CRU block in place of the normal data stream (RSD). The Transmit Serial Data Output TSDP/N is accessible in the DLEB mode. DLEB takes precedence over LOS_SD.

Receive Built-In Self Test Mode

The S19252 circuitry includes a PRBS generator and a checker. The receive built-in self test allows for the verification of the parallel input and output data paths in the S19252. The S19252 goes in the receive BIST mode when RX_BIST_EN is programmed to logic high.

Once the S19252 is in the receive BIST mode, the PRBS generator will start sending the pattern through the parallel output data path. The pattern can be a PRBS pattern or a user defined pattern depending upon the PRBS_SELECT[1:0] settings. See Table 13 for details. The user defined pattern can be loaded through the BIST_PTRN[15:0] register. There are two modes of receive BIST operation:

1. Normal operation with LLEB disabled
2. Normal operation with LLEB enabled

When the line loopback mode is not active, the parallel output data (POUTP/N[15:0]) must be looped back externally into the parallel input (PINP/N[15:0]) for the receive PRBS checker to work with the receive PRBS generator. If the line loopback mode is enabled, the POUTP/N[15:0] outputs will be internally looped back into the PINP/N[15:0] inputs.

Once the RX_BIST_EN input is programmed to logic high, the receive PRBS checker will be activated but will not start checking for the valid data pattern until TX_LOCKDET is active. This ensures that valid data is being passed through the receive channel. Once the TX_LOCKDET is active, the checker will begin its initialization phase for 15 CRU_REFCLK cycles. The receive checker reads the parallel data output and figures out the next pattern in the initialization phase. After the checker is initialized, it will compare the parallel data input with the calculated pattern. If the parallel data input does not match the calculated pattern, the RX_BIST_ERR flag will be set active and the number of errors will start accumulating on the BER_COUNT[11:0] register. The bit error rate range can be selected with the appropriate setting of the BER_SELECT[2:0]. See Table 14 for details of setting the range for bit error rate.

The RX_BIST_ERR flag can be cleared by asserting RX_BIST_CLR in the RX_BIST_EN mode or by resetting (RSTB) the S19252. Once the RX_BIST_CLR signal has been received by the checker, it will go back to the initialization phase. RX_BIST_CLR is an active high level sensitive input. In order for the checker to clear the RX_BIST_ERR flag, the RX_BIST_CLR must be asserted high.

Also the BER_RSTB input register resets the BER_COUNT[11:0] after each terminal count. BER_RSTB is a active high input. When active BER_COUNT[11:0] is not reset after each terminal count, but instead continues to accrue errors. When inactive, BER_COUNT[11:0] is reset to zero error value after each terminal count. The TERM_COUNT output monitors for the terminal count of the PRBS checker. The terminal count is set by the BER_SELECT[2:0] register. See Table 14 for details. Each transition of TERM_COUNT signal indicates that the terminal count has been reached. This signal is initially set low upon RSTB or when TX_BIST_EN/RX_BIST_EN are activated. The TERM_COUNT makes a low to high transition when the first terminal count is reached. A transition on TERM_COUNT will set the BER_COUNT[11:0] register to zero depending upon the BER_RSTB setting. When BER_RSTB is active (high), BER_COUNT[11:0] is not reset after each terminal count, but instead continues to accrue errors.

The BER_OVERFLOW output will indicate if the BER_COUNT[11:0] has overflowed. When the BER_OVERFLOW goes active, the bit error rate range select (BER_SELECT[2:0]) needs to be changed. This signal is active high and is latched high. This signal monitors the RX checker count when the RX_BIST_EN is active and TX checker count when TX_BIST_EN is active.

Input/Output Controls

Mode Control

S19252 has external mode control pins that offers users device IO configuration selections. Mode control is accomplished by external pins. The following are the features of mode control as shown in Table 15:

- The S19252 can be configured to operate with MDIO serial interface.
- The S19252 can be configured to operate with I2C serial interface.
- The S19252 can be configured to operate with SPI serial interface.

Table 15: Mode Control

SCANMODE	MODE_2	MODE_1	MODE_0	Operation Modes	Related Table
0	0	0	0	MDIO Interface (default)	See Table 16
0	0	0	1	I2C Interface	
0	0	1	0	SPI Interface	
0	0	1	1	Reserved	
0	1	0	0		
0	1	0	1		
0	1	1	0		
X	1	1	1		

Serial Interface Mode

The S19252 has multiple serial interface modes that support MDIO, I2C and SPI interfaces. See Table 16.

Table 16: Serial Interface Mode

SCANMODE	MODE_2	MODE_1	MODE_0	MPIO_7	MPIO_6	MPIO_5	MPIO_4	MPIO_3	MPIO_2	MPIO_1	MPIO_0	Termination and Mode Description
MDIO												
Pull Down	Pull Down				Pull Down	Pull Up	Pull Up	Pull Down	Pull Down	Pull Down	Pull Down	On-Chip Internal MDIO Terminations
0	0	0	0	-	ADDRESS4	MDIO	MDC	ADDRESS3	ADDRESS2	ADDRESS1	ADDRESS0	MDIO
I2C												
Pull Down	Pull Down					Pull Up	Pull Up	Pull Down	Pull Down	Pull Down	Pull Down	On-Chip Internal I2C Terminations
0	0	0	1	SDA	SCL	-	-	-	ADDRESS2	ADDRESS1	ADDRESS0	I2C
SPI												
Pull Down	Pull Down					Pull Up	Pull Up	Pull Down	Pull Down	Pull Down	Pull Down	On-Chip Internal SPI Terminations
0	0	1	0	-	-	SDI	SCK	SDO	CS	-	-	SPI

MDIO Bus and Address Register

S19252 uses (as Default) a simple bi-directional two-wire bus for efficient inter-IC control. This bus reads from and writes into most of the S19252 control logic. The following are some important features of MDIO bus:

- The S19252 has a unique address on the bus and a simple master/slave relation exists at all times.
- Only two bus lines are required; a Management Data Input/Output line (MDIO) and a Management Data Control line (MDC). All address/data (MDIO) bits to the S19252 and read data (MDIO) bits for the host are sampled on the rising edge of the clock (MDC).

The register mapping has been outlined below. The serial port interface is based on the IEEE802.3u MII Management Interface standard. Communication occurs across two wires and is formatted in frames. The two wires are clock (MDC) and data (MDIO). There is no preamble required before a frame as described in the IEEE standard. At the rising edge of RSTB, the S19252 loads the device address into a register from the ADDRESS[4:0] pins and uses it to decode accesses to its registers. The ADDRESS[4:0] default is defined by the user. These address bits are used to uniquely identify each S19252 device if multiple S19252 devices are controlled by a single microprocessor. Because there are five address lines, 2^5 = 32 S19252 devices that can be configured by a single microprocessor. A frame is formatted as shown in Table 17.

Start of frame: Start of frame is indicated by 01 pattern.

Operation code: For read transaction, 10; For write transaction, 01.

Device Address: The S19252 compares the five address bits of device address to the latched address bits (see Table 17). If they are equal, the S19252 proceeds with the access. If they are not equal, the S19252 ignores the access and does not drive the MDIO signal.

Register address: This field is used to select the registers to be accessed. The register address is 8 bits. The upper 3 page address bits MDIO_PAGE[2:0] are located in register 0x00 bits [7:5]. The remaining lower 5 register address bits are within the MDIO frame shown below as RRRRR. To find the current MDIO register page address read register address 0x00. The page address may be changed while in any page.

When accessing register address range from 0x20 to 0x9C use the MDIO_PAGE[2:0] pointer bits to address the upper pages. At power up the MDIO_PAGE pointer will default to page 0x00 for address range 0x00 to 0x1F.

Turnaround: The two bits between address field and data field are used to avoid contention on the MDIO during a read transaction. For a read transaction, MDIO should be in tri-state for the first cycle of the turnaround. The S19252 drives zero during the second cycle of the turnaround. For a write transaction, the system should drive one during the first cycle of the turnaround and zero during the second cycle of the turnaround.

Data field: Bits 15:8 are always zero. Bits 7:0 contain the contents of the selected register. On reads, reserved register bits will be zero. The first bit transmitted is bit 15.

Idle condition: A final clock puts MDIO back in an idle state (MDIO is tri-stated and pulled-up).

Table 17: Serial Port Frame Format

	START OF FRAME	OPERATION CODE	DEVICE ADDRESS	REGISTER ADDRESS	TURN AROUND	DATA	IDLE
Read Frame Format While in Same Page							
Read	01	10	AAAAA	RRRRR	Z0	00000000DDDDDDDD	Z
Write Frame Format While in Same Page							
Write	01	01	AAAAA	RRRRR	10	00000000DDDDDDDD	Z
Read Frame Sequence While Changing Page Address[XXX]							
Write	01	01	AAAAA	00000	10	00000000**XXX**DDDDD	Z
Read	01	10	AAAAA	RRRRR	Z0	00000000DDDDDDDD	Z
Write Frame Sequence While Changing Page Address[XXX]							
Write	01	01	AAAAA	00000	10	00000000**XXX**DDDDD	Z
Write	01	01	AAAAA	RRRRR	10	00000000DDDDDDDD	Z

I²C BUS® and Address Register

S19252 has the option to use a simple I²C bi-directional two-wire bus for efficient inter-IC control. All register controlled features and functions are programmed via the I²C BUS®. A detailed register map description can found in the S19252 Programming Manual.

The following are some important features of I²C BUS®:

- The S19252 has a unique I²C address with the upper 4 bits[7:4] fix at 1101 and bits [3:1] the device ADDRESS[2:0] bits (see Table 16).
- The S19252 I²C interface operates as a slave configuration at all times.
- Only two bus lines are required; a serial Data Input/ Output line (SDA) and a Clock line (SCL).

The serial port interface is based on the I²C. Communication occurs across two wires and is formatted in frames. The two wires are clock (SCL) and data (SDA). At the rising edge of RSTB, the S19252 loads the device address into a register from the device ADDRESS[2:0] pins and uses it to decode access to its I²C port. The ADDRESS[2:0] default is 000 if no pull ups are connected to these bits. The address bits are used to uniquely identify the S19252 device if multiple I²C devices are controlled by a single microprocessor. A frame is formatted as shown in Figure 6.

I²C Start/Repeat Conditions: A falling edge on SDA during SCL high time.

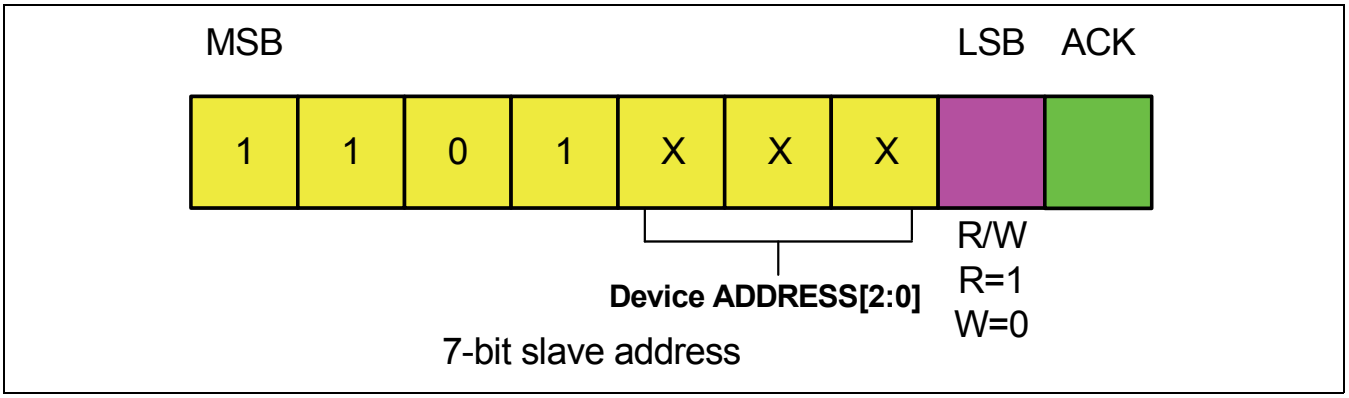
I²C Acknowledge: A low assertion on the SDA line from the receiver after a data transfer.

I²C Not Acknowledge: A high left on the SDA line by the receiver after a data transfer.

Stop Code: A rising edge on SDA during SCL high time. After this condition, the bus becomes tristated, and both SDA and SCL are pulled high.

REFCLKP/N is not required for read/write registers access through the I²C interface.

Figure 6: Two Wire Slave Address



Serial Peripheral Interface (SPI)

S19252 has the option to use a simple SPI bi-directional serial bus for efficient inter-IC control. All register controlled features and functions are programmed via the SPI bus. A detailed register map description can found in the S19252 Programming Manual. The SPI bus is a simple communications system with a master which shifts data into the slave while the slave simultaneously shifts data out. Serial EEPROM manufactures have developed a defacto standard protocol for write and reads over SPI that will be supported by the SPI. SPI as defined uses two pins to define the operating mode: CPOL (clock polarity) and CPHA (clock phase). Of the four combinations of these two signals, two of the modes are supported by most serial EEPROMs:

mode 0, 0; (CPOL = 0, CPHA = 0)

mode 1, 1; (CPOL = 1, CPHA = 1)

The SPI will support modes 0, 0 and 1, 1. From a slave point of view both modes are identical when using the standard protocol, in that the data is sampled on the rising edge of the clock and presented on the falling edge of the clock.

The SPI interface operates at a SPI_SCK frequency up to 10 MHz.

SPI Pin Signals

spi_sck: Clock (SCK). The *spi_sck* pin is an input that synchronizes the data transfer between the master and slave devices. Slave devices ignore the *spi_sck* signal unless the slave select pin (*spi_cs_n*) is active (low) and *spi_hold_n* is inactive (high). In both supported modes for both the master and slave SPI devices, data is shifted out on the falling edge of the *spi_sck* signal and is sampled on the rising edge where data is stable.

spi_sdo: Slave Data Out (also referred to as MISO - Master In Slave Out).

spi_sdi: Slave Data In (also referred to as MOSI - Master Out Slave In).

spi_cs_n: Slave Chip Select (CS_n). This pin is used to enable the SPI slave for a transfer. If the *spi_cs_n* pin of a slave is inactive (high), the device ignores *spi_sck* clocks and keeps the *spi_sdo* output pin in the high-impedance state.

spi_cpol: Clock Polarity (CPOL). The clock polarity pin is used to select either an active high clock (*spi_cpol* = 1) or active low clock (*spi_cpol*= 0). *This pin is not present in this implementation.*

SPI Protocol

Register reads and writes will follow a protocol similar to SPI implementations for serial EEPROMs. Read and write transfers are at least three bytes in length with the first byte containing the 2-bit read or write opcode, the second byte containing the register address, and the third byte the write data or returned read data.

Multi-byte reads and writes are accomplished by simply continuing to write (or read) bytes while *spi_cs_n* remains active. If *autoinc_en* is set the register address is automatically incremented after each write or read.

The chip select line *spi_cs_n* must go active before the transfer begins and must go inactive after the transfer ends. To maintain this protocol *spi_cs_n* cannot remain or be tied active low. This requirement differs from allowable *spi_cs_n* behavior when CPHA= 1 in the original SPI specification.

The READ opcode is 00000011b and the WRITE opcode is 00000010b. A detected invalid opcode will result in no registers being written and the spi_so output will remain high Z.

JTAG Interface

To perform JTAG operations, RSTB must be pulsed low prior to JTAG testing or RSTB must be held low for the duration of the JTAG usage.

SONET and Ethernet Jitter Criteria

SONET Jitter Transfer

The following jitter transfer requirement applies to STS-192 interfaces as defined in GR-253-CORE. For STS-192 interfaces, the jitter transfer function shall be under the curve in Figure 7 when input sinusoidal jitter up to the jitter tolerance mask level in Figure 8 is applied.

The jitter transfer measurements only apply in the RLP-TIME and LLEB modes for the S19252. The external PLL must be used to meet jitter transfer in the RLP-TIME and the LLEB modes.

SONET Jitter Tolerance

The following jitter tolerance requirement applies to STS-192 interfaces as defined in GR-253-CORE. STS-192 interfaces shall tolerate, as a minimum, input jitter applied according to the mask in Figure 8.

Figure 7: SONET STS-192 Jitter Transfer Characteristics

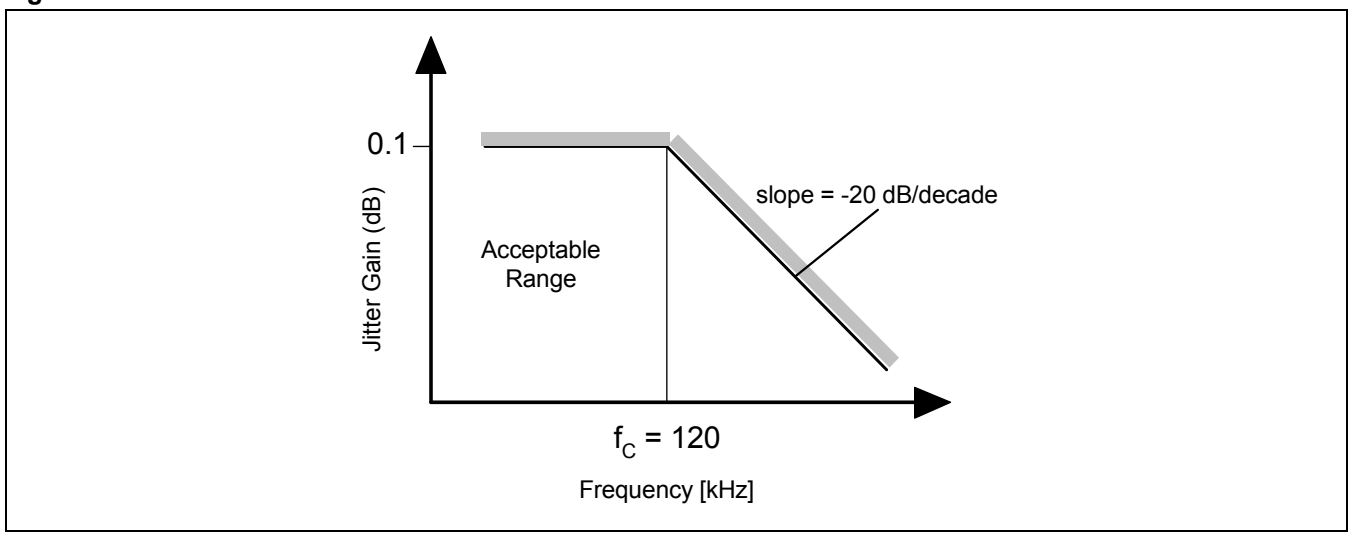
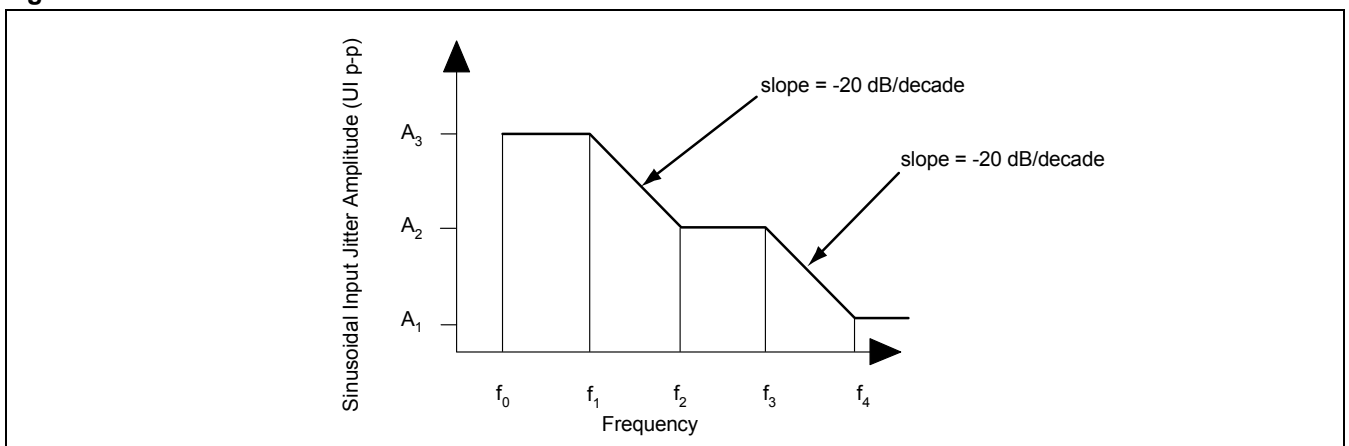


Figure 8: SONET STS-192 Jitter Tolerance Mask



OC-N Level	f_0 (Hz)	f_1 (Hz)	f_2 (Hz)	f_3 (kHz)	f_4 (kHz)	A_1 UI_{PP}	A_2 UI_{PP}	A_3 UI_{PP}
OC-192	10	2k	20k	400	4000	0.15	1.5	15

SONET Jitter Generation

The following jitter generation requirement applies to STS-192 interfaces as defined in GR-253-CORE.

According to GR-253-CORE, jitter generation shall not exceed 0.10 UI_{PP} for STS-192 interfaces when measured using a bandpass measurement filter with a high-pass cutoff frequency of 4 MHz and a low-pass cutoff frequency of at least B3 = 80 MHz.

The S19252 meets the Telecordia Jitter Generation Specification by having a worst-case jitter generation of 50 mUI_{pp} in the normal mode of operation.

10 Gigabit Ethernet Jitter Tolerance

The following 10 Gigabit Ethernet jitter tolerance requirement applies to 10GBASE-ER as defined in IEEE 802.3ae. This total jitter is composed of three components: deterministic jitter; random jitter; and an additional sinusoidal jitter.

The three fundamental components of Jitter Tolerance testing are:

- Input Jitter (Dj and Rj)
- Sinusoidal Jitter
- Test Pattern (Test patterns are different for 10GBASE-R and 10GBASE-W)

Input Jitter (amount of Dj and Rj)

Dj: 0.35 UI pk-pk

Rj: 0.015 UI rms

The random jitter (R_J) component of the input signal has uniform spectral content over the measurement frequency range of at least 1 MHz to 1 GHz. Input Signal must pass the bathtub curves between BERs of 10^{-6} and 10^{-12} as shown in Figure 9.

The input jitter used to test receiver jitter tolerance is specified by the receiver input jitter mask defined in by the following equations (W and sigma are Dj and Rj respectively):

$$Log_{10}(BER) \geq A - B\left(\frac{t - 0.5W}{\sigma}\right)^2$$

$$Log_{10}(BER) \geq A - B\left(\frac{1 - t - 0.5W}{\sigma}\right)^2$$

Where:

$$A = -1.75, B = \frac{Log10(e)}{2} = 0.217$$

Sinusoidal Jitter

The Sj applied for tolerance testing is defined by the jitter mask shown in Figure 10 and Table 18 (per IEEE 802.3ae). The Loop Bandwidth (LB) for S19252 is approximately 8 MHz.

Test Pattern

Test pattern is chosen per IEEE 802.3ae Section 52.9.1. The test pattern is a static pattern and can be loaded into a BERT. IEEE 802.3ae specifies two pseudo-random test patterns for 10GBASE-ER testing. One pattern represents typical scrambled data while the other represents a less typical pattern which could happen by chance and is thought to be more demanding of the transmission process including the clock recovery sub-system. Both patterns are balanced over their length of 33792 bits.

Test pattern is constructed from 4 Segments

- 1 segment is constructed with 128 Blocks
- 1 block is 2 Sync Bits and 64 Payload Bits
- Pay load bits are generated with the scrambler shown in Figure 11.
- Scrambler seeded per Tables 19 and 20.
- Data input is set to 1 or 0.

Figure 9: Input Jitter Mask for Receiver Test

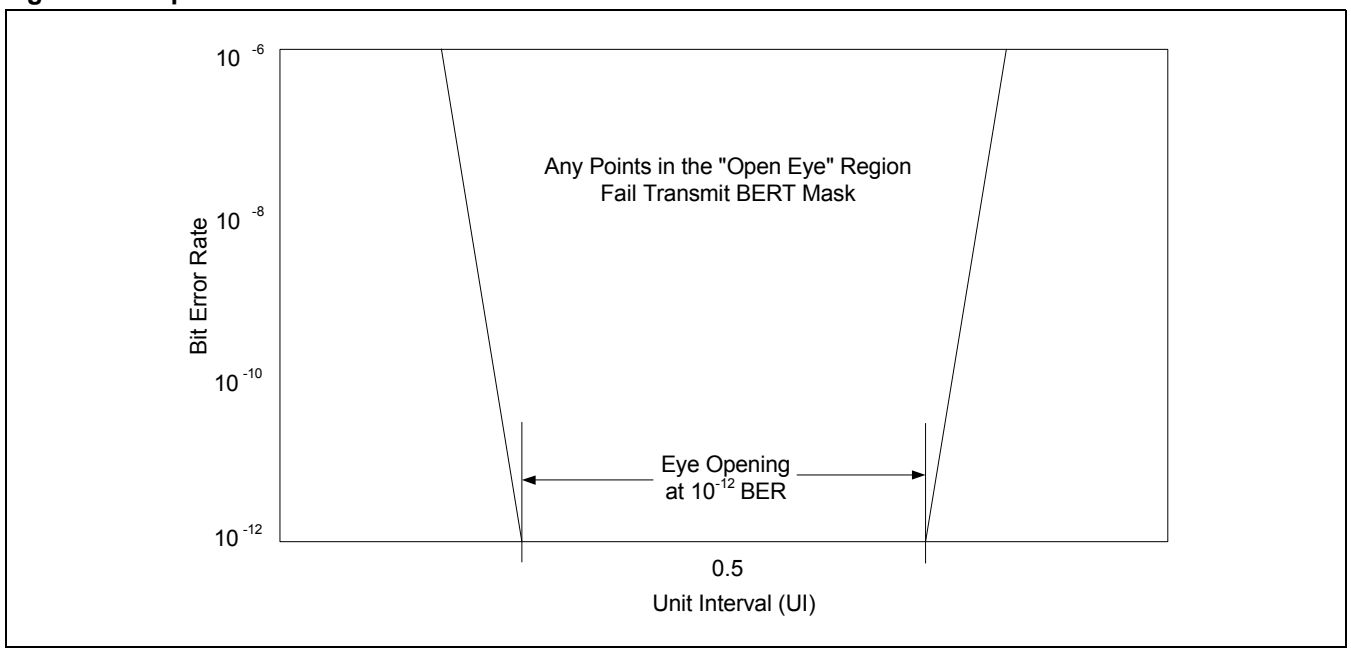


Figure 10: Applied Sinusoidal Jitter - 10 GbE

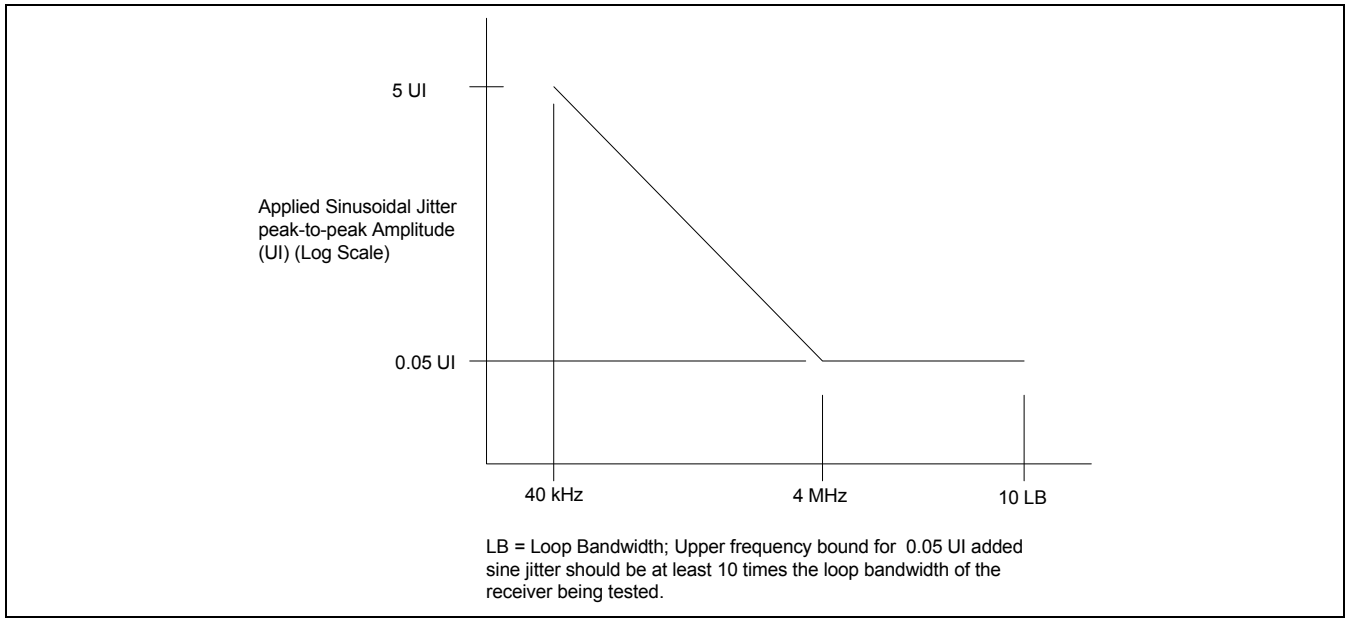


Table 18: Applied Sinusoidal Jitter

Frequency Range	Sinusoidal Amplitude Jitter (UI Peak to Peak)
f < 40 kHz	NA
40 kHz < f < 4 MHz	$(2 \times 10^5)/f$
4 MHz < f < 10 LB	0.05

Figure 11: Scrambler and Descrambler

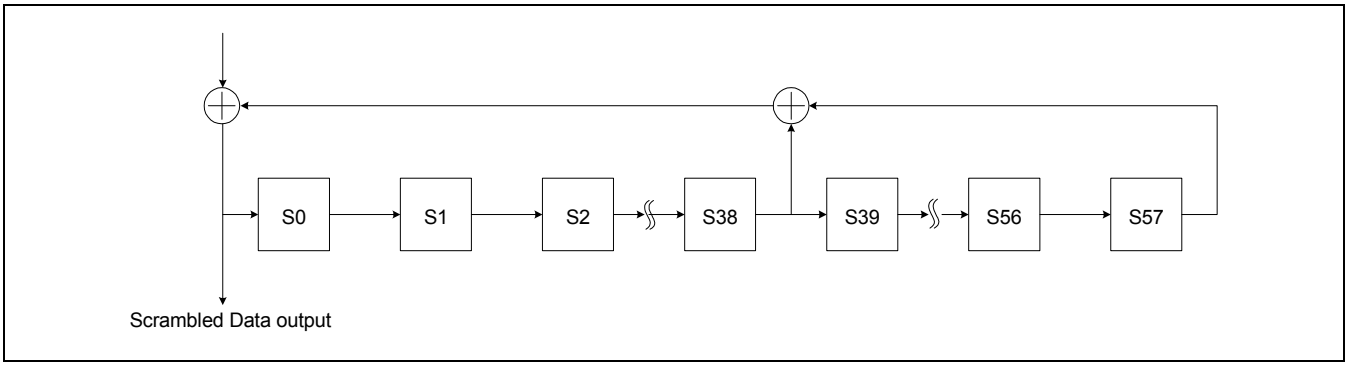


Table 19: Pattern Segments

Segments	Seed [57:0]
A_n	0x3C8B44DCAB6804F
B_n	0x34906BB85A38884
A_i	Inverted Seed for A_n
B_i	Inverted Seed for B_n

Table 20: Test Patterns

Pattern	Sequence of Segments
1	B_n B_i B_n B_i
2	A_n A_i A_n A_i

Register Map

Table 21 below contains the register map summary for the S19252 device. When programming the S19252 device, care should be taken to preserve the default state of all RESERVED register bits. Consult the Programmer's Reference Manual, PRM2010, for the functional details.

Register Access Type Definitions

- RW = Read/Write Access
- RO = Read Only Access
- N/A = Access Type Not Applicable

Table 21: Register Map Summary

Addr.	Reset Value[A]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00[B]	0000 0000	MDIO_PAGE[2]	MDIO_PAGE[1]	MDIO_PAGE[0]	FREEZE_SYNC_DATA	Reserved	Reserved	Reserved	Reserved
		RW	RW	RW	RW	N/A	N/A	N/A	N/A
0x01	0000 0001	XVCO	XVCO155	Reserved	KILLPCLK	KILLPOCLK	KILLRXMCK	KILLTXMCK	DLEB
		RW	RW	N/A	RW	RW	RW	RW	RW
0x02	1000 1100	FIFOLOCKINIT	RX_FORCELOCK	TX_FORCELOCK	GBE_RATESEL	LCKREFN	LLEB	LOS_SDC	Reserved
		RW	RW	RW	RW	RW	RW	RW	N/A
0x03	1001 1110	AUTO_FIFO_INIT	PHINIT	RLPTIME	LVDS_INPUT_AC_EN	Reserved	Reserved	Reserved	Reserved
		RW	RW	RW	RW	N/A	N/A	N/A	N/A
0x04	1000 0001	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RX_RSTB
		N/A	N/A	N/A	N/A	N/A	N/A	N/A	RW
0x05	1001 0100	RX622SEL	CLKSTOP_VAL	RX_PD	SD_POL	SHORTLOCK	SONET_RATESEL	Reserved	Reserved
		RW	RW	RW	RW	RW	RW	N/A	N/A
0x06	1111 0001	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	TX_RSTB
		N/A	N/A	N/A	N/A	N/A	N/A	N/A	RW
0x07	0000 0000	Reserved	Reserved	Reserved	TX_PD	Reserved	Reserved	Reserved	Reserved
		N/A	N/A	N/A	RW	N/A	N/A	N/A	N/A
0x08	010- --00	DUO_BINARY_EN	TSCLK_PD	TSCLK_SQ_EN	TSCLK_SW[2:0]			Reserved	Reserved
		RW	RW	RW	RW			N/A	N/A
0x09	---1 0---	TSD_SLEW[2:0]			TSD_SQ_EN	TSD_SQ_POL	TSD_SW[2:0]		
		RW			RW	RW	RW		
0x0A	0011 1011	INVERT_RXDATA	INVERT_TXDATA	KILLPOUTB	KILLTXDATB	RX_SQ_EN	RX_SQ_POL	RX_SQ[1:0]	
		RW	RW	RW	RW	RW	RW	RW	
0x0B	0000 0000	RX_DATA_SWAP	TX_DATA_SWAP	Reserved	Reserved	TAP0_CNTL[3:0]			
		RW	RW	N/A	N/A	RW			
0x0C	0000 0011	TAP1_CNTL[3:0]				TAP2_CNTL[3:0]			
		RW				RW			
0x0D-0x0F	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
0x10	x001 010-	Reserved	Reserved	RX_LOS_CNTL	Reserved	Reserved	Reserved	Reserved	Reserved
		N/A	N/A	RW	N/A	N/A	N/A	N/A	N/A

Table 21: Register Map Summary (Continued)

Addr.	Reset Value[A]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x11-15	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
0x16	xxxx xxxx	PA_DCOFFADJ_FB[7:0]							
		RO							
0x17	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
0x18	xxxx 1000	Reserved	Reserved	Reserved	Reserved	ADAPOFFADJ	Reserved	Reserved	Reserved
		N/A	N/A	N/A	N/A	RW	N/A	N/A	N/A
0x19	---- -----	PAOFFADJ[7:0]							
		RW							
0x1A-1B	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
0x1C	0--- ----	Reserved	Reserved]	Reserved]	PAEQ_LINKOPT1[4:0]				
		N/A	N/A	N/A	RW				
0x1D	0000 0000	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
0x1E	xxxx x---	Reserved	Reserved	Reserved	Reserved	Reserved	PAEQ_LINKOPT2[4:2]		
		N/A	N/A	N/A	N/A	N/A	RW		
0x1F	--xx xxx0	PAEQ_LINKOPT2[1:0]		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		RW		N/A	N/A	N/A	N/A	N/A	N/A
0x20[B]	0000 000	MDIO_PAGE[2]	MDIO_PAGE[1]	MDIO_PAGE[0]	FREEZE_SYNC_DATA	Reserved	Reserved	Reserved	Reserved
		RW	RW	RW	RW	N/A	N/A	N/A	N/A
0x21-23	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
0x24	1111 1x10	Reserved	Reserved	Reserved	Reserved	Reserved	PA_LOS_MEM	PA_LOS_POL	Reserved
		N/A	N/A	N/A	N/A	N/A	RO	RW	N/A
0x25-0x2E	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
0x2F	0000 0000	LOS_VTH_AST[7:0]							
		RW							
0x30	0000 0000	LOS_VTH_DST[7:0]							
		RW							
0x31	110- --11	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
0x32	xxxx xxxx	RSSI[7:0]							
		RO							
0x33	1000 00xx	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RSSI_HIRANG	Reserved
		N/A	N/A	N/A	N/A	N/A	N/A	RO	N/A

Table 21: Register Map Summary (Continued)

Addr.	Reset Value[A]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x34	0010 1010	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PAOFFADJ[9:8]	
		N/A	N/A	N/A	N/A	N/A	N/A	RW	
0x35-3F	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
0x40[B]	0000 0000	MDIO_PAGE[2]	MDIO_PAGE[1]	MDIO_PAGE[0]	FREEZE_SYNC_DATA	Reserved	Reserved	Reserved	Reserved
		RW	RW	RW	RW	N/A	N/A	N/A	N/A
0x41 - 0x5F	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
0x60[B]	0000 0000	MDIO_PAGE[2]	MDIO_PAGE[1]	MDIO_PAGE[0]	FREEZE_SYNC_DATA	Reserved	Reserved	Reserved	Reserved
		RW	RW	RW	RW	N/A	N/A	N/A	N/A
0x61 - 0x78	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
0x79	0011 1111	RXREFA_NOTB	RXREFSEL	TXREFA_NOTB	TXREFSEL	Reserved	Reserved	Reserved	Reserved
		RW	RW	RW	RW	N/A	N/A	N/A	N/A
0x7A-7E	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
0x7F	0110 0101	PHASE_ADJ[2:0]			Reserved	Reserved	Reserved	Reserved	Reserved
		RW			N/A	N/A	N/A	N/A	N/A
0x80[B]	0000 0000	MDIO_PAGE[2]	MDIO_PAGE[1]	MDIO_PAGE[0]	FREEZE_SYNC_DATA	Reserved	Reserved	Reserved	Reserved
		RW	RW	RW	RW	N/A	N/A	N/A	N/A
0x81	1000 0001	Reserved	Reserved	Reserved	RX_VCO_RANGE[1:0]		TX_VCO_RANGE[1:0]		Reserved
		N/A	N/A	N/A	RW		RW		N/A
0x82	xxxx xx11	PHERR	RX_LOCKDET	RXLOCK_FLT	TX_LOCKDET	TXLOCK_FLT	TX_RX_ALARM	Reserved	Reserved
		RO	RO	RO	RO	RO	RO	N/A	N/A
0x83	0xxx x100	BER_AUTO_RANGE	BER_EXPC[2:0]			BER_OVERFLOW	BER_SELECT[2:0]		
		RW	RO			RO	RW		
0x84	xxxx xxxx	BER_COUNT[11:4]							
		RO							
0x85	xxxx x00x	BER_COUNT[3:0]				BIST_ACTIVE	RX_BIST_CLR	RX_BIST_EN	RX_BIST_ERR
		RO				RO	RW	RW	RO
0x86	00x1 0111	TX_BIST_CLR	TX_BIST_EN	TX_BIST_ERR	BER_RSTB	TX_ERR_INSERT	Reserved	Reserved	Reserved
		RW	RW	RO	RW	RW	RW	RW	RW
0x87	1100 1100	BIST_PTRN[15:8]							
		RW							
0x88	1100 1100	BIST_PTRN[7:0]							
		RW							

Table 21: Register Map Summary (Continued)

Addr.	Reset Value[A]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x89	0011 000x	PRBS_RXCHK_INV	PRBS_RXGEN_INV	PRBS_SELECT[1:0]		PRBS_TXCHK_INV	PRBS_TXGEN_INV	RX_ERR_INSERT	TERM_COUNT
		RW	RW	RW		RW	RW	RW	RO
0x8A-91	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
0x92	1000 1111	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	AUTOINC_EN
		N/A	N/A	N/A	N/A	N/A	N/A	N/A	RW
0x93	xx0x xxxx	Reserved	Reserved	Reserved	ADDRESS[4:0][C]				
		N/A	N/A	N/A	RW				
0x94	---- ----	RX_VCO_RES_PROCESS[1]	Reserved	Reserved	RX_VCO_RES_PROCESS[0]	Reserved	Reserved	Reserved	Reserved
		RW	N/A	N/A	RW	N/A	N/A	N/A	N/A
0x95 - 0x96	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
0x97	---- ----	VERSION_ID[3]	Reserved	Reserved	VERSION_ID[2:1]		Reserved	Reserved	VERSION_ID[0]
		RW	N/A	N/A	RW		RW	RW	RW
0x98	---- ----	TX_VCO_RES_PROCESS[1:0]		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
0x99	---- ----	REVISION_ID[4:0]					Reserved	Reserved	Reserved
		RW					N/A	N/A	N/A

A – RESET VALUE DESCRIPTIONS: The reset value of the SHADED CELLS may vary by part and are denoted with a dash “-” in the associated bit locations as these reset values are fused at wafer sort. The reset value for a complete block(s) of registers that are listed as “Reserved” are denoted with a single “-” as these reset values are ‘don’t cares’ for the end user. The reset values for the Read-Only registers are denoted with an “x” in the associated bit locations as their default states may be dependant on status signals or programmable inputs.
B – Register locations 0x00, 20, 40, 60, 80 all contain the same value no matter which location is written. Consult address 0x00 (Table 2) in the Programmers Reference Manual for the detailed description of the bit level controls contained in these registers.
C – The reset value of the ADDRESS[4:0] bits are dependant on the value of the ADDRESS[4:0] input pin.

Pin Assignments and Descriptions

Table 22: Input Pin Assignments and Descriptions

Pin Name		Level	I/O	Pin#	Description
Transmitter Inputs					
TX_DATA SWAP = 0	TX_DATA SWAP = 1				
PINP0 PINN0 PINP1 PINN1 PINP2 PINN2 PINP3 PINN3 PINP4 PINN4 PINP5 PINN5 PINP6 PINN6 PINP7 PINN7 PINP8 PINN8 PINP9 PINN9 PINP10 PINN10 PINP11 PINN11 PINP12 PINN12 PINP13 PINN13 PINP14 PINN14 PINP15 PINN15	PINP15 PINN15 PINP14 PINN14 PINP13 PINN13 PINP12 PINN12 PINP11 PINN11 PINP10 PINN10 PINP9 PINN9 PINP8 PINN8 PINP7 PINN7 PINP6 PINN6 PINP5 PINN5 PINP4 PINN4 PINP3 PINN3 PINP2 PINN2 PINP1 PINN1 PINP0 PINN0	LVDS	I	A13 B13 A11 B11 D12 E12 E11 D11 G18 G17 E18 D18 C16 C15 D14 E14 H18 H17 F14 F15 A17 A16 B15 A15 J17 J18 F18 F17 B18 A18 D17 D16	**Parallel Data Input**. A 16-bit parallel 622.08 Mbps. (or equivalent FEC/10 Gigabit Ethernet rate) word, aligned to the Parallel Input Clock (PICLK). PINP/N[15] is the most significant bit (corresponding to bit 1 of each word, the first bit transmitted). PINP/N[0] is the least significant bit (corresponding to bit 16 of each word, the last bit transmitted). PINP/N[15:0] is sampled on the rising edge of PICLK. Internally terminated 100 Ω line-to-line. This input is not internally biased. While TX_DATA_SWAP is equal to either 0 or 1 PINP/N[15] in the appropriate column is the most significant bit (corresponding to bit 1 of each word, the first bit transmitted).
PICLKP PICLKN		LVDS	I	B14 A14	**Parallel Input Clock**. A 622.08 MHz nominally 50% duty cycle input clock, to which PINP/N[15:0] is aligned. PICLK is used to transfer the data on the PIN inputs into a FIFO and holding register in the parallel-to-serial converter. Internally terminated 100 Ω line to line. This input is not internally biased.
REFCLKAP REFCLKAN		Diff CML	I	C5 C6	**Transmit Reference Clock A**. Input used as the reference for the internal bit clock frequency synthesizer. This is a default reference clock source for CSU. This input is internally biased and terminated. This input must be AC coupled.

Table 22: Input Pin Assignments and Descriptions (Continued)

Pin Name	Level	I/O	Pin#	Description
TXCAP1 TXCAP2	Analog		A4 A5	**Transmit Loop Filter Capacitors**. Connections for external loop filter capacitors and resistors. See Figure 27, *External Loop Filter Components*, and Table 41 *Transmit and Receive External Loop Filter Components*
XVCO	Register 0x01h	I		**External Voltage Controlled Oscillator Select.** This active high input selects CSU_IN as the reference clock for the CSU block. In this mode, CSU block uses CSU_IN as the reference clock instead of using CSU_REFCLK directly. This signal can be accessed through the serial bus register (Default = 0).
XVCO155	Register 0x01h	I		**External Voltage Controlled Oscillator 155MHz Select.** This active high input selects 155MHz XVCO rate or divide by 64 equivalent rate while in this mode. When this input is low the XVCO rate is 622MHz or equivalent divide by 16 rate. This signal can be accessed through the serial bus register (Default = 0).
REFSEL	Register 0x79h	I		**Reference Select**. Selects the reference clock frequency of the transmit reference clock (CSU_REFCLK). See Table 3, *Reference Frequency (CSU REFCLK) for the Clock Synthesis Unit*. This signal can be accessed through the serial bus register (Default = 1).
PHINIT	Register 0x03h	I		**Phase Initialization**. Asynchronous input that initializes the PHINIT. See Figure 28, *FIFO Initialization*. This signal can be accessed through the serial bus register (Default = 0).
AUTO_FIFO_INIT	Register 0x03h	I		**FIFO Initialization**. This active high control input internally connects the transmit FIFO signals (PHERR and PHINIT) and automatically initializes the FIFO in case of a PCLK/PICLK set-up or hold time violation. This input can be accessed through the serial bus register (Default = 1).
KILLPCLK	Register 0x01h	I		**Kill PCLK Output.** Active high For normal operation, KILLPCLK is low. When this input is high, it will force the PCLK output to a state specified by the CLKSTOP_VAL register bit. This signal can be accessed through the serial bus register (Default = 0).
KILLTXMCK	Register 0x01h	I		**Kill TX_MCK Clock Output.** Active high. For normal TX_155MCK operation, KILLTXMCK is low. When this input is high, it will force the TX_155MCK output to a state specified by the CLKSTOP_VAL register bit. This signal can be accessed through the serial bus register (Default = 0).
TX_BIST_EN	Register 0x86h	I		**Transmit Built-In Self Test Enable.** This active high input enables the transmit built-in self test mode. In this mode the PRBS generator will start sending the pattern through the parallel inputs and transmit checker will be activated. This signal can be accessed through the serial bus register (Default = 0).
TX_BIST_CLR	Register 0x86h	I		**Transmit Built-In Self Test Clear.** This active high level sensitive input clears the transmit built-in self test error. The TX_BIST_ERR flag can be cleared by asserting TX_BIST_CLR high in the BIST mode or by resetting (RSTB) the S19252. This signal can be accessed through the serial bus register (Default = 0).

Table 22: Input Pin Assignments and Descriptions (Continued)

Pin Name	Level	I/O	Pin#	Description
TAP[2:0]_CNTL	Register 0x0B-0Ch	I		**Transmitter De-Emphasis 3 Tap FIR Filter**. This feed forward equalization control on the transmitter output provides additional gain to compensate for dispersion losses in FR4. TAP0 and TAP2 each have an adjustment range of 0 to 16. TAP1 provides no adjustment. (Default: TAP0 = 0, TAP2 = 3)
CSU_INP CSU_INN	REFCLK Diff CML	I	B7 A7	**Clock Synthesizer Input**. Input to the internal CSU. Used to generate the serial transmit data. This input is internally biased and terminated. This input must be AC coupled.
TXPD	LVCMOS Pull Down	I	E9	**Transmitter Power Down**. (Active high) For transmitter power down set to logic 1 (high) when S19252 is used as receiver.
TX_DATA_SWAP	Register 0x0Bh	I		**Parallel Input Data Bus Reversal.** Reverses the order of the parallel input data bus (PINP/N[15:0]). TX_DATA_SWAP input should be programmed to logic low (Default) when S19252 is used with 300-pin MSA connector. TX_DATA_SWAP input should be programmed to logic high when S19252 is used with 200-pin MSA connector. This signal can be accessed through the serial bus register (Default = 0).
LVDS_INPUT_AC_EN	Register 0x03h	I		**LVDS Input AC Enable.** When enabled provides input bias for AC coupled LVDS (PINP/N[15:0] and PICLKP/N) inputs. When (PINP/N[15:0] and PICLKP/N) inputs are DC coupled this control must be disabled to allow DC input level shifting circuit operation. This control can be accessed through serial bus register (Default = 1).
Receiver Inputs				
SERDATIP SERDATIN	High Speed Diff CML	I	R1 U1	**Serial Data Input.** Differential high-frequency serial data input to limiting post-amp for small signal gain. Internally biased and terminated 100 Ω line-to-line (50 Ω + 50 Ω with center tap capacitor). This input must be AC coupled.
CENTER_TAP	Analog	I	N1	**Center Tap Input.** This input should be connected to a broadband 0.01 µF capacitor to ground.
PAOFFADJ9 PAOFFADJ8 PAOFFADJ7 PAOFFADJ6 PAOFFADJ5 PAOFFADJ4 PAOFFADJ3 PAOFFADJ2 PAOFFADJ1 PAOFFADJ0	Register 0x34h 0x19h	I		**Post-Amp Offset Adjust.** Used to correct duty cycle distortion on the input data signal. See Table 9 for details. This signal can be accessed through the serial bus register. The default state will depend up on the fuse settings and may vary from one device to another.
ADAPOFFADJ	Register 0x18h	I		**Adaptive Post-Amp Offset Adjust Enable.** Enables the adaptive offset adjustment control. See Table 10 for details. This signal can be accessed through the serial bus register (Default = 1).

Table 22: Input Pin Assignments and Descriptions (Continued)

Pin Name	Level	I/O	Pin#	Description
PAEQ_LINKOPT14 PAEQ_LINKOPT13 PAEQ_LINKOPT12 PAEQ_LINKOPT11 PAEQ_LINKOPT10	Register 0x1E-1Fh	I		**Post-Amp Equalization Link Optimization 1 Adjust (ISI Compensation Control).** Used to adjust serial data input dispersion optimization control. This control compensates for the ISI. This control can be accessed through the serial bus register (Default = 0,0,1,1,0).
PAEQ_LINKOPT24 PAEQ_LINKOPT23 PAEQ_LINKOPT22 PAEQ_LINKOPT21 PAEQ_LINKOPT20	Register 0x1Ch	I		**Post-Amp Equalization Link Optimization 2 Adjust.** Used to adjust input serial data peaking control. This control boosts the frequency response of the input signal. This control can be accessed through the serial bus register (Default = 0,0,0,0,0).
PHASE_ADJ2 PHASE_ADJ1 PHASE_ADJ0	Register 0x7Fh	I		**Phase Adjust.** Used to adjust the phase between the recovered clock and data. The phase adjust can improve the bit error rate and link budget. See Table 8 for details. This signal can be accessed through the serial bus register (Default = 0,1,1).
REFCLKBP REFCLKBN	REFCLK Diff CML	I	D9 D8	**Receive Reference Clock B**. The default of this input used as the reference for the internal bit clock frequency synthesizer of the CRU. But it can be used for either TX or RX reference. 155.52 or 622.08 MHz (or equivalent FEC/10 Gigabit Ethernet frequency) input used as the reference for the internal bit clock frequency synthesizer. This input is internally biased and terminated. This input must be AC coupled.
RXCAP1 RXCAP2	Analog		V5 V6	**Receive Loop Filter Capacitors**. Connections for external loop filter capacitors and resistors. See Figure 27, *External Loop Filter Components*, and Table 41, *Transmit and Receive External Loop Filter Components*.
LCKREFN	Register 0x02h	I		**Lock to Reference.** Active low. When active, the CRU PLL is forced to lock to the local reference clock input (CRU_REFCLK). If unused, connect to logic ‘1’ for normal operation. This signal can be accessed through serial bus register (Default = 1).
LOS_SD	LVCMOS Pull Up	I/O	R9	**Loss of Signal/Signal Detect.** Dual purpose pin. Direction controlled with LOS_SDC memory map register. When LOS_SDC is low, LOS_SD will act as an input. As an output pin: Loss of Signal indication output for receiver. As an LVCMOS single-ended input to be driven by the external optical receiver module to indicate a loss of received optical power. When a loss-of-light condition occurs, the internal PLL will be forced to lock to the CRU_REFCLK input signal. The POUTP/N will be forced to a logic ‘0’ state when LOS_SD is inactive. The active level of this input may be programmed by SD_POL.
SD_POL	Register 0x05h	I		**Signal Detect Polarity.** This signal will set the LOS_SD input as either active high or active low. Setting this pin low will set the LOS_SD input as active low. Setting this pin high will set the LOS_SD input as active high. This signal can be accessed through the serial bus register (Default = 1).
KILLPOUTB	Register 0x0Ah	I		**Kill Parallel Data Output.** Active low. For normal operation, KILLPOUTB is high. When this input is low, it will force the POUT[15:0] output to a logic ‘0’ state. This signal can be accessed through the serial bus register (Default = 1).

Table 22: Input Pin Assignments and Descriptions (Continued)

Pin Name	Level	I/O	Pin#	Description
KILLRXMCK	Register 0x01h	I		**Kill RX_MCK Clock Output.** Active High. For normal operation, KILLRXMCK is low. When this input is high, it will force the RX_MCK output to state as specified by the CLKSTOP_VAL register bit. This signal can be accessed through the serial bus register (Default = 0).
KILLPOCLK	Register 0x01h	I		**Kill POCLK Output.** Active high For normal operation, KILLPOCLK is low. When this input is high, it will force the POCLK output to a state specified by the CLKSTOP_VAL register bit. This signal can be accessed through the serial bus register (Default = 0).
RX_BIST_EN	Register 0x85h	I		**Receive Built-In Self Test Enable.** This active high input enables the receive built-in self test mode. In this mode the PRBS generator will start sending the pattern through the parallel data output and receive checker will be activated. This signal can be accessed through the serial bus register (Default = 0).
RX_BIST_CLR	Register 0x85h	I		**Receive Built-In Self Test Clear.** This active high level sensitive input clears the receive built-in self test error. The RX_BIST_ERR flag can be cleared by asserting RX_BIST_CLR high in the BIST mode or by resetting (RSTB) the S19252. This signal can be accessed through the serial bus register (Default = 0).
RXPD	LVCMOS Pull Down	I	B10	**Receive Power Down.** (Active high) For receiver power down set to logic 1 (high) when S19252 is used as Transmitter.
RX_DATA_SWAP	Register 0x0Bh	I		**Parallel Output Data Bus Reversal.** Reverses the order of the parallel output data bus (POUTP/N[15:0]). RX_DATA_SWAP input should be programmed to logic low (Default) when S19252 is used with 300-pin MSA connector. RX_DATA_SWAP input should be programmed to logic high when S19252 is used with 200-pin MSA connector. This signal can be accessed through the serial bus register (Default = 0).
Common Inputs				
RSTB	LVCMOS Pull Up	I	G15	**Master Reset**. Reset input for the S19252. Must remain low for 100 ns to accurately reset the transmitter. During reset, PCLK does not toggle. For normal operation, connect to $V_{DD\_3.3V}$. RSTB while low will set all MII registers and all logic to the default state. This signal can be accessed through an external pin and is (active low).
DLEB	Register 0x01h	I		**Diagnostic Loopback Enable**. This active low input selects the Diagnostic Loopback Mode. In this mode, the transmitter outgoing serial data is re-routed to the receiver. This signal can be accessed through serial bus register (Default = 1).
LLEB	Register 0x02h	I		**Line Loopback Enable**. This active low input selects the Line Loopback Mode. In this mode, the receiver parallel data is routed to the transmitter and re-transmitted back to the source. See Table 11 for details. This signal can be accessed through the serial bus register (Default = 1).

Table 22: Input Pin Assignments and Descriptions (Continued)

Pin Name	Level	I/O	Pin#	Description
RLPTIME	Register 0x03h	I		**Reference Loop Timing**. This active high input selects Reference Loop Timing Mode. In this mode, the transmitter CSU utilizes the receiver POCLK instead of the CSU_REFCLK. See Table 12 for details. This signal can be accessed through the serial bus register (Default = 0).
CLKSTOP_VAL	Register 0x05h	I		**Clock Stop Value.** When a clock is killed, this register bit specifies the steady state value of the killed clock. A low value programs the killed clock to a low steady state value. A high value programs the killed clock to high steady state value. This signal is only accessible by serial bus control. (Default = 0).
BIST_PTRN[15:0]	Register 0x87-88h	I		**User Defined BIST Pattern (BIST_PTRN[15:0]).** This user defined pattern is output from the transmit or the receive pattern generator. This pattern is loaded on the rising edge of TX_BIST_EN or RX_BIST_EN. The user defined pattern can be selected by proper setting of the PRBS_SEL[1:0]. This input can be accessed through the serial bus register.
PRBS_SELECT[1:0]	Register 0x89h	I		**Pattern Select (PRBS_SELECT[1:0]).** The pattern select bits select between the different PRBS patterns and the user defined pattern. See Table 13 for details. This input can be accessed through the serial bus register (Default = 0,0).
BER_SELECT[2:0]	Register 0x83h	I		**Bit Error Rate Range Select (BER_SELECT[2:0]).** The bit error rate range select bits selects the appropriate bit error rate range for reporting the but error rate. See Table 14 for details. This input can be accessed through the serial bus register (Default =1,0,0).
BER_RSTB	Register 0x86h	I		**Bit Error Rate Reset (BER_RSTB).** This input selects whether the BER_COUNT[11:0] is reset after each terminal count. Active high. When active, BER_COUNT[11:0] is not reset after each terminal count, but instead continues to accrue errors. This input can be accessed through the serial bus register (Default = 0).

Table 23: Output Pin Assignments and Descriptions

Pin Name	Level	I/O	Pin#	Description
Transmitter Outputs				
TSDP TSDN	High Speed diff CML	O	G1 J1	**Transmit Serial Data**. Serial data stream signals, normally connected to an optical transmitter module. Output return loss, S_{22} of -12dB at 15 GHz.
TSCLKP TSCLKN	High Speed diff CML	O	B1 D1	**Transmit Serial Clock**. Serial clock signals, normally connected to a lab test equipment or an optical laser module.
PCLKP PCLKN	LVDS	O	B9 A9	**Parallel Clock.** A 622.08 MHz (or equivalent FEC/10 Gigabit Ethernet rate) reference clock. It is normally used to coordinate data transfers between upstream logic and the S19252 device.
TX_155MCKP TX_155MCKN	LVDS	O	D10 E10	**155.52 MHz Clock Output.** 155.52 MHz (or equivalent FEC/10 GbE/ 10 G FC rates) clock output from CSU_REFCLK. The output can be connected to the reference clock input (CRU_REFCLKP/N) of the clock recovery function.
TX_LOCKDET	LV CMOS & Register Pull Up	O	J15	**Transmit Lock Detect**. Active high. Goes active after the PLL has locked to the clock provided on the CSU_REFCLK pins. TX_LOCKDET is an asynchronous output.
PHERR	Register 0x82h	O		**Phase Error**. Pulses high during each PCLK cycle for which there is a potential FIFO overrun/underrun condition. No additional external components required. Should be directly connected to PHINIT through serial bus register.
PD_UPP PD_UPN PD_DWNP PD_DWNN	Phase Detector Diff CML	O	A8 B8 D7 E7	**Phase Detector Output**. This output is used to drive an external charge pump which, in turn, drives the external VCO. The external VCO output is then fed into the CSU_INP/N input to be used as the transmit reference clock for the CSU block.
TX_BIST_ERR	Register 0x86h	O		**Transmit Built-In Self Test Error.** This output indicates a bit error in the transmit built-in self test loop.

Table 23: Output Pin Assignments and Descriptions (Continued)

Pin Name		Level	I/O	Pin#	Description
Receiver Outputs					
POCLKP POCLKN		LVDS	O	N18 M18	**Parallel Output Clock.** Regenerated 622.08 MHz (or equivalent FEC/10 Gigabit Ethernet rate) differential output clock, synchronized to the parallel output data. See Figure 24, *Receiver Timing Characteristics*.
RX_DATA SWAP = 0	RX_DATA SWAP = 1				
POUTP0 POUTN0 POUTP1 POUTN1 POUTP2 POUTN2 POUTP3 POUTN3 POUTP4 POUTN4 POUTP5 POUTN5 POUTP6 POUTN6 POUTP7 POUTN7 POUTP8 POUTN8 POUTP9 POUTN9 POUTP10 POUTN10 POUTP11 POUTN11 POUTP12 POUTN12 POUTP13 POUTN13 POUTP14 POUTN14 POUTP15 POUTN15	POUTP15 POUTN15 POUTP14 POUTN14 POUTP13 POUTN13 POUTP12 POUTN12 POUTP11 POUTN11 POUTP10 POUTN10 POUTP9 POUTN9 POUTP8 POUTN8 POUTP7 POUTN7 POUTP6 POUTN6 POUTP5 POUTN5 POUTP4 POUTN4 POUTP3 POUTN3 POUTP2 POUTN2 POUTP1 POUTN1 POUTP0 POUTN0	LVDS	O	R10 T10 V10 V11 U12 V12 V13 U13 U9 V9 R11 T11 U14 V14 R15 R16 R13 R14 U15 V15 V17 U17 R18 P18 V18 U18 N16 P16 L17 L18 K17 K18	**Parallel Output Data.** Re-timed data from the Demultiplexer (DeMUX) at a rate of 622.08 Mbps (or equivalent FEC/10 Gigabit Ethernet rate). Bit 15 is the first bit received. POUTP/N[15] is the most significant bit (corresponding to bit 1 of each word, the first bit received). POUTP/N[0] is the least significant bit corresponding to bit 16 of each word, the last bit received. While RX_DATA_SWAP is equal to either 0 or 1 POUTP/N[15] in the appropriate column is the most significant bit (corresponding to bit 1 of each word, the first bit received).
RX_LOCKDET		LV CMOS & Register Pull Up	O	H15	**Receive Lock Detect.** Active high. Clock recovery indicator. Active when the internal clock recovery has locked onto the incoming data stream. RX_LOCKDET is an asynchronous output.
RX_MCKP RX_MCKN		LVDS	O	U8 V8	**Recovered 622.08 MHz Clock.** With RX622SEL=1 A 622.08 MHz (or equivalent FEC/10 Gigabit Ethernet rate) clock output derived from the internal receive serial clock (RSCLK). RX_MCK[P:N] output is 155 MHz (or equivalent FEC/10 Gigabit Ethernet rate) with RX622SEL=0.

Table 23: Output Pin Assignments and Descriptions (Continued)

Pin Name	Level	I/O	Pin#	Description
RX_BIST_ERR	Register 0X85h	O		**Receive Built-In Self Test Error.** This output indicates a bit error in the receive built-in self test loop.
Common Outputs				
TX_RX_ALARM	LV CMOS & Register Pull Up	O	L15	**Transmit and Receive Alarm Output.** This output is an electrical “OR” of all the transmit and receive alarms [[(“NOT” TX_LOCKDET) “OR” (PHERR)] “OR” (“NOT” RX_LOCKDET)].
BIST_ACTIVE	Register 0x85h	O		**Built In Self Test Active (BIST_ACTIVE).** This output indicates that the BIST checker is active and is progressively checking data. This output can be accessed through the serial bus register.
BER_COUNT[11:0]	Register 0x84-85h	O		**Bit Error Rate Count (BER_COUNT[11:0]).** This output holds the bit error rate being received by the checker with the exponent being determined by the BER_SELECT[2:0] input. This output can be accessed through the serial bus register. Read BER_COUNT[3:0] first then BER_COUNT[11:4] for accurate error count information.
BER_OVERFLOW	Register 0x83h	O		**Bit Error Rate Overflow (BER_OVERFLOW).** Active high. This output indicates that the BER_COUNT[11:0] has overflowed and bit error rate range select (BER_SELECT[2:0]) needs to be changed. This signal is latched high. This output can be accessed through the serial bus register.
TERM_COUNT	Register 0X89H	O		**Terminal Count Monitor (TERM_COUNT).** This output monitors for the terminal count of the PRBS checker. The terminal count is set by the BER_SELECT[2:0] register. See Table 14 for details. This output can be accessed through the serial bus register.

Table 24: S19252 JTAG Pin Assignments and Descriptions

Pin Name	Level	I/O	Pin#	Description
TCK	LVCMOS Pull up	I	L11	**Test clock**. JTAG input clock used to sample data on the TDI and TDO pins
TDI	LVCMOS Pull up	I	L10	**Test data in.** Input pin for serial data stream to be sent to the S19252. TDI is sampled on the rising edge of TCK.
TMS	LVCMOS Pull up	I	M11	**Test mode select.** Controls the operating mode of the JTAG interface. TMS is sampled on the rising edge of TCK.
TDO	LVCMOS	O	L12	**Test data out.** Output pin for serial data stream from the S19252. TDO is updated on the falling edge of TCK.
TRSTB	LVCMOS Pull down	I	M12	**Test port reset.** Active-low input used to reset the JTAG interface.

Table 25: S19252 MPIO Pin Assignments and Descriptions

Pin Name		Level[1]	I/O	Pin#	Description
Register Control Interface Pins	**MDIO/I2C Device Addressing Pins**				
MPIO_7 (SDA)		I2C	I/O	M16	**Serial Data Line (SDA)**. I2C serial data line. Bi-directional. This bus reads from and writes into the S19252 control logic.
MPIO_6 (SCL)		I2C	I/O	M15	**Serial Clock Line (SCL)**. I2C serial clock line.This pin is used as I2C serial clock line (SCL) when MODE[2:0] = 001. **Reserved address Line.** This address bit is used to uniquely identify each S19252 device MDIO interface mode if multiple S19252 devices are controlled by a single microprocessor and MODE[2:0] = 000.
	ADDRESS4	& LV CMOS Pull down			
MPIO_5 (MDIO) (SPI/SDI)		LV CMOS Pull up	I/O	N15	**Management Data Control Input/Output Bus.** Bi-directional 2-wire bus for efficient control. This bus reads from and writes into most of the S19252 control logic when MODE[2:0] = 000. This pin is used as SDI input signal in the SPI serial interface when MODE[2:0] = 010.
MPIO_4 (MDC) (SPI/SCK)		LV CMOS Pull up	I/O	P15	**Management Clock Control Input.** Clock for Bi-directional MDIO bus when MODE[2:0] = 000. This pin is used as SCK input signal in the SPI serial interface when MODE[2:0] = 010.
MPIO_3 (SPI/SDO)	ADDRESS3	LV CMOS Pull down	I/O	K15	**Reserved address Line.** This address bit is used to uniquely identify each S19252 device for MDIO interface mode if multiple S19252 devices are controlled by a single microprocessor when MODE[2:0] = 000. This pin is used as SDO output signal in the SPI serial interface when MODE[2:0] = 010.
MPIO_2 (SPI/CS)	ADDRESS2	LV CMOS Pull down	I/O	E15	**Reserved address Line.** This address bit is used to uniquely identify each S19252 device for MDIO and I2C interface modes if multiple S19252 devices are controlled by a single microprocessor when MODE[2:0] = 000 or 001. This pin is used as CS input signal in the SPI serial interface when MODE[2:0] = 010.
MPIO_1	ADDRESS1	LV CMOS Pull down	I/O	E17	**Reserved address Line.** This address bit is used to uniquely identify each S19252 device for MDIO and I2C interface modes if multiple S19252 devices are controlled by a single microprocessor.
MPIO_0	ADDRESS0	LV CMOS Pull down	I/O	D13	**Reserved address Lines.** These address bits are used to uniquely identify each S19252 device for MDIO and I2C interface modes if multiple S19252 devices are controlled by a single microprocessor.
MODE_2 MODE_1 MODE_0		LV CMOS Pull down	I	E13 F13 A10	**Operating Mode Selection Control.** These inputs configure the operation mode for the S19252. When these inputs all pulled down, the serial communication is configured as MDIO. See Table 15 and 16 for further info.

Table 25: S19252 MPIO Pin Assignments and Descriptions (Continued)

Pin Name		Level[1]	I/O	Pin#	Description
SCAN-MODE		LV CMOS Pull down	I/O	G16	**Reserved Scan Mode Control.** This active high input puts the chip into scan mode. See Table 15 for further info

1. See Table 16 for termination of serial interface configuration.

Table 26: Power and Ground Pin Assignments and Descriptions

Pin Name	Level	Pin #	Description
VDD_12	+1.2 V	D15, G10, G11, G12, H12, J12, J13, K6, K7, M13, M14, N12	CMOS power supply
VDD_CML_RX	+1.2 V	N9, P9	CML RX power supply
VDD_CML_TX	+1.2 V	F8, F9, G4, H4, H5, J4, J5, K3, K4, K5, L1, L2, L3	CML TX power supply
AVDD_TX	+1.2 V	E5, E6, F5, F6, F7	Transmit analog power supply
AVDD_RX[1]	+1.2 V	P6, P7, P8, R6	Receive analog power supply
AVDD33_PA	+3.3 V	N5, N6, P3, P4, P5, R3, R4, R5, T3, T4, U3, V3	Post-Amp analog power supply
VDD_33	+3.3 V	E8, F12, H13, H14, K12, K13, L13, N13, P10, P11, P14, R12	I/O power supply
VSS	GND	A1, A2, A3, A6, A12, B2, B3, B4, B5, B6, B12, B16, B17, C1, C2, C3, C4, C7, C8, C9, C10, C11, C12, C13, C14, C17, C18, D2, D3, D4, D5, D6, E1, E2, E3, E4, E16, F1, F2, F3, F4, F10, F11, F16, G2, G3, G5, G6, G7, G8, G9, G13, G14, H1, H2, H3, H7, H8, H9, H10, H11, H16, J2, J3, J6, J7, J8, J9, J10, J11, J14, J16, K1, K2, K8, K9, K10, K11, K14, K16, L4, L5, L6, L7, L8, L9, L14, L16, M1, M2, M3, M4, M5, M6, M7, M8, M9, M10, M17, N2, N3, N4, N7, N8, N10, N11, N14, N17, P1, P2, P12, P13, P17, R2, R7, R8, R17, T1, T2, T5, T6, T7, T8, T9, T12, T13, T14, T15, T16, T17, T18, U2, U4, U5, U6, U7, U10, U11, U16, V1, V2, V4, V7, V16	Ground
NC		H6	No Connection (Float)

1. AVDD_RX is susceptible to power supply transient noise. A linear regulator is recommended. See transient level in Table 30.

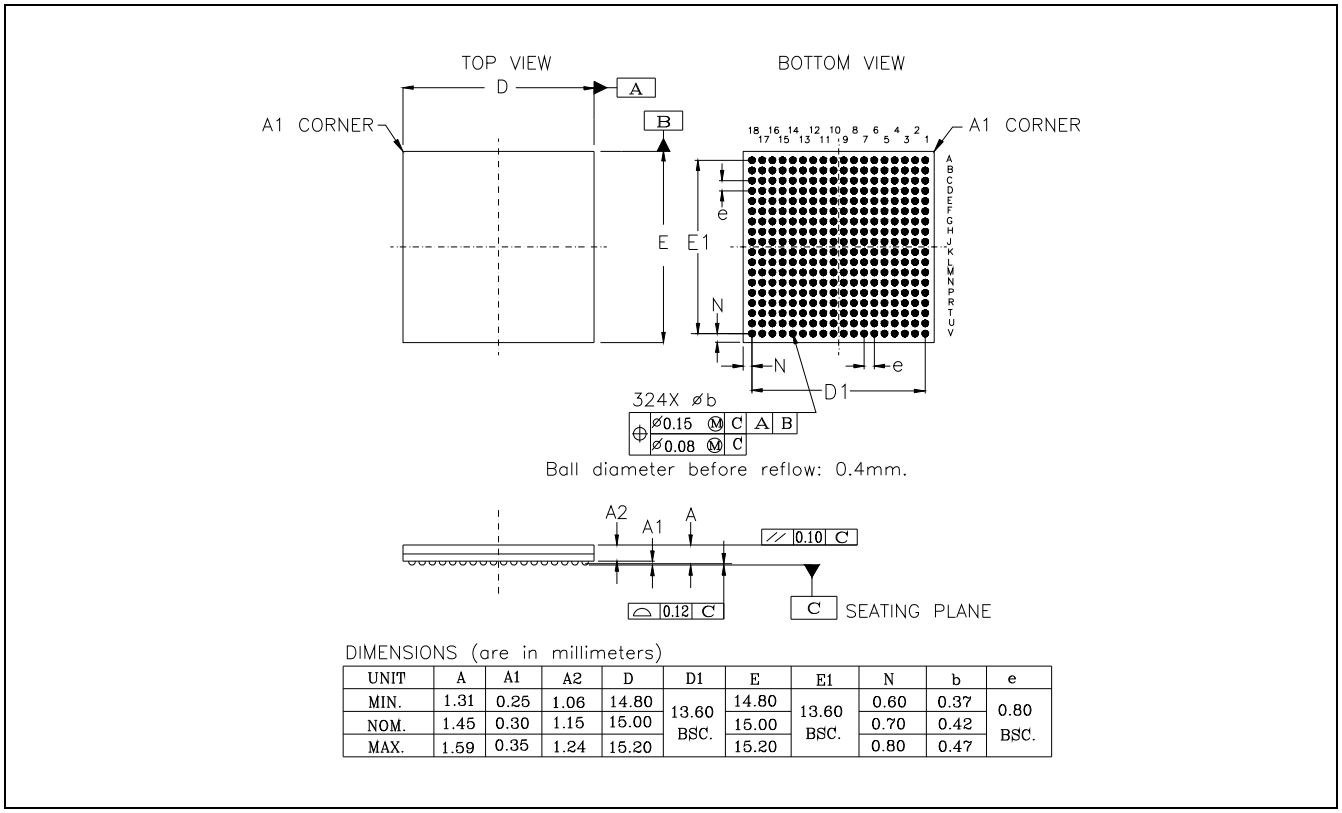
S19252 – 324 PBGA Pinout - 0.8 mm Pitch (Bottom View) Data_swap = 0

Figure 12: S19252 – 324 PBGA Pinout - 0.8 mm Pitch (Bottom View) Data_swap = 0

	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	PINN14	PINP10	PINN10	PINN11	PICLKN	PINP0	VSS	PINP1	MODE_0	PCLKN	PD_UPP	CSUINN	VSS	TXCAP2	TXCAP1	VSS	VSS	VSS
B	PINP14	VSS	VSS	PINP11	PICLKP	PINN0	VSS	PINN1	RXPD	PCLKP	PD_UPN	CSUINP	VSS	VSS	VSS	VSS	VSS	TSCLKP
C	VSS	VSS	PINP6	PINN6	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	REFCLKAN	REFCLKAP	VSS	VSS	VSS	VSS
D	PINN5	PINP15	PINN15	VDD_12	PINP7	MPIO_0	PINP2	PINN3	TX_155MCKP	REFCLKBP	REFCLKBN	PD_DWNP	VSS	VSS	VSS	VSS	VSS	TSCLKN
E	PINP5	MPIO_1	VSS	MPIO_2 (SPI/CS)	PINN7	MODE_2	PINN2	PINP3	TX_155MCKN	TXPD	VDD_33	PD_DWNN	AVDD_TX	AVDD_TX	VSS	VSS	VSS	VSS
F	PINP13	PINN13	VSS	PINN9	PINP9	MODE_1	VDD_33	VSS	VSS	VDD_CML_TX	VDD_CML_TX	AVDD_TX	AVDD_TX	AVDD_TX	VSS	VSS	VSS	VSS
G	PINP4	PINN4	SCAN-MODE	RESETB	VSS	VSS	VDD_12	VDD_12	VDD_12	VSS	VSS	VSS	VSS	VSS	VDD_CML_TX	VSS	VSS	TSDP
H	PINP8	PINN8	VSS	RXLOCK-DET	VDD_33	VDD_33	VDD_12	VSS	VSS	VSS	VSS	VSS	NC	VDD_CML_TX	VDD_CML_TX	VSS	VSS	VSS
J	PINN12	PINP12	VSS	TXLOCK-DET	VSS	VDD_12	VDD_12	VSS	VSS	VSS	VSS	VSS	VSS	VDD_CML_TX	VDD_CML_TX	VSS	VSS	TSDN
K	POUTN15	POUTP15	VSS	MPIO_3 (SPI/SDO)	VSS	VDD_33	VDD_33	VSS	VSS	VSS	VSS	VDD_12	VDD_12	VDD_CML_TX	VDD_CML_TX	VDD_CML_TX	VSS	VSS
L	POUTN14	POUTP14	VSS	TXRXA-LARM	VSS	VDD_33	TDO	TCK	TDI	VSS	VSS	VSS	VSS	VSS	VSS	VDD_CML_TX	VDD_CML_TX	VDD_CML_TX
M	POCLKN	VSS	MPIO_7 (SDA)	MPIO_6 (SCL)	VDD_12	VDD_12	TRSTB	TMS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
N	POCLKP	VSS	POUTP13	MPIO_5 (MDIO) (SPI/SDI)	VSS	VDD_33	VDD_12	VSS	VSS	VDD_CML_RX	VSS	VSS	AVDD33_PA	AVDD33_PA	VSS	VSS	VSS	CENTER TAP
P	POUTN11	VSS	POUTN13	MPIO_4 (MDC) (SPI/SCK)	VDD_33	VSS	VSS	VDD_33	VDD_33	VDD_CML_RX	AVDD_RX	AVDD_RX	AVDD_RX	AVDD33_PA	AVDD33_PA	AVDD33_PA	VSS	VSS
R	POUTP11	VSS	POUTN7	POUTP7	POUTN8	POUTP8	VDD_33	POUTP5	POUTP0	LOS_SD	VSS	VSS	AVDD_RX	AVDD33_PA	AVDD33_PA	AVDD33_PA	VSS	SERDATP
T	VSS	VSS	VSS	VSS	VSS	VSS	VSS	POUTN5	POUTN0	VSS	VSS	VSS	VSS	VSS	AVDD33_PA	AVDD33_PA	VSS	VSS
U	POUTN12	POUTN10	VSS	POUTP9	POUTP6	POUTN3	POUTP2	VSS	VSS	POUTP4	RXMCKP	VSS	VSS	VSS	VSS	AVDD33_PA	VSS	SERDATN
V	POUTP12	POUTP10	VSS	POUTN9	POUTN6	POUTP3	POUTN2	POUTN1	POUTP1	POUTN4	RXMCKN	VSS	RXCAP2	RXCAP1	VSS	AVDD33_PA	VSS	VSS

S19252 – 324 PBGA 0.8 mm Pitch Package Mechanical Drawing

Figure 13: S19252 – 324 PBGA 0.8 mm Pitch Package Mechanical Drawing



DIMENSIONS (are in millimeters)

UNIT	A	A1	A2	D	D1	E	E1	N	b	e
MIN.	1.31	0.25	1.06	14.80	13.60 BSC.	14.80	13.60 BSC.	0.60	0.37	0.80 BSC.
NOM.	1.45	0.30	1.15	15.00		15.00		0.70	0.42	
MAX.	1.59	0.35	1.24	15.20		15.20		0.80	0.47	

PACKAGE MATERIAL NOTE:
Standard Package: Ball Composition - 63/37 Sn/Pb.
RoHS Compliant Package: Ball Composition - 96.5/3.0/0.5 Sn/Ag/Cu.

Table 27: Thermal Management (0.8 mm Pitch Package)[1]

Device	Θjc	Θja	Airflow
S19252	8.8 °C/Watt	33.4 °C/Watt	0 LFM[2]
		28.2 °C/Watt	100 LFM[2]
		26.7 °C/Watt	200 LFM[2]

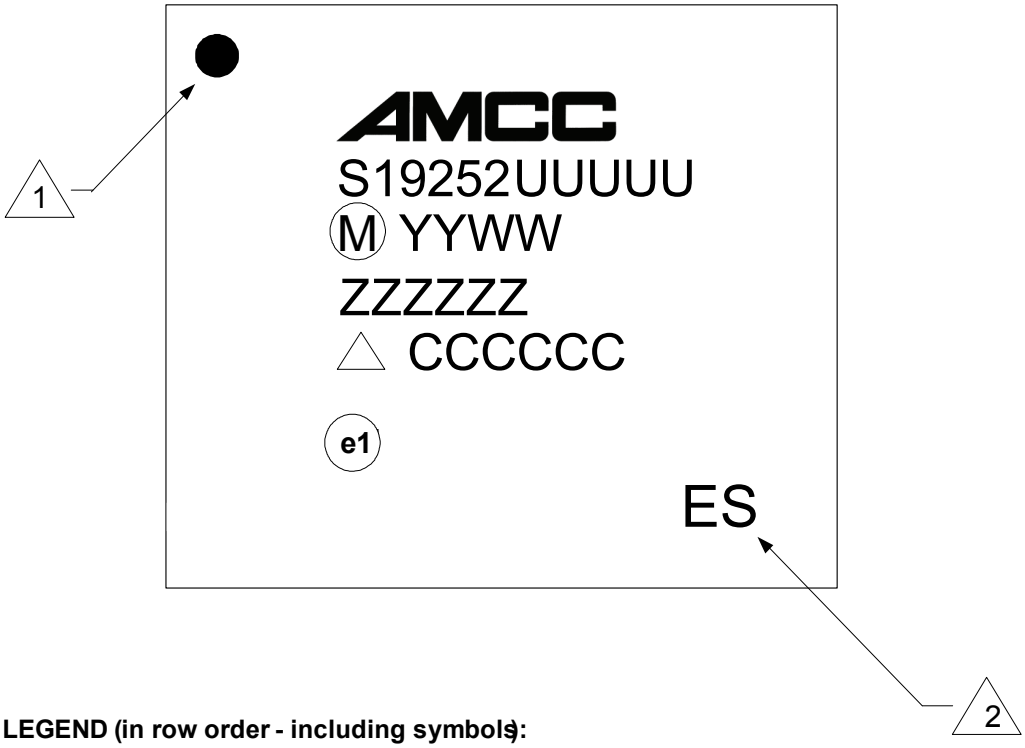
1. Θja values can be used in conjunction with the desired ambient temperature and device power consumption to determine the available thermal margin in the device. Consult application note GAN2001 for more details on thermal resistance calculations.
2. When the device is used without airflow or insufficient airflow, a heatsink is required.

S19252 – 324 PBGA Package Marking Drawing

Figure 14: S19252 – 324 PBGA Package Marking Drawing (Top View)

NOTES (Unless Otherwise Specified):

1. Dot Represents PIN1 (A01) Designator
2. ES (Engineering Sample) designator. When present, this signifies pre-production grade material. Pre-production material is not guaranteed to meet the specifications in this document.



LEGEND (in row order - including symbols):

ROW #1:		AMCC Logo
ROW #2:		AMCC Device Part Number UUUUU. Listed options (See ordering Information)
ROW #3:	M	Mask Protection Symbol YY: Assembly Year Code WW: Assembly Week Code
ROW #4:		ZZZZZZ AMCC 6: Digit Lot Code
ROW #5:	△	ESD Symbol CCCCCC: Assembly Location (Country of Origin)
ROW #6:	e1	RoHS Compliant Symbol (per JEDEC: JESDE97). When present, this signifies a lead free second level interconnect
ROW #7:		Engineering Sample (ES) Designator (only on Pre-Production Devices).

Performance Specifications

Table 28: Performance Specifications

Parameter	Min	Typ	Max	Units	Conditions
CSU and CRU VCO Specifications					
Nominal VCO Center Frequency (CSU and CRU)	9.95		11.32	GHz	
TX and RX VCO frequency ([T/R]X_VCO_Range = 00)	9.95		10.00	GHz	Refer to Application Note AN2019 for Data Rate Selection Register Control Settings VCO frequency guaranteed with ± 600 ppm offset
TX and RX VCO frequency ([T/R]X_VCO_Range = 01)	10.30		10.32	GHz	
TX and RX VCO frequency ([T/R]X_VCO_Range = 10)	10.51		10.71	GHz	
TX and RX VCO frequency ([T/R]X_VCO_Range = 11)	11.00		11.32	GHz	
Frequency difference at which the receive PLL goes out of lock (CRU_REFCLK compared to the divided down VCO clock). LOCKDET is de-asserted when PLL goes out of lock.	± 350		± 600	ppm	
Frequency difference at which receive PLL goes into lock (CRU_REFCLK compared to the divided down VCO clock). LOCKDET is asserted 0.5 ms after PLL goes into lock.	± 220		± 530	ppm	LOCKDET “into lock” status is only valid when the incoming data is within ±800 ppm of the VCO clock. Note the VCO clock is a multiple of the CRU_REFCLK when out of lock.
CRU Acquisition phase lock time			500	us	After the release of RSTB, with device already powered up and with a valid CRU_REFCLK. Guaranteed but not tested.
SONET Jitter Specifications					
SONET J_{tol} Jitter Tolerance (SERDATIP/N) with PAEQUADJ[2:0] = 0,0,0	See Figure 8			UI (p-p)	10 Hz – 2.4 kHz (Sinusoidal)
				UI (p-p)	2.4 kHz – 24 kHz (Sinusoidal)
				UI (p-p)	24 kHz – 400 kHz (Sinusoidal)
				UI (p-p)	400 kHz – 4 MHz (Sinusoidal)
				UI (p-p)	4 MHz–80 MHz (Sinusoidal) SONET spec of 0.15 UI is met across the entire range of 9.95 to 10.709 GHz

Table 28: Performance Specifications (Continued)

Parameter	Min	Typ	Max	Units	Conditions
SONET J_{tr} jitter transfer Internal RSCLK to TSD in RLPTIME mode with the use of external VCO			See Figure 7	dB	0 Hz – 120 kHz
				dB	> 120 kHz*
SONET Jitter Generation - Measurements with Reference Clock Phase Noise as shown in Figures 20 and 21.					
J_{gen} jitter generation (9.95G rate) TSD (Normal Mode with 622.08 MHz CSU_REFCLK, TAP2=3)		2.4	5.5	mUI (RMS)	In-lock, for 4 MHz to 80 MHz B.W. SONET pattern with PRBS31 bulk filled
		15	35	mUI (p-p)	
J_{gen} jitter generation (10.709G rate) TSD (Normal Mode with 622.08 MHz CSU_REFCLK, TAP2=5)		2.7	6.0	mUI (RMS)	
		19	50	mUI (p-p)	
J_{gen} jitter generation (9.95G rate) TSD (Normal Mode with 622.08 MHz CSU_REFCLK, TAP2=3)		3.4	6.0 [1]	mUI (RMS)	In-lock, for 50 kHz to 80 MHz B.W. SONET pattern with PRBS31 bulk filled
		27	45	mUI (p-p)	
J_{gen} jitter generation (10.709G rate) TSD (Normal Mode with 622.08 MHz CSU_REFCLK, TAP2=5)		3.6	6.5	mUI (RMS)	
		32	55	mUI (p-p)	
J_{gen} Jitter Generation (9.95G rate) TSD (Normal Mode with 155.52 MHz CSU_REFCLK, TAP2=3)		2.4	6.0	mUI (RMS)	In-lock, for 4 MHz to 80 MHz B.W. SONET pattern with PRBS31 bulk filled
		15	35	mUI (p-p)	
J_{gen} Jitter Generation (10.709G rate) TSD (Normal Mode with 155.52 MHz CSU_REFCLK, TAP2=5)		2.9	6.5	mUI (RMS)	
		21	50	mUI (p-p)	
J_{gen} Jitter Generation (9.95G rate) TSD (Normal Mode with 155.52 MHz CSU_REFCLK, TAP2=3)		5.7	8.5	mUI (RMS)	In-lock, for 50 kHz to 80 MHz B.W. SONET pattern with PRBS31 bulk filled
		60	100	mUI (p-p)	
J_{gen} Jitter Generation (10.709G rate) TSD (Normal Mode with 155.52 MHz CSU_REFCLK, TAP2=5)		5.5	8.0	mUI (RMS)	
		55	85	mUI (p-p)	

Table 28: Performance Specifications (Continued)

Parameter	Min	Typ	Max	Units	Conditions
J_{gen} jitter generation (9.95G rate) TSD (RLPTIME, XVCO 622 Mode, TAP2=5)		2.7	5.5	mUI (RMS)	In-lock, integrated phase noise of the external VCO should be -54dBc or better within 4 MHz to 80 MHz B.W. SONET pattern with PRBS31 bulk filled
J_{gen} (10.709G rate)		2.3	6.0	mUI (RMS)	
J_{gen} jitter generation (9.95G rate) TSD (RLPTIME, XVCO 155 Mode, TAP2=5)		2.3	6.0	mUI (RMS)	
J_{gen} (10.709G rate)		2.9	6.5	mUI (RMS)	
J_{gen} jitter generation (9.95G rate) TSD (RLPTIME, XVCO 622 Mode, TAP2=5)		3.8	6.0	mUI (RMS)	In-lock, integrated phase noise of the external VCO should be -54dBc or better within 50 kHz to 80 MHz B.W. SONET pattern with PRBS31 bulk filled
J_{gen} (10.709G rate)		3.3	6.5	mUI (RMS)	
J_{gen} jitter generation (9.95G rate) TSD (RLPTIME, XVCO 155 Mode, TAP2=5)		5.4	8.5	mUI (RMS)	
J_{gen} (10.709G rate)		4.7	8.0	mUI (RMS)	
10 Gigabit Ethernet and XFP (XFI) Jitter Specifications					
Receiver Jitter Tolerance J_{tol} - 10GbE & 10GFC (Figure 15, Point D)	0.65 TJ			UI_{pp}	• SONET OC-192 framed data, payload filled with PRBS31 • 10.3125 Gbps • 50 mV differential input
	0.05 DCD			UI_{pp}	
	0.30 DDJ			UI_{pp}	
	0.25 RJ			UI_{pp}	
	0.05 SJ			UI_{pp}	See Figures 10
Receiver Jitter Tolerance J_{tol} - SONET/ SDH/G.709 (Figure 15, Point D)	0.3	0.6		UI_{pp}	SONET OC-192 framed data, payload filled with PRBS23, 9.953 Gbps and 10.709 Gbps
Sinusoidal Jitter Tolerance (Receiver)	See Figures 18 and 19 for the Telecom and Datacom mask				
Eye Mask X1 (Receiver)			0.325	UI	See Figure 17, X1=0.225 if total non DDJ is measured
Eye Mask Y1 (Receiver)	55			mV	See Figure 17.
Eye Mask Y2 (Receiver)			525	mV	See Figure 17.
Transmitter Output Jitter for Datacom (Figure 15, Point A, Broadband Jitter)			0.20	UI_{pp}	10.3125 Gbps (CJTPAT pattern, DIV66 REFCLK)
Deterministic Jitter TSD (Transmitter) (Figure 15, Point A)			0.15	UI (p-p)	Normal Mode. (CJTPAT pattern, DIV66 REFCLK)
Total Jitter TSD (Transmitter) (Figure 15, Point A)			0.30	UI (p-p)	Normal Mode. (CJTPAT pattern, DIV66 REFCLK)
Eye Mask X1 (Transmitter)			0.15	UI	See Figure 16.

Table 28: Performance Specifications (Continued)

Parameter	Min	Typ	Max	Units	Conditions
Eye Mask X2 (Transmitter)			0.40	UI	See Figure 16.
Eye Mask Y1 (Transmitter)	180			mV	See Figure 16.
Eye Mask Y2 (Transmitter)			385	mV	See Figure 16.
J_{gen} jitter generation TSD (Normal Mode with 622.08 MHz CSU REFCLK)		3.6	6.5	mUI (RMS)	In-lock, 50kHz to 8MHz B.W. From 9.9 GHz to 10.709 GHz
J_{gen} jitter generation TSD (Normal Mode with 622.08MHz CSU REFCLK)		32	55	mUI (p-p)	In-lock, 50kHz to 8MHz B.W. From 9.9 GHz to 10.709 GHz
J_{gen} jitter generation TSD (Normal Mode with 155 MHz CSU REFCLK)		5.5	8.0	mUI (RMS)	In-lock, 50kHz to 8MHz B.W. From 9.9 GHz to 10.709 GHz
J_{gen} jitter generation TSD (Normal Mode with 155 MHz CSU REFCLK)		55	85	mUI (p-p)	In-lock, 50kHz to 8MHz B.W. From 9.9 GHz to 10.709 GHz
SFP+ (SFI) Jitter Specifications					
Total Jitter TSD (Transmitter) (Figure 15, Point B)			0.16	UI (p-p)	≤ 11.1 Gbps (SPAT pattern, DIV64 REFCLK)
Data Dependent Jitter TSD (Transmitter) [2] (Figure 15, Point B)			0.07	UI (p-p)	≤ 11.1 Gbps (SPAT pattern, DIV64 REFCLK)
Uncorrelated Jitter TSD (Transmitter) (Figure 15, Point B)			7	mUI (RMS)	≤ 11.1 Gbps (SPAT pattern, DIV64 REFCLK)
Eye Mask X1 (Transmitter)			0.14	UI	See Figure 16.
Eye Mask X2 (Transmitter)			0.35	UI	See Figure 16.
Eye Mask Y1 (Transmitter)	90			mV	See Figure 16.
Eye Mask Y2 (Transmitter)			350	mV	See Figure 16.
J_{gen} jitter generation TSD (Normal Mode with 155 MHz CSU REFCLK), (Figure 15, Point B)			70	mUI (p-p)	In-lock, 4MHz to 80MHz B.W. From 9.9 GHz to 11.1 GHz
J_{gen} jitter generation TSD (Normal Mode with 155 MHz CSU REFCLK), (Figure 15, Point B)			210	mUI (p-p)	In-lock, 50kHz to 80MHz B.W. From 9.9 GHz to 11.1 GHz
Receiver Jitter Tolerance J_{tol} - 10GbE & 10GFC (Figure 15, Point C)	0.7 TJ			UI_{pp}	BER 1E-12
	0.42 DJ			UI_{pp}	
Eye Mask X1 (Receiver)			0.35	UI	See Figure 17, X1=0.225 if total non DDJ is measured
Eye Mask Y1 (Receiver)	150			mV	See Figure 17.

Table 28: Performance Specifications (Continued)

Parameter	Min	Typ	Max	Units	Conditions
Eye Mask Y2 (Receiver)			425	mV	See Figure 17.
Receiver LOS					
LOS Assert time			100	µS	
LOS De-assert time			100	µS	
LOS Assert Voltage	8		400	mV_{pp}	Differential (minimum run length of 4)
LOS De-assert Voltage	10		400	mV_{pp}	Differential (minimum run length of 4)
Reference Clock Specifications					
Reference clock frequency tolerance (CSU_REFCLK)	-100		+100	ppm	± 20 ppm is required to meet SONET output frequency specification.
CSU or CRU reference clock input duty cycle	45		55	%	
Reference clock rise and fall times for 155.52 MHz (or equivalent FEC/10 Gigabit Ethernet rate) CSU_REFCLK and CRU_REFCLK.	0.2		0.8	ns	20% to 80% of amplitude.
Reference clock rise and fall times for 622.08 MHz (or equivalent FEC/10 Gigabit Ethernet rate) CSU_REFCLK.	0.1		0.3	ns	20% to 80% of amplitude.
CSU_IN (External VCO Output) duty cycle	45		55	%	
CSU_IN (External VCO Output) rise and fall times	0.1		0.3	ns	20% to 80% of amplitude.
High Speed Input (SERDATI) Specifications					
High-Speed Input Sensitivity - SERDATIP/N serial input data (when driven differentially) 9.95328 Gbps Data Rate	10			mV	Differential measurement. BER better than 10^{-12} with PRBS 2^{31} -1 jitter free input data and equalization turned on and optimized
High-Speed Input Sensitivity - SERDATIP/N serial input data (when driven differentially) 10.709 Gbps Data Rate	11			mV	Differential measurement. BER better than 10^{-12} with PRBS 2^{31} -1 jitter free input data and equalization turned on and optimized
High-Speed Input Sensitivity - SERDATIP/N serial input data (when driven differentially) 11.3 Gbps Data Rate	15			mV	Differential measurement. BER better than 10^{-12} with PRBS 2^{31} -1 jitter free input data and equalization turned on and optimized

Table 28: Performance Specifications (Continued)

Parameter	Min	Typ	Max	Units	Conditions
High-Speed Input Sensitivity - SERDATIP/N serial input data (when driven single-ended) 9.95328 Gbps Data Rate	10			mV	Single-ended [3] measurement. BER better than 10^{-12} with PRBS 2^{31}-1 jitter free input data and equalization turned on and optimized
High-Speed Input Sensitivity - SERDATIP/N serial input data (when driven single-ended) 10.709 Gbps Data Rate	11			mV	Single-ended [3] measurement. BER better than 10^{-12} with PRBS 2^{31}-1 jitter free input data and equalization turned on and optimized
High-Speed Input Sensitivity - SERDATIP/N serial input data (when driven single-ended) 11.3 Gbps Data Rate	15			mV	Single-ended [3] measurement. BER better than 10^{-12} with PRBS 2^{31}-1 jitter free input data and equalization turned on and optimized
L_{CID} consecutive identical digits at serial Data Input			80	bits	Number of bits with no transitions (ITU spec is 72)
Other Specifications					
LVCMOS Frequency of Operation			10	MHz	
LVCMOS Rise Time (20% - 80%)	1		15	ns	10pFcapacitive load
LVCMOS Fall Time (20% - 80%)	1		15	ns	
Power Sequencing Requirement	NONE				

1. Jitter generation Max value (Normal Mode with 622.08 MHz CSU_REFCLK) is 3.0 mUI (RMS) with condition: In-lock, for 50 KHz to 80 MHz B.W. 1010 pattern.
2. Transmitter DDJ (with a PRBS9 pattern) is SFP+ compliant for FR4 lengths with less than 3.6db of loss. The requirement is up to 6.0db of loss.
3. The unused input is terminated through a series 50 ohm resistor and capacitor to GND on the test board.

Figure 15: S19252 with XFP System Performance Points

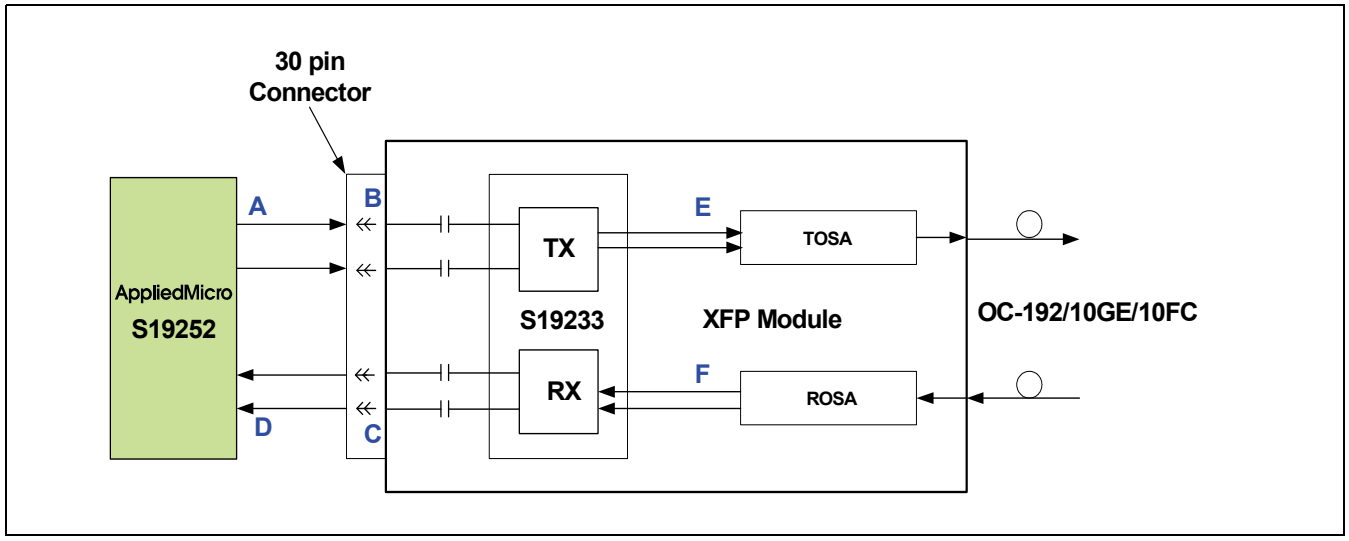


Figure 16: XFI Transmitter Differential Output Compliance Mask

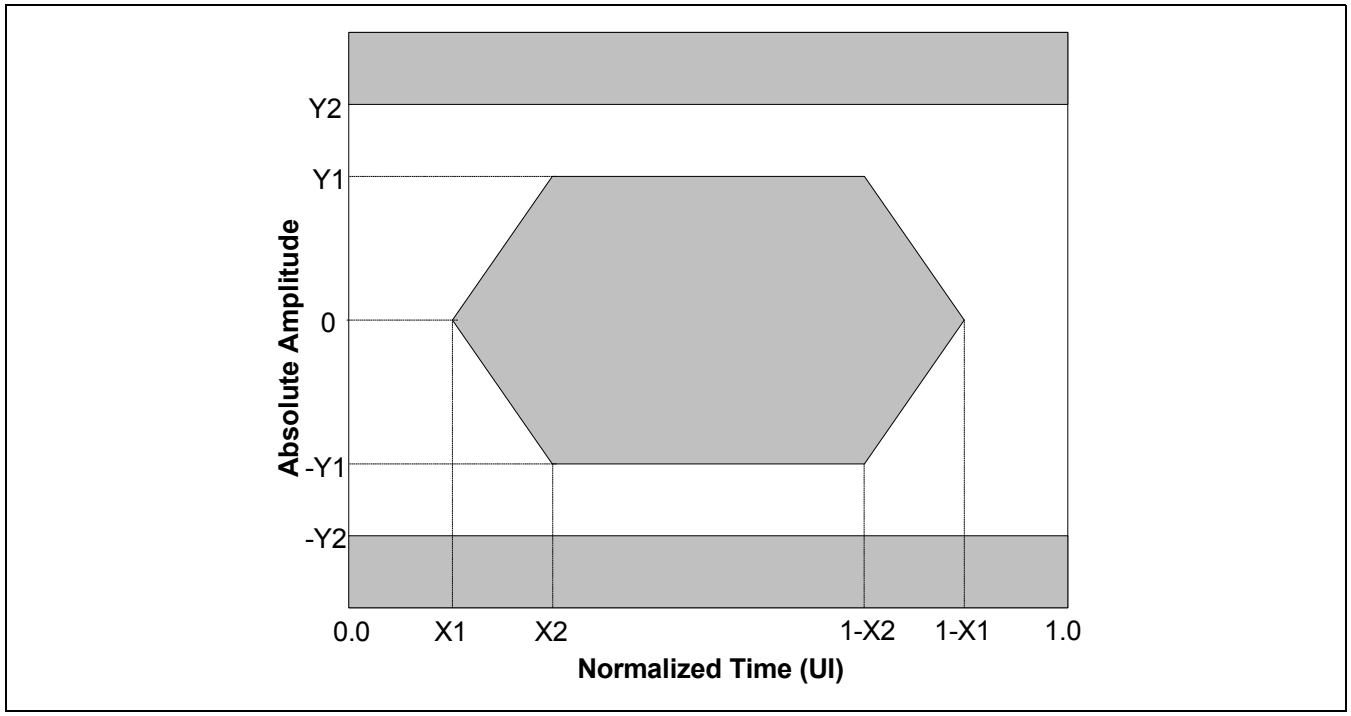


Figure 17: XFI Receiver Differential Input Compliance Mask

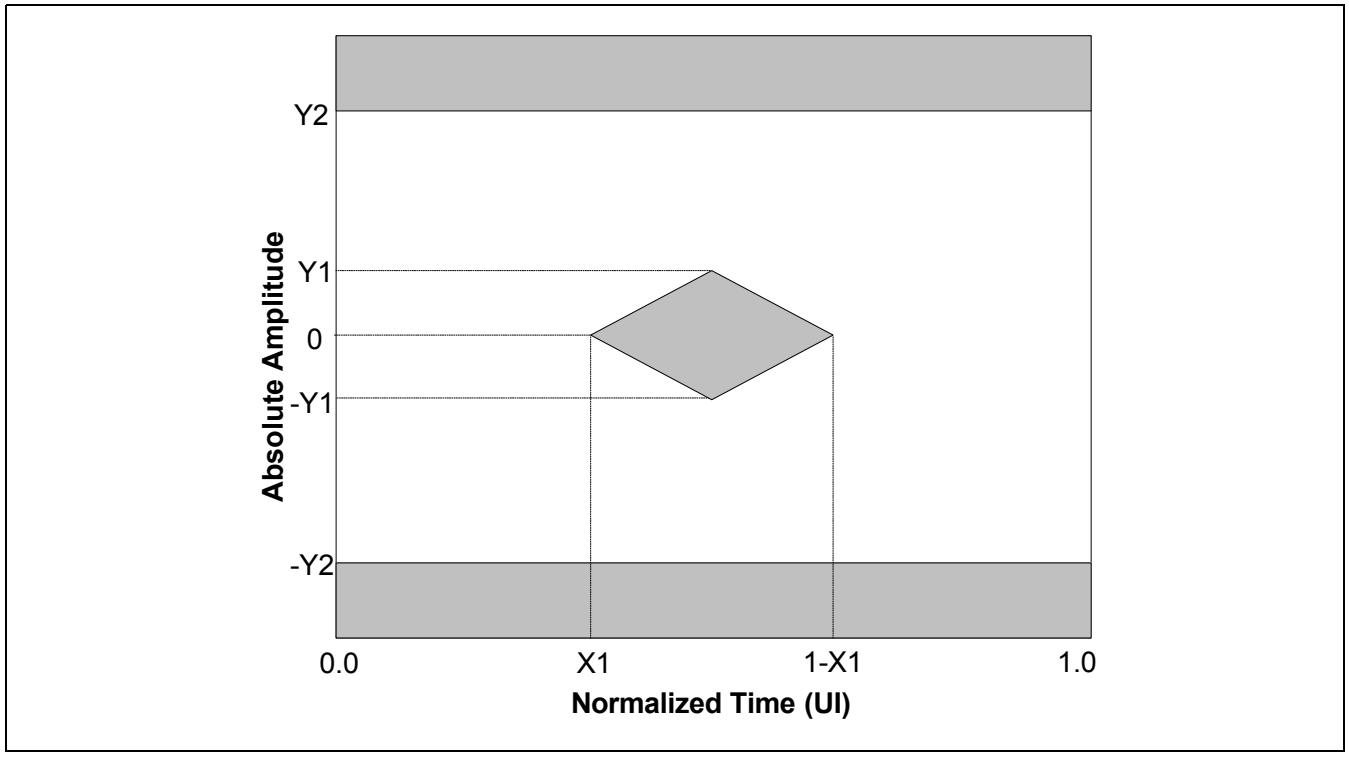


Figure 18: XFI Receiver Input Telecom Sinusoidal Jitter Tolerance

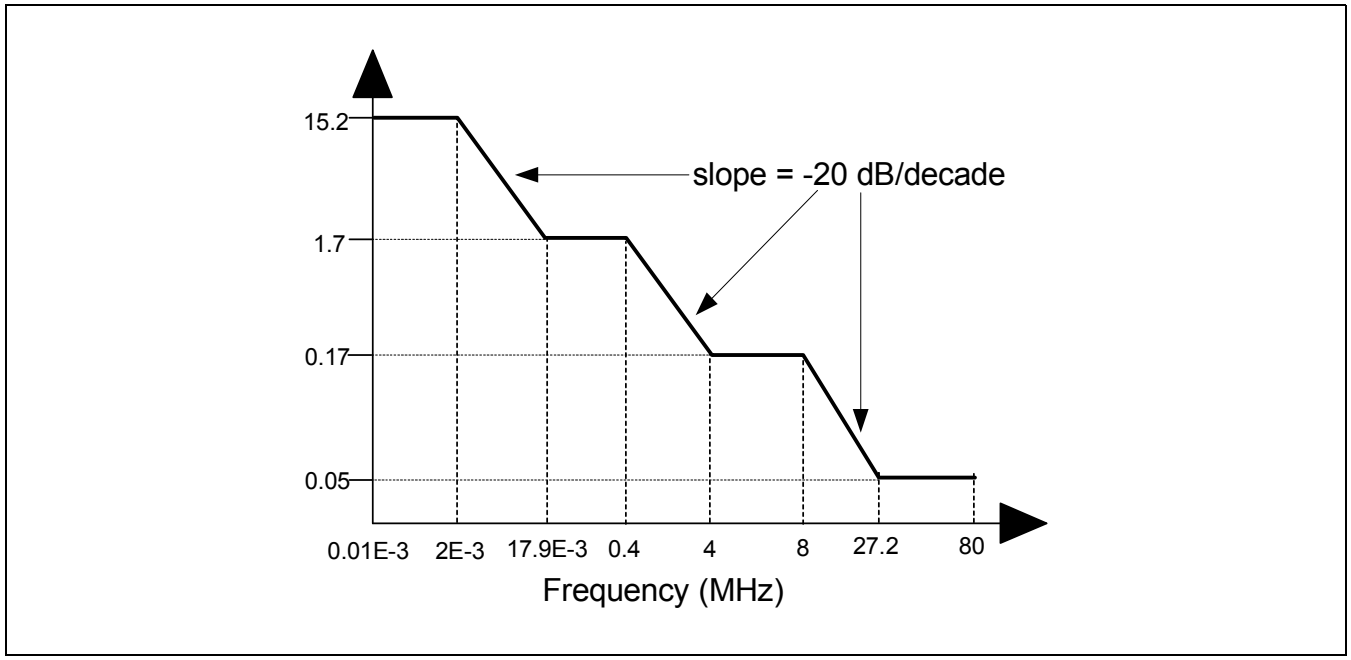


Figure 19: XFI Receiver Input Datacom Sinusoidal Jitter Tolerance

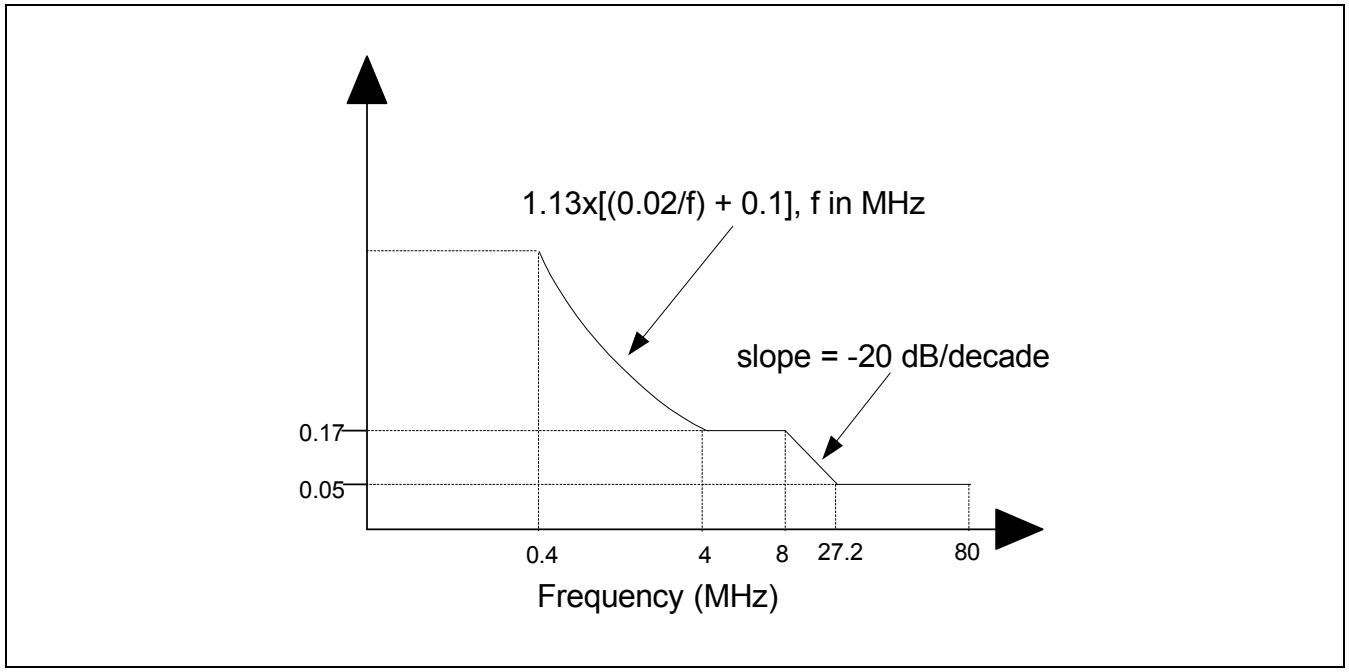


Figure 20: 622.08 MHz CSU_REFCLK Phase Noise

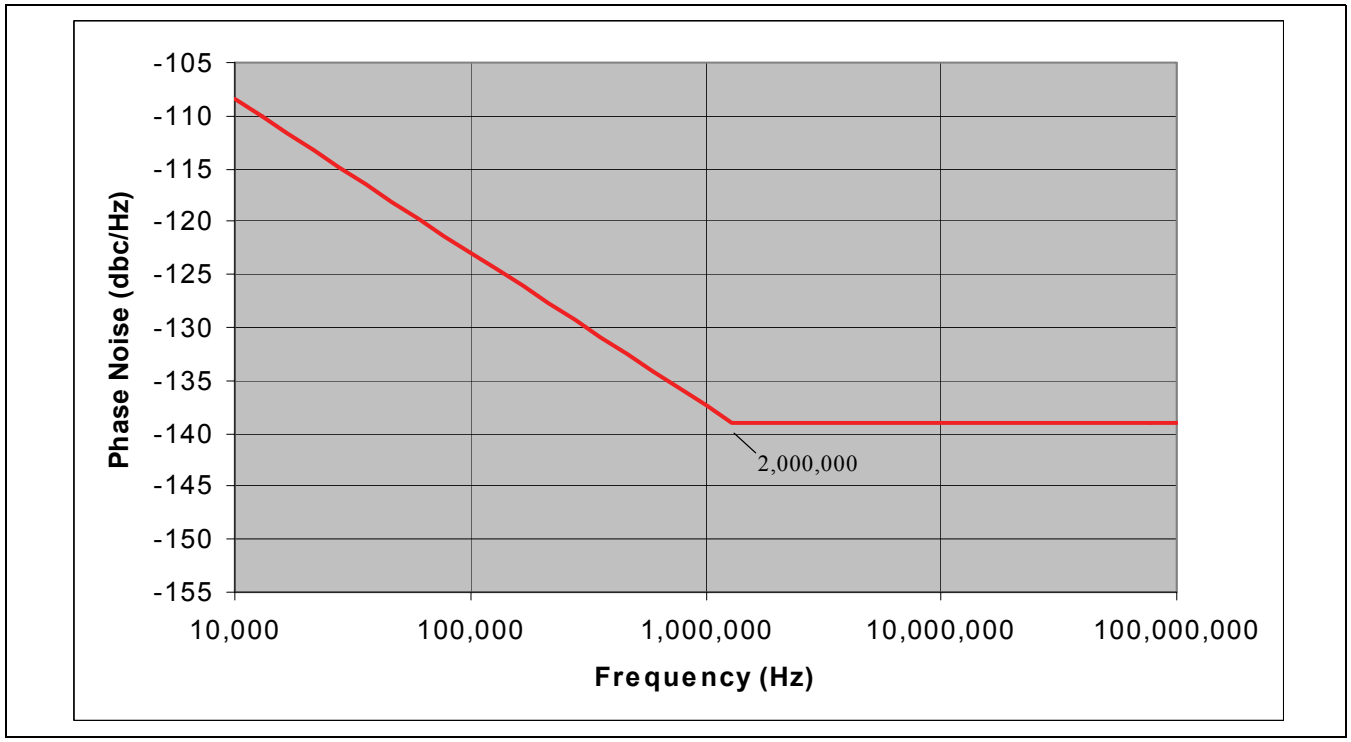
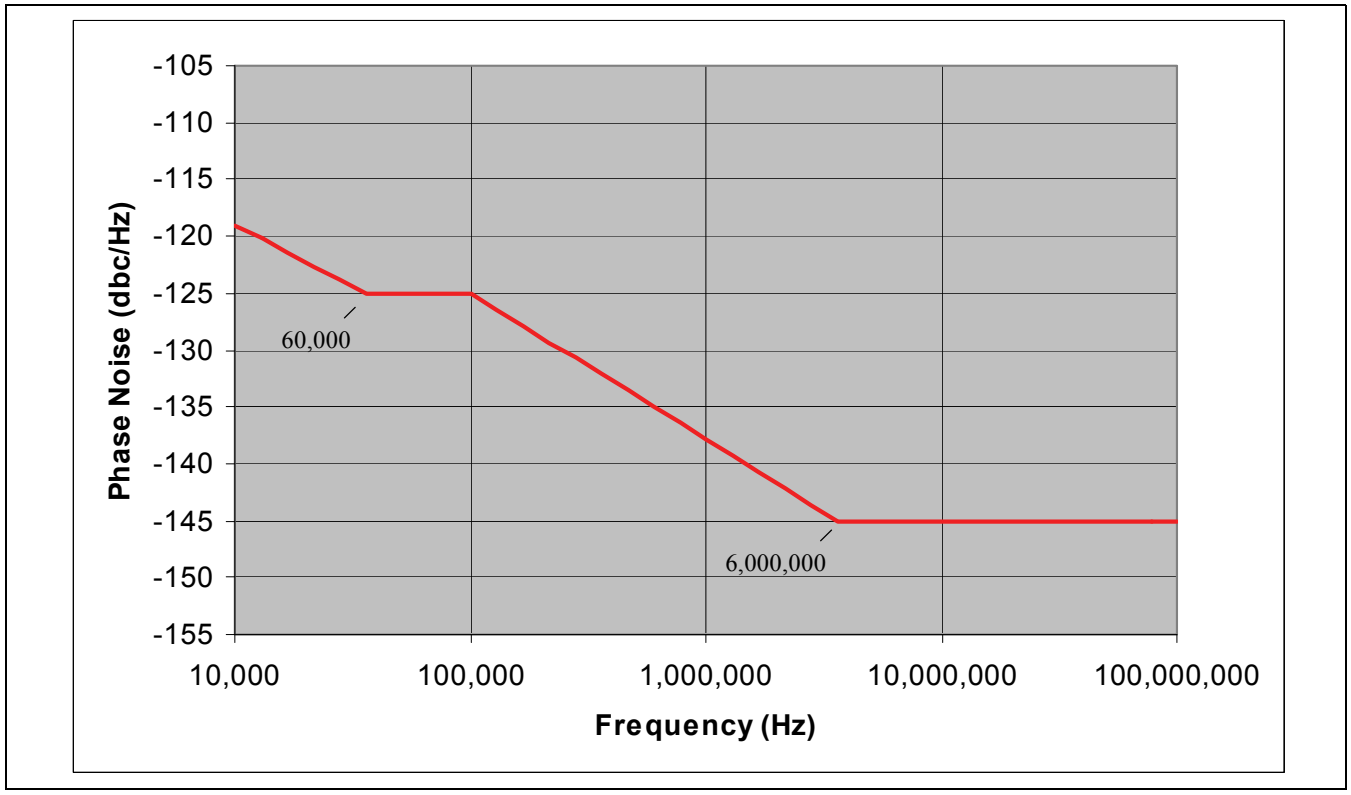


Figure 21: 155.52 MHz CSU_REFCLK Phase Noise



Electrical Specifications

Table 29: Absolute Maximum and Minimum Ratings

The following are the absolute maximum stress ratings for the S19252 device. Stresses beyond those listed may cause permanent damage to the device. Absolute maximum ratings are stress ratings only, and operation of the device at the maximums stated or at any other conditions beyond those indicated in the "Recommended Operating Conditions" of the document is not inferred. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Min	Typ	Max	Units	Conditions
Storage temperature	-55		150	°C	
V_{DD} 1.2 V supply	-0.2		1.3	V	
VDD 3.3 V supply	-0.2		3.575	V	
CML input voltage	-0.5		$V_{DD\_1.2V}$ +0.2	V	
LVCMOS control input voltage	-0.5		$V_{DD\_3.3V}$ +0.2	V	
LVDS input voltage	-0.5		+2.4	V	
CML output current per pin			8	mA	
CML input current per pin			8	mA	
LVCMOS output current per pin			2	mA	
LVCMOS input current per pin			1	mA	
LVDS output current per pin			4	mA	
LVDS input current per pin			2	mA	
Electrostatic Discharge (ESD) Exposure [1]: Human Body Model (HBM)			2000	V	All pins pass except those listed below
			1500	V	SERDATI[P/N] and CENTER_TAP pins pass
			1C		Device JESD22-A114-B Class Rating

1. The S19252 is rated to the following ESD voltages based upon JEDEC standard: JESD22-A114-B. Adherence to standards for ESD protection should be taken during the handling of the devices to ensure that the devices are not damaged. The standards to be used are defined in ANSI standard ANSI/ESD S20.20-1999, "Protection of Electrical and Electronic Parts, Assemblies and Equipment." Contact your local FAE or sales representative for applicable ESD application notes.

Table 30: Recommended Operating Conditions

The device will meet all electrical specifications at junction temperature under bias of 125°C but part lifetime and reliability may be reduced. It is recommended that prudent thermal management techniques are used to maximize device lifetime.

Parameter	Min	Typ	Max	Units
Ambient temperature under bias	-40		+85	°C
Junction temperature under bias			+125	°C
Voltage on $V_{DD\_1.2\ V}$ with respect to GND	1.14	1.20	1.26	V
Voltage on $V_{DD\_3.3\ V}$ with respect to GND	3.135	3.3	3.465	V
$I_{CC\_1.2\ V}$ supply current		551	694	mA
$I_{CC\_3.3\ V}$ supply current		174	213	mA
1. Power dissipation (at power up reset with no 10G CLKOUT, no LOS/RSSI, and no FFE) (when using 1.2 V and 3.3 V supplies)		1.08	1.39[1]	W
2. Power dissipation (at power up reset with no 10G CLKOUT, LOS/RSSI enabled, and no FFE) (when using 1.2 V and 3.3 V supplies)		1.19	1.54[1]	W
3. Power dissipation (default at power up reset with no 10G CLK-OUT, no LOS/RSSI, and FFE enabled) (when using 1.2 V and 3.3 V supplies)		1.10	1.41[1]	W
4. Power dissipation (at power up reset with 10G CLKOUT enabled, no LOS/RSSI, and no FFE) (when using 1.2 V and 3.3 V supplies)		1.11	1.43[1]	W
5. Power dissipation (at power up reset with 10G CLKOUT, LOS/RSSI, and FFE enabled) (when using 1.2 V and 3.3 V supplies)		1.21	1.61[1]	W
Power supply transient pulse (slope) rejection for 1.2 V power supply (1 Hz to 10 KHz)	200			uS (10% - 90%)
Power supply transient pulse (amplitude) rejection for 1.2 V power supply (1 Hz to 10 KHz)			10	mV_{P-P}
Power supply noise rejection for 1.2 V power supply (6 kHz – 2 MHz)			50	mV_{P-P}
Power supply noise rejection for 3.3V power supply (6 kHz – 2 MHz)			50	mV_{P-P}

1. Use maximum Power Dissipation and Table 27 for Thermal Management considerations.

Table 31: LVCMOS Input/Output Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{IH}	Input high-voltage	2.0			V	
V_{IL}	Input low-voltage			0.65	V	
I_{IH}	Input high current			45	µA	
I_{IL}	Input low current			30	µA	
V_{OH}	Output high-voltage	2.4			V	I_{OH} = 600 µA
V_{OL}	Output low-voltage			0.4	V	I_{OL} = -600 µA

Table 32: High-Speed CML Input/Output Characteristics (TSD, TSCLK, SERDATI)

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{ODIFF}	Serial Output Differential Voltage Default: Low Swing [1]	400		700	mV	Output loading is 100 Ω line-to-line. See Figure 29.
	High Swing [2]	700		1100		
$V_{OSINGLE}$	Serial Output Single Ended Voltage, Default: Low Swing [1]	200		350	mV	Output loading is 100 Ω line-to-line. See Figure 29.
	High Swing [2]	350		550		
V_{ODIFF}	TSCLK Output Differential Voltage	400		850	mV	Output loading is 100 Ω line-to-line. See Figure 29.
$V_{OSINGLE}$	TSCLK Output Single Ended Voltage	200		425	mV	Output loading is 100 Ω line-to-line. See Figure 29.
SDD22	Differential Output Return Loss (For XFP Applications) [3]	12			dB	0.05 - 0.1 GHz
		12			dB	0.1 - 6.0 GHz
					dB	6.0 -15GHz - SDD22= 10-16.6 Log10(f/6.0), with f in GHz
SCC22	Common Mode Output Return Loss (For XFP Applications)	6			dB	0.01 - 15 GHz. Common mode reference impedance is 25 Ω.
R_{ODIFF}	Differential Output Impedance		100		Ω	Impedance based on s-parameter
V_{IDIFF}	Differential Input Voltage Swing			1600	mV	See Figure 29.
$V_{ISINGLE}$	Single-ended Input Voltage Swing			800	mV	See Figure 29.
R_{IDIFF}	Differential Input Impedance	80	100	120	Ω	

Table 32: High-Speed CML Input/Output Characteristics (TSD, TSCLK, SERDATI)

Parameter	Description	Min	Typ	Max	Units	Conditions
SDD11	Differential Input Return Loss (For XFP Applications)	20			dB	0.05 - 0.1 GHz
		10			dB	0.1 - 7.5 GHz
					dB	7.5 - 15 GHz - SDD11= 10-16.6 Log10(f/7.5) from with f in GHz
SCC11	Common Mode Input Return Loss (For XFP Applications)	6			dB	0.1 - 15 GHz.
SCD11	Differential to Common Mode Input Conversion (For XFP Applications)	12			dB	0.1 - 15 GHz.

1. Serial Output Voltage V_{ODIFF} and $V_{OSINGLE}$ for Low Swing level is controlled by TSD_SW[2:0] with a typical value of 1.
2. Serial Output Voltage V_{ODIFF} and $V_{OSINGLE}$ for High Swing level is controlled by TSD_SW[2:0] with a typical value of 5.
3. XFP informative SDD22 is 20 db (0.05 - 0.1 GHz), 10 db (0.1 - 7.5 GHz) and [10 - 16.6 Log_{10} (f/7.5)] db (7.5 - 15 GHz) of which the S19252 does not meet the parameters at some spot frequencies in the range of 0.05 - 0.1 GHz and 7.5 - 10 GHz.

Table 33: Phase Detector CML Output Characteristics (PD_UP/DWN)

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{ODIFF}	Serial Output Differential Voltage	900		1300	mV	With PDUPP/PDDWNN and PDUPN/PDDWNP cross-coupled. Over process, voltage and temperature range. Output loading is 600 Ω line-to-line. See Figure 29.
$V_{OSINGLE}$	Serial Output Single Ended Voltage	450		650	mV	With PDUPP/PDDWNN and PDUPN/PDDWNP cross-coupled. Over process, voltage and temperature range. Output loading is 600 Ω line-to-line. See Figure 29.

Table 34: REFCLK CML Input Characteristics (REFCLKA, REFCLKB, CSU_IN)

Parameter	Description	Min	Typ	Max	Units	Conditions
ΔV_{INDIFF}	Differential Input Voltage Swing	300		1800	mV	See Figure 29
$\Delta V_{INSINGLE}$	Single-Ended Input Voltage Swing	150		900	mV	See Figure 29.
V_{INBIAS}	Input Bias Range (AC Coupled)	V_{DD}-0.5		V_{DD}-0.2	V	See Figure 29.
R_{DIFF}	Differential Input Resistance	80	100	120	Ω	

Table 35: LVDS Input/Output Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{IH}	Input high-voltage	900		2400	mV	
V_{IL}	Input low-voltage	800		1900	mV	
V_{IC}	Input common mode voltage	850		1800	mV	
$V_{INSINGLE}$	Single-ended input voltage swing	100 [1]		650	mV	See Figure 29.
V_{INDIFF}	Differential input voltage swing	200		1300	mV	See Figure 29.
R_{IN}	Receiver differential input impedance	80		120	Ω	
V_{OH}	Output high-voltage	1160		1550	mV	100 Ω line-to-line
V_{OL}	Output low-voltage	925		1200	mV	100 Ω line-to-line
$V_{OUTSINGLE}$	Single-ended output voltage swing	250		450	mV	100 Ω line-to-line [2] See Figure 29.
$V_{OUTDIFF}$	Differential output voltage swing	500		900	mV	100 Ω line-to-line See Figure 29.
R_{OUT}	Output impedance	40		140	Ω	

1. 100 mV single-ended input swing is functional up to $V_{IC} \leq 1800$ mV (SFI-4 Phase 1 implies $V_{IC} \leq 2350$ mV). 500 mV single-ended input swing is the minimum input swing required when operating up to $V_{IH} \leq 2400$ mV.
2. LVDS to ground termination: A DC Block must be used when 50 ohms to ground termination is used for any LVDS output.

Table 36: Transmitter Timing Characteristics

Parameter	Description	Min	Typ	Max	Units
Duty Cycle	622 PICLK duty cycle = tD_{PICLK}/T_0	40		60	%
Duty Cycle	PCLKP/N duty cycle	45		55	%
Duty Cycle	TX_155 MCK duty cycle	45		55	%
t_{SUTSD}	TSD set-up time with respect to rising edge of TSCLK. See Figure 22.	25			ps
t_{HTSD}	TSD hold time with respect to rising edge of TSCLK. See Figure 22.	25			ps
t_{SUPIN}[1]	PINP/N[15:0] set-up time with respect to rising edge of PICLKP. See Figure 23.	250			ps
t_{HPIN}[1]	PINP/N[15:0] hold time with respect to rising edge of PICLKP. See Figure 23.	250			ps
t_r/t_f	CML output rise and fall time (20% – 80%) - TSD (Low Swing)	24			ps
	CML output rise and fall time (20% – 80%) - TSD (High Swing)			35	ps
	LVDS input rise and fall time (20% – 80%)	100		300	ps
	LVDS output rise and fall time (20% – 80%)	100		250	ps
	LVCMOS output rise and fall Time (20% – 80%) (10 pF load condition)	1		15	ns
FIFO drift	PCLK to PICLK drift after the FIFO is centered			2	PCLK cycles

1. 200 mV p-p single-ended input swing

Figure 22: Transmitter TSCLK to TSD Timing Characteristics

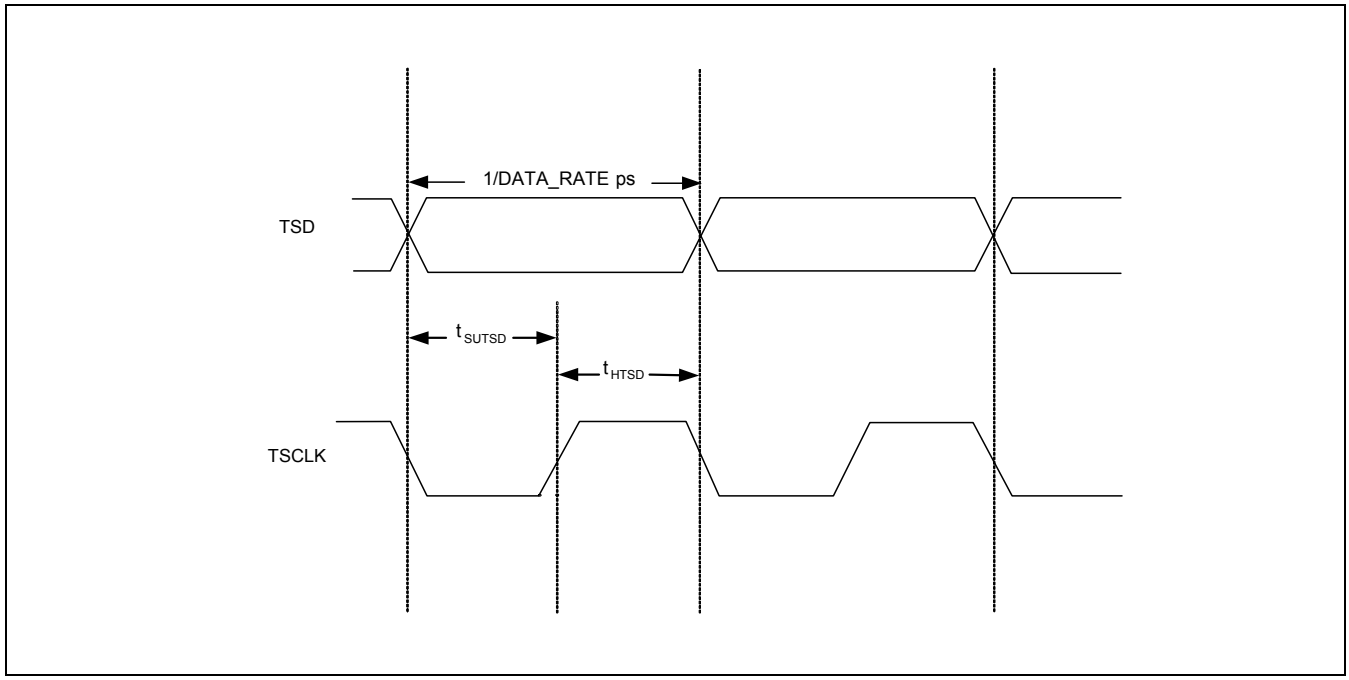


Figure 23: Transmitter Timing Characteristics

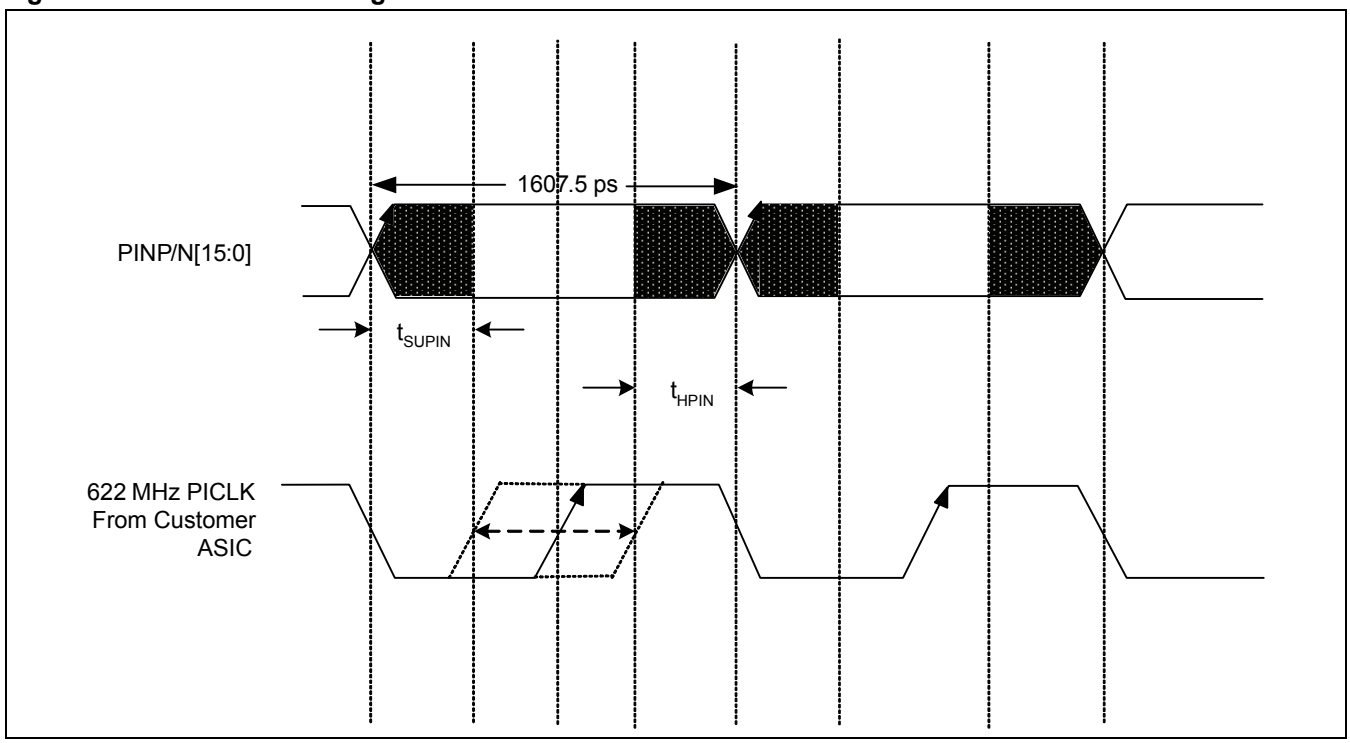
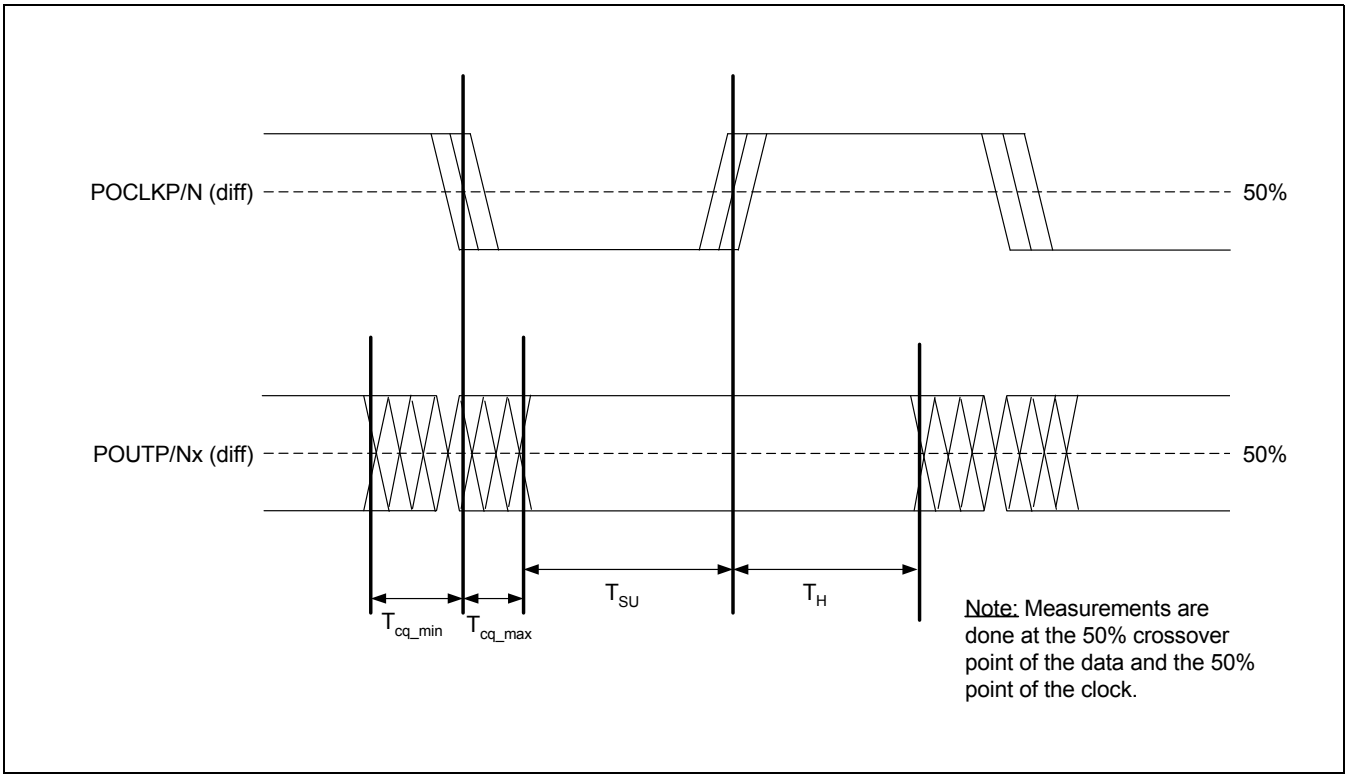


Table 37: Receiver Timing Characteristics

Parameter	Description	Min	Typ	Max	Units
Duty Cycle	POCLK duty cycle	45		55	%
	POCLK Jitter Generation (Normal Mode with CRU locked to SERDATI, PRBS 2^{31}-1)			40	ps_{p-p}
RX_MCKP/N Duty Cycle	RX_MCKP/N duty cycle	45		55	%
T_{cq_min} T_{cq_max}	POUTP/N delay from POCLKP/N falling edge. See Figure 24.			±185	ps
T_{SU}	POUTP/N set up time with respect to rising edge of POCLKP/N rising. See Figure 24.	525			ps
T_H	POUTP/N hold time with respect to rising edge of POCLKP/N rising. See Figure 24.	525			ps
t_r/t_f	LVDS output rise and fall time (20% - 80%).	100		250	ps
	LVCMOS output rise and fall time (20% - 80%) (10pF load condition)	1		15	ns

Figure 24: Receiver Timing Characteristics



1. When a setup time is specified on LVDS signals between an input and a clock, the setup time is the time in picoseconds from the 50% point of the input to the 50% point of the clock.
2. When a hold time is specified on LVDS signals between an input and a clock, the hold time is the time in picoseconds from the 50% point of the clock to the 50% point of the input.

Table 38: MDIO Timing Characteristics

Parameter	Description	Min	Typ	Max	Units
t_{SU}	Input set-up time from MDIO to MDC	10			ns
t_{H}	Input hold time from MDIO to MDC	10			ns
t_{Delay}	MDC to MDIO Clock to data delay	0		80	ns
	MDC frequency			10	MHz
	Input Capacitance			6	pF
	Bus Loading Capacitance			60	pF

Figure 25: I2C BUS® Timing Diagram

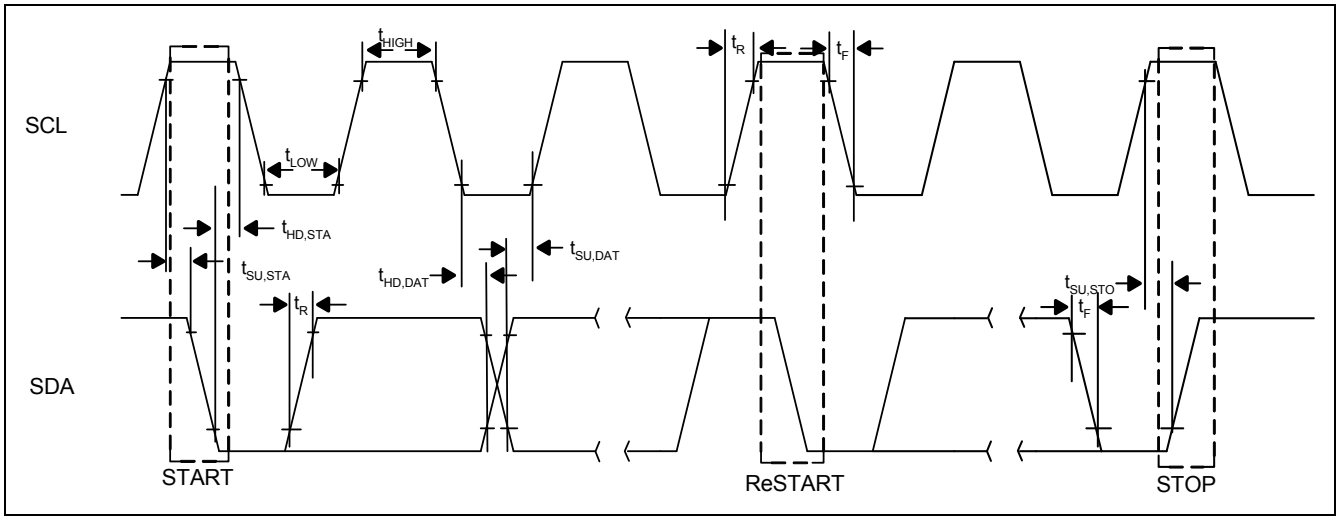


Table 39: I2C BUS® LVCMOS Input/Output & Timing Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
I2C Timing Characteristics						
t_{LOW}	Clock pulse width low	1.3			µs	Serial Clock Operating Frequency: 400kHz Max
t_{HIGH}	Clock pulse width high	0.6			µs	
$t_{HD,STA}$	START Hold Time	0.6			µs	
$t_{SU,STA}$	START Set-up Time	0.6			µs	
$t_{HD,DAT}$	Data In Hold Time	0			µs	
$t_{SU,DAT}$	Data In Set-up TIme	0.3			µs	
$t_{SU,STO}$	STOP Set-up TIme	0.6			µs	
t_R	Input Rise Time (400 kHz)			300	ns	From ($V_{IL,MAX}$-0.15) to ($V_{IH,MIN}$+0.15)
t_F	Input Fall Time (400 kHz)			300	ns	From ($V_{IH,MIN}$+0.15) to ($V_{IL,MAX}$-0.15)

Figure 26: SPI BUS Timing Diagram

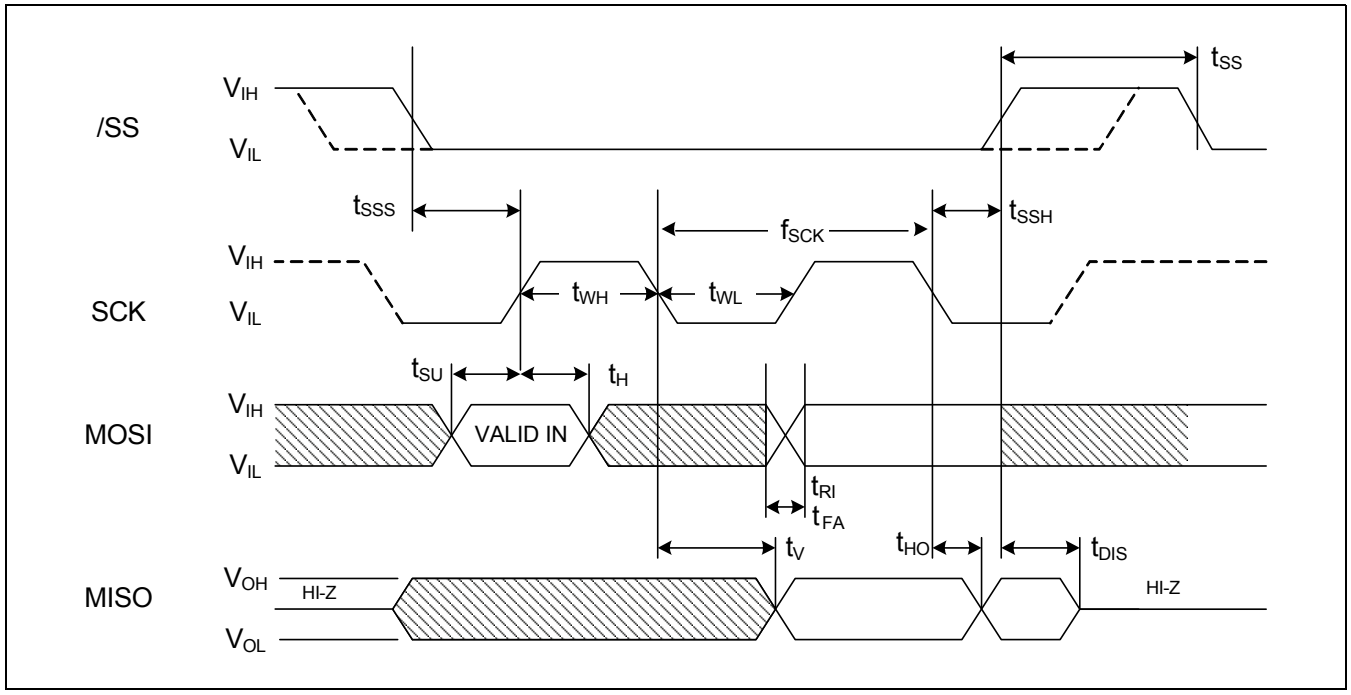


Table 40: SPI BUS Timing Characteristics [1]

Symbol	Parameter	Min.	Max.	Units	Test Conditions
f_{SCK}	Clock Frequency		10	MHz	C_L = 10 pF Input and output DC voltage levels: See 3.3 V LVCMOS spec f_{SCK} = 10 MHz Max
t_{WH}	SCK High Time	40		ns	
t_{WL}	SCK Low Time	40		ns	
t_{SU}	Data Setup Time	20		ns	
t_H	Data Hold Time	20		ns	
t_V	Output Valid from Clock Low		40	ns	
t_{HO}	Output Hold Time	0		ns	
t_{DIS}	Output Disable Time		75	ns	
t_{SSS}	/SS Setup Time	100		ns	
t_{SSH}	/SS Hold TIme	100		ns	
t_{SS}	/SS Width	100		ns	
t_{RI} & t_{FA}	Input rise and fall times		10	ns	

1. Timing guaranteed by design.

External Loop Filter Components

Table 41: Transmit and Receive External Loop Filter Components, See Figure 27

REFCLK	Reference Designator	Description	Value	Unit
155.52 MHz CSU_REFCLK 155.52 MHz CRU_REFCLK XVCO = 0	R_1, R_2,	Resistor, Surface Mount, 0402	100	Ω
	C_1	Capacitor, Surface Mount	10	µF
	R_3, R_4	Resistor, Surface Mount, 0402	180	Ω
	C_2	Capacitor, Surface Mount	10	µF
622.08 MHz CSU_REFCLK 622.08 MHz CRU_REFCLK XVCO = 0	R_1, R_2,	Resistor, Surface Mount, 0402	51	Ω
	C_1	Capacitor, Surface Mount	10	µF
	R_3, R_4	Resistor, Surface Mount, 0402	180	Ω
	C_2	Capacitor, Surface Mount	10	µF
155.52/622.08 MHz CSU_REFCLK 155.52 MHz CRU_REFCLK XVCO = 1 (622.08 MHz XVCO)	R_1, R_2,	Resistor, Surface Mount, 0402	51	Ω
	C_1	Capacitor, Surface Mount	10	µF
	R_3, R_4	Resistor, Surface Mount, 0402	180	Ω
	C_2	Capacitor, Surface Mount	10	µF
155.52/622.08 MHz CSU_REFCLK 155.52 MHz CRU_REFCLK XVCO = 1 (155.52 MHz XVCO)	R_1, R_2,	Resistor, Surface Mount, 0402	100	Ω
	C_1	Capacitor, Surface Mount	10	µF
	R_3, R_4	Resistor, Surface Mount, 0402	180	Ω
	C_2	Capacitor, Surface Mount	10	µF

The transmit and receive external loop filter component values are valid for all rates listed in Table 3 for transmitter and Table 7 for receiver. Note - CSU and CRU resistor values stated in table are based on S19252PBID material. The resistor values may require adjustment for some applications.

Figure 27: External Loop Filter Components

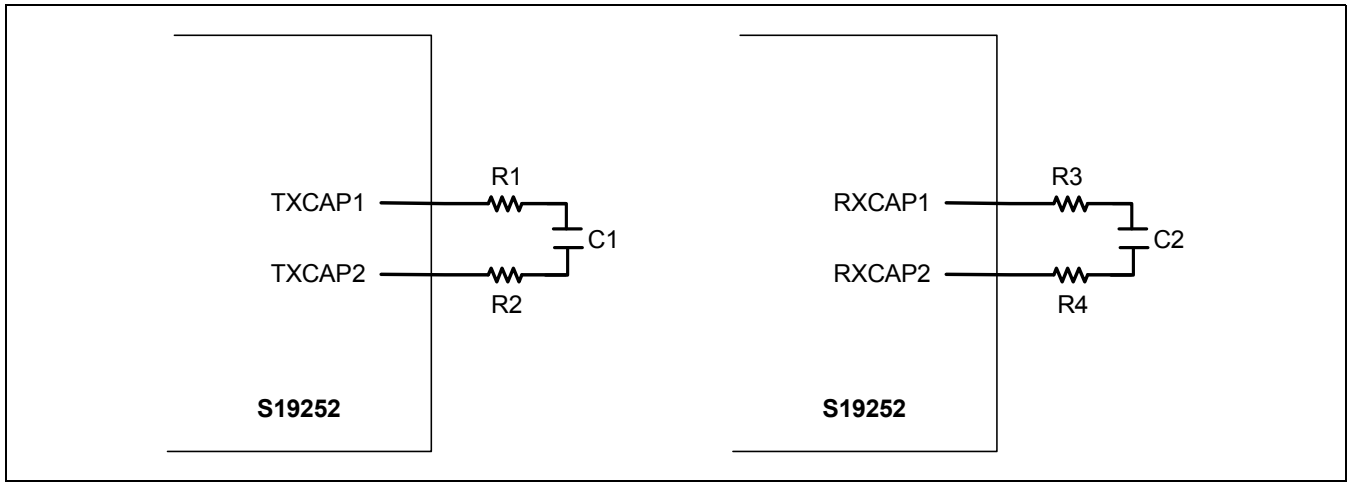


Figure 28: FIFO Initialization

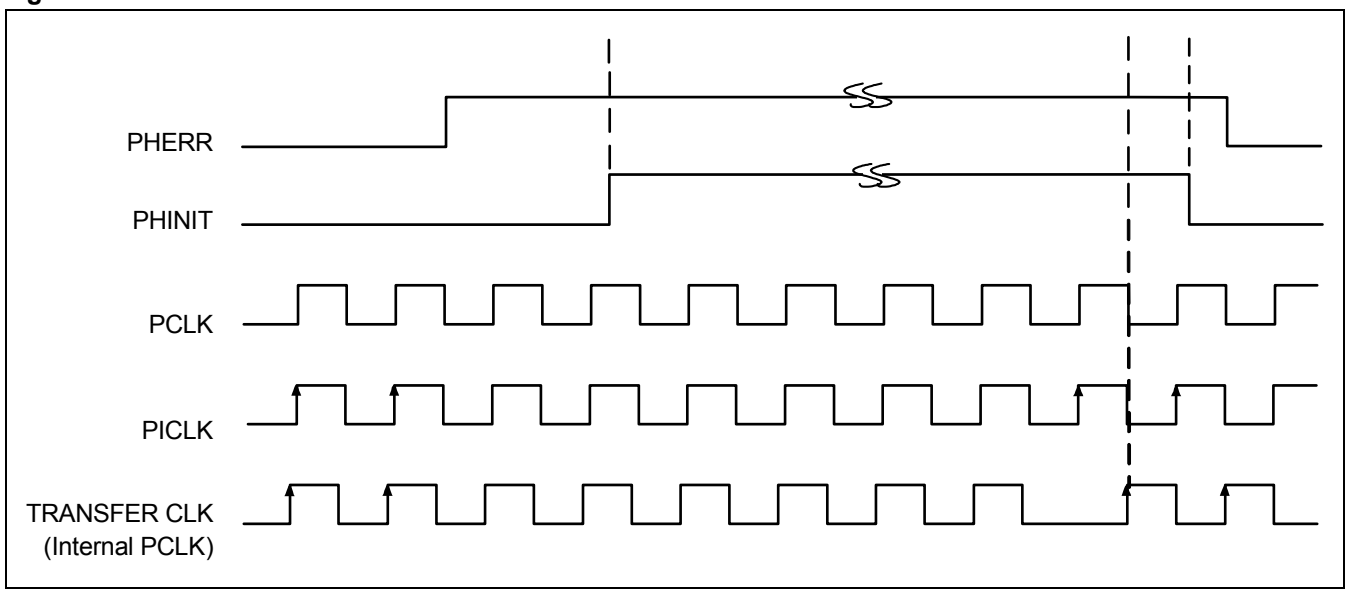
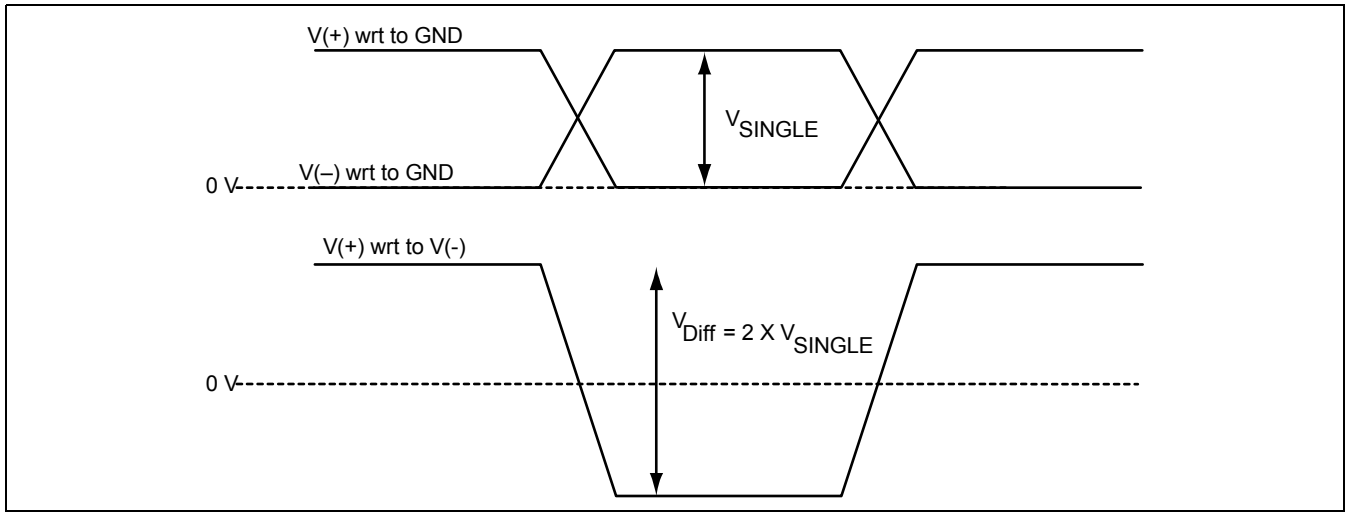


Figure 29: Differential Voltage Measurement



Note: WRT = With Respect To

Recommended Terminations

Figure 30: S19252 Differential CML Output to +5 V/+3.3 V PECL Input AC Coupled Termination

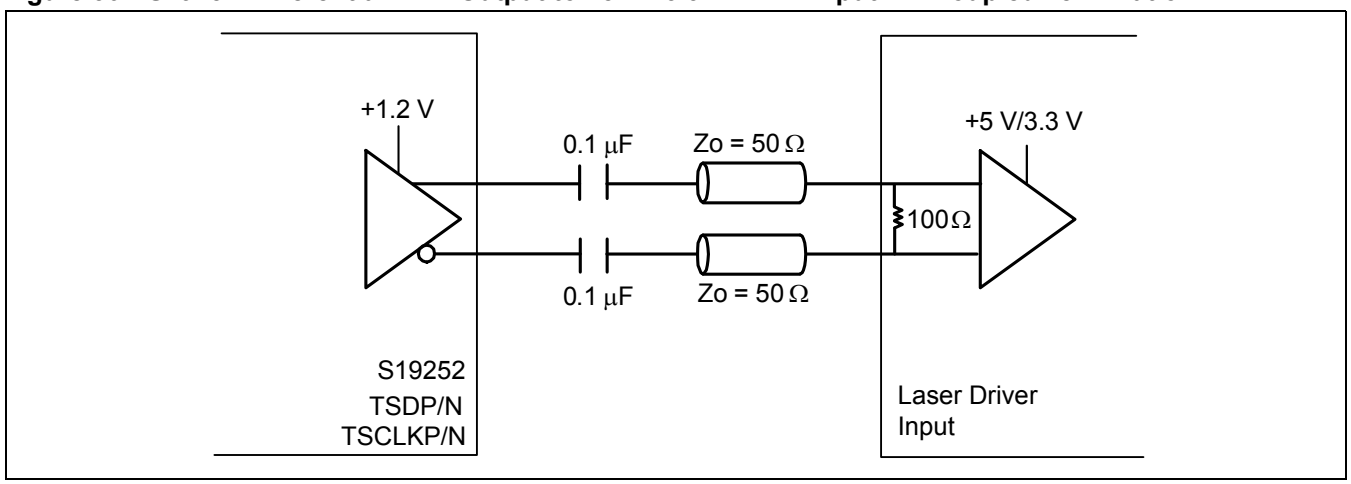


Figure 31: S19252 LVDS Driver to LVDS Input Termination

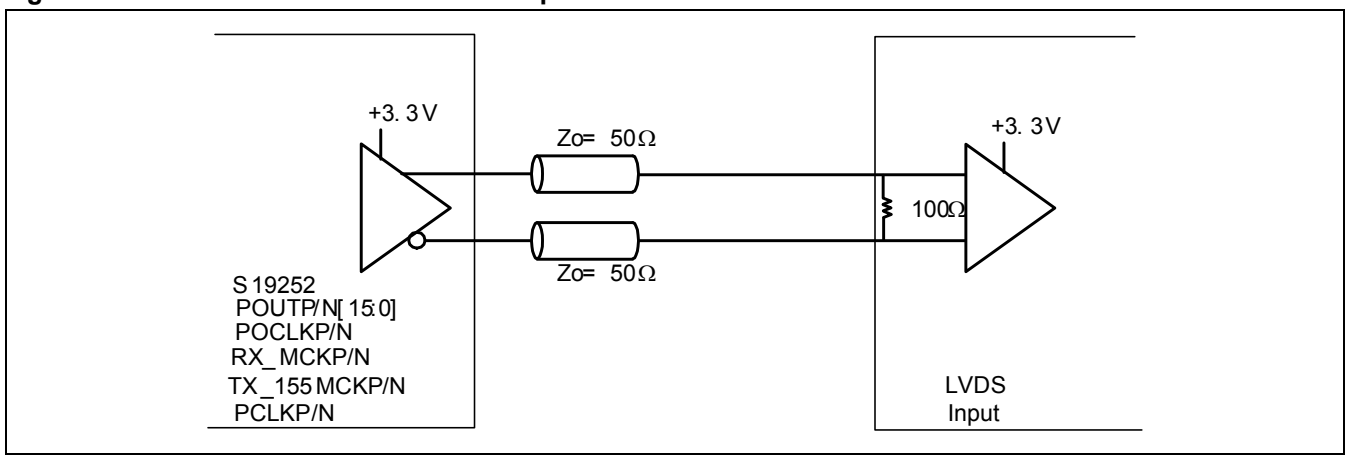


Figure 32: +5 V Differential PECL Driver to S19252 Differential CML Input AC Coupled Termination

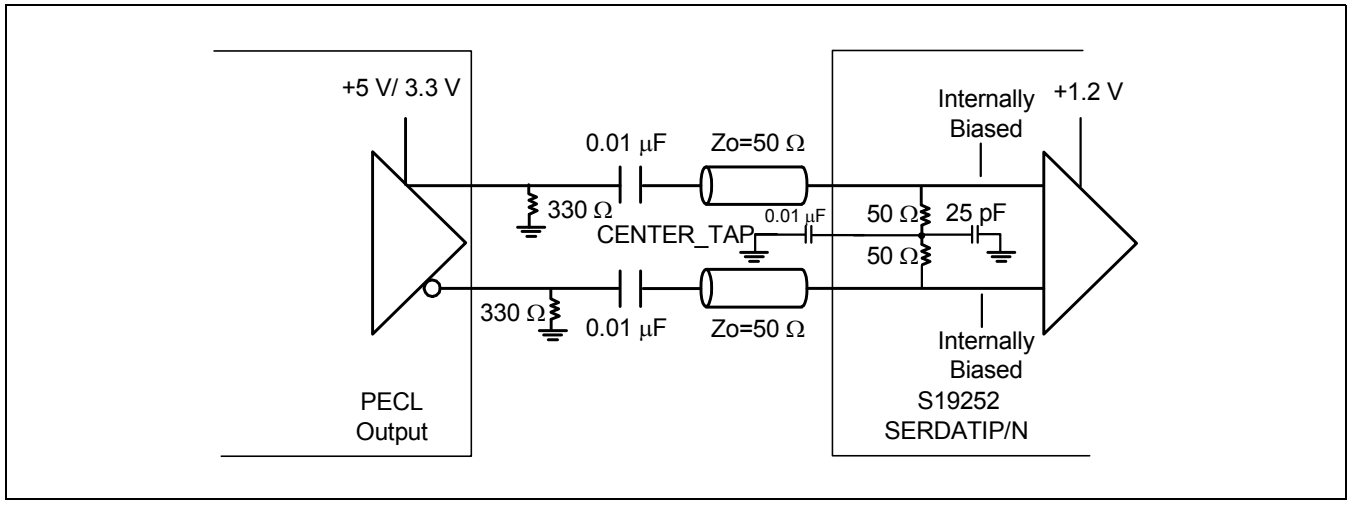


Figure 33: +5 V/+3.3 V Differential PECL Driver to S19252 CML Reference Clock Input AC Coupled Termination

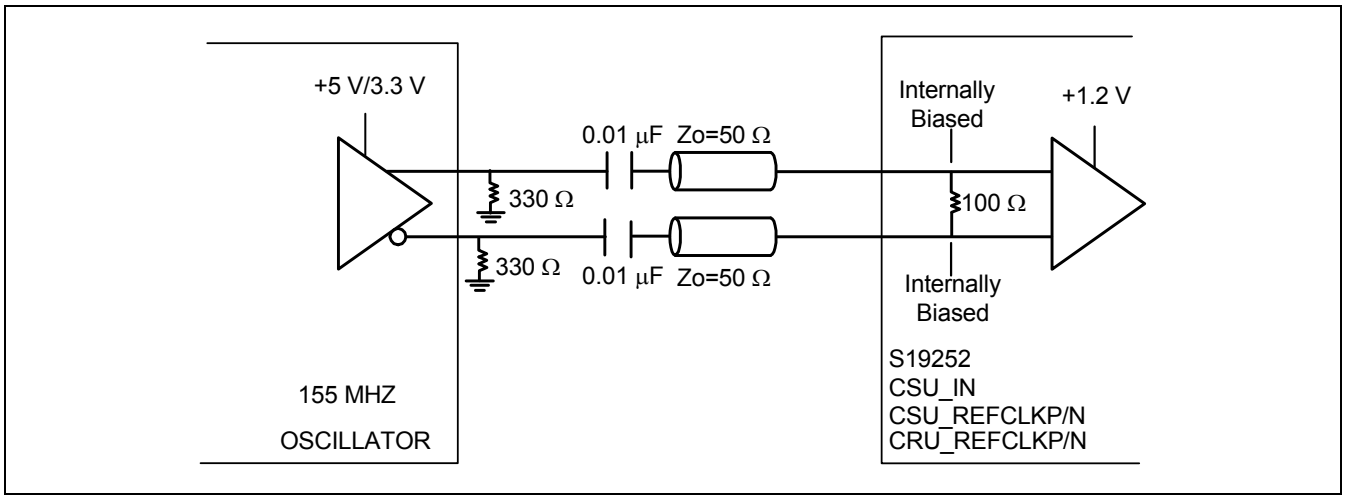
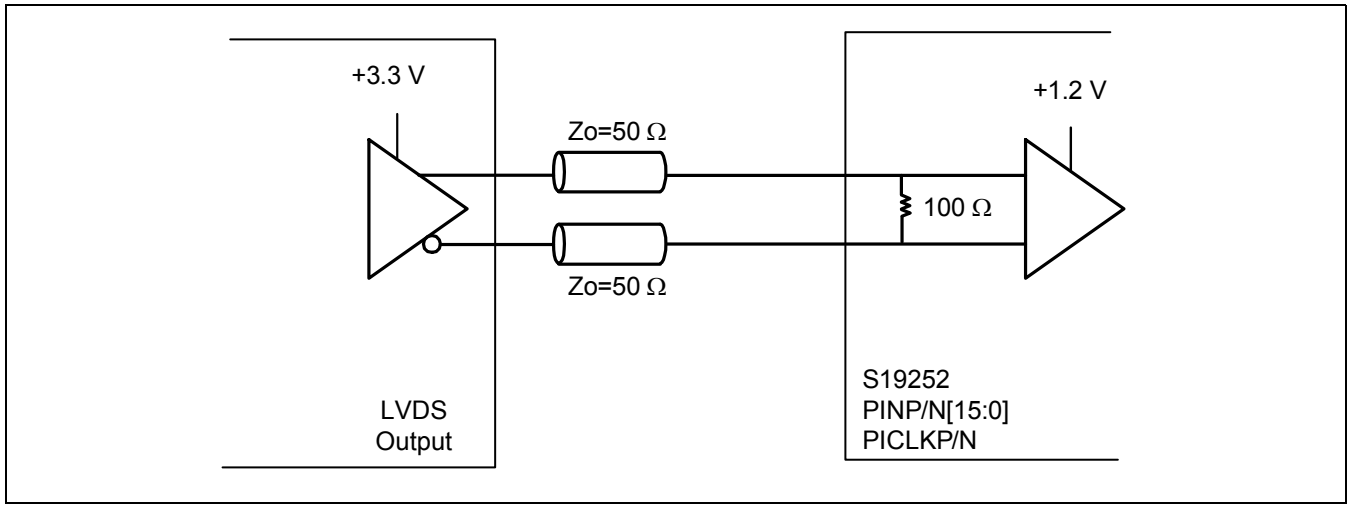


Figure 34: LVDS Driver to S19252 LVDS Inputs

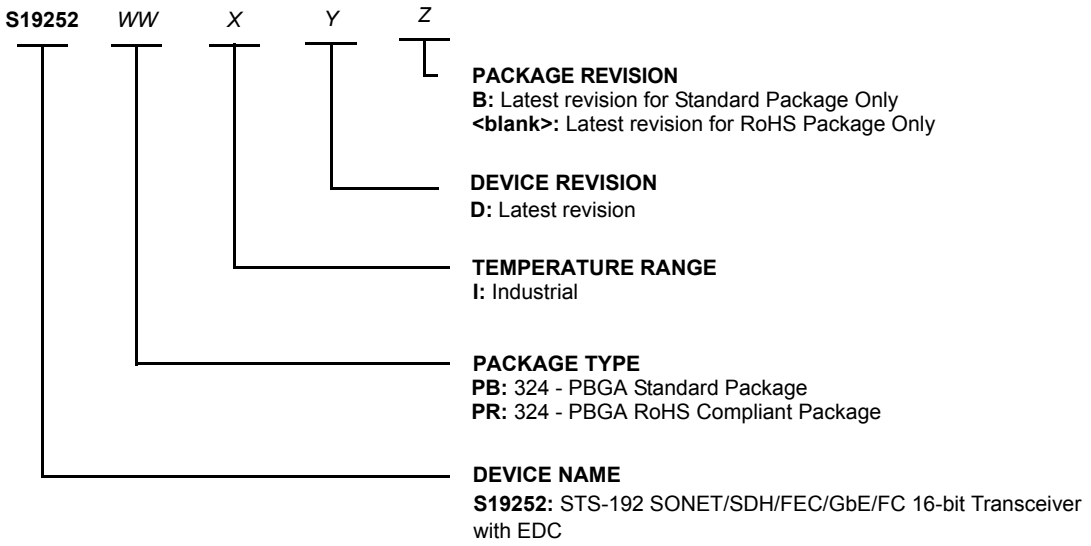


Document Revision History

Revision	Date	Description
5.03	6/15/10	CHANGE PERTAINING TO PCN1304, “LOCKDET VALID WINDOW” • Page 59, Add conditions for PLL lockdet CHANGES UNRELATED TO PCN • Page 1, Clarification with General, Transmitter and Receiver Features • Page 8, Add footnote for SFP+ • Page 58, Figure14 updated • Table 28, Add footnote for SFP+ • Removed the word Green from RoHS statements throughout DS
5.02	4/06/09	• Page 2, DS phase name replaced with Released and associated bullets updated for clarity. • Page 3, Add footnote 2 to Tx rate selection Table 3 • Page 8, Change rev/date of GR-253-CORE SONET Jitter Specifications under Standards Compliance List • Page 11, Add TX_RSTB paragraph • Page 12, Add footnote 2 to Rx rate selection Table 7 • Page 15, Add RX_RSTB paragraph • Page 34, Update I2C refclk requirement statement • Page 38, Changed SONET Jitter Gen requirement statement in accordance to GR-253-CORE • Page 48 and 50, Add logic level description for TXPD and RXPD • Page 59, Updated Figure 14 Package Marking • Page 72, Updated TSCLK swing levels in Table 32 • Page 73, Add note 1 and 2 for TSD output swing level control reference • Last page, Updated Ordering Information
5.01	6/4/08	• Page 9, Updated Figure 5 for PICLK, CSU_REFCLK, TSD_SW and TSD_SLEW. • Page 10, Updated PINP/N[15:0], PICLKP/N and added LVDS_INPUT_AC_EN paragraph. • Page 11, Update XVCO155 paragraph, changed MDIO to serial. • Page 13, Updated CSU_IN paragraph figure numbering call out. • Page 14, Update LVDS termination info. • Page 20, Update LVDS termination info and POCLK polarity clarification for SPI4-1. • Page 21, Corrected typo in RLPTIME paragraph. • Page 25, Updated Loop Timing paragraphs and remove SLPTIME reference. • Page 26, Update FIFO Init paragraph Figure number call out. • Page 32, Updated MDIO paragraphs with clock edge info and address paging info. • Page 48, Updated Table 22 to include LVDS_INPUT_AC_EN description and minor update of TXPD info. • Page 50, Updated RXPD info Table 22. • Page 60, Changed Table 28 to include 11.003G rate, add comment on ppm offset and round off frequencies. • Page 60, Table 28, Changed CRU Lock time units from ms to us. • Page 61, Updated Table 28 to add JG REFCLK phase noise info. and Corrected one Tap2 setting for 10.7g 50k-80M. • Page 62, Updated Table 28 to correct figure reference. • Page 69, Replace phase noise Figure 20 and 21 plots with current test data. • Page 71, Updated Table 30 typo; Power line 4 and 5 text swap. • Page 74, Updated Table 35 to include note 2. • Page 90, Update Ordering info by removing note 1 from PRID device.
5.00	12/14/07	• Production Release

Ordering Information

Device Code	Product
S19252PBIDB	**S19252 - STS-192 SONET/SDH/FEC/GbE/FC 16-bit Transceiver with EDC** Industrial Temp, Standard Package
S19252PRID	**S19252 - STS-192 SONET/SDH/FEC/GbE/FC 16-bit Transceiver with EDC** Industrial Temp, RoHS Compliant Package



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