FEATURES
- Software-Selectable Cable Termination for:
  - RS232 (V.28)
  - RS423 (V.10)
  - RS422 (V.11)
  - RS485
  - EIA530
  - EIA530-A
  - V.35
  - V.36
  - X.21
- Outputs Won’t Load the Line with Power Off

APPLICATIONS
- Data Networking
- CSU and DSU
- Data Routers

DESCRIPTION
The LTC1344A features six software-selectable multiprotocol cable terminators. Each terminator can be configured as an RS422 (V.11) 100Ω minimum differential load, V.35 T-network load or an open circuit for use with RS232 (V.28) or RS423 (V.10) transceivers that provide their own termination. When combined with the LTC1543 and LTC1544, the LTC1344A forms a complete software-selectable multiprotocol serial port. A data bus latch feature allows sharing of the select lines between multiple interface ports.

The LTC1344A is similar to the LTC1344 except for a difference in the Mode Selection table.

The LTC1344A is available in a 24-lead SSOP.

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**ABSOLUTE MAXIMUM RATINGS**

(Note 1)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICC</td>
<td>Supply Current</td>
<td>All Digital Pins = GND or VCC</td>
<td>0.4</td>
<td>1.0</td>
<td>mA</td>
<td></td>
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</table>

**Terminator Pins**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>RV.35</td>
<td>Differential Mode Impedance</td>
<td>All Loads (Figure 1), −2V ≤ VCM ≤ 2V (Commercial)</td>
<td>90</td>
<td>104</td>
<td>110</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>Common Mode Impedance</td>
<td>All Loads (Figure 2), −2V ≤ VCM ≤ 2V (Commercial)</td>
<td>135</td>
<td>153</td>
<td>165</td>
<td>Ω</td>
</tr>
<tr>
<td>RV.11</td>
<td>Differential Mode Impedance</td>
<td>All Loads (Figure 1), VCM = 0V (Commercial)</td>
<td>100</td>
<td>104</td>
<td>110</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>Common Mode Impedance</td>
<td>All Loads (Figure 1), −7V ≤ VCM ≤ 7V (Commercial)</td>
<td>100</td>
<td>104</td>
<td>100</td>
<td>Ω</td>
</tr>
</tbody>
</table>

**ILEAK** | High Impedance Leakage Current | All Loads, −7V ≤ VCM ≤ 7V | ±1  | ±50 | μA   |

**Logic Inputs**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
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<tr>
<td>VIH</td>
<td>Input High Voltage</td>
<td>All Logic Input Pins</td>
<td>2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VIL</td>
<td>Input Low Voltage</td>
<td>All Logic Input Pins</td>
<td>0.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>IIN</td>
<td>Input Current</td>
<td>All Logic Input Pins</td>
<td>±10</td>
<td></td>
<td></td>
<td>μA</td>
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</table>

The ● denotes specifications which apply over the full operating temperature range.

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** All currents into device pins are positive; all currents out of device pins are negative. All voltages are reference to ground unless otherwise specified.

**Note 3:** All typicals are given at VCC = 5V, VEE = −5V, TA = 25°C.
TYPICAL PERFORMANCE CHARACTERISTICS

V.11 or V.35 Differential Mode Impedance vs Temperature

V.11 or V.35 Differential Mode Impedance vs Common Mode Voltage

V.11 or V.35 Differential Mode Impedance vs Supply Voltage (VCC)

V.11 or V.35 Differential Mode Impedance vs Negative Supply Voltage (VEE)

V.35 Common Mode Impedance vs Temperature

V.35 Common Mode Impedance vs Common Mode Voltage

V.35 Common Mode Impedance vs Supply Voltage (VCC)

V.35 Common Mode Impedance vs Negative Supply Voltage (VEE)

Supply Current vs Temperature
**PIN FUNCTIONS**

**M0 (Pin 1):** TTL Level Mode Select Input. The data on M0 is latched when **LATCH** is high.

**V_{EE} (Pin 2):** Negative Supply Voltage Input. Can connect directly to the LTC1543 V_{EE} pin. Connect a 1\mu F capacitor to ground.

**R1C (Pin 3):** Load 1 Center Tap.

**R1B (Pin 4):** Load 1 Node B.

**R1A (Pin 5):** Load 1 Node A.

**R2A (Pin 6):** Load 2 Node A.

**R2B (Pin 7):** Load 2 Node B.

**R2C (Pin 8):** Load 2 Center Tap.

**R3A (Pin 9):** Load 3 Node A.

**R2B (Pin 10):** Load 2 Node B.

**R3C (Pin 11):** Load 3 Center Tap.

**GND (Pin 12):** Ground Connection for Load 1 to Load 3.

**GND (Pin 13):** Ground Connection for Load 4 to Load 6.

**V_{CC} (Pin 14):** Positive Supply Input. 4.75V \leq V_{CC} \leq 5.25V.

**LATCH (Pin 21):** TTL Level Logic Signal Latch Input. When **LATCH** is low the input buffers on M0, M1, M2 and DCE/DTE are transparent. When **LATCH** is high the logic pins are latched into their respective input buffers. The data latch allows the select lines to be shared between multiple I/O ports.

**DCE/DTE (Pin 22):** TTL Level Mode Select Input. DCE mode is selected when high and DTE mode when low. The data on DCE/DTE is latched when **LATCH** is high.

**M2 (Pin 23):** TTL Level Mode Select Input 1. The data on M2 is latched when **LATCH** is high.

**M1 (Pin 24):** TTL Level Mode Select Input 2. The data on M1 is latched when **LATCH** is high.

**TEST CIRCUITS**

![Figure 1. Differential V.11 or V.35 Impedance Measurement](image1)

![Figure 2. V.35 Common Mode Impedance Measurement](image2)
**MODE SELECTION**

<table>
<thead>
<tr>
<th>LTC1344A MODE NAME</th>
<th>DCE/DTE</th>
<th>M2</th>
<th>M1</th>
<th>M0</th>
<th>R1</th>
<th>R2</th>
<th>R3</th>
<th>R4</th>
<th>R5</th>
<th>R6</th>
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<tr>
<td>V.10/RS423</td>
<td>X</td>
<td>0</td>
<td>0</td>
<td>0</td>
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<td>Z</td>
<td>Z</td>
<td>Z</td>
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<tr>
<td>RS530A</td>
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<td>V.11</td>
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<td>Z</td>
<td>V.11</td>
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<td>Z</td>
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<td>No Cable</td>
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<td>1</td>
<td>1</td>
<td>V.11</td>
<td>V.11</td>
<td>V.11</td>
<td>V.11</td>
<td>V.11</td>
<td>V.11</td>
</tr>
</tbody>
</table>

X = don’t care, 0 = logic low, 1 = logic high

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**Figure 3. LTC1344A Modes**

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Multiprotocol Cable Termination

One of the most difficult problems facing the designer of a multiprotocol serial interface is how to allow the transmitters and receivers for different electrical standards to share connector pins. In some cases the transmitters and receivers for each interface standard can be simply tied together and the appropriate circuitry enabled. But the biggest problem still remains: how to switch the various cable termination required by the different standards.

Traditional implementations have included switching resistors with expensive relays or requiring the user to change termination modules every time the interface standard has changed. Custom cables have been used with the termination in the cable head. Another method uses separate termination built on the board, and a custom cable which routes the signals to the appropriate termination. Switching the termination using FETs is difficult because the FETs must remain off even though the signal voltage is beyond the supply voltage for the FET drivers or the power is off.

The LTC1344A solves the cable termination switching problem via software control. The LTC1344A provides termination for the V.10 (RS423), V.11 (RS422), V.28 (RS232) and V.35 electrical protocols.

V.10 (RS423) Termination

A typical V.10 unbalanced interface is shown in Figure 4. A V.10 single-ended generator output A with ground C is connected to a differential receiver with input A' connected to A and input C' connected to the signal return ground C. Usually no cable termination is required for V.10 interfaces but the receiver inputs must be compliant with the impedance curve shown in Figure 5.

In V.10 mode, both switches S1 and S2 are turned off so the only cable termination is the input impedance of the V.10 receiver.

V.11 (RS422) Termination

A typical V.11 balanced interface is shown in Figure 6. A V.11 differential generator with outputs A and B with ground C is connected to a differential receiver with ground C'. Usually no cable termination is required for V.11 interfaces but the receiver inputs must be compliant with the impedance curve shown in Figure 7.

In V.11 mode, both switches S1 and S2 are turned off so the cable is terminated with a 103Ω impedance.
V.28 (RS232) Termination

A typical V.28 unbalanced interface is shown in Figure 8. A V.28 single-ended generator output A with ground C is connected to a single-ended receiver with input A' connected to A, ground C' connected via the signal return ground to C. The V.28 standard requires a 5k terminating resistor to ground which is included in almost all compliant receivers as shown in Figure 9. Because the termination is included in the receiver, both switches S1 and S2 in the LTC1344A are turned off.

V.35 Termination

A typical V.35 balanced interface is shown in Figure 10. A V.35 differential generator with outputs A and B with ground C is connected to a differential receiver with ground C', inputs A' connected to A, B' connected to B. The V.35 interface requires a T-network termination at the receiver end and the generator end. In V.35 mode both switches S1 and S2 in the LTC1344A are turned on as shown in Figure 11.

The differential impedance measured at the connector must be $100\Omega \pm 10\Omega$ and the impedance between shorted terminals A' and B' to ground C' must be $150\Omega \pm 15\Omega$. The input impedance of the V.35 receiver is connected in parallel with the T-network inside the LTC1344A, which could cause the overall impedance to fail the specification.
The generator differential impedance must be 50Ω to 150Ω and the impedance between shorted terminals A and B to ground C must be 150Ω ±15Ω. For the generator termination, switches S1 and S2 are both on and the top side of the center resistor is brought out to a pin so it can be bypassed with an external capacitor to reduce common mode noise as shown in Figure 12.

Any mismatch in the driver rise and fall times or skew in the driver propagation delays will force current through the center termination resistor to ground causing a high frequency common mode spike on the A and B terminals. The common mode spike can cause EMI problems that are reduced by capacitor C1 which shunts much of the common mode energy to ground rather than down the cable.

The LATCH Pin

The LATCH pin (21) allows the select lines (M0, M1, M2 and DCE/DTE) to be shared with multiple LTC1344As, each with its own LATCH signal. When the LATCH pin is held low the select line input buffers are transparent. When the LATCH pin is pulled high, the select line input buffers latch the state of the Select pins so that changes on the select lines are ignored until LATCH is pulled low again. If the latch feature is not used, the LATCH pin should be tied to ground.
PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

G Package
24-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE
**TYPICAL APPLICATION**

Figure 13 shows a typical application for the LTC1344A using the LTC1543 mixed mode transceiver chip to generate the clock and data signals for a serial interface. The LTC1344A VEE supply is generated from the LTC1543 charge pump and the select lines M0, M1, M2 and DCE/DTE are shared by both chips. Each driver output and receiver input is connected to one of the LTC1344A termination ports. Each electrical protocol can then be chosen using the digital select lines.

**Figure 13.** Typical Application Using the LTC1344A

**RELATED PARTS**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>LTC1334</td>
<td>Single Supply RS232/RS485 Transceiver</td>
<td>2 RS485 Dr/Rx or 4 RS232 Dr/Rx Pairs</td>
</tr>
<tr>
<td>LTC1343</td>
<td>Multiprotocol Serial Transceiver</td>
<td>Software Selectable Multiprotocol Interface</td>
</tr>
<tr>
<td>LTC1345</td>
<td>Single Supply V.35 Transceiver</td>
<td>3 Dr/3 Rx for Data and CLK Signals</td>
</tr>
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<td>LTC1346A</td>
<td>Dual Supply V.35 Transceiver</td>
<td>3 Dr/3 Rx for Data and CLK Signals</td>
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<td>Multiprotocol Serial Transceiver</td>
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<tr>
<td>LTC1544</td>
<td>Multiprotocol Serial Transceiver</td>
<td>Software Selectable Transceiver for Control Signals</td>
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