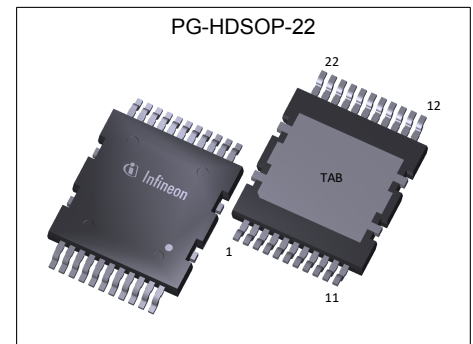


MOSFET

600V CoolMOS™ SJ S7 Power Device

IPQC60R040S7 enables the best price performance for low frequency switching applications. CoolMOS™ S7 boasts the lowest $R_{DS(on)}$ values for a HV SJ MOSFET, with distinctive increase of energy efficiency.

CoolMOS™ S7 is optimized for “static switching” and high current applications. It is an ideal fit for solid state relay and circuit breaker designs as well as for line rectification in SMPS and inverter topologies.



Features

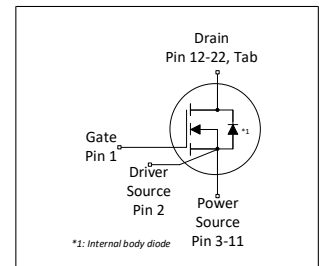
- CoolMOS™ S7 technology enables 40mΩ $R_{DS(on)}$ in the smallest footprint
- Optimized price performance in low frequency switching applications
- High pulse current capability
- Kelvin Source pin improves switching performance at high current
- QDPAK bottom side cooling package is MSL1 compliant, total Pb-free and suitable for standard PCB assembling flow, enabling simple system integration

Benefits

- Minimized conduction losses (eliminate / reduce heat sink)
- Increased system performance
- More compact and easier design
- Lower BOM or/and TCO over prolonged life time

Compared to electromechanical devices:

- Faster switching times
- Higher reliability and longer system life time
- Shock & vibration resistance
- No contact arcing, bouncing or degradation over life time



RoHS

Potential applications

- Solid state relays and circuit breakers
- Line rectification in high power/performance applications e.g. Computing, Telecom, UPS and Solar

Product validation

Fully qualified according to JEDEC for Industrial Applications

Please note: The source and sense source pins are not exchangeable. Their exchange might lead to malfunction. For paralleling 4pin MOSFET devices the placement of the gate resistor is generally recommended to be on the Driver Source instead of the Gate.

Table 1 Key Performance Parameters

| Parameter | Value | Unit |
|-------------------------|-------|------|
| $R_{DS(on),max}$ | 40 | mΩ |
| $Q_{g,typ}$ | 83 | nC |
| V_{SD} | 0.82 | V |
| Pulsed I_{SD}, I_{DS} | 207 | A |

| Type / Ordering Code | Package | Marking | Related Links |
|----------------------|-------------|----------|----------------|
| IPQC60R040S7 | PG-HDSOP-22 | 60R040S7 | see Appendix A |

Table of Contents

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1 Maximum ratings
 at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---------------------------------------|----------------------|--------|------|------|------------------|--|
| | | Min. | Typ. | Max. | | |
| Drain current rating | I_D | - | - | 14 | A | $T_C=140^\circ\text{C}$ Current is limited by $T_{j\max} = 150^\circ\text{C}$; Lower case temp does increase current capability |
| Pulsed drain current ¹⁾ | $I_{D,\text{pulse}}$ | - | - | 207 | A | $T_C=25^\circ\text{C}$ |
| Avalanche energy, single pulse | E_{AS} | - | - | 159 | mJ | $I_D=2.8\text{A}$; $V_{DD}=50\text{V}$; see table 10 |
| Avalanche current, single pulse | I_{AS} | - | - | 2.8 | A | - |
| MOSFET dv/dt ruggedness ²⁾ | dv/dt | - | - | 20 | V/ns | $V_{DS}= 0\text{V to } 300\text{V}$ |
| Gate source voltage (static) | V_{GS} | -20 | - | 20 | V | static |
| Gate source voltage (dynamic) | V_{GS} | -30 | - | 30 | V | AC ($f>1\text{ Hz}$) |
| Power dissipation | P_{tot} | - | - | 272 | W | $T_C=25^\circ\text{C}$ |
| Storage temperature | T_{stg} | -55 | - | 150 | $^\circ\text{C}$ | - |
| Operating junction temperature | T_j | -55 | - | 150 | $^\circ\text{C}$ | - |
| Mounting torque | - | - | - | n.a. | Ncm | - |
| Diode forward current rating | I_S | - | - | 14 | A | $T_C=140^\circ\text{C}$ Current is limited by $T_{j\max} = 150^\circ\text{C}$; Lower case temp does increase current capability |
| Diode pulse current ¹⁾ | $I_{S,\text{pulse}}$ | - | - | 207 | A | $T_C=25^\circ\text{C}$ |
| Reverse diode dv/dt ³⁾ | dv/dt | - | - | 5 | V/ns | $V_{DS}=0\text{ to } 300\text{V}$, $I_{SD}\leq 13\text{A}$, $T_j=25^\circ\text{C}$ see table 8 |
| Maximum diode commutation speed | di/dt | - | - | 1000 | A/ μs | $V_{DS}=0\text{ to } 300\text{V}$, $I_{SD}\leq 13\text{A}$, $T_j=25^\circ\text{C}$ see table 8 |
| Insulation withstand voltage | V_{ISO} | - | - | n.a. | V | V_{rms} , $T_C=25^\circ\text{C}$, $t=1\text{min}$ |

¹⁾ Pulse width t_p limited by $T_{j\max}$

²⁾ The dv/dt has to be limited by appropriate gate resistor

³⁾ Identical low side and high side switch

2 Thermal characteristics

Table 3 Thermal characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|------------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - case | R_{thJC} | - | - | 0.46 | °C/W | - |
| Thermal resistance, junction - ambient | R_{thJA} | - | - | 62 | °C/W | device on PCB, minimal footprint |
| Thermal resistance, junction - ambient for SMD version | R_{thJA} | - | 45 | 55 | °C/W | Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm ² (one layer, 70µm thickness) copper area. Tap exposed to air. PCB is vertical without air stream cooling. |
| Soldering temperature, reflow soldering allowed | T_{sold} | - | - | 260 | °C | reflow MSL1 |

3 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

For applications with applied blocking voltage >70% of the specified blocking voltage, it is required that the customer evaluates the impact of cosmic radiation effect in early design phase and contacts the Infineon sales office for the necessary technical support by Infineon

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|----------------------------------|---------------|--------|----------------|-------|----------|---|
| | | Min. | Typ. | Max. | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | 600 | - | - | V | $V_{GS}=0V, I_D=1mA$ |
| Gate threshold voltage | $V_{(GS)th}$ | 3.5 | 4.0 | 4.5 | V | $V_{DS}=V_{GS}, I_D=0.79mA$ |
| Zero gate voltage drain current | I_{DSS} | - | - | 2 | μA | $V_{DS}=600V, V_{GS}=0V, T_j=25^\circ C$ $V_{DS}=600V, V_{GS}=0V, T_j=150^\circ C$ |
| Gate-source leakage current | I_{GSS} | - | - | 100 | nA | $V_{GS}=20V, V_{DS}=0V$ |
| Drain-source on-state resistance | $R_{DS(on)}$ | - | 0.036 0.084 | 0.040 | Ω | $V_{GS}=12V, I_D=13A, T_j=25^\circ C$ $V_{GS}=12V, I_D=13A, T_j=150^\circ C$ |
| Gate resistance | R_G | - | 0.8 | - | Ω | $f=1MHz, \text{open drain}$ |

Table 5 Dynamic characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|--------------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Input capacitance | C_{iss} | - | 3128 | - | pF | $V_{GS}=0V, V_{DS}=300V, f=250kHz$ |
| Output capacitance | C_{oss} | - | 50 | - | pF | $V_{GS}=0V, V_{DS}=300V, f=250kHz$ |
| Effective output capacitance, energy related ¹⁾ | $C_{o(er)}$ | - | 168 | - | pF | $V_{GS}=0V, V_{DS}=0 \text{ to } 300V$ |
| Effective output capacitance, time related ²⁾ | $C_{o(tr)}$ | - | 1476 | - | pF | $I_D=\text{constant}, V_{GS}=0V, V_{DS}=0 \text{ to } 300V$ |
| Output charge | Q_{oss} | - | 443 | - | nC | $V_{GS}=0V, V_{DS}=0 \text{ to } 300V$ |
| Turn-on delay time | $t_{d(on)}$ | - | 23 | - | ns | $V_{DD}=300V, V_{GS}=13V, I_D=13A, R_G=8.0\Omega; \text{ see table 9}$ |
| Rise time | t_r | - | 5 | - | ns | $V_{DD}=300V, V_{GS}=13V, I_D=13A, R_G=8.0\Omega; \text{ see table 9}$ |
| Turn-off delay time | $t_{d(off)}$ | - | 120 | - | ns | $V_{DD}=300V, V_{GS}=13V, I_D=13A, R_G=8.0\Omega; \text{ see table 9}$ |
| Fall time | t_f | - | 9 | - | ns | $V_{DD}=300V, V_{GS}=13V, I_D=13A, R_G=8.0\Omega; \text{ see table 9}$ |

Table 6 Gate charge characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-----------------------|---------------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Gate to source charge | Q_{gs} | - | 17 | - | nC | $V_{DD}=300V, I_D=13A, V_{GS}=0 \text{ to } 12V$ |
| Gate to drain charge | Q_{gd} | - | 28 | - | nC | $V_{DD}=300V, I_D=13A, V_{GS}=0 \text{ to } 12V$ |
| Gate charge total | Q_g | - | 83 | - | nC | $V_{DD}=300V, I_D=13A, V_{GS}=0 \text{ to } 12V$ |
| Gate plateau voltage | $V_{plateau}$ | - | 5.4 | - | V | $V_{DD}=300V, I_D=13A, V_{GS}=0 \text{ to } 12V$ |

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 300V

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 300V

Table 7 Reverse diode characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-------------------------------|-----------|--------|------|------|---------|--|
| | | Min. | Typ. | Max. | | |
| Diode forward voltage | V_{SD} | - | 0.82 | - | V | $V_{GS}=0V, I_F=13A, T_j=25^\circ C$ |
| Reverse recovery time | t_{rr} | - | 360 | - | ns | $V_R=300V, I_F=13A, di_F/dt=100A/\mu s$; see table 8 |
| Reverse recovery charge | Q_{rr} | - | 5.5 | - | μC | $V_R=300V, I_F=13A, di_F/dt=100A/\mu s$; see table 8 |
| Peak reverse recovery current | I_{rrm} | - | 32 | - | A | $V_R=300V, I_F=13A, di_F/dt=100A/\mu s$; see table 8 |

4 Electrical characteristics diagrams

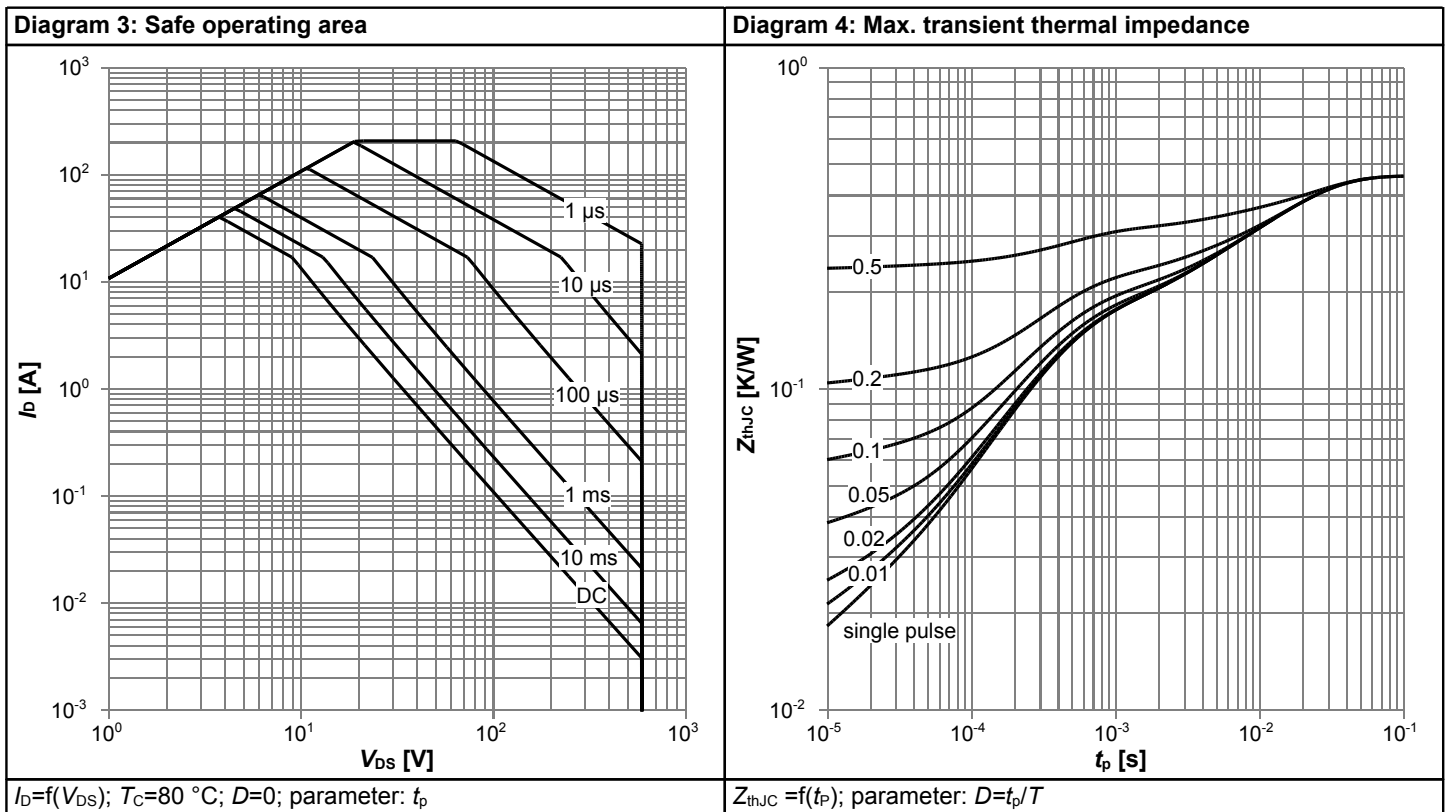
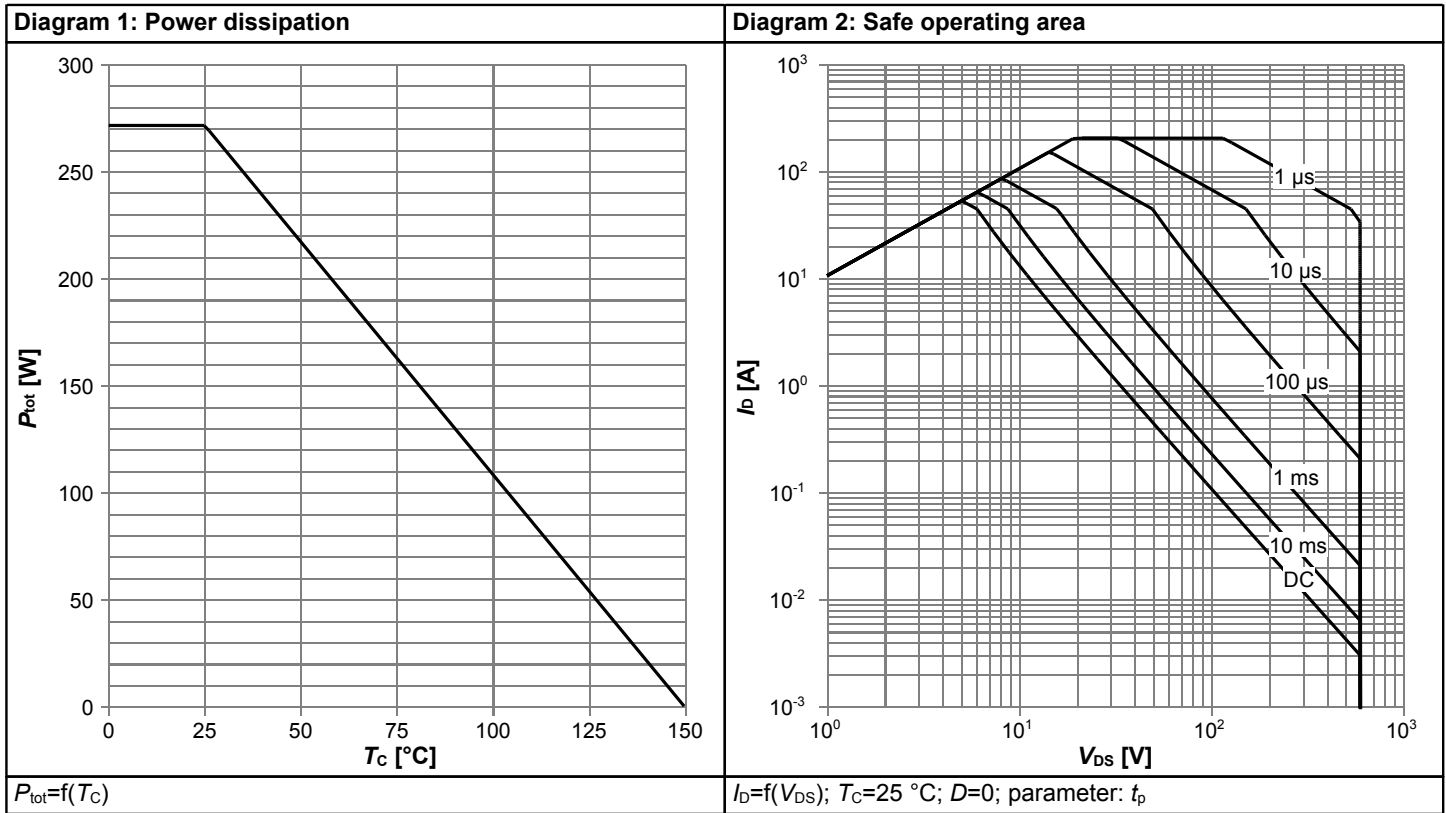
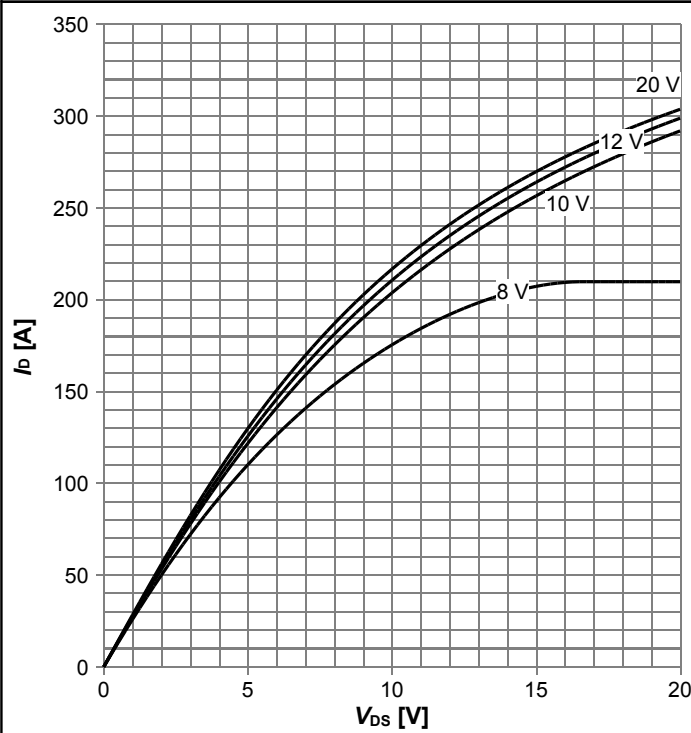
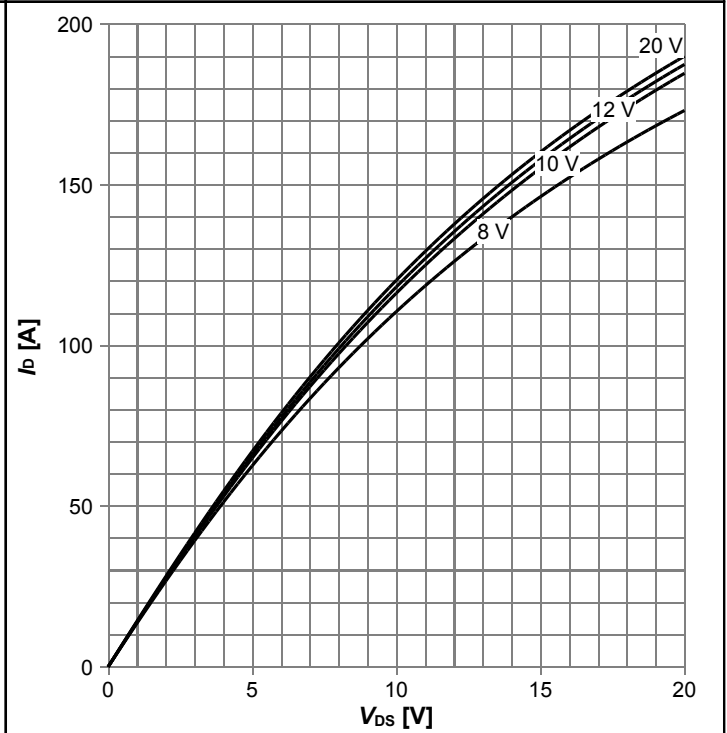


Diagram 5: Typ. output characteristics



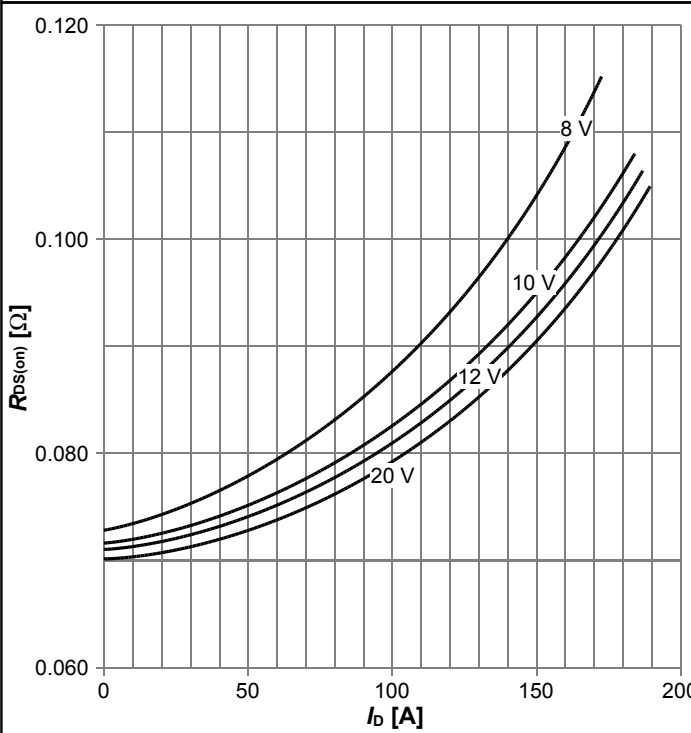
$I_D=f(V_{DS})$; $T_j=25\text{ °C}$; parameter: V_{GS}

Diagram 6: Typ. output characteristics



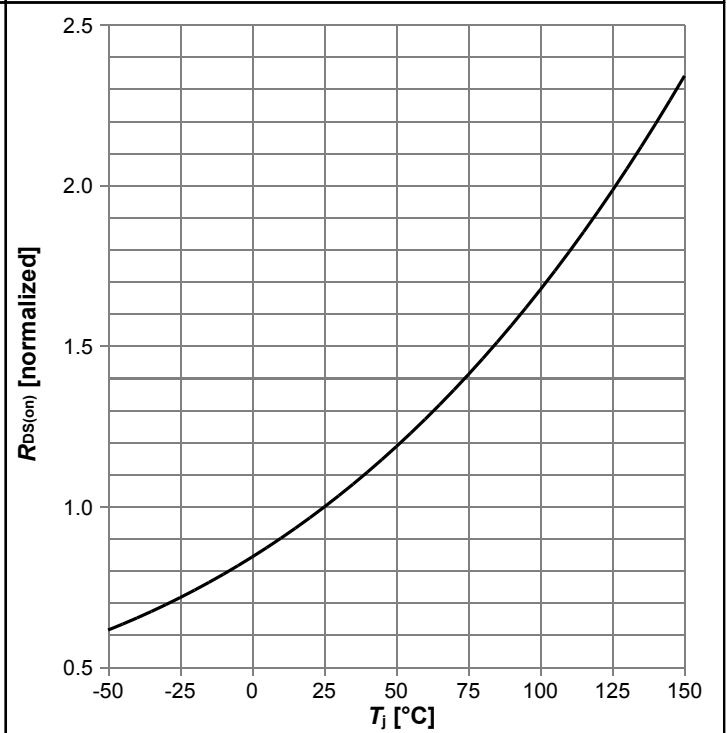
$I_D=f(V_{DS})$; $T_j=125\text{ °C}$; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



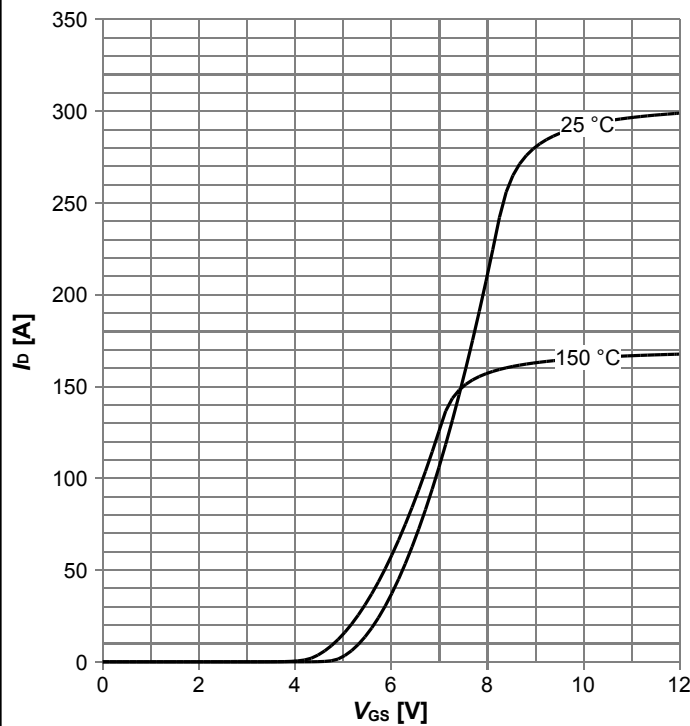
$R_{DS(on)}=f(I_D)$; $T_j=125\text{ °C}$; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



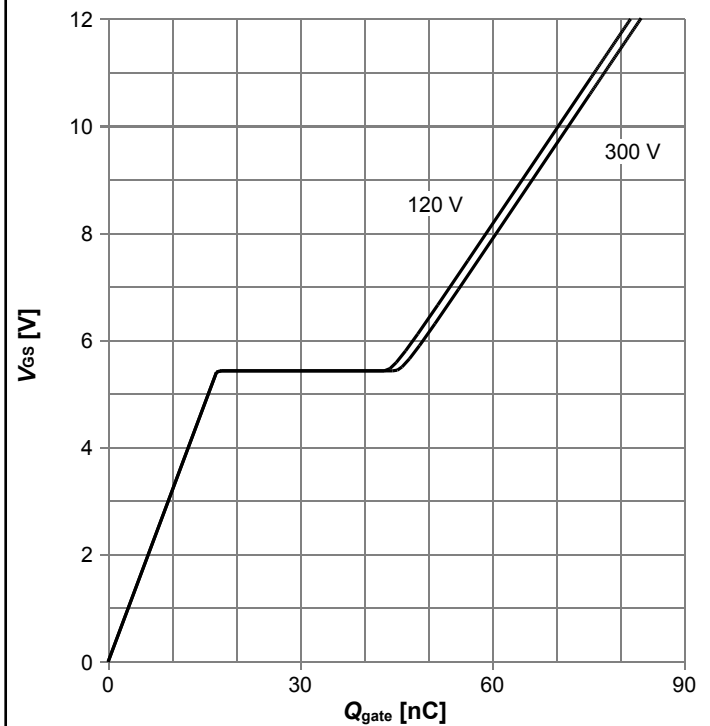
$R_{DS(on)}=f(T_j)$; $I_D=13\text{ A}$; $V_{GS}=12\text{ V}$

Diagram 9: Typ. transfer characteristics



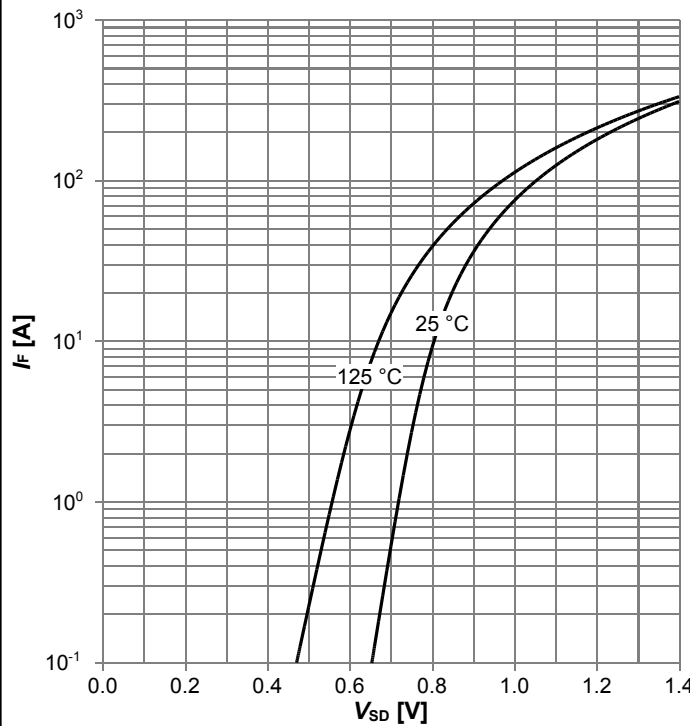
$I_D=f(V_{GS}); V_{DS}=20V$; parameter: T_j

Diagram 10: Typ. gate charge



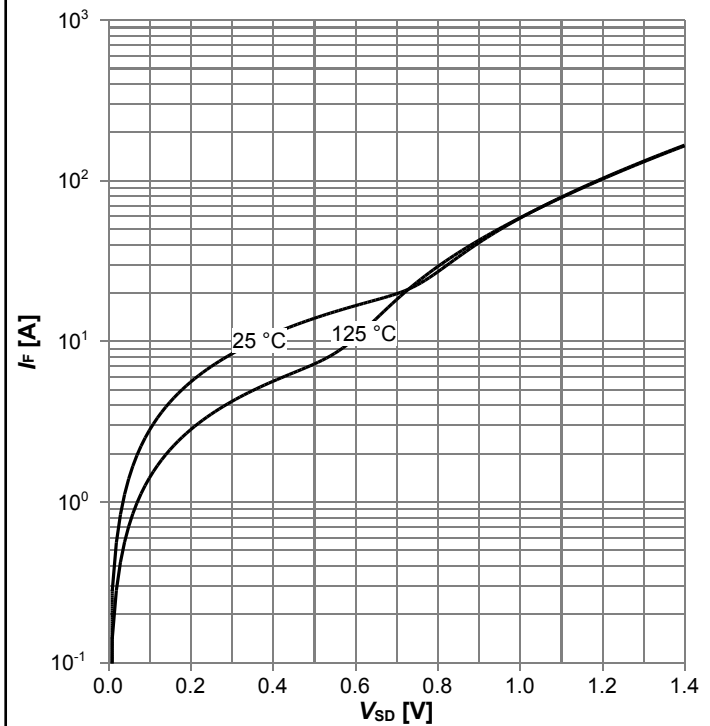
$V_{GS}=f(Q_{gate}); I_D=13\text{ A pulsed}$; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode



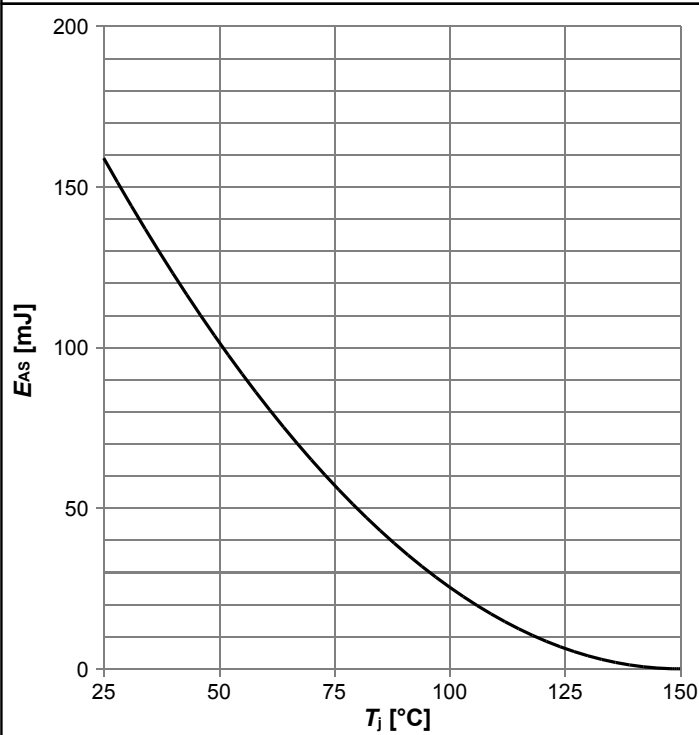
$I_F=f(V_{SD}); V_{GS}=0\text{ V}$; parameter: T_j

Diagram 12: Forward characteristics of reverse diode



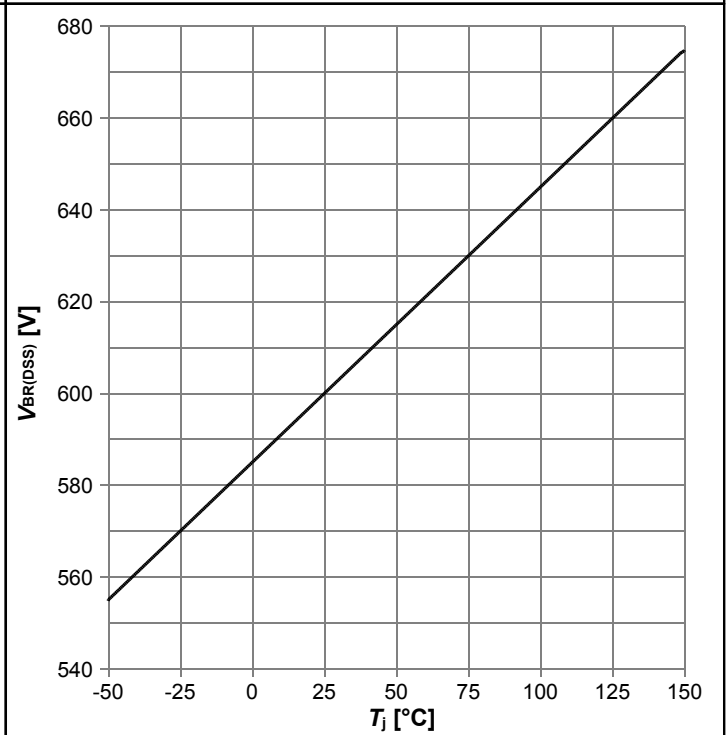
$I_F=f(V_{SD}); V_{GS}=12\text{ V}$; parameter: T_j

Diagram 13: Avalanche energy



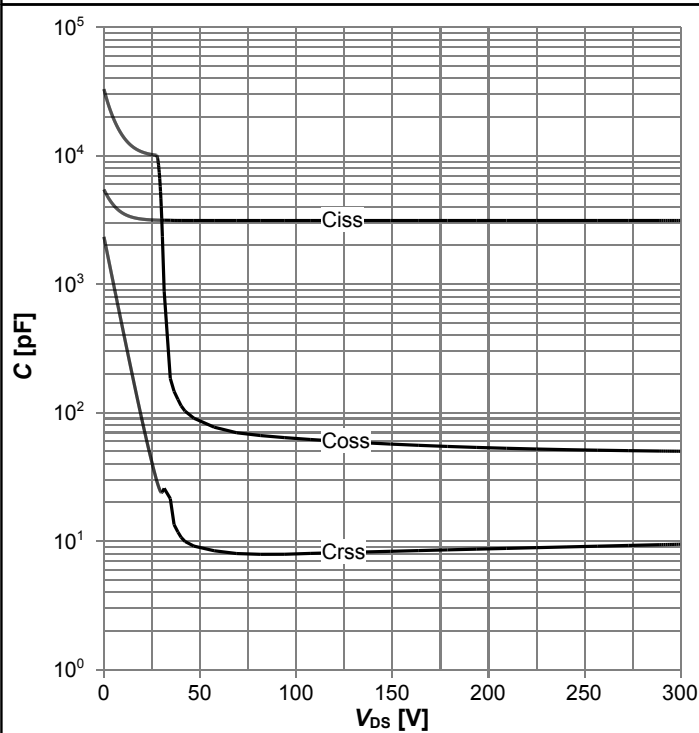
$E_{AS}=f(T_j); I_D=2.8 \text{ A}; V_{DD}=50 \text{ V}$

Diagram 14: Drain-source breakdown voltage



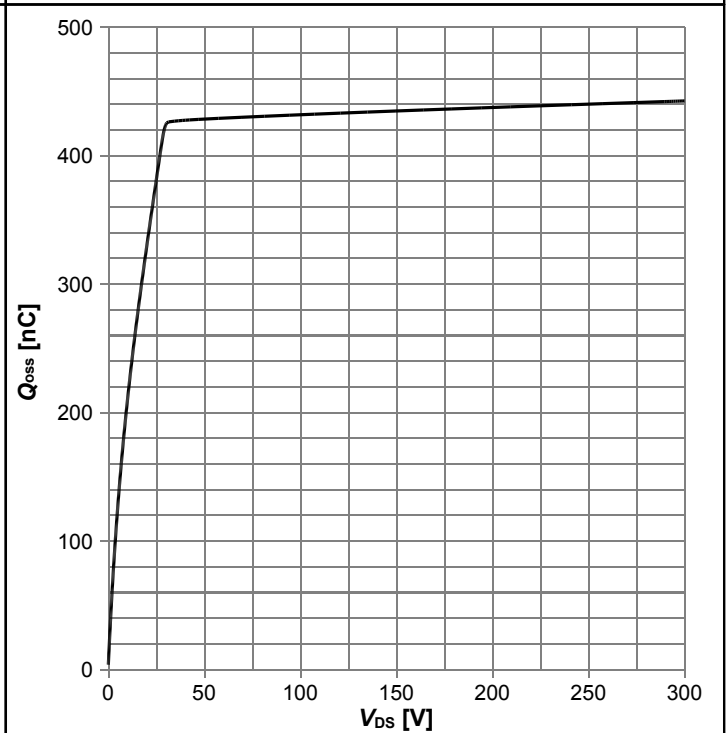
$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Diagram 15: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0 \text{ V}; f=250 \text{ kHz}$

Diagram 17: Typ. Qoss output charge



$Q_{oss}=f(V_{DS}); V_{GS}=0 \text{ V}$

5 Test Circuits

Table 8 Diode characteristics



Table 9 Switching times (ss)

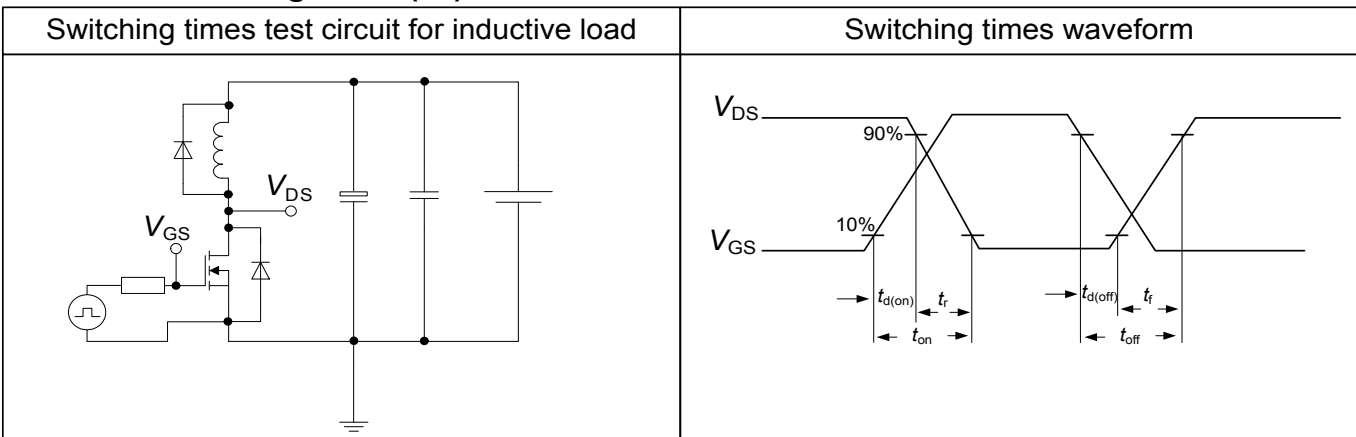
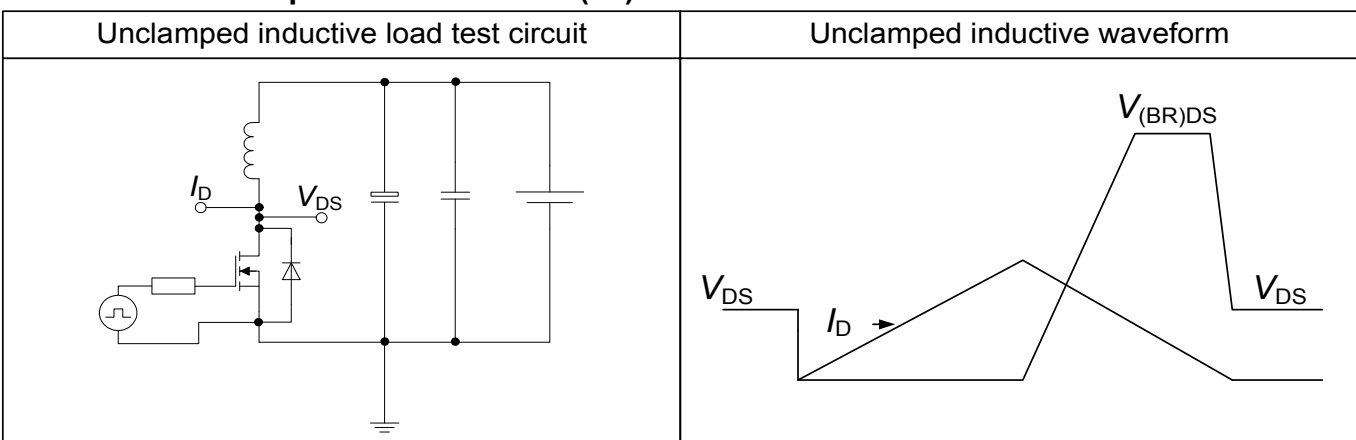
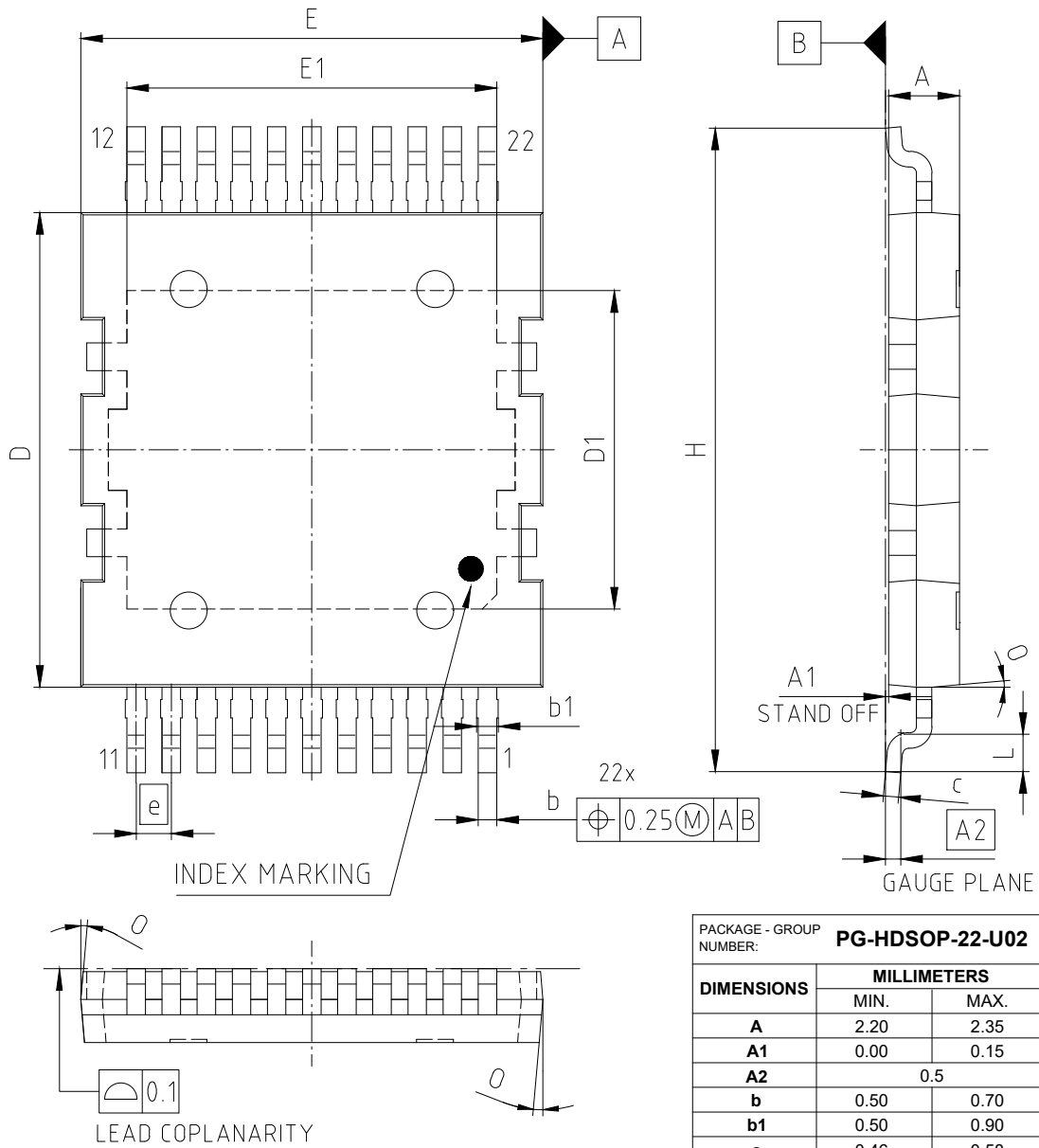


Table 10 Unclamped inductive load (ss)



6 Package Outlines



| PACKAGE - GROUP NUMBER: | | PG-HDSOP-22-U02 | |
|-------------------------|-------------|------------------------|--|
| DIMENSIONS | MILLIMETERS | | |
| | MIN. | MAX. | |
| A | 2.20 | 2.35 | |
| A1 | 0.00 | 0.15 | |
| A2 | 0.5 | | |
| b | 0.50 | 0.70 | |
| b1 | 0.50 | 0.90 | |
| c | 0.46 | 0.58 | |
| D | 15.30 | 15.50 | |
| D1 | 10.23 | 10.43 | |
| E | 14.90 | 15.10 | |
| E1 | 11.91 | 12.11 | |
| e | 1.14 | | |
| N | 22 | | |
| H | 20.81 | 21.11 | |
| L | 1.20 | 1.40 | |
| O | 5° | | |

Figure 1 Outline PG-HDSOP-22, dimensions in mm

7 Appendix A

Table 11 Related Links

- IFX CoolMOS S7 Webpage: www.infineon.com
- IFX CoolMOS S7 application note: www.infineon.com
- IFX CoolMOS S7 simulation model: www.infineon.com
- IFX Design tools: www.infineon.com

Revision History

IPQC60R040S7

Revision: 2022-11-23, Rev. 2.0

Previous Revision

| Revision | Date | Subjects (major changes since last revision) |
|----------|------------|--|
| 2.0 | 2022-11-23 | Release of final version |

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