SRD30
~1.06—3.3 Gbits/s Serializer and Deserializer (Macro)

Features
- Designed to operate in Ethernet, Fibre Channel, and SONET/SDH (synchronous digital hierarchy) applications.
- Selectable data rate (1.06 Gbits/s—1.6 Gbits/s, 2.12 Gbits/s—3.33 Gbits/s).
- 100 MHz—168 MHz reference clock frequency range. Option for a 622 MHz reference clock.
- 16-bit or 20-bit parallel I/O interface in full-rate mode.
- Programmable control and configuration interface to define the various device configurations.
- Analog modularity and digital library interface for design flexibility.
- Automatic lock-to-reference in absence of receive data.
- CML high-speed interface I/O for use with backplane or cable media.
- Programmable transmit pre-emphasis optimized for backplane applications.
- Requires one external resistor for bias current generation.
- Requires no external components for clock recovery and frequency synthesis.
- 80 mW per transceiver (typical) at 3.125 Gbits/s.
- Low powerdown dissipation.
- Multiple output amplitude modes for reduced power consumption in chip-to-chip applications.
- 1.0 V ± 5% power supply.
- Additional power supply options are available for compatibility with high speed I/O in older technologies.
- 0 °C—125 °C junction temperature.

Potential Applications
- Drives chip-to-chip and across backplanes.
- SONET
- Fibre Channel
- 10 Gbit Ethernet (XAUI)

Description
The SRD30 is a high-speed serializer/deserializer (SerDes) macrocell designed for Agere’s AGR90 ASIC platform. This macrocell includes a current mode logic (CML) high-speed serial interface and makes use of a proprietary CDR architecture along with the sharing of a PLL across multiple RX and TX channels to reduce area and power consumption. These characteristics make it suitable for applications that require high channel counts.

Figure 1. SRD30 Block Diagram
Modular Macrocell

- Consists of the following three smaller blocks:
  - PLL.
  - Transmit channel block (TX).
  - Receiver channel block (RX).

- Five standard configurations as follows:
  - Nine RX blocks and one PLL.
  - Nine TX blocks and one PLL.
  - Ten RX/TX block pairs and one PLL.
  - One TX block and one PLL.
  - Four RX/TX block pairs and one PLL.

Channels

- Ten RX/TX pairs maximum per macro.
- Elimination or selective powering down of unnecessary blocks within a macro, along with multiple macro configurations, allows 1—10 channels.

Interfaces

- High speed: current mode logic (CML) ac and dc coupling allowed. LVDS and LVPECL compatibility is available with off-chip components.
- Parallel data: CMOS selectable between a 16-bit or 20-bit parallel I/O in full-rate mode. In half-rate mode, the transmitter has an 8-/10-bit interface.
- Registers and control logic: a four-line serial interface, allowing each channel to be addressed individually with minimal routing.

Power Consumption

- 80 mW per channel (typical, including common circuitry) consumed when all ten channels are operating at 3.125 Gbits/s.
- If less than ten channels are operating, the power consumption per channel increases to include more of the common circuitry.

Independent Powerdown

- Independent user-selectable powerdown of the following:
  - CML buffers.
  - Individual transmit blocks.
  - Individual receive blocks.
  - PLL.

Reset

- Resets any macro or any RX/TX block within the device.
- Includes a power-on reset circuit within the macros. This circuit is used solely to reset the SerDes blocks within a macro after a powerup event. (No external access to the output of this circuit is provided.)

PLL (Phase-Locked Loop)

- The PLL is based on a differential ring oscillator at half of the intended data rate.
- The synthesized frequency can be programmed to either 8X or 10X the reference frequency.
- PLL relock without reset: the PLL can relock without requiring a reset (for example, after switching reference clocks).
- A PLL lock indicator is provided.

Transmitter

- Each transmit (TX) block serializes a parallel data word with a width of 16 bits or 20 bits depending on the control register setting.
- The TX block transforms the parallel input word into a serial data stream by using a high-speed clock that is synthesized from the TX reference clock by the PLL.

Transmit Pre-Emphasis

- The transmit block output buffer can be programmed through the serial register interface to select between no pre-emphasis and one of four levels of pre-emphasis.
- Pre-emphasis boosts the high frequencies in the transmitted data to compensate for losses present in backplanes, thus extending the useful range of transmission.
Reduced Amplitude Output

- The TX block output buffer can be programmed through the serial interface to provide one of four different levels of output amplitude: 1.0 V, 0.85 V, 0.7 V, and 0.55 V.
- These amplitude modes meet most standard requirements and allow chip-to-chip applications and other less stringent applications to reduce the power consumption.

Skew Between Blocks

- The skew will be less than 1.25 UI between transmit blocks if the blocks are within a macro or within an adjacent macro and use the same reference clock with a maximum skew of 100 ps (±50 ps) between macros.
- Two macros totaling 17 channels at 2.5 Gbits/s will have less than 400 ps skew between any two channels.

Receiver

- The receive block (RX) transforms a high-speed serial bit stream into a stream of parallel words and recovers a high-speed clock from the serial data.
- The receive block (RX) further divides this clock down to provide a clock that has a frequency equal to the parallel word rate and that is phase-aligned to the word boundary.
- The CDR block that forms the core of the receiver is a proprietary design that results in significant power and area savings.

Loss of Signal and Signal Level Detector

- Simple analog loss of signal detector with a fixed threshold between an 85 mVp-p differential and 175 mVp-p differential.

Automatic Lock to Reference

- The receive CDR automatically locks to reference in the absence of receive data. When a loss of signal is indicated, the reference clock is automatically switched to the RX serial inputs (this can also be disabled by setting a bit in the serial control I/F).
- The receiver can also be forced to lock to reference by setting a bit in the serial control I/F.

Loss of Reference Clock

- If the reference clock (REFCLK) bit is lost, the VCO in the PLL is forced to its lowest frequency.
- An alarm bit in the PLL status register indicates this condition. This condition is also indicated by the core output signals of the PLL.

High-Speed Clock Output

- A clock at a 1/8 or 1/10 data rate from both the transmitter and the receiver blocks is provided to circuitry outside the macrocell.

Testability Features

- Allows testability within the ASIC.
- Test modes are not encoded, allowing mixing and matching of test modes.
- Self-synchronizing PRBS compatible with Agilent® and Anritsu® bit error rate test systems.
- Internal loopback for parallel and serial data for RX/TX macro option.
- Independent transmit and receive built-in self-test.

Digital Library Interface

- Standard digital library interface allowing digital blocks from the Agere library or custom blocks to be integrated into the device.
- Examples include PRBS, link state machine, 8b/10b encoder, byte aligner, and custom blocks.
Advanced Product Brief

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