

8K x 8 HIGH-SPEED CMOS STATIC RAM

JANUARY 2020

FEATURES

- High-speed access time: 10 ns
- CMOS low power operation
 - 1 mW (typical) CMOS standby
 - 125 mW (typical) operating
- TTL compatible interface levels
- Single 5V power supply
- Fully static operation: no clock or refresh required
- Lead-free available

DESCRIPTION

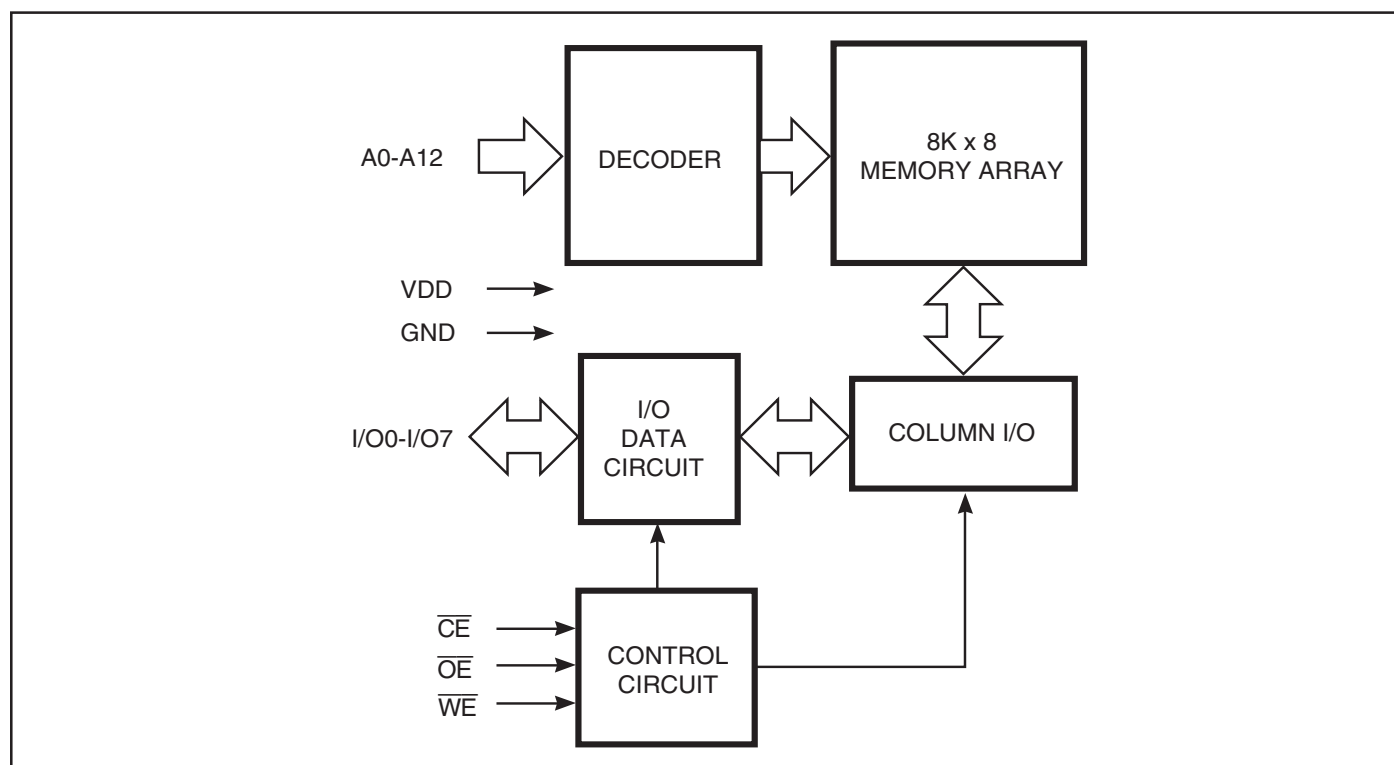
The *ISSI* IS61C64AL is a very high-speed, low power, 8192-word by 8-bit static RAM. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 10 ns with low power consumption.

When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down to 150 μ W (typical) with CMOS input levels.

Easy memory expansion is provided by using one Chip Enable input, $\overline{CE}$. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.

The IS61C64AL is packaged in the JEDEC standard 28-pin, 300-mil SOJ, and TSOP.

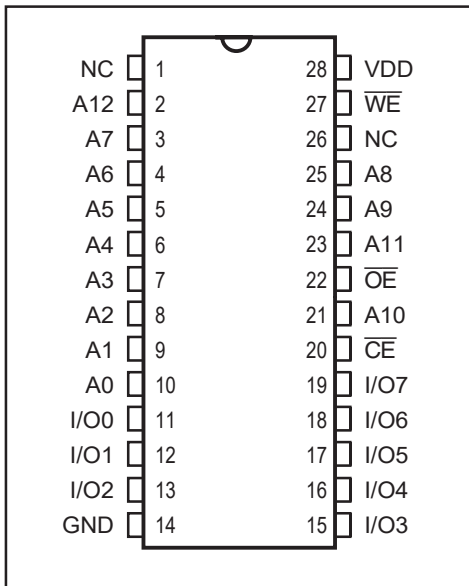
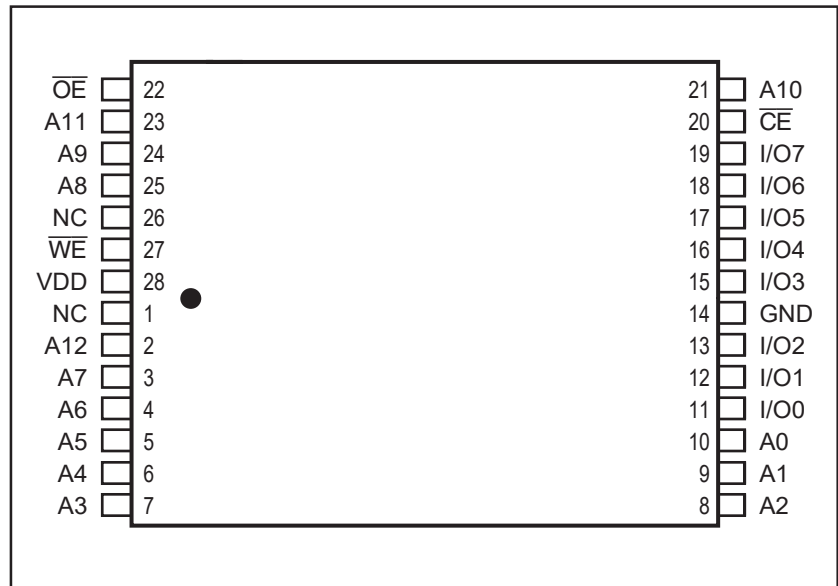
FUNCTIONAL BLOCK DIAGRAM



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TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O Operation	V _{DD} Current
Not Selected (Power-down)	X	H	X	High-Z	I _{SB1} , I _{SB2}
Output Disabled	H	L	H	High-Z	I _{CC}
Read	H	L	L	DOUT	I _{CC}
Write	L	L	X	DIN	I _{CC}

PIN CONFIGURATION
28-Pin SOJPIN CONFIGURATION
28-Pin TSOP (Type 1)

PIN DESCRIPTIONS

A0-A12	Address Inputs
$\overline{CE}$	Chip Enable 1 Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
NC	No Connect
V _{DD}	Power
GND	Ground

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
V _{TERM}	Terminal Voltage with Respect to GND	−0.5 to +7.0	V
T _{STG}	Storage Temperature	−65 to +150	°C
P _T	Power Dissipation	1.5	W
I _{OUT}	DC Output Current (LOW)	20	mA

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	Speed	V _{DD} ⁽¹⁾
Commercial	0°C to +70°C	-10	5V ± 5%
Industrial	−40°C to +85°C	-10	5V ± 5%

Note:

1. If operated at 12ns, V_{DD} range is 5V ± 10%.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{DD} = Min., I _{OH} = −4.0 mA	2.4	—	V
V _{OL}	Output LOW Voltage	V _{DD} = Min., I _{OL} = 8.0 mA	—	0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{DD} + 0.5	V
V _{IL}	Input LOW Voltage ⁽¹⁾		−0.3	0.8	V
I _{LI}	Input Leakage	GND ≤ V _{IN} ≤ V _{DD}	Com. Ind.	−1 2	1 2 μA
I _{LO}	Output Leakage	GND ≤ V _{OUT} ≤ V _{DD} , Outputs Disabled	Com. Ind.	−1 −2	1 2 μA

Note:

1. V_{IL} = −3.0V for pulse width less than 10 ns.

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions		-10		-12		Unit
				Min.	Max.	Min.	Max.	
I _{CC1}	V _{DD} Operating Supply Current	V _{DD} = Max., $\overline{CE}$ = V _{IL}	Com.	—	20	—	20	mA
		I _{OUT} = 0 mA, f = 0	Ind.	—	25	—	25	
I _{CC2}	V _{DD} Dynamic Operating Supply Current	V _{DD} = Max., $\overline{CE}$ = V _{IL}	Com.	—	45	—	35	mA
		I _{OUT} = 0 mA, f = f _{MAX}	Ind.	—	50	—	45	
			typ. ⁽²⁾		25		25	
I _{SB1}	TTL Standby Current (TTL Inputs)	V _{DD} = Max.,	Com.	—	1	—	1	mA
		V _{IN} = V _{IH} or V _{IL} $\overline{CE} \geq V_{IH}$, f = 0	Ind.	—	2	—	2	
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{DD} = Max.,	Com.	—	350	—	350	μA
		$\overline{CE} \geq V_{DD} - 0.2V$,	Ind.	—	450	—	450	
		V _{IN} ≥ V _{DD} - 0.2V, or V _{IN} ≤ 0.2V, f = 0	typ. ⁽²⁾		200		200	

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V_{DD} = 5V, T_A = 25°C. Not 100% tested.

CAPACITANCE^(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	8	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	10	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 5.0V.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

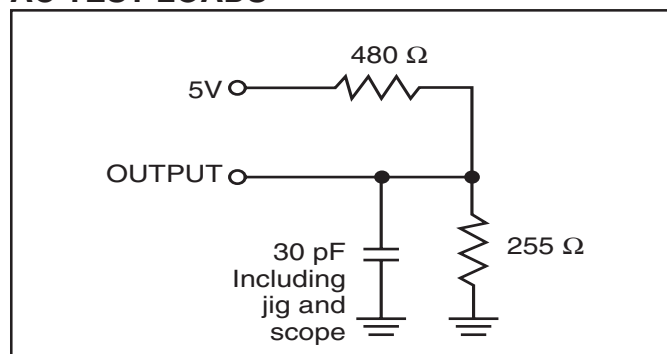
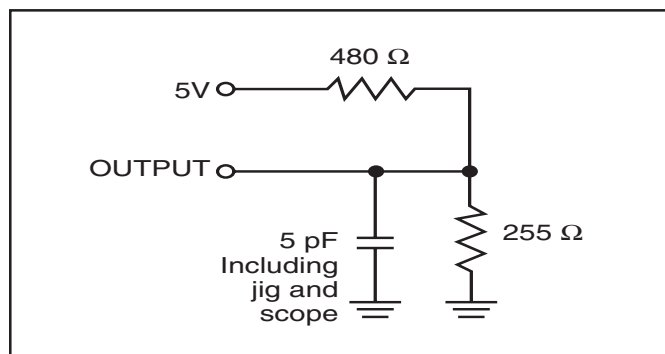
Symbol	Parameter	-10 ns		-12 ns		Unit
		Min.	Max	Min.	Max.	
t_{RC}	Read Cycle Time	10	—	12	—	ns
t_{AA}	Address Access Time	—	10	—	12	ns
t_{OHA}	Output Hold Time	2	—	2	—	ns
t_{ACS}	$\overline{CE}$ Access Time	—	10	—	12	ns
t_{DOE}	$\overline{OE}$ Access Time	—	6	—	6	ns
$t_{LZOE}^{(2)}$	$\overline{OE}$ to Low-Z Output	0	—	0	—	ns
$t_{HZOE}^{(2)}$	$\overline{OE}$ to High-Z Output	—	5	—	6	ns
$t_{LZCS}^{(2)}$	$\overline{CE}$ to Low-Z Output	2	—	3	—	ns
$t_{HZCS}^{(2)}$	$\overline{CE}$ to High-Z Output	—	5	—	7	ns
$t_{PU}^{(3)}$	$\overline{CE}$ to Power-Up	0	—	0	—	ns
$t_{PD}^{(3)}$	$\overline{CE}$ to Power-Down	—	10	—	12	ns

Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

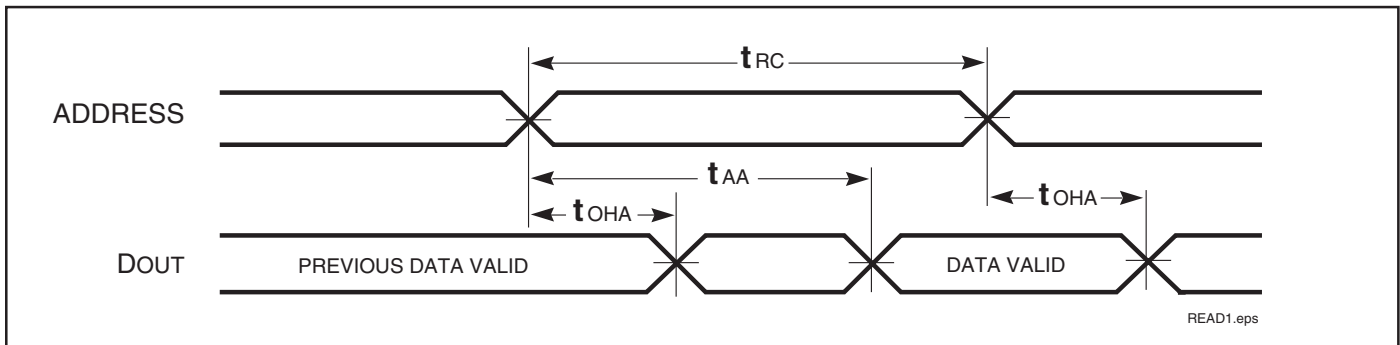
AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Levels	1.5V
Output Load	See Figures 1 and 2

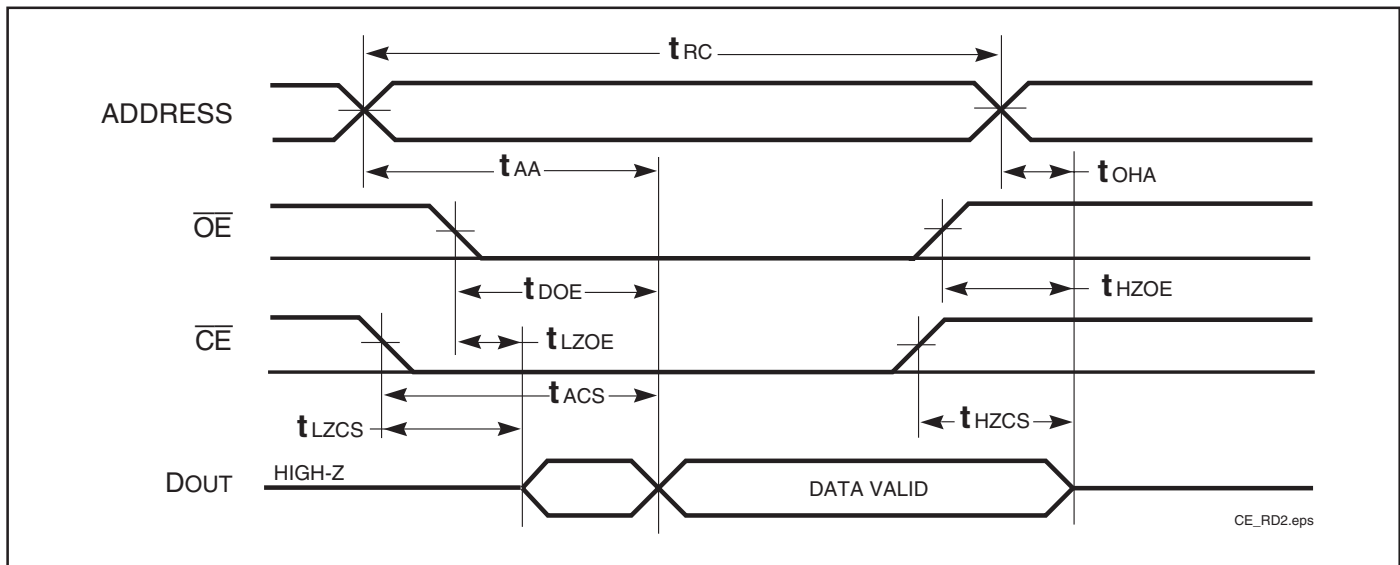
AC TEST LOADS**Figure 1****Figure 2**

AC WAVEFORMS

READ CYCLE NO. 1^(1,2)



READ CYCLE NO. 2^(1,3)



Notes:

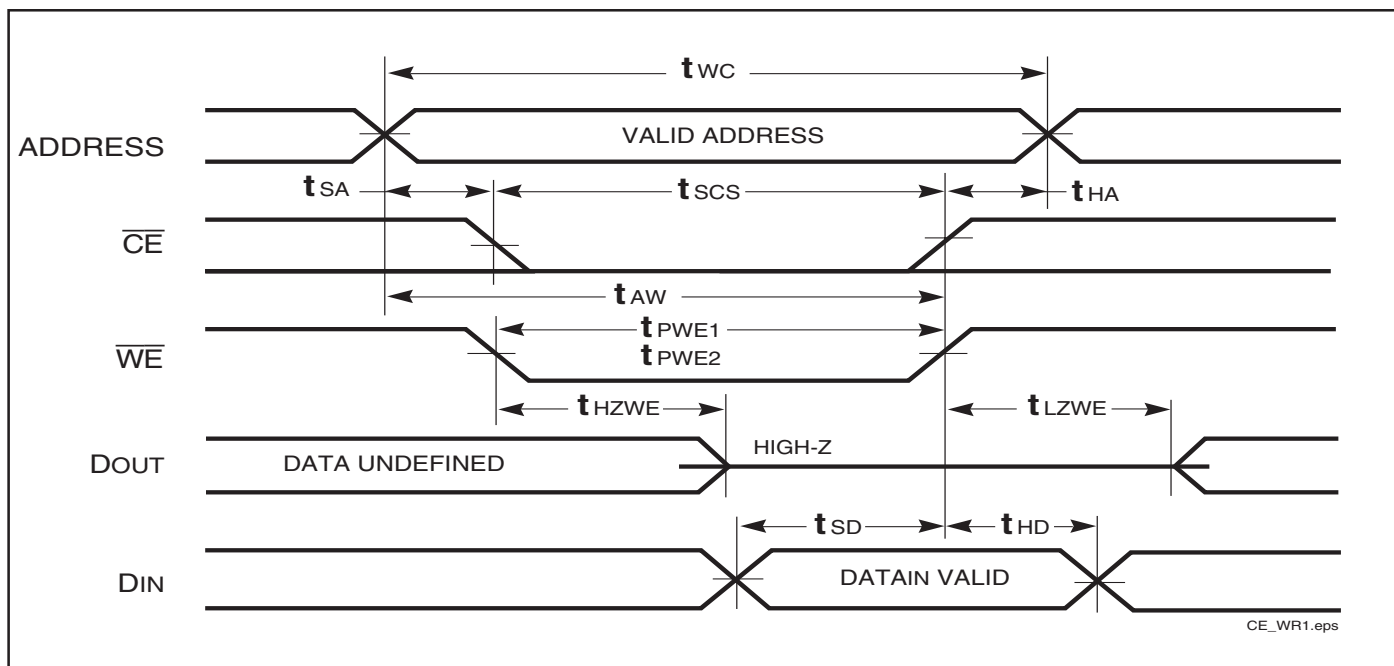
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL} .
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

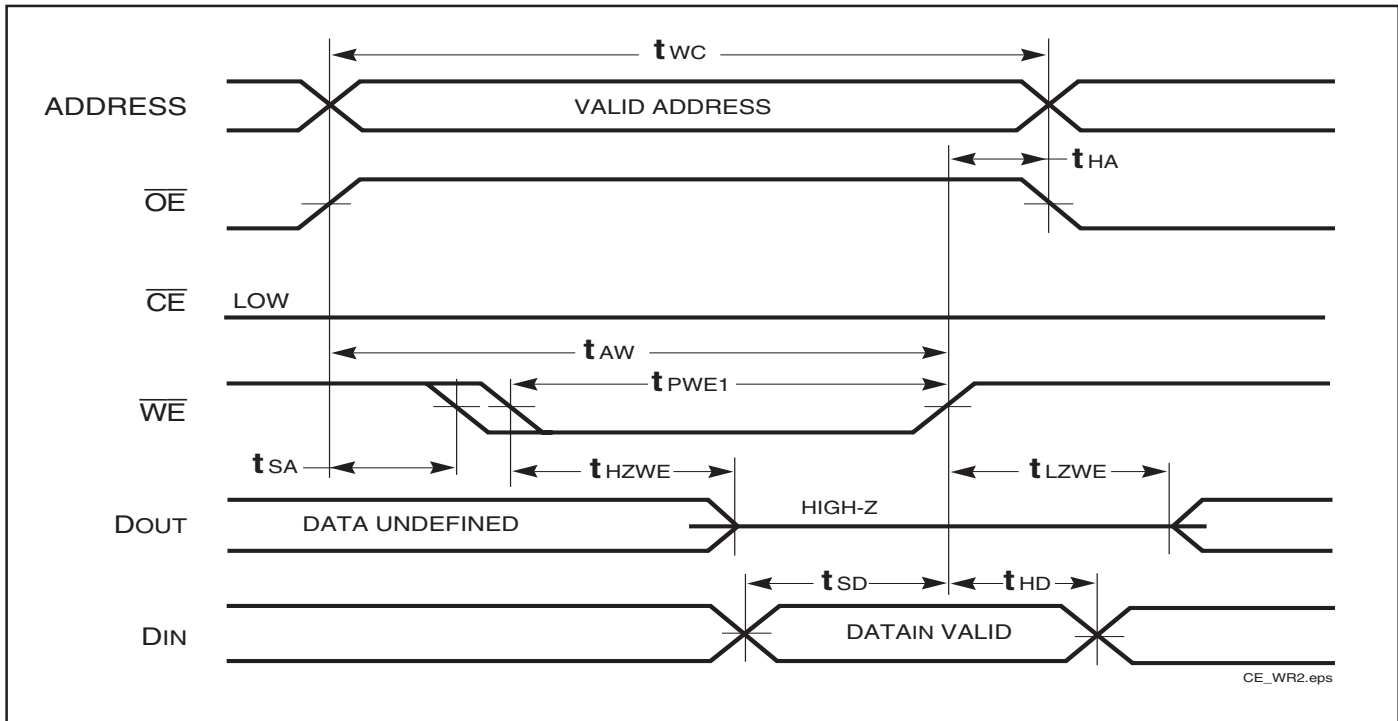
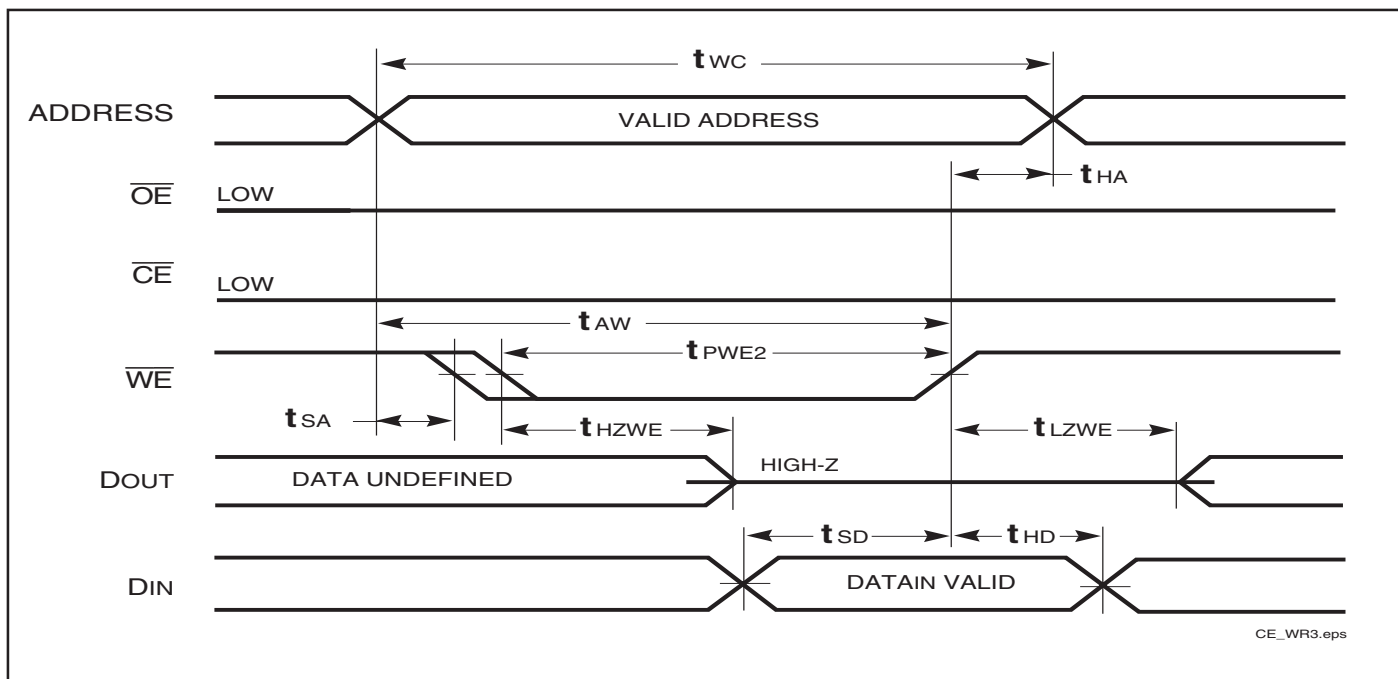
WRITE CYCLE SWITCHING CHARACTERISTICS^(1,3) (Over Operating Range)

Symbol	Parameter	-10 ns		-12 ns		Unit
		Min.	Max	Min.	Max.	
t_{WC}	Write Cycle Time	10	—	12	—	ns
t_{SCS}	$\overline{CE}$ to Write End	9	—	10	—	ns
t_{AW}	Address Setup Time to Write End	9	—	10	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	ns
t_{PWE1}	$\overline{WE}$ Pulse Width ($\overline{OE}$ LOW)	9	—	9	—	ns
t_{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$ HIGH)	8	—	8	—	ns
t_{SD}	Data Setup to Write End	7	—	7	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	ns
$t_{HZWE}^{(2)}$	$\overline{WE}$ LOW to High-Z Output	—	6	—	6	ns
$t_{LZWE}^{(2)}$	$\overline{WE}$ HIGH to Low-Z Output	0	—	0	—	ns

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

AC WAVEFORMS**WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)^(1,2)**

WRITE CYCLE NO. 2 ($\overline{OE}$ is HIGH During Write Cycle) ^(1,2)**WRITE CYCLE NO. 3** ($\overline{OE}$ is LOW During Write Cycle) ⁽¹⁾**Notes:**

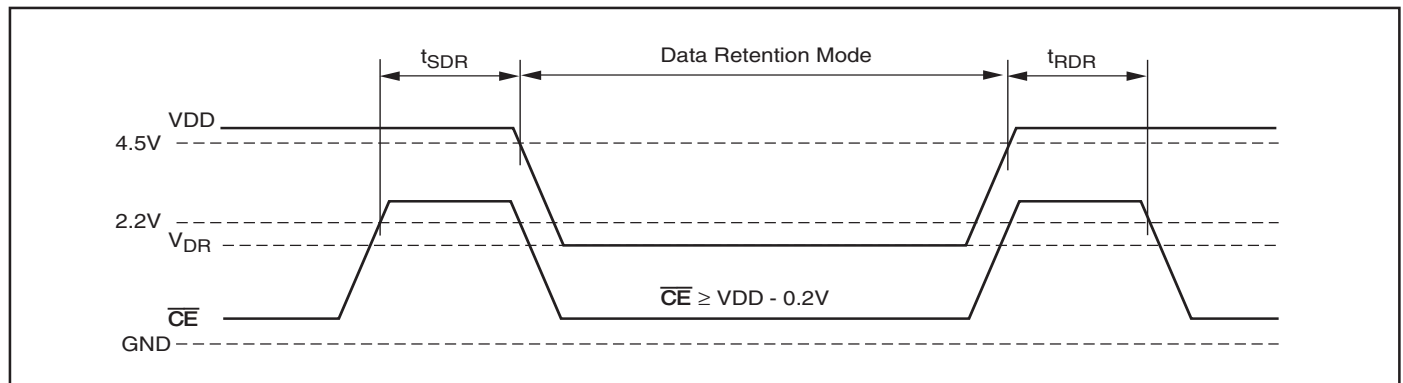
1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} \geq V_{IH}$.

DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ. ⁽¹⁾	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform	2.0		5.5	V
I_{DR}	Data Retention Current	$V_{DD} = 2.0V, \overline{CE} \geq V_{DD} - 0.2V$ $V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq V_{SS} + 0.2V$	—	50	90	μA
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform	0		—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform	t_{RC}		—	ns

Note:

1. Typical Values are measured at $V_{DD} = 5V$, $T_A = 25^\circ C$ and not 100% tested.

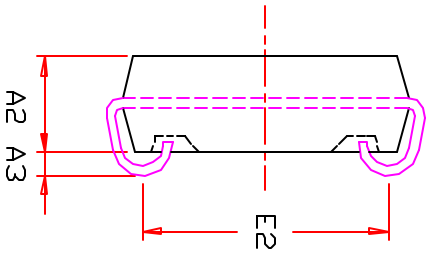
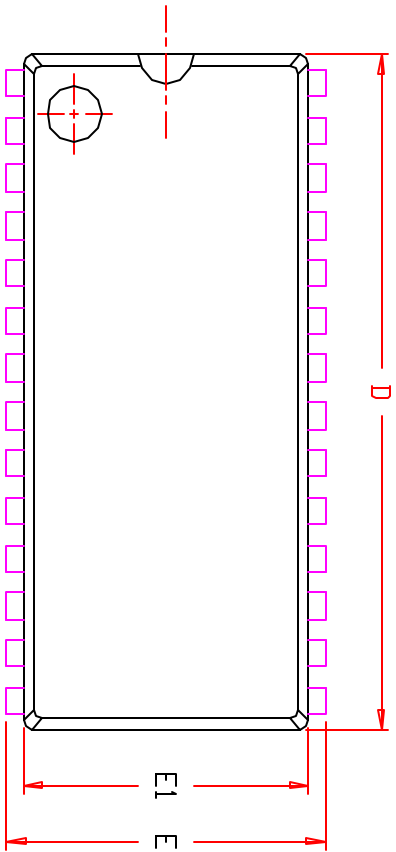
DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)



ORDERING INFORMATION

Industrial Range: -40°C to +85°C

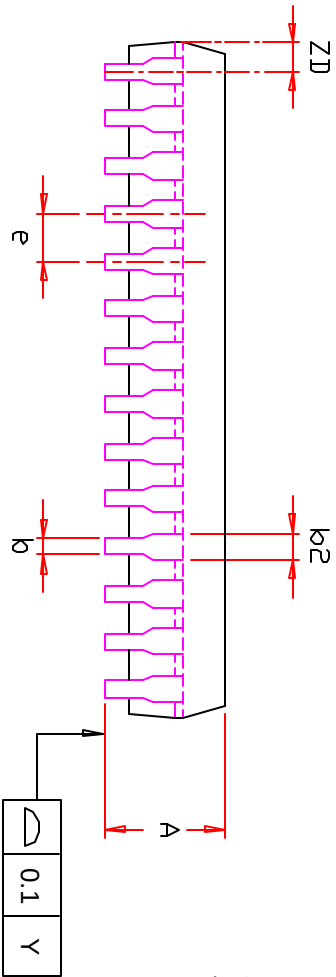
Speed (ns)	Order Part No.	Package
10	IS61C64AL-10JLI	300-mil Plastic SOJ, Lead-free
	IS61C64AL-10TLI	Plastic TSOP, Lead-free



SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A	3.05		3.76
A2	2.41	2.54	2.67
A3	0.64		1.09
k	0.36		0.56
k2	0.66		0.81
D	17.70		18.54
E	8.26	8.56	8.81
E1	7.42		7.75
E2	6.22		7.29
e	1.27 BSC		
ZD	0.95 REF.		
Y	0.1		

NOTE :

1. Controlling dimension : mm
2. Dimension D1 adn E do not include mold protrusion .
3. Dimension b2 does not include dambar protrusion/intursion.
4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.



ISSI

TITLE

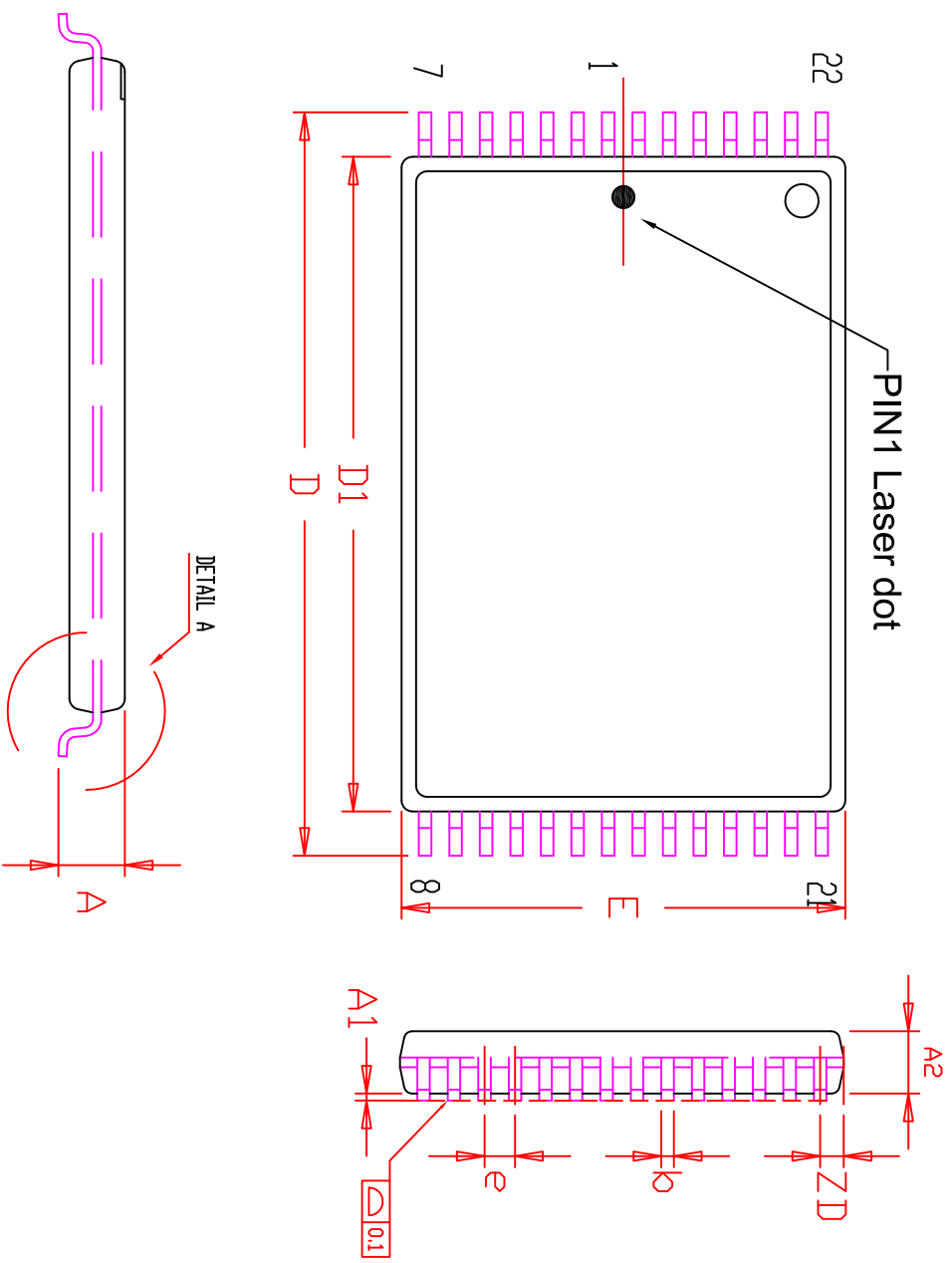
28L 300mil SOJ
Package Outline

REV.

C

DATE

07/05/2006



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.95		1.20	0.037		0.047
A1	0.05		0.20	0.002		0.008
A2	0.90		1.05	0.035		0.041
b	0.17	0.22	0.27	0.007	0.009	0.011
D	13.20	13.40	13.60	0.520	0.528	0.535
D1	11.70	11.80	11.90	0.461	0.465	0.469
E	7.90	8.00	8.10	0.311	0.315	0.319
e	0.55 BSC.			0.022 BSC.		
L	0.30	0.50	0.70	0.012	0.020	0.028
L1	0.25 BSC.			0.010 BSC.		
ZD	0.425 REF.			0.017 REF.		
Θ	0	3°	5°	0	3°	5°
C	0.12		0.21	0.12		0.21

NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D1 AND E DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.
4. Reference Document : JEDEC MO-183

ISSI	TITLE	28L 8x13.4mm TSOP-1	REV.	G	DATE	10/28/2019
	Package Outline					