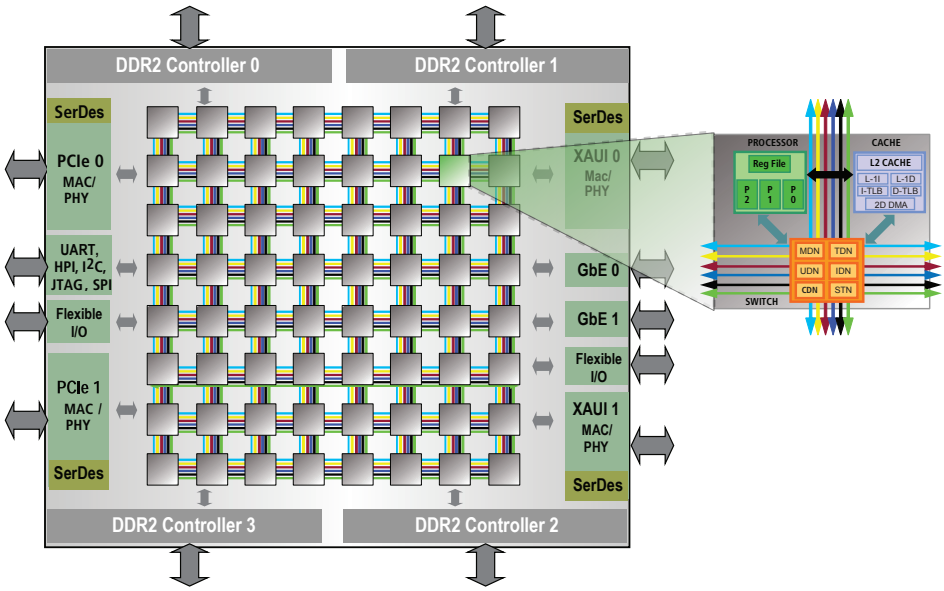
TILE*Pro*64™ Processor

Product Brief

Overview

The TILE*Pro*64™ processor brings multicore computing to the next level, enabling embedded applications to achieve the highest compute performance in the market. This latest-generation processor features 64 identical processor cores (tiles) interconnected with Tilera's iMesh™ on-chip network. Each tile consists of a complete, full-featured processor as well as L1 and L2 cache and a non-blocking switch that connects the tiles into the mesh. The TILE*Pro*™ family incorporates Tilera's Dynamic Distributed Cache (DDC™) technology that accelerates coherent cache performance by a factor of two compared with other multicores. As with all Tilera® processors, each tile can independently run a full operating system, or multiple tiles grouped together can run a multi-processing OS like SMP Linux.



The TILE*Pro*64 processor slashes board real estate requirements and system costs by integrating a complete set of memory and I/O controllers, therefore eliminating the need for an external north bridge or south bridge. New TileDirect™ technology provides coherent I/O directly into the tile caches to deliver ultimate low-latency packet processing performance.

The TILE*Pro*64 Processor is programmed in ANSI standard C and C++, enabling developers to leverage their existing software investment. Tiles can be grouped in clusters to apply the appropriate amount of horsepower to each application. Since multiple operating system instances can be run on the TILE*Pro*64 simultaneously, it can replace multiple CPU subsystems for both the data plane and control plane.

Combining multiple C-programmable processor tiles with the iMesh multicore technology enables the TILE*Pro*64 to achieve the performance of a fixed function ASIC or FPGA in a powerful software-programmable solution.

	Features	Enables
Massively Scalable Performance	• 8 x 8 grid general purpose processor cores (tiles) • 32-bit VLIW processors with 64-bit instruction bundle • 3-deep pipeline with up to 3 instructions per cycle • 5.6 Mbytes of on-chip cache • Up to 443 billion operations per second (BOPS) • 37 Tbps of on-chip mesh interconnect enables linear application scaling • 200 Gbps memory bandwidth with four 64-bit DDR2 controllers	• 20 Gbps of nProbe • 15+ Gbps Snort® • H.264 HD encode for 10 streams of 1080p30 (baseline profile, customer codec) • x.264 HD encode for 4 streams of 720p30 (main profile) • 15+ channels of OFDM baseband processing
Power Efficiency	• 700MHz, 866MHz operating frequency • 19-23 W @700MHz for typical applications • Idle tiles can be put into low-power sleep mode • Power efficient inter tile communications	• Highest performance per watt • Simple thermal management and power supply design • Small system form factor • Low operating cost
Integrated Solution	• Four 64-bit DDR2 memory controllers with optional ECC • Two 10GbE XAUI interfaces; configurable MAC or PHY mode • Two 4-lane PCIe interfaces; root complex or endpoint mode • Two GbE MAC interfaces • Flexible I/O interface	• Reduces BOM cost - standard interfaces on-chip • Dramatically reduced board real estate • Direct interface to leading L2-L3 switch vendors
Multicore Development Environment Options	• ANSI standard C/C++ compiler • Advanced profiling and debugging designed for multicore programming • Supports SMP Linux with 2.6 kernel • TMC libraries for efficient inter-tile communication	• Run off-the-shelf C/C++ programs • Reduce debug and optimization time • Faster time to production code • Standard multicore communication mechanisms

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Target Applications

The TILE*Pro* family offers both flexibility and performance to support a wide range of compute-intensive applications, including advanced networking, digital multimedia and telecom, and wireless infrastructure.

Processing Flexibility

The processor core in the TILE*Pro*64 combines the features of a general-purpose CPU together with powerful signal processing and SIMD capabilities. As a result, it can integrate multiple functions on a single processor, reducing system cost and simplifying system design. For example, it can transcode multiple streams of video and perform audio echo cancelling while simultaneously running encryption and network stack functions.

A robust protection-level hierarchy together with virtual memory and Tilera's Multicore Hardwall™ technology provides kernel-level protection related to both shared memory and user-level streaming and messaging.

Intelligent Networking Products

The TILE*Pro*64 processor is ideally suited for 10-20Gbps intelligent network services:

- Intrusion detection/prevention (IDS/IPS)
- Unified Threat Management (UTM)
- L4-7 deep packet inspection
- Network monitoring and forensics
- Quality of Service (QoS) provisioning

Digital Multimedia Products

The TILE*Pro*64 processor also excels at digital multimedia processing, easily taking the place of multiple DSPs or FPGAs:

- Video transcoding/transrating
- Professional video encoding
- Streaming IPTV and video on demand
- Ad insertion
- Video post-production processing

Wireless Infrastructure

In current GSM/CDMA and next generation WiMAX and LTE wireless networks, the TILE*Pro*64 processor delivers programmable computing solutions for:

- Base transceiver station (BTS)
- Base station controller (BSC)
- Wireless backbone gateways (GGSN, SGSN, media gateway)

Development Environment

Tilera's Multicore Development Environment™ (MDE) is a complete, standards-based multicore programming solution that enables developers to take full advantage of the parallel processing potential of the Tile Processor™ architecture.

Powerful innovations allow the developer to take a Gentle Slope Programming™ approach to multicore software development. By leveraging open source software and the developer's existing software code base, impressive results can be achieved in an extremely short period of time. As developers become more familiar with large-scale multicore, they can take advantage of the enhanced tools and libraries offered in the MDE.

Tilera's MDE includes:

- Standard Eclipse-based IDE
- ANSI C/C++ compiler
- Multi-tile, timing-accurate simulator
- Whole chip debug and performance analysis
- Line-by-line profiling
- Complete SMP Linux support
- TMC library for efficient inter-communication
- PCIe hardware development platforms

Scalable Processing and Ease of Use for Embedded Application Developers

The TILE*Pro*64 addresses developers' needs for scalable multiprocessor performance, with the highest performance per watt, and ease of programming. The TILEPro family specifically accelerates threaded and shared-memory applications, giving unprecedented results with unmodified code. With the on-chip iMesh network, Dynamic Distributed Cache architecture, and the industry's best multicore development tools, Tilera provides solutions that are uniquely suited to today's networking, multimedia, and wireless applications.

Ordering Information

Part Number	Description	I/O Interfaces	Processor Frequency	DDR2 Memory Speed	Number of Tiles	Package	Operating Temperature
TLR3-6480BG-7C	Standard Speed	2 XAUI, 2 PCIe, 2GbE	700 MHz	800 MHz	64	1517 BGA	0-70º
TLR3-6480BG-9C	High Performance	2 XAUI, 2 PCIe, 2GbE	866 MHz	800 MHz	64	1517 BGA	0-70º

For more information on Tilera products, visit www.tilera.com

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