TP3001B Datasheet

Product Version TP3001B

Release Version 0.6

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Telepath Technologies Co., Ltd.

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Document number:
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Contents

Figures

Tables

1 TP3001B Introduction

TP3001B is a baseband receiver that supports CMMB mobile TV standard. It can deliver CMMB mobile TV reception on all kinds of handheld devices together with a RF tuner.

Telepath Technologies Co. Ltd, the developer of TP3001B baseband demodulator, is committed to provide the best chipset solution and services to our partners to enable mobile TV reception in their products. To enable a fast design in, TP3001B development kit will be provided to our Partners to speed their design process of low-cost, high-performance CMMB-compatible solutions. The development kit includes the following items:

① End-to-end (RF and baseband) reference design

② CMMB signal source

③ TP3001B evaluation board

④ TP3001B specifications

⑤ TP3001B Firmware and SDK

⑥ Performance monitor(BER,BLER,RSSI)

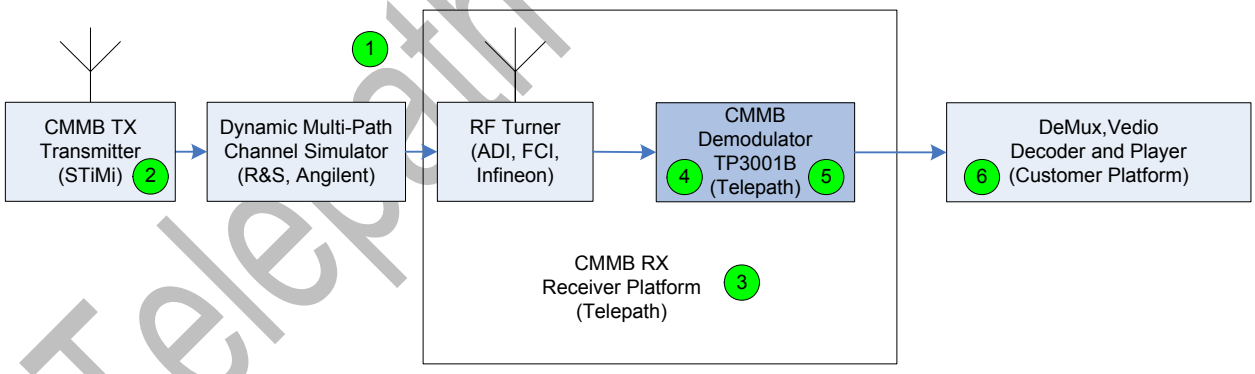

Figure 1-1 TP3001B Product Solution- Single Mode

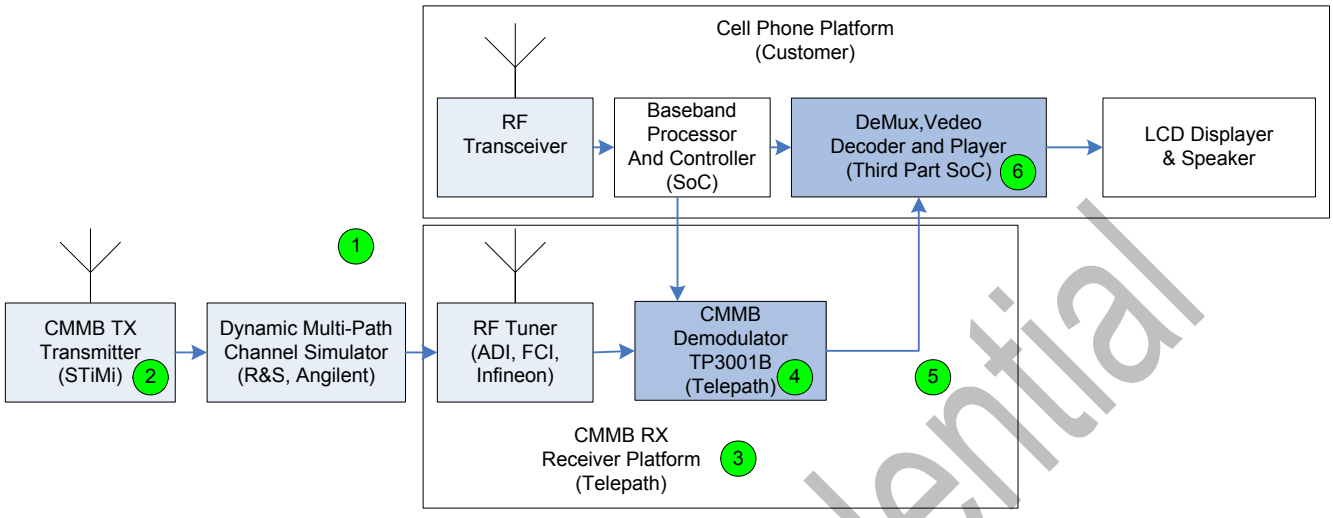

Figure 1-2 TP3001B Product Solution- Dual Mode

1.1 Key Features

- Fully CMMB Standard GY/T 220.1-2006 and GY/T 220.2-2006 compatible
- Support 8 MHz bandwidth mode with 4K FFT mode
- Automatic and intelligent power saving control
- Time slicing for dynamic power saving
- BPSK/QPSK/16QAM demodulation modes for different data throughput
- On chip LDPC decoder and RS decoder for best mobile channel performance
- Able to receive two service channels simultaneously
- Support up to 12 timeslots for BPSK, 6 timeslots for QPSK and 2 timeslots for 16QAM simultaneously
- Able to provide service channels with different data rates, for example, 1×512kbps + 1×256kbps, or 2×384kbps
- On-chip 10-bit Analog-to-Digital Converter (ADC) and low frequency DAC for baseband analog input and tuner AGC
- Differential I/Q analog input
- Crystal oscillator: 10MHz/20MHz ± 10ppm
- I2C for tuner control and Demod configuration
- Serial interface for multiplexing sub-frame stream
- Configurable baseband AGC voltage output
- LFBGA81 package (8mm×8mm×1.3mm)
- CMOS 0.13μm

1.2 Block Diagram

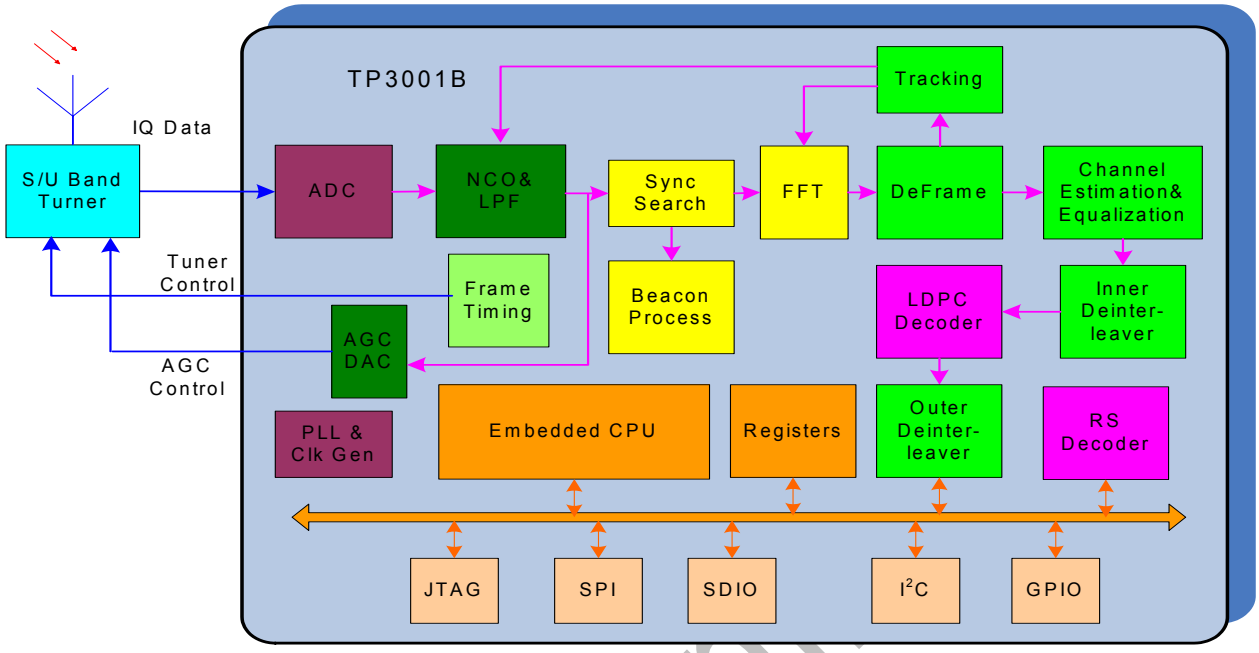

Figure 1-3 TP3001B Block Diagram

2 Powering the TP3001B

2.1 TP3001B Supplies

The demodulator has two groups of power supply domains including IO and core.

The core domain consists of three different 1.2V±10% groups that should be connected to the same 1.2V supply.

The IO domain consists of four different multi-voltage 3.3V±10%. Unlike the core domain each IO group can be powered by different voltage.

2.2 TP3001B Power Sequence and Reset Timing

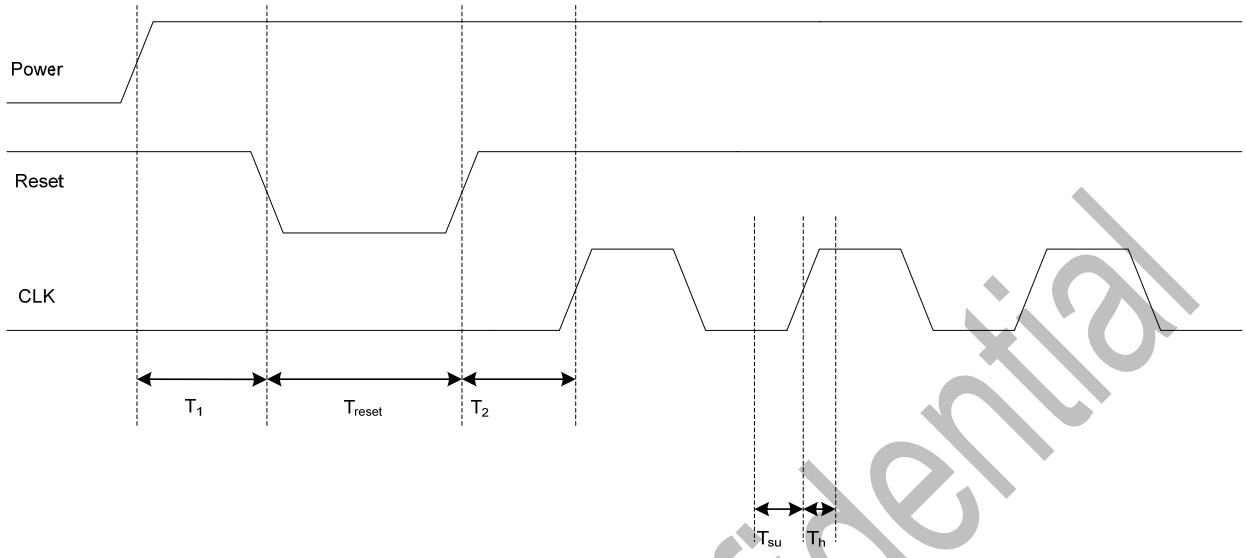

Figure 2-1 TP3001B Power Sequence and Reset Timing

Timing descriptions:

Table 2-1. Timing Signals Description

Parameter	Value	Description
T1		The delay between power on and reset.
Treset		Reset active time(negative polarity)
T2		The delay between reset and clock posedge.
Tsu		The setup time before clock posedge
Th		The hold time after clock posedge

2.3 TP3001B Power States and Power Modes

There are two power states in TP3001B, Power Down and RX (Active receive) modes.

In the RX state, there are also two modes: with timing slicing mode and without timing slicing mode.During signal receiving at RX mode, , TP3001B works with timing slicing mode for power saving..

3 Clocking the TP3001B Chipset

There are two crystals that can be applied in TP3001B, 10MHz and 20MHz.
± 10ppm frequency offset is required for both crystals. If the offset is smaller, the performance is better.

The SCAN_CLK pin is be used to select different crystals.

4 TP3001B Interface Modes

4.1 Scope

TP3001B receive I/Q data from RF tuner, and transfer data to the host processor, so its interfaces include the following: SDIO, SPI, I2C.

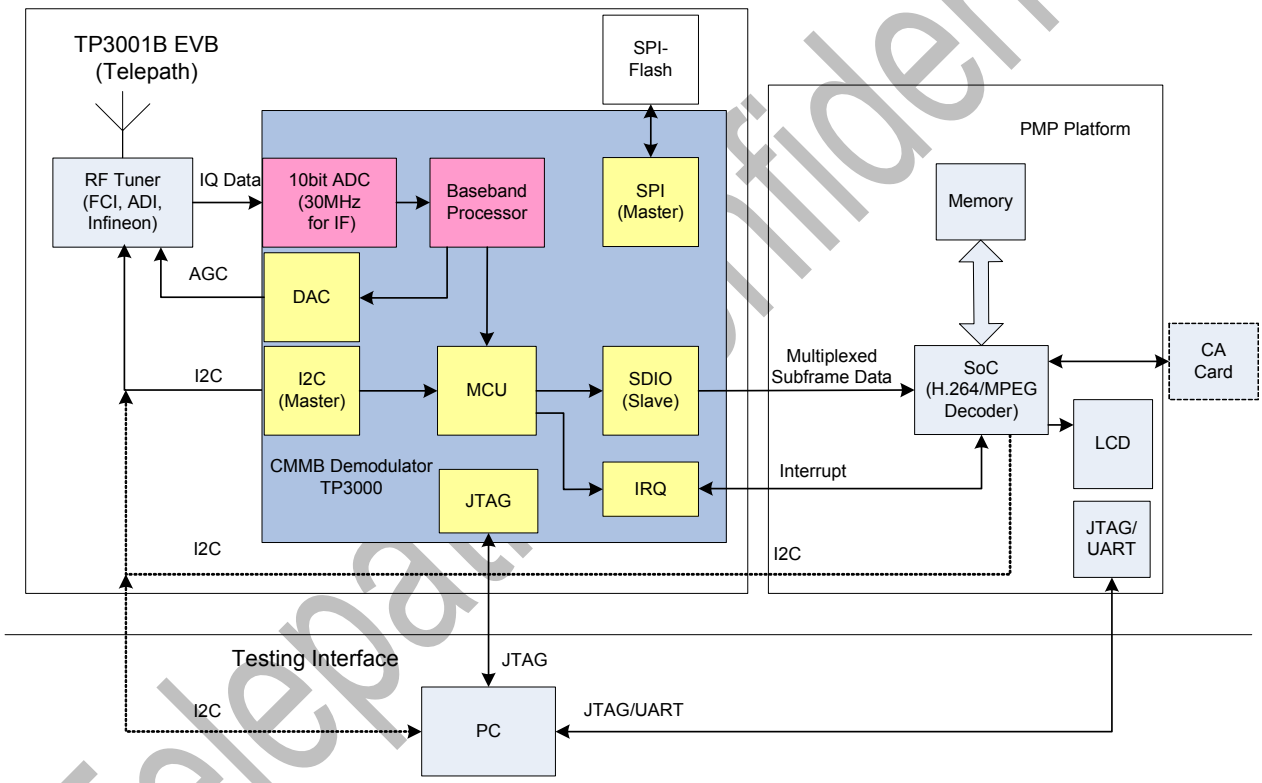

Figure 4-1 TP3001B Evaluation Board

4.2 SDIO Interface

The SDIO interface can run at the SD1, SD4 and SPI mode, and it meets SDIO specification 1.2.

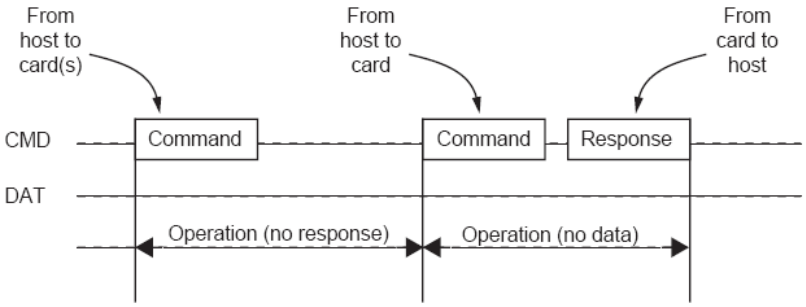

Figure 4-2 Typical Command Response timing

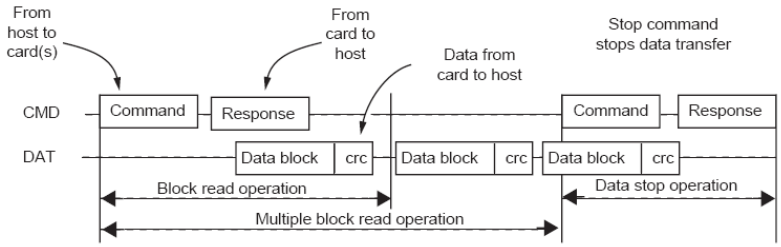

Figure 4-3 Typical multi block read timing

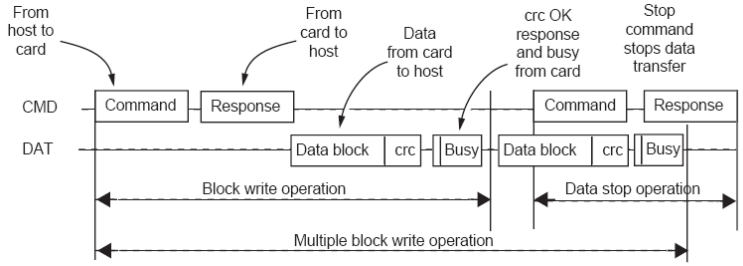

Figure 4-4 Typical multi block write timing

4.3 SPI Interface

Signal descriptions:

Table 4-1. SPI Description

Signal Name	Input/Output	Bit width	description
miso	I	1	Spi bus slave input.
mosi	O	1	Spi bus master output
sck	O	1	Spi bus clock signal
ss_n	O	1	Spi bus slave select signal

The SPI master supports only eight-bits transfer mode.

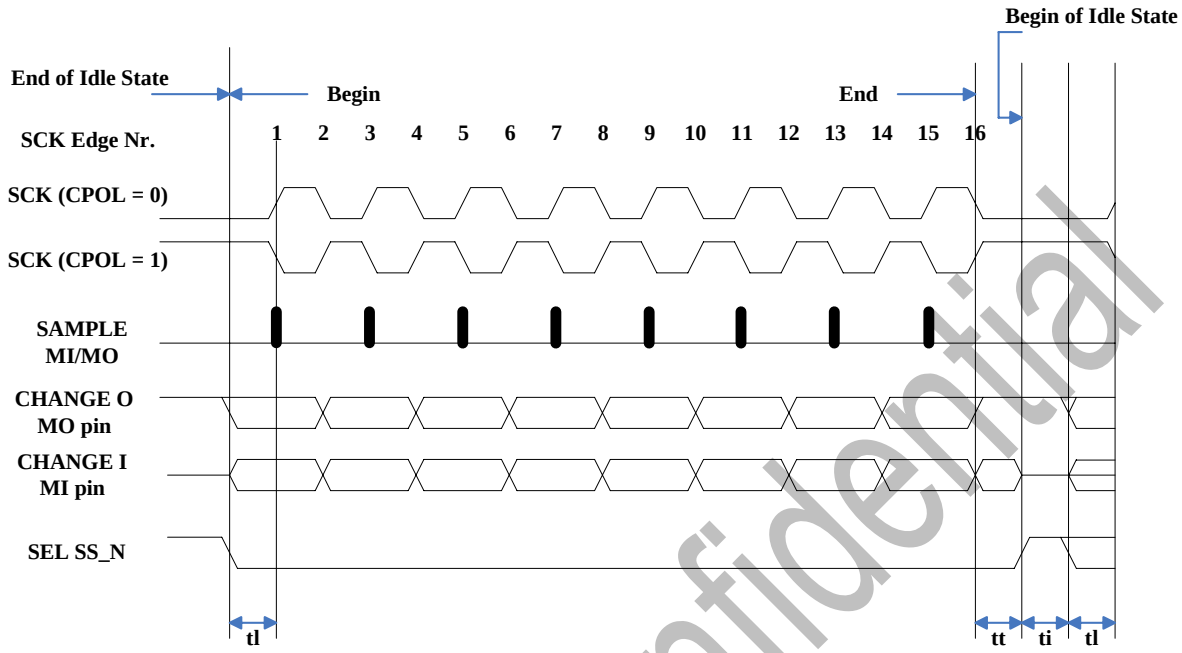

Figure 4-5 SPI Clock Format 0 (CPHA = 0)

tl = Minimum leading time before the first SCK edge
tt = Minimum trailing time after the last SCK edge
ti = minimum idling time between transfers (minimum SS_N high time)
tl, tt and ti are guaranteed for the master mode and required for the slave mode.

Figure 6-1 is a timing diagram of an SPI transfer where CPHA = 0. SCK waveforms are shown for CPOL = 0 and CPOL = 1. The SS pin must be either high or reconfigured as a general-purpose output not affecting the SPI.

The SS line is always deasserted and reasserted between successive transfers for at least minimum idle time.

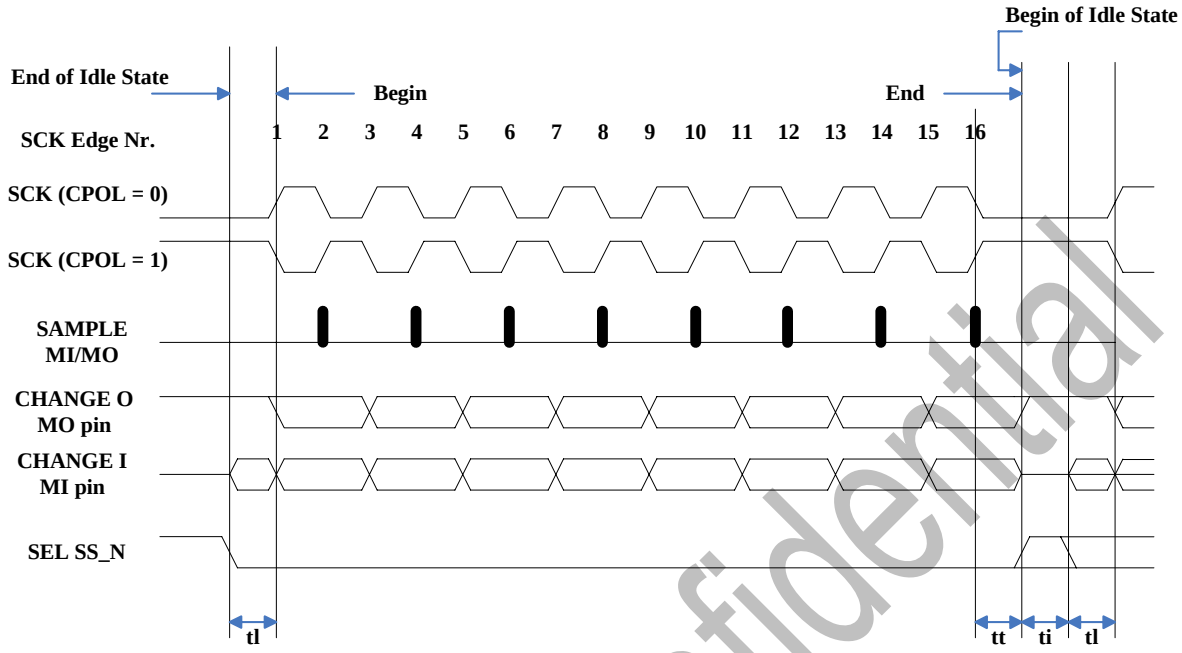

Figure 4-6 SPI Clock Format 1 (CPHA = 1)

tl = Minimum leading time before the first SCK edge
tt = Minimum trailing time after the last SCK edge
ti = minimum idling time between transfers (minimum SS_N high time)

Figure 6-2 shows two clocking variations for CPHA = 1. The SS pin must be either high or reconfigured as a general-purpose output not affecting the SPI.

4.4 I2C Interface

It is the standard I2C interface.

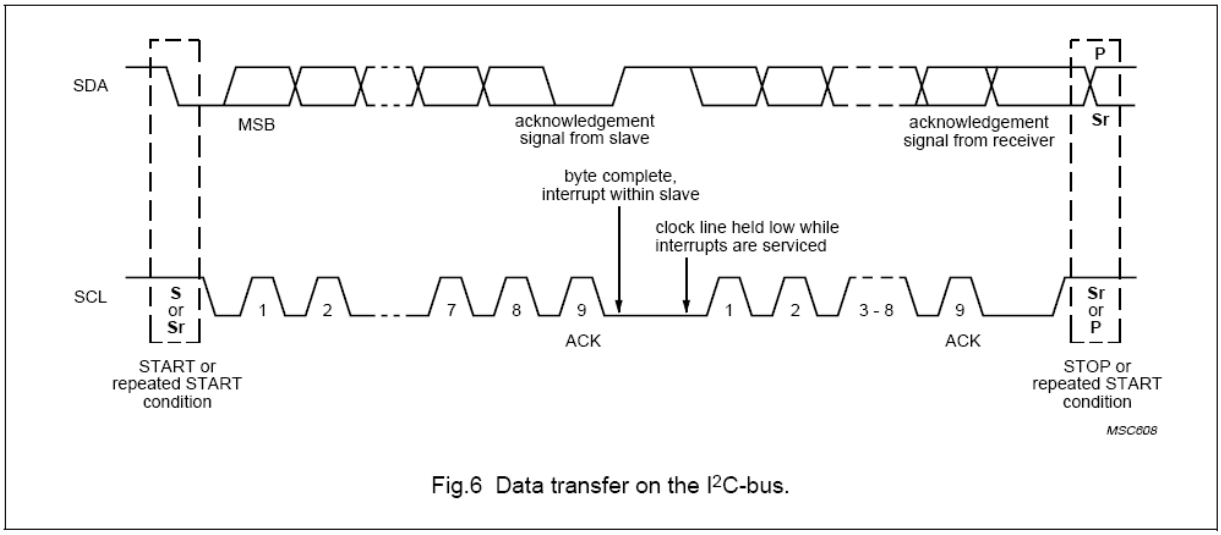

Fig.6 Data transfer on the I²C-bus.

Figure 4-7 I2C Interface

SDA means a serial data line.
SCL means a serial clock line.

5 RF Front End

The interface between TP3001B and RF tuners includes the following three types:
I/Q signals: TP3001B has a built in ADC, therefore, the RF tuner needs to output differential I/Q signals to TP3001B.
I2C control port: TP3001B needs to configure the tuner via this I2C port.
AGC: The TP3001B build in DAC outputs an analog signal to control the output signal strength of RF tuner.

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6 TP3001B Boot Sequence

TP3001B needs an external flash memory to store the boot image.

6.1 Boot Phases

Table 6-1. Boot Phases and Reset Combination

	Power up	Reset	Code download	Firmware initialize
Initial system power up	yes	yes	yes	yes
Chip reset		yes	yes	yes
System reset				yes

6.2 Power Up

The power up sequence of TP3001B is controlled by the external PMU. This part of sequence happens only once during the system power up.

6.3 Reset

The TP3001B reset sequence can be triggered by RESETn pin.

6.4 Code Download

After TP3001B is reset, MCU will run the bootloader in ROM to download firmware program to PRAM(32K bytes) through SPI interface, at the end of downloading, the bootloader program will change code page from ROM to PRAM and reset PC and other register to run the firmware.

This EEPROM to store firmware code is SPI interface EEPROM, now TP3001B uses SST25LF020A EEPROM, and other types of EEPROM are also supported.

6.5 Firmware Initialization

The TP3001 firmware structure is illustrated in Figure 6-1. Figure 6-1 states the working sequence of TP3001B.

After the chip is powered on and initialized, the firmware image will be downloaded to the TP3001B. In the working modes, TP3001B will be in one of the following states:

1. Receiving SDIO ctrl command, for example, get TS0 information, firmware processes SDIO ctrl command and goes back to idle state.
2. Receiving data, firmware will demux received data and send it through SDIO interface.
3. When TS0 is changed, firmware will demux new TS0 information and set new TS0 flag.

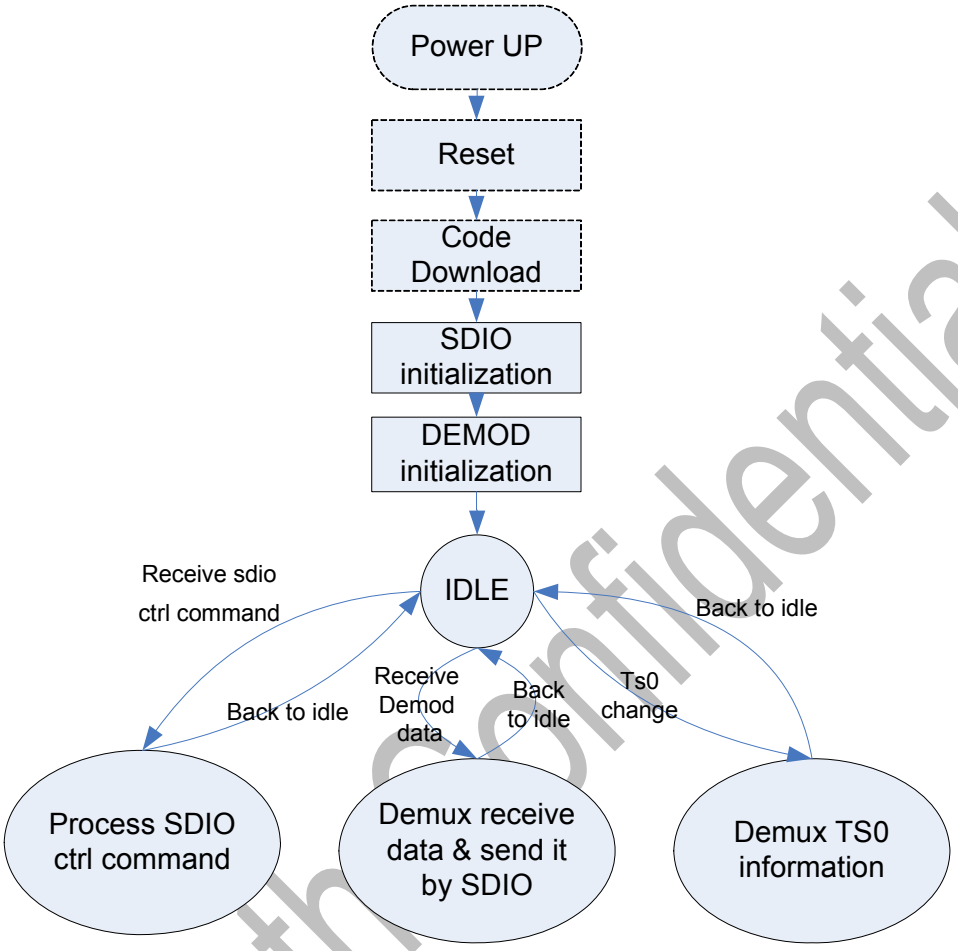

Figure 6-1 TP3001B Firmware Initialization

7 TP3001B Interface Drivers

7.1 Software Architecture

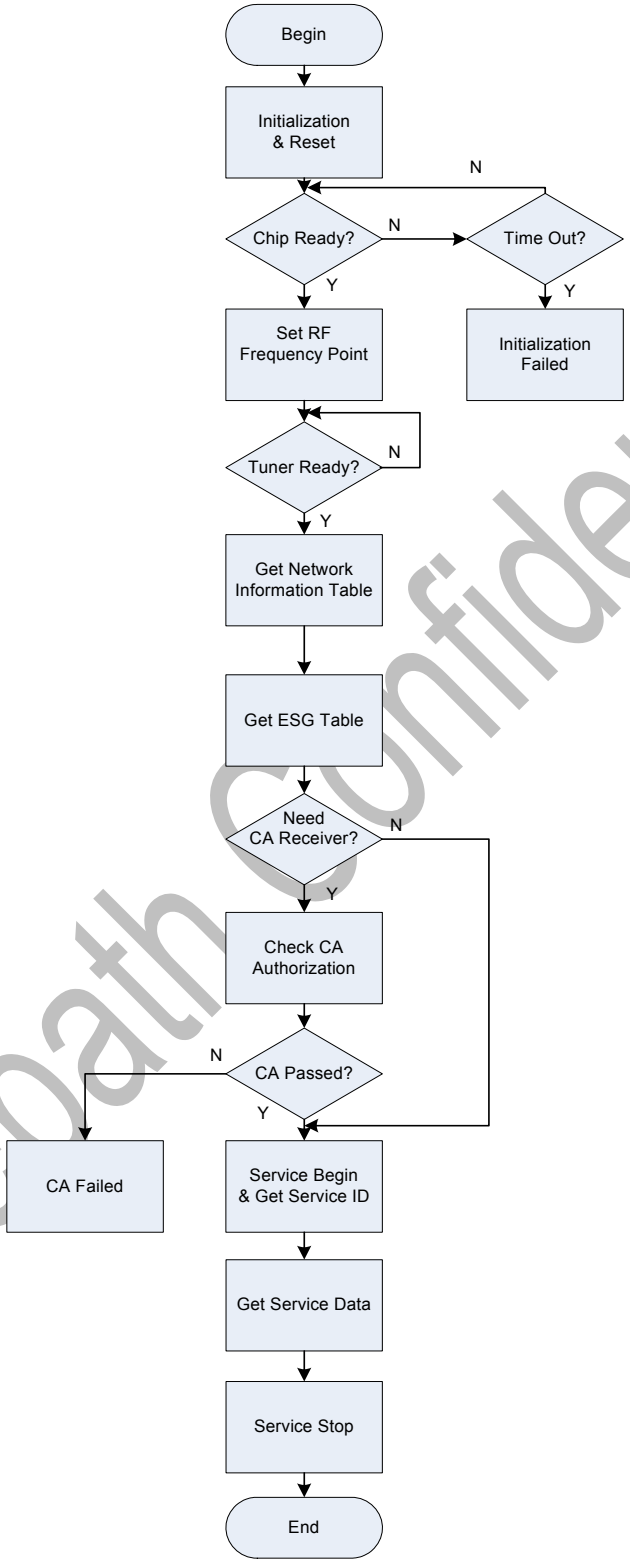

Figure 7-1 TP3001B Service Working Flow

7.2 SDIO Driver

When receiving data, TP3001B SDIO works at slave mode.

7.3 SPI Driver

When down loading code, SPI works at master mode.
When receiving data, SPI works at slave mode.

7.4 Application Functions

Table 7-1 TP3001B Customer Interface Functions

Function	Parameter	Return Value	Description
1. Init_Demodulator	**Frequency**	Null	Set the receiver frequency.
2. StartServiceID	**ServiceID**	Unsigned Integer 0x0000:failed 0x0001:success	Receive the service of one index, Index: 0x0000: control message 0x0001: ESG 0x0002: CA Others: invalid.
3. StopServiceID	**ServiceID**	Null	Stop the service of one index.
4. PauseServiceID	**ServiceID**	Null	Suspend the service of one index.
5. RestartServiceID	**ServiceID**	Null	Recover the service of one index.
6. GetTs0Contable	**ServiceID**	Null	Get the information of TS0, 0x00: reserved 0x01: NIT 0x02: CMCT 0x03: CSCT 0x04: SMCT 0x05: SSCT 0x06: ESG 0x0F-0x0F: reserved. 0x10: Emergency 0x11-0xFF: reserved.
7. Stop_ Demodulator	**Null**	Null	Stop the demodulator.
8. Get_Signal_State	**type**		Get the register map parameter.
9. Get_SPI_Data_Length	**null**	Unsigned integer	Get the spi data length.

10. Get_CPU_State	**Null**	CPUState	CPU State: 0x00: search 0x01: wait 0x02: demod 0x03: reserve
11. Is_Init_Demod_OK	**null**	Unsigned integer	0xBD is successful. Other values are invalid.

8 TP3001B Package Information

There are three statistic outputs in this EVB. Customers can evaluate the performance easily with these parameters.

8.1 Package Data

LFBGA81: Low-Profile Fine-Pitch Ball-Grid Array; 81 balls (ball diameter 0.4 mm; pitch 0.8 mm); body 8×8×1.3mm.

8.2 Package View

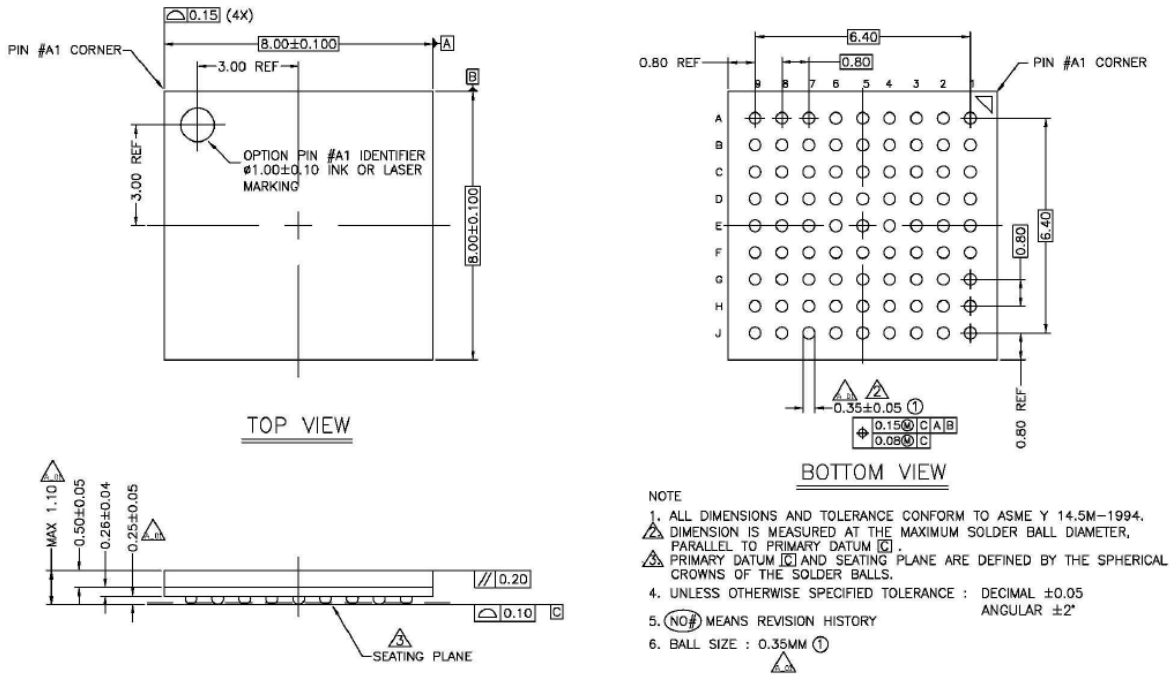

Figure 8-1 TP3001B Package View

8.3 BGA Land Grid Assignment

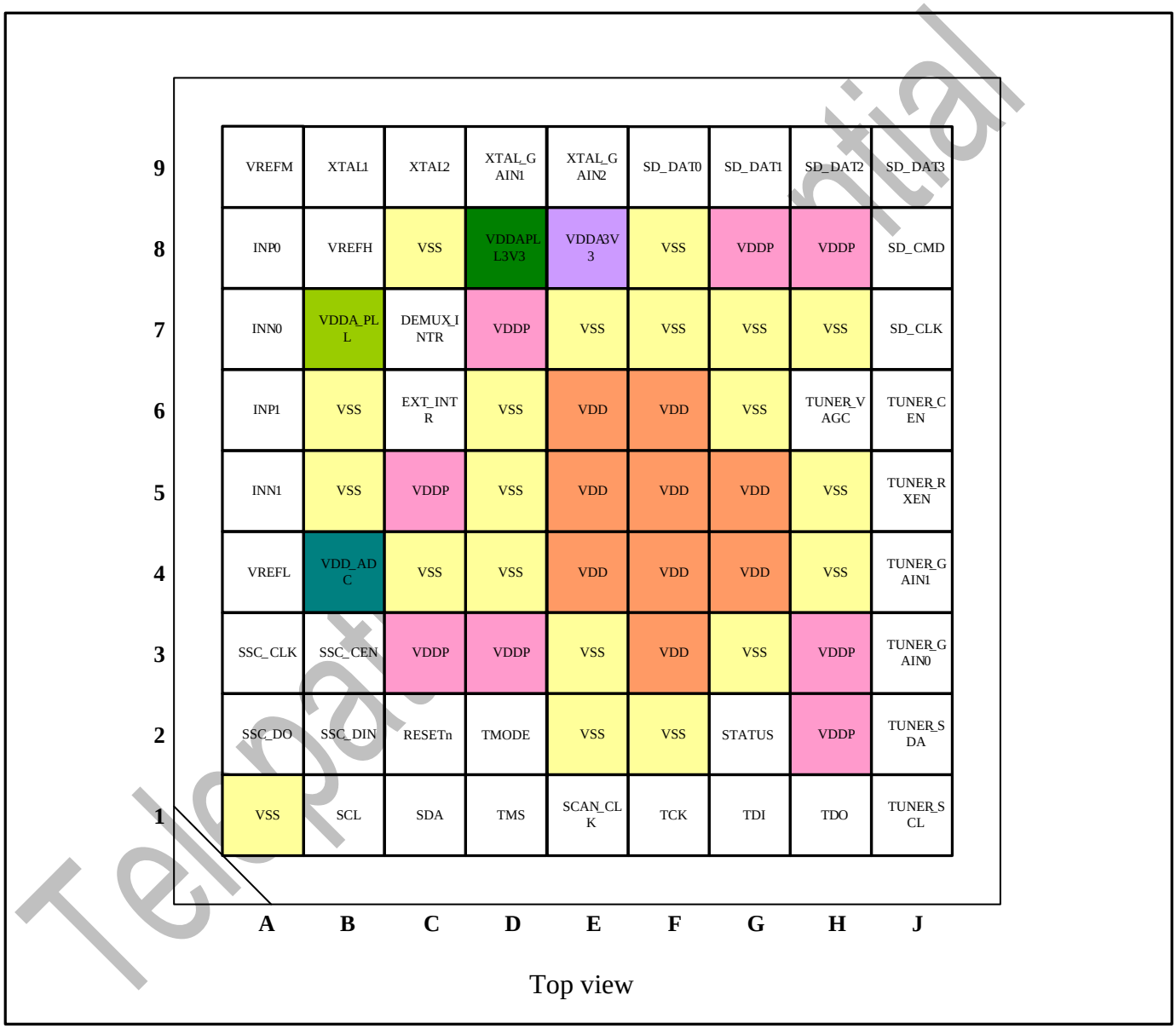

Figure 8-2 TP3001B BGA Ball Out

8.4 Pin-out Description

Pins description:

Table 8-1. Pin-out Description

Pin #	Name	Type	Functional Description
A1	VSS	–	Ground supply (0 V)
A2	SSC_DO	O	SSC/SPI data out
A3	SSC_CLK	O	SSC/SPI clock output
A4	VREFL	Analog	ADC reference voltage
A5	INN1	Analog	Q Channel negative differential input
A6	INP1	Analog	Q Channel positive differential input
A7	INN0	Analog	I Channel negative differential input
A8	INP0	Analog	I Channel positive differential input
A9	VREFM	Analog	ADC reference voltage
B1	SCL	I	I2C control interface clock
B2	SSC_DIN	O	SSC/SPI data in
B3	SSC_CEN	O	SSC/SPI chip enable
B4	VDD_ADC	–	Supply voltage for the pads (1.2V)
B5	VSS	–	Ground supply (0 V)
B6	VSS	–	Ground supply (0 V)
B7	VDDA_PLL	–	PLL 1.2V analog power supply
B8	VREFH	Analog	ADC reference voltage
B9	XTAL1	Analog	Crystal
C1	SDA	IO	I2C control interface data
C2	RESETn	I	System asynchronous reset
C3	VDDP	–	Power supply(3.3V)
C4	VSS	–	Ground supply (0 V)
C5	VDDP	–	Power supply(3.3V)
C6	EXT_INTR	I	External interrupt from multimedia chip
C7	DEMUX_INTR	O	Demux interrupt output to multimedia chip
C8	VSS	–	Ground supply (0 V)
C9	XTAL2	Analog	Crystal
D1	TMS	I	Test mode
D2	TMODE	I	Test mode enable
D3	VDDP	–	Power supply(3.3V)
D4	VSS	–	Ground supply (0 V)
D5	VSS	–	Ground supply (0 V)
D6	VSS	–	Ground supply (0 V)
D7	VDDP	–	Power supply(3.3V)
D8	VDDAPLL3V3		Oscillator power supply
D9	XTAL_GAIN1	Analog	Oscillator pad gain adjust, pull-up, default is “1”
E1	SCAN_CLK	I	Crystal frequency selection, “0” select 10MHz, “1” select 20MHz
E2	VSS	–	Ground supply (0 V)
E3	VSS	–	Ground supply (0 V)
E4	VDD	–	Core supply (1.2V)
E5	VDD	–	Core supply (1.2V)

Pin #	Name	Type	Functional Description
E6	VDD	–	Core supply (1.2V)
E7	VSS	–	Ground supply (0 V)
E8	VDDA3V3	–	DAC 3.3V power supply
E9	XTAL_GAIN2	Analog	Oscillator pad gain adjust, pull-down, default is “0”
F1	TCK	I	Test clock
F2	VSS	–	Ground supply (0 V)
F3	VDD	–	Core supply (1.2V)
F4	VDD	–	Core supply (1.2V)
F5	VDD	–	Core supply (1.2V)
F6	VDD	–	Core supply (1.2V)
F7	VSS	–	Ground supply (0 V)
F8	VSS	–	Ground supply (0 V)
F9	SD_DAT0	I/O	SDIO data 0
G1	TDI	I	Test data in
G2	STATUS	O	Receiver status indication
G3	VSS	–	Ground supply (0 V)
G4	VDD	–	Core supply (1.2V)
G5	VDD	–	Core supply (1.2V)
G6	VSS	–	Ground supply (0 V)
G7	VSS	–	Ground supply (0 V)
G8	VDDP	–	Power supply(3.3V)
G9	SD_DAT1	I/O	SDIO data 1
H1	TDO	O	Test data out
H2	VDDP	–	Power supply(3.3V)
H3	VDDP	–	Power supply(3.3V)
H4	VSS	–	Ground supply (0 V)
H5	VSS	–	Ground supply (0 V)
H6	TUNER_VAGC	Analog	Tuner baseband gain voltage
H7	VSS	–	Ground supply (0 V)
H8	VDDP	–	Power supply(3.3V)
H9	SD_DAT2	I/O	SDIO data 2
J1	TUNER_SCL	O	Tuner I2C interface bus clock
J2	TUNER_SDA	IO	Tuner I2C interface bus data
J3	TUNER_GAIN0	O	Tuner RF step gain
J4	TUNER_GAIN1	O	Tuner RF step gain
J5	TUNER_RXEN	O	Tuner reception enable (active mode)
J6	TUNER_CEN	O	Tuner chip enable (power up)
J7	SD_CLK	I	SDIO clock
J8	SD_CMD	I/O	SDIO command
J9	SD_DAT3	I/O	SDIO data 3

9 DC Characteristics

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9.1 Absolute Maximum Ratings

Table 9-1. Limiting Values

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
VDD	Core power supply	1.08	1.32	V
VDDA	Analog power supply	2.97	3.63	V
VDDP	Pad power supply	2.97	3.63	V
VI	DC input voltage	0	3.63	V
II	DC input current		20	mA
Tlead	Lead temperature (soldering 10sec)		260	℃
Tstg	Storage temperature	-65	150	℃
Tj	Junction temperature	-20	125	℃
T_{amb}	Ambient temperature	-20	85	℃

9.2 DC Characteristics and Operating Conditions

Table 9-2. Characteristics and Operating Conditions

SYMBOL	Parameter	Conditions	MIN.	TYP.	MAX.	UNIT
Core						
VDD	power supply for core	VDD=1.2±10%	1.08	1.2	1.32	V
Pads						
VDDP	power supply for normal Pads	VDDP=3.3±10%	2.97	3.3	3.63	V
DAC supply power						
VDDA3V3	power supply for DAC	VDDA3V3=3.3±10%	2.97	3.3	3.63	V
PLL supply power						
VDDAPLL3V3	power supply for PLL 3.3v analog part	VDDAPLL3V3=3.3±10%	2.97	3.3	3.63	V
VDDAPLL	power supply for PLL 1.2 analog part	VDDA_PLL=1.2±10%	1.08	1.2	1.32	V
ADC supply power						
VDD_ADC	power supply for ADC	VDD_ADC=1.2±10%	1.08	1.2	1.32	V
Tamb	ambient temperature		-20		85	°C
Vih	HIGH level input voltage		2			V
Voh	HIGH level output voltage		2.4			V
Vil	LOW level input voltage				0.8	V

Vol	LOW level output voltage				0.4	V
Ci	input capacitance			3.55		pF
Co	output capacitance			3.55		pF

10 Ordering Information

Release History

Date	Revision	Change
2008-01-10	0.4	

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