**BRIEF PRODUCT SPECIFICATION**

**nAD10110-18a**

**10-bit 110 MSPS Analog-to-Digital Converter IP**

**FEATURES**
- TSMC CL018G 1.8 V Technology
- 10-bit Pipeline ADC
- 5 to 110 MSPS Conversion Rate
- Excellent Dynamic Performance
  - 59 dBFS SNR at Fin = 10 MHz
  - 73 dBc SFDR at Fin = 10 MHz
- Dynamic Power Scaling
  - ~0.73 mW per MSPS
- Low Power Consumption
  - 80 mW at 110 MSPS
  - 20 mW at 25 MSPS
- Power Saving Idle Modes
- 0.77 mm² Core Area
- Internal Voltage Reference
- 1.5 V p-p Differential Input Swing

**APPLICATIONS**
- Communication Receive Channel
  - WLAN 802.11x / WiMAX 802.16x / DVB
- CMOS Imaging Sensors
- TV / Video / Radio Decoders
- Graphic Capture

**GENERAL DESCRIPTION**

The nAD10110-18a is a monolithic, high-speed, low power, analog-to-digital converter silicon IP. It uses a fully differential multistage pipeline architecture with digital error correction to provide 10-bit accuracy from 5 to 110 MSPS conversion speed. The core includes a sample-and-hold and an internal voltage reference that provides a nominal full-scale range of 1.5 V peak-to-peak. The IP is designed for high dynamic performance at input frequencies up to Nyquist and beyond. It thus represents an ideal solution for demanding applications like broadband communication, digital imaging and multimedia. The ADC consumes only 80 mW at 110 MSPS operation. Dynamic power scaling means that the power consumption scales linearly with approximately ~0.73 mW per MSPS. Combined with power saving idle modes the ADC is suitable for battery powered devices. Output data is available in a binary offset coded format. Three out-of-range indicator bits are also available for determining if the input signal is over-range, under-range or out-of-range.

Implemented in a generic 0.18 µm CMOS process, operating from a single 1.8 V supply and employing a fully differential architecture it represents an ideal ADC for highly integrated mixed-signal systems.

**QUICK REFERENCE DATA**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>1.6</td>
<td>1.8</td>
<td>2.0</td>
<td>V</td>
</tr>
<tr>
<td>Power Dissipation, at 110 MSPS</td>
<td>80</td>
<td>±0.3</td>
<td>±0.5</td>
<td>LSB</td>
</tr>
<tr>
<td>Differential Non Linearity</td>
<td></td>
<td>±0.4</td>
<td>±1.0</td>
<td>LSB</td>
</tr>
<tr>
<td>Integral Non Linearity</td>
<td>59</td>
<td></td>
<td></td>
<td>dBFS</td>
</tr>
<tr>
<td>Signal-to-Noise Ration, F_N = 10 MHz</td>
<td>73</td>
<td></td>
<td></td>
<td>dBC</td>
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<tr>
<td>Spurious-Free-Dynamic Range, F_N = 10 MHz</td>
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</table>

**Figure 1. Functional block diagram**

Table 1. nAD10110-18a quick reference data
ABOUT NORDIC SEMICONDUCTOR

Founded in 1983, Nordic Semiconductor ASA (OSE:NOD) is a Fabless Semiconductor specializing in short-range radio communication and high-speed data conversion. Nordic is head quartered in Trondheim, Norway.

MIXED SIGNAL IP OFFERINGS

Leading and emerging Fabless Semiconductor companies around the globe leverage Nordic’s portfolio of off-the-shelf mixed signal intellectual property for the design of highly integrated circuits for broadband communication, digital imaging and video.

Our IP portfolio includes medium resolution (8 to 12-bit), high-speed (40 MSPS+) data converters (ADC and DAC) and low jitter clock generation (PLL) implemented in the latest deep submicron CMOS technologies. Featuring low power consumption, low-silicon area, and a minimum of required external components and technology options our products offers cost efficient integration of high-performance data converters in cost sensitive, high volume integrated circuit designs.

DELIVERABLES

Our mixed signal intellectual property is delivered as technology specific hard macros. Upon licensing we provide a complete design-kit and documentation that enables efficient, low risk, design-in and integration. The design kit for our off-the-shelf IPs includes:

- Full datasheet
- Evaluation board and samples
- Silicon validation report
- Integration Guidelines
- Physical design database (flat gds2)
- LVS Netlist (spice compatible)
- Footprint (.lef format)
- HDL model (verilog model)
- Timing model (.lib)
- Design-in and integration support

FURTHER INFORMATION

For further information about this product, such as full datasheet, silicon validation report, availability and licensing terms please contact us at: datacon@nordicsemi.no