LTC2900
Programmable Quad Supply Monitor with Adjustable Reset Timer

FEATURES
- Simultaneously Monitors Four Supplies
- 16 User Selectable Combinations of 5V, 3.3V, 3V, 2.5V, 1.8V, 1.5V and/or ±Adjustable Voltage Thresholds
- Guaranteed Threshold Accuracy: ±1.5% of Monitored Voltage Over Temperature
- Low Supply Current: 43µA Typ
- Adjustable Reset Time
- Small MSOP and 3mm × 3mm DFN Packages
- Manual Reset Pin
- Open-Drain RST Output (LTC2900-1)
- Push-Pull RST Output (LTC2900-2)
- Power Supply Glitch Immunity
- Guaranteed RST for VCC ≥ 1V

APPLICATIONS
- Desktop and Notebook Computers
- Multivoltage Systems
- Telecom Equipment
- Portable Battery-Powered Equipment
- Network Servers

DESCRIPTION
The LTC®2900 is a programmable supply monitor for systems with up to four supply voltages. One of 16 preset or adjustable voltage monitor combinations can be selected using an external resistor divider connected to the program pin. The preset voltage thresholds are accurate to ±1.5% over temperature.

The reset delay time is adjustable using an external capacitor and the manual reset input may be used with a momentary switch to issue reset pulses with programmed duration. Tight voltage threshold accuracy and glitch immunity ensure reliable reset operation without false triggering. The RST output is guaranteed to be in the correct state for VCC down to 1V. The LTC2900-1 features an open-drain RST output, while the LTC2900-2 has a push-pull RST output.

The 43µA supply current makes the LTC2900 ideal for power conscious systems and it may be configured to monitor less than four inputs. The parts are available in the 10-lead MSOP and the 10-lead 3mm × 3mm DFN packages.

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TYPICAL APPLICATION
Quad Supply Monitor (5V, 3.3V, 2.5V, 1.8V)
LTC2900

**ABSOLUTE MAXIMUM RATINGS**  
(Notes 1, 2, 3)

V1, V2, V3, V4, VPG, PBR ..........................  –0.3V to 7V  
RST (LTC2900-1) ........................................ –0.3V to 7V  
RST (LTC2900-2) ........................................ –0.3V to (V2 + 0.3V)  
CRT ................................................  –0.3V to (VCC + 0.3V)  
VREF ................................................  –0.3V to (VCC + 0.3V)  
Reference Load Current (I\textsubscript{VREF}) .................................. ±1mA  
V4 Input Current (– ADJ Mode) ............................... –1mA  

**Operating Temperature Range**  
LTC2900-1C/LTC2900-2C .............................. 0°C to 70°C  
LTC2900-11/LTC2900-2I .............................. –40°C to 85°C  

**Storage Temperature Range**  
.............................. –65°C to 150°C  

**Lead Temperature (Soldering, 10 sec)**  
.............................. 300°C  

 Consult LTC Marketing for parts specified with wider operating temperature ranges.

**PACKAGE/ORDER INFORMATION**  

**ORDER PART NUMBER**  
LTC2900-1CMS  
LTC2900-2CMS  
LTC2900-1IMS  
LTC2900-2IMS  

**MS PACKAGE**  
10-LEAD PLASTIC MSOP  

**ORDER PART NUMBER**  
LTC2900-1DD  
LTC2900-2DD  
LTC2900-1ID  
LTC2900-2ID  

**DD PACKAGE**  
10-LEAD (3mm × 3mm) PLASTIC DFN  

Consult LTC Marketing for parts specified with wider operating temperature ranges.

**ELECTRICAL CHARACTERISTICS**  
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T\textsubscript{A} = 25°C. VCC = 5V, unless otherwise noted. (Note 3)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>V\textsubscript{RT50}</td>
<td>5V, 5% Reset Threshold</td>
<td>V1 Input Threshold</td>
<td>●</td>
<td>4.600</td>
<td>4.675</td>
<td>4.750</td>
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<tr>
<td>V\textsubscript{RT30}</td>
<td>3.3V, 5% Reset Threshold</td>
<td>V1, V2 Input Threshold</td>
<td>●</td>
<td>3.036</td>
<td>3.086</td>
<td>3.135</td>
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<td>V\textsubscript{RT25}</td>
<td>2.2V, 5% Reset Threshold</td>
<td>V2, V3 Input Threshold</td>
<td>●</td>
<td>2.760</td>
<td>2.805</td>
<td>2.850</td>
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<td>V\textsubscript{RT18}</td>
<td>1.8V, 5% Reset Threshold</td>
<td>V3, V4 Input Threshold</td>
<td>●</td>
<td>2.300</td>
<td>2.338</td>
<td>2.375</td>
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<td>V\textsubscript{RT15}</td>
<td>1.5V, 5% Reset Threshold</td>
<td>V3, V4 Input Threshold</td>
<td>●</td>
<td>1.656</td>
<td>1.683</td>
<td>1.710</td>
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<td>V\textsubscript{RTA}</td>
<td>ADJ Reset Threshold</td>
<td>V3, V4 Input Threshold</td>
<td>●</td>
<td>0.092</td>
<td>0.500</td>
<td>0.508</td>
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<td>V\textsubscript{RTAN}</td>
<td>–ADJ Reset Threshold</td>
<td>V4 Input Threshold</td>
<td>●</td>
<td>–1.8</td>
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<td>18</td>
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<tr>
<td>V\textsubscript{OC}</td>
<td>Minimum Internal Operating Voltage</td>
<td>RST in Correct Logic State, VCC Rising Prior to Program</td>
<td>●</td>
<td>1</td>
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<td>V\textsubscript{CCMINP}</td>
<td>Minimum Required for Programming</td>
<td>VCC Rising</td>
<td>●</td>
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<tr>
<td>V\textsubscript{REF}</td>
<td>Reference Voltage</td>
<td>VCC ≥ 2.3V, I\textsubscript{VREF} = ±1mA, C\textsubscript{REF} ≤ 1000pF</td>
<td>●</td>
<td>1.192</td>
<td>1.210</td>
<td>1.228</td>
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<td>V\textsubscript{PG}</td>
<td>Programming Voltage Range</td>
<td>VCC ≥ V\textsubscript{CCMINP}</td>
<td>●</td>
<td>0</td>
<td>V\textsubscript{REF}</td>
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<tr>
<td>I\textsubscript{VPG}</td>
<td>VPG Input Current</td>
<td>VPG = V\textsubscript{REF}</td>
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<td>±20</td>
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<tr>
<td>I\textsubscript{V1}</td>
<td>V1 Input Current</td>
<td>V1 = 5V, I\textsubscript{VREF} = 12μA, (Note 4)</td>
<td>●</td>
<td>43</td>
<td>75</td>
<td></td>
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**ELECTRICAL CHARACTERISTICS**  The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at \( T_A = 25^\circ \text{C} \). \( \text{V}_{\text{CC}} = 5\text{V} \), unless otherwise noted. (Note 3)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
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<th>UNITS</th>
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</thead>
<tbody>
<tr>
<td>( I_{V2} )</td>
<td>V2 Input Current</td>
<td>( V2 = 3.3\text{V} )</td>
<td>●</td>
<td>0.8</td>
<td>2</td>
<td>( \mu\text{A} )</td>
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<tr>
<td>( I_{V3} )</td>
<td>V3 Input Current</td>
<td>( V3 = 2.5\text{V} ) ( V3 = 0.55\text{V} ) (ADJ Mode)</td>
<td>●</td>
<td>–15</td>
<td>12</td>
<td>( \mu\text{A} )</td>
</tr>
<tr>
<td>( I_{V4} )</td>
<td>V4 Input Current</td>
<td>( V4 = 1.8\text{V} ) ( V4 = 0.55\text{V} ) (ADJ Mode) ( V4 = –0.05\text{V} ) (–ADJ Mode)</td>
<td>●</td>
<td>–15</td>
<td>8</td>
<td>( \mu\text{A} )</td>
</tr>
<tr>
<td>( I_{CRT(UP)} )</td>
<td>CRT Pull-Up Current</td>
<td>( \text{V}_{\text{CRT}} = 0\text{V} )</td>
<td>●</td>
<td>–1.4</td>
<td>–2</td>
<td>–2.6</td>
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<tr>
<td>( I_{CRT(DN)} )</td>
<td>CRT Pull-Down Current</td>
<td>( \text{V}_{\text{CRT}} = 1.3\text{V} )</td>
<td>●</td>
<td>10</td>
<td>20</td>
<td>30</td>
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<tr>
<td>( t_{RST} )</td>
<td>Reset Time-Out Period</td>
<td>( \text{C}_{\text{RT}} = 1500\text{pF} )</td>
<td>●</td>
<td>5</td>
<td>7</td>
<td>9</td>
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<tr>
<td>( t_{UV} )</td>
<td>Vx Undervoltage Detect to RST</td>
<td>( \text{VX} ) Less Than Reset Threshold ( \text{V}_{\text{RTX}} ) by More Than 1%</td>
<td>●</td>
<td>150</td>
<td></td>
<td>( \mu\text{s} )</td>
</tr>
<tr>
<td>( V_{OL} )</td>
<td>Output Voltage Low RST</td>
<td>( I_{\text{SINK}} = 2.5\text{mA} ); ( \text{V1} = 3\text{V} ); ( \text{V2} = 3\text{V} ); ( \text{V3}, \text{V4} = 0\text{V} ); ( \text{VPG} = 0\text{V} )</td>
<td>●</td>
<td>0.15</td>
<td>0.4</td>
<td>( \text{V} )</td>
</tr>
<tr>
<td>( V_{OL} )</td>
<td>Output Voltage Low RST (LTC2900-1) (Note 5)</td>
<td>( I_{\text{SINK}} = 100\mu\text{A} ); ( \text{V2} = 1\text{V} ); ( \text{V1}, \text{V3}, \text{V4} = 0\text{V} )</td>
<td>●</td>
<td>0.05</td>
<td>0.3</td>
<td>( \text{V} )</td>
</tr>
<tr>
<td>( V_{OH} )</td>
<td>Output Voltage High RST (LTC2900-2) (Note 6)</td>
<td>( I_{\text{SOURCE}} = 200\mu\text{A} )</td>
<td>●</td>
<td>0.8 • ( \text{V2} )</td>
<td></td>
<td>( \text{V} )</td>
</tr>
</tbody>
</table>

**Manual Reset Pin**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IH} )</td>
<td>PBR Input Threshold High</td>
<td>( \text{V}_{\text{CC}} = 3.3\text{V} ) to 5.5V</td>
<td>●</td>
<td>1.6</td>
<td></td>
<td>( \text{V} )</td>
</tr>
<tr>
<td>( V_{IL} )</td>
<td>PBR Input Threshold Low</td>
<td>( \text{V}_{\text{CC}} = 3.3\text{V} ) to 5.5V</td>
<td>●</td>
<td>0.4</td>
<td></td>
<td>( \text{V} )</td>
</tr>
<tr>
<td>( t_{PBW} )</td>
<td>PBR Input Pulse Width</td>
<td>( \text{V}_{\text{CC}} = 3.3\text{V} )</td>
<td>●</td>
<td>150</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{PBD} )</td>
<td>Manual Reset Propagation Delay</td>
<td>( \text{V}<em>{\text{CC}} = 3.3\text{V} ); ( \text{V}</em>{\text{PBR}} ) Falling</td>
<td>●</td>
<td>0.1</td>
<td>1</td>
<td>( \mu\text{s} )</td>
</tr>
<tr>
<td>( I_{PBR} )</td>
<td>PBR Pull-Up Current</td>
<td>( \text{V}_{\text{PBR}} = 0\text{V} )</td>
<td>●</td>
<td>–10</td>
<td></td>
<td>( \mu\text{A} )</td>
</tr>
</tbody>
</table>

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** All currents into pins are positive, all voltages are referenced to GND unless otherwise noted.

**Note 3:** The greater of \( \text{V1}, \text{V2} \) is the internal supply voltage \( \text{V}_{\text{CC}} \).

**Note 4:** Under static no-fault conditions, \( \text{V1} \) will necessarily supply quiescent current. If at any time \( \text{V2} \) is larger than \( \text{V1} \), \( \text{V2} \) must be capable of supplying the quiescent current, programming (transient) current and reference load current.

**Note 5:** The RST output pin on the LTC2900-1 has an internal pull-up to \( \text{V2} \) of typically 6\( \mu\text{A} \). However, an external pull-up resistor may be used when faster rise times are required or for \( \text{V}_{\text{OH}} \) voltages greater than \( \text{V2} \).

**Note 6:** The push-pull RST output pin on the LTC2900-2 is actively pulled up to \( \text{V2} \).

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**TEST CIRCUITS**

- **Figure 1. RST \( V_{OH} \) Test**
- **Figure 2. RST \( V_{OL} \) Test**
- **Figure 3. Active Pull-Up RST \( V_{OH} \) Test**
TYPICAL PERFORMANCE CHARACTERISTICS

5V Threshold Voltage vs Temperature

3.3V Threshold Voltage vs Temperature

3V Threshold Voltage vs Temperature

2.5V Threshold Voltage vs Temperature

1.8V Threshold Voltage vs Temperature

1.5V Threshold Voltage vs Temperature
**TYPICAL PERFORMANCE CHARACTERISTICS**

### ADJ Threshold Voltage vs Temperature

- **Threshold Voltage, VRTA (V)**
  - 0.508
  - 0.506
  - 0.504
  - 0.502
  - 0.500
  - 0.498
  - 0.496
  - 0.494

- **Temperature (°C)**
  - –40
  - –20
  - 0
  - 20
  - 40
  - 60

### –ADJ Threshold Voltage vs Temperature

- **Threshold Voltage, VRTAN (V)**
  - 0.018
  - 0.012
  - 0.006
  - 0
  - –0.006
  - –0.012
  - –0.018

- **Temperature (°C)**
  - –40
  - –20
  - 0
  - 20
  - 40
  - 60

### VREF vs Temperature

- **VREF (V)**
  - 1.228
  - 1.222
  - 1.216
  - 1.210
  - 1.204
  - 1.198
  - 1.192

- **Temperature (°C)**
  - –40
  - –20
  - 0
  - 20
  - 40
  - 60

### Currents vs Temperature

- **IV1 vs Temperature**
  - V1 = 5V
  - V2 = 3.3V
  - V3 = 2.5V
  - V4 = 1.8V

- **IV2 vs Temperature**
  - V1 = 5V
  - V2 = 3.3V
  - V3 = 2.5V
  - V4 = 1.8V

- **IV3 vs Temperature**
  - V1 = 5V
  - V2 = 3.3V
  - V3 = 2.5V
  - V4 = 1.8V

### Typical Transient Duration vs Comparator Overdrive (V1, V2)

- **Typical Transient Duration (µs)**
  - 0
  - 50
  - 100
  - 150
  - 200
  - 250
  - 300
  - 350
  - 400

- **Comparator Overdrive Voltage (% of VRTX)**
  - 0.1

- **Temperature (°C)**
  - –40
  - –20
  - 0
  - 20
  - 40

### Typical Transient Duration vs Comparator Overdrive (V3, V4)

- **Typical Transient Duration (µs)**
  - 0
  - 50
  - 100
  - 150
  - 200
  - 250
  - 300
  - 350
  - 400

- **Comparator Overdrive Voltage (% of VRTX)**
  - 0.1
**PIN FUNCTIONS**

**V3 (Pin 1):** Voltage Input 3. Select from 2.5V, 1.8V, 1.5V or ADJ. See Table 1 for details.

**V1 (Pin 2):** Voltage Input 1. Select from 5V or 3.3V. See Table 1 for details. The greater of (V1, V2) is also V_{CC} for the device. Bypass this pin to ground with a 0.1\mu F (or greater) capacitor.

**CRT (Pin 3):** Reset Delay Time Programming Pin. Attach an external capacitor (C_T) to GND to set a reset delay time of 4.6ms/nF. Leaving the pin open generates a minimum delay of approximately 50\mu s. A 47nF capacitor will generate a 216ms reset delay time.

**RST (Pin 4):** Reset Logic Output. Active low with weak pull-up to V2 (LTC2900-1) or active pull-up to V2 (LTC2900-2). Pulls low when any voltage input is below the reset threshold and held low for the programmed delay time after all voltage inputs are above threshold. May be pulled above V2 using an external pull-up (LTC2900-1 only).

**PBR (Pin 5):** Manual Reset Pin. Attach a push-button switch between this pin and ground. A logic low on this pin will pull RST low. When the PBR pin returns high, RST will return high after the programmed reset delay assuming all four voltage inputs are above threshold. A weak internal pull-up allows the pin to be left floating for normal monitor operation. When using a switch, the switch is debounced through the reset circuitry using the delay provided by the C_T timing capacitor.

**GND (Pin 6):** Ground.

**VPG (Pin 7):** Voltage Threshold Combination Select Input. Connect to an external 1% resistive divider between V_{REF} and GND to select 1 of 16 combinations of preset and/or ±adjustable voltage thresholds (see Table 1). Do not add capacitance on the VPG pin.

**VREF (Pin 8):** Buffered Reference Voltage. A 1.210V nominal reference used for the programming voltage (VPG) and for the offset of negative adjustable applications. The buffered reference can source and sink up to 1mA. The reference can drive a bypass capacitor of up to 1000pF without oscillation.

**V4 (Pin 9):** Voltage Input 4. Select from 1.8V, 1.5V, ADJ or –ADJ. See Table 1 for details.

**V2 (Pin 10):** Voltage Input 2. Select from 3.3V, 3V or 2.5V. See Table 1 for details. The greater of (V1, V2) is also V_{CC} for the device. Bypass this pin to ground with a 0.1\mu F (or greater) capacitor. RST is weakly pulled up to V2 (LTC2900-1). RST is actively pulled up to V2 in the LTC2900-2.
Power-Up

The greater of V1, V2 is the internal supply voltage (VCC). On power-up, VCC will power the drive circuits for the RST pin. This ensures that the RST output will be low as soon as V1 or V2 reaches 1V. The RST output will remain low until the part is programmed. After programming, if any one of the VX inputs is below its programmed threshold, RST will be a logic low. Once all the VX inputs rise above their thresholds, an internal timer is started and RST is released after the programmed delay time. If VCC < (V3 – 1) and VCC < 2.4V, the V3 input impedance will be low (1kΩ typ).

Monitor Programming

The LTC2900 input voltage combination is selected by placing the recommended resistive divider from VREF to GND and connecting the tap point to VPG, as shown in Figure 4. Table 1 offers recommended 1% resistor values for the various modes. The last column in Table 1 specifies optimum VPG/VREF ratios (±0.01) to be used when programming with a ratiometric DAC.

During power-up, once V1 or V2 reaches 2.4V max, the monitor enters a programming period of approximately 150µs during which the voltage on the VPG pin is sampled and the monitor is configured to the desired input combination. Do not add capacitance to the VPG pin. Immediately after programming, the comparators are enabled and supply monitoring will begin.

Table 1. Voltage Threshold Programming

<table>
<thead>
<tr>
<th>MODE</th>
<th>V1 (V)</th>
<th>V2 (V)</th>
<th>V3 (V)</th>
<th>V4 (V)</th>
<th>R1 (kΩ)</th>
<th>R2 (kΩ)</th>
<th>VPG</th>
<th>VREF</th>
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<tbody>
<tr>
<td>0</td>
<td>5.0</td>
<td>3.3</td>
<td>ADJ</td>
<td>ADJ</td>
<td>Open</td>
<td>Short</td>
<td>0.00</td>
<td>0.00</td>
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<tr>
<td>1</td>
<td>5.0</td>
<td>3.3</td>
<td>ADJ</td>
<td>–ADJ</td>
<td>93.1</td>
<td>9.53</td>
<td>0.09</td>
<td>0.00</td>
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<td>3.3</td>
<td>2.5</td>
<td>ADJ</td>
<td>ADJ</td>
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<td>2.5</td>
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Supply Monitoring

The LTC2900 is a low power, high accuracy programmable quad supply monitoring circuit with a common reset output and a manual reset input. Reset timing is adjustable using an external capacitor. Single pin programming selects 1 of 16 input voltage monitor combinations. All four voltage inputs must be above predetermined thresholds for the reset not to be invoked. The LTC2900 will assert the reset output during power-up, power-down and brownout conditions on any one of the voltage inputs. The inverting inputs on the V3 and/or V4 comparators are set to 0.5V when the positive adjustable modes are selected (Figure 5). The tap point on an external resistive divider, connected between the positive voltage being
sensed and ground, is connected to the high impedance noninverting inputs (V3, V4). The trip voltage is calculated from:

\[ V_{\text{TRIP}} = 0.5V \left( 1 + \frac{R3}{R4} \right) \]

In the negative adjustable mode, the noninverting input on the V4 comparator is connected to ground (Figure 6). The tap point on an external resistive divider, connected between the negative voltage being sensed and the VREF pin, is connected to the high impedance inverting input (V4). VREF provides the necessary level shift required to operate at ground. The trip voltage is calculated from:

\[ V_{\text{TRIP}} = -V_{\text{REF}} \left( \frac{R3}{R4} \right) \], \quad V_{\text{REF}} = 1.210V \text{ Nominal} \]

In a negative adjustable application, the minimum value for R4 is limited by the sourcing capability of VREF (±1mA). With no other load on VREF, R4 (minimum) is:

\[ 1.21V \div 1mA = 1.21k\Omega \]

Tables 2 and 3 offer suggested 1% resistor values for various adjustable applications.

| Table 2. Suggested 1% Resistor Values for the ADJ Inputs |
|-------------|-------------|-------------|-------------|
| V\text{SUPPLY} (V) | V\text{TRIP} (V) | R3 (k\Omega) | R4 (k\Omega) |
| 12          | 11.25       | 2150        | 100         |
| 10          | 9.4         | 1780        | 100         |
| 8           | 7.5         | 1400        | 100         |
| 7.5         | 7           | 1300        | 100         |
| 6           | 5.6         | 1020        | 100         |
| 5           | 4.725       | 845         | 100         |
| 3.3         | 3.055       | 511         | 100         |
| 3           | 2.82        | 464         | 100         |
| 2.5         | 2.325       | 365         | 100         |
| 1.8         | 1.685       | 237         | 100         |
| 1.5         | 1.410       | 182         | 100         |
| 1.2         | 1.120       | 124         | 100         |
| 1           | 0.933       | 86.6        | 100         |
| 0.9         | 0.840       | 68.1        | 100         |

| Table 3. Suggested 1% Resistor Values for the –ADJ Input |
|-------------|-------------|-------------|-------------|
| V\text{SUPPLY} (V) | V\text{TRIP} (V) | R3 (k\Omega) | R4 (k\Omega) |
| –2          | –1.87       | 187         | 121         |
| –5          | –4.64       | 464         | 121         |
| –5.2        | –4.87       | 487         | 121         |
| –10         | –9.31       | 931         | 121         |
| –12         | –11.30      | 1130        | 121         |
APPLICATIONS INFORMATION

Although all four supply monitor comparators have built-in glitch immunity, bypass capacitors on V1 and V2 are recommended because the greater of V1 or V2 is also the VCC for the device. Filter capacitors on the V3 and V4 inputs are allowed.

Power-Down

On power-down, once any of the VX inputs drop below their threshold, RST is held at a logic low. A logic low of 0.4V is guaranteed until both V1 and V2 drop below 1V. If the bandgap reference becomes invalid (VCC < 2V typ), the part will reprogram once VCC rises above 2.4V max.

Monitor Output Rise and Fall Time Estimation

The RST output has strong pull-down capability. If the external load capacitance (CLOAD) is known, output fall time (10% to 90%) is estimated using:

\[ t_{\text{FALL}} = 2.2 \times R_{\text{PD}} \times C_{\text{LOAD}} \]

where \( R_{\text{PD}} \) is the on-resistance of the internal pull-down transistor. The typical performance curve (\( V_{\text{OL}} \) vs \( I_{\text{SINK}} \)) demonstrates that the pull-down current is somewhat linear versus output voltage. Using the 25°C curve, \( R_{\text{PD}} \) is estimated to be approximately 40Ω. Assuming a 150pF load capacitance, the fall time is about 13.2ns.

Although the RST output of the LTC2900-1 is considered to be “open-drain,” it does have weak pull-up capability (see RST Pull-Up Current vs V2 curve). Output rise time (10% to 90%) is estimated using:

\[ t_{\text{RISE}} = 2.2 \times R_{\text{PU}} \times C_{\text{LOAD}} \]

where \( R_{\text{PU}} \) is the on-resistance of the pull-up transistor. The on-resistance as a function of the V2 voltage at room temperature is estimated using:

\[ R_{\text{PU}} = \frac{6 \times 10^5}{V_2 - 1} \Omega \]

with \( V_2 = 3.3V \), \( R_{\text{PU}} \) is about 260k. Using 150pF for load capacitance, the rise time is 86μs. If the output needs to pull up faster and/or to a higher voltage, a smaller external pull-up resistor may be used. Using a 10k pull-up resistor, the rise time is reduced to 3.3μs for a 150pF load capacitance.

The LTC2900-2 has an active pull-up to V2 on the RST output. The typical performance curve (RST Pull-Up Current vs V2 curve) demonstrates that the pull-up current is somewhat linear versus the V2 voltage and \( R_{\text{PU}} \) is estimated to be approximately 625Ω. A 150pF load capacitance makes the rise time about 206ns.

Selecting the Reset Timing Capacitor

The reset time-out period is adjustable in order to accommodate a variety of microprocessor applications. The reset time-out period, \( t_{\text{RST}} \), is adjusted by connecting a capacitor, \( C_{\text{RT}} \), between the CRT pin and ground. The value of this capacitor is determined by:

\[ C_{\text{RT}} = t_{\text{RST}} \times 217 \times 10^{-9} \]

with \( C_{\text{RT}} \) in Farads and \( t_{\text{RST}} \) in seconds. The \( C_{\text{RT}} \) value per millisecond of delay can also be expressed as \( C_{\text{RT}}/\text{ms} = 217 \) (pF/ms).

Leaving the CRT pin unconnected will generate a minimum reset time-out of approximately 50μs. The reset time-out period is limited by the largest available low leakage capacitor. The accuracy of the time-out period will be affected by capacitor leakage (the nominal charging current is 2μA) and capacitor tolerance. A low leakage ceramic capacitor is recommended.
### APPLICATIONS INFORMATION

**Ensuring Reset Valid for \( V_{CC} \) Down to 0V (LTC2900-2)**

Some applications require the reset output (RST) to be valid with \( V_{CC} \) down to 0V. The LTC2900-2 is designed to handle this requirement with the addition of an external resistor from RST to ground. The resistor will provide a path for stray charge and/or leakage currents, preventing the RST output from floating to undetermined voltages when connected to high impedance (such as CMOS logic inputs). The resistor value should be small enough to provide effective pull-down without excessively loading the active pull-up circuitry. Too large a value may not pull down well enough. A 100k resistor from RST to ground is satisfactory for most applications.

### TYPICAL APPLICATIONS

#### Quad Supply Monitor with Push-Button Reset

5V, 3V, 1.8V, 12V (ADJ)

![Quad Supply Monitor with Push-Button Reset](Image)

#### 5V, –5V Monitor and Unused V2, V3 Inputs

Pulled Above Trip Thresholds

![5V, –5V Monitor and Unused V2, V3 Inputs](Image)
TYPICAL APPLICATIONS

5V, 3.3V, 12V, –5.2V Monitor with Manual Reset and LED Indication on RST

Low Voltage Quad Supply Monitor 3.3V, 2.5V, 1V (ADJ), 0.9V (ADJ)
PACKAGE DESCRIPTION

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699)

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF WEED-2.
   CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
4. EXPOSED PAD SHALL BE SOLDER PLATED
5. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

TOP VIEW—EXPOSED PAD

BOTTOM VIEW—EXPOSED PAD
PACKAGE DESCRIPTION

MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661)

RECOMMENDED SOLDER PAD LAYOUT

NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.
Monitor Eight Supplies Using Supervisory Cascade

12V (ADJ), 5V, 3.3V, 3.3V, 2.5V, 1.8V (ADJ), 1V (ADJ), –5V (–ADJ)

Related Parts

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<th>DESCRIPTION</th>
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<td>5V Supply Monitor, Watchdog Timer and Battery Backup</td>
<td>4.65V Threshold</td>
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<tr>
<td>LTC694-3.3</td>
<td>3.3V Supply Monitor, Watchdog Timer and Battery Backup</td>
<td>2.9V Threshold</td>
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<td>LTC699</td>
<td>5V Supply Monitor and Watchdog Timer</td>
<td>4.65V Threshold</td>
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<td>LTC1326</td>
<td>Micropower Precision Triple Supply Monitor for 5V, 3.3V and ADJ</td>
<td>4.725V, 3.118V, 1V Thresholds (±0.75%)</td>
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<td>Precision Triple Supply Monitor for PCI Applications</td>
<td>Meets PCI tFAIL Timing Specifications</td>
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<td>Individual Monitor Outputs in MSOP</td>
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