SDP Biased Series - 5x6 QFN

Description
This new SDP Biased series provides overvoltage protection for applications such as VDSL2, ADSL2, and ADSL2+ with minimal effect on data signals. This latest silicon design innovation results in a capacitive loading characteristic that is compatible with these high bandwidth applications. This surface mount QFN package provides a surge capability that exceeds most worldwide standards and recommendations for lightning surge withstand capability of secondary protectors.

Features & Benefits
- Compatible with VDSL2 (30MHz)
- Balanced overvoltage protection
- Low distortion
- Low insertion loss
- Low profile
- SO-8 footprint compatible
- Fails short circuit when surged in excess of ratings
- 2nd level interconnect is Pb-free per IPC/JEDEC J-STD-609A.01

Applicable Global Standards
- TIA-968-A
- TIA-968-B
- ITU K.20/21 Enhanced Level
- ITU K.20/21 Basic Level
- IEC 61000-4-5
- GR 1089 Inter-building
- GR 1089 Intra-building
- YD/T 1082
- YD/T 993
- YD/T 950

Agency Approvals

<table>
<thead>
<tr>
<th>Agency</th>
<th>Agency File Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>UL</td>
<td>E133083</td>
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</tbody>
</table>

Pinout Designation

- Tip in: 1 8 Tip out: 2 7
- Bias: 3 6
- Ground: 4 5
- Ring in: 4 5 Ring out: 3 6

Schematic Symbol

- Line In (1)
- Bias (2)
- Ground (3)
- Line Out (8)
- Line Out (5)
- Bias (6)
- Ground (7)

Electrical Characteristics

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Marking</th>
<th>( V_{DRM} @ I_{HM} = 5 \mu A )</th>
<th>( V_{s} @ 100V/\mu s )</th>
<th>( I_{L} )</th>
<th>( I_{P} )</th>
<th>( V_{r} @ I_{R} = 2.2 ) Amps</th>
<th>Capacitance</th>
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<tbody>
<tr>
<td></td>
<td></td>
<td>( V_{min} )</td>
<td>( V_{max} )</td>
<td>mA ( )</td>
<td>mA ( max )</td>
<td>A max</td>
<td>( V_{max} )</td>
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<tr>
<td>SDP0080Q38CB</td>
<td>SDP-8C</td>
<td>6</td>
<td>25</td>
<td>50</td>
<td>800</td>
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<td>SDP0220Q38CB</td>
<td>SDP02C</td>
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<td>SDP13C</td>
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<td>SDP1800Q38CB</td>
<td>SDP18C</td>
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<td>SDP2600Q38CB</td>
<td>SDP26C</td>
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<td>SDP3100Q38CB</td>
<td>SDP31C</td>
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<td>SDP3500Q38CB</td>
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<td>400</td>
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<td>800</td>
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<td>8</td>
</tr>
</tbody>
</table>

Notes:
- Absolute maximum ratings measured at \( T_{A} = 25^\circ C \) (unless otherwise noted).
- Devices are bi-directional (unless otherwise noted).
- Part with * is under development.

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**V-I Characteristics**

- **Parameter Name**: Test Conditions
- **Value**: Units
- **I_{DSM}**: Maximum non-repetitive on-state current, 50/60Hz
  - 0.5s: 6.5 A
  - 1s: 4.6 A
  - 2s: 3.4 A
  - 5s: 2.3 A
  - 30s: 1.3 A
  - 900s: 0.73 A

**Capacitance vs. Voltage**

- **Parameter Name**: Test Conditions
- **Value**: Units
- **Line Voltage (V)**
  - 0V
  - 3.3V
  - 5V
  - 12V
  - 24V
  - 30V
  - 50V

**Notes:**

- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C.
- The device must initially be in thermal equilibrium with -40°C < T_{J} < +150°C.

**Surge Ratings**

- **Series**: 2x10µs, 1.2x50µs/8x20µs, 10x700/5x310µs, 10x1000µs, 600V_{RMS}, 1 cycle
- **I_{TPP}**: A min
- **I_{TSAM}**: A min

**Thermal Considerations**

- **Package**: 5x6 QFN
- **Symbol**: T_{J}
- **Parameter**: Junction Temperature
- **Value**: -40 to +150 °C
- **Symbol**: T_{STG}
- **Parameter**: Storage Temperature Range
- **Value**: -40 to +150 °C
- **Symbol**: R_{JA}
- **Parameter**: Thermal Resistance: Junction to Ambient
- **Value**: 100 °C/W

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SIDACtor® Protection Thyristors
Broadband Optimized™ Protection

**Normalized V_s Change vs. Junction Temperature**

- **Normalized DC Holding Current vs. Case Temperature**

**Soldering Parameters**

- **Reflow Condition**: Pb-Free assembly (see Fig. 1)
- **Pre Heat**:
  - Temperature Min ($T_{s(min)}$) +150°C
  - Temperature Max ($T_{s(max)}$) +200°C
  - Time (Min to Max) ($t_s$) 60-180 secs.
- **Average ramp up rate (Liquidus Temp ($T_l$) to peak)** 3°C/sec. Max.
- **$T_{s(max)}$ to $T_l$ - Ramp-up Rate**: 3°C/sec. Max.
- **Reflow**:
  - Temperature ($T_l$) (Liquidus) +217°C
  - Temperature ($t_l$) 60-150 secs.
- **Peak Temp ($T_p$)** +260(±0/-5)°C
- **Time within 5°C of actual Peak Temp ($t_p$)** 30 secs. Max.
- **Ramp-down Rate**: 6°C/sec. Max.
- **Time 25°C to Peak Temp ($T_p$)** 8 min. Max.
- **Do not exceed**: +260°C

**Environmental Specifications**

- **High Temp Voltage Blocking**: 80% Rated $V_{Drm}$ ($V_{sc}$ Peak) +125°C or +150°C, 504 or 1008 hrs. MILSTD-750 (Method 1040) JEDEC, JESD22-A-101
- **Temp Cycling**: -65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MILSTD-750 (Method 1051) EIA/JEDEC, JESD22-A-104
- **Biased Temp & Humidity**: 52 $V_{sc}$ (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
- **High Temp Storage**: +150°C 1008 hrs. MILSTD-750 (Method 1031) JEDEC, JESD22-A-101
- **Low Temp Storage**: -65°C, 1008 hrs.
- **Thermal Shock**: 0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MILSTD-750 (Method 1056) JEDEC, JESD22-A-106
- **Resistance to Solder Heat**: +260°C, 30 secs. MILSTD-750 (Method 2031)

**Physical Specifications**

- **Lead Material**: Copper Alloy
- **Terminal Finish**: 100% Matte-Tin Plated
- **Body Material**: UL recognized epoxy meeting flammability classification 94V-0

**Additional Information**

- Datasheet
- Resources
- Samples

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Dimensions – 5x6 QFN

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<tr>
<th>Dimension</th>
<th>Inches</th>
<th>Millimeters</th>
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<tbody>
<tr>
<td>A</td>
<td>0.187</td>
<td>4.745</td>
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<td>B</td>
<td>0.226</td>
<td>5.745</td>
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<tr>
<td>C</td>
<td>0.054</td>
<td>1.374</td>
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<tr>
<td>D</td>
<td>0.165</td>
<td>4.199</td>
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<tr>
<td>E</td>
<td>0.027</td>
<td>0.686</td>
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<tr>
<td>F</td>
<td>0.011</td>
<td>0.279</td>
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<tr>
<td>G</td>
<td>0.047</td>
<td>1.194</td>
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<td>H</td>
<td>0.032</td>
<td>0.800</td>
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<tr>
<td>I</td>
<td>0.027</td>
<td>0.686</td>
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<td>J</td>
<td>0.100</td>
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<td>K</td>
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<td>0.686</td>
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<td>L</td>
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<td>0.381</td>
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Part Numbering

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<th>Type</th>
<th>SDP xxx 0 Q38 C B</th>
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<tr>
<td>TYPE</td>
<td>SIDACtor DSL Protector</td>
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<td>MEDIAN VOLTAGE</td>
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<td>CONSTRUCTION VARIABLE</td>
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Part Marking

XXXXXX – Part Marking Code
(Refer to Electrical Characteristics Table)

XXXXX – Date Code

Packing Options

<table>
<thead>
<tr>
<th>Package Type</th>
<th>Description</th>
<th>Quantity</th>
<th>Added Suffix</th>
<th>Industry Standard</th>
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<tr>
<td>Q38</td>
<td>5x6x1.5 QFN Tape and Reel Pack</td>
<td>4000</td>
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<td>EIA-481-D</td>
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### Tape and Reel Specifications — 5x6 QFN

**Reel Dimension**

![Reel Dimension Diagram](image)

**Tape Leader and Trailer Dimensions**

![Tape Leader and Trailer Diagram](image)

**Tape Dimension Items**

![Tape Dimension Diagram](image)

<table>
<thead>
<tr>
<th>Symbols</th>
<th>Description</th>
<th>Inches</th>
<th>Millimeters</th>
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<tbody>
<tr>
<td>A</td>
<td>Reel Diameter</td>
<td>N/A</td>
<td>12.992 N/A 330.0</td>
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<tr>
<td>B</td>
<td>Drive Spoke Width</td>
<td>0.059</td>
<td>1.50 N/A</td>
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<tr>
<td>C</td>
<td>Arbor Hole Diameter</td>
<td>0.504</td>
<td>12.80 13.50</td>
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<tr>
<td>D</td>
<td>Drive Spoke Diameter</td>
<td>0.795</td>
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<td>N</td>
<td>Hub Diameter</td>
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<td>W₁</td>
<td>Reel Inner Width at Hub</td>
<td>0.488</td>
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<td>Pocket Width at Bottom</td>
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<td>B₂</td>
<td>Pocket Length at Bottom</td>
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<td>D₂</td>
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<td>E₂</td>
<td>Feed Hole Position 2</td>
<td>0.400</td>
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<td>K₀</td>
<td>Pocket Depth</td>
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<td>P₀</td>
<td>Feed Hole Pitch</td>
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<td>P₁</td>
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<td>W₀</td>
<td>Cover Tape Width</td>
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