Princeton Technology Corp.
Tel: 886-2-66296288
Fax: 886-2-29174598
URL: http://www.princeton.com.tw

DESCRIPTION

PT2240 is programmable encoder utilizing CMOS Technology specially designed for remote control applications. It has a maximum of 22 Address which may be designed by a one-time programmable process. It can support up to 8 Data Bits and is housed in 8 or 16-pin DIP or SOP. It encodes address and data codes into a coded waveform suitable for RF modulation. The pin assignments and application circuit are optimized for easy PCB Layout and cost saving advantage. Furthermore, PT2240's intrinsic feature of being able to support 2/3/4/6/8 data bits considerably reduces inventory pressures.

FEATURES

- CMOS Technology
- Low Power Consumption
- Least External Components
- High Noise Immunity
- Single Resistor Oscillator
- Operating Voltage: 1.8~15 V
- Up to 8 Data Pins
- Up to 222 Address Codes
- One-Time Programmable Process
- Available in SO or DIP Package
- Reduction of Inventory Pressures

APPLICATIONS

- Burglar Alarm System
- Car Security System
- Car/Garage Door Controller
- Home/Office Security System
- Personal Alarm System

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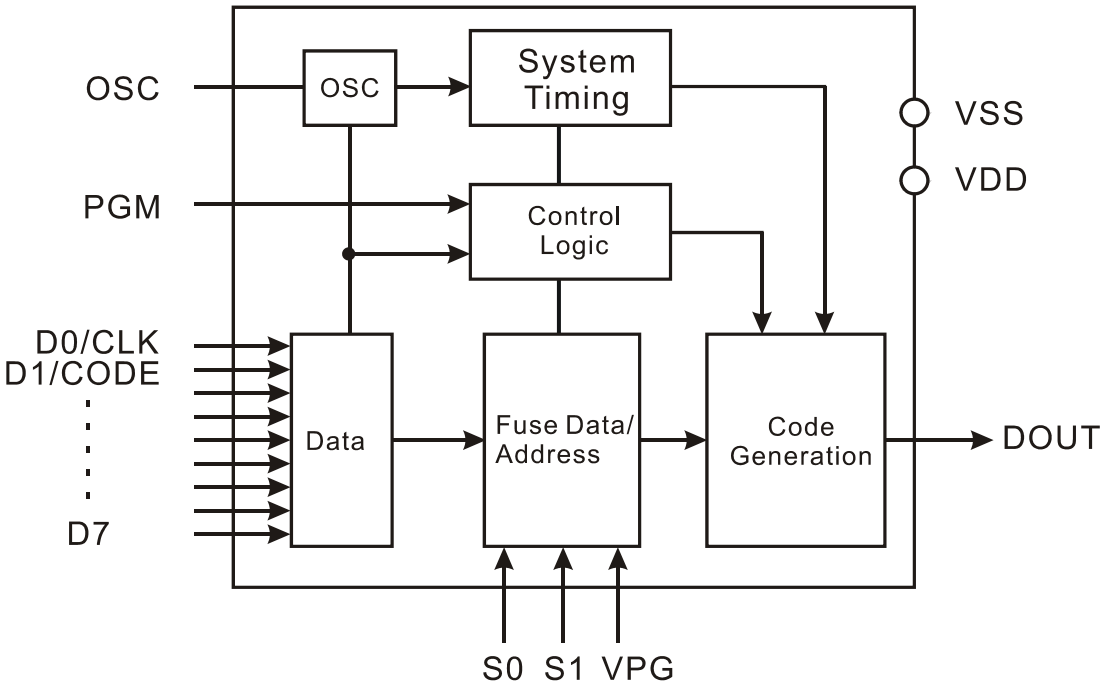
BLOCK DIAGRAM



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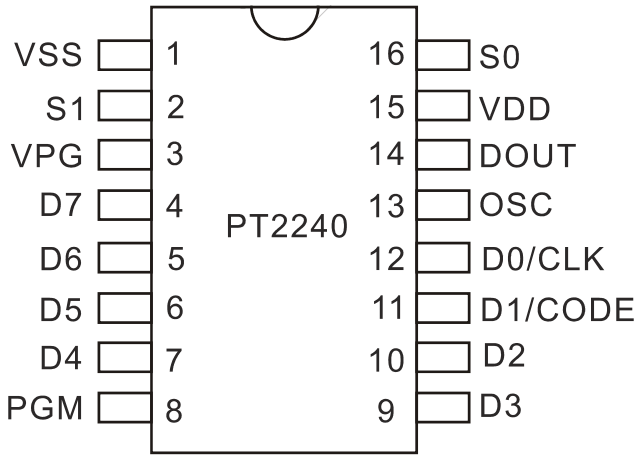
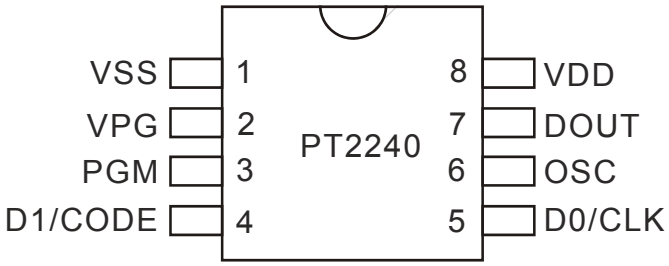
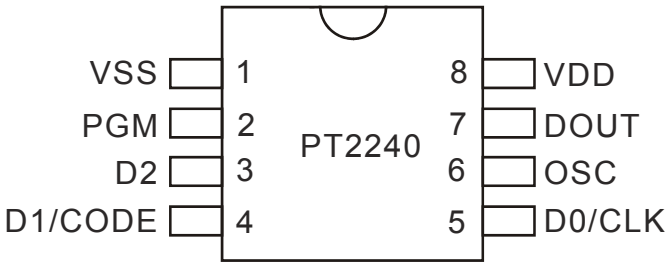
PIN CONFIGURATION



PT2240 (16 PINS)



PT2240 (8 PINS)



PT2240-D3 (8 PINS)

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PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.		
			16 pin	8 pin	8 pin (D3)
VSS	-	Negative Power Supply	1	1	1
S1,S0	I	Select Pin Normal = ”High” These pins are used select the number of data pins if set to “Low”.	2,16	-	-
VPG	I	Voltage Program Pin Normal = “floating” When this pin is set to ”LOW”, the programmed “LOW” bits can be burnt-out.	3	2	-
D2～D7	I	Data Pins (Internal Pull-Low Resistor) These pins are determined by the state of S1 and S0.	4,5,6,7, 9,10	-	-
D2	I	Data Pin	-	-	3
PGM	I	Program Pin Normal = “Low” (Internal Pull-Low Resistor) PT2240 can be programmed if this pin is set to “High”.	8	3	2
D1/CODE	I	Data/Code Input Pin Normal = “Low” (Internal Pull-Low Resistor) 1. When PGM = “High”, this pin functions as a Code Input Terminal. 2. When PGM = “Low”, this pin functions as a Normal Data Input Terminal	11	4	4
D0/CLK	I	Data/Clock Input Pin Normal = “Low” (Internal Pull-Low Resistor) 1. When PGM = “High”, this pin functions as a Clock Input Terminal. 2. When PGM = “Low”, this pin functions as a Data Input Terminal	12	5	5
OSC	I	Oscillator Pin	13	6	6
Dout	O	Data Output Pin Normal = “Low” When PGM = “High”, this pin shows the programming status of PT2240.	14	7	7
VDD	–	Positive Power Supply	16	8	8

FUNCTION DESCRIPTION

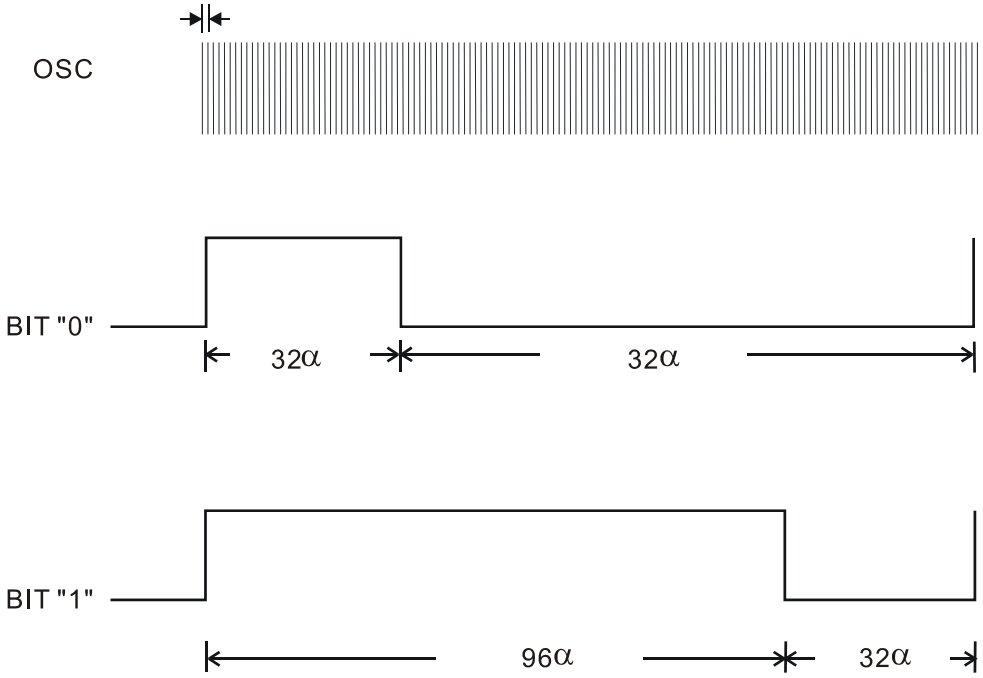
PT2240 encodes the address code (which are one-time programmable) and data set at D2 ~ D7 and A0 ~ A15 into a special waveform and outputs it to the DOUT. This waveform is fed to the RF modulator for transmission. The transmitted radio frequency is received by the RF demodulator and reshaped into the special waveform. PT2270 may be used to decode the waveform and set the corresponding output pin(s). Thus completing a remote control encoding and decoding function.

CODE BITS

A Code Bit is the basic component of the encoded waveform, and can be classified as either an (Address/Data) Bit or a SYNC (Synchronous) Bit.

ADDRESS/DATA BIT WAVEFORM

An Address/Data Bit can be designated as either Bit “0” or “1” if it is in High or Low State respectively. One bit waveform consists of one pulse cycle and each pulse cycle has 128 oscillating time periods. For further details, please refer to the diagram below.
As you can see in the diagram above, Bit “0” consist of a “HIGH“ Pulse for 32α (where α = oscillating time period) then changes to “LOW” Pulse for 96α. Likewise, for Bit “1”, the “HIGH” Pulse for 96α is followed by “LOW” Pulse for 32α.



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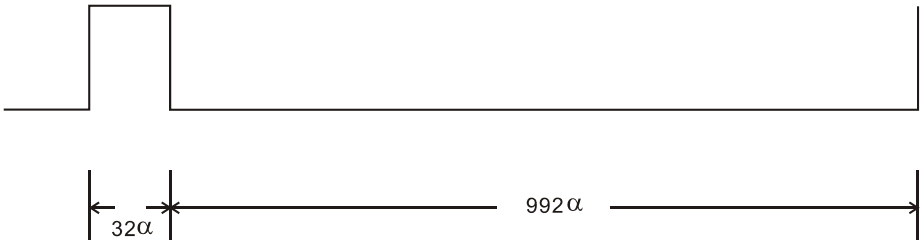
SYNC. BIT WAVEFORM

The Synchronous Bit Waveform is 8 bits long with 1/32 bit width pulse. Please refer to the diagram below.



CODE WORD

A group of Code Bits is called a Code Word. A Code Word consists of 24 Address/Data Bits followed by one Sync Bit. Please refer to the diagram below:

A_0	A_1	A_2	A_3	……..	D_7/A_{16}	D_6/A_{17}	D_5/A_{18}	D_4/A_{19}	D_3/A_{20}	D_2/A_{21}	D_1	D_0	SYNC.

First Bit Transmitted

Note: A_N = Address Bits D_N = Data Bits

S0	S1	Data Type	Address Bit/Data Bit													Sync Bit
1	1	2	A0	A1	A2	A3	·····	A16	A17	A18	A19	A20	A21	D1	D0	SYNC.
1	0	4	A0	A1	A2	A3	·····	A16	A17	A18	A19	D3	D2	D1	D0	SYNC.
0	1	6	A0	A1	A2	A3	·····	A16	A17	D5	D4	D3	D2	D1	D0	SYNC.
0	0	8	A0	A1	A2	A3	·····	D7	D6	D5	D4	D3	D2	D1	D0	SYNC.

PT2240 provides (four) data selections, namely: 2/4/6/8 Data Type which may be defined by the S_0 and S_1 Pins. Up to 8 data bits may be selected. Please refer to the diagram below:

PROGRAMMING

Address Bits of PT2240 are programmable only once and the Output Code Word contains 22 Address Bits, 2 Data Bits, and one Sync Bit.

WRITE

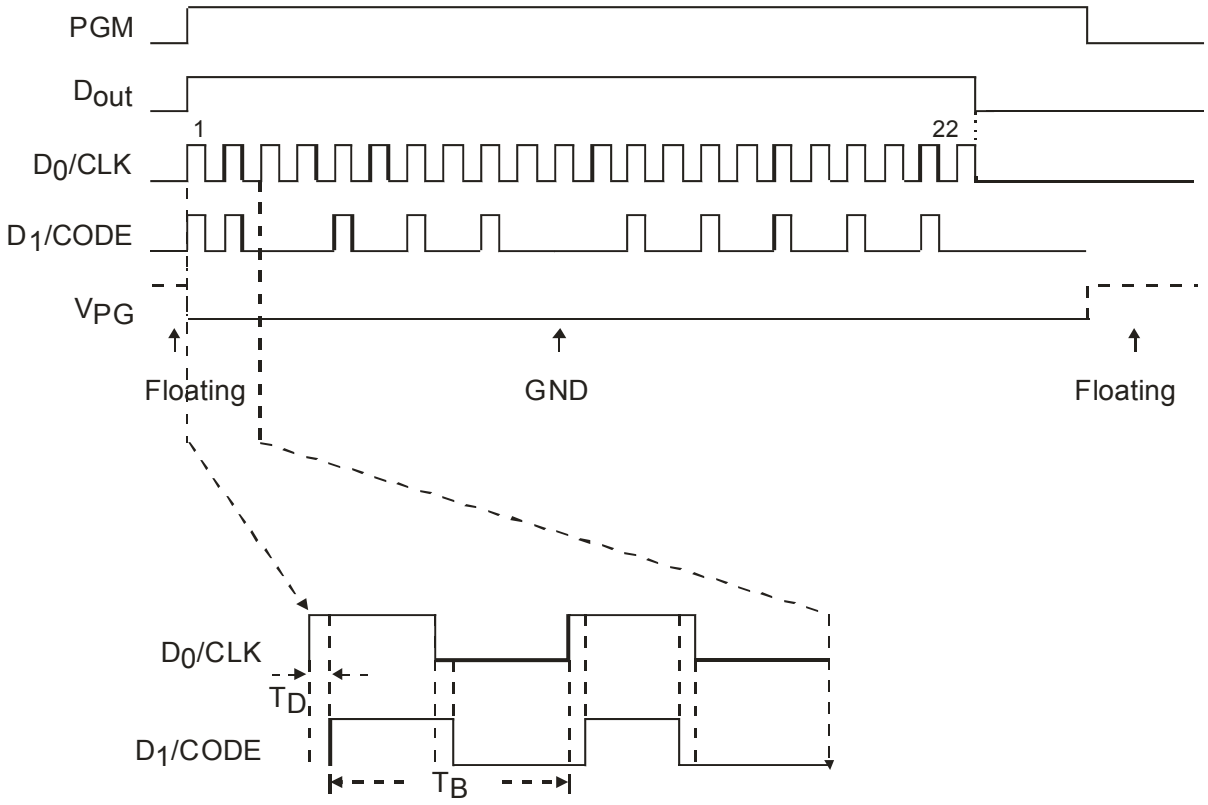
When PGM is set to “HIGH” Level, the WRITE is activated and D_{OUT} changes from “LOW” to “HIGH”. The PT2240 is now ready to be programmed. It must be noted that the first to receive programming instruction is A0 followed by A1 and so forth.

In the WRITE Mode, D_1/CODE signal determines the value of the Address Bit. When D_1/CODE is “HIGH”, the corresponding Address Bit is set to “1”. Conversely, when D_1/CODE is “Low” (or floating), the corresponding Address Bit is set to “0”. After the 22^{nd} pulse, D_{OUT} changes from “HIGH” to “LOW” indicating that the address programming has been completed.

DATA PROGRAMMING IN PT2240

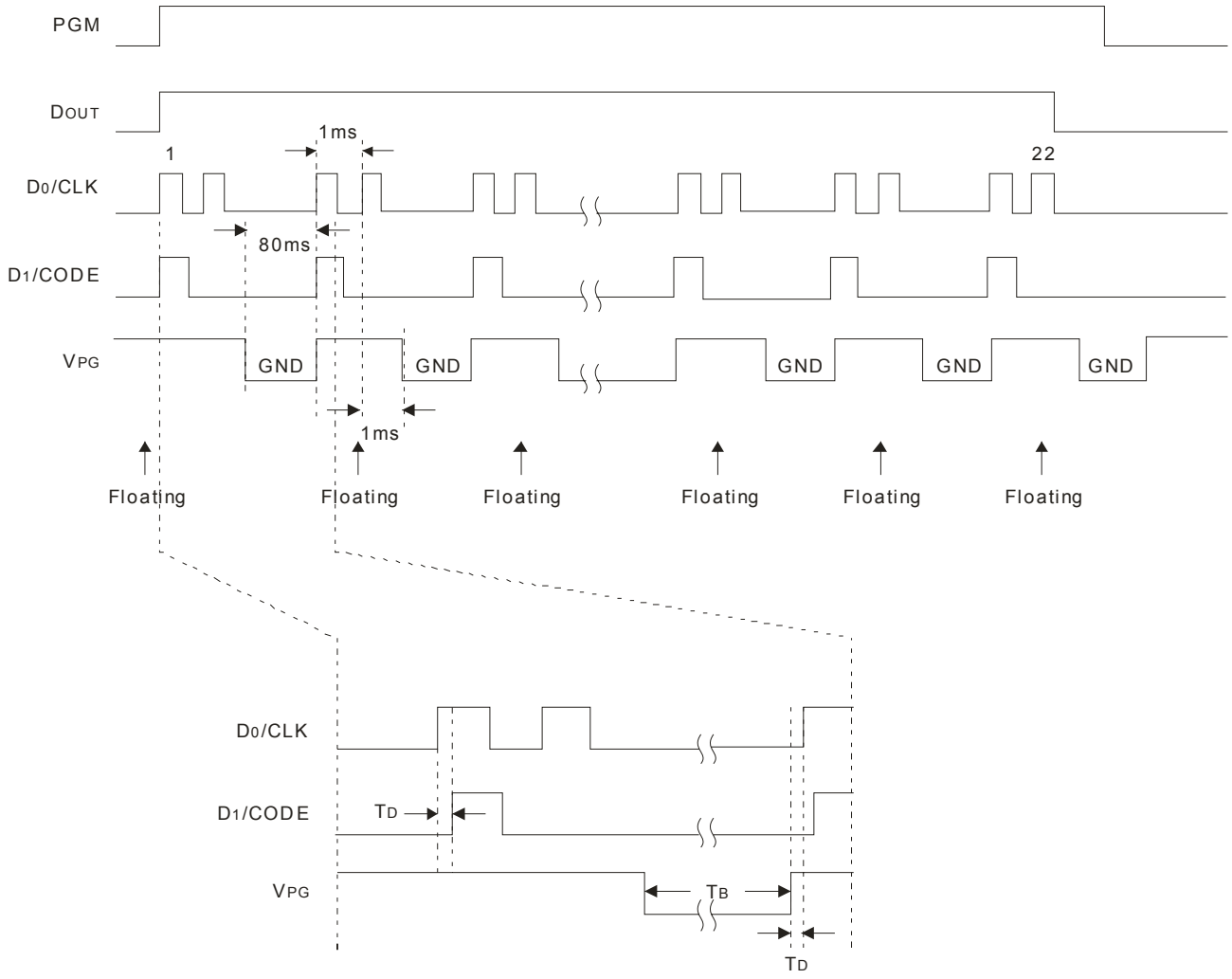
When V_{PG} is “LOW”, at least 80ms is needed to burn out the fuse so that data may be programmed into the PT2240. There are two ways to program PT2240: One Bit Programming and Two-Bit Programming Methods.

More than 100mA is needed to burn out one fuse. One or two fuses can be burnt out at a time. In programming PT2240, the WRITE Procedures must be repeated until the 22 Address Bits have been completely programmed. Please refer to the diagram below:



Note: Address Code = 1100 1010 1000 1010 1010 10
T_D= Delay Time
T_B = Burn-Out Time of the Fuse

Figure 6 shows the One-Bit Programming Technique for the Address Code - **1100 1010 1000 1010 1010 10** -- whereby data are written or programmed into the IC one-bit at a time. As shown in the figure above, the rising sides of the CLK and the CODE must have a delay time (T_D) greater than 0.1 ms. Moreover, the rising sides of the CODE and the CLK must have a burn out time (T_B) greater than 80 ms.

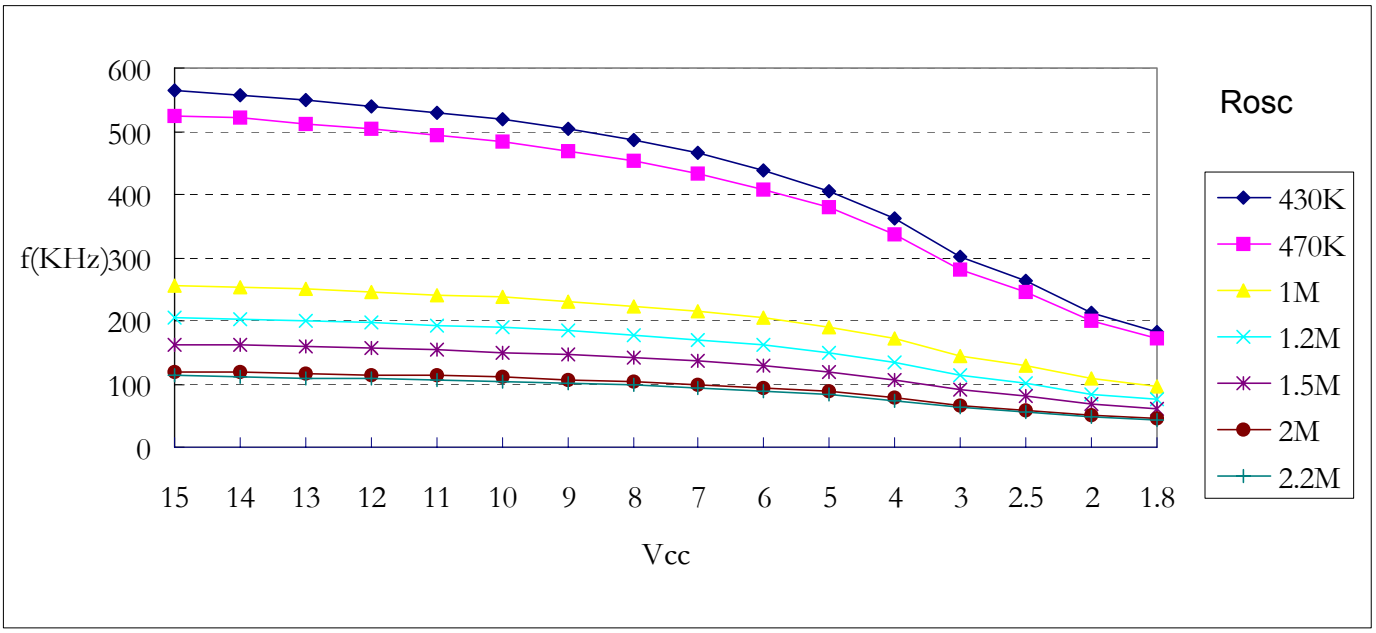


In the Two-Bit Programming Technique, whereby data are written/programmed into the chip two bits at a time, the CLK should be more than 1ms, however, the burn-out time should be greater than 80ms.

Please refer to the PT2240 Application Notes and the PT2240 Programming Manual.

OSCILLTOR

The built-in oscillator circuit of PT2240 allows a precision oscillator to be constructed by connecting an external resistor (Rosc) to the OSC Pin. The typical oscillator frequency with various resistor values for PT2240 is given below:



OUTPUT PIN (DOUT)

While programming PT2240, the state of the IC may be determined by D_{OUT}. During the PROGRAM Mode, D_{OUT} changes from “LOW” to “HIGH”. When the signal inputted from the D_0/CLK Pin‘s reaches the 22nd falling edge of the CLK, the DOUT state changes from “HIGH” to “LOW”. During the rising edge of the 23rd CLK, D_{OUT} is changes from “LOW” to “HIGH”. It must be noted that PT2240 can only be programmed once.

Under normal condition, the D_{OUT} Output Code Format does not include a carrier. Please refer to the diagram below:

DATA PIN

PT2240 can support up to a maximum of 8 data pins which can be determined by the S_1 and S_0 Pins. Please refer to table below:

S0	S1	Data pin	Data Bits	Address Bits
1	1	D0,D1	2	22
1	0	D0,D1,D2,D3	4	20
0	1	D0,D1,D2,D3,D4,D5	6	18
0	0	D0,D1,D2,D3,D4,D5,D6,D7	8	16

Data Bits, D_2 ~ D_7 can de defined by S_0 and S_1. Address Bits – A_{21} ~ A_{16} -- may be set to either “1” or “0” and does not affect the outputs of D_2 ~ D_7. If the data bits are all set to “HIGH”, they do not conflict with each other, and the Output Data Bits are all “HIGH”.

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ABSOLUTE MAXIMUM RATING

(Ta>25℃)

Parameter	Symbol	Conditions	Rating	Unit
Power Supply	V_{DD}		-0.3～15	V
Input Voltage (w.r.t. V_{SS})	V_{IN}	V_{DD}=12V All outputs not connected	V_{SS}-0.3~V_{DD}+0.3	V
Operating Temperature	Topr	V_{DD}=12V	-40 ~ +85	℃
Storage Temperature	Tstg	-	-65 ~ +150	℃

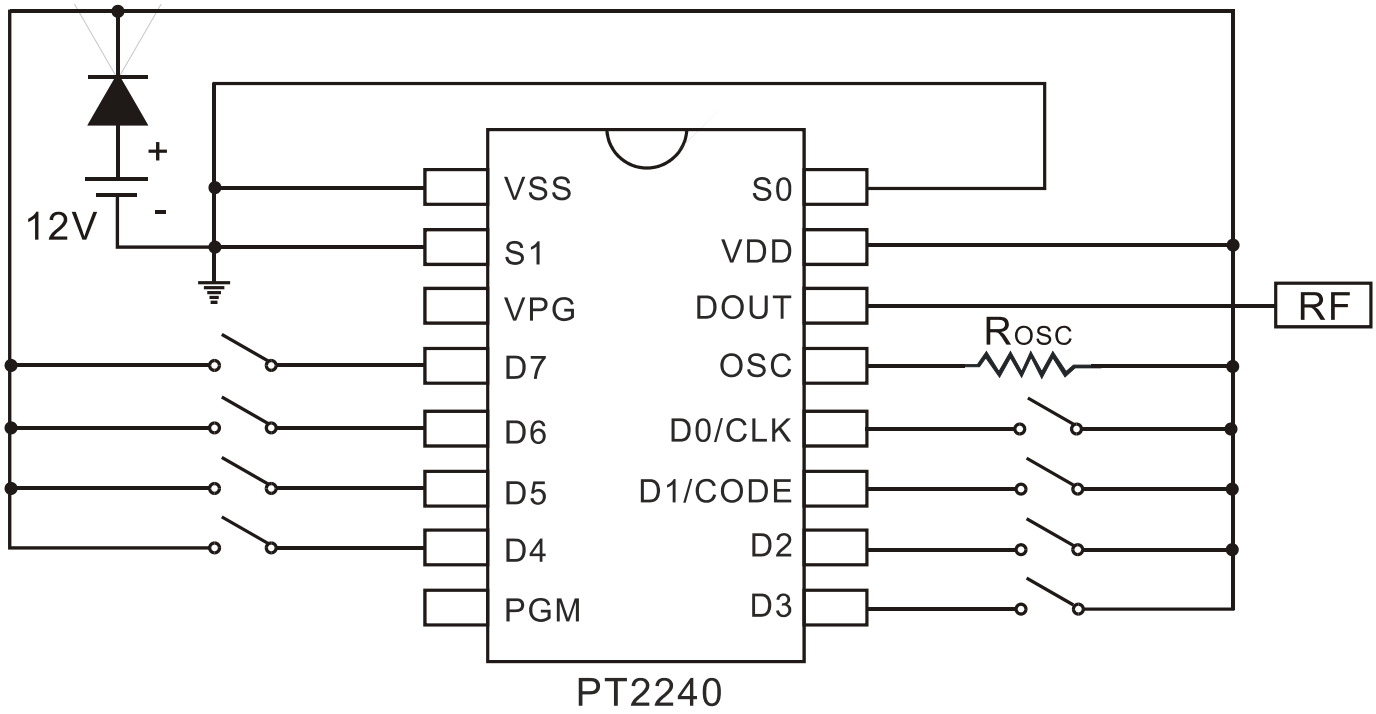
DC ELECTRICAL CHARACTERISTICS

(TA>25℃, V_{DD}=12V)

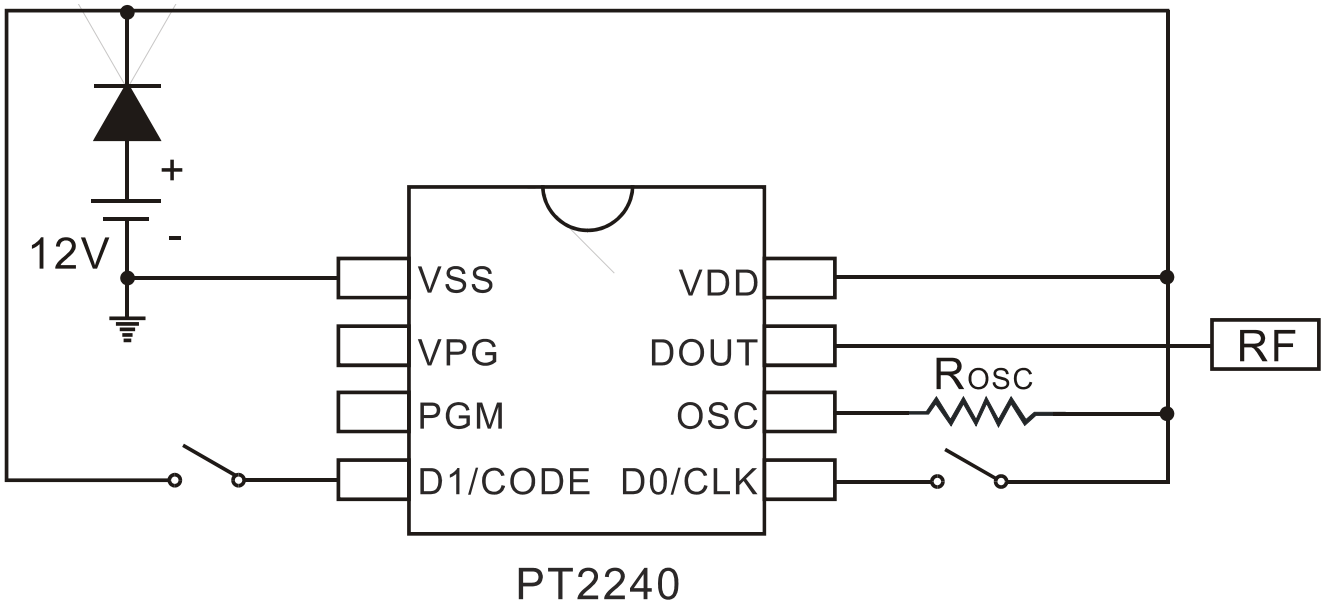
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating Voltage	V_{DD}		1.8	12	15	V
Stand-by Current	I_{SB}	OSC Connected to “Low”, other pins floating	-		1	μA
Operating Current	I_{OP}	Connect One Data Pin to “High”	-		5	mA
D_{OUT} Output Current	I_{OH}	V_{DD}=12V, V_{OH}=5V	20	25		mA
		V_{DD}=9V, V_{OH}=4.5V	12	15		mA
		V_{DD}=3V, V_{OH}=1.5V	1.2	1.4		mA

APPLICATION CIRCUIT

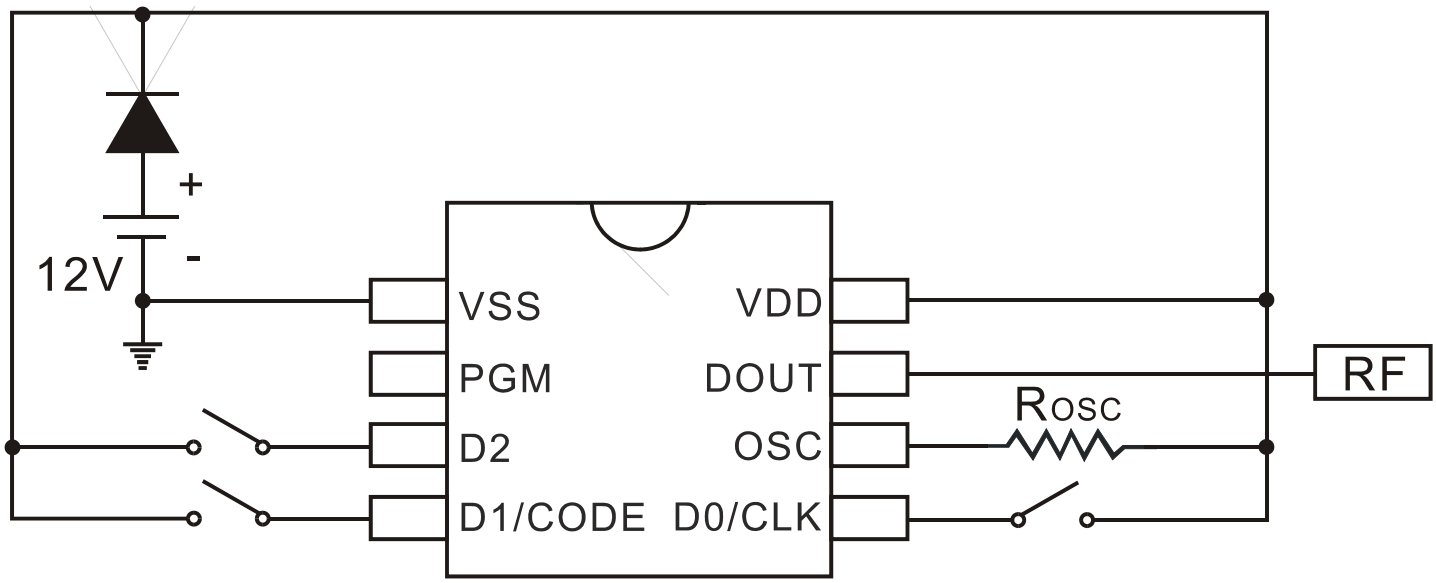
16 PINS, 8 DATA



8 PINS, 2DATA



8PINS, 3DATA



PT2240-D3

Note:
In order that IC protection is assured, please make sure that a diode is connected between the battery and the VDD. If the diode is not connected and the battery polarity was inverted, then the IC will fail.

ORDER INFORMATION

Valid Part Number	Package Type	Top Code	Address Codes
PT2240-D3	8 Pins, DIP, 300mil)	PT2240-D3	Programmable
PT2240P-D3	8 Pins, DIP, 300 mil)	PT2240P-D3	Programmed
PT2240-D3S	8 Pins, SOP, 150 mil)	PT2240-D3S	Programmable
PT2240P-D3S	8 Pins, SOP, 150 mil)	PT2240P-D3S	Programmed
PT2240	8 Pins, DIP, 300 mil)	PT2240	Programmable
PT2240-S	8 Pins, SOP, 150 mil)	PT2240-S	Programmable
PT2240P	8 Pins, DIP, 300 mil)	PT2240P	Programmed
PT2240P-S	8 Pins, SOP, 150 mil)	PT2240P-S	Programmed
PT2240-16	16 Pins, DIP, 300 mil)	PT2240-16	Programmable
PT2240-16S	16 Pins, SOP, 150 mil)	PT2240-16S	Programmable
PT2240P-16	16 Pins, DIP, 300 mil)	PT2240P-16	Programmed
PT2240P-16S	16 Pins, SOP, 150 mil)	PT2240P-16S	Programmed
PT2240-D3 (L)	8 Pins, DIP, 300mil)	PT2240-D3	Programmable
PT2240P-D3 (L)	8 Pins, DIP, 300 mil)	PT2240P-D3	Programmed
PT2240-D3S (L)	8 Pins, SOP, 150 mil)	PT2240-D3S	Programmable
PT2240P-D3S (L)	8 Pins, SOP, 150 mil)	PT2240P-D3S	Programmed
PT2240 (L)	8 Pins, DIP, 300 mil)	PT2240	Programmable
PT2240-S (L)	8 Pins, SOP, 150 mil)	PT2240-S	Programmable
PT2240P (L)	8 Pins, DIP, 300 mil)	PT2240P	Programmed
PT2240P-S (L)	8 Pins, SOP, 150 mil)	PT2240P-S	Programmed
PT2240-16 (L)	16 Pins, DIP, 300 mil)	PT2240-16	Programmable
PT2240-16S (L)	16 Pins, SOP, 150 mil)	PT2240-16S	Programmable
PT2240P-16 (L)	16 Pins, DIP, 300 mil)	PT2240P-16	Programmed
PT2240P-16S (L)	16 Pins, SOP, 150 mil)	PT2240P-16S	Programmed

Notes:
1. (L) = Lead Free
2. The Lead Free mark is put in front of the date code.

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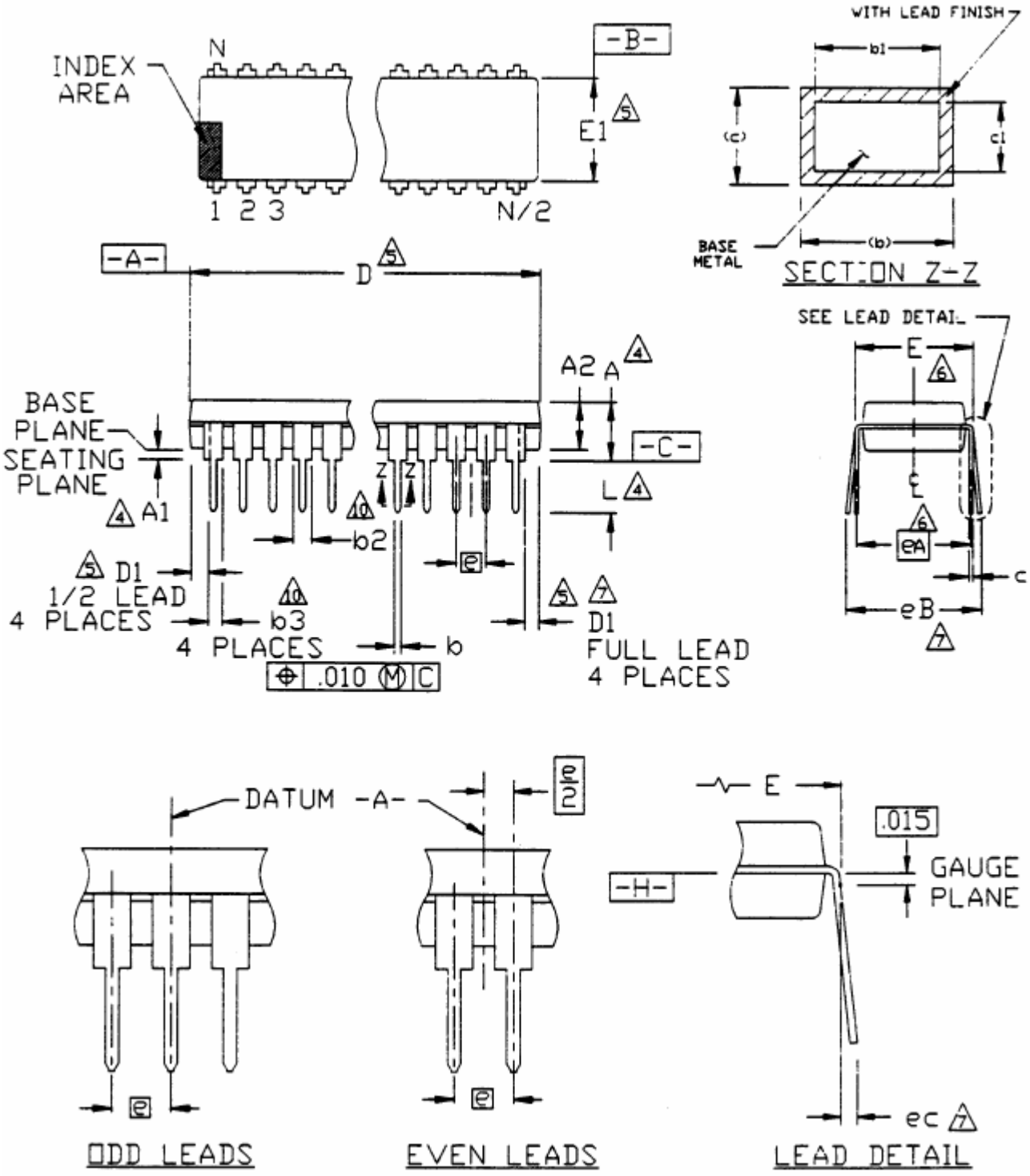
PACKAGE INFORMATION

8 PINS, DIP, 300MIL



Symbol	Min.	Nom.	Max.
A	-	-	0.210
A1	0.015	-	-
A2	0.115	0.130	0.195
b	0.014	0.018	0.022
b1	0.014	0.018	0.020
b2	0.045	0.060	0.070
b3	0.030	0.039	0.045
c	0.008	0.010	0.014
c1	0.008	0.010	0.011
D	0.355	0.365	0.400
D1	0.005	-	-
E	0.300	0.310	0.325
E1	0.240	0.250	0.280
e	0.100 BSC.		
eA	0.300 BSC.		
eB	-	-	0.430
eC	0.000	-	0.060
L	0.115	0.130	0.150

Notes：

1. All dimensions are in INCHS.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimensions “A”, “A1” and “L” are measured with the package seated in JEDEC Seating Plane Gauge GS-3.
4. “D”, “D1” and “E1” dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch.
5. “E” and “eA” measured with the leads constrained to be perpendicular to datum -C-.
6. “eB” and “eC” are measured at the lead tips with the loads unconstrained.
7. “N” is the number of terminal positions. (N=8)
8. Pointed or rounded lead tips are preferred to ease insertion.
9. “b2” and “b3” maximum dimensions are not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25 mm).
10. Variation BA has a b3 dimension and is 1/2 lead package.
11. Distance between leads including dambar protrusions to be 0.005 inch minimum.
12. Datum plane -H- coincident with the bottom of lead, where lead exits body.
13. Refer to JEDEC MS-001 Variation BA.

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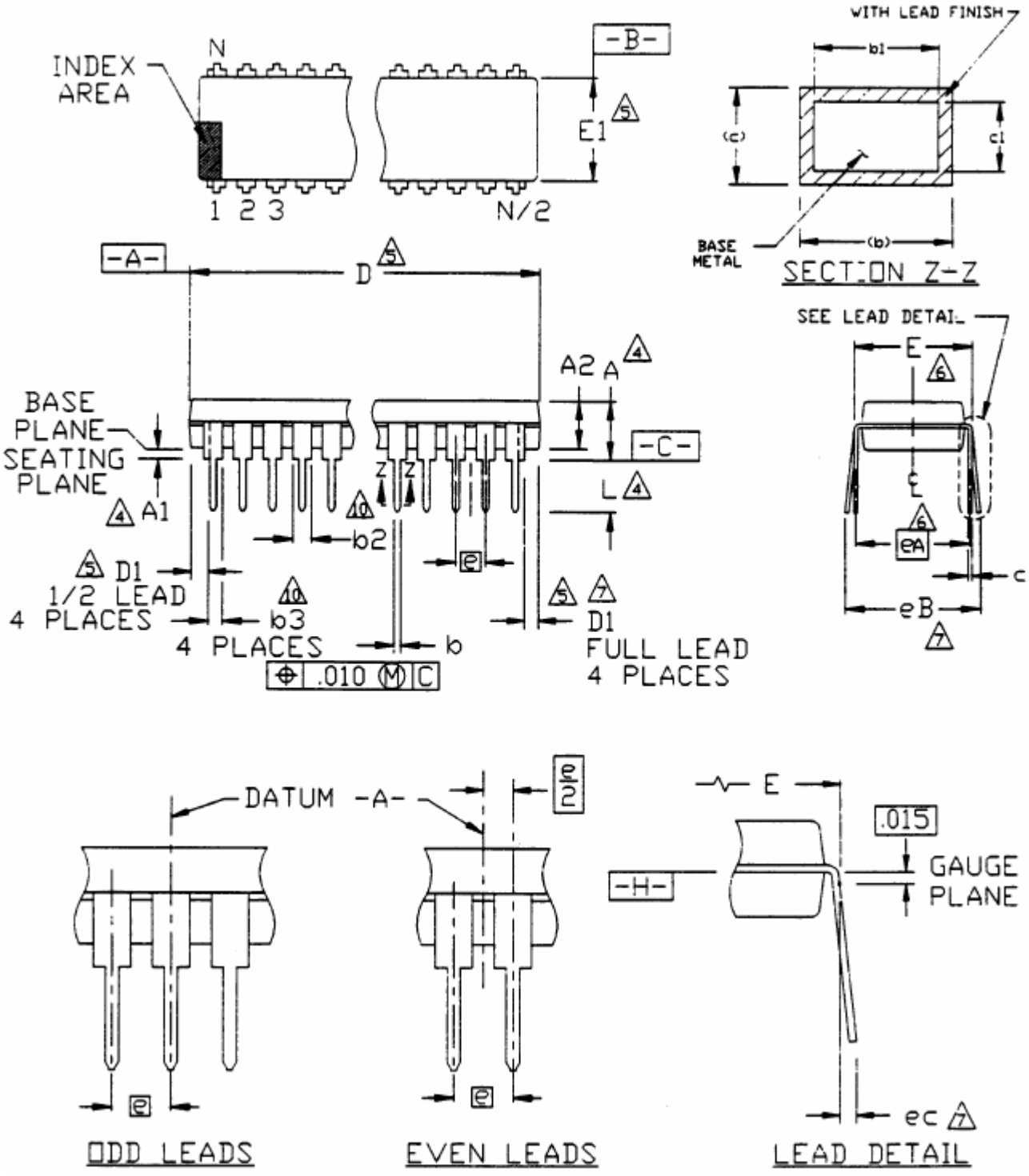
16 PINS, DIP, 300MIL



Symbol	Min.	Nom.	Max.
A	-	-	0.210
A1	0.015	-	-
A2	0.115	0.130	0.195
b	0.014	0.018	0.022
b1	0.014	0.018	0.020
b2	0.045	0.060	0.070
b3	0.030	0.039	0.045
c	0.008	0.010	0.014
c1	0.008	0.010	0.011
D	0.735	0.755	0.775
D1	0.005	-	-
E	0.300	0.310	0.325
E1	0.240	0.250	0.280
e	0.100 BSC.		
eA	0.300 BSC.		
eB	-	-	0.430
eC	0.000	-	0.060
L	0.115	0.130	0.150

Notes：

1. All dimensions are in INCHS.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimensions “A”, “A1” and “L” are measured with the package seated in JEDEC Seating Plane Gauge GS-3.
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7. “N” is the number of terminal positions. (N=16)
8. Pointed or rounded lead tips are preferred to ease insertion.
9. “b2” and “b3” maximum dimensions are not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25 mm).
10. Variation BA has a b3 dimension and is 1/2 lead package.
11. Distance between leads including dambar protrusions to be 0.005 inch minimum.
12. Datum plane -H- coincident with the bottom of lead, where lead exits body.
13. Refer to JEDEC MS-001 Variation BB.

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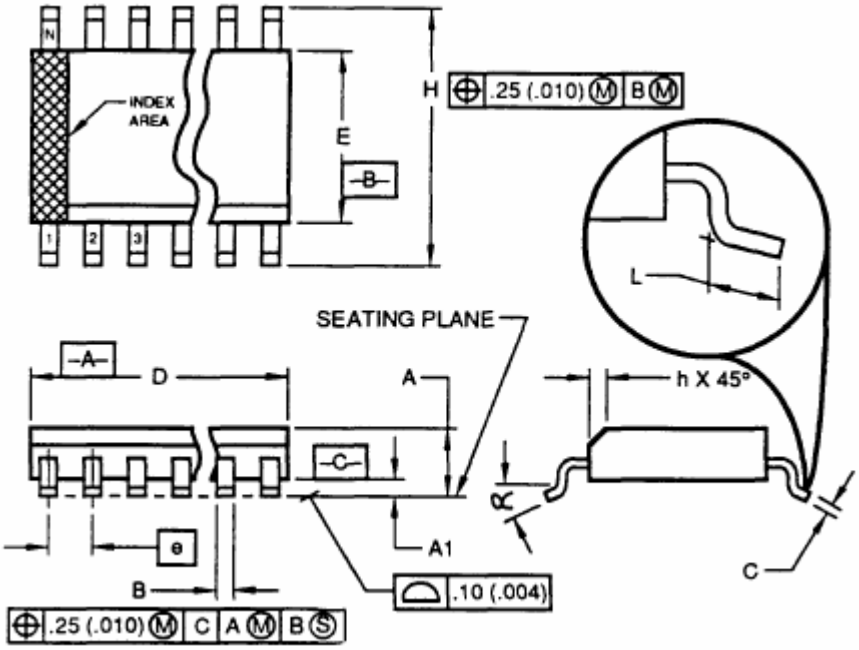
8 PINS, SOP, 150 MIL



Symbol	Min.	Max.
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC.	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Note:

1. Dimensioning and tolerancing per ANSI Y14.5-1982.
2. Dimension D does not include mold flash, protrusions or gate burrs. Mold Flash, protrusion or gate burrs shall not exceed 0.15mm (0.006 in) per side.
3. Dimension E does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. The chamfer on the body is optional. It is not present, a visual index feature must be located within the crosshatched area.
5. L is the length of the terminal for soldering to a substrate.
6. N=Number of terminal position (N=8)
7. The lead width B as measured 0.36 mm (0.014 in) or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.24 in)
8. Controlling dimension: MILLIMETER.
9. Refer to JEDEC MS-012, Variation AA.

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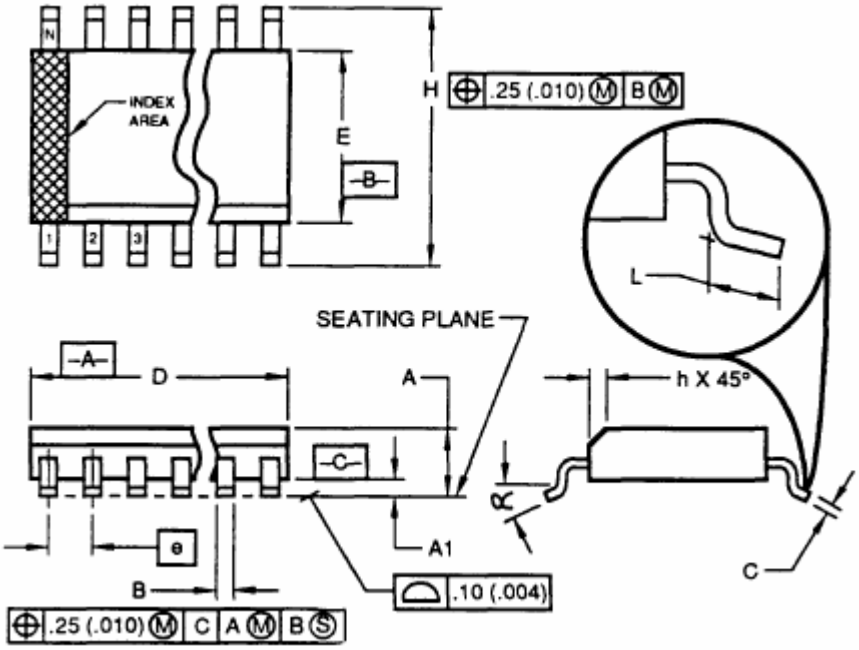
16 PINS, SOP, 150 MIL



Symbol	Min.	Max.
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	9.80	10.00
E	3.80	4.00
e	1.27 BSC.	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Note:

1. Dimensioning and tolerancing per ANSI Y14.5-1982.
2. Dimension D does not include mold flash, protrusions or gate burrs. Mold Flash, protrusion or gate burrs shall not exceed 0.15mm (0.006 in) per side.
3. Dimension E does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. The chamfer on the body is optional. It is not present, a visual index feature must be located within the crosshatched area.
5. L is the length of the terminal for soldering to a substrate.
6. N=Number of terminal position (N=16)
7. The lead width B as measured 0.36 mm (0.014 in) or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.24 in)
8. Controlling dimension: MILLIMETER.
9. Refer to JEDEC MS-012, Variation AC.

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