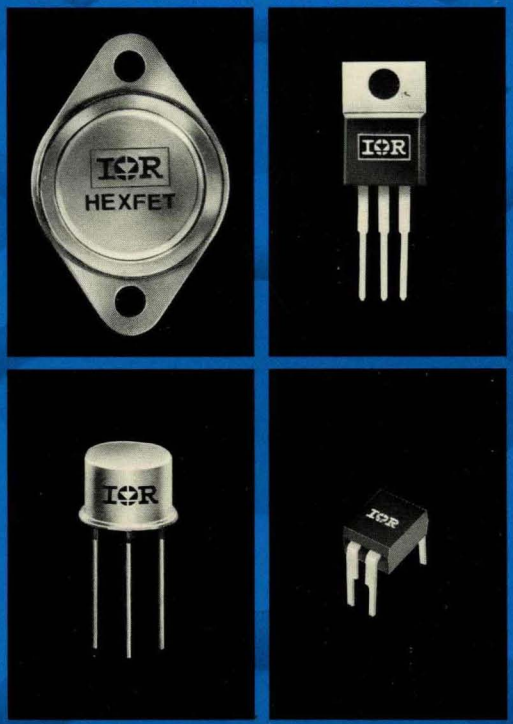
INTERNATIONAL RECTIFIER HEXFETS

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NUMBER 1 IN POWER MOSFETs!



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INTERNATIONAL RECTIFIER

HEXFET DATABOOK

POWER MOSFET APPLICATION AND PRODUCT DATA

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INTERNATIONAL RECTIFIER

HEXFET®* DATABOOK

POWER MOSFET APPLICATION AND PRODUCT DATA

1982-83

FIRST PRINTING
HDB-2

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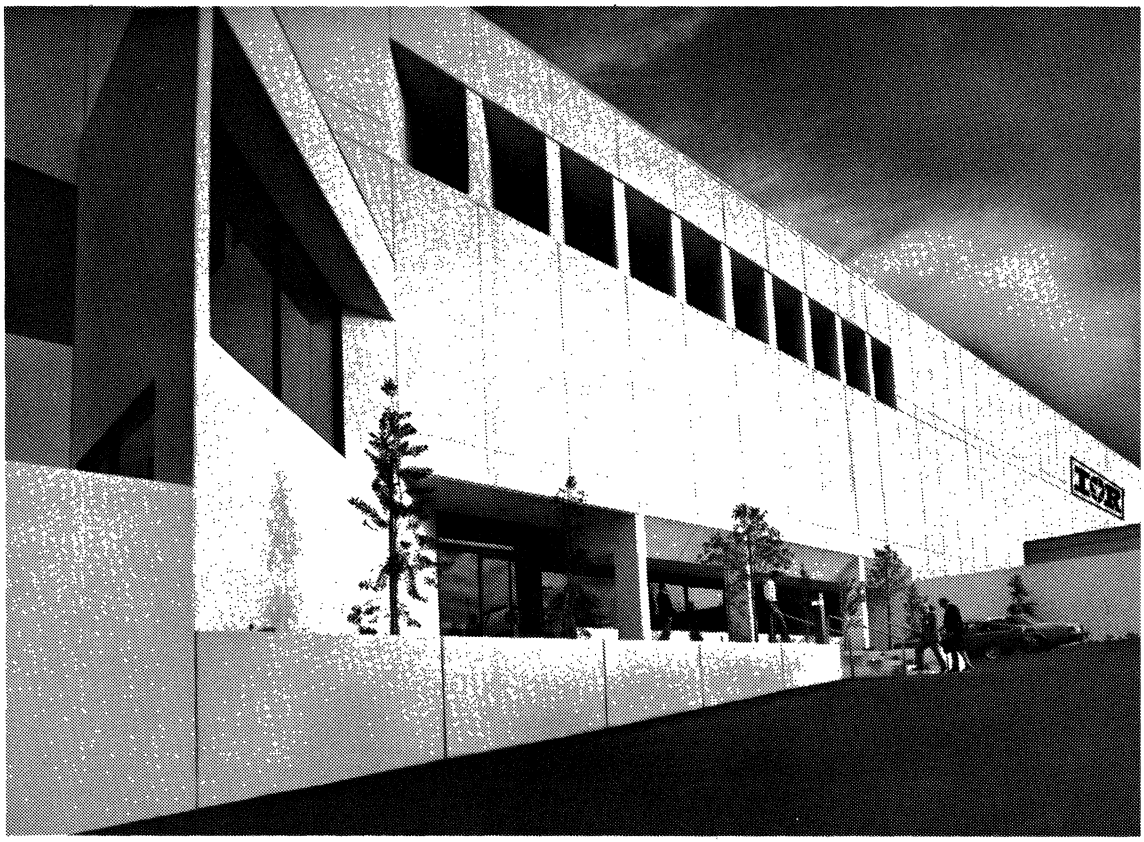
PREFACE

In mid-1979, International Rectifier introduced a new series of power MOSFETs to industry that opened vast, new opportunities for designers of any equipment, system or power supply that had, until that time, been limited by the performance characteristics of bipolar transistors.

International Rectifier's "HEXFET" technology, so named because of a structure based on thousands of hexagonal cells in densities up to 500,000 per square inch, brought the first MOSFETs to the power range capable of matching the on-resistance of bipolar transistors. For the first time, the advantages of power MOSFETs could be utilized without a sacrifice in efficiency.

This technological feat has sparked a revolution in design, capitalizing on the advantages of voltage control, extremely high switching speeds, temperature stability and the rugged physical characteristics of power MOSFETs. There are few circuits previously designed with bipolar transistors that cannot now be designed with MOSFETs to perform far better, in less space, with fewer components, and without the complexity of protective circuits required by the bipolar counterparts.

Along with this contribution to technology,



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International Rectifier brought a commitment to power MOSFETs that has made the company today's leader in the field.

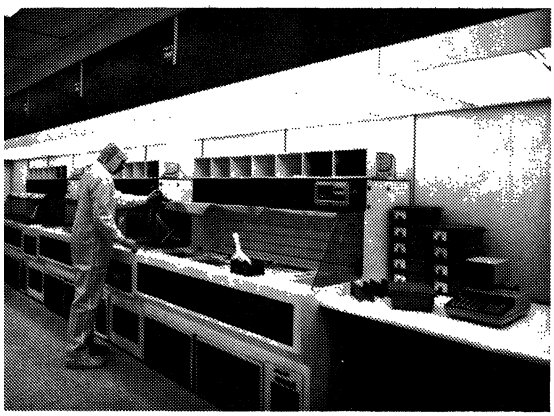
A commitment to quality. A commitment to production that enabled the company to ship more power MOSFETs in the 25-watt and above range than all other power MOSFET manufacturers in the world combined during 1980. A commitment to distribution that has put yesterday's laboratory achievement onto Distributors shelves around the world. Perhaps the most convincing proof of the total commitment International Rectifier has made is pictured below. This new structure houses today's largest state-of-the-art, high technology facility in the world devoted exclusively to power MOSFET wafer fabrication. On stream now, its initial production capacity is sufficient to supply today's entire industry requirements for power MOSFETs, and is expandable to meet all demands to be experienced during the evolution from bipolar transistors to power MOSFETs in the equipment of tomorrow.

This DATABOOK lists todays broadest line of readily available power MOSFETs. More types and packages will follow to make your design job easier and your products better.

We're committed to that.









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Quality, Reliability, and the HEXFET

It is International Rectifier's stated objective to make the HEXFET the most reliable semiconductor device ever manufactured. In order to meet this goal IR budgets approximately $1,000,000 a year to measure, record and improve the reliability of our HEXFET.

HEXFET Quality Today

All lots are screened at outgoing inspection to a 0.1% AQL. This corresponds roughly to a 1000 part per million defect rate. The purpose of screening HEXFETs to such tight levels is to provide our customers with parts that will no longer require an incoming inspection, hence resulting in a significant savings and reduced inventory.

100% Visual Inspection

All HEXFETs, commercial or Hi-Rel, plastic or hermetic, are 100% pre-cap or pre-encapsulation inspected. This inspection ensures proper wire bond placement, no damage to the semiconductor chip, as well as general appearance of the die bond and die coat, where applicable. International Rectifier's reliability group has correlated these inspection criteria to improved long term reliability results on such tests as HTRB (High Temp Reverse Bias) and gate stress.

Traceability

All parts are tested, marked and shipped so as to maintain wafer lot and assembly lot traceability. International Rectifier feels lot traceability is an essential part of our reliability program so that, if, anytime in the future, a customer has a problem or a question concerning HEXFETs they have received, IR can attempt to correlate, the effect with the part's process history.

100% Reliability Tests

Before any part is released for customer shipment, each and every wafer and assembly lot goes through an extensive series of tests designed to indicate the ultimate reliability that can be expected. This is called our Reliability Certification Program.

From each lot a sample of 80 pieces is taken. Forty pieces are put through a series of accelerated life tests (the tests are listed in table 1). Another 40 parts are destructively tested to determine the ultimate process limits; this guarantees that the parts are rugged and that there has been no 'drift' in the process parameters (See table 2). Finally, 40 parts are kept with all the lot travelers and test results so that if a future question requires data we did not take we can always run a statistically valid test and correlate our findings with those of our customer.

If any lot does not meet any of our high standards during these tests it will not be shipped.

Table 1: Reliability Certification - Accelerated Tests

TEST	SAMPLE SIZE	REJECT ON	PURPOSE
HTRB T_J=150° C	40	1	Detect temperature dependent failure modes and any change in performance parameters with temp.
GATE STRESS T_J=150° C	40	1	Check the reliability of gate oxide and oxide/silicon interface.

Table 2: Reliability Certification - Destruction Tests

TEST	SAMPLE SIZE	REJECT ON	PURPOSE
SOA FAIL POINTS	10	1	Check power handling capability
GATE DIELECTRIC STRENGTH	10	1	Check oxide integrity.
AVALANCHE ENERGY	10	1	Check ability to handle inductive overloads.
THERMAL RESISTANCE	10	1	Check Integrity of header/solder/die interface.

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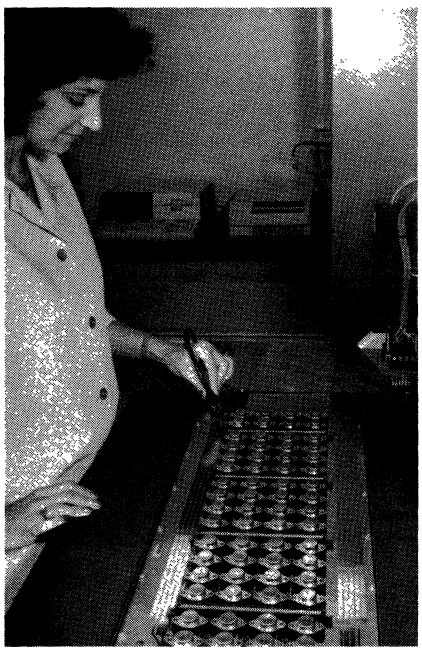
Long Term Reliability Reports

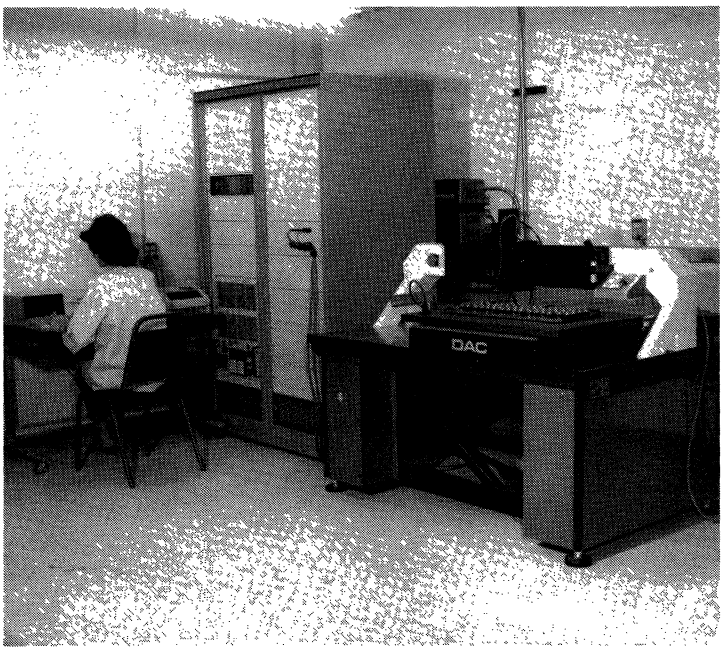
Finally, International Rectifier publishes quarterly HEXFET Reliability Reports which summarize all the reliability data we have taken during that period. Once a year the results are summarized. The reliability data accumulated in this report is outlined in Table 3. Reliability Reports are available to all customers on request.

Specifying a HEXFET power MOSFET for your design assures the ultimate in reliability and performance.

Table 3: Reliability Report

TEST	CONDITIONS	PURPOSE
85/85 (plastic packages) T_J=85°C	.85 V_{DS} 85% relative humidity 1000 hours	Check ability of non-hermetic packages to operate with bias in high relative humidity.
Power Cycles	$\Delta T = 70°K$	Determine number of power cycles the package/solder/die combination can withstand.
HTRB	.8 V_{DS} $T_J = 150°C$	Determine failures per 1000 hrs. for each failure mode and temperature dependent activation energy.





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Applying International Rectifier's Power MOSFETs

By BRIAN R. PELLY

International Rectifier's Power MOSFETs open the door to the design of advanced products by offering the superior characteristics of Field Effect Transistors at true high power levels. Power MOSFETs simplify circuitry because they are voltage-controlled devices and require only very small instantaneous currents from the signal source. They achieve switching times of less than 100 nanoseconds at high current levels. They have great ruggedness because of the absence of the second breakdown failure mechanism of bipolar transistors. In parallel operation they inherently "current share" rather than "current hog." The stability of the gain and response time characteristics over a wide temperature range is outstanding. The net result is a radically advanced power transistor of universal application capability.

HEXFET™ Technology

International Rectifier now offers a truly advanced line of power MOSFETs termed the HEXFETs™. The HEXFETs are IR's second generation power MOSFET design and feature uniquely advanced technology. The HEXFET technology achieves both new high power records in switching ratings for field effect transistors and new economies in MOSFET production costs. IR's

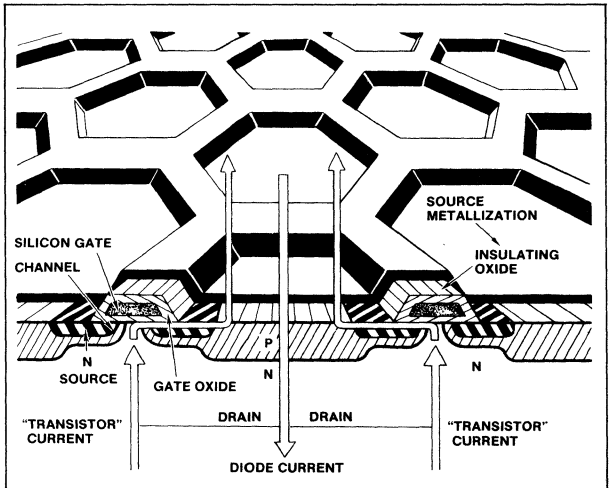


Figure 1. Basic HEXFET Structure

The HEXFET Structure

The HEXFET surface is characterized by a multiplicity of closed hexagonal source cells (over 500,000 per square inch) from which the name HEXFET is derived. In cross section, the HEXFET is based on a double-diffused (DMOS) structure. A channel is formed by double diffusion at the periphery of each hexagonal source cell. An insulating gate oxide layer covers the channel. A silicon gate then overlays both the insulating oxide and channel. The silicon gate in turn is insulated from the source by an additional oxide layer. All of the hexagonal source cells are then parallel connected by a continuous sheet of metalization which forms the source terminal.

Transistor action occurs by penetration of an electric field into the channel area which modulates the conductivity between drain and source. Conventional current flow is from the drain substrate, across the channel surface, and vertically out the source terminal.

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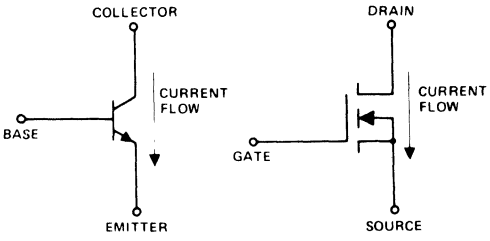


Figure 2. Electrical Symbols for Bipolar and MOSFET

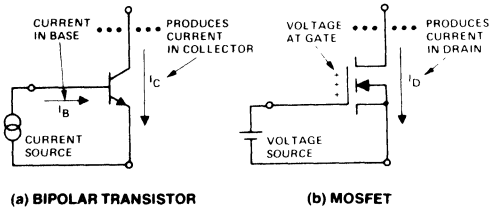


Figure 3. Bipolar Transistor is Current-Driven, MOSFET is Voltage-Driven

HEXFETs set the stage for large scale usage in applications which previously could be handled only by the bipolar technology.

Until recently, large-area MOSFET devices combining the low on-resistance and the high-voltage characteristics of a true power transistor could not be fabricated. With IR's HEXFET technology, however, on-resistances as low as 0.05 ohms are possible at the 100 volt level. Voltage ratings as high as 500 volts are possible by making a tradeoff with higher on-resistance. HEXFET switching ratings in excess of 4 kilowatts are available in a single device.

The HEXFET Structure

As implied, the HEXFET structure involves a hexagonal device geometry. At the core is a radically new hexagonal cellular structure, illustrated diagrammatically in Figure 1. It is this hexagonal geometry, along with advanced MOS processing, that gives the HEXFET an on state resistance, $R_{DS(on)}$, one-third of that possible with the best previous MOSFET technology, in a given die size. At a given current level, therefore, the HEXFET can achieve a forward voltage drop quite comparable to the collector-emitter saturation voltage of high performance bipolar transistors that have about the same die size.

A planar, non V-groove structure, the HEXFET conducts current vertically. For high packing density, it uses a silicon-gate structure. The density of the hexagonal source cells on the top surface of the silicon die is over half a million cells per square inch. Electrons flow from a source cell through the channel which is around the periphery of that cell and then into the drain body. The bottom surface of the drain body is in electrical and thermal contact with the header.

The efficient hexagonal source pattern, the silicon gate, and advanced MOS processing techniques all combine to produce the HEXFETs' unique performance characteristics.

Some Basic Considerations

As we have seen, the HEXFET is IR's advanced design of power MOSFET. Power MOSFETs are majority carrier semiconductor devices, and their construction and principles of operation are fundamentally different from those of traditional bipolar transistors, which are minority carrier semiconductors. These fundamental differences must be understood if full advantage is to be taken of the MOSFETs' special performance features.

MOSFET Symbol and Terminology

The collector, base and emitter terminology for the terminals of a bipolar transistor is replaced by drain, gate, and source, respectively for a MOSFET. Figure 2 shows the circuit symbol for an N-channel MOSFET, and makes a comparison with a conventional bipolar transistor.

Driving the Power MOSFET

The conventional bipolar transistor is essentially a current-driven device. As illustrated in Figure 3 (a), a current must be applied between the base and emitter terminals to produce a flow of current in the collector. The amount of drive required to produce a given output depends upon the gain, but invariably a current must be made to flow into the base terminal to produce a flow of current in the collector.

The MOSFET is fundamentally different; it is a voltage-controlled device. A voltage must be applied between the gate and source terminals to produce a flow of current in the drain, as illustrated in Figure 3(b). The gate is isolated electrically from the source by a layer of silicon oxide. Theoretically no current flows into the gate when a DC voltage is applied to it — though in practice there will be an extremely small leakage current, in the order of nanoamperes.

With no voltage applied between the gate and source electrodes, the impedance between the drain and source terminals is very high, and only a small leakage current flows in the drain until the applied voltage exceeds the drain-to-source avalanche voltage. This is illustrated in Figure 4.

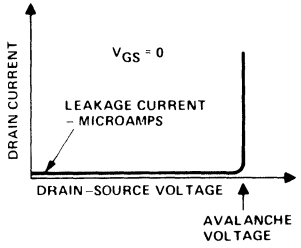


Figure 4. Drain-Source Blocking Characteristic

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When a voltage is applied between the gate and source terminals, an electric field is set up within the MOSFET. This field modulates the resistance between the drain and source terminals, and permits a current to flow in the drain in response to the applied drain circuit voltage. The amount of current that flows depends upon the amount of voltage applied to the gate, assuming that the impedance of the external drain circuit is not limiting.

Because the gate draws only a minute DC leakage current, the DC current gain is extremely high, typically in the order of 10^9. In fact, this is a rather meaningless parameter for a power MOSFET, and it is not normally used. Because a flow of *current* in the drain is produced essentially by a *voltage* applied to the gate, a more useful parameter for the MOSFET is the *transconductance*. This is the change of drain current brought about by a 1 volt change of gate voltage.

The extremely low drive current requirement of the power MOSFET, and the associated extremely high power gain, are a major advantage over the conventional bipolar transistor or Darlington. This feature will often make it possible to drive the power MOSFET directly from CMOS or TTL integrated circuit logic.

The Static Operating Characteristics

The fundamental drain-source operating characteristics of the power MOSFET are illustrated in Figure 5(a). For comparison, Figure 5(b) shows the corresponding collector-emitter characteristics for a conventional bipolar transistor.

For any given value of gate voltage there are essentially two clearly separate regions on the drain current-voltage characteristic (with an intermediate zone that connects the two). The first is a "constant resistance" region. As the drain-to-source voltage is increased, the current increases almost proportionately, though in practice the resistance does increase at higher currents. At a certain current level, however, a channel pinchoff effect is reached within the device, and the operating characteristic moves into a constant current region.

The bipolar transistor also exhibits a generally similar type of collector characteristic. It does not, however, show a truly resistive effect in its saturation region, nor does it exhibit nearly such a well regulated constant current characteristic.

For switching applications, the On-Resistance $R_{DS(ON)}$ of the power MOSFET is obviously an important characteristic because it determines the power loss for a given drain current. The lower the On-Resistance the higher the current handling capability of the device. On-Resistance is thus an important "figure of merit" of the power MOSFET.

Threshold Voltage and Transconductance

Inspection of the static drain-source operating characteristics of Figure 5 reveals that as the gate-to-source voltage is increased from zero, initially the drain current does not increase significantly. Only once a certain threshold gate voltage has been reached, does the drain current start to increase appreciably.

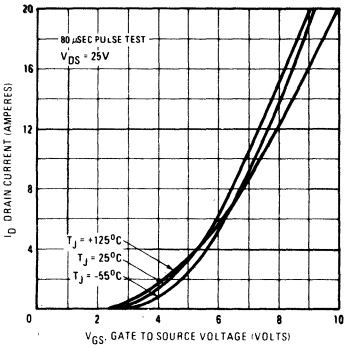


Figure 6. Transfer Characteristics (IRF130)

This is illustrated more clearly by the typical relationships between drain current and gate voltage shown in Figure 6. It is seen that in the operating region beyond the threshold gate voltage, the relationship between the drain current and the gate voltage is approximately linear. Stated another way, the rate of change of drain current with gate voltage — the transconductance referred to earlier — becomes relatively constant at higher values of drain current.

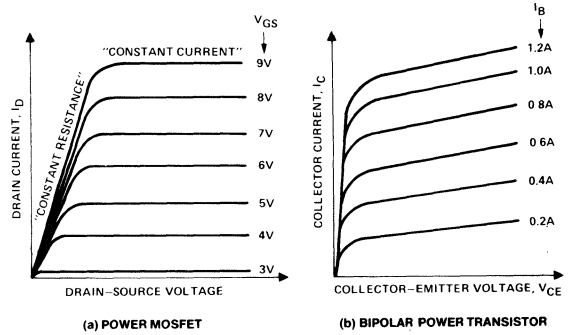


Figure 5. Comparison of Idealized Output Characteristics of Power MOSFET and Bipolar Transistor

Features of IR Power MOSFETs

Basic Characteristics

Table 1 shows the available types at the time of publication of this article, September, 1979. Other types will continue to be introduced, and the reader should check with IR for the latest product information.

All IR's MOSFETs will conduct their rated continuous drain current, I_D, with less than 10 volts, V_{GS}, applied from gate-to-source. Conduction will begin before 3 volts $V_{GS(th)}$, threshold voltage is applied to the gate. The threshold voltage is always greater than 1 volt, which allows leakage currents from a previous stage to be easily bypassed to ground. A cutoff condition of the power stage is thereby assured without any special reverse-biasing. All units have a maximum junction operating temperature of 150°C.

Rated at 100V, 28A continuous and 70A pulsed, the IRF150 (Table 1) brings on-resistance down to the lowest value to date of any power MOSFET — 0.055Ω maximum. Typical on-resistance, just 0.04Ω, produces a 1.0V saturation-voltage drop

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PARAMETER			Data Sheet PD 9.302				Data Sheet PD 9.304				Data Sheet 9.303				Data Sheet PD 9.305			
			IRF 330	IRF 331	IRF 332	IRF 333	IRF 350	IRF 351	IRF 352	IRF 353	IRF 130	IRF 131	IRF 132	IRF 133	IRF 150	IRF 151	IRF 152	IRF 153
V_{DS}	Drain-Source Voltage (Max.)	V	400	350	400	350	400	350	400	350	100	60	100	60	100	60	100	60
I_D	Continuous Drain Current (Max.)	A	4		3.5		11		10		12		10		28		24	
I_{DM}	Pulsed Drain Current (Max.)	A	8		7		25		20		30		25		70		60	
$R_{DS(on)}$	On-State Resistance (Max.)	Ohms	1		1.5		0.3		0.4		0.18		0.25		0.055		0.08	
P_D	Power Dissipation (Max.)	W	75				150				75				150			
g_{fs}	Forward Transconductance (Typical)	Mhos	3.5				9				5				10			
$t_{d(on)}$	Turn on Delay Time (Typical)	ns	50				60				50				60			
t_r	Rise Time (Typical)	ns	100				150				150				200			
$t_{d(off)}$	Turn off delay time (Typical)	ns	100				400				100				300			
t_f	Fall time (Typical)	ns	100				150				150				200			
C_{iss}	Input Capacitance (Max.)	pF	1000				4000				1000				4000			

Table 1. Ratings and Characteristics of IR's High Current HEXFETs. September 1979

at 25A, which is low enough to compare with the $V_{VE(SAT)}$ of a bipolar transistor of similar size, and lower than that of a Darlington transistor.

Such a small forward voltage drop is particularly impressive in light of the fact that the HEXFET requires only nanoamperes of gate drive, not the amperes of base drive a bipolar needs. In addition, the MOSFET does not suffer the loss of switching speed the bipolar does when driven hard into saturation.

The IRF350 (Table 1) is a high voltage version of the die size used for the IRF150 transistor. Rated at 400V and 11A continuous, 25A pulsed, the IRF350 has a maximum on-resistance of 0.30Ω. Moreover, an ability to switch 4.4kW continuously makes the IRF350 by far the highest-power MOSFET available anywhere in the world at the time of writing.

At a case temperature of 25°C, both of these HEXFETs have a continuous dissipation rating of 150W. Thermal impedance, from junction to case, is 0.83°C/W. Both the IRF150 and IRF350 families are in standard TO-3 metal cases, with copper base and 0.06in. diameter pins for high electrical and thermal conductivity.

The lower power IRF130 and IRF330 families provide voltage ratings and maximum on-resistance values essentially equivalent to the first generation IRF100 and IRF300 MOSFET families (now obsolescent). The HEXFETs accomplish the specifications with a transistor die about one-third the size of the original MOSFET types.

Able to handle 12A continuous, 30A pulsed, the 100V IRF130 holds on-resistance to a maximum 0.18Ω. And providing greater blocking voltage and lower current capability, the IRF330 is rated at 400V and 4.0A continuous, 8.0A pulsed. Its maximum on-resistance is 1.0Ω.

At a case temperature of 25°C, these lower power HEXFETs can dissipate 75W of dc power. Their internal thermal impedance is 1.6°C/W. Again, the package is the industry-standard TO-3 case, with 0.04in diameter pins.

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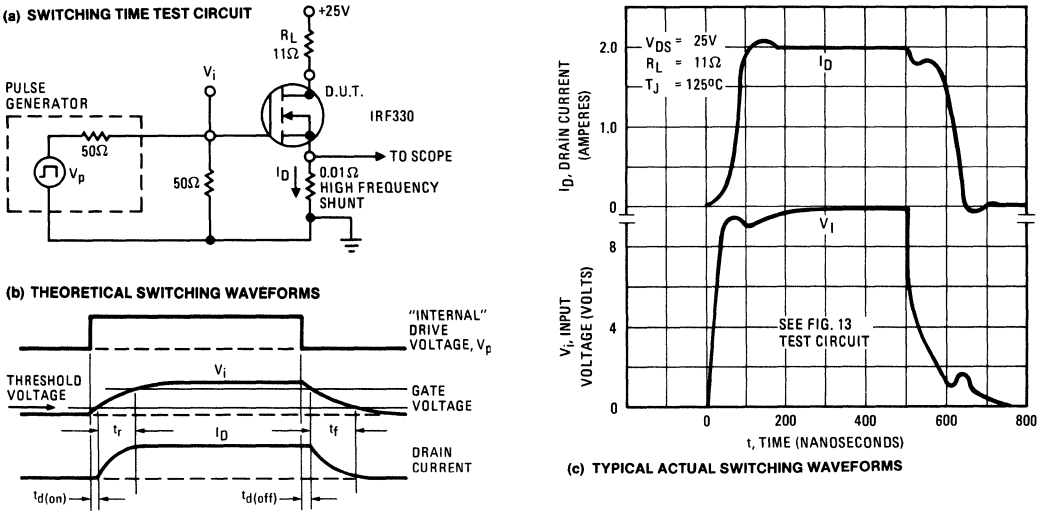


Figure 7. Switching the MOSFET

Switching Times

MOSFET power transistors are much faster than bipolar power transistors of comparable size, primarily because they do not have minority carrier delay times. The response times of MOSFETs are determined primarily by the device capacitances, and secondarily by such factors as the extremely short channel transit time of the electrons.

The input capacitance, C_{iss}, is the primary factor which determines the response time of a MOSFET. Although MOSFETs can be controlled by extremely low currents (i.e. high source impedances), the relatively long charge and discharge time of the input capacitance, C_{iss}, results in a tradeoff of response time against extreme sensitivity. A first order approximation of the response time of a MOSFET can be made by determining the time constant which results from the input capacitance times the effective source impedance.

Figure 7 shows typical switching waveforms of an IRF330 when driven by a 500 nanosecond-wide pulse. A good first order understanding of the switching response times $t_{d(on)}$, t_r, $t_{d(off)}$, and t_f, can be made by considering the power MOSFET an ideal switch with a 3 volt "on" threshold. The output current can be considered controlled, without delay, by the instantaneous gate voltage which, in turn, is controlled by the time constant formed by R_{input} x C_{iss}.

With these concepts in mind, the switching waveshapes of Figure 7(b) and the response times can be more easily understood. The turn-on delay, $t_{d(on)}$, is primarily the time for the transistor gate capacitance to be charged by the control signal to the threshold level of 3 volts maximum. The rise time, t_r, is the gate charging time required to drive from the threshold voltage, through the linear control region, to the gate voltage (typically 5 to 8 volts) required for full conduction of the drain current. In turn-off the procedure is reversed, and the turn-off delay time, $t_{d(off)}$, is primarily the time required for the gate capacitance to discharge from the gate overdrive saturation voltage (typically 10 volts) to the active gate control region (typically 5 to 8 volts). Finally, the fall time, t_f, is primarily the time delay required for the input capacitance to discharge through the active control region to the gate threshold voltage.

Figure 8 shows typical relationships for the IRF330 between the amplitude of the applied gate voltage signal, the turn off delay time, the fall time, and the rise time of the drain current, with the simple "resistive" gate drive circuit shown in Figure 7. Note that the turn off delay time increases with increasing gate drive, for the reasons already explained. The rise time of the drain current, on the other hand, decreases with increasing gate drive; this is because the higher the applied gate drive signal the faster the gate to source voltage reaches the level needed to support the drain current. The fall time of the drain current remains practically constant with applied gate drive; this is because the decay of the gate-to-source voltage below the point at which the drain current I_D can no longer be maintained, is practically independent of the amplitude of the applied gate signal.

Typical relationships between switching times and gate circuit re-

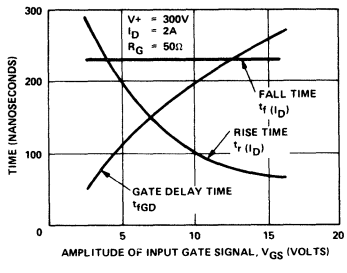


Figure 8. Typical relationships between Switching Times and Applied Gate Voltage (IRF330)

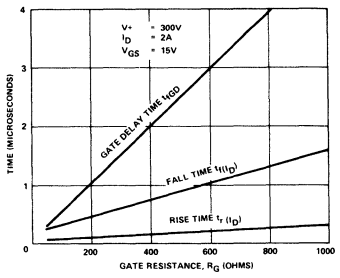


Figure 9. Typical relationships between Switching Times and Gate Circuit Resistance (IRF330)

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sistance are shown in Figure 9. Predictably, the higher the gate resistance, the longer the switching times, because of the longer time constant $R_G C_{iss}$.

Simple Capacitive Speed-Up Circuit

The alert designer will realise that circuit techniques for forcing the charge on C_{iss}, give a means of controlling the response time of the MOSFET, or alternatively the input impedance level at which a given response time occurs.

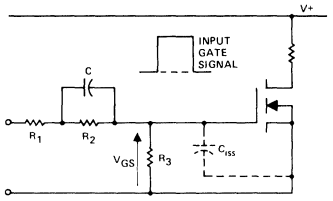


Figure 10. Gate Speed-up Circuit

Figure 10 shows a simple gate "speed-up" circuit. The circuit produces a significant reduction in the switching times, at the expense of the need for an increased amplitude of input gate signal, and an increased, (but still comparatively low) current drain on the drive source. When switching on, the capacitor C initially provides a low impedance path for the applied gate pulse, bypassing the resistor R_2, and thus the input capacitance C_{iss} of the MOSFET is rapidly charged. When switching off, the capacitor C is charged positively on its left-hand terminal; the charged capacitor forces a discharge current through the input capacitance of the MOSFET, thus making it switch off rapidly.

A point to remember about this gate speed-up circuit is that to be effective it does require an increase in the amplitude of the source signal voltage, because of the voltage dividing effect of R_3 with R_1 and R_2. Another point is that the resistor R_3 draws a continuous current from the gate drive source. Clearly it is desirable that the value of R_3 should be as high as possible. Figure 11 shows typical switching times for different values of R_3, for a given values of R_1, R_2 and C. It is seen that very fast switching times — in the order of 50 nanoseconds — can be obtained with the gate-to-source resistance R_3 as high as 10k Ohms. This represents a continuous current drain on the gate drive source of about 1mA. This is an order of magnitude lower than the drive current required for a comparably rated bipolar Darlington, which in any event exhibits switching times more than an order of magnitude longer.

Figure 12 shows typical relationships between the switching speeds of the IRF330 and the drain current, with and without a gate speed-up circuit. Note the drastic reduction in the turn off delay and fall times with the speed-up circuit, at drain current levels above 1A. The increase in the fall time at low levels of drain current is due to the drain-to-source capacitance, C_{oss}. The lower the drain current, the higher the load resistance R, and the greater the time constant RC_{oss}. A typical relationship between C_{oss} and drain to source voltage is shown in Figure 13.

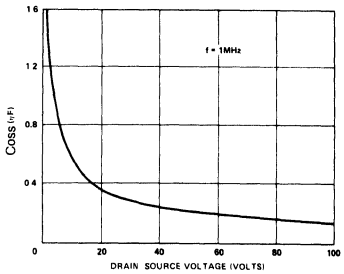


Figure 13. Typical relationships between Drain-Source Voltage and Drain-Source Self Capacitance (IRF330)

Simple external circuit techniques such as this can be used to obtain the fast switching speeds possible with power MOSFETs, yet maintain extremely high effective gain, thereby keeping complexity to a minimum. Power MOSFETs operating at many amperes and kilowatt power levels can commonly be driven directly from linear and digital IC components, whilst switching times still much faster than those of bipolar power transistors are easily achieved.

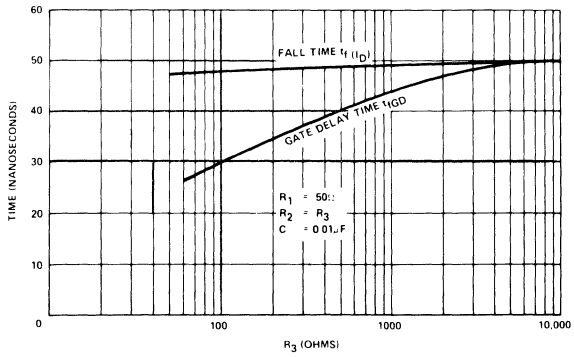


Figure 11. Values in Gate Speed-up Circuit and Switching Times (IRF330)

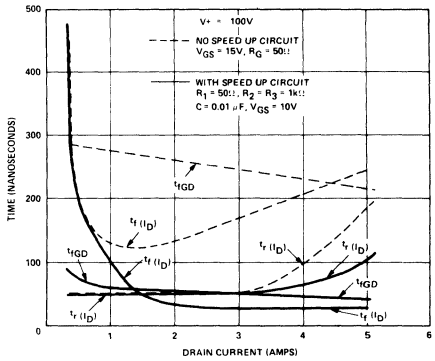


Figure 12. Typical relationships between Switching Times and Drain Current with and without Gate Speed-up Circuit (IRF330)

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Switching Times with an Inductive Load

So far we have considered the switching of the power MOSFET with a simple resistive load. In many applications the load during the switching interval will be essentially inductive, and it is often of more practical interest to the circuit designer to know the switching times with an inductive load. Figure 14 shows a simple circuit with a clamped inductive load; corresponding idealized switching waveforms are shown in Figure 15. Note that at switch-on the current first rises, then the voltage falls. At switch off the drain voltage rises, then the current falls. Note that this assumes that the load is sufficiently inductive that current flows continuously in it; through the MOSFET when it is switched on, and through the clamping diode when the MOSFET is switched off. It is also assumed that stray circuit inductance between the clamping diode and the MOSFET is negligible. Thus at switch on, load current that is already flowing in the clamping diode commutates into the MOSFET, and the transfer of this current is unrestricted by stray circuit inductance. In general this assumption for the switch on condition is somewhat pessimistic, but it can be approximated in certain circuits.

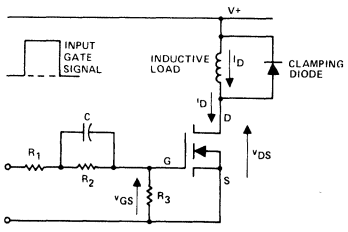


Figure 14. Simple circuit with Clamped Inductive Load

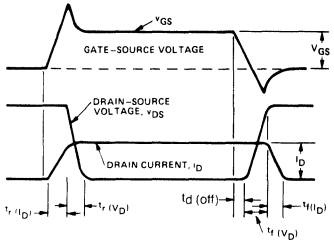


Figure 15. Idealized Switching Waveforms for Clamped Inductive Load

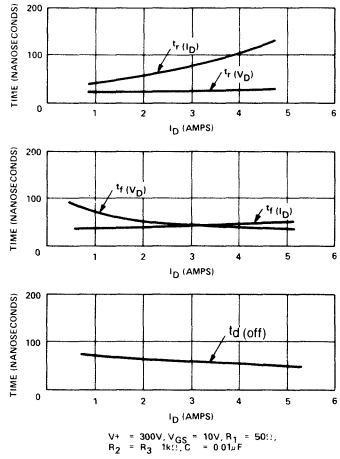


Figure 16. Typical relationships between Switching Times and Drain Current with Clamped Inductive Load and Gate Speed-up Circuit (IRF330)

Figure 16 shows typical relationships between the switching times and the drain current for a clamped inductive load with a gate speed-up circuit.

Maximum Operating Frequency

Because the switching times of the power MOSFET are very fast — at least an order of magnitude faster than those of comparably rated bipolar transistors — the energy dissipated during switching is very much lower, and the power MOSFET is able to operate at switching frequencies an order of magnitude or more higher.

Relationships between operating frequency and switching efficiency of the IRF330 power MOSFET with a resistive load, are shown in Figure 17. This data is based upon actual measured values of switching energy at a supply voltage of 300V, and a 50% duty cycle. Figure 17 takes account of the losses in the power MOSFET itself, and not of other components in the circuit; it does not therefore represent the overall circuit efficiency. Clearly, so far as the MOSFET itself is concerned, switching frequencies up to 500kHz or higher are quite feasible. The switching efficiency is defined as:

$$\text{Switching Efficiency} = \frac{\text{Power Input} - \text{MOSFET losses}}{\text{Power Input.}}$$

Safe Operating Area

One of the outstanding features of IR's power MOSFETs is that they do not display the second breakdown phenomenon which is frequently the Achilles heel of bipolar transistors. A simple physical explanation accounts for this superiority. If localized, potentially destructive, heating occurs within a MOSFET transistor, the carrier mobility in that area decreases. As a result the MOSFET has a positive temperature coefficient and acts in a self-protective manner by forcing currents to be uniformly distributed through the silicon die. In contrast a bipolar transistor, particularly under conditions of high collector-emitter voltage, displays

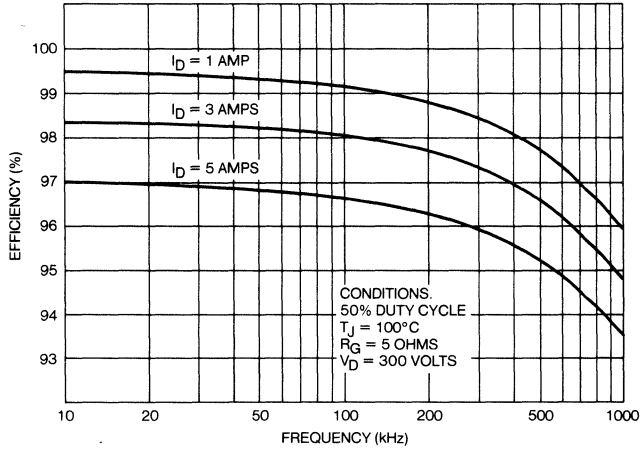


Figure 17. Switching Efficiency (IRF330)

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"current crowding" in the base region, which causes hot spots. Because of the bipolar's negative temperature coefficient, these hot spots tend to further "hog" the current and cause instantaneous, catastrophic destruction of the die.

As any power transistor circuit designer will know, the rated maximum power dissipation of the bipolar actually applies only over a very limited range of collector voltage, typically up to 10% of rated V_{CEO}. At higher voltages, the dc power dissipation is severely limited by second breakdown. Typically, at rated voltage the permissible power dissipation is only 5% of full rated power.

The Safe Operating Area of the IRF330 series MOSFET is shown as an example in Figure 18. Note that the DC current is limited throughout the voltage range only by the 75 watt power dissipation slope. There are no secondary slopes in the DC dissipation curve (or the pulse curve) that indicate the second breakdown limit commonly seen on bipolar Safe Operating Area curves. Note also the high values of pulse current and the corresponding long time periods for which the pulse power can be safely tolerated.

The IRF330, for example, can tolerate 0.375 amperes at 200 volts on a DC basis. By contrast, the popular 2N6545, a bipolar transistor with the same voltage rating, but double the continuous current rating, has only a 0.06 ampere DC second breakdown limit at 200 volts. At one millisecond pulse width and 300 volts, the IRF330 rates at 1.0 amperes versus only 0.45 amperes for the 2N6545.

The absence of second breakdown means that the power MOSFET is generally a much more rugged device than the bipolar transistor. This is extremely important, both for "linear" and "switching" applications.

The V_{DS} absolute maximum rating of MOSFETs should not be exceeded by allowing them to operate in the avalanche region. However, it is possible to reliably turn off high level inductive currents, which can generate high voltage inductive transients, by using a simple voltage clamp circuit. All of IR's MOSFETs have a clamped inductive rating such that the maximum rated pulse current can be turned off with a 100 microhenry inductor in series. Because MOSFETs are very fast devices, caution must be taken that the voltage clamp device has a sufficiently fast response, and that it is closely coupled to the drain-source terminals. A zener diode connected physically as close as possible to the drain and source terminals generally will provide acceptable voltage clamping.

The transconductance, g_{fs}, of a MOSFET is maximum at the highest allowable drain currents. In contrast, the DC gain, h_{FE}, of a bipolar transistor, decreases drastically at high collector currents. The high transconductance of MOSFETs at high currents, combined with the excellent SOA rating, result in MOSFETs being superb pulse amplifiers. All of IR's power MOSFETs have a pulsed current rating, I_{DM}, that is at least twice the continuous current rating, I_D. IR's power MOSFETs operate excellently in the pulse region as long as the allowable average power dissipation, safe operating area, and ±20 volt maximum gate voltage ratings are not exceeded.

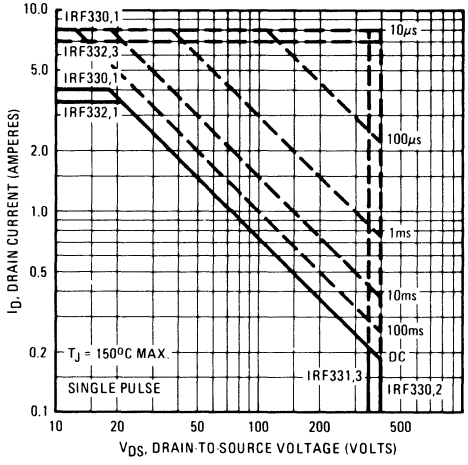


Figure 18. Maximum Safe Operating Area. (IRF330/333)

Temperature Stability

MOSFETs have outstanding gain and switching time stability with temperature variations, relative to the stability of typical bipolar transistors. The transconductance of IR Power MOSFETs typically varies less than ±20% from the 25°C value, over a −55°C to 125°C range. The DC current gain of a power bipolar commonly varies by a factor of 2 or 3 over this temperature range.

A rough comparison of the typical DC gain stability for an IR power MOSFET versus a power bipolar would yield a transconductance, g_{fs}, temperature coefficient of about −0.2% per °C versus a bipolar current gain, h_{FE}, temperature coefficient of about +0.8% per °C — a four-fold difference.

Reference to Figure 6 will show that the threshold voltage (bias point) and the transconductance (DC gain) move with temperature in compensating directions. Therefore, an operating point on the DC transfer characteristic maintains unusually good open loop stability. Drift-free operation becomes easy in a linear, closed loop system.

The switching time of IR power MOSFETs is essentially independent of operating temperature. This is a tremendous advantage relative to bipolar transistors, for which the 25°C switching times and associated power losses commonly increase by a factor of 2 or 3 at the higher actual operating temperatures. The extraordinary switching time stability of MOSFETs results because the response times are primarily dependent on the input capacitance, C_{iss}, which is essentially temperature invariant.

The on-resistance, $R_{D(ON)}$ of power MOSFETs, has a positive temperature coefficient, of approximately +0.7% per°C. This is an advantage in paralleling MOSFETs, and as has been seen it also accounts for their excellent safe operating area. However, in determining the on-state power losses in a switching mode, the increased value of $RD_{(ON)}$ at the actual maximum junction operating

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temperature must be used. Sufficient heatsink must always be used so that a thermal runaway situation cannot occur.

Paralleling

Power MOSFETs are easy to parallel, because the positive temperature coefficient forces current sharing among the paralleled devices. Current sharing resistors, with their associated power losses, are not necessary. Some resistance in series with the gates (typically 100 ohms) and close paralleled lead connections may be necessary to assure that the good high frequency response of the MOSFETs does not cause oscillations.

MOS Caution

The ±20 volt absolute maximum gate voltage rating of IR power MOSFETs should never be exceeded, or permanent damage can occur.

Zener diode protection should be used if there is a danger of transient gate overvoltages. This caution applies also to the buildup of static charge. IR power MOSFETs have large gate capacitances and thick oxide layers relative to low level MOS devices, where static charge damage can be particularly dangerous. Though significantly more rugged than such low level MOS devices, reasonable precautions which are normally taken in handling MOS devices should be observed until the installation of MOSFETs in a circuit.

APPLICATIONS

Power MOSFETs offer tremendous operating advantages over conventional bipolar transistors, and they will undoubtedly replace bipolars in many existing applications. In order to take full advantage of their unique operating features, and thus to produce an optimum overall system design, it will almost never be sufficient merely to make a one-for-one replacement of a bipolar with a MOSFET in an otherwise unmodified circuit. The much lower drive requirement of the MOSFET will usually mean that very significant simplifications can be made in the drive circuitry; the vastly superior switching speed will offer the possibility for lower losses, or higher operating frequency, or both; and the superior safe operating area will offer greater loading and overloading capability, and minimization or elimination of protective snubber components.

Many potential applications of Power MOSFETs are obvious, and are already being actively pursued by circuit development engineers throughout the world. A great number of as yet unexplored applications will surely emerge, as the unique advantages of IR's power MOSFETs become more widely understood, and as power MOSFET technology itself develops and matures.

In the following sections we will briefly review some of the most obvious application areas. This may help to stimulate the imagination of the reader to perceive new applications for power MOSFETs in his own particular field of expertise.

Switching Power Supplies

Switching DC power supplies are rapidly replacing conventional 50 or 60Hz transformer/rectifier supplies. The basic principle of the switching power supply is illustrated in Figure 19. This switching scheme by comparison with the conventional line frequency power supply, offers smaller overall size, due to much smaller transformer and smoothing components, faster response, better regulation, and higher efficiency.

Switching power supplies presently use bipolar transistors, and usually operate in the 20-35 kHz frequency range. Higher operating frequencies are not generally practical, because bipolar switching times are too long. From the system viewpoint, an increase in the switching frequency to 200 kHz or higher would offer the possibility for further reductions in size, weight, and response time. Such high operating frequencies now become a practical reality, with the availability of IR's power MOSFETs. Other potential advantages would be elimination of electrolytic capacitors, smaller EMI filters, and simplified drive and snubber circuits.

The MOSFET also offers advantages in the existing 20 to 30 kHz range, in terms both of reduced overall losses, because of reduced switching losses, and reduced circuit complexity, because of the minimal gate drive requirement.

Audio Amplifiers

The power MOSFET offers a quite linear input to output transfer characteristic. This means that with appropriate biasing it can be used as a simple high quality audio amplifier, illustrated in a simplified form in Figure 20.

The excellent Safe Operating Area of power MOSFETs make them particularly well suited for class B amplifiers, which require extreme low fre-

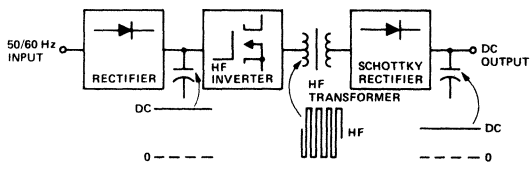


Figure 19. Basic Principle of Switching Power Supply

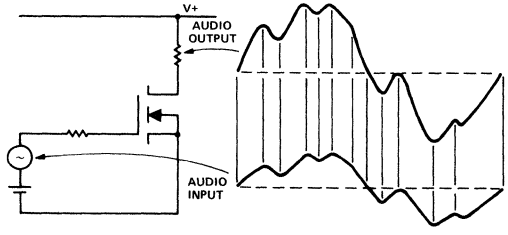


Figure 20. Basic Principle of Audio Amplification using Power MOSFET

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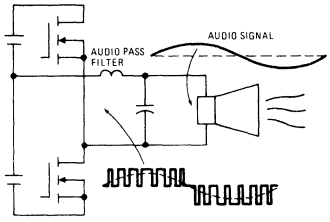


Figure 21. Class D Audio Amplifier — Basic Principle

quency response at high power levels. The wide MOSFET bandwidth makes good high frequency response of the amplifier easy.

Another type of audio amplifier uses the class D pulsewidth modulation principle, illustrated diagrammatically in Figure 21. Implementation of this type of amplifier with bipolar transistors has not generally been successful, because the carrier frequency must be much higher than the audio frequency to produce a good quality output. The relatively long switching times of the bipolar are a fundamental limitation. With the availability of IR's power MOSFETs, these limitations are eliminated. This type of approach offers the possibility for an audio amplifier of extremely high efficiency, small size, and high fidelity.

Motor Speed Control

The use of bipolar transistors for speed control of both DC and AC motors is taking a firm hold in the marketplace, for power ratings up to several tens of horsepower. Basic chopper and inverter schemes for motor speed control using power MOSFETs are shown in Figure 22. The use of variable frequency DC to AC inverters, for efficient control of the speed of AC induction motors is becoming particularly topical in view of the present day emphasis on energy saving techniques.

In these circuits the switching frequency typically will be in the range of a few hundred Hz, to a few kHz. This, of course, is well within the capability of bipolar transistors. MOSFETs can however offer significant advantages, because of their substantially reduced drive power requirements, and improved safe operating area and ruggedness. These features will result in simplification of peripheral circuitry, improved reliability, and improved response time.

The ease of paralleling power MOSFETs for higher power output is also an important advantage, whilst the somewhat higher conduction voltage drop and hence higher power loss of the MOSFET is but a slight disadvantage — more theoretical than practical. The extra heatsink required to accommodate the greater power dissipation of the MOSFET is minimal indeed, and is greatly outweighed by the advantages to be gained.

AM Transmitters

Conventional AM broadcasting transmitters operate in the 0.5 to 1.6 MHz range. They use vacuum tubes, which are relatively bulky and unreliable. Newer designs are using parallel connected bipolar transistors.

Typically an AM transmitter using bipolars requires about 60 devices, for each kilowatt of output power. The high operating frequency pushes the limits of bipolar operation, paralleling is difficult, and the required reliability is not easy to achieve.

Power MOSFETs are capable of operation within the required frequency range, and are easily parallelable. The total number of devices would be drastically reduced; for example 8 IRF350's would be needed for each kilowatt of output power, as compared to 60 bipolar transistors. Another advantage of the MOSFET system would be that it is able to handle mismatch and fault conditions, and the driver stages would be much simpler. A basic schematic of an AM transmitter using power MOSFETs is shown in Figure 23.

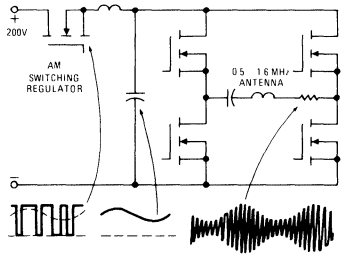


Figure 23. AM Transmitter — Basic Principle

Induction Heating

The heating of metal by energizing an induction coil that couples magnetic flux and induces a flow of eddy current into the work piece is an established principle, that is widely used throughout industry. It is an efficent, clean and cost effective means of melting, heating, hardening, annealing and welding of metals.

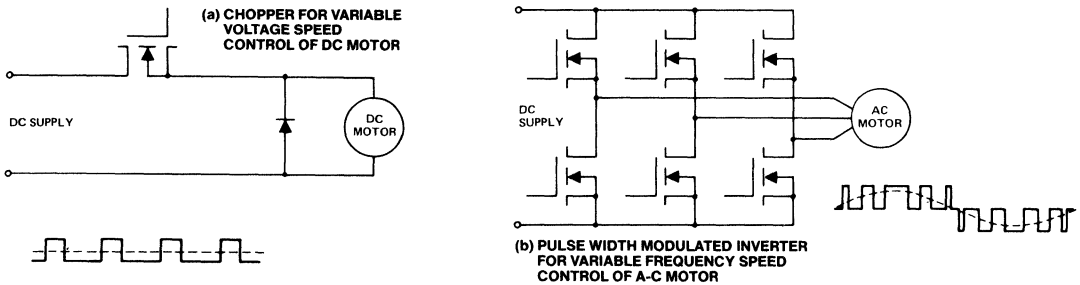


Figure 22. Basic schemes for Variable Speed Control of DC and AC Motors using Power MOSFETs

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Induction heating systems cover a wide range of frequencies, starting at line frequency and progressing up to around 500kHz. The lower frequency ranges, up to 20kHz or so, today are generally covered by variable frequency thyristor inverters, which have now largely replaced the older fixed frequency rotating generator sets.

Power levels of induction heating equipment extend up to several megawatts at the lower end of the frequency spectrum. As the required frequency increases, generally the power requirement decreases.

For frequencies in the 100 to 500kHz range vacuum tube oscillators, with ratings from a few kilowatts upwards, are presently the normal means of producing the required frequency. These are not too efficient, typically about 60%, they are quite large, and they require periodic maintenance.

The availability of IR's power MOSFETs offers the opportunity for realising efficient, compact and reliable solid state RF induction heating generators at the required power ratings, at frequencies up to 500kHz.

Another use of induction heating that has been proposed is in domestic cooking. Heating currents are induced from an induction coil directly into the cooking utensil. This technique offers dramatic improvements in efficiency and response time.

Commercial exploitation of this principle has not so far generally been successful, primarily because of the complexity of the required high frequency inverter circuitry. The availability of IR's power MOSFETs makes possible a complete reappraisal of the induction cooker.

High Frequency Welding

Modern DC power supplies use high frequency switching techniques to obtain greater compactness, improved efficiency and faster response. This very same switching technique is also applicable to DC welding supplies. These traditionally use a bulky mains frequency transformer, often a ballast impedance to obtain the required output regulation, and an output rectifier to provide the required DC.

Figure 24 shows a basic schematic of a possible high frequency welding system using power MOSFETs. IR's power MOSFETs can deliver several kilowatts of power at frequencies well above the audio range; this type of scheme would provide a compact, portable, silent, efficient welder, with fast response and excellent controllability.

Fluorescent Lighting

Conventional mains frequency fluorescent lighting requires bulky inductive ballasting and power factor capacitors, and is relatively inefficient. It is well known that by using high frequency to supply the fluorescent tube, power consumption for a given light output can be reduced by 30 to 35%, whilst tube life can be substantially increased, and bulky ballast components are eliminated.

• Fluorescent lighting schemes using high frequency bipolar transistor inverters are presently used in applications such as transportation and emergency lighting systems.

Application of high frequency techniques to the general consumer market has so far been inhibited by the relative complexity of the drive circuitry required for the bipolar transistor. IR's power MOSFETs with their extremely simple drive requirements are potentially ideal for this application.

A basic schematic of a high frequency fluorescent lighting scheme using MOSFETs is shown in Figure 25.

Other Applications

The applications discussed above are just a few of the many potential uses of IR's power MOSFETs. Other immediate application areas are high frequency generators for diathermy, drivers for high power bipolar transistors and thyristors, pulsewidth modulated high current supplies for spark erosion, beam control of video displays for computer terminals, and VLF and HF generators.

Summary

Power MOSFETs have numerous operating characteristics which are distinctly superior to those of power bipolar transistors. These superiorities occur because MOSFETs have fundamentally different operating principles. Understanding the operating principles and superiorities of MOSFETs will allow the creative designer to make fundamental improvements in many types of transistorized products, as well as to innovate entirely new types of product.

The introduction of IR HEXFETs — the world's most advanced form of power MOSFETs — further underscores the importance of MOSFET technology for the circuit designs of the future. □

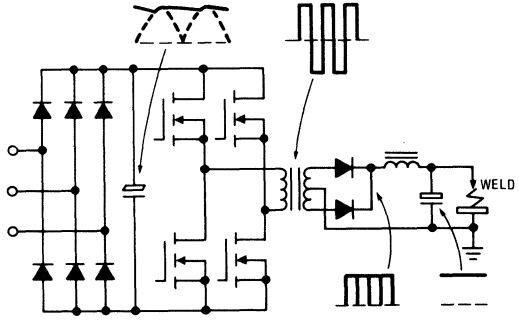


Figure 24. HF Welding System — Basic Principle

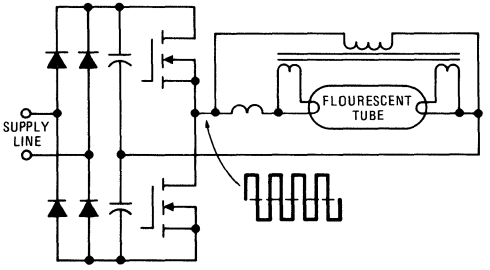


Figure 25. HF Lighting System — Basic Principle

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The Do's and Don'ts of Using Power HEXFETs®

By BRIAN R. PELLY

Summary

In common with all power semiconductor devices, power MOSFETs have their own technical subtleties, which must be properly understood if the designer is to get the most out of them. In this article, some of the most common "Do's and Don'ts" of using power HEXFETs are explained.

Introduction

Power HEXFETs offer many advantages over conventional bipolar transistors, in both linear and switching applications. These advantages include very fast switching, absence of second breakdown, wide safe operating area, and extremely high gain. Typical applications are high frequency switching power supplies, chopper and inverter systems for DC and AC motor speed control, high frequency generators for induction heating, ultrasonic generators, audio amplifiers, AM transmitters, computer peripherals, telecommunications equipment, and a host of special military and space needs.

There are several basic types of power MOSFETs available. Original designs used so-called V-groove or U-groove structures, while the trend today is towards vertical D-MOS technology, with a closed cellular source configuration. This technology was first embodied in the HEXFET structure, shown in Figure 1.

Current flows vertically through the silicon from the drain, through the body of the device, then horizontally through the channel region, and vertically out of the source, as illustrated. The flow of transistor current is controlled by the voltage applied between the gate and source terminals; the applied gate voltage sets up a field in the channel region, which modulates the resistance of the device. The gate is isolated electrically from the body; as a result, the power HEXFET has a very high, almost infinite, DC gain.

A feature of power MOSFETs is that they inherently have built into them an integral reverse body-drain diode. The existence of this diode is explained by reference to Figure 1. When the source terminal is made positive with respect to the drain, current can flow through the middle of the source cell, across a forward biased P-N junction. In the "reverse" direction, the power HEXFET thus behaves like a P-N junction rectifier. The integral body-drain diode is a real circuit element, and its current handling capability is typically as high as that of the transistor itself. Some circuits require an "inverse" rectifier to be connected across the switching device, and in these circuits it will often be possible to utilize the body-drain diode of the HEXFET, provided the proper precautions are taken.

In this application note, some of the most common do's and don'ts of using power HEXFETs are described. The objective is to help the user get the most out of these remarkable devices, while reducing "on the job" learning time to a minimum.

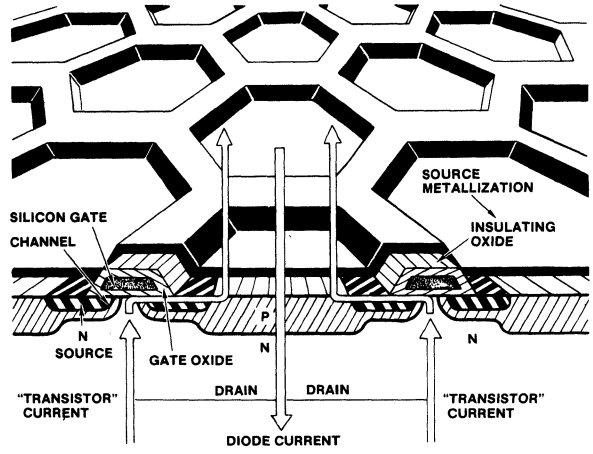


Figure 1. Basic HEXFET Structure

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Be Careful When Handling & Testing Power HEXFETs

The user's first "contact" with the power HEXFET could be a package of parts arriving on his desk. Even at this stage, it behooves one to be knowledgeable about some elementary precautions.

Power HEXFETs, being MOS devices, can potentially be damaged by static charge when handling, testing or installing into a circuit. The problem is rather slight by comparison with that experienced with low level MOS devices. Power HEXFETs are, after all, *power* devices; as such, they have much greater input capacitance, and are much more able to absorb static charge without excessive build-up of voltage. In order to avoid possible problems, however, the following procedures should be followed as a matter of good practice, wherever possible:

- HEXFETs should be left in their anti-static shipping bags, or conductive foam, or they should be placed in metal containers or conductive tote bins, until required for testing or connection into a circuit. The person handling the device should ideally be grounded through a suitable wrist strap, though in reality this added precaution is seldom essential.
- HEXFETs should be handled by the package, not by the leads.

When checking the electrical characteristics of the power HEXFET on a curve tracer, or in a test circuit, the following precautions should be observed:

- Test stations should use electrically conductive floor and table mats that are grounded. Suitable mats are available commercially.
- When inserting HEXFETs into a curve tracer or a test circuit, voltage should not be applied until all terminals are solidly connected into the circuit.
- When using a curve tracer, a resistor should be connected in series with the gate to damp spurious oscillations that can otherwise occur on the trace. A suitable value of resistance is 100 ohms.
- For repeated testing, it is convenient to build this resistor into the test fixture.
- When switching from one test range to another, voltage and current settings should be reduced to zero, to avoid the generation of potentially destructive voltage surges during switching.

The next step is to connect the power HEXFET into an actual circuit. The following simple precautions should be observed:

- Work stations should use electrically grounded table and floor mats.
- Soldering irons *should be grounded.*

Now that the power HEXFET has been connected into its circuit, it is ready for the power to be applied. From here on, success in applying the device becomes a matter of the integrity of the circuit design, and of what circuit precautions have been taken to guard against unintentional abuse of the HEXFET's ratings.

The following are the interrelated device and circuit considerations that lead to reliable, trouble-free design.

Beware of Unexpected Gate-to-Source Voltage Spikes

Excessive voltage will punch through the gate-source oxide layer and result in permanent damage.

This seems obvious enough, but it is not so obvious that transient gate-to-source overvoltages can be generated that are quite unrelated to, and well in excess of, the amplitude of the applied drive signal. The problem is illustrated by reference to Figure 2.

If we assume that the impedance, Z, of the drive source is high, then any positive-going change of voltage applied across the drain and source terminals (caused, for example, by the switching of another device in the circuit) will be reflected as a positive-going voltage transient across the source and the drain terminals, in the approximate ratio of:

$$\frac{1}{1 + \frac{C_{gs}}{C_{dg}}}$$

The above ratio is typically about 1 to 6. This means that a change of drain-to-source voltage of 300V, for example, could produce a voltage transient approaching 50V between the gate and source terminals. This calculation is based upon the worst case assumption that the transient impedance of the drive circuit is high by comparison with the gate-to-source capacitance of the HEXFET. This situation can, in fact, be quite easily approximated if the gate drive circuit contains inductance — for example, the leakage inductance of an isolating drive transformer. This inductance exhibits a high impedance for short transients, and effectively decouples the gate from its drive circuit for the duration of the transient.

The positive-going gate-to-source voltage transient produced under the above circumstances is undesirable because it may exceed the gate voltage rating of the device, causing permanent damage; moreover, it tends to turn the device ON "unintention-

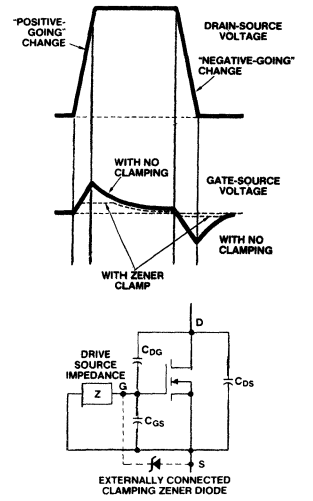


Figure 2. A Rapidly Changing Applied Drain-Source Voltage will Produce Gate-Source Voltage Transients

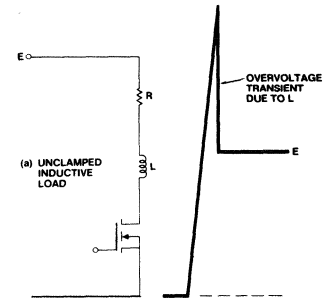


Figure 3. Drain-Source Overvoltage Transient when Switching Off with Unclamped Inductive Load

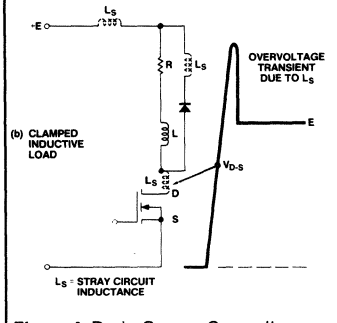


Figure 4. Drain-Source Overvoltage Transient Produced by Stray Circuit Inductance When Switching Off with Clamped Inductive Load

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ally", causing transient current overloading of this and other devices in the circuit.

It is, of course, true that since the applied drain transient results in a voltage at the gate which tends to turn the HEXFET device ON, the overall effect is to an extent self-limiting so far as the gate voltage transient is concerned. Whether this self-limiting action will prevent the voltage transient at the gate from exceeding the gate-source voltage rating of the device depends upon the impedance of the external circuit. Spurious turn-on is of itself undesirable, of course, though in practical terms one may grudgingly be able to accept this circuit operating imperfection, provided the safe operating area of the device is not violated.

As a minimum solution to the problem, the gate-source terminals must be provided with a voltage clamp (a conventional zener diode is suitable for this purpose) to prevent the gate-source voltage rating from being exceeded. A more fundamental solution, of course, is to make the impedance of the gate circuit low enough that not only is the gate-source voltage rating not exceeded, but also the voltage transient at the gate is contained to a level at which spurious turn-on does not occur.

It should be remembered that a collapse of voltage across the HEXFET (i.e., a negative-going dv/dt) will produce a transient negative voltage spike across the gate-source terminals. In this case, of course, there will be no tendency for the device to turn ON, and hence no tendency for the effect to be self-limiting. A zener diode connected to clamp positive transients will automatically clamp negative-going transients, limiting them to the forward conduction voltage drop of the zener.

Beware of Drain-Source Voltage Spikes Induced by Switching

The uninitiated designer is often not aware that self-inflicted overvoltage transients can be produced when the device is switched OFF, even though the DC supply voltage for the drain circuit is well below the V_{DS} rating of the HEXFET.

Figure 3 shows how a voltage spike is produced when switching the device OFF, as a result of inductance in the circuit. The faster the HEXFET is switched, the higher the overvoltage will be. Inductance is always present to some extent in a practical circuit, and therefore, there is always danger of inducing overvoltage transients when switching OFF. Usually, of course, the main inductive component of the load will be "clamped", as shown in Figure 4. Stray circuit inductance still exists, however, and overvoltage transients will still be produced as a result — to say nothing of the fact that the clamping diode may not provide an instantaneous clamping action, due to its "forward recovery" characteristic.

The first approach to this problem is to minimize stray circuit inductance, by means of careful attention to circuit layout, to the point that whatever residual inductance is left in the circuit can be tolerated. If the device has an inductive energy rating, use can be made of this rating for this situation. Generally, however, such ratings do not yet exist for power HEXFETs, and a clamping device should be connected, physically as close as possible to the drain and source terminals, as shown in Figure 5. A conventional zener diode, or a "transorb" clamping device, are satisfactory for this purpose. An alternative clamping circuit is shown in Figure 6. The capacitor C is a reservoir capacitor and charges to a substantially constant voltage, while the resistor R is sized to dissipate the "clamping energy" while maintaining the desired voltage across the capacitor. The diode D must be chosen so that its forward recovery characteristic does not significantly spoil the transient clamping action of the circuit.

A simple RC snubber can also be used, as shown in Figure 7. Note, however, that an RC snubber not only limits the peak voltage, it also slows down the effective switching speed. In so doing, it absorbs energy during the whole of the switching period, not just at the end of it, as does a voltage clamp. A snubber is therefore less efficient than a true voltage clamping device.

Note that the highest voltage transient occurs when switching the highest level of current. The waveform of the voltage across the HEXFET should be checked with a high-speed oscilloscope at the full load condition to ensure that switching voltage transients are within safe limits.

Do Not Exceed the Peak Current Rating

All HEXFETs have a specified maximum peak current rating. This is conservatively set at a level that guarantees long-term reliability, and it should not be exceeded.

It is often overlooked that peak transient currents can be obtained in a practical circuit that are well in excess of the expected normal oper-

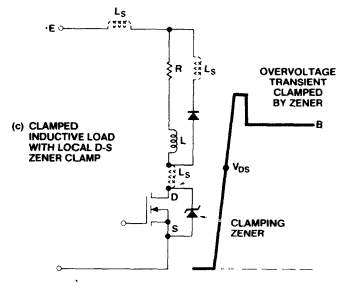


Figure 5. Overvoltage Transient at Switch-Off Clamped by Local Drain-Source Zener

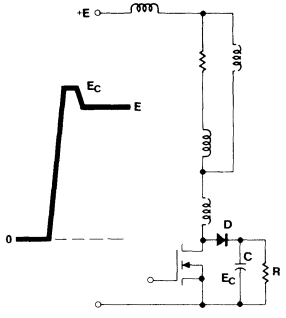


Figure 6. Overvoltage Transient at Switch-Off Limited by Local Diode-Capacitor-Resistor Clamp

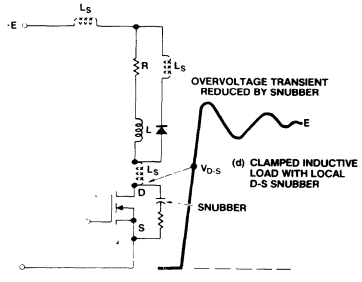


Figure 7. Overvoltage Transient at Switch-Off Limited by Local Capacitor-Resistor Snubber

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ating current, unless proper precautions are taken. Heating, lighting and motor loads, for example, consume high in-rush currents if not properly controlled. A technique that ensures that the peak current does not exceed the capability of the HEXFET is to use a current sensing control that switches OFF the HEXFET whenever the current instantaneously reaches a preset limit.

Unexpectedly high transient current can also be obtained as a result of rectifier reverse recovery, when a HEXFET is switched ON rapidly into a conducting rectifier. This is illustrated in Figure 8. The solution is to use a faster rectifier, or to slow down the switching of the HEXFET to limit the peak reverse recovery current of the rectifier.

Do Not Operate at an RMS Current In Excess of the Rating

All HEXFETs have a maximum continuous direct current rating, I_D. The internal bonding wires, bonding pads, and source metallization of the HEXFET are designed to carry this rated current continuously. The total continuous RMS current handled by the HEXFET should not exceed the I_D rating. This means that in a switching application, for example, if the peak current is I_{PK}, and the duty cycle is D, as illustrated in Figure 9, then the maximum permissible value of I_{PK} is $I_D/\sqrt{D}$, so long as this value is less than the $I_{D(max)}$ rating.

Stay Within the Thermal Limits

The power HEXFET, being a power device, is thermally limited. It must be mounted on a heatsink that is adequate to keep the junction temperature within the rated $T_{J(max)}$ (150° C) under the "worst case" condition of maximum power dissipation and maximum ambient temperature.

It must be remembered that in a switching application, the total power is due to the conduction loss and the switching loss. Switching time and hence switching losses are essentially independent of temperature, but the conduction losses increase with increasing temperature, because $R_{D(on)}$ increases with temperature. This must be taken into account when sizing the heatsink. The required thermal resistance of the heatsink can be calculated as follows:

The transistor conduction power, P_T, is given approximately by:

$P_T = I_T^2 R_{D(on)} [1 + 0.007 (\Delta T_{JA} + T_A - 25)]$

where I_T = RMS value of "transistor current"

$R_{D(on)}$ = ON resistance at 25° C

T_A = ambient temperature - °C

ΔT_{JA} = temperature rise, junction-to-ambient

The term within the brackets [ ] accounts for the typical 0.7% increase in $R_{D(on)}$ per degree C temperature rise above 25° C. The data sheet can be consulted for a more accurate value of temperature coefficient for any specific device.

The switching energy depends upon the voltage and current being switched and the type of load. The total switching loss, P_S, is the total switching energy, ϵ_T, multiplied by the operating frequency, f. ϵ_T is the sum of the energies due to the individual switchings that take place in each fundamental operating cycle.

$$P_S = \epsilon_T \cdot f$$

The total power dissipation is the sum of the conduction power, P_T, and the switching power, P_S.

$$P = P_T + P_S$$
$$= I_T^2 R_{D(on)} [1 + 0.007 (\Delta T_{JA} + T_A - 25)] + P_S$$

Since:

$$\Delta T_{JA} = P R_{JA}$$

where:

R_{JA} = junction-to-ambient thermal resistance

The required value of R_{JA} for a given value of ΔT_{JA} is given by:

$$R_{JA} = \frac{\Delta T_{JA}}{I_T^2 R_{D(on)}[1+0.007(\Delta T_{JA}+T_A-25)]+P_S}$$

The junction-to-ambient thermal resistance, R_{JA}, is made up of the internal junction-to-case thermal resistance, R_{JC}, plus the case-to-heatsink thermal resistance, R_{CS}, plus the sink-to-ambient thermal resistance, R_{SA}. The first two terms are fixed for the device, and the required thermal resistance of the heatsink, R_{S-A}, for a given junction temperature rise ΔT_{J-A}, can be calculated from:

$$R_{S-A} = R_{J-A} - (R_{JC} + R_{C-S})$$

Pay Attention to Circuit Layout

Stray inductance in the circuit can cause overvoltage transients, slowing down of the switching speed, unexpected unbalance of current between parallel connected devices, and unwanted oscillations.

In order to minimize these effects, stray circuit inductance must be minimized. This is done by keeping conduction paths as short as possible, by minimizing the area of current loops, by using twisted pairs of leads, and

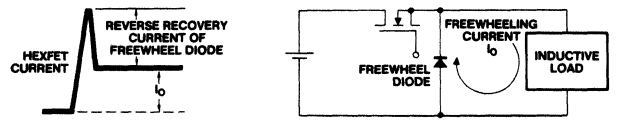


Figure 8. Switching on the HEXFET into a Conducting Rectifier Can Result in High Peak Current, due to Reverse Recovery of Rectifier.

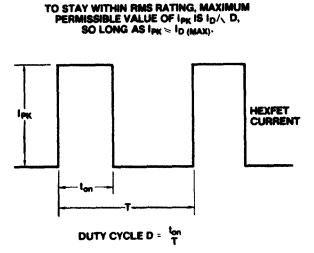


Figure 9. To Stay Within I_D RMS Rating, Maximum Permissible Value of I_{PK} is $I_D/\sqrt{D}$, so long as $I_{PK} \leq I_{D(max)}$.

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by using ground plane construction. Local decoupling capacitors alleviate the affects of any residual circuit inductance, once these measures have been taken.

Circuit layout should be kept as symmetrical as possible in order to maintain balanced currents in parallel connected HEXFETs. The gates of parallel connected devices should be decoupled by small ferrite beads placed over the gate connections, or by individual resistors in series with each gate. These measures prevent parasitic oscillations.

Be Careful When Using the Integral Body-Drain Diode

The HEXFET's integral body-drain diode exhibits minority carrier reverse recovery. Reverse recovery presents a potential problem when switching any rectifier off; the slower the rectifier, the greater the problem. The HEXFET's rectifier is relatively fast — not as fast as the fastest discrete rectifiers available, but considerably faster than comparably related conventional general purpose rectifiers. By comparison with the HEXFET itself, on the other hand, the switching speed of the integral reverse rectifier is quite slow. The switching speed of a circuit which utilizes the body-drain diode of the HEXFET may therefore be limited by the rectifier. Whether this will be so depends upon the circuit and the operating conditions.

The most common applications of the HEXFET in which the switching speed, and hence frequency, will potentially be limited by the rectifier, are DC to DC choppers, and inverters for regulated power supplies, electric motor controllers, and so on, in which "multiple" voltage pulses are used. Fortunately, these applications generally do not require ultra-fast switching, and hence they can tolerate the reverse recovery characteristic of the rectifier.

Regardless of the overall circuit configuration, or the particular application, the "local" circuit operating situation that is troublesome occurs when the freewheeling current from an inductive load is commutated from the integral rectifier of one HEXFET to the transistor of an "opposite" HEXFET, the two devices forming a tandem series connected pair across a low impedance voltage source, as shown in Figure 10. This "local" circuit configuration occurs in most chopper and inverter schemes.

If the incoming HEXFET switches ON too rapidly, the peak reverse recovery current of the integral body-drain diode of the opposite HEXFET will rise too rapidly, the peak reverse recovery current rating will be exceeded, and the device may possibly be destroyed.

The peak reverse recovery current of the rectifier can be reduced by slowing down the rate of change of current during the commutation process. The rate of change of current can be controlled by purposefully slowing down the rate of rise of the gate driving pulse. Using this technique, the peak current can be reduced to almost any desired extent, at the expense of prolonging the high dissipation switching period. The oscillograms in Figure 11 illustrate the effect. By slowing the total switch-ON time from 300ns to 1.8μs, the peak current of the IRF330 has been decreased from 20A to 10A. The energy dissipation associated with the "unrestrained" switch-ON in Figure 11(a) is 0.9mJ, whereas it is 2.7mJ for the controlled switch-ON of Figure 11(b). Note, however, that the average switching losses at a switching frequency of, say 5kHz, are quite manageable — 4.5W and 13.5W for Figures 11(a) and 11(b), respectively.

Note also that it is not necessary to slow the switching-OFF of the HEXFET, hence the energy dissipation at switch-OFF will be relatively small by comparison with that at switch-ON. For operation at frequencies up to a few kHz, where ultra-fast switching is not mandatory, slowing the applied gate drive signal to reduce the peak reverse recovery current of the "opposite" rectifier offers a good practical solution.

Be On Your Guard When Comparing Current Ratings

The user can be forgiven if he assumes that the continuous drain current rating, I_D, that appears on the data sheet represents the current at which the device can actually be operated continuously in a practical system. To be sure, that's what it should represent; unfortunately it often does not.

Most manufacturers assign a "continuous" current rating to the device which in practical terms cannot be used, because the resulting conduction power dissipation would be so large as to require a heatsink with an impractically low thermal resistance, and/or an impractically low ambient operating temperature.

Table 1 is an illustration of the present lack of standardization of current ratings amongst different MOSFET manufacturers. The devices with higher ON-resistance are seen to have generally higher current ratings assigned to them than the lower ON-resistance parts — a tra-

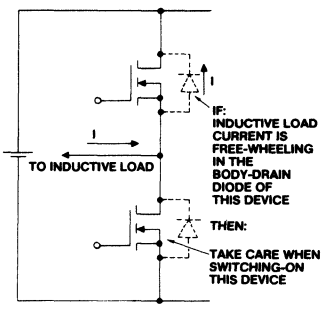
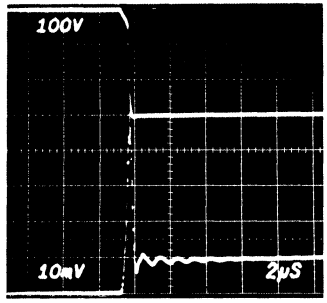
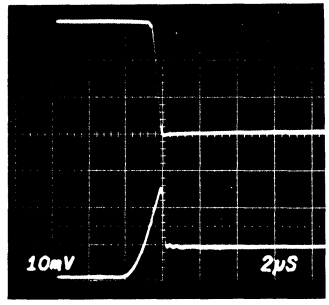


Figure 10. Local Circuit Configuration and Operating Condition Requiring Special Care When Using the HEXFET's Integral Body-Drain Diode.



(a) $I_{(max)}$ = 20A, di/dt = 50A/μs. Switching time = 300 nsec.



(b) $I_{(max)}$ 20A, di/dt = 50A/μs. Switching time 1.8μs.

Figure 11. Oscillograms of IRF330 Switching into Reverse Rectifier of Another IRF330 with Freewheeling Current of 4A.
Top Trace: Voltage 100V/div.
Bottom Trace: Current 4A/div.
Time Scale: 2μs/div.

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vesty of the "correct" situation that would, and should, exist if all types of given chip size and junction-to-case thermal resistance were rated on the basis of a given power dissipation.

The best advice to the user is to compare different types *on the basis of ON-resistance,* and not of I_D rating. Fortunately, all manufacturers specify $R_{D(on)}$ at 25° C, and this provides a common basis for comparison. This parameter, taken in conjunction with the junction-case thermal resistance (which, unfortunately, not all manufacturers specify), is a much better indication of the HEXFET's true current handling capability.

Table 1. Comparison of Different Manufacturers' Practices for Assigning Current Ratings (All Parts are Rated 400V)

Device Type	$R_{D(on)}$ Ohms	I_D Amps	$R\theta_{j-c}$ °C/W	Calculated $T_{C(max)}$ Applicable to I_D °C
IRF330	1.0	4	1.67	90
MTP565	1.5	5	1.67	25
HPWR6504	1.0	5	1.39	80
VN4001A	1.5	8	?	<25 ?
VN0340B1	1.5	8	?	<25 ?

Conclusions

Power HEXFETs have many advantages. When properly applied they yield an overall system design that frequently has fewer components, is lighter and more compact, and has better performance than can be obtained with other types of devices.

In common with all power semiconductors, power HEXFETs do have their own little technical subtleties. If these subtleties are properly understood, the potential pitfalls can be easily overcome, at minimal cost — and potentially great reward. □

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Current Ratings, Safe Operating Area, and High Frequency Switching Performance of Power HEXFETs®

By S. CLEMENTE, B.R. PELLY, R. RUTTONSHA

Summary

This application note discusses the current handling capability, safe operating area, and power dissipation of a HEXFET power MOSFET. It is shown that the HEXFET's ability to carry current is essentially limited only by junction heating, both for the "switched" and "linear" modes of operation — unlike the bipolar transistor, which is limited by gain and second breakdown. For this reason, peak current ratings of HEXFETs are phenomenally high by comparison with those of bipolar transistors.

Examples are given which show how the HEXFET's current carrying ability can be utilized, and how the power dissipation of a HEXFET compares with that of a fast switching bipolar transistor, as a function of operating frequency.

Introduction

International Rectifier HEXFETs are well established in a variety of applications which previously have been served by bipolar transistors, and are continuing to find many new applications. Designers who are familiar with the practical derating factors that need to be applied when designing with bipolar transistors frequently do not realize that the criteria for determining HEXFET ratings are quite different, and as a result often select a HEXFET which is oversized for the job. This can have a significant bearing on the cost effectiveness of the design.

The purpose of this application note is to explain the basis of the current ratings and Safe Operating Area (SOA) of power HEXFETs, and thus enable the user to make a properly informed choice of HEXFET for his particular application.

A practical comparison of the power losses of a HEXFET and a bipolar transistor is also given. Whereas the conduction losses of a bipolar are generally lower than those of the HEXFET, the switching losses are significantly higher. Base drive power for the bipolar also reduces efficiency.

Test results are presented which illustrate the difference in losses of the HEXFET and the bipolar transistor as a function of frequency. The HEXFET is shown to be generally more efficient above frequencies in the 20 to 40 kHz range.

Bipolar Transistor Current Ratings

It will help to set the stage by first considering the basis of the current ratings of a bipolar transistor. Whereas the continuous and peak current ratings of a bipolar that are "headlined" in the data sheet are theoretically valid, they are hardly ever usable in practice. A basis for specifying the current ratings of bipolar transistors has been adopted in the industry which unfortunately is not representative of usable current levels; it simply provides a yardstick for making comparisons between different products on a reasonably common basis.

The Achilles' heel of the bipolar's current carrying capability is the critical question of the attendant gain, saturation voltage and switching time at *elevated operating temperature*. These supporting parameters are usually specified at "rated" current at a junction temperature of 25° C (where they give the appearance of acceptability), but the data sheet usually does not specify their values at higher "operating" junction temperature (where they are usually not so acceptable).

In reality the bipolar is not intended to be used at its headlined "rated" continuous current. To do so would require an inconveniently large amount of drive current, and the saturation voltage and switching times would be hard to live with in a practical design, in which the normal junction operating temperature would, of course, be well in excess of 25° C.

A good maximum design operating level for a bipolar transistor is typically 60 to 70% of the headlined "continuous" collector current rating; experienced users know this and design to it. Device manufacturers know it, too; this is why the data sheet specifies the minimum gain, maximum saturation voltage and maximum switching times at elevated junction temperature (usually 100° C), at a collector current which is 60 to 70% of the headlined "rated" value, but not at the "rated" current itself.

An example will illustrate this. The industry-standard 2N6542/3 bipolar transistor has a "headlined" continuous collector rating of 5A. The maximum value of $V_{CE(SAT)}$, the corresponding forced gain, and the maximum switching times at elevated temperature (T_C = 100° C) are, however, specified at a collector current of only 3A. If the designer really

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wants to use this device at its headlined "rated" current, he will have to refer to the manufacturer to determine the critical "worst case" supporting data needed to design the circuit; this information will not be found on the data sheet.

The rated *peak* collector current of a bipolar is even more tenuous than the rated continuous value. This is usually specified without reference to the required base drive current. Consider the 2N6542/3. The peak collector current rating headlined on the data sheet is 10A. Not specified is the base current needed to produce this collector current.

The DC gain curve, reproduced from the data sheet in Figure 1, terminates at the "continuous" collector current rating of 5A. Bearing in mind that this is anyway a typical curve, it is a matter of conjecture what the minimum gain will be at a collector current of 10A, at elevated operating temperature — and hence what base current will be needed to support the 10A peak collector current rating.

In reality the gain will likely be less than the unity. The 2N6542/3 device would therefore have to be driven with a *base* current of at least 10A in order to utilize its peak collector current rating of 10A — an untenable situation for most practical designs.

Current Ratings of MOSFETs

Continuous Ratings

The MOSFET is quite a different device to a bipolar, and its continuous I_D rating is based upon quite different considerations. Whereas the usable current of a bipolar is basically limited by gain, this is not the case with a power MOSFET. Figure 2 shows a typical relationship between transconductance of a HEXFET and a drain current. Transconductance increases with increasing drain current — just the opposite situation than with a bipolar transistor. Obviously the HEXFET — unlike the bipolar — is not going to "run out of gain" as the drain current increases.

Switching speed is generally much faster than that of a bipolar. With proper drive circuit design, switching speed of a HEXFET varies relatively slightly as the current increases, and is not a factor in determining the rated current. This can be deduced from Figure 3, which shows a typical relationship between gate charge, gate voltage, and drain current for a HEXFET. For a given gate charging current, switching speed is directly proportional to gate charge. The gate charge required for switching, and hence switching speed itself, is not influenced greatly by the amplitude of the drain current, and not at all by junction operating temperature.

The major criterion on which the continuous rating of a HEXFET is based is *heat removal.* The HEXFET will carry as much current as the cooling system will permit, while keeping peak junction temperature within the rated maximum value. The more efficient the heat dissipator to which the HEXFET is attached, the lower the case temperature will be, the greater the permitted case-to-junction temperature rise, the greater the permitted internal power dissipation, and the greater permissible current. These considerations are, of course, exactly the same as those which apply to other non-gain-limited power semiconductor devices, such as rectifiers and thyristors.

Usable current, I_D, for a HEXFET is therefore:

$$I_D = \sqrt{\frac{T_{Jmax} - T_C}{R_{DS(on)}\, R_{th(JC)}}}$$

where $R_{DS(on)}$ is the limiting value of the on-resistance *at rated* $T_{(Jmax)}$, *at the appropriate value of* I_D, R_{thJC} is the maximum value of internal junction-to-case thermal resistance, and T_C is the case temperature.

Figure 4 shows the continuous current rating of the IRF330 HEXFET as a function of case temperature. Note that below a case temperature of 25° C, the continuous I_D rating is limited by the current carrying capacity of the internal source bonding wire. But this is not a practical limitation.

Figure 4 also shows the relationship between HEXFET internal power dissipation and drain current. Power is proportional to the square of the current, so rises quite rapidly as cur-

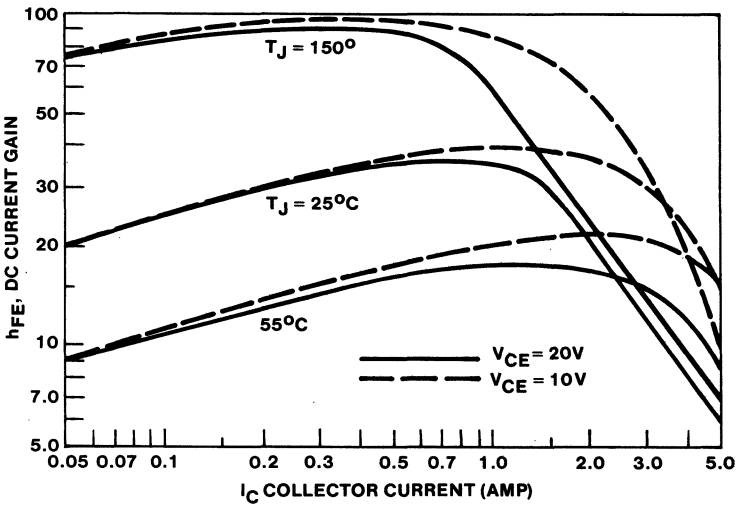


Figure 1. Typical DC Current Gain, 2N6542/3 Bipolar Transistor

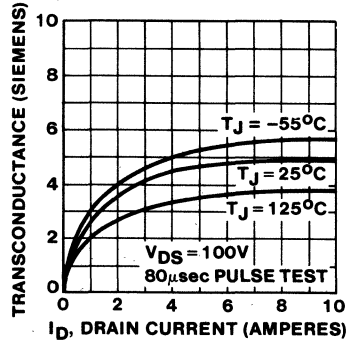


Figure 2. Transconductance Vs. Drain Current of the IRF330.

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rent increases. The required heatsink DC thermal resistance decreases quite rapidly with increasing continuous drain current, for two reasons. First, permissible case-to-ambient temperature decreases; and second, power dissipation increases.

For this reason the usable *continuous direct* current of a power MOSFET for most practical purposes relates to a case temperature around 90 to 100° C. This allows a sufficient differential between case and ambient temperature for the heat dissipator to handle the heat transfer, maintaining the case temperature at or below the permitted maximum.

The "headlined" continuous current rating shown on the data sheets of most power MOSFETs is usually *greater* than the above practically usable level of *continuous* drain current. This is because the case temperature adopted by the industry to which the "headlined" continuous I_D rating applies is only 25° C.

Figure 5 shows typical heatsinks for TO-3 and TO-220 packaged HEXFETs that allow them to operate in a 40° C ambient at a *continuous direct* drain current that is 60 to 70% of the rated continuous drain current at T_C = 25° C; the corresponding *steady* case temperature is about 100° C.

Actually, the continuous current rating of a MOSFET is often of little direct use to the designer, other than as a benchmark. This is because in many switching applications the MOSFET operates at a switching duty cycle considerably less than 100%, and what is really of interest is the current-carrying capability of the device under the *actual* "switched" operating conditions. This is discussed in the next section.

Switching "Duty Cycle" Ratings

As has been seen, the basic criterion that determines the current-carrying capability of a HEXFET is *junction heating*. For most practical purposes, the HEXFET can carry any waveform of current under any "duty cycle", just so long as the peak junction temperature is kept within the rated $T_{(Jmax)}$ (150° C). (The RMS content of the current wave must not exceed the continuous I_D rating, in order not to exceed the RMS current carrying capability of the source bonding wire. Compliance with this will generally be a natural result of compliance with the condition above.)

Peak junction temperature for any "duty cycle" application can be calculated directly from the transient thermal impedance characteristics for the device, as given in the data sheet. Transient thermal impedance curves for the IRF330 HEXFET are shown in Figure 6. Each of these curves is normalized to the steady DC junction-to-case thermal resistance (1.67 deg. C/Watts for the IRF330).

The curve labelled "single pulse" shows the rise of junction temperature per watt of power dissipation as a function of pulse duration. As expected, junction temperature rise increases as pulse duration increases — leveling off to a steady value for pulse durations above 1 second or so.

The "single pulse" curve is useful for determining transient junction temperature rise for single or very low duty cycle pulses of power; it is not *directly* usable for repetitive power pulses, such as are usually encountered in switching applications. The remaining curves in Figure 6 show effective thermal impedance for repetitive operation at different duty cycles, and allow peak junction temperature rise for repetitive operation to be calculated directly. These curves are approximately related to the single pulse curve, by the following relationship:

Effective normalized thermal impedance.

= D+(1 - D) x (normalized transient thermal impedance for single pulse of duration t).

The effective thermal impedance,* when multiplied by the power dissipation *during the conduction period t* (i.e., the power *within* the conduction pulse itself, *not* the power averaged over the whole cycle), gives the value of the repetitive peak junction-to-case temperature rise.

As seen from Figure 6, the effective thermal impedance for any duty cycle D increases as pulse duration increases, showing that the peak junc-

**Thermal Impedance = Normalized Value x DC Thermal Resistance*

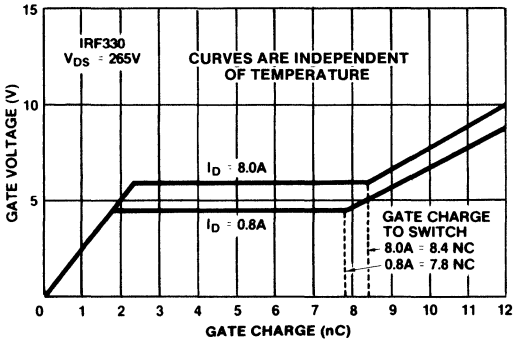


Figure 3. Typical Relationships for IRF330 HEXFET Between Gate Charge, Gate Voltage and Amplitude of Drain Current Being Switched.

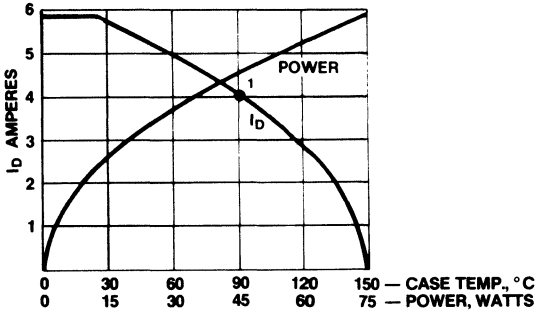
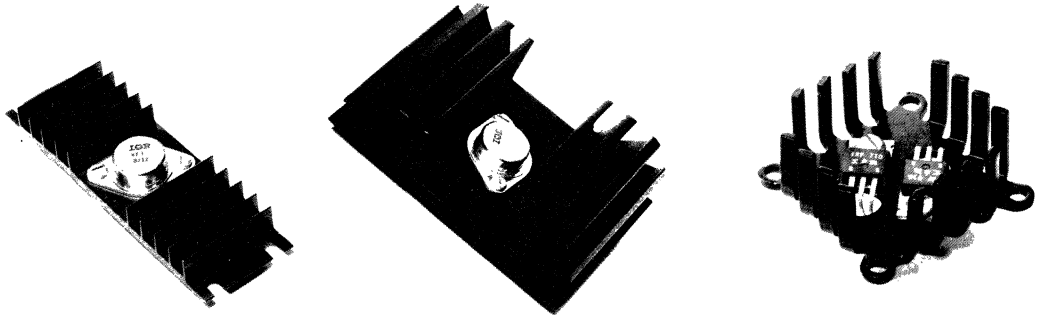


Figure 4. Case Temperature and Power as Function of I_D for IRF330 HEXFET.

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(a) Type 621-A heatsink gives 4A continuous rating for IRF331 with 5 CFM airflow in 40° C ambient.

(b) Type 641-A heatsink gives 3.5A continuous rating for IRF331 with natural convection cooling in 40° C ambient.

(c) Type 689-75 B-4 heatsink gives 1A continuous rating for IRF710 with natural convection cooling in 40° C ambient.

Figure 5. Typical Heatsinks for HEXFETS. (Heatsinks by Wakefield)

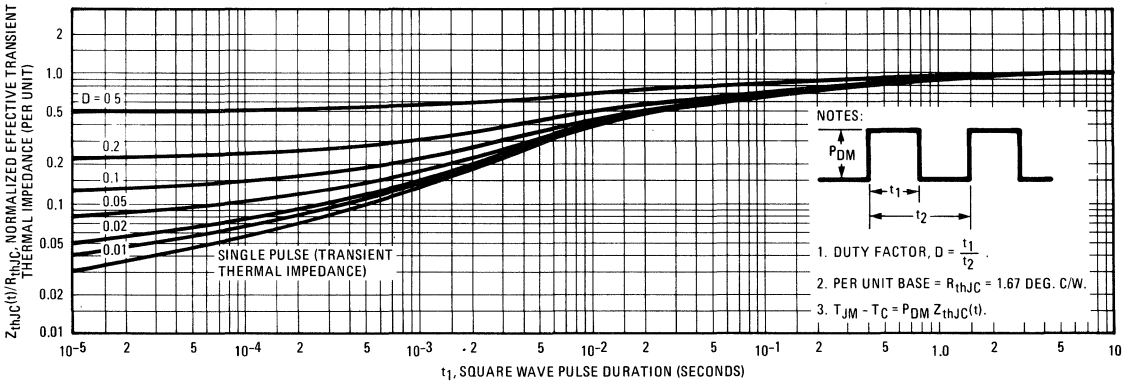


Figure 6. Normalized Transient Thermal Impedance Curves for IRF330 HEXFET. Curves are normalized to DC Thermal Resistance (1.67°C/W for IRF330).

tion temperature rise increases as frequency decreases. The reason for this is illustrated by the waveforms in Figure 7 (a) and (b). Both sets of waveforms are for the same power dissipation and duty cycle, but for different operating frequencies. The cycle-by-cycle fluctuations of junction temperature at 20Hz (Figure 7[a]) are clearly greater than at 200Hz (Figure 7[b]). As frequency increases, thermal inertia of the junction "irons out" instantaneous temperature fluctuations, and the junction responds more to average, rather than peak, power dissipation. At frequencies above a few kHz, and duty cycles above 20% or so, cycle-by-cycle temperature fluctuations usually become small, and peak junction temperature rise becomes equal to the average power dissipation multiplied by the DC junction-to-case thermal resistance, within one or two percent.

To determine the absolute value of the peak junction temperature, it is, of course, necessary to know the case temperature T_C under steady operating conditions. Because of thermal inertia, the heatsink responds only to average power dissipation (except at extremely low frequencies which generally will not be of practical interest). T_C is therefore given by:

$$T_C = T_A + (R_{thC\text{-}S} + R_{thS\text{-}A})\, P_{AV}$$

where:

T_A = ambient temperature
$R_{thC\text{-}S}$ = case-to-sink thermal resistance
$R_{thS\text{-}A}$ = sink-to-ambient thermal resistance
P_{AV} = average power dissipation = peak power x duty cycle, for rectangular pulses of power

Peak Current Ratings

The underlying limitation on current handling capability of a HEXFET is junction heating. It is able to carry peak current well in excess of its continuous I_D rating, provided that the rated junction temperature is not exceeded. There is, however, an upper limit on the permissible current, defined by the rated I_{DM}. Most HEXFETs have an I_{DM} rating that is about 4X the continuous I_D rating at T_C = 25° C. This is a very substantial peak current carrying capability by comparison with the I_{CM} rating of a bipolar — especially when it is rec-

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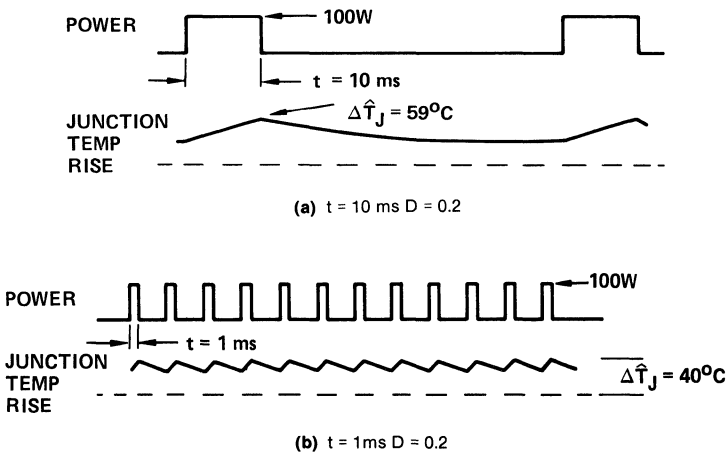


Figure 7. Waveforms of Power and Junction Temperature for Repetitive Operation, showing that Peak Junction Temperature is Function of Operating Frequency. IRF330.

ognized that the I_{DM} rating of a HEXFET is *usable,* whereas the I_{CM} rating of a bipolar generally is not.

The I_{DM} limit of a HEXFET is determined by the fact that it is, after all, fundamentally a "linear" device. As drain current increases, the point eventually is reached at which the HEXFET goes into "linear" operation and starts to act, in effect, as a current limiter. This point depends upon the drive voltage applied to the gate, the safe limit of which is determined by the thickness of the oxide that insulates the gate from the body of the device. I_{DM} ratings of all HEXFETs are achievable with an applied gate voltage that is equal to the maximum permissible gate-to-source voltage of 20V.

Designers often do not know how to interpret the I_{DM} rating. Data sheets typically give little or no supporting information, and no direct indication of whether this is a non-repetitive or repetitive rating. The fact is that the I_{DM} rating of all HEXFETs can be used *both* for *repetitive* and *non-repetitive* operation, so long as the junction temperature is kept within the rated T_{Jmax}. Peak junction temperature can be calculated from the thermal impedance data for the device (shown in Figure 6). The I_{DM} rating is simply a "ceiling"; below this ceiling, the designer is free to move, provided the T_{Jmax} rating is not violated.

Use of the HEXFET's peak current ratings is illustrated by the oscillograms in Figures 8 through 10. Figure 8 shows operation of the 500V rated IRF450 at a repetitive peak current of 52A. The conduction time of the rectangular current pulse is 7 μs, and the operating frequency is 1kHz. The rated continuous I_D (at T_C = 25° C) of this device is 13A, and its rated I_{DM} is 52A.

Figure 9 illustrates the use of the I_{DM} rating of the 100V IRF150 HEXFET for a "single shot" low duty cycle application, such as capacitor charging or motor starting. The peak current is 150A, decaying to 50A in approximately 10 milliseconds. Figure 10 illustrates similar duty, but in this case, the initial peak current is 100A, decreasing to 30A in approximately 400 milliseconds. The rated continuous I_D (at T_C = 25° C) of the IRF150 is 40A, and its rated I_{DM} is 160A.

It should be pointed out that the on-resistance of any MOSFET does increase as current increases. As shown in Figure 11, the on-resistance of a 100V rated HEXFET at its rated I_{DM} with 20V applied to the gate is tyically 1.4 x the value at the rated I_D; the corresponding multiplier for a 400V rated HEXFET is 2.9. This increase of on-resistance must, of course, be taken into account when making thermal calculations and designing for use of the I_{DM} rating.

Safe Operating Area of MOSFET

It has been tacitly assumed so far that the HEXFET is operated as a "closed switch" in the "fully en-

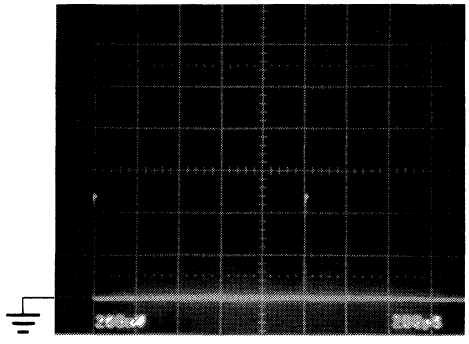


Figure 8. 52A, 7 μs Pulses Being Carried by the IRF450 at Frequency of 1kHz.

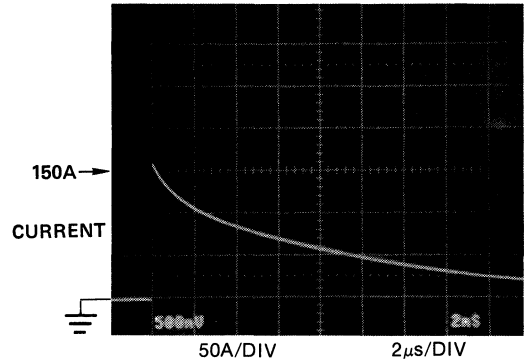


Figure 9. Single Shot 150A peak Exponentially Decaying Pulse Applied to the IRF150. Time Constant ≒ 8msec

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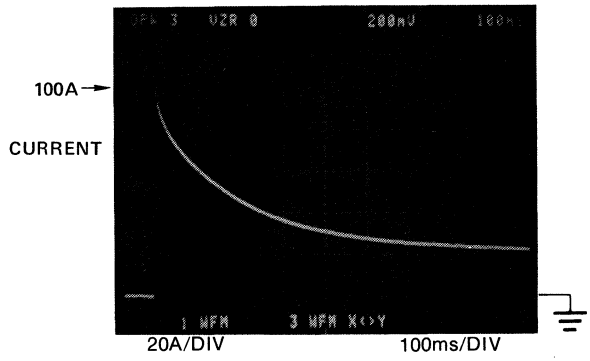


Figure 10. Single Shot 100A peak Exponentially Decaying Pulse Applied to IRF150. Time Constant ≒ 300msec

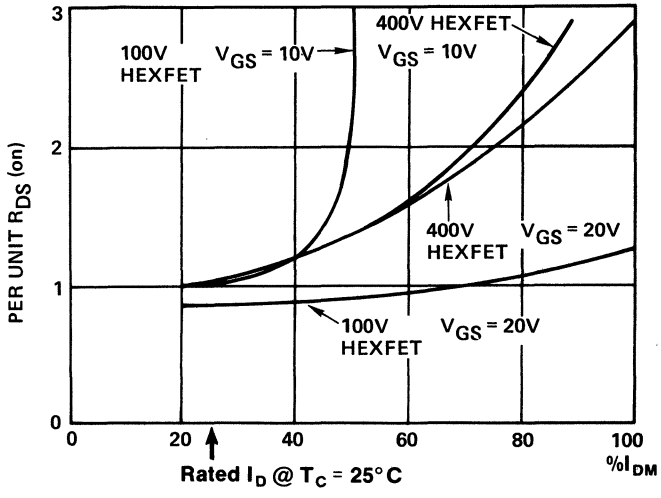


Figure 11. Typical Variation of On-Resistance with Drain Current. 100% I_{DM} ≒ 4 x I_D @ T_C = 25 °C

hanced" mode; the amount of current that the switch can handle has been shown to be calculatable for any specific design situation from a knowledge of the conduction losses, the effective transient thermal impedance, and the heatsink thermal resistance.

MOSFET data sheets generally show a graph of Safe Operating Area, for single pulses of power of varying duration, which for the most part cover areas of "linear" rather than "fully enhanced" operation. These curves embrace drain current and voltage values up to rated I_{DM} and V_{DS}, respectively. A typical SOA curve, for the IRF330, is shown in Figure 12.

SOA curves for HEXFETs are based upon a case temperature of 25° C, and an internal power dissipation that increases the junction temperature to 150° C at the end of the power pulse. Since HEXFETs, unlike bipolar transistors, do not exhibit second breakdown, SOA curves for each pulse duration invariably follow a line of constant power at all voltages less than rated maximum V_{DS} and more than the "fully enhanced" $V_{DS(on)} = I_D \times R_{DS(on)}$.

The SOA curves for HEXFETs in reality are redundant, because they can be calculated directly from the single pulse transient thermal impedance data. Nor are they particularly useful from the circuit design viewpoint, because they apply to single pulses at a case temperature of 25° C — conditions not generally encountered in practice.

Why, then, are the SOA curves included in the MOSFET's data sheet? The reason is that if they were not, their absence would raise questions in designers' minds. Users who are accustomed to bipolar transistors have come to look upon the SOA curves for these devices as being vital — as indeed they are — because they define the bipolar's second breakdown limits.

SOA curves for HEXFETs, on the other hand, are in essence nothing more than a graphical statement of the absence of second breakdown — vital information, to be sure, but information which in reality need not be conveyed through a set of somewhat arbitrary curves.

The oscillograms in Figure 13 (a) and (b) are a verification of the HEXFET's SOA data. Figure 13 (a) shows a 10 microsecond 150A pulse of current being applied to the 100V IRF150 HEXFET, with an applied drain-to-source voltage of *80V*. Figure 13 (b) shows a 10 microsecond 50A pulse of current being applied to the 500V rated IRF450 with an applied drain-to-source voltage of *400V*.

Design Examples

The following examples illustrate typical design procedures:

Repetitive Operation — 30% Duty Cycle

A 400V rated HEXFET and a corresponding heatsink are required for continuous operation with a rectangular current waveform. Amplitude of the current is 3.5A, duty cycle is 30%, and ambient temperature is 45° C. Switching losses and cycle-by-cycle fluctuations of junction temperature can be ignored.

Candidate devices would be the IRF332 and IRF320. Key ratings and characteristics for these devices are shown in Table 1.

Conduction losses for IRF332:
= 3.5 x 11.55 x 0.3
= 12.1W

Required R_{thJ-A} = $\frac{(150 - 45)}{12.1}$
= 8.7° C/W

Required R_{thS-A} = 8.7 - 1.97
6.7° C/W

Conduction losses for IRF320:
= 3.5 x 13.9 x 0.3
= 14.6W

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$$\text{Required } R_{thJ\text{-}A} = \frac{(150 - 45)}{14.6}$$
$$= 7.2°C/W$$
$$\text{Required } R_{thS\text{-}A} = 7.2 - 3.12$$
$$= 4°C/W$$

These calculations show that either of the candidate HEXFETs could serve the application. The smaller IRF320 (almost half the chip size of the IRF332) would require a relatively larger (though quite practical) heatsink, and would dissipate 14.6 instead of 1.21W giving about a 1% reduction in overall system efficiency.

The final choice of device will depend upon trade-offs between economics, size, and performance. The main purpose of this example has been to demonstrate that there *is* a choice, and that either of two HEXFET types are viable candidates.

Repetitive Operation at High Peak Current, Low Duty Cycle

It is required to find the thermal resistance of the heatsink needed to operate the 400V, 5.5A (continuous) rated IRF330 HEXFET with a repetitive rectangular current waveform of amplitude 18A. On-time is 10 microseconds, and duty cycle is 0.1%. Ambient temperature is 40°C.

The limiting on-resistance of the IRF330 at I_D = 5.5A at 25°C is 1.0 ohm. Knowing that 100% I_{DM} = 22A, the limiting value of $R_{DS(on)}$ at I_D = 18A can be estimated from Figure 11 to be 2.3 ohms at 25°C. From the relationship between $R_{DS(on)}$ and temperature given in the data sheet, $R_{DS(on)}$ at T_J = 150°C and I_D = 18A will be about 5.1 ohms.

$$\text{Power per pulse} = 18^2 \times 5.1$$
$$= 1.652 \times 10^3 W$$

Junction-to-case transient thermal impedance for 10 μs pulse (from Figure 6):

$$= 1.67 \times 0.03$$
$$= 0.05°C/W$$

Table 1. Design details for IRF332 and IRF320 HEXFET's

		IRF332	IRF320
V_{DS}	Volts	400	400
I_D @ T_C = 25°C	Amps	4.5	3.0
$V_{DS(on)}$ @ 5A, 150°C	Volts	11.55	13.9
$R_{thJ\text{-}C}$	°C/W	1.67	3.12
$R_{thC\text{-}S}$	°C/W	0.2	0.2
Approximate die size	mil²	19,250	11,700

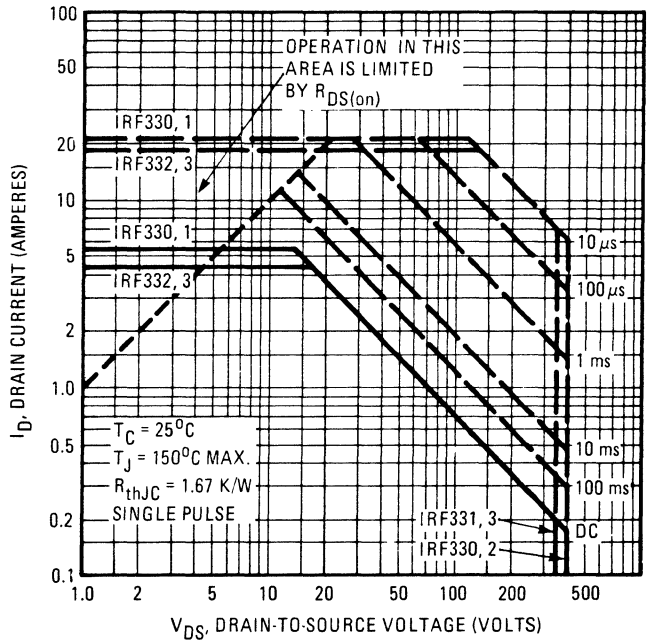
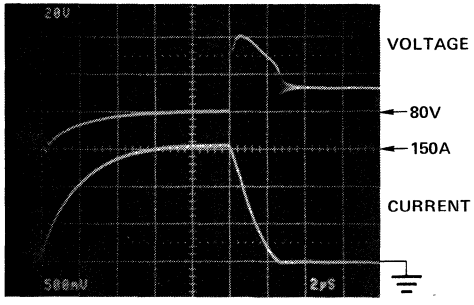
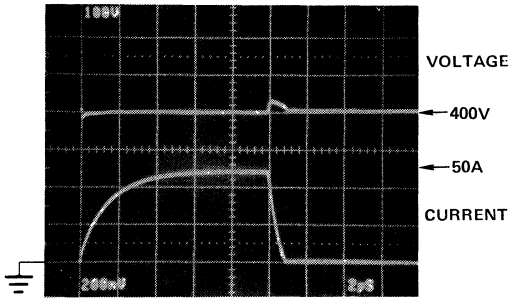


Figure 12. Safe Operating Area, IRF330 HEXFET.



(a) IRF150, 50A/div, 2μs/div



(b) IRF450, 20A/div, 2μs/div

Figure 13. Oscillograms Verifying SOA Curves of HEXFETs, Demonstrating the Absence of Second Breakdown

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Junction-to-case temperature rise due to 18A pulse:

$= 1.652 \times 10^3 \times 0.05$

$= 82.6°C.$

Maximum permissible case temperature:

$= 150 - 82.6 = 67.4°C$

$T_C - T_A = 67.4 - 40 = 27.4°C$

Average power dissipation:

$= 0.01 \times 1.652 \times 10^3$

$= 1.652W$

$$\therefore R_{thC\text{-}A} = \frac{27.4}{1.652} = 16.6°C/W$$

High Peak Current, Single Pulse Operation

The IRF330 HEXFET is to be pulsed with a current having an initial amplitude of 20A, and an exponential waveform with a time constant of 150 μsec. Case temperature is 30°C. Verify that the peak junction temperature does not exceed 150°C.

As an approximation, an equivalent rectangular pulse of current will be assumed, with an amplitude of 15A, and a duration of 150 microseconds.

$R_{DS(on)}$ for the IRF330 @ I_D = 15A, T_J = 25°C, is 1.8 ohms. At 150°C, $R_{DS(on)}$ is approximately 2.2 x this value (see above example), and is about 4.0 ohms.

Equivalent "rectangular power":

$= 15^2 \times 4.0 = 900W$

Junction-to-case transient thermal impedance for 150 microsecond pulse (from Figure 6):

$= 0.065 \times 1.67 = 0.11°C/W$

$\therefore$ Junction-to-case temperature rise

$= 0.11 \times 900 = 99°C$

$\therefore T_J = 30 + 99°C = 129°C$

Hence, this operating condition is within the capability of the IRF330.

Comparison of MOSFET and Bipolar Losses

Conduction power in a bipolar transistor is generally lower than in a MOSFET, but switching energy is usually considerably higher. The bipolar, therefore, tends to be more efficient at low frequency, while the MOSFET is more efficient at high frequency.

In an effort to close the gap between bipolar and MOSFET performance in high frequency switching applications, several new types of fast switching bipolar transistors have recently been introduced, with switching times in the order to 100 to 200 nanoseconds. It is pertinent to compare the losses of these new bipolar types with those of comparably rated MOSFETs.

Figure 14 shows measured power dissipation as a function of frequency for the IRF330 HEXFET, the industry-standard 2N6542/3 bipolar transistor, and a newly introduced fast switching bipolar. Power losses were obtained by measuring the case temperature rise of the device mounted on a calibrated heatsink. Thermal resistance from case-to-ambient was approximately 4.5 deg. C/W. A clamped inductive load was used.

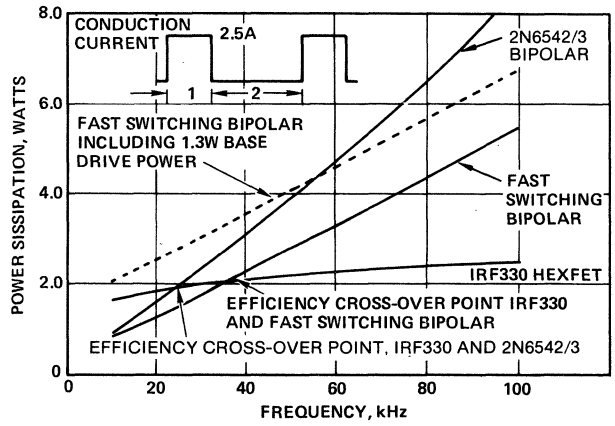


Figure 14. Power Dissipation Versus Frequency for 2N6542/3, Fast Switching Bipolar, and IRF330 HEXFET. Supply Voltage = 270V. Conduction Duty Cycle = 0.33. Current Amplitude = 2.5A.

Details of the three device types listed are summarized in Table 2. Note that the die area for the HEXFET is approximately 80% of that of each of the bipolar transistors — thus, the comparison is weighted in favor of the larger-die bipolar devices.

Figure 14 shows that the frequency crossover point for the HEXFET and the 2N6542/3 is approximately 25kHz, while it is approximately 35kHz for the HEXFET and the fast-switching bipolar transistor. Operating conditions were: circuit supply voltage = 270V, peak current = 2.5A, duty cycle = 33%.

Note that the "full" curves represent *only* the dissipation *within* the device. Additional power is dissipated in the external base drive circuit of the bipolar. The "dashed" curve for the fast-switching bipolar includes an additional 1.3W of external base drive power. This corresponds to an 8V, 0.5A drive circuit, operating at 33% duty cycle.

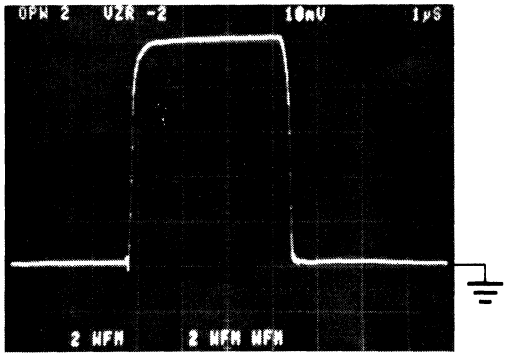
Figure 15 shows collector current and voltage oscillograms for the fast-switching bipolar transistor operating at 100kHz, and Figure 16 shows drain current and voltage oscillograms for the HEXFET at 100kHz. Note the sharper HEXFET waveforms, confirming its faster switching speed.

Oscillograms of base drive current for the bipolar and gate drive current for the HEXFET are shown in Figure 17 (a) and (b), respectively. The bipolar requires a significant base drive current both at turn-on — about 1A peak — and at turn-off — 2.5A peak. The HEXFET, by comparison, consumes about 0.3A for a few nanoseconds at turn-on, and about 0.2A for a few nanoseconds at turn-off. This current charges and

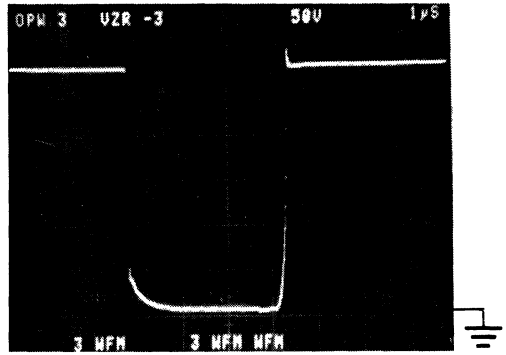
Table 2. Details of Devices Tested

	IRF330 HEXFET	2N6542/3 Bipolar	Fast-Switching Bipolar	
V_{DS} Volts	400	400	450	$V_{CEO(SUS)}$
$I_{D\ cont}$ A @ T_C = 25°C	6	5	5	$I_{C\ cont}$ A @ T_C = 25°C
Die Area mil²	19,500	25,000	25,000	Die Area mil²

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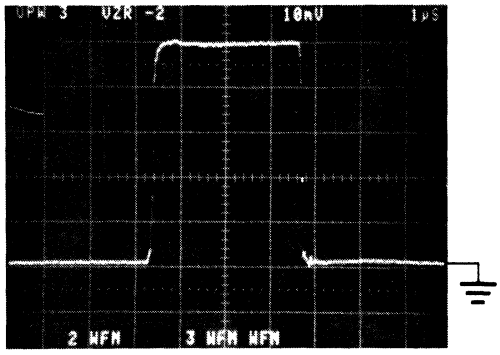


(a) Collector Current. 0.5A/Div, 1μs/Div

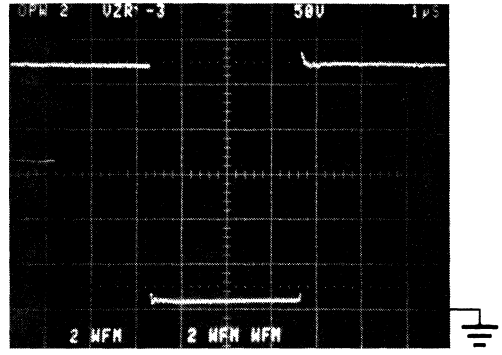


(b) Collector Voltage. 50V/Div, 1μs/Div

Figure 15. Collector Current and Voltage Waveforms for Fast-Switching Bipolar Operating at 100kHz.

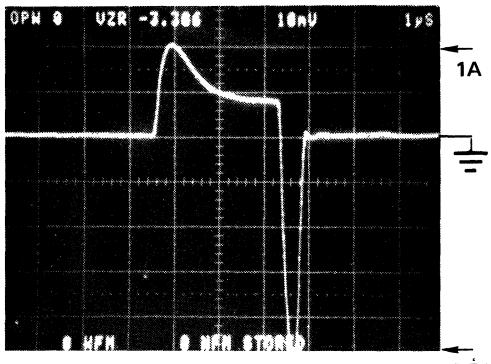


(a) Drain Current. 0.5A/Div, 1μs/Div

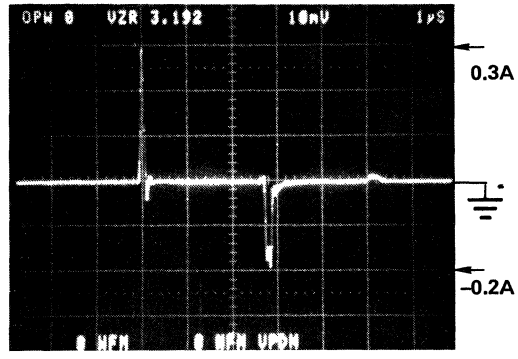


(b) Collector Voltage. 50V/Div, 1μs/Div

Figure 16. Drain Current and Voltage Waveforms for IRF330 HEXFET Operating at 100kHz.



(a) Bipolar. 0.5A/Div 1μs/Div



(b) HEXFET. 0.1A/Div 1μs/Div

Figure 17. (a) Base Drive Current for Fast Switching Bipolar Operating at 2.5A, 100kHz. V_{CC} = 270V

(b) Gate Drive Current for IRF330 HEXFET Operating at 2.5A, 100kHz. V_{DD} = 270V.

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discharges the self-capacitance of the device. Note the change of current scale between Figure 17 (a) and (b). Average gate drive power for the HEXFET is negligible — about one-fiftieth of a watt at 100kHz. Although the bipolar is driven with 1A peak base current, it nonetheless exhibits a noticeable voltage "tailing" at turn-on, as seen in Figure 15 (b).

The oscillograms in Figure 18 compare the instantaneous power and energy dissipation for the fast-switching bipolar and the HEXFET. Figure 18 (a) shows instantaneous power, while Figure 18 (b) shows the integral of the power; in other words, the accumulated energy dissipated during the conduction period.

Clearly the energy expended in the bipolar at turn-on and at turn-off is greater than in the HEXFET, while the energy expended in the HEXFET during the conduction period is greater than in the bipolar. These oscillograms do not give precise quantitative data because of the lack of resolution of the oscilloscope at these fast-switching speeds; they do, nonetheless, provide a good qualitative picture of the different switching and conduction losses in the two types of devices.

Figure 19 shows a comparison of power losses versus frequency for the HEXFET and the fast-switching bipolar, for the same 2.5A current and 33% duty cycle, but at a circuit voltage of only 70V — instead of the previous 270V. While the HEXFET losses are about the same as in the higher voltage circuit, the lower supply voltage greatly de-emphasizes the switching losses of the bipolar, giving a higher frequency crossover point (almost 70kHz). These curves, however, are not representative of a typical operating situation, since the 70V circuit voltage is unrealistically low for 400 to 450V rated devices.

Finally, the curves in Figure 20 show power losses versus frequency for the HEXFET and the fast-switching bipolar, operating at a peak current of 5A in a 270V circuit, at a duty cycle of 33%. Although the conduction losses of the HEXFET are more than 4x greater than with I_D = 2.5A, the switching losses of the bipolar are also significantly greater. Additionally, the bipolar's base drive current has to be increased significantly to maintain acceptable switching performance, as shown by the oscillogram in Figure 21. Interestingly, the frequency "crossover point" is not greatly different from that obtained at 2.5A — about 42kHz versus 35kHz, ignoring external base drive power, and about 20kHz, taking this into account.

Conclusions

The main purpose of this application note has been to show that the current-carrying capability of a power MOSFET is determined essentially by *thermal* considerations, un-

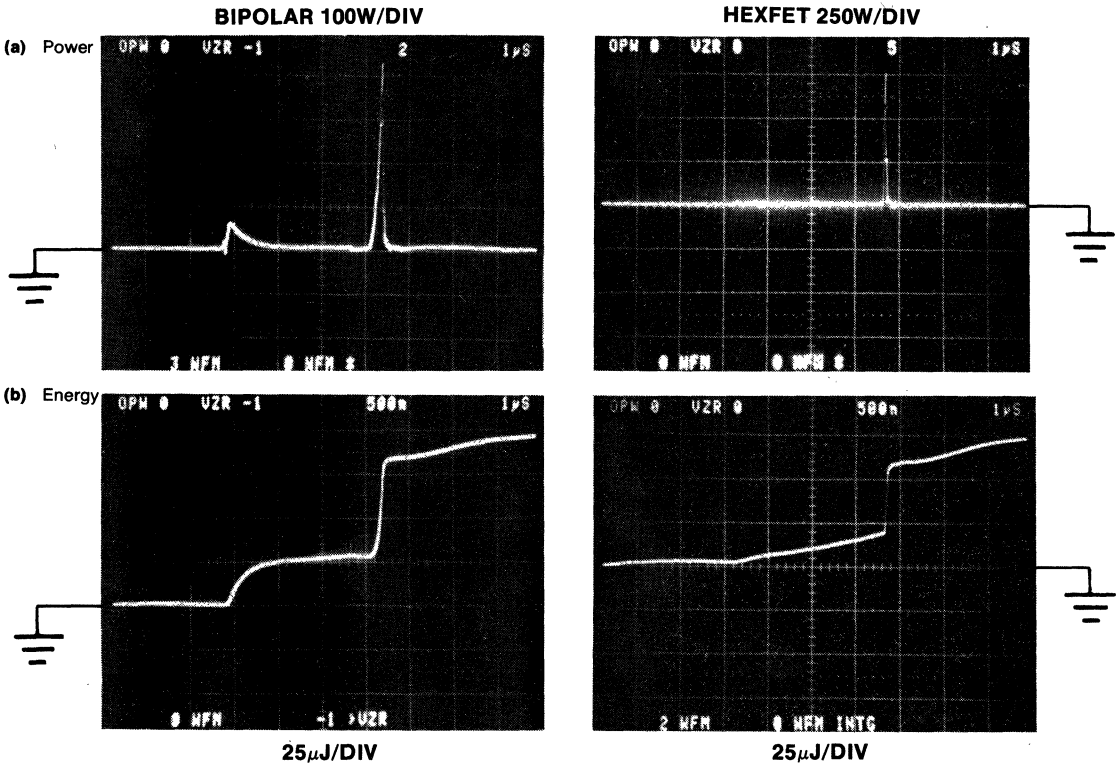


Figure 18. Oscillographs of (a) Power and (b) Energy for Fast-Switching Bipolar Transistor and HEXFET from Turn-On to Turn-Off. Circuit Voltage = 270V. Switched Current = 2.5A. Duty Cycle = 33%. Frequency = 100 kHz.

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like that of the bipolar transistor, which is limited by *gain*. With proper thermal design, the HEXFET can be operated at much higher peak current than a comparable bipolar.

A practical comparison of power losses of a HEXFET and a fast-switching bipolar transistor in a switching application shows that the HEXFET is generally more efficient above frequencies in the 20 to 40 kHz range. □

Editors' Note: This Application Note AN-949 is a much expanded version of the subject discussed in Application Note AN-945, "Understanding HEXFET Current Ratings — A Necessity for the Cost-Conscious Designer," which this application note supersedes.

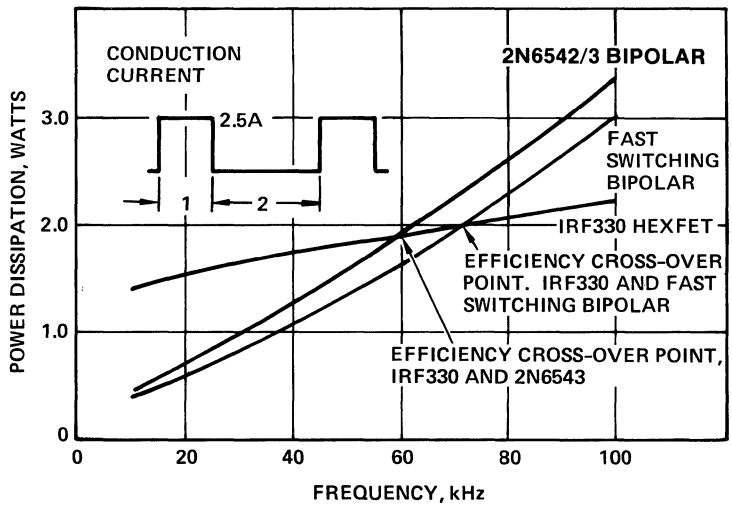


Figure 19. Power Dissipation Versus Frequency for 2N6542/3, Fast-Switching Bipolar and IRF330 HEXFET. Supply Voltage = 70V. Conduction Duty Cycle = 0.33. Current Amplitude = 2.5A.

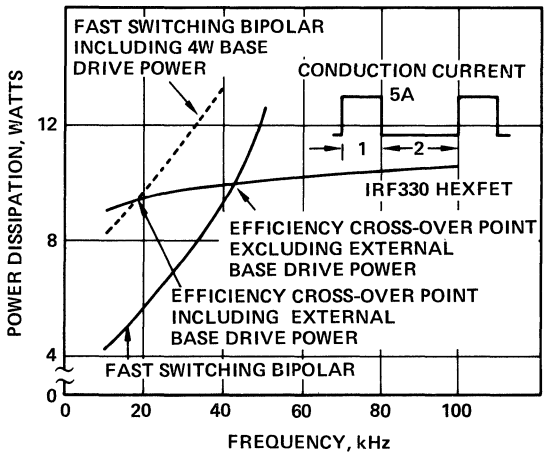


Figure 20. Power Dissipation Versus Frequency for Fast-Switching Bipolar and IRF330. Supply Voltage = 270V. Conduction Duty Cycle = 0.33. Current Amplitude = 5A.

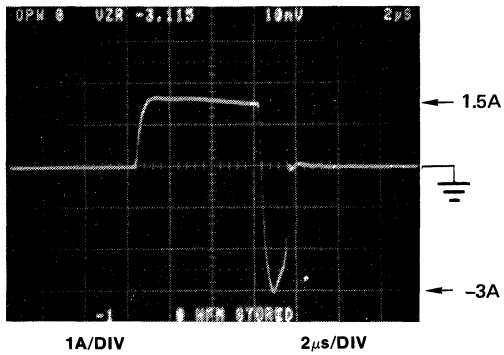


Figure 21. Base Drive Current for Fast-Switching Bipolar. Circuit Voltage = 270V. Collector Current = 5A. Operating Frequency = 50kHz.

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A New Gate Charge Factor Leads to Easy Drive Design for Power MOSFET Circuits

By B. R. PELLY

Designers unfamiliar with MOSFET characteristics begin drive circuit design by determining component values based on the gate-to-source, or input, capacitance listed on the data sheet. While RC values derived in this manner do serve as a starting point in design, they can only be considered as a first-order benchmark.

If the designer wants to switch the MOSFET in 100 nanoseconds, an RC value based on the gate-to-source capacitance is determined to provide a suitable, theoretical time constant. The RC value does not solve the entire problem because the gate-to-drain capacitance must also be accounted for in charge time.

Although the gate-to-source capacitance is an important value, the gate-to-drain capacitance is actually more significant — and more difficult to deal with — because it is a non-linear capacitance affected as a function of voltage; the gate-to-source capacitance is also affected as a voltage function, but to a much lesser extent. This gate-to-drain capacitance function is similar to that found in vacuum tube amplifiers.

The gate-to-drain capacitance effect is akin to the "Miller" effect, a phenomenon by which a feedback path between the input and output of an electronic device is provided by the interelectrode capacitance. This affects the total input admittance of the device which results in the total dynamic input capacitance generally being greater than the sum of the static electrode capacitances. The phenomenon of the effects of the plate impedance and voltage gain on the input admittance was first studied in vacuum tube triode amplifier circuits by John M. Miller.

Essentially, at high frequencies where the grid-to-plate (gate-to-drain) capacitance is not negligible, the circuit is not open but involves a capacitance that is a function of the voltage gain.

Solving for the "Miller" effect is not exactly a straightforward process, even with vacuum tubes where much is known, but is even more difficult in MOSFETs. In actuality, the gate-to-drain capacitance though smaller in static value than the gate-to-source capacitance, goes through a voltage excursion that is often more than 20 times that of the gate-to-source capacity. Therefore, the gate-to-drain or "Miller" capacitance typically requires more actual charge than the input capacitance.

To account for both gate-to-source and gate-to-drain capacitance in a way readily usable by designers, each HEXFET from International Rectifier is tested to yield a specification termed "gate charge," that can be used to calculate drive circuit requirements.

A typical test circuit that can be used to measure the gate charge is

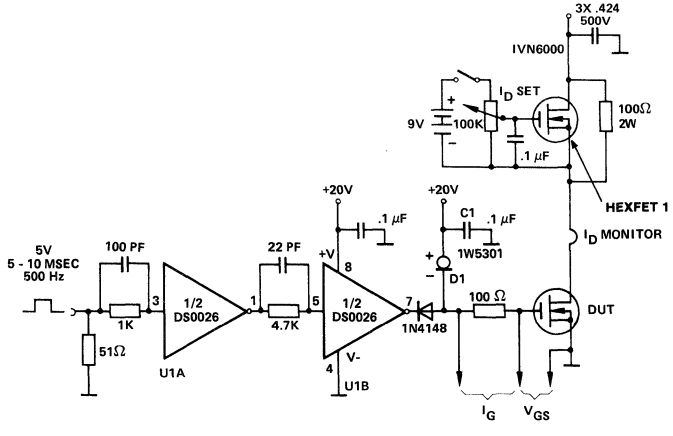


Figure 1. HEXFET Gate Charge Circuit.

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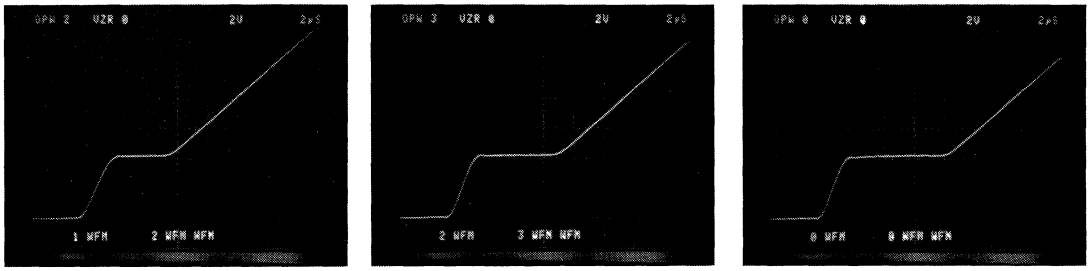


Figure 2. Gate Charge Waveform for Different Values of Drain Voltage (IRF130: I_G = 1.5 mA, I_D = 1A, V_{DD} = 10, 40 and 80 Volts).

shown in Figure 1. In this circuit, an approximately constant current is supplied to the gate of the device-under-test from the 0.1 μF capacitor C1, through the regulator diode D1. A constant current in the drain circuit is set by setting the voltage on the gate of HEXFET 1, so the net measurement of the charge consumed by the gate is relative to a given current and voltage in the source-to-drain path.

An oscillogram of the gate-to-source voltage during testing, shown in Figure 2, relates the gate voltage to time. Since a constant current is supplied to the gate, the horizontal time scale is directly proportional to the charge supplied to the gate. With a suitable scaling factor, therefore, this oscillogram is a plot of gate voltage versus charge.

The point on the oscillogram of the second voltage rise indicates where the device is fully switched on. During the first voltage rise, the gate-to-source capacitance is charging, and during the flat portion, the gate-to-drain capacitance is charging. This oscillogram therefore clearly differentiates between the charge required for the gate-source and gate-to-drain ("Miller") capacitances. At the second voltage rise, both capacitances are charged to the extent needed to switch the given voltage and current. A more detailed explanation of the interpretation of this data is given later.

The graph in Figure 3 represents gate voltage versus gate charge in nanocoulombs for an IRF130. Although the second voltage rise indicates the point at which the switching operation is completed, normal design safety margins will dictate that the level of drive voltage applied to the gate is greater than that which is just required to switch the given drain current and voltage. The total charge consumed by the gate will therefore in practice be higher than the minimum required — but not necessarily significantly so. For example, the gate charge required to switch 12 A at 80 V is 15 nanocoulombs (point A), and the corresponding gate voltage is about 7 V. If the applied drive voltage has an amplitude of 10 V (i.e. a 3 V margin), then the total gate charge actually consumed would be about 20 nanocoulombs, (point B).

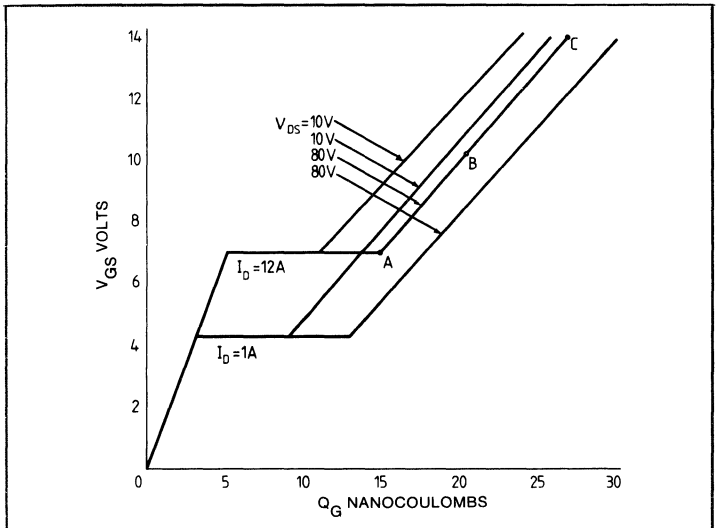


Figure 3. Gate Voltage Versus Gate Charge for the IRF130.

As shown on the graph, whether switching 10 or 80 volts in the drain circuit, there is a much less than proportional difference in the charge required. This is because the "Miller" capacitance is a nonlinear function of voltage, and decreases with increasing voltage.

The importance of the gate charge data to the designer is illustrated as follows. Taking the previous example, about 15 nanocoulombs of gate charge are required to switch a drain voltage of 80 V and a drain current of 12 A. Since the 15 nC gate charge is the product of the gate input current and the switching time, if 1.5 A is supplied to the gate, the device will be switched in 10 ns. It follows that if 15 mA is supplied to the gate, then switching occurs in 1 μs, and so on.

These simple calculations immediately tell the designer the trade-offs between the amount of current available from the drive circuit and the achievable switching time. With gate charge known, the designer can develop a drive circuit appropriate to the switching time required.

Consider a typical practical example of a 100 kHz switcher, in which it is required to achieve a switching time of 100 nanoseconds. The required gate drive current is derived by simply dividing the gate charge, 15 $\times$ 10^{-9}, by the required switching time, 100 $\times$ 10^{-9}, giving 150 mA. From this calculation, the designer can further arrive at the drive circuit impedance. If the drive circuit app-

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lies 14 V to the gate, for instance, then a drive impedance of about 50 ohms would be required. Note that throughout the "flat" part of the switching period (Figure 3), the gate voltage is constant at about 7 V. The difference between the applied 14 V and 7 V is what is available to drive the required current through the drive circuit resistance.

The gate charge data also lets the designer quickly determine average gate drive power. The average gate drive power, P_{DRIVE}, is $Q_G V_{Gf}$. Taking the above 100 kHz switcher as an example, and assuming a gate drive voltage V_G of 14 V, the appropriate value of gate charge Q_G is 27 nanocoulombs (point C on Figure 3). The average drive power is therefore $27 \times 10^{-9} \times 14 \times 10^5 = 0.038$ Watts. Even though the 150 mA drive current which flows during the switching interval may appear to be relatively high, the average power is miniscule (0.004%) in relation to the power being switched in the drain current. This is because the drive current flows for such a short period that the average power is negligible.

Thus actual drive power for MOSFETs is minute compared to bipolar requirements, which must sustain switching current during the entire ON condition. Average drive power, of course, increases at higher frequencies, but even at 5 MHz it would be only 1.9 W.

The Gate Charge Curve

The oscillograms of the gate-to-source voltage in Figure 2 neatly delineate between the charge required for the gate-to-source capacitance, and the charge required for the gate-to-drain, or "Miller" capacitance. The accompanying simplified test circuit and waveform diagram (Figures 4 and 5 respectively) give the explanation.

Before time t_0, the switch S is closed; the device under test (DUT) supports the full circuit voltage, V_{DD}, and the gate voltage and drain current are zero. S is opened at time t_0; the gate-to-source capacitance starts to charge, and the gate-to-source voltage increases. No current flows in the drain until the gate reaches the threshold voltage.

During period t_1 to t_2, the gate-to-source capacitance continues to charge, the gate voltage continues to rise and the drain current rises proportionally. So long as the actual drain current is still building up towards the available drain current, I_D, the freewheeling rectifier stays in conduction, the voltage across it remains low, and the voltage across the DUT continues to be virtually the full circuit voltage, V_{DD}. The top end of the drain-to-gate capacitance C_{GD} therefore remains at a fixed potential, whilst the potential of the lower end moves with that of the gate. The charging current taken by C_{GD} during this period is small, and for practical purposes it can be neglected, since C_{GD} is numerically small by comparison with C_{GS}.

At time t_2, the drain current reaches I_D, and the freewheeling rectifier shuts off; the potential of the drain now is no longer tied to the supply voltage, V_{DD}. The drain current now stays constant at the value I_D enforced by the circuit, whilst the drain voltage starts to fall. Since the gate voltage is inextricably related to the drain current by the intrinsic transfer characteristic of the DUT (so long as operation remains in the "active" region), the gate voltage now stays constant because the "enforced" drain current is constant. For the time being, therefore, no further charge is consumed by the

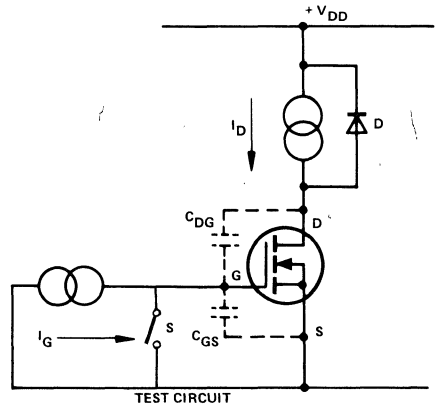


Figure 4. Basic Gate Charge Test Circuit

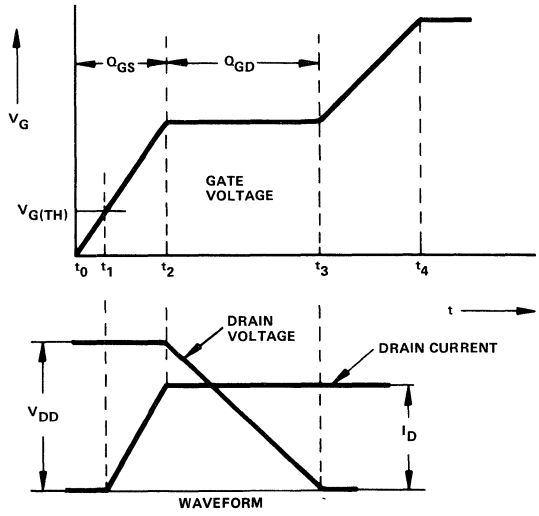


Figure 5. Basic Gate Charge Waveforms

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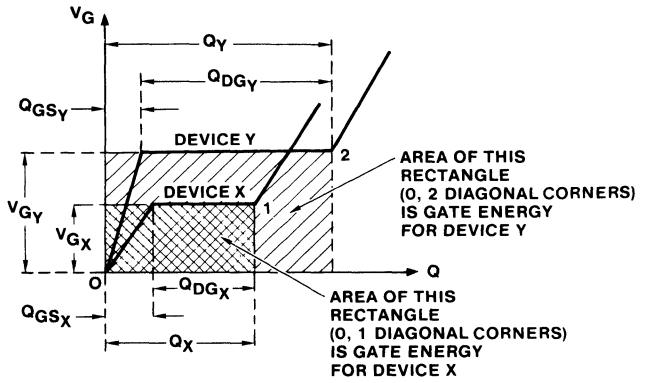


Figure 6. Comparison of Gate Charge Characteristics of Different Device Types.

gate-to-source capacitance, because the gate voltage remains constant. Thus the drive current now diverts, in its entirety, into the "Miller" capacitance C_{GD}, and the drive circuit charge now contributes exclusively to discharging the "Miller" capacitance.

The drain voltage excursion during the period t_2 to t_3 is relatively large, and hence the total drive charge is typically higher for the "Miller" capacitance C_{GD} than for the gate-to-source capacitance C_{GS}. At t_3 the drain voltage falls to a value equal to $I_D \times R_{DS(ON)}$, and the DUT now comes out of the "active" region of operation. (In bipolar transistor terms, it has reached "saturation.") The gate voltage is now no longer constrained by the transfer characteristic of the device to relate to the drain current, and is free to increase. This it does, until time t_4, when the gate voltage becomes equal to the voltage "behind" the gate circuit current source.

The time scale on the oscillogram of the gate-to-source voltage is directly proportional to the charge delivered by the drive circuit, because charge is equal to the product of current and time, and the current remains constant throughout the whole sequence. Thus the length of the period t_0 to t_1 represents the charge Q_{GS} consumed by the gate-to-source capacitance, whilst the length of the period t_2 to t_3 represents the charge Q_{GD} consumed by the gate-to-drain or "Miller" capacitance. The total charge at time t_3 is the charge required to switch the given voltage V_{DD} and current I_D.

The additional charge consumed after time t_3 does not represent "switching" charge; it is simply the excess charge which will be delivered by the drive circuit because the amplitude of the applied gate drive voltage normally will be higher (as a matter of good design practice) than the bare minimum required to accomplish switching.

Beware When Comparing Different Products

Manufacturers sometimes make technical claims for their products that appear to be plausible, but which in actuality do not stand up to scrutiny.

A case in point concerns the input capacitance of a power MOSFET. Statements such as "the input capacitance of device Y is less than that of device X, ergo Y is a faster switch than X", are frequently bandied about, but are just as frequently erroneous.

Apart from the obvious speciousness of many such statements — "apples" are frequently not compared with "apples", and obviously larger chips have more self capacitance than smaller ones — the more basic fundamentals are generally overlooked.

As this application note shows, of "bottom line" importance is the total gate charge required for switching. The lower the charge, the lower is the gate drive current needed to achieve a given switching time.

A general comparison between hypothetical MOSFETs brands "X" and "Y" is illustrated in the Figure. Device X has a higher input capacitance; hence the initial slope of its gate charge characteristic is less than that of device Y. Q_{GS} of device X is, however, about the same as that of device Y, because it has a higher transconductance and therefore requires less voltage on its gate for the given amount of drain current (V_{GX} is less than V_{GY}). The "Miller" charge consumed by device X is considerably less than that consumed by device Y. The overall result is that the total charge required to switch device X, Q_X, is considerably *less* than that required to switch device Y, Q_Y.

Had the comparison between devices X and Y been made on the more superficial basis of input capacitances, it would have been concluded — erroneously — that Y is "better" than X.

Another consideration is the energy required for switching. Again, device X scores handsomely over device Y in this example. The energy is the product of the gate charge and the gate voltage, and is represented by the area of the rectangle whose corner lies at the "switching point". (Point 1 for device X, and point 2 for device Y.) It is obvious that X requires significantly less gate energy than Y.

To summarize: beware of superficial comparisons. Check the full facts before deciding which MOSFET really has the edge in switching performance.□

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Gate Drive Characteristics and Requirements for Power HEXFETs®

By STEVE CLEMENTE

Introduction

The conventional bipolar transistor is essentially a current-driven device. As illustrated in Figure 1(a), a current must be applied between the base and emitter terminals to produce a flow of current in the collector. The amount of a drive required to produce a given output depends upon the gain, but invariably a current must be made to flow into the base terminal to produce a flow of current in the collector.

The HEXFET is fundamentally different; it is a voltage-controlled power MOSFET device. A voltage must be applied between the gate and source terminals to produce a flow of current in the drain (see Figure 1b). The gate is isolated electrically from the source by a layer of silicon oxide. Theoretically, therefore, no current flows into the gate when a DC voltage is applied to it — though in practice there will be an extremely small leakage current, in the order of nanoamperes. With no voltage applied between the gate and source electrodes, the impedance between the drain and source terminals is very high, and only a small leakage current flows in the drain until the applied voltage exceeds the drain-to-source avalanche voltage.

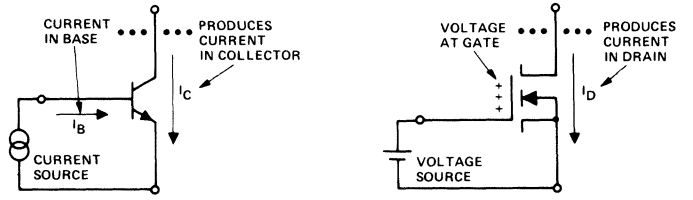
When a voltage is applied between the gate and source terminals, an electric field is set up within the HEXFET. This field modulates the resistance between the drain and source terminals, and permits a current to flow in the drain in response to the applied drain circuit voltage.

Although it is common knowledge that HEXFET transistors are more easily driven than bipolars, a few basic considerations have to be kept in mind in order to avoid a loss in performance or outright device failure.

Gate Voltage Limitations

Figure 2 shows the basic HEXFET structure. The silicon oxide layer between the gate and the source regions can be easily perforated if the gate-to-source voltage exceeds 20V, even if the current is limited to a very low value.

Since the perforation of this oxide layer is one of the most common causes of device failure, great care should be exercised not to exceed the gate-to-source maximum voltage rating. It should be kept in mind, also, that even if the applied gate voltage is kept below the maximum rated gate



(a) Bipolar Transistor (b) HEXFET

Figure 1. Bipolar Transistor is Current Driven, HEXFET is Voltage Driven

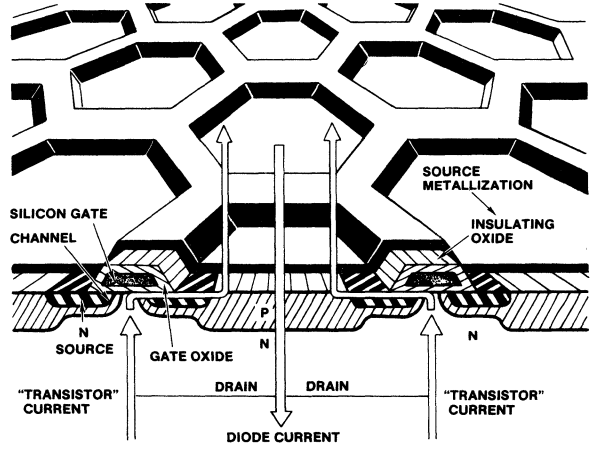


Figure 2. Basic HEXFET Structure

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voltage, the stray inductance of the gate connection, coupled with the gate capacitance, may generate ringing voltages that could lead to the destruction of the oxide layer. Overvoltages can also be coupled through the drain-gate self-capacitance due to transients in the drain circuit. For these reasons, it is advisable to connect a zener diode between gate and source to provide a reliable clamp on the gate voltage. A small resistor or a ferrite bead will normally be adequate to swamp out undesired oscillations.

The Impedance of the Gate Circuit

In comparing power HEXFETs to bipolar transistors, the point is often made that the former require hardly any drive power. This is certainly true, and is the main reason why the drive circuit is normally an order of magnitude simpler than for the bipolar counterparts.

However, whenever more than mediocre performance is required, careful thought should be given to the design and layout of the drive stage, particularly as far as its equivalent internal impedance is concerned. For this reason, a word is in order on the bearing that this internal impedance has on the device performance.

For a device to be turned ON, a certain charge has to be supplied to the gate to raise it to the desired voltage, whether in the linear region, or in the "saturation". Ideally, the best way to achieve this is by means of a voltage source, capable of supplying any amount of current in the shortest possible time. If the device is operated as a switch, a large transient current capability of the drive circuit reduces the time spent in the linear region, thereby reducing the switching losses. On the other hand, if the device is operated in the linear mode, a relatively large current capability in the gate drive circuit minimizes the relevance of the Miller effect, improving the bandwidth of the stage and reducing the harmonic distortion.

The above considerations can be identified with a detailed analysis of the basic switching waveforms at turn-ON and turn-OFF for a clamped inductive load, as shown in Figures 3 and 5. Figure 3 shows the waveforms of the drain current, drain-to-source voltage and gate voltage during the turn-ON interval. For the sake of simplicity, the equivalent impedance of the drive circuit has been assumed

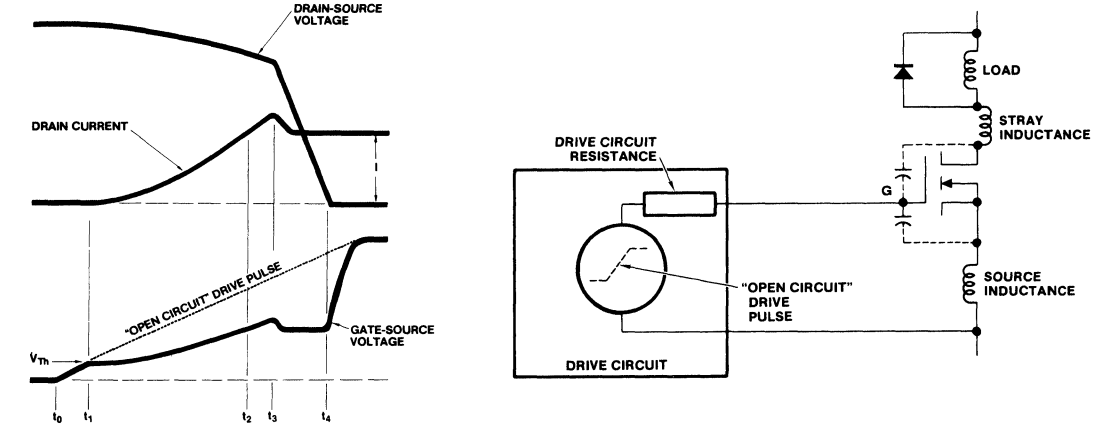


Figure 3. Waveforms at Turn-On

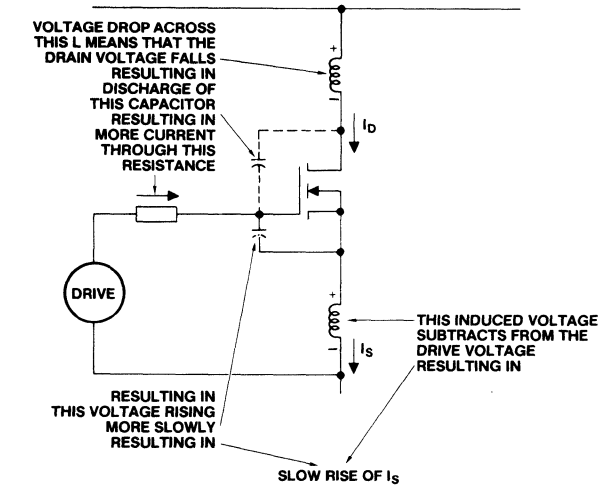


Figure 4. Diagrammatic Representation of Effects When Switching-ON

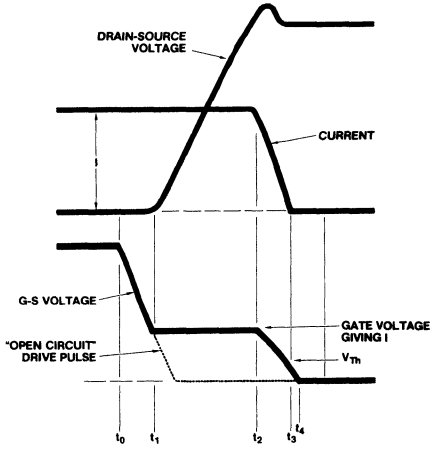


Figure 5. Waveforms at Turn-OFF

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as purely resistive.

At time, t_0, the drive pulse starts to rise. At t_1 it reaches the threshold voltage of the HEXFET, and the drain current starts to increase. At this point, two things happen which make the gate-source voltage waveform deviate from its original "path". First, inductance in series with the source which is common to the gate circuit develops an induced voltage, as a result of the increasing source current. This voltage counteracts the applied gate drive voltage, and slows down the rate of rise of voltage appearing directly across the gate and source terminals; this in turn slows down the rate of rise of the source current. This is a negative feedback effect; increasing current in the source produces a counteractive voltage at the gate, which tends to resist the change of current.

The second factor that influences the gate-source voltage is the so-called "Miller" effect. During the period t_1 to t_2 some voltage is dropped across "unclamped" stray circuit inductance in series with the drain, and the drain-source voltage starts to fall. The decreasing drain-source voltage is reflected across the drain-gate capacitance, pulling a discharge current through it, and increasing the effective capacitive load on the drive circuit. This in turn increases the voltage drop across the source impedance of the drive circuit, and decreases the rate of rise of voltage appearing between the gate and source terminals. Obviously, the lower the impedance of the gate drive circuit, the less this effect will be. This also is a negative feedback effect; increasing current in the drain results in a fall of drain-to-source voltage, which in turn slows down the rise of gate-source voltage, and tends to resist the increase of drain current. These effects are illustrated diagramatically in Figure 4.

This state of affairs continues throughout the period t_1 to t_2, whilst the current in the HEXFET rises to the level of the current, I_M, already flowing in the freewheeling rectifier, and it continues into the next period, t_2 to t_3, whilst the current increases further, due to the reverse recovery of the freewheeling rectifier.

At time t_3 the freewheeling rectifier starts to support voltage, whilst the drain current and the drain voltage start to fall. The rate of fall of drain voltage is now governed almost exclusively by the Miller effect, and an equilibrium condition is reached, under which the drain voltage falls at just the rate necessary for the voltage between gate and source terminals to satisfy the level of drain current established by the load. This is why the gate-to-source voltage falls as the recovery current of the freewheeling rectifier falls, then stays constant at a level corresponding to the drain current, whilst the drain voltage is falling. Obviously, the lower the impedance of the gate-drive circuit, the higher the discharge current through the drain-gate self-capacitance, and the faster will be the full time of the drain voltage.

Finally, at time t_4, the HEXFET is switched fully ON, and the gate-to-source voltage rises rapidly towards the applied "open circuit" value.

Similar considerations apply to the turn-OFF interval. Figure 5 shows theoretical waveforms for the HEXFET in the circuit of Figure 4 during the turn-OFF interval. At t_0 the gate-drive starts to fall. At t_1 the gate voltage reaches a level that just sustains the drain current, I, and the device enters the linear mode of operation. The drain-to-source voltage now starts to rise. The Miller effect governs the rate-of-rise of drain voltage, and holds the gate-to-source voltage at a level corresponding to the constant drain current. The lower the impedance of the drive circuit, the greater the charging current into the drain-gate capacitance, and the faster will be the rise time of the drain voltage. At t_3 the rise of drain voltage is complete, and the gate voltage and drain current start to fall at a rate determined by the gate-source circuit impedance.

In some circuit configurations, even if the performance is of no great concern, it may be important to minimize the impedance in the gate drive circuit to minimize unwanted voltage transients on the gate. With reference to Figure 6, when one HEXFET is turned ON or OFF, a step of voltage is applied between drain and source of the other device on the same leg. This step of voltage is coupled to the gate through the gate-to-drain capacitance, and it can be large enough to turn the device ON for a short instant.

To prevent this from occurring, the gate circuit impedance and/or the rate-of-rise of the step have to be reduced to the extent that the voltage coupled to the gate is below the threshold voltage or some other suitably chosen safe value.

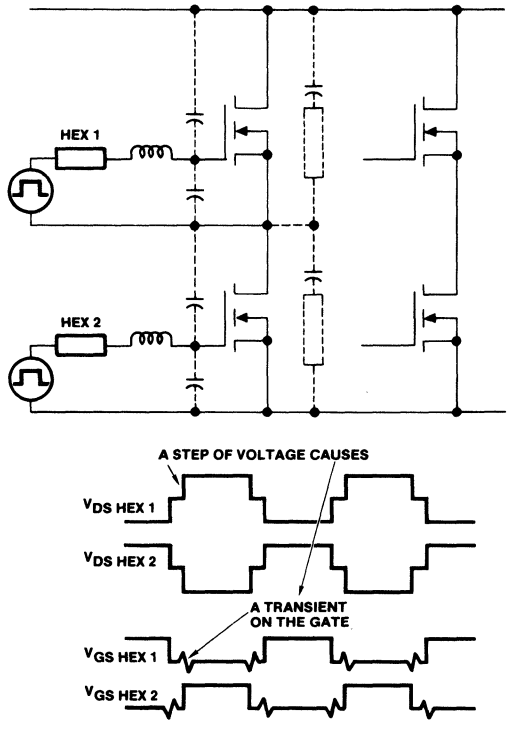


Figure 6. Transients of Voltage Induced on the Gate by Rapid Changes on the Drain-to-Source Voltage

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Driving HEXFETs From TTL

Table 1 shows the guaranteed sourcing and sinking currents for different TTL families at their respective voltages. From this table, taking as an example the 74LS series, it is apparent that, even with a sourcing current as low as 0.4 mA, the guaranteed logic one voltage is 2.4V (2.7 for 74LS and 74S), and that is lower than the possible threshold of a HEXFET. The use of a pull-up resistor on the output (Figure 7) would take this voltage up to 5V, but it would still not be sufficient to guarantee "saturated" switching of the HEXFET, unless the current to be switched is substantially less than the rated value of the HEXFET.

More specifically, with reference to the output characteristics (Figure 3 of the data sheet), it can be seen that for a low voltage device (e.g., IRF130) the drain current corresponding to a gate voltage of 5V is approximately half its DC rated value, while for a high voltage device (e.g., IRF330) it is higher than the DC rated current. It should be emphasized though, that the curves show typical values and that, with a V_{GS} = 5V, saturation is not guaranteed for either DC or pulse rated conditions for any device.

Figure 8 shows a typical application of a TTL inverter driving a IRF320 with the waveforms that would normally be expected. The 74LS05 is an open collector device, but waveforms do not change significantly for a totem pole device. With reference to the drain voltage (bottom waveform) it is apparent that the device turns on much more slowly than it turns off. This is because the gate-to-source and gate-to-drain capacitances are charged exponentially through the pull-up resistor, while they are discharged through a saturated bipolar

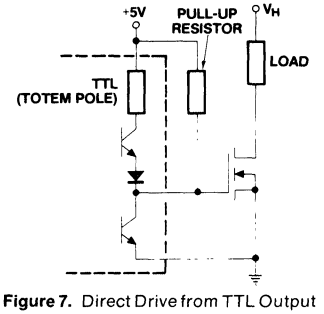
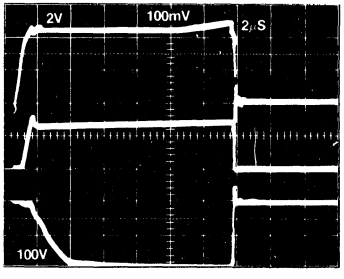


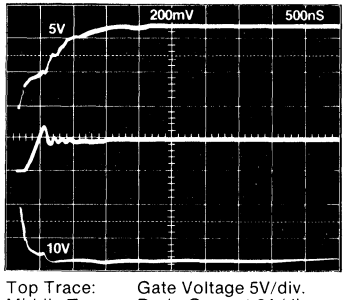
Figure 7. Direct Drive from TTL Output

Table 1. Driving HEXFETs from TTL (Totem Pole Outputs)

Logic Conditions	54/74	54H/74H	(54L)/ 74L	(54LS)/ 74LS	74S
Logic Zero Min. sink current for V_{OL}	16mA ≤0.4V	20mA ≤(0.4V)/	(2)/3.6mA ≤(0.3V)/ 0.4V	(4)/8 ≤(0.4V)/ 0.5V	20mA 0.5V
Logic One Max. source current for V_{OH}	-0.4mA ≥2.4V	-0.5mA ≥2.4V	-0.2mA ≥2.4V	-0.4mA ≥(2.5)/ 2.7V	-1.0mA ≥2.7V
Typical Gate Propagation Delay	10ns	7ns	50ns	12ns	4ns



Top Trace: Gate Voltage 2V/div.
Middle Trace: Drain Current 1A/div.
Bottom Trace: Drain Voltage 100V/div.
Time Scale: 2μs/div.



Top Trace: Gate Voltage 5V/div.
Middle Trace: Drain Current 2A/div.
Bottom Trace: Drain Voltage 10V/div.
Time Scale: 500ns/div.

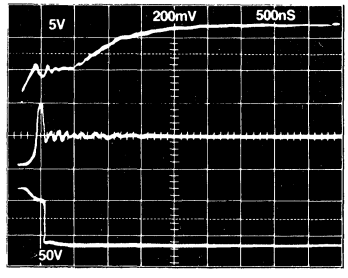


Figure 10. Waveforms Associated with the Circuit in Figure 9, at Different Drain Voltage. Same Scales except Bottom Trace: 100V/div.

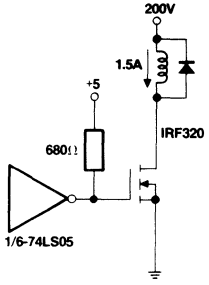


Figure 8. Waveforms Associated with a HEXFET Driven by a TTL Gate

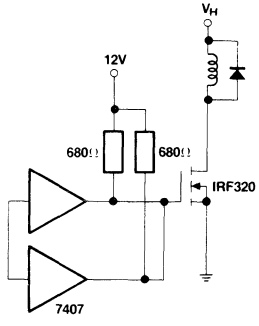


Figure 9. Waveforms Obtained with High Voltage TTL Driver

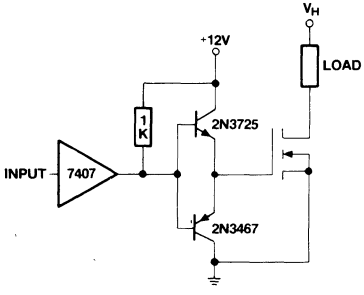


Figure 11. Simple Interface to Drive HEXFETs from TTL

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transistor. The waveforms show also, that the device stays in the linear region for 9 microseconds and that, at the end of this time, the gate is finally free to rise to 5V, after the gate-to-drain capacitance has been fully charged. The main reason for such a poor performance is, of course, the fact that the maximum voltage available on the gate is 5V. The performance improves substantially if two or three gates are connected in parallel to charge or discharge this capacitance.

For guaranteed "saturation" and fast switching, high voltage open collector buffers can be used (7406, 7407, etc.), possibly with several devices connected in parallel.

Figure 9 shows the waveforms that can be obtained with two parallel high voltage drivers pulled up to 12V. Whilst a dramatic improvement can be seen with respect to Figure 8, the performance is still well below what can ultimately be obtained from a HEXFET. The waveforms in Figures 9 and 10 are for the same device, with the same drive circuit and the same drain current, but with different drain voltages. At higher voltages, C_{GD} takes a longer time to discharge, so the device stays in the linear region for more than 0.5 microseconds before reaching saturation.

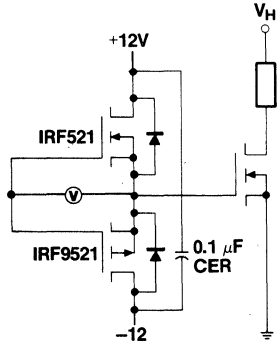


Figure 12. High Performance Driver

Whenever better switching performance is required, interface circuits should be added to provide fast current sourcing and sinking to the gate capacitances. One simple interface circuit is the one shown in Figure 11.

It is a complementary emitter follower stage, capable of sinking or sourcing approximately 1A. The choice of the output transistor is important when switching times have to be in the order of 40ns.

They should have good gain at high currents to be capable of delivering whatever current is required by the Miller effect during the allowed switching time. To gain a better insight on the operation of these transistors, we can attempt a rough calculation of the current they have to supply in a switching operation. Disregarding for a moment the Miller effect, if C_{GS} is 700pF (IRF330) and we want to charge it linearly to 12V in 40ns, a current pulse is required equal to:

$$I = \frac{C_{GS} \times V_{GS}}{t_s}$$

$$= \frac{0.7 \times 10^{-9} \times 12}{40.10^{-9}} = 0.21A$$

In the simplistic assumption that the gate-to-drain capacitance is discharged in the same time, assuming a drain voltage of 200V, we have:

$$I = \frac{C_{DG} \times V_{DS}}{t_s}$$

$$= \frac{40 \times 0.10^{-12} \times (200\text{-}12)}{40\ 10^{-9}} = 0.188A$$

In the final assumption that the two currents add up and that the switching frequency is 100kHz, we can obtain an approximate figure for the power lost in one driver transistor:

$P = V_{CE} \times I_C \times t_s \times f = 1 \times 0.398 \times 40.10^{-9} \times 100\ 10^3 = 1.6mW$

The conclusion is that the driver devices have to be capable of supplying 0.4A without significant voltage drop, but that hardly any power is dissipated in them. Core drivers (2N3725, 2N3244), seem to be the most suitable devices. Unfortunately, the gain of these devices drops very fast for currents over 0.5A. Audio drivers (2N5320, 2N5322), have better gain at high currents but are slower. A double buffer stage may be advisable in some applications with fast switching bipolar devices (2N-2369A and 2N4208 or MPS2369 and MPS3640) driving two HEXFETs, as shown in Figure 12.

Buffer stages can also be implemented with special purpose integrated circuits like the ones shown in Figure 13. These buffers have guaranteed switching times and high current sourcing and sinking capability. Furthermore, they are directly compatible with 5V TTL.

Driving HEXFETs from C-MOS

While the same general considerations presented above for TTL would also apply to C-MOS, there are three substantial differences that should be kept in mind:

1. C-MOS has a more balanced source/sink characteristic that, on a first approximation, can be thought of as a 500 ohm resistance for operation over 8V and a 1k ohm for operation under 8V (Table 2).
2. C-MOS can operate from higher supply voltages than 5V so that HEXFET saturation can be guaranteed.
3. Switching times are longer than TTL (Table 2).

When C-MOS outputs are directly coupled to the gate of a HEXFET, the dominant limitation to performance is not the switching time, but the internal impedance (assuming that C-MOS are operated from a 10V

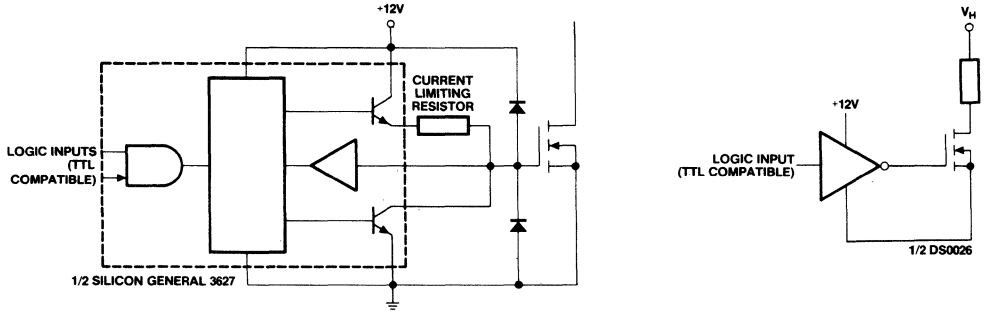


Figure 13. Buffer Stages Implemented with Special Purpose Drivers

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or higher voltage supply). It will certainly not be able to turn OFF the HEXFET as fast as the TTL, while the turn-ON waveform will be slightly better than what can be achieved with a 7407 with a 680 ohm pull-up resistor. Of course, gates can be paralleled in any number to lower the impedance and this makes C-MOS a very simple and convenient means of driving HEXFETs. Drivers can also be used, like the 4049 and 4050 which have a much higher current sinking capability (Table 2), but they do not yield any significant improvement in current sourcing.

For better switching speeds, buffer circuits should be considered, not only to provide better current sourcing and sinking capability, but also to improve over the switching times of the C-MOS output itself. The circuit shown in Figure 11 (without the pull-up resistor which would not be needed), and Figure 12 will improve the drive capability, while the circuits in Figure 13 will improve both drive capability and switching times, but require a TTL compatible drive signal (5V). Another possibility, of course, is to interface C-MOS to TTL and then use the TTL drive circuits.

Driving HEXFETs From Linear Circuits

The complementary emitter follower configuration of Figure 11 can also be used in linear applications to improve drive capability from an op-amp or other analog source (Figure 14).

Table 2. Driving HEXFETs from C-MOS (Buffered)

	Standard Buffered Outputs			4049/4050 Drivers		
Logic Conditions \ Logic Supply Voltage	5V	10V	15V	5V	10V	15V
Logic Zero: Approximate sink current for $V_{OL} \leq 1.5V$	1.5mA	3.5mA	4mA	20mA	40mA	40mA
Logic One: Minimum source current for V_{OH}	-0.51mA $\geq$4.6V	-1.3mA $\geq$9.5V	-3.4mA $\geq$13.5V	-1.25mA $\geq$2.5V	-1.25mA $\geq$9.5V	-3.75mA $\geq$13.5V
Typical switching times of logic drive signals:						
RISE	100ns	50ns	40ns	100ns	50ns	40ns
FALL	100ns	50ns	40ns	40ns	20ns	15ns

If the driving signal is generated by an operational amplifier, the use of power operational amplifiers (e.g., μA791) that can supply as much as 1A can be considered. In practice, their slew rate is so low (0.5V/μs) that their current capability would be redundant and the usable bandwidth would be less than 25kHz. A larger bandwidth can be obtained with better operational amplifiers followed by a current booster, like the ones shown in Figures 15 or 16. For a system bandwidth of 1MHz, the op-amp bandwidth must be significantly higher than 1MHz and its slew rate at least 30V/μs. Presently, there are several devices capable of this performance, e.g., LF157, LM110, μA715, HA2620, etc. If a larger bandwidth is needed, special purpose current amplifiers can be used, like the HA2630 (bandwidth 8MHz, slew rate 500V/μs, 0.4A output current) or very fast operational amplifiers like the NE5539 (bandwidth 48MHz, slew rate 600V/μs) followed by a current booster.

When analog signals determine the switching frequency or duty cycle of a HEXFET, as in PWM applications, a voltage comparator is normally used to command the switching. Here, too, the limiting factors are the slew rate of the comparator and its current drive capability. Response times under 40ns can be obtained at the price of low output voltage swing (TTL compatible) and this implies the use of output buffers like the ones shown in Figures 9, 11, 12 and 13. If better switching speeds

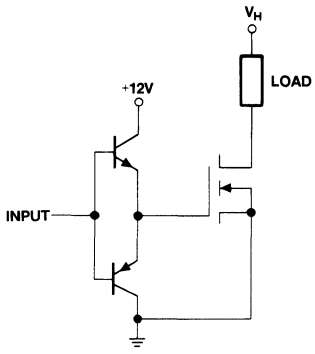


Figure 14. Current Booster for Analog Applications

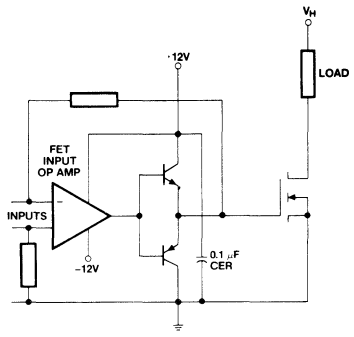


Figure 15. Dual Supply Op-Amp Drive Circuit

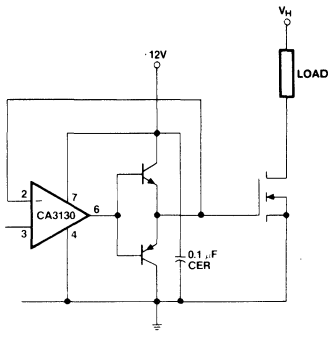


Figure 16. Single Supply Op-Amp Drive Circuit (Voltage Follower)

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are desired, a fast op-amp should be used. Figure 17 shows a typical comparator connection.

In many applications, when the HEXFET is turned on, current transfers from a freewheeling diode into the HEXFET. If the switching speed is high and the stray inductances in the diode path are small, this transfer can occur in such a short time as to cause a reverse recovery current in the diode high enough to destroy it. For this reason, it may be necessary to slow down the turn-on of the HEXFET while leaving the turn-off as fast as practical. Pulse shaping circuits can be used for this purpose, like the ones in Figures 18 and 19.

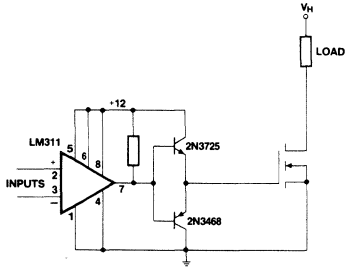


Figure 17. Comparator Drive

In linear applications, the use of special circuits like the LM391 audio driver with an output booster can be considered. The LM391 has separate source and sink outputs.

Drive Circuits Not Referenced to Ground

To drive a HEXFET into saturation, an appropriate voltage must be applied between the gate and source. If the load is connected between source and ground, and the drive voltage is applied between gate and ground, the effective voltage between gate and source decreases as the device turns on. An equilibrium point is reached in which the amount of current flowing in the load is such that the voltage between gate and source maintains that amount of drain current and no more.

For this reason, it is often advantageous to have the gate drive circuit referenced to the source rather than to the ground. There are basically three ways of floating the gate drive circuit with respect to ground:

1. By means of optically coupled isolators.
2. By means of pulse transformers.
3. By means of DC to DC chopper circuits with transformer isolation.

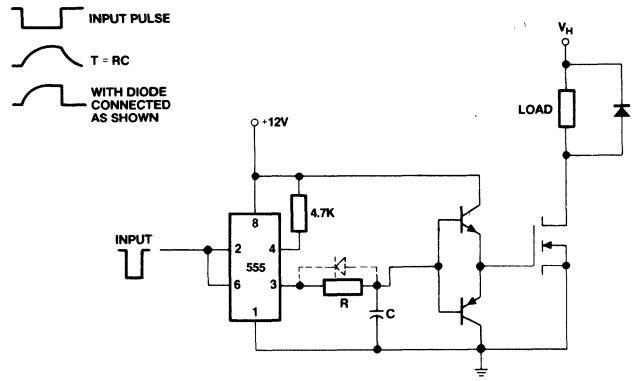


Figure 18. 555 as Schmitt Trigger in a Pulse Shaping Application

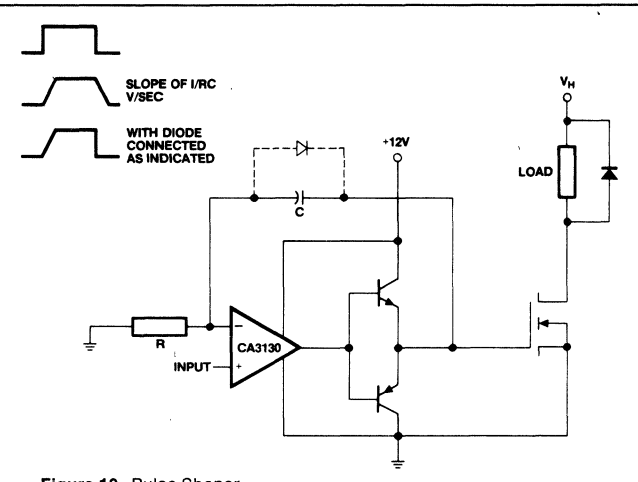


Figure 19. Pulse Shaper

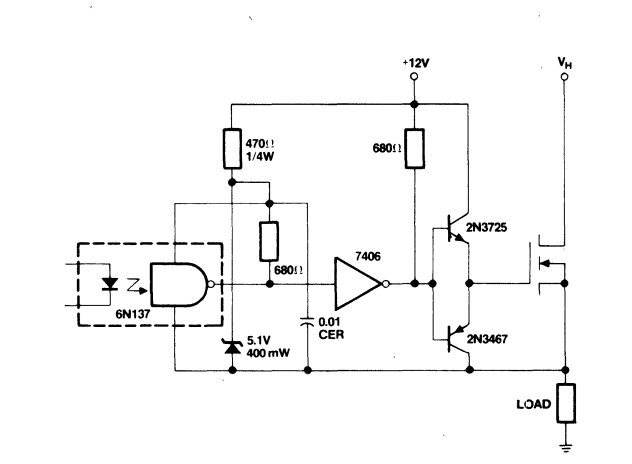


Figure 20. Opto Coupler Drive Circuit

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Opto couplers require a separate supply grounded to the source on the receiving end of the optical link. Optically coupled gates (TTL compatible) are available with 50ns delay times and 25ns rise and fall times. They can be used to a few MHz, but they require a booster stage at the output, as shown in Figure 20. C-MOS level translators, like the 4504, could be used in place of the 7406. If speed is not a major factor, a simplified circuit can be used like the one shown in Figure 21.

The Schmitt trigger function of the 74C14 could be accomplished with a 555, which has fairly good switching and driving capabilities (100ns, 0.2A).

One of the major difficulties encountered in the use of opto couplers is their susceptibility to noise. This is of particular relevance in applications where high currents are being switched rapidly. They do, however, offer a simple means of transmitting a signal that contains a DC component. Pulse transformers, on the other hand, can only transfer to the secondary the AC component of the input signal. Consequently, their output voltage swings from negative to positive by an amount that changes with the duty cycle. Furthermore, whatever leakage inductance the transformer has, reduces its effectiveness as a gate drive circuit. To overcome these difficulties, a signal conditioning stage may be necessary; this requires a separate power supply. It remains, however, a reliable approach with high noise immunity, whenever the duty cycle has a fixed known minimum.

Chopper circuits are fairly complex, expensive and limited in bandwidth and performance. They do have their advantages, though, like the possibility of transferring a DC component, noise immunity and the fact that with some additional circuitry, the separate supply can be avoided.

Considering the small amount of power that is required to drive the gate of a HEXFET, it may be possible in some applications to develop a supply for the gate drive circuit directly from the drain voltage. Figure 22 shows a possible way implementing such a circuit. □

If the duty cycle is small, or the frequency is low, the circuit in Figure 23 should be considered. The size of Q, R, and C depend on the duty cycle of the drain voltage waveform as well as its frequency and the amount of gate capacitance that has to be driven.

Obviously, this circuit will not work if the HEXFET may be kept in the on-state for an undetermined period of time and there is lower frequency limit below which C becomes quite large and the circuit is not attractive any longer. □

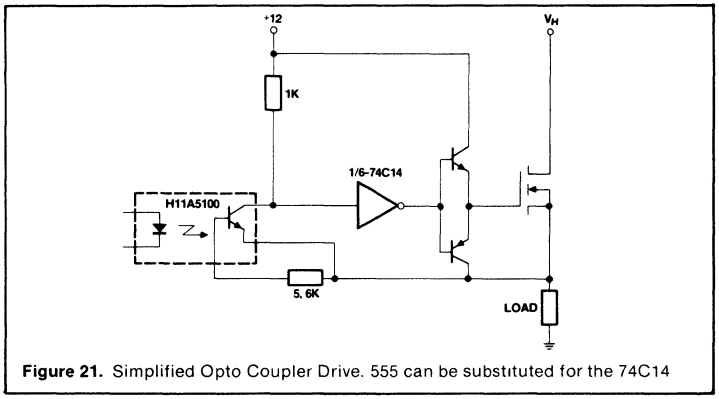


Figure 21. Simplified Opto Coupler Drive. 555 can be substituted for the 74C14

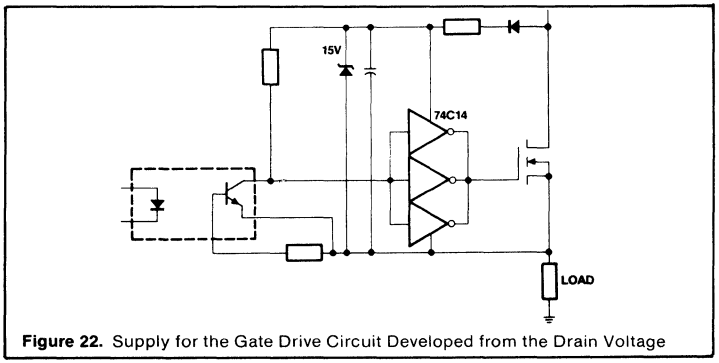


Figure 22. Supply for the Gate Drive Circuit Developed from the Drain Voltage

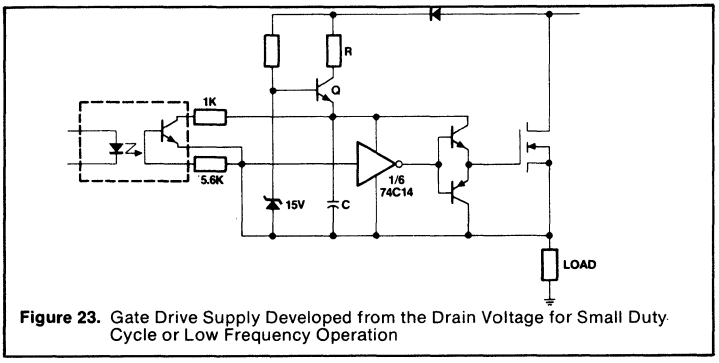


Figure 23. Gate Drive Supply Developed from the Drain Voltage for Small Duty Cycle or Low Frequency Operation

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The HEXFET® Integral Body Diode — Its Characteristics and Limitations

By S. CLEMENTE, B.R. PELLY, and B. SMITH

Summary

All power HEXFETs have an integral reverse rectifier or "body diode" built into them. The current rating of the reverse rectifier is equal to that of the transistor. This article details the characteristics of the body diode, and shows where and how to use it.

Introduction

A not too well-known feature of HEXFETs (actually in general, of all power MOSFETs) is that they inherently have built into them an integral reverse p-n junction rectifier or "body diode." This is illustrated in the equivalent circuit diagram of Figure 1. Far from being an inconsequential "parasitic" component, the integral body diode is a real circuit element with a current handling capability as high as that of the transistor itself, and, as it normally happens with practical circuit components, its own set of characteristics and limitations.

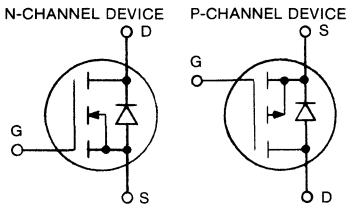


Figure 1. Complete Symbols for the HEXFET

The integral body diode may or may not be important in a practical circuit. In some applications it is irrelevant, because the circuit operation is such that the voltage across the transistor never reverses; hence, the forward conduction characteristic of the diode never comes into play. Other circuits require the switching device to support "negative" voltage as well as "positive" voltage. In that event, a rectifier must be connected in series with the HEXFET, because the integral body diode does not allow it to support "negative" voltage. This is no different, of course, than with a bipolar transistor, which also cannot support significant reverse voltage (but, unlike the HEXFET, nor can it carry significant reverse current).

There are other circuits which actually require a "reverse" rectifier across the switching device. In these circuits, it will often be possible to utilize "free of charge" the integral body diode built into IR's HEXFET, thereby obviating the need for additional discrete rectifiers in the circuit. This *can* be a significant added bonus of using the HEXFET, though, as will be seen, certain precautions *may* be necessary.

The purpose of this application note is to discuss some of the uses, as well as the characteristics, ratings and limitations of the integral body diode in IR's HEXFETs. Solutions to the potential circuit problems will be considered, and design procedures given. The intention is to give the circuit designer the information he needs to assess the importance and applicability of this "hidden" component in IR's HEXFETs.

Some Basic Circuit Applications

The following discussion deals with various circuit examples; this will give a basic understanding of where the reverse rectifier is important, and where it can be utilized.

First, there are circuits in which the reverse rectifier has no effect. The flyback converter shown in Figure 2a is an example. Here, the voltage across the HEXFET is always positive; the integral body diode plays no part in the circuit operation, and it stays unobtrusively in the background. The same is true in the "forward" converter circuit, shown in Figure 2b. There are many circuits of this type.

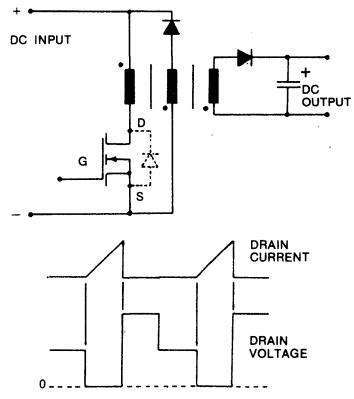


Figure 2a. Flyback Converter Circuit

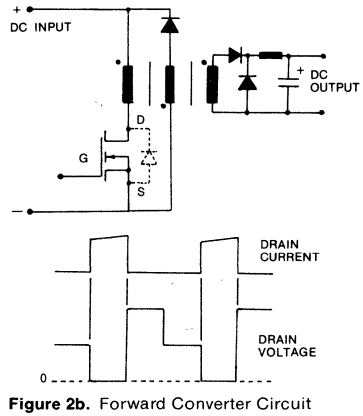


Figure 2b. Forward Converter Circuit

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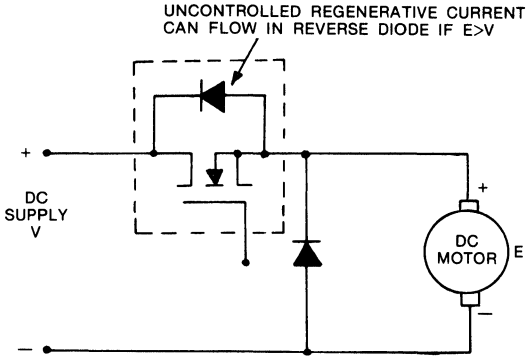


Figure 3. DC Chopper Circuit for Motor Speed Control

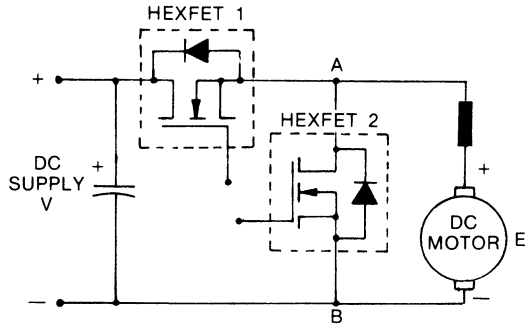


Figure 4a. HEXFET Circuit for Providing Speed Control and Regenerative Braking of DC Motor

The integral body diode has no obvious effect upon the operation of the DC to DC chopper circuit shown in Figure 3. If a situation could arise, however, where the motor is driven at overspeed by an "overhauling" load, "uncontrolled" current would flow through the integral body diode. If this can occur, then a rectifier should be connected in series with the HEXFET, to prevent the flow of energy back to the DC source, assuming that a regenerative braking facility is not required.

If, on the other hand, it is required to provide a controlled regenerative braking facility, then this can be neatly furnished by the circuit shown in Figure 4a, which utilizes two HEXFETs. For the motoring mode of operation, HEXFET 1 is chopped on and off at some suitable repetition rate, typically a few hundred Hz to a few kHz, to provide control of the average level of voltage applied to the motor. HEXFET 2 is off, but its integral body diode acts as the conventional free-wheeling rectifier, and carries the motor current when HEXFET 1 is instantaneously off.

For the regenerative braking mode of operation, HEXFET 2 is chopped on and off, to control the regenerative current fed back from the motor. HEXFET 1 is off, but its integral body diode carries the motor current when HEXFET 2 is instantaneously off, thus carrying the motor current back into the DC supply. Theoretical operating waveforms are shown in Figure 4b.

Another example of the use of the integral body diode is shown in Figure 5. Here, two HEXFETs connected in series opposition form a bi-directional AC switch. When control terminal 3 is driven positive with respect to control terminal 4, both HEXFETs are on, and the switch is closed for current flow in either direction. Current in one

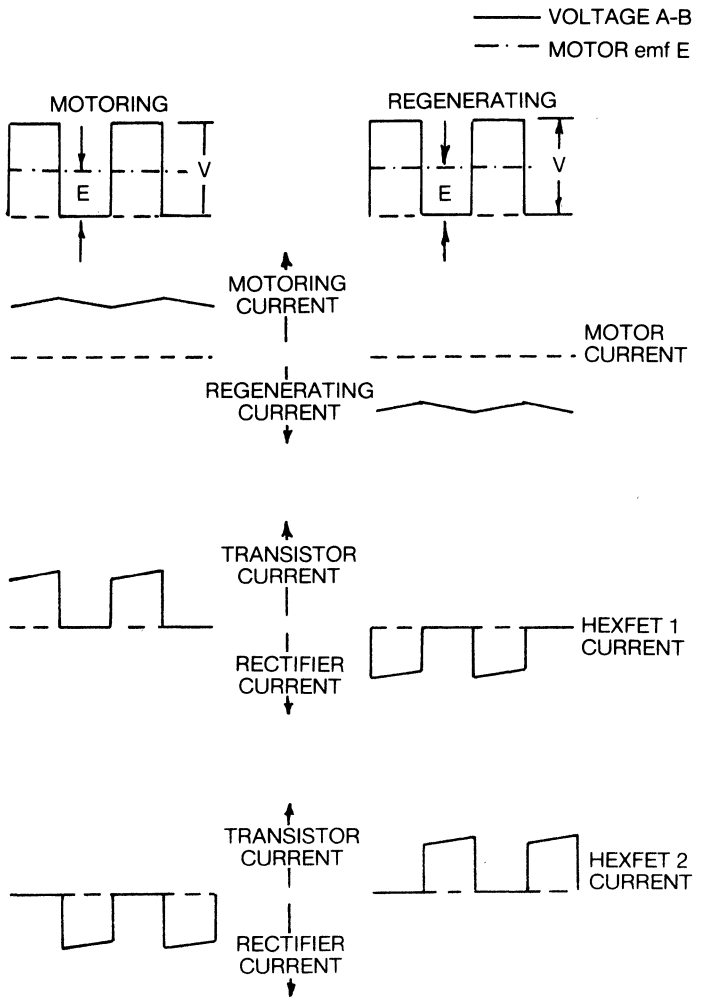


Figure 4b. Operating Waveforms for Circuit of Figure 4a.

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direction flows via the transistor of HEXFET 1 and the body diode of HEXFET 2; in the other, it flows through the transistor of HEXFET 2 and the body diode of HEXFET 1. When control terminal 3 is driven to the same potential, or negative, with respect to control terminal 4, the AC switch is off, and it blocks voltage in either direction.

Perhaps the most obvious use of the integral body diode built into IR's HEXFETs is in voltage-fed DC to AC inverter circuits of the types commonly used for switching power supplies, motor speed controllers, and general purpose AC power supplies. In these types of circuit, the basic principle is to switch the DC supply voltage in alternating directions across the load, in accordance with a prescribed switching pattern. The waveform of the output current is determined by the characteristics of the load.

For all loads other than purely resistive, there are intervals during which the polarity of the output current is instantaneously opposite to that of the impressed voltage. This means that each switch within the inverter must be capable of carrying current in the "reverse" direction. In a conventional inverter circuit, this facility is provided by connecting a reverse rectifier across each switching device. These rectifiers are often known as "reactive feedback" rectifiers.

The integral body diode in the HEXFET can automatically serve as the reactive feedback rectifier. A simple "half bridge" DC to AC inverter circuit operating from a "split" DC supply is shown in Figure 6a. The circuit can be operated in a simple square wave mode, in which case a single voltage pulse is produced for each half cycle of the output, or it can be operated in a more complex "multi-pulse" mode, with many voltage pulses being produced for each fundamental output half cycle. This latter technique significantly reduces the harmonic distortion at the output.

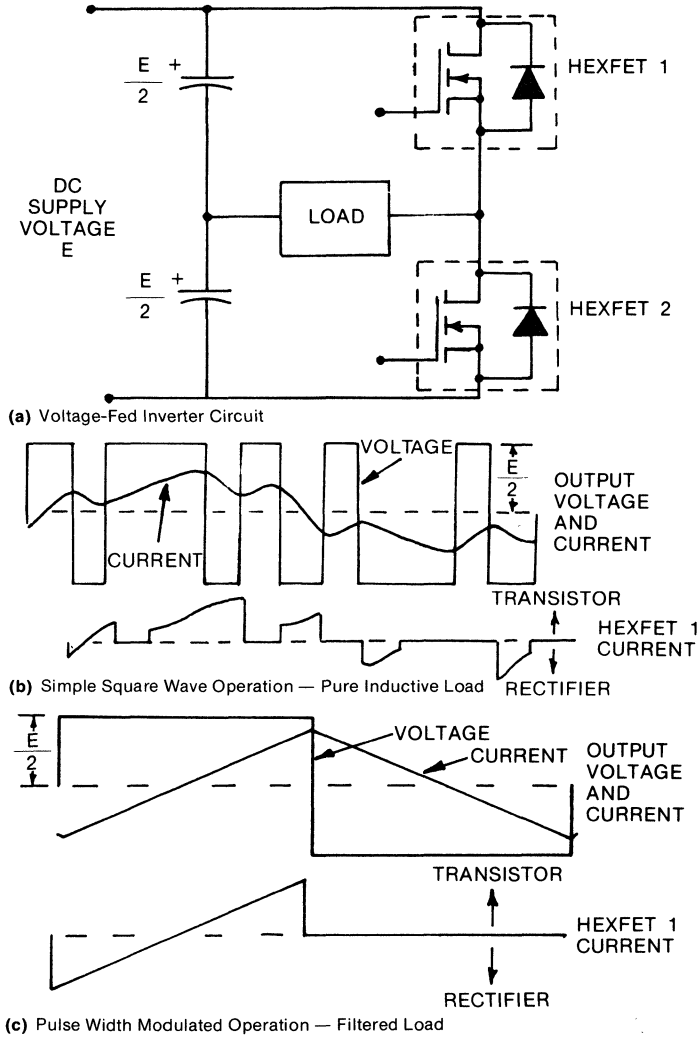


Figure 6. Simple Voltage-Fed Inverter and Theoretical Operating Waveforms

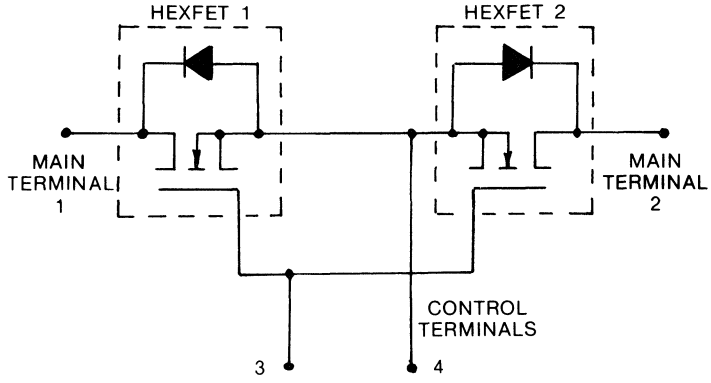


Figure 5. Bidirectional AC Switch Using Two HEXFETs in Series Opposition

These two operating techniques are illustrated by the waveforms in Figures 6b and 6c respectively. These waveforms show that current flows both in the "positive" direction, through the transistor, and in the "negative" direction, through the integral body diode, during separate intervals. The "reactive feedback" rectifiers, therefore, play an essential and important role in the operation of the circuit.

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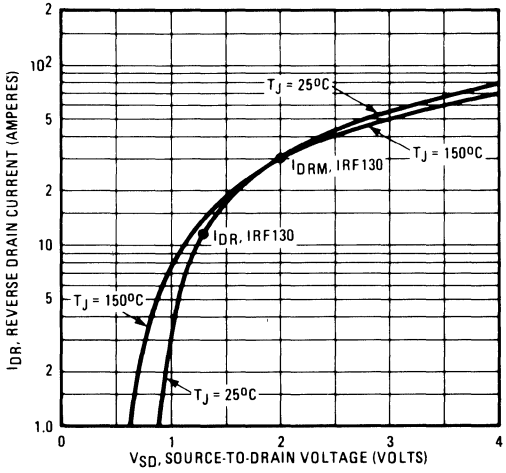


Figure 7a. Conduction Voltage Drop vs. Current in Integral Reverse Rectifier (IRF130, 530, Series HEXFET)

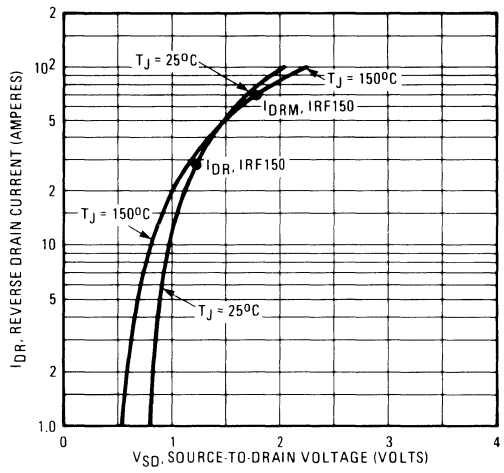


Figure 7b. Conduction Voltage Drop vs. Current in Integral Reverse Rectifier (IRF150 Series HEXFET)

Ratings and Characteristics of the Reverse Rectifier

The integral body diode built into the HEXFET consists basically of a conventional p-n junction. Its electrical characteristics, therefore, are basically those of a conventional silicon rectifier.

Current Ratings

The peak current rating of the integral body diode I_{DRM}, defines the maximum permissible peak "rectifier" current, just as the peak current rating of the transistor, I_{DM}, defines the maximum permissible peak "transistor" current. The "rectifier" and "transistor" peak current ratings are the same as one another, as also are the RMS ratings.

Conduction Voltage

Relationships between the conduction voltage drop of the integral diode and the instantaneous current through it, at junction temperatures of 25°C and 150°C, are shown in Figure 7. The rated pulsed current level, I_{PK}, is indicated for reference on these diagrams. The voltage drop across the integral body diode is relatively low, and ranges between 1 to 2V at normal operating currents.

A point of interest is that the conduction voltage drop of the integral body diode can be modified by applying positive drive voltage to the gate of the HEXFET. Figure 8 shows what happens as the gate to source voltage is increased. At low current levels, the conduction voltage drop across the rectifier decreases as the drive voltage is increased.

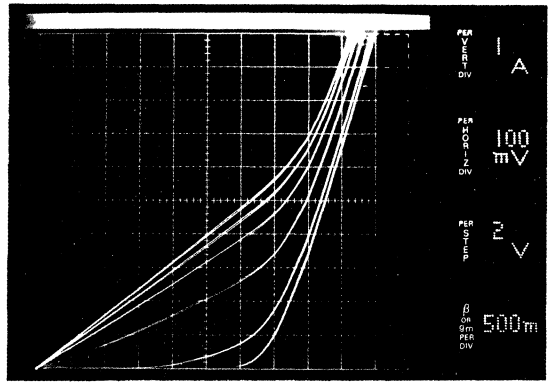


Figure 8. Typical Curves of forward conduction voltage vs. current through integral reverse rectifier, with varying amounts of applied gate-source voltage. IRF130 V_{GS} = 0, + 2, + 4, + 6, + 8, + 10V.

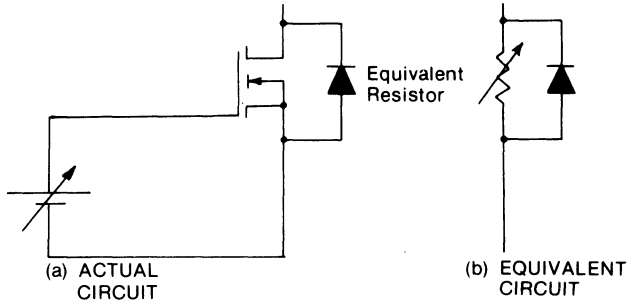


Figure 9. Varying applied gate voltage results in varying equipment resistor across reverse rectifier.

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The physical explanation for this is simple. As the gate voltage is increased, the channel resistance of the transistor reduces due to the applied electric field, just as it does for the normal "transistor" direction of current flow. The reverse rectifier is thus shunted by the channel resistance, and the equivalent circuit is as shown in Figure 9.

At low current levels, the voltage drop across the channel resistance is lower than it would be across the rectifier on its own, and most of the current flows through the equivalent resistor. As the current is increased, the voltage drop across the rectifier is lower than it would be across the resistor in its own; most of the current now flows through the rectifier. The resistor then has little effect, and the influence of the applied gate drive voltage is minimal.

Reverse Recovery

An important practical consideration is the reverse recovery characteristic of the integral body diode. This diode is a conventional p-n junction, and therefore it exhibits a classical reverse recovered charge; that is to say, when the diode switches off, the current through it reverses for a short period, as illustrated in Figure 10.

Values of t_a and t_b* for values of initial conduction current and di/dt other than those indicated in the data sheet can be estimated from the approximate normalized relationships shown in Figure 11.

The reverse recovery of the integral body diode must be carefully considered in the design of a practical circuit, and it may be necessary to make definite provisions to alleviate its effect. This is discussed in the next section.

*The minimum values of t_b are important because it defines the degree of "softness" of recovery, and hence also the level of voltage transient induced in circuit inductance during this period.

Rectifier Reverse Recovery -Circuit Considerations-

The HEXFET's integral body diode exhibits minority carrier reverse recovery. Reverse recovery presents a potential problem when switching any rectifier off; the slower the rectifier, the greater the problem. The HEXFET's rectifier is relativey fast — not as fast as the fastest discrete rectifiers available, but considerably faster than comparably related conventional general purpose rectifiers. By comparison with the HEXFET itself, on the other hand, the switching speed of the integral reverse rectifier is quite slow. The switching speed of a circuit utilizing the reverse rectifier of the HEXFET

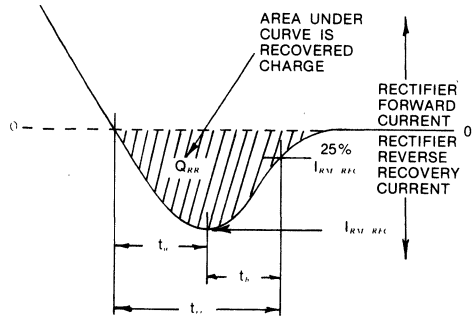


Figure 10. Rectifier Reverse Recovery

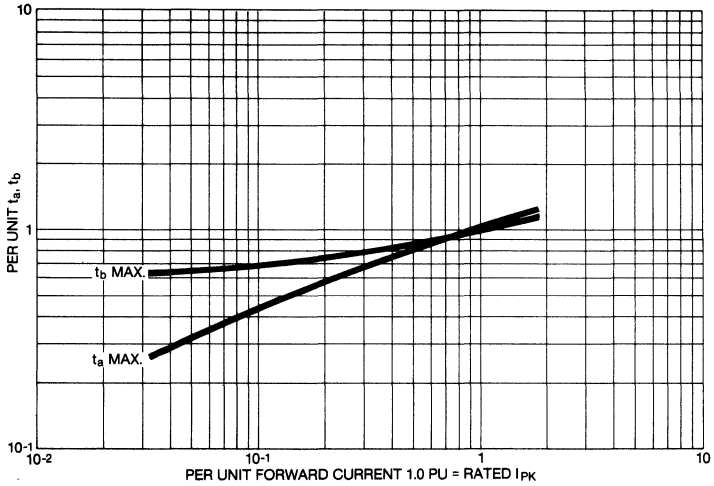


Figure 11a. Approximate correction factors for t_a and t_b as function of per unit initial forward rectifier current

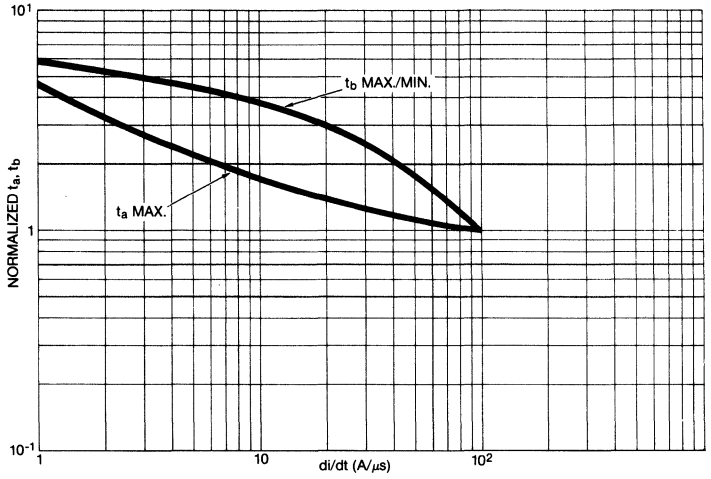


Figure 11b. Approximate Correction Factors for t_a and t_b as function of di/dt

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may therefore be limited by the rectifier. Whether this will be so depends upon the circuit and the operating conditions, as discussed later.

The most common applications of the HEXFET in which the switching speed, and hence frequency, will potentially be limited by the rectifier, are DC to DC choppers and inverters for regulated power supplies, electric motor controllers, and so on, in which "multiple" voltage pulses are used.

Effect of Reverse Recovery on Circuit Operation

Regardless of the overall circuit configuration, or the particular application, the "local" circuit operating situation that is troublesome occurs when free-wheeling current from an inductive load is commutated from the reverse rectifier of one HEXFET to the transistor of an "opposite" HEXFET, the two devices forming a tandem series connected pair across a low impedance voltage source. This "local" circuit configuration occurs in most chopped and inverter schemes. The operating sequence is depicted in Figure 12 and associated theoretical operating waveforms are shown in Figure 13.

Throughout the commutating sequence, which of course is short by comparison with the overall fundamental operating cycle of the circuit, a constant current I_o flows through an external inductive load. During the operating period t_o, the current I_o flows through the rectifier of HEXFET 2. At the start of the operating period t_1, HEXFET 1 is turned on, and the load current starts to transfer to the transistor of HEXFET 1. The current i_1 in HEXFET 1 increases, whilst the current i_2 flowing in the rectifier of HEXFET 2 decreases. The sum of i_1 and i_2 is equal to I_o. At the end of period t_1, the current flowing in HEXFET 1 is equal to the load current I_o, and the current flowing in the rectifier of HEXFET 2 is instantaneously zero.

Note that during period t_1 (also during the subsequent period t_a) the voltage across HEXFET 1 theoretically is virtually the full source voltage. This is because so long as the rectifier of HEXFET 2 remains conducting, the voltage across it can be only its conduction voltage; the difference between this relatively small voltage and the total source voltage is developed across HEXFET 1.

This ignores the effect of stray circuit impedance. In practice, some of the source voltage will be dropped across the circuit impedance, and the voltage across HEXFET 1 will be less than the source voltage, by the voltage drop across the circuit impedance. A possible voltage across HEXFET 1 that takes account of the voltage drop across circuit and inductance is represented by the dashed wave in Figure 13a.

If the rectifier was "perfect," with no recovered charge, the commutation process would be complete at the end of period t_1. In practice, the rectifier current reverses during the recovery period, before the rectifier begins to support voltage. This happens during periods t_a and t_b (Figure 12c). During period t_a the reverse current i_2 increases until it reaches its peak value, $I_{RM(REC)}$. In the meantime, the current i_1 through HEXFET 1, is now the sum of the rectifier reverse current i_2 and the output current I_o, and its peak value, I_{MAX}, is the sum of I_o and $I_{RM(REC)}$. During period t_a, the voltage across HEXFET 1 still theoretically remains virtually equal to the source voltage, because the voltage across the rectifier of HEXFET 2 is still relatively low.

During the final period t_b, the rectifier of HEXFET 2 begins to support reverse voltage. The reverse rectifier recovery current i_2 decreases, and the voltage across HEXFET 1 falls to its final conduction level. Note the effect that circuit inductance has in producing an overvoltage transient across the rectifier, as illustrated by the dashed wave in Figure 13c.

Certain important points are evi-

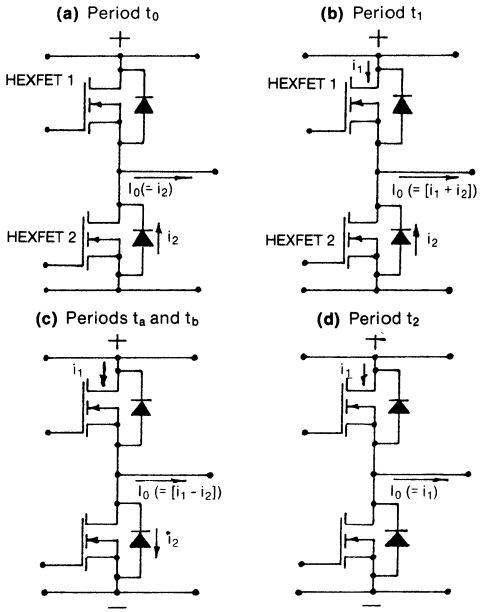


Figure 12. Commutation of Freewheeling Current I_o from the Rectifer of HEXFET 2 to the Transistor of HEXFET 1. HEXFET 1 and HEXFET 2 Form a Tandem Series Connected Pair Across a DC Source.

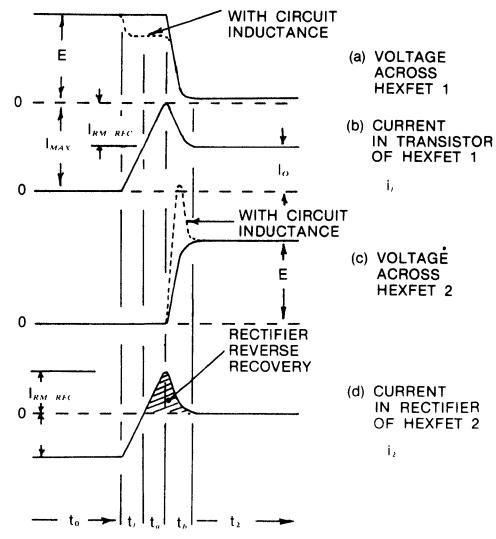
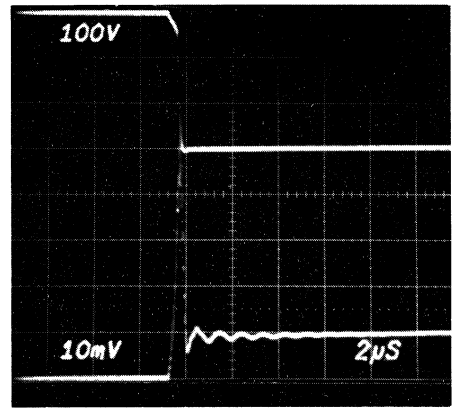


Figure 13. Theoretical Voltage & Current Waveforms for Commutating Sequence Depicted in Figure 12.

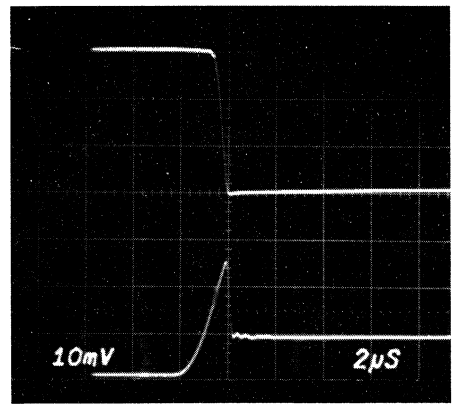
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dent. First, t_f, t_a, and, to a lesser extent, t_b, are high dissipation periods. Second, the peak current in HEXFET 1 is the sum of the load current and the rectifier reverse recovery current, and this peak current occurs at an instant when the voltage across the HEXFET is high. It is important that this peak current does not violate the HEXFET's I_{DM} rating. In fact, if the HEXFET is switched at a speed close to its limiting capability, and no other special precautions are taken, it may well do. A marginal situation for the IRF330 is illustrated by the voltage and current oscillograms in Figure 14a. Here, the IRF330 HEXFET is switched from a 300V source into a freewheeling current of about 4A (flowing in the integral rectifier of a second IRF330) at a rate of change of current of about 50A/μs. The peak current, I_{MAX}, in the HEXFET reaches a value that comes very close to the pulsed current rating. If the peak current was to substantially exceed the rating, diode failure could result, as explained in the last section. Fundamentally, the peak reverse recovery current of the rectifier can be reduced only by slowing down the rate of change of current during the commutation process. This is illustrated in Figure 15. Note that these waveforms assume a linear rate of change of current. The peak reverse current could also be reduced by slowing down the rate of change just in the reverse recovery region.

The rate of change of current can be controlled either by inserting inductance into the circuit, or by purposefully slowing down the rate of rise of the gate driving pulse. Theoretical switching waveforms obtained with



(a) I_{MAX} = 20A, di/dt = 50A/μs (t_1 + t_a) = 300 nanoseconds



(b) I_{MAX} = 20A, di/dt = 50A/μs (t_1 + t_a) = 300 1.8 μs

Figure 14. Oscillograms of IRF330 Switching into Reverse Rectifier of Another IRF330 with Freewheeling Current of 4A. Top Trace: Voltage 100V/div. Bottom Trace: Current 4A/div. Time Scale: 2 μs/div.

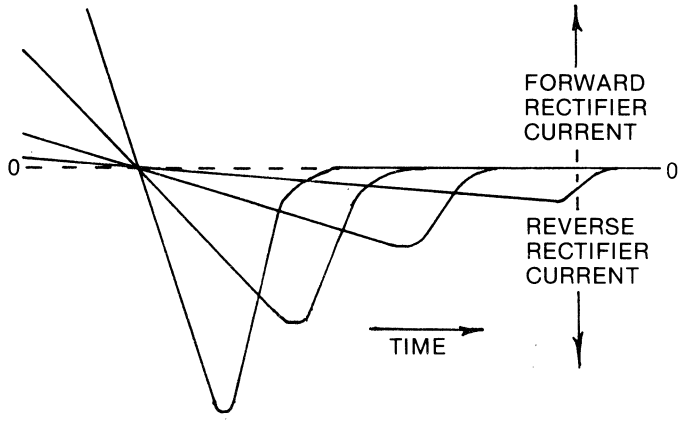


Figure 15. Reducing the Peak Rectifier Reverse Current by Reducing the Rate of Change of Current.

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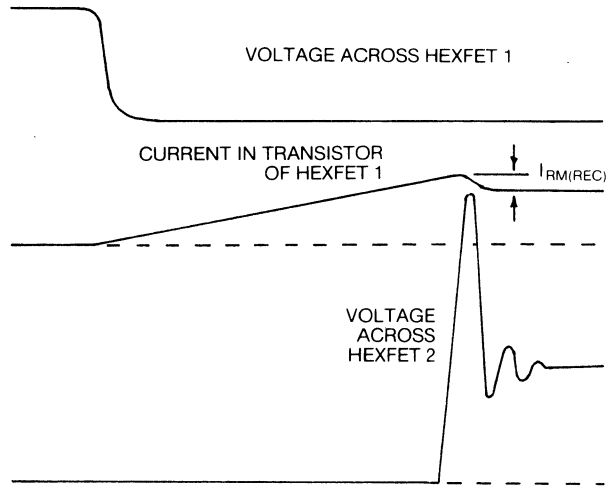
these alternative techniques are illustrated in Figure 16.

From the waveforms in Figure 16a, it is seen that an inductor in series with the HEXFET not only slows down the rate of change of current, it also supports the bulk of the source voltage, that would otherwise be developed across the HEXFET during the turn-ON interval. The energy in the HEXFET at switch-ON is therefore substantially reduced. There are, however, some disadvantageous side effects. First, the energy stored in the inductor inherently produces an overvoltage transient when the rectifier recovers, as shown. This voltage transient must be limited by an RC snubber or a voltage clamp, which dissipates the stored energy. Second, the inductance creates an overvoltage transient across the HEXFET when it is switched OFF (at a later point in the cycle, not shown in Figure 16). This overvoltage, again, must be clamped; unfortunately, the energy dissipated in the clamp at turn-OFF is significantly greater than the energy saved at turn-ON.

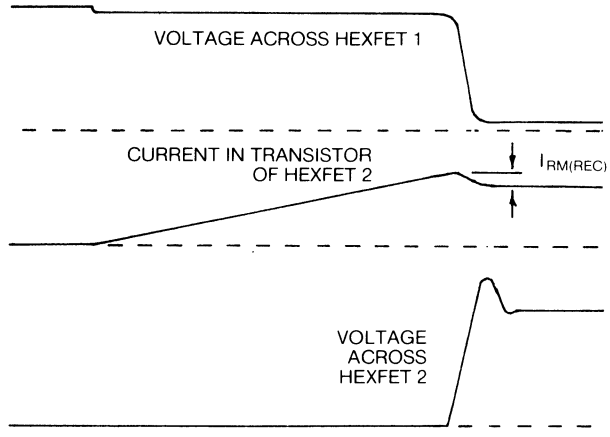
The other solution mentioned, which avoids the need for an additional power circuit inductor, is simply to slow down the switching-ON of the HEXFET by appropriately slowing down the rise of the applied gate drive signal. The effect on the circuit operation is illustrated in Figure 16b.

The peak current carried by the HEXFET can be reduced to almost any desired extent, at the expense of prolonging the high dissipation period, and hence increasing the energy dissipation at switch-ON. The practical oscillograms in Figure 14b illustrate this technique. By slowing the total switch-ON time ($t_i + t_a$) from 300ns to 1.8μs, the peak current, I_{MAX} has been decreased from 20A to 10A. The energy dissipation associated with the "unrestrained" switch-ON in Figure 14a is 0.9mJ, whereas it is 2.7mJ for the controlled switch-ON of Figure 14b.

Note that it is not necessary to slow the switching-OFF of the HEXFET, hence the energy dissipation at switch-OFF will be relatively small by comparison with that at switch-ON. For operation at frequencies up to a few kHz, where ultra fast switching is not mandatory, slowing of the applied gate drive signal to reduce the peak reverse recovery current of the rectifier (of the opposite device) will offer a good practical solution.



(a) Slowing the Rate of Change of Current by Inserting a Series Inductor



(b) Slowing the Rate of Change of Current by Slowing the Applied Drive Signal

Figure 16. Alternative Circuit Techniques for Controlling the Peak Reverse Recovery Current

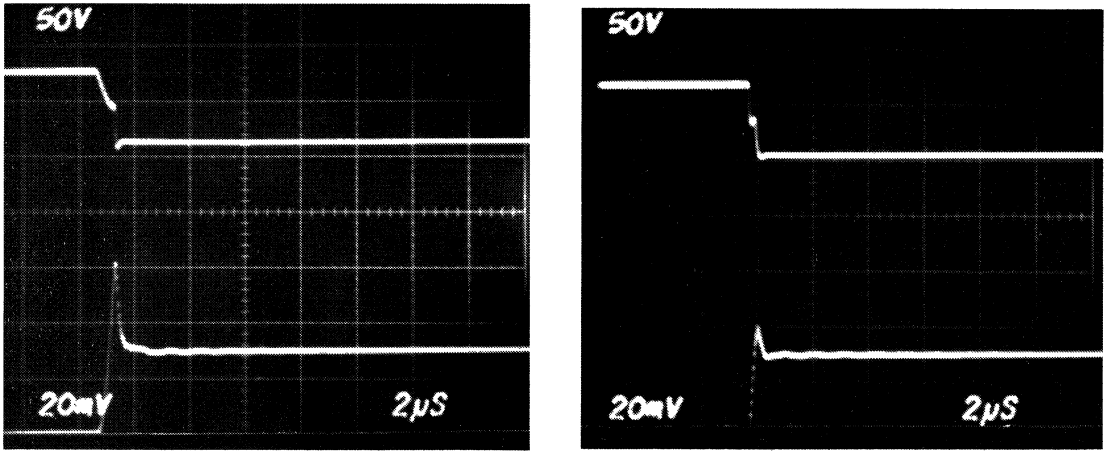
Use of External Fast Recovery Rectifier

As will be seen in the next section, for many applications where high switching frequency is required, the reverse recovery characteristic of the integral body diode is not a factor, even though this rectifier is used to carry inductive load current.

There will, however, be some high-frequency applications which require a reverse rectifier in which reverse recovery will be critically important, and in which the reverse recovery time of the integral reverse rectifier will not be fast enough.

In this event, the first approach is to connect an external fast recovery rectifier, or Schottky rectifier, across the HEXFET. So long as the conduction voltage drop of the external rectifier is appropriately lower than that of the integral rectifier, the external rectifier will carry the bulk of the "freewheeling" current, and the reverse recovery characteristic seen in the circuit will be that of the fast external rectifier. An example of the reduction in peak reverse recovery current obtained by connecting an external fast rectifier across the HEXFET is illustrated in

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(a) I_{MAX} = 25A, di/dt = 40A/μs
Switching Energy ≒ 500 μJ

(b) I_{MAX} = 12A, di/dt = 40A/μs
Switching Energy ≒ 120 μJ

Figure 17. Oscillograms of IRF130 Switching into a Current of 12A Freewheeling in (a) The Reverse Rectifier of Another IRF130 and (b) an External Fast Rectifier Connected Directly Across the Reverse Rectifier of an IRF130.

Figure 17. With an external rectifier across the IRF130, the peak current at switch-ON is reduced from 25A to 16A, and the switching energy in the HEXFET is reduced from 500 to 120μJ.

This solution will generally be applicable for low voltage HEXFETs, for which compatible low voltage drop fast recovery rectifiers or Schottky rectifiers are commercially available. For high voltage HEXFETs, however, fast recovery rectifiers are not yet generally available with sufficiently low conduction voltage. For these applications, it may be necessary to connect a rectifier or Schottky rectifier in series with the HEXFET, and a separate, high voltage, fast recovery rectifier across the combination. The series rectifier will block reverse current from flowing through the integral reverse rectifier of the HEXFET, thereby alleviating the recovery problem by shifting it to the faster external rectifier. (fig. 18)

Where Reverse Recovery *Is Not* Critical

All "full wave" voltage-fed inverter circuits use at least one of the tandem-switch circuit modules shown in Figure 12 (or an equivalent derivative thereof). A half bridge circuit, for example, uses one of these modules; a full single-phase bridge circuit uses two, and a three-phase bridge circuit uses three.

As has been seen, reverse recovery presents a difficulty when commutating current from a rectifier to a transistor. Whether or not this operating condition occurs depends upon the operating mode of the circuit. It does *not* occur in an inverter in which each

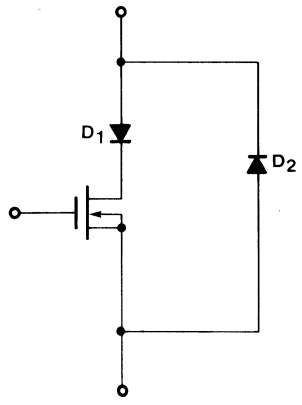


Figure 18. Cure for Reverse Conduction

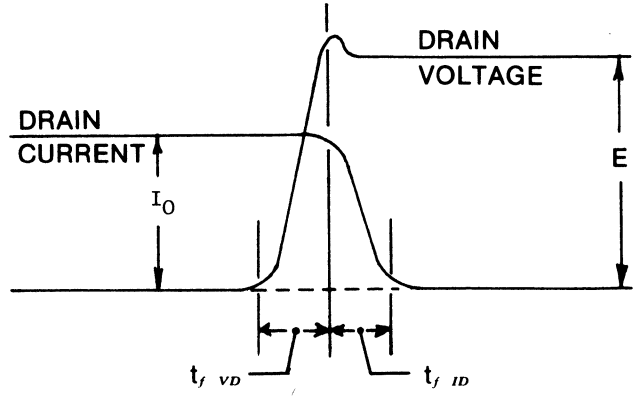
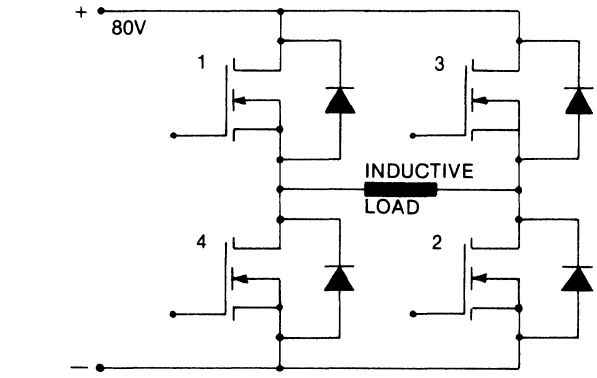
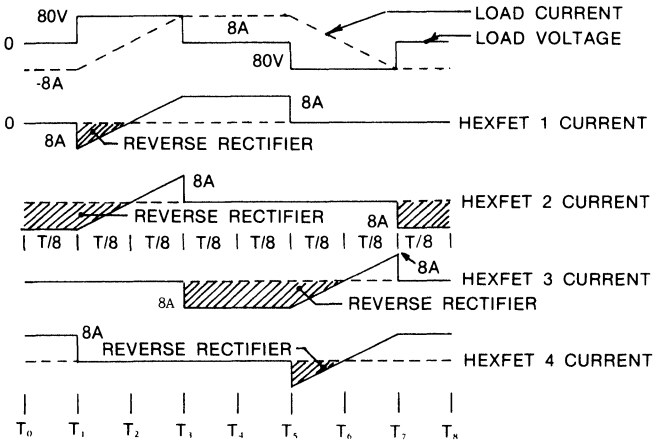


Figure 19. Voltage and Current Wave-forms When Switching Output Current I_o from Transistor to Opposite Rectifier

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(a) DC to AC Inverter With Inductive Load



(b) Theoretical Operating Waveforms

Figure 20. Inverter Circuit and Waveforms

output half cycle comprises a single voltage pulse, so long as the load is resistive or inductive. With a resistive load, the rectifiers do not come into play. With an inductive load, current is commutated from a transistor into an opposite rectifier; but never from a rectifier into an opposite transistor (it simply reverses naturally from the rectifier to the transistor of the *same* device, at an instant determined by the phase angle of the load, not by the inverter switching). Inspection of the waveforms in Figure 6c and Figure 20b will verify this rule. This is an important point, because it means that the reverse rectifier of the HEXFET is not frequency limiting conventional "single voltage pulse" switching inverter circuits (i.e., most common switching mode power supply circuits), even though these circuits can utilize the rectifier to carry inductive current.

Where Reverse Recovery *Is* Cricital

The situation is different with a capacitive load, for which the current leads the voltage. For a capacitive load, the current is instantaneously "negative" in a given switch at the moment of commutation, and current is now commutated from a rectifier to the opposite transistor. But this is of no great practical concern, since most practical loads are not capacitive.

The critical commutation situation will, however, be obtained in an inverter in which multiple output voltage pulses are produced during the course of each fundamental output cycle. The classical pulse width modulated inverter, commonly used for variable speed control of AC machines, stand-by power supplies, and so on, is an example. Inspection of the waveforms in Figure 6c will verify that the critical commutation condition (i.e., commutation of current from a rectifier to an opposite transistor) does indeed occur in this pulse width modulated (PWM) circuit.

Since operation under these conditions can sometimes lead to unexplained failures, if appropriate solutions are not adopted, it may be interesting to examine in more detail the equivalent circuit of a power MOSFET, taking into account its parasitic elements. As shown in Figure 21, the integral reverse diode is actually the base-collector junction of a bipolar transistor that has a base-emitter short.

If (for reasons that we shall examine later) this bipolar transistor goes into conduction at a time when the power MOSFET is supposed to block forward voltage (i.e. $V_{GS} = 0$) a potentially hazardous circuit operation would ensue that, depending on the specific power circuit, could lead to catastrophic failure. As we shall now briefly examine, there are three conceivable ways of causing unwanted conduction of the bipolar transistor shown in Figure 21.

The first is by avalanching the collector-base junction. If the voltage rating of the device is exceeded by a significant amount and if the supply has a suitably low internal impedance, the injection of minority carriers into the base region will cause, at some point, the bipolar transistor to go into conduction. This is knows as a "switchback" effect and is shown in Figure 22.

Some proprietary elements in the geometry and in the process of HEXFETs make them particularly well suited to absorb energy in avalanche without loss of blocking capability, as it appears from the waveforms for an unclamped inductive energy test shown in Figures 23 and 24.

The second possible way of getting the bipolar transistor into conduction is by applying a very steep voltage pulse on the drain. The collector-to-base capacitance (Figure 21) would couple such a pulse to the base of the transistor which could, conceivably, go into conduction. However, as shown in Ref. 1, for such a phenomenon to occur, the dv/dt of the voltage pulse would have to be well in excess of 75V/ns and HEXFETs are totally insensitive to practically achievable levels of dv/dt.

Finally, the bipolar could go in conduction if a relatively high dv/dt is applied to the device when the diode is recovering after forward conduction. As explained in Ref. 1, if the collector-base junction is forward biased the effective value of C1 (Figure 21) can

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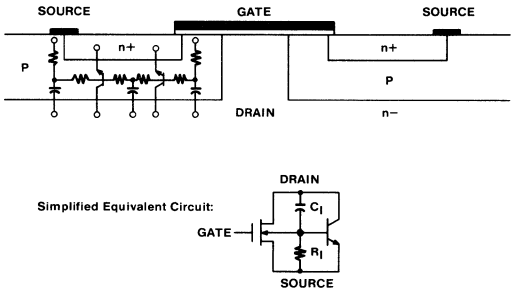


Figure 21. Parasitic Elements in the MOSFET Structure

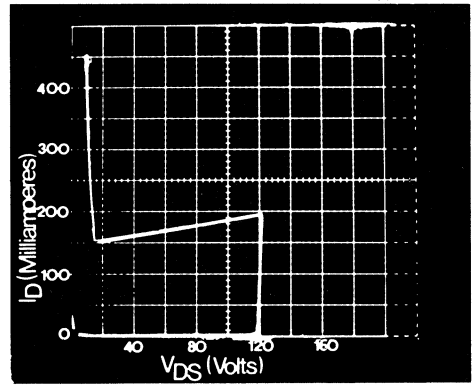
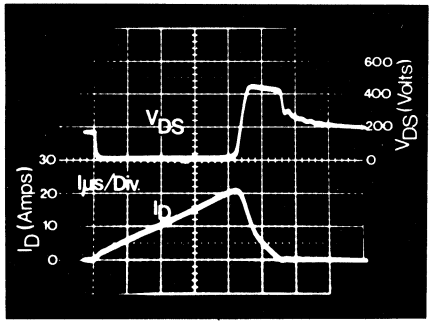


Figure 22. Undesirable switching during avalanche condition



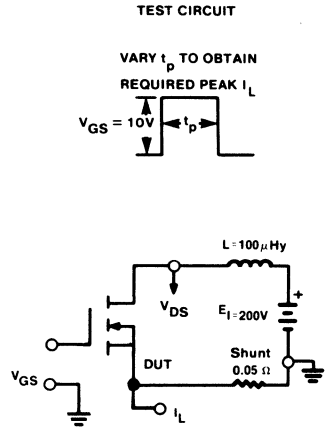
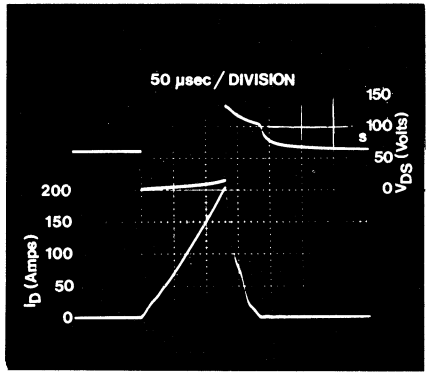


Figure 23. IRF330 Avalanche Energy Test



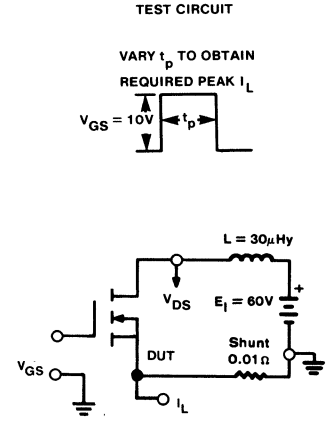


Figure 24. IRF150 Avalanche Energy Test

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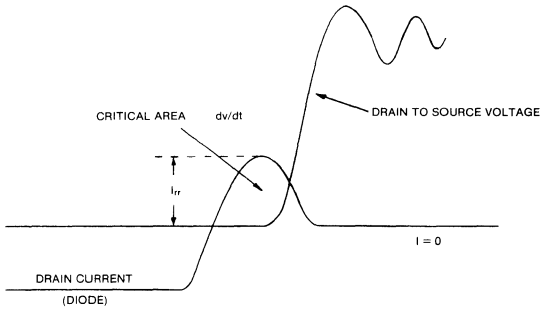


Figure 25. Current and Voltage Waveforms During Body Diode Recovery

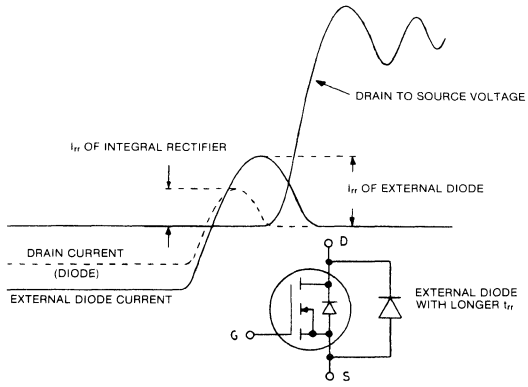


Figure 26. Effect of an External Diode With Longer t_{rr} on the dv/dt Applied to the Body Diode During Reverse Recovery

be many times greater. This, combined with the fact that minority carriers are already present in the base region, can cause spurious triggering at much lower values of dv/dt.

It should be emphasized, however, that this would only occur in those circuits in which multiple output voltage pulses are produced during the course of each fundamental output cycle, as shown in Figure 6c. On the other hand, in those circuits (like power supplies) that only generate a single voltage pulse for each half cycle of the output, as shown in Figure 6b, no dv/dt is applied to the diode during reverse recovery because at that time the diode itself is short circuited by its own conducting MOSFET and current transfers gradually from the diode into the same MOSFET of which the diode is a part. This would not necessarily be true, however, under abnormal operating conditions caused, for example, by logic malfunctions, misgatings due to noise or double pulsing of the control integrated circuit.

In those applications where a substantial dv/dt is likely to be applied during the reverse recovery, means should be provided to limit its value at that specific time (Figure 25).

In addition to the well known RC techniques employed to limit the dv/dt, a simple but often effective way of achieving the same result is shown in Figure 26. The connection of a diode with longer reverse recovery in parallel with the integral diode ensures that it will have recovered completely before any reverse voltage is applied to it.

Conclusions

The HEXFET's integral body diode, far from being a "parasitic" component, can be utilized in its own right, and indeed has a current rating equal to that of the transistor. This application note has shown where and how to use this diode, what cautions should be observed, and where it cannot be used.

Generally, the HEXFET's integral body diode will be applicable in the following areas:

(a) DC to AC inverters, which operate with one voltage pulse per output half cycle. In these circuits, the use of the integral body diode does not limit the switching frequency, so long as the load is inductive (as it normally is).
(b) Multi-pulse (PWM) DC to AC inverters, such as those used for variable frequency speed control of AC machines, and genearl purpose AC power supplies. Rectifier switching speed will usually restrict operating frequency to the 5-10 kHz range, but in many cases this will not be practically limiting.
(c) DC to DC choppers, such as are used in regenerative DC motor controllers. Again, rectifier switching speed will usually limit switching frequency to the 5-10kHz range.
(d) Bidirectional AC switching circuits.

The HEXFET's integral body diode has so far been largely overlooked. Circuit designers can now take serious note of it; it represents yet another potential application advantage of IR's HEXFETs. □

References

R. Severns: "dv/dt Effects in MOSFETs and Bipolar Junction Transistor Switches," PESC-81 Record, IEEE Power Electronics Specialists Conference, 1981

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CHAPTER 7
APPLICATION NOTE 940

An Introduction to International Rectifier P-Channel HEXFETs®

By S. CLEMENTE

With the introduction of International Rectifier's line of P-Channel power HEXFETs, a new option is available to the designer that can simplify circuitry while optimizing performance and parts count. This application note discusses the basic characteristics of P-Channel HEXFETs and gives a conceptual overview of typical circuit applications.

Basic Characteristics of P-Channel HEXFETs

Like their N-Channel counterparts, International Rectifier P-Channel HEXFETs are all presently enhancement mode devices; that is, application of voltage between the gate and the source terminals enhances the conductivity and allows current to flow, while no drain current flows when the gate is shorted to the source. For drain current to flow, the gate voltage has to be increased (in absolute value) towards the drain voltage. In a P-Channel device, the conventional flow of drain current is in the "negative" direction — that is, current flows out of the drain, with a negative gate-to-source voltage applied (Figure 1).

While the basic physical principles of operation for P- and N-Channel HEXFETs are similar, the different resistivity of the base silicon material has a distinct bearing on their specific characteristics, as well as upon cost. Since the resistivity of P-type silicon is much higher than that of N-type silicon, the P-Channel device requires a larger active area to achieve the same on-resistance and current rating.

This difference in resistivity of the basic silicon material is an obstacle to the construction of a P-Channel device that is truly electrically complementary in all respects to an N-Channel counterpart. Since for a given drain-source voltage capability, the on-resistance is the most basic parameter, the P-Channel HEXFET device will have the larger active area needed to achieve the same on-resistance as its complementary N-Channel counterpart. Gate threshold voltage, transconductance and self-capacitances are equalized as nearly as possible by accurate device design. Table 1 shows the parameters of two typical complementary P- and N-Channel HEXFETs (the IRF9130 and the IRF120) and shows to what extent their major parameters match one another. Voltage ratings, on-resistance, threshold voltage and, of course, package configuration, are exactly the same. Input capacitance and transconductance are also fairly closely matched. However, those parameters that are closely related to the die area, specifically thermal resistance, pulsed current rating, safe operating area and, to some extent, continuous current rating, are different, as would be expected. While these last parameters do not affect circuit operation directly, they have a bearing on circuit design and, whenever matched operation is required, the P-Channel device will operate with a larger safety margin with respect to its current ratings and thermal limits.

A close analysis of the data sheet would also show that the temperature variations of the threshold voltage, on-resistance and transconductance for a P- and an N-Channel are slightly different. This difference can, however, be considered a second order effect in most practical applications.

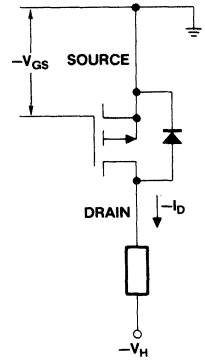


Figure 1. P-Channel power HEXFET

As shown in Figure 1, the P-Channel HEXFET, like its N-Channel counterpart, has an integral reverse rectifier, whose anode is connected to the drain. This diode is specified as a real circuit element with a current handling capability as high as that of the transistor itself. It is a very valuable circuit component in some applications.

Circuit Applications

In the following sections, we present a brief overview of the areas where a P-Channel can be used to particular advantage.

Grounded Loads

One area where P-Channel HEXFETs yield circuit simplification and

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cost savings is where the load is connected to ground. This is mandated in many automotive and aircraft applications and, sometimes, in household appliances. In these applications, in addition to wide safe operating area and excellent switching characteristics that are common to all HEXFETs, the use of a P-Channel device allows the load to be tied to the drain so that the gate drive can be referenced to one side of the supply. If an N-Channel were used, a separate supply would be required, referenced to the source, for the gate drive voltage.

Figure 2(a) shows how such a circuit would operate when driven from a C-MOS gate. However, if the load is operated at voltages above 15V, the logic ground cannot be connected to the load ground, and a separate supply is needed for the logic circuits,

Table 1.

	N-Channel	P-Channel
Device Type	IRF120	IRF9130
Drain-to-Source Voltage (Max.)	100V	-100V
Die Size	8.04mm²	13.25mm²
On-Resistance (Maximum)	0.3Ω	0.3Ω
On-State Drain Current @ T_C = 90°C	6A	-8A
Pulsed Drain Current	15A	-30A
Gate Threshold Voltage (Minimum-Maximum)	2 to 4V	-2 to -4V
Forward Transconductance (Typical)	2.5 S	3.5 S
Input Capacitance (Typical)	450pF	500pF
Output Capacitance (Typical)	200pF	300pF
Reverse Transfer Capacitance (Typical)	50pF	100pF
Maximum Thermal Resistance	3.12 deg. C/W	1.67 deg. C/W
Package	TO-3	TO-3

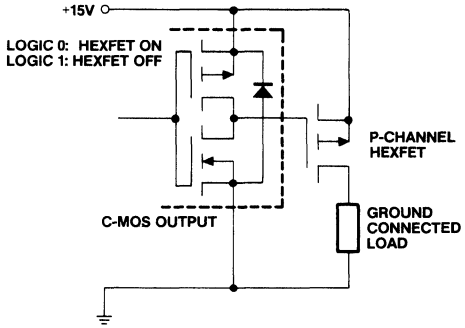


Figure 2(a). Switching Ground Connected Loads Operating from Low Voltages

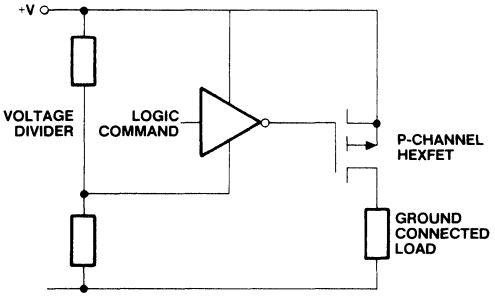


Figure 2(b). Switching Ground Connected Load at Higher Voltages

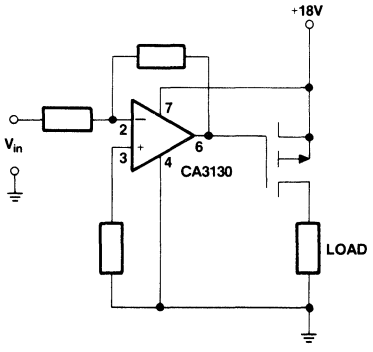


Figure 3(a). Driving Grounded Load in Linear Mode (Low Voltage)

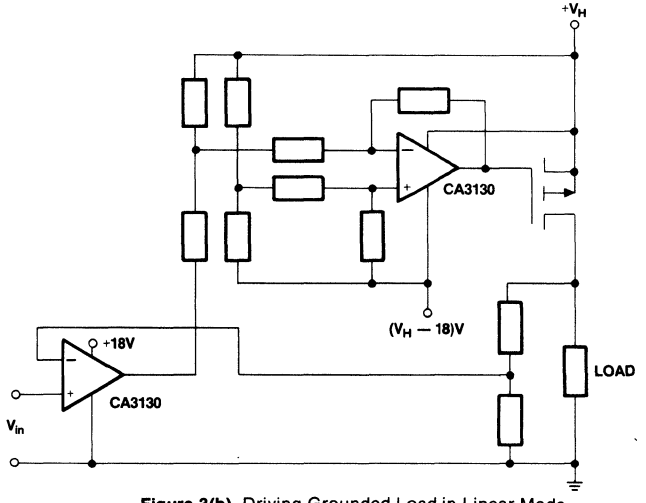


Figure 3(b). Driving Grounded Load in Linear Mode (High Voltage)

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as shown in Figure 2(b). An alternative approach is to drive the P-Channel HEXFET through a level shifter, as shown in Figure 5. Notice that to achieve the same result with an N-Channel HEXFET, a separate supply referenced to the source would be required.

A P-Channel device can also be operated in linear mode as shown in Figure 3. The device lends itself readily to voltage or current regulation which can be achieved through the use of suitable feedback. In the applications shown in Figures 3(a) and 3(b), the device drops whatever excess voltage is available from the unregulated supply. For parallel connection of devices, or where fast slew rate is important, a current boosting stage at the output of the operational amplifier may be required.

Totem Pole Switching Circuits

One of the most common building blocks for switching applications is the "totem pole." It is used in a variety of applications, such as switching power supplies, DC-to-AC converters, AC motor speed controllers, AM transmitters and Class D switching audio amplifiers.

Figure 4 shows one such circuit, implemented with two N-Channel HEXFETs, and its associated gate drive circuit. Since the drive circuits have to be referenced to the respective sources, they are isolated from each other. The most commonly used techniques to develop an "isolated" gate drive signal are optical isolators, transformer coupling and "bootstrapping." Optical isolators, shown in Figure 4, require a separate supply and are relatively slow and susceptible to noise. Pulse transformers, on the other hand, can only transfer to the secondary an AC signal (Figure 8), and hence have a limitation on the maximum and minimum possible switching duty cycle. They also always have some unwanted amount of leakage inductance. "Bootstrapping" is a technique for deriving a local gate drive voltage via a capacitor connected in the main drain circuit. Whereas it is satisfactory in many applications, it again has limitations regarding permissible duty cycle and maximum operating frequency.

The totem pole shown in Figure 5, using one N-Channel and one P-Channel HEXFET, is a step forward in the simplification of the drive circuit, since the gate drive signals are now referenced to separate ends of the DC supply. As shown, the drive signal referenced to the other rail can be developed by means of a simple level shifter. Furthermore, if the supply voltage is less than 20V, the two gates can be connected together and driven with respect to either end of the supply (Figure 6).

When using this type of totem pole, care should be exercised to have a gate drive signal with fast rise time. If the two gates are independent, as in Figure 5, another possibility is to have a deadband between the turn-on gate command of the P-Channel and that of the N-Channel equal to the rise time of the gate drive signal. Unless this is done, a short circuit current will flow through the two devices during the transition times,

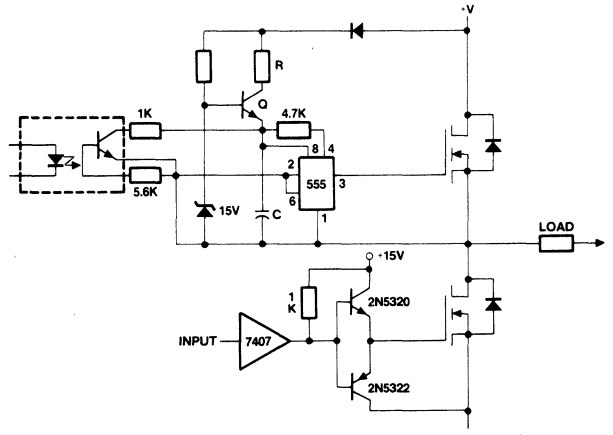


Figure 4. N-Channel Totem Pole and its Associated Drive Circuits

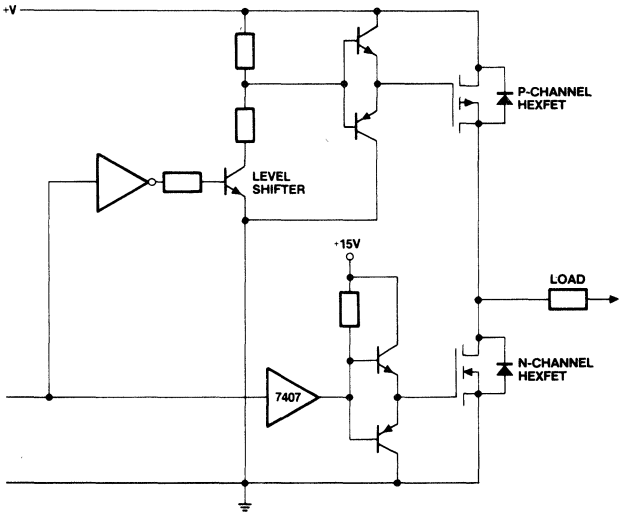


Figure 5. P/N-Channel Combination Totem Pole and its Associated Drive Circuits. Load is Connected to the Drains.

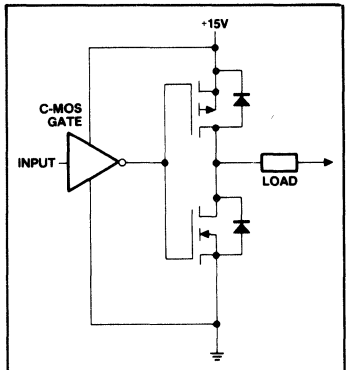


Figure 6. P/N-Channel HEXFET Totem Pole with Drive Circuit for Operation at Low Voltages

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as shown in Figure 7. However, the current regulating characteristic of power MOSFETs tends to limit the amount of this current and, while it may significantly increase the switching losses, it would not necessarily reach catastrophic values.

Should a common reference be desired for both gate drive signals, the circuit configuration shown in Figure 8 can be used. The positions of the P- and N-Channel HEXFET devices have been interchanged so that both have the load connected to the source. The gate drive signals are now referenced to the same point; however, this point is neither of the two supply leads. This is probably the circuit configuration that affords the simplest and most noise-immune gate drive circuit. An added advantage of this circuit is that it will not draw a short circuit current (Figure 7), because it is inherently impossible to drive both devices ON simultaneously.

Application of the Switching Totem Pole

The switching totem pole is used in a number of different applications. Some of the most common are the following:

- DC-to-AC inverters for battery operated supplies, stand-by and uninterruptible power systems.
- Variable frequency inverter for high efficiency speed control of AC induction motors.
- Regenerative speed control of DC motors.

Taking as an example this last application, we show in Figure 9 a way of implementing a DC motor speed control with regenerative braking capability with a complementary totem pole.

In the "motoring" mode of operation, HEXFET 1 is switched ON and OFF, at an appropriate repetition rate, and provides control of the average voltage applied to the motor. HEXFET 2 is OFF, but its integral reverse body-drain diode acts as the conventional freewheeling rectifier, and carries the freewheeling motor current during the periods when HEXFET 1 is OFF. When the motor is required to act as a generator and return energy to the DC source, HEXFET 2 is chopped ON and OFF, and controls the current fed back from the motor to the supply. In this operating mode, HEXFET 1 is OFF, but its integral reverse rectifier carries motor current back to the DC source during the intervals when HEXFET 2 is OFF. The circuit shown in Figure 10 could equally well be used and would offer the advantage of a common reference point for both gate drive signals, as mentioned previously. For this application, since only one device at a time is operated within any given control cycle, there is no danger of drawing a short circuit current.

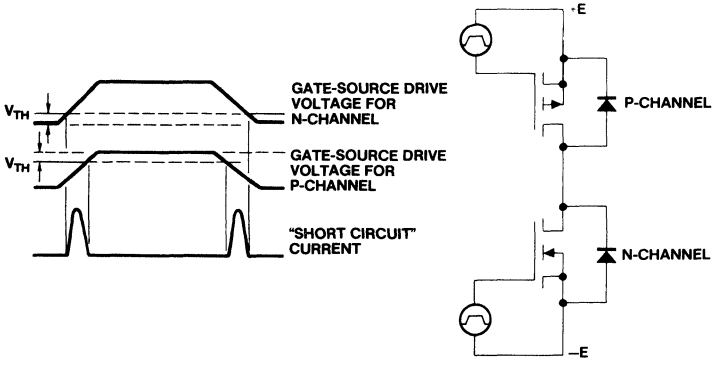


Figure 7. Short Circuit Current Caused by Overlapping Gate Signals

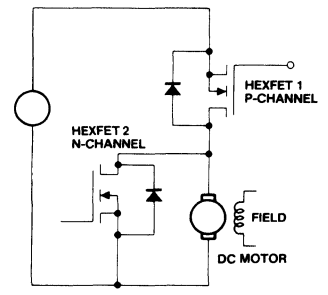


Figure 9. Regenerative DC Motor Controller

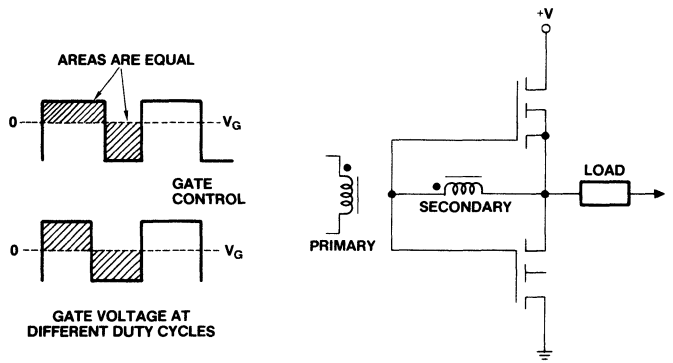


Figure 8. N/P-Channel Combination Totem Pole and its Associated Drive Circuits

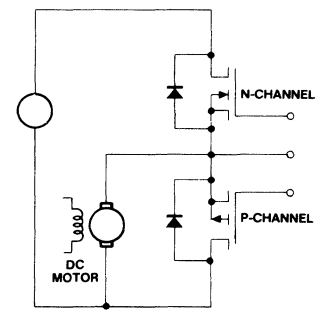


Figure 10. Alternative Configuration for the Regenerative DC Motor Controller

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Another consideration in choosing between the circuit connections of Figure 9 or Figure 10 is the current rating of the two devices. Normally, the device that is being switched during regeneration does not need to have a current rating as high as the motoring device, since friction and windage in the motor contribute to the braking torque. Therefore, the P-Channel HEXFET, because of its lower current rating for a given die size, may be a better choice for the regenerative operation.

Apart from being the basic building block of a large variety of inverter circuits, totem poles can be profitably used to drive large transistors or a parallel combination of them whenever high performance is required (Figure 11). This circuit can be used either in linear or switching applications and provides a good low impedance gate drive source. The integral reverse rectifiers clamp possible voltage transients on the gate.

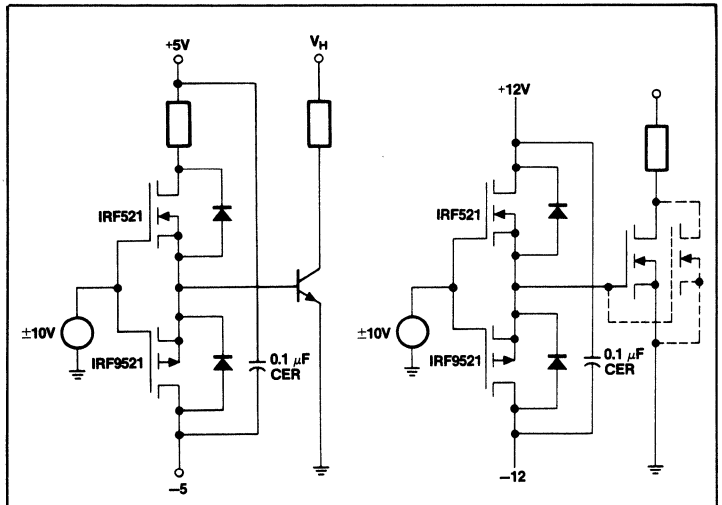


Figure 11. High Performance Drivers

Linear Application of Complementary Pairs

Because of the wide range of linearity of g_{fs}, immunity from secondary breakdown, high speed and intrinsic freedom from thermal runaway, power HEXFETs are ideally suited for operation as linear amplifiers, alone or in complementary pairs. When used in linear mode, the gate has to be biased to some level, depending on the type of operation desired. Several circuit configurations will achieve this end; they are inevitably simpler than would be required for bipolar transistors, since power MOSFETs require very little drive power and are not subject to thermal runaway.

Figure 12 shows the basic biasing scheme for linear operation, but much simpler versions can be developed for specific applications, as shown in Figure 13. The zener diodes should be chosen to give the desired bias current in relation to the available supply voltage. The gain bandwidth product that can be obtained with this stage driven by a simple differential amplifier is much larger than what can be obtained by a more complex bipolar configuration. The slew rate would also be much better.

Summary

P-Channel HEXFETs are electrical complements to International Rectifier N-Channel types. The availability of these devices offers new design options to the circuit engineer, and opens up the possibility for new HEXFET applications that were not before feasible with N-Channel types alone. □

Acknowledgements

The amplifier circuit shown in Figure 13 was developed by H. Schar of International Rectifier GmbH, Frankfurt, West Germany.

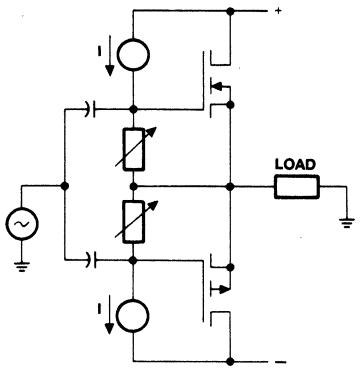


Figure 12. Basic Biasing Scheme for Linear Operation

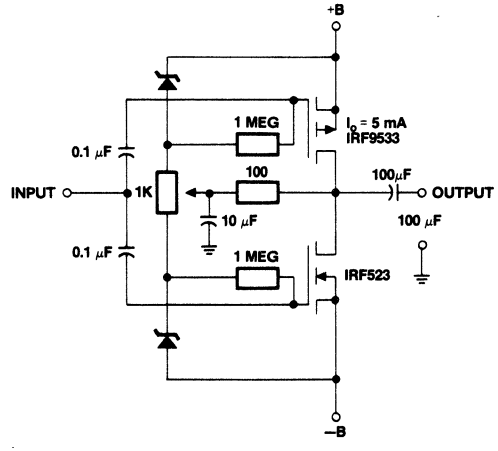


Figure 13. Simple Biasing Scheme for linear Operation

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Understanding HEXFET® Switching Performance

By S. Clemente, B.R. Pelly, A. Isidori

Abstract

A simple analytical technique for predicting the switching performance of the HEXFET is presented.

Closed-form solutions for the gate voltage, drain current, and drain voltage during the switching interval, in terms of each of the relevant device and circuit parameters, are derived.

A specific design example is considered, in which the effects are demonstrated of the drive circuit resistance, drain circuit inductance, and drive voltage, on the switching time and switching energy.

I. Introduction

The HEXFET is an almost ideal switch, which is characterized by very high gain and extremely fast switching characteristics. While users often ignore the intricacies of the switching operation, on the assumption that this is not critical to the overall design, the fact is that a clear understanding of the factors that affect switching can have a profound effect upon the system performance, particularly in high frequency circuits, and is, therefore, of vital interest to the user who needs to optimize his design.

Another reason why many users have a rather incomplete understanding of the HEXFET's switching operation is that the device is still relatively new, and HEXFET circuit design know-how has not yet matured. Users also tend to relate to their experience with bipolar transistors. The switching operation of bipolars is very difficult to analyze, and hence an empirical "try it and see" approach has generally held sway over more rigorous analytical techniques.

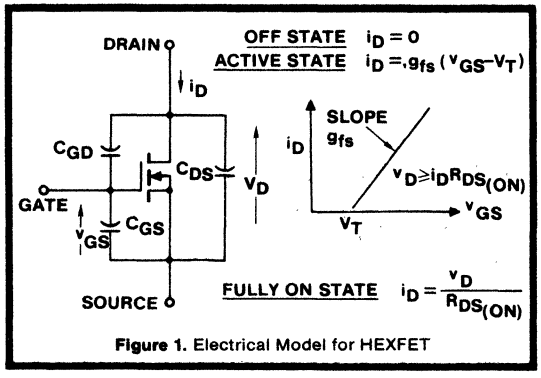


Figure 1. Electrical Model for HEXFET

One of the major "incidental" benefits of the HEXFET—in addition to its very real operating advantages—is that it lends itself rather well to analytical modeling; its operation can, therefore, be predicted rather easily at the design stage.

The primary objective of this application note is to show how, starting with a simple model of the HEXFET and using logical reasoning, the principles that govern the HEXFET's operation in a switching circuit can be readily predicted, and approximate mathematical relationships that describe these waveforms can be readily derived. Emphasis will be placed upon an understanding of basic principles.

II. The HEXFET Model

The electrical model for the HEXFET is shown in Figure 1. The self-capacitances are actually nonlinear functions of the applied voltage; also, to some extent, of the drain current. For purposes of analysis, however, these capacitances will be assumed to have fixed values; this does not detract from our basic objective, which is to understand fundamental principles.

This simple model of the HEXFET is assumed to have a linear transfer characteristic, with slope g_{fs} and gate threshold voltage V_T. The external drain current is assumed to be instantaneously responsive to the gate voltage, for operation in the active region.

Under transient switching conditions, charging and discharging currents flow through the various self-capacitive elements. The paths for components of these currents is through the drain-to-source terminals. The presence of these internal capacitive currents is assumed *not* to affect the transfer characteristic between the gate voltage and the external drain current.

The presence of C_{DS} will also generally be ignored for operations in the active region. This is valid because the effect of the gate-to-drain capacitance C_{GD}—providing, as it does, a coupling path from the drain circuit to the relatively sensitive gate circuit—generally "swamps" the effect of C_{DS}.

III. The Circuit Model

The clamped load is assumed to have sufficient inductance that the current flowing in it has a constant value I_O throughout the switching interval (Figure 2). The inductance L_ℓ represents "unclamped" stray circuit inductance.

The effect of the common source inductance L_S, shown dashed in Figure 2, will generally be neglected. This is not

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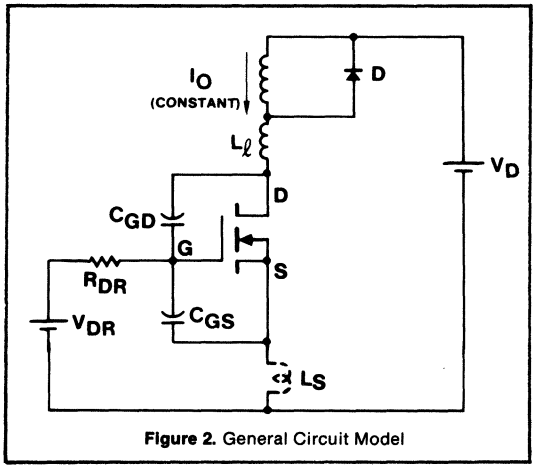


Figure 2. General Circuit Model

because it is necessarily negligible, but because to include it in a general analysis complicates the issue, making clarity of presentation and a grasp of fundamental principles more difficult. We prefer instead to consider the modifying effect of this inductance once the basic analysis is complete.

A number of switching circuits can be resolved into the equivalent circuit shown in Figure 2, or variants thereof, and in this sense the analysis is fairly general. The main point, however, is that the chosen circuit serves as a vehicle for obtaining an understanding of basic principles; once this has been accomplished the designer will be well equipped to deal with the switching operating of the HEXFET in any circuit.

IV. Nomenclature

v_D	Instantaneous drain-source voltage
v_{GS}	Instantaneous gate-source voltage
v_{GD}	Instantaneous gate-drain voltage
V_D	Steady applied drain circuit voltage
V_{DR}	Applied positive gate drive voltage (turn-on)
V_T	Gate threshold voltage
V_F	Positive gate drive "forcing" voltage (V_{DR} - V_T)
$-V_2$	Applied negative gate drive voltage (turn-off)
V_D*	Initial value of drain-source voltage at start of interval
V_{GS}*	Initial value of gate-source voltage at start of interval
V_{CLAMP}	Drain-source clamping voltage
i_D	Instantaneous current flowing into drain terminal
i_{GS}	Instantaneous current in C_{GS}
i_{GD}	Instantaneous current in C_{GD}
I_O	Steady current in clamped inductive load
I_D*	Initial value of current flowing into drain terminal at start of interval
R_{DR}	Gate drive circuit resistance
$R_{DS(ON)}$	On-state resistance of HEXFET
R_ℓ	Stray drain circuit resistance
L_ℓ	Stray drain circuit inductance
L_S	Inductance in series with source that is common to gate circuit
C_{GS}	Gate-source capacitance of HEXFET
C_{GD}	Gate-drain capacitance of HEXFET
C_{DS}	Drain-source capacitance of HEXFET
C_G	C_{GS} + C_{GD}
C_D	C_{DS} + C_{GD}
g_{fs}	Transconductance of HEXFET
p	Differential operator

V. Analysis of Switching Operation

Each switching sequence, either from the OFF to the ON condition, or vice versa, is subdivided into a number of separate intervals, for which different constraints and conditions apply. Each interval will be considered in sequence. The end-conditions for one interval become the starting conditions for the next. For simplicity we will take t = 0 at the start of each new interval.

The approach will be to consider each time interval in a qualitative manner, and through a process of reasoning based upon the known conditions and constraints, deduce as much as we can about the general shapes of the dynamic waveforms of drain voltage, drain current and gate voltage.

For certain time intervals this qualitative reasoning leads directly to the parametric analytic solution for that interval; for other time intervals, however, the analytic solutions are not so quickly obtained, except for parametric extremes at each end of the possible spectrum of external circuit conditions; a wide middle range of conditions remains for which derivation of the parametric solutions is rather too lengthy to be presented in its entirety, and in these cases we will simply state the final solutions.

A. TURN-ON

Turn-On Delay Interval 1

The circuit model for this interval is shown in Figure 3, and operating waveforms are shown in Figure 4. The applied drive

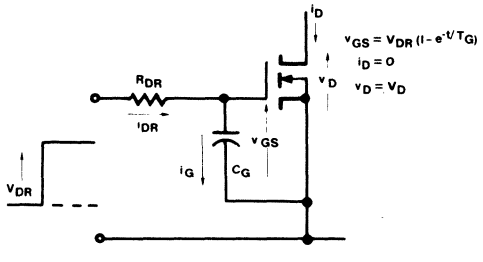


Figure 3. Circuit Model for Turn-On Delay Interval

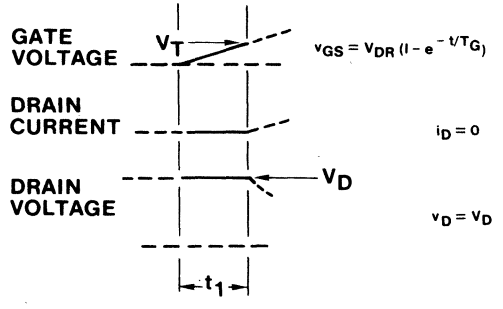


Figure 4. Waveforms for Turn-On Delay Interval (t_1)

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voltage is assumed to rise instantaneously to its full value; however, the voltage actually appearing between the gate and source terminals, which directly controls the external drain current, rises at a finite rate determined by the gate-to-source and drain-to-source self-capacitances. No drain current flows so long as the gate voltage is less than the threshold voltage, V_T. The end of the turn-on delay period is defined as the point at which the gate-to-source voltage becomes equal to the threshold voltage.

The analytic solution for the turn-on delay is almost trivial. Since no drain current flows, the drain voltage remains at V_D. Both the "drain" terminal of C_{GD} and the "source" terminal of C_{GS} sensibly do not change their potentials. The drive source voltage, V_{DR}, 'sees' the parallel combination of $C_{GD} + C_{GS} = C_G$, through the series resistor R_{DR}. The gate-to-source voltage v_{GS} follows a classical exponential:

$$v_{GS} = V_{DR}\left(1 - e^{-t/T_G}\right) \quad (1)$$

where

$$T_G = R_{DR}C_G \quad (2)$$

Turn-On Interval 2

The general circuit model for this interval is shown in Figure 5. The drain current now rises as the drain voltage falls. Which of these events is completed first depends upon the external circuit parameters. When one of these events is completed (or both simultaneously) the interval ends.

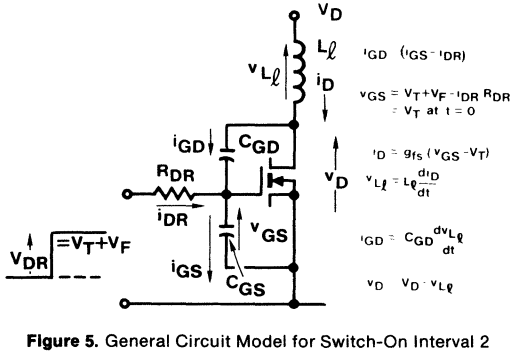


Figure 5. General Circuit Model for Switch-On Interval 2

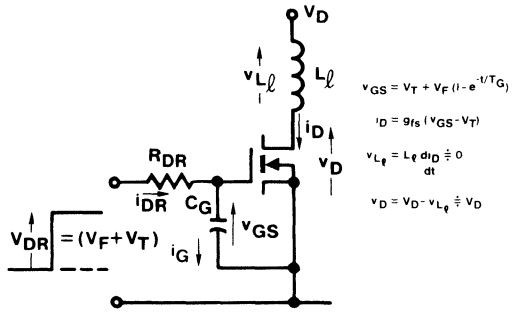


Figure 6. Circuit Model for Switch-On Interval 2
Small L_ℓ/R_{DR}

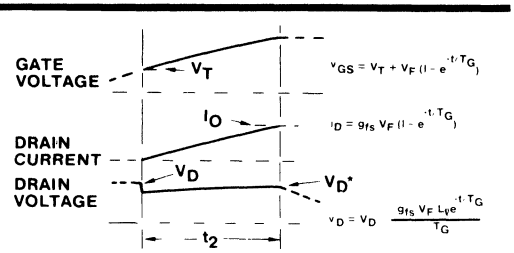


Figure 7. Waveforms for Turn-On Interval 2
Small L_ℓ/R_{DR}

$$\frac{L_\ell}{R_{DR}} < \frac{C_{GS}^2}{10C_{GD}g_{fs}}$$

Since the drain current i_D is less than the current I_O throughout this period, the difference between I_O and i_D must continue to circulate in the freewheeling rectifier D, forcing this diode to stay in conduction. This keeps the potential at the "top" of L_ℓ virtually constant at V_D.

As the gate-to-source voltage rises above the threshold level, the drain current starts to increase since drain current is proportional to gate voltage. The drain voltage also starts to fall because the increasing drain current induces a voltage across L_ℓ. As the drain voltage falls, current i_{GD} flows out of the "Miller" capactance C_{GD}; this current is drawn from the drive source, and deprives the gate-source capacitance C_{GS} of a portion of the charging current it would otherwise have received. This, in turn, reduces the rate of change of gate voltage, and hence also of drain current.

A dynamically "intertwined" situation obviously exists, by virtue of the "negative feedback" effect that couples the drain circuit to the gate circuit via the "Miller" capacitance C_{GD}. The "strength" of this feedback depends upon the ratio of the external circuit parameters L_ℓ to R_{DR}, as we will now see.

Large L_ℓ means large impedance to the rate of change of drain current, while small R_{DR} means fast gate circuit response, and hence potentially fast rate of change of drain current. With a high ratio of L_ℓ to R_{DR} the reactance of the drain circuit will therefore be high, the voltage drop across L_ℓ will be high, the "Miller" effect will predominate, and the rate of change of drain current will be unable to match the applied gate circuit stimulus. High L_ℓ/R_{DR}, therefore, means that the switching speed is severely limited by the constraints of the drain circuit; the drive circuit is "too fast" for the drain circuit.

Small L_ℓ/R_{DR} ratio means just the opposite; the potential rate of change of drain current is now much faster than the drive circuit actually allows. The voltage drop across L_ℓ is small, the "Miller" effect is small, and the gate circuit largely controls the switching time, virtually unimpeded by the drain circuit. Both of these extreme conditions are rather easy to analyze.

For intermediate L_ℓ/R_{DR}, the drain circuit and gate circuit responses can be envisioned as being reasonably "compatible" with one another. From a purist's viewpoint, compatibility of the gate and drain circuit responses might be considered to be the "correct" design point, because the gate circuit is neither too fast nor too slow for the drain circuit.

Small L_ℓ/R_{DR}

We will start the analysis by considering the situation when L_ℓ/R_{DR} is small. The circuit model is shown in Figure 6, and switching waveforms are shown in Figure 7. Since there is very little voltage developed across L_ℓ, the drain voltage v_D stays virtually at the circuit voltage, V_D, until the drain current has risen to its full load value I_O.

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Because the rate of change of drain voltage is small (almost zero), virtually no current flows through C_{GD}, and the drive circuit continues to see the simple parallel combination of C_{GD} and C_{GS} (as it did during the turn-on delay period). The gate-to-source voltage, v_{GS}, therefore, continues to rise exponentially:

$$v_{GS} = V_F \left(1 - e^{-t/T_G}\right) \quad (3)$$

The drain current rises in sympathy with the gate voltage:

$$i_D = g_{fs} V_F \left(1 - e^{-t/T_G}\right) \quad (4)$$

The drain voltage is equal to the circuit voltage V_D, less the small (almost negligible) voltage drop across L_ℓ:

$$v_D = V_D \frac{g_{fs} V_F L_\ell e^{-t/T_G}}{T_G} \quad (5)$$

The period ends when $i_D = I_O$.

It remains to quantify how small the ratio L_ℓ / R_{DR} must be for equations (3) through (5) to remain valid. The essential condition is that the rise of drain current must, for all practical purposes, be exclusively under the influence of the applied drive voltage. This means that whatever voltage change occurs across L_ℓ should not be noticed in the gate circuit. The current through C_{GD} will, therefore, be small by comparison with the current through C_{GS} (C_{GS} is typically about 10 x C_{GD}; however, a sufficiently large voltage change at the drain would produce a current through C_{GD} which is comparable to or larger than that through C_{GS}.

The essential condition therefore is that i_{GD} [$\doteq C_{GD}(dv_D/dt)$] should be small by comparison with i_{GS} [$\doteq C_{GS}(dv_{GS}/dT)$].

By differentiation of equations (3) and (5), this yields:

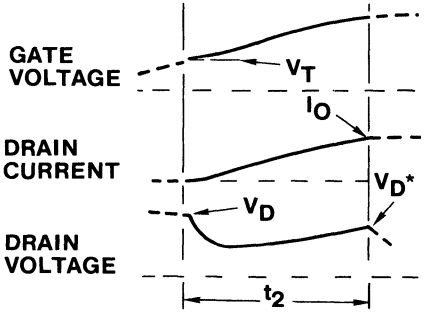
$$\frac{L_\ell}{R_{DR}} << \frac{C^2_{GS}}{g_{fs} C_{GD}} \quad (6)$$

Table 1 puts the above criterion into perspective, and shows typical value of L_ℓ and the corresponding "minimum" values of R_{DR}, for various HEXFETs. Clearly the values of R_{DR} needed to satisfy this condition are very high relative to most

Table 1: Limiting values of R_{DR} that define which equations (turn-on interval 2, and turn-off interval 3) are applicable, for various HEXFETs.

		Small L_ℓ / R_{DR}	Intermediate L_ℓ / R_{DR}		Large L_ℓ / R_{DR}
		$\frac{L_\ell}{R_{DR}} < \frac{C_{GS}^2}{10 C_{CG} g_{fs}}$	$\frac{L_\ell}{R_{DR}} < \frac{C_{GS}^2}{4 C_{GD} g_{fs}}$	$\frac{L_\ell}{R_{DR}} > \frac{C_{GS}^2}{4 C_{GD} g_{fs}}$	$\frac{L_\ell}{R_{DR}} > \frac{10 C_{GS}^2}{C_{GD} g_{fs}}$
Applicable Equations		3-5, 37-39	8-10, 40-42	14-16, 43-45	24-26, 46-48
1RF510 (100V, 2.5A)	L_ℓ 100 nH	R_{DR}-2.4kΩ min	R_{DR} -960Ω min	R_{DR}-960Ω max	R_{DR}-40Ω max
	L_ℓ 1 µH	R_{DR}-24kΩ min	R_{DR}-9.6kΩ min	R_{DR}-9.6kΩ max	R_{DR}-400Ω max
1RF130 (100V, 9A)	L_ℓ 100 nH	R_{DR}-1.3kΩ min	R_{DR}-520Ω min	R_{DR}-520Ω max	R_{DR}-20Ω max
	L_ℓ 1 µH	R_{DR}-13kΩ min	R_{DR}-5.2kΩ min	R_{DR}-5.2kΩ max	R_{DR}-200Ω max
1RF150 (100V, 25A)	L_ℓ 100 nH	R_{DR} -410Ω min	R_{DR}-165Ω min	R_{DR}-165Ω max	R_{DR}-6Ω max
	L_ℓ 1 µH	R_{DR}-4.1kΩ min	R_{DR}-1.65kΩ min	R_{DR}-1.65kΩ max	R_{DR}-60Ω max
1RF710 (400V, 1A)	L_ℓ 100 nH	R_{DR}-620Ω min	R_{DR}-325Ω min	R_{DR}-325Ω max	R_{DR}-13Ω max
	L_ℓ 1 µH	R_{DR}-6.2kΩ min	R_{DR}-3.25kΩ min	R_{DR}-3.25kΩ max	R_{DR}-130 max
1RF330 (400V, 3.5A)	L_ℓ 100 nH	R_{DR}-420Ω min	R_{DR}-170Ω min	R_{DR}-170Ω max	R_{DR}-7Ω max
	L_ℓ 1 µH	R_{DR}-4.2kΩ min	R_{DR}-1.7kΩ min	R_{DR}-1.7kΩ max	R_{DR}-70Ω max
1RF350 (400V, 9A)	L_ℓ 100 nH	R_{DR}-120Ω min	R_{DR}-50Ω min	R_{DR}-50Ω max	R_{DR}-2Ω max
	L_ℓ 1 µH	R_{DR}-1.2kΩ min	R_{DR}-500Ω min	R_{DR}-500Ω max	R_{DR}-20Ω max

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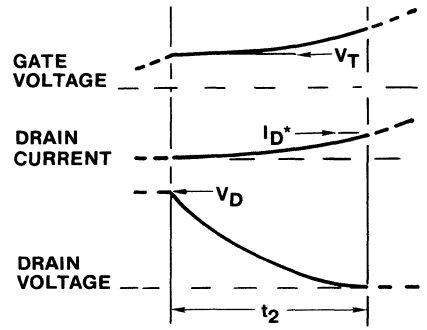
$$v_{GS} = V_T + V_F - \frac{V_F}{(T_1 - T_2)}\left\{T_1 e^{-t/T_1} - T_2 e^{-t/T_2}\right\}$$

$$i_D = g_{fs} V_F \left\{1 - \frac{1}{(T_1 - T_2)}\left(T_1 e^{-t/T_1} - T_2 e^{-t/T_2}\right)\right\}$$

$$v_D = V_D - \frac{g_{fs} V_F L_\ell}{(T_1 - T_2)}\left\{e^{-t/T_2} - e^{-t/T_1}\right\}$$

Figure 8(a). Waveforms for Turn-On Interval 2, Intermediate L_ℓ/R_{DR}

$$\frac{C_{GS}^2}{10 C_{GD} g_{fs}} < \frac{L_\ell}{R_{DR}} < \frac{C_{GS}^2}{4 C_{GD} g_{fs}}$$



$$v_{GS} = V_T + V_F - V_F e^{-t/T_3}\left\{\cos \omega_3 t + \frac{1}{\omega_3 T_3} \sin \omega_3 t\right\}$$

$$i_D = g_{fs} V_F - g_{fs} V_F e^{-t/T_3}\left\{\cos \omega_3 t + \frac{1}{\omega_3 T_3} \sin \omega_3 t\right\}$$

$$v_D = V_D - g_{fs} V_F \omega_3 L_\ell e^{-t/T_3}\left\{1 + \frac{1}{\omega_3^2 T_3^2}\right\} \sin \omega_3 t$$

Figure 8(b). Waveforms for Turn-On Interval 2, Intermediate L_ℓ/R_{DR}

$$\frac{C_{GS}^2}{4 C_{GD} g_{fs}} < \frac{L_\ell}{R_{DR}} < 10\,\frac{C_{GS}^2}{C_{GD} g_{fs}}$$

normal application requirements. This condition will not, therefore, be frequently met in practice; its consideration here is useful, however, because it helps to introduce the overall problem.

Intermediate L_ℓ/R_{DR}

We will now consider the situation when the ratio of L_ℓ/R_{DR} is not small, but has some intermediate value; the voltage drop across L_ℓ due to the increasing drain current becomes significant, and the current through C_{GD} cannot be neglected. The general circuit model of Figure 5 applies, and typical switching waves are illustrated in Figure 8(a) and (b).

The mathematical analysis is a little too lengthy to keep touch with physical realities. We will, therefore, confine ourselves to a simple statement of the results.

There are two possible sets of solutions, depending upon whether or not the system is critically damped. If overdamped, then:

$$\frac{L_\ell}{R_{DR}} < \frac{C_{GS}^2}{4 C_{GD} g_{fs}} \qquad (7)$$

Note the similarity of condition (7) to (6). Table 1 also shows typical values of L_ℓ and corresponding minimum values of R_{DR} that satisfy equation (7). This condition is certainly more likely to be encountered than condition (6), though once again it is generally not representative of most typical practical situations.

The gate voltage, v_{GS}, the drain current, i_D, and the drain voltage v_D, are:

$$v_{GS} = V_T + V_F - \frac{V_F}{(T_1 - T_2)}\left\{T_1 e^{-t/T_1} - T_2 e^{-t/T_2}\right\} \qquad (8)$$

$$i_D = g_{fs} V_F \left\{1 - \frac{1}{(T_1 - T_2)}\right\}\left\{T_1 e^{-t/T_1} - T_2 e^{-t/T_2}\right\} \qquad (9)$$

$$v_D = V_D - \frac{g_{fs} V_F L_\ell}{(T_1 - T_2)}\left\{e^{-t/T_2} - e^{-t/T_1}\right\} \qquad (10)$$

where

$$T_1 = \frac{2 L_\ell C_{GD} R_{DR} g_{fs}}{R_{DR} C_{GS} + \sqrt{R_{DR}^2 C_{GS}^2 - 4 L_\ell C_{GD} R_{DR} g_{fs}}} \qquad (11)$$

$$T_2 = \frac{2 L C_{GD} R_{DR} g_{fs}}{R_{DR} C_{GS} - \sqrt{R_{DR}^2 C_{GS}^2 - 4 L_\ell C_{GD} R_{DR} g_{fs}}} \qquad (12)$$

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The end of the time interval will generally be marked by the drain voltage having fallen all the way to $i_D \times R_{DS(ON)}$, with the drain current not having completed its rise.

For an "underdamped" system, the converse of (7) applies:

$$\frac{L_\ell}{R_{DR}} > \frac{C_{GS}^2}{4C_{GD}g_{fs}} \tag{13}$$

The minimum values of R_{DR} shown in Table 1 that satisfy equation (7) now become the maximum values that satisfy equation (13). Generally, most practical situations will be covered by equation (13).

The gate voltage v_{GS}, the drain current i_D, and the drain voltage v_D, are:

$$v_{GS} = (V_T + V_F) - V_F e^{-t/T_3}\left\{\cos \omega_3 t + \frac{\sin \omega_3 t}{\omega_3 T_3}\right\} \tag{14}$$

$$i_D = g_{fs}V_F - g_{fs}V_F e^{-t/T_3}\left\{\cos \omega_3 t + \frac{\sin \omega_3 t}{\omega_3 T_3}\right\} \tag{15}$$

$$v_D = V_D - g_{fs}V_F \omega_3 L_\ell e^{-t/T_3}\left\{1 + \frac{1}{\omega_3^2 T_3^2}\right\} \sin \omega_3 t \tag{16}$$

where

$$T_3 = \frac{2L_\ell C_{GD} g_{fs}}{C_{GS}} \tag{17}$$

$$\omega_3 = \frac{\sqrt{4L_\ell C_{GD} R_{DR} g_{fs} - R_{DR}^2 C_{GS}^2}}{2L_\ell C_{GD} R_{DR} g_{fs}} \tag{18}$$

The end of the time interval will be marked either by the drain circuit i_D reaching I_O, or the drain voltage v_D collapsing to $i_D \times R_{DS(ON)}$, whichever occurs first.

Large L_ℓ/R_{DR}

Now consider the situation when L_ℓ/R_{DR} has a large value—representing a "fast drive" circuit with a "slow" drain circuit. The equivalent circuit model is shown in Figure 9, and switching waves are illustrated in Figure 10. Note that we are ignoring the gate-to-source capacitance C_{GS}. This is valid because with large L_ℓ/R_{DR} ratio the "Miller" effect predominates and current through C_{GS} is small by comparison with that through C_{GD}.

The inductance L_ℓ now presents such a high impedance that the increase of drain current "requested" by the drive circuit cannot be satisfied; the drive circuit is largely impotent to bring about the drain current that it asks for.

The drain voltage now collapses relatively quickly—generally well before the current rise is completed. The end of the period is marked by the HEXFET reaching the essential condition of a "closed switch"—the voltage across it having collapsed completely.

The mathematics are rather simple; in order to gain insight, it is useful to proceed through the analysis step by step:

$$v_{GS} = (V_T + V_F) - i_{DR}R_{DR} \tag{19}$$

$$i_D = g_{fs}(v_{GS} - V_T)$$

Therefore, from (19):

$$i_D = g_{fs}(v_F - i_{DR}R_{DR}) \tag{20}$$

$$\therefore pL_\ell i_D = -pL_\ell g_{fs}R_{DR}i_{DR} \tag{21}$$

$$v_D = V_D - pL_\ell i_D$$

Therefore from (21):

$$v_D = V_D + pL_\ell g_{fs}R_{DR}i_{DR} \tag{22}$$

$$i_{DR} = -pC_{GD}v_D$$

Therefore from (22):

$$\therefore (p^2 L_\ell C_{GD} g_{fs} R_{DR} + 1)\, i_{DR} = 0 \tag{23}$$

Equation (23) is a classical second order differential, with purely "oscillatory" terms.

By imposing the appropriate boundary conditions [$v_{GS} = V_T$ at $t = 0$, and $pLi_D = 0$ at $t = 0$ (since $i_{GD} \neq \infty$)], the following solutions are obtained:

$$v_{GS} = V_F(1 - \cos \omega_1 t) \tag{24}$$

$$i_D = g_{fs}V_F(1 - \cos \omega_1 t) \tag{25}$$

$$v_D = V_D - \omega_1 L_\ell g_{fs} V_F \sin \omega_1 t \tag{26}$$

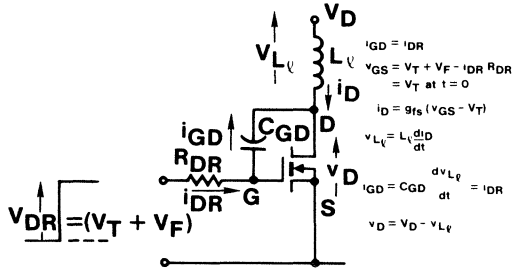


Figure 9. Circuit Model for Turn-On Interval 2, High L_ℓ/R_{DR}

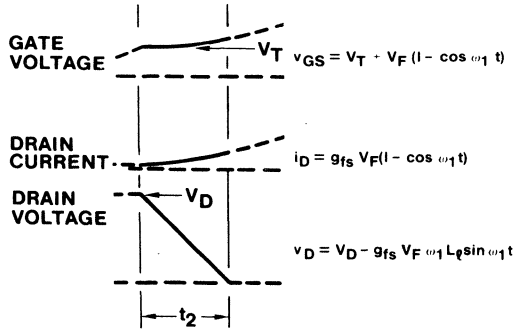


Figure 10. Waveforms for Turn-On Interval 2 Large L_ℓ/R_{DR}

$$\frac{L_\ell}{R_{DR}} > \frac{10C_{GS}^2}{C_{GD}g_{fs}}$$

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$$= V_D - \sqrt{\frac{g_{fs}L_\ell}{C_{GD}R_{DR}}} \sin \omega_1 t \qquad (27)$$

where

$$\omega_1 = \frac{1}{\sqrt{g_{fs}C_{GD}R_{DR}L_\ell}} \qquad (28)$$

It remains now to establish how large $L\ell/R_{DR}$ must be for the above simple relationships to be valid.

The starting assumption was that the current through C_{GS} is small by comparison with the "Miller" current i_{GD} through C_{GD}. This implies:

$$R_{DR} << \frac{1}{\omega_1 C_{GS}}$$

$$\therefore R_{DR} << \frac{\sqrt{g_{fs}C_{GD}R_{DR}L_\ell}}{C_{GS}}$$

$$\therefore \frac{L_\ell}{R_{DR}} >> \frac{C_{GS}^2}{C_{GD}g_{fs}} \qquad (29)$$

Table I shows maximum values of R_{DR} for various HEXFET's for different values of $L\ell$ that satisfy the above condition. It is clear that this condition, and hence expressions (24) through (26), will generally apply only to relatively low impedance drive circuits.

Simple qualitative checks on the above relationships will prove their validity. From equation (28), ω_1 increases as R_{DR} or $L\ell$ decreases. The rate of rise of drain current, therefore, increases as either of these parameters decrease, which is to be expected. From equation (27), the voltage across $L\ell$ is proportional to $L\ell/R_{DR}$. Thus increasing $L\ell$ or decreasing R_{DR} gives increasing voltage across $L\ell$—again, to be expected.

The end of the interval occurs when either the drain current i_D reaches I_O, or the drain voltage collapses to zero [more precisely when it becomes equal to $i_D \times R_{DS(ON)}$]. If I_O or V_F, or both, are small, i_D could reach I_O before the collapse of drain voltage is complete. In practice, the voltage collapse will generally occur well before the current has risen to I_O. To take an example, with the IRF150 HEXFET (rated 25A at 100° C) operating in a 60V circuit, with a gate forcing voltage V_F of 7V, $L\ell$ = 1 μH, and R_{DR} = 2Ω, the voltage collapse will be completed by the time the drain current has risen to 0.25A (i.e., about 1% of rated current).

This result is to be expected; we have already reasoned that for large $L\ell/R_{DR}$ ratio, the HEXFET essentially acts as a closed switch, the voltage across it collapsing quickly, with the current rising much more slowly, at a rate determined by the external circuit inductance.

Turn-On Interval 3

The second time interval ends at the completion either of the drain current rise or the drain voltage fall. The completion of the remaining event—voltage fall, or current rise—whichever it is, takes place during the third time interval.

Fortunately, since only the drain voltage *or* the drain current are now still changing, the analysis is easy, and is independent of the ratio of $L\ell/R_{DR}$. If the drain current is no longer changing, then $L\ell$ is irrelevant, since there is no voltage drop across it, whilst if the drain voltage is no longer changing, the HEXFET already acts as a closed switch, and R_{DR} is irrelevant.

Consider first the situation when the voltage completes its fall during the third interval. The equivalent circuit model is shown in Figure 11. At the start of the period the drain voltage is V_D*. Since the drain current is constant, v_{GS} must also be constant:

$$v_{GS} = V_T + \frac{I_0}{g_{fs}} \qquad (30)$$

Therefore i_{DR} is also constant:

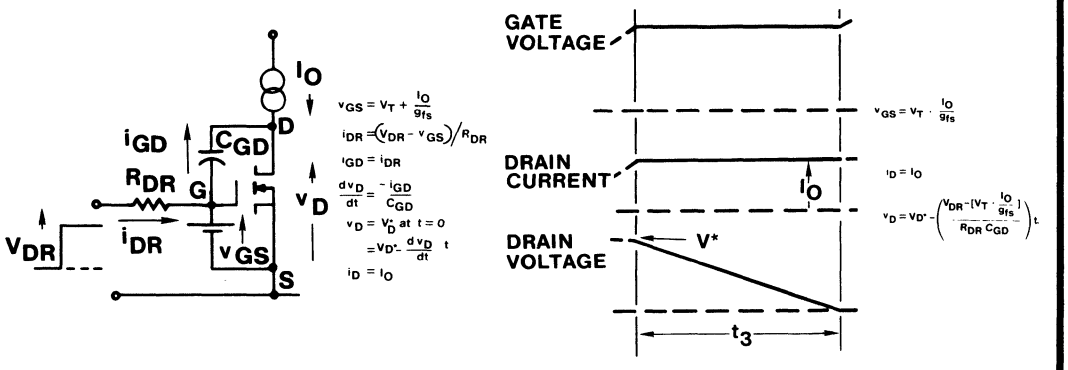
$$i_{DR} = \frac{1}{R_{DR}}(V_{DR} - V_{GS}) = \frac{V_{DR} - (V_T + I_0/g_{FS})}{R_{DR}} \qquad (31)$$

Since v_{GS}, is constant, no current flows in C_{GS}, and all of i_{DR} flows in C_{GD}. The rate of change of voltage across C_{GD} is therefore:

$$\frac{dv_{GD}}{dt} = \frac{i_{DR}}{C_{GD}} = \frac{V_{DR} - (V_T + I_0/g_{fs})}{R_{DR}C_{GD}} \qquad (32)$$

The rate of change of drain-source voltage is equal to the rate of change of drain-gate voltage, since v_{GS} is constant. Therefore, the drain voltage is:

$$v_D = V_D^* - \left(\frac{V_{DR} - (V_T + I_0/g_{fs})}{R_{DR}C_{GD}}\right) t \qquad (33)$$



Figures 11 and 12. Circuit Model and Waveforms for Turn-On Interval 3, i_D is Already Equal to I_O. v_D Collapses.

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We will now consider the situation when the current completes its rise during the third time interval, the drain voltage having already collapsed.

The equivalent circuit model is shown in Figure 13 and switching waveforms are shown in Figure 14. The drain current i_D is:

$$i_D = I_D^* + \frac{V_D}{L_\ell} t \qquad (34)$$

The gate voltage continues to increase exponentially during the third interval, at time constant T_G [equation (2)]. This, however, has no influence over the drain current or voltage, since the HEXFET is already "fully on."

Turn-On Interval 4

The gate voltage completes its exponential charge, at time constant T_G, to the level of the applied drive voltage V_{DR}. This has no influence over the drain current or voltage, since the switching sequence in the drain circuit has already been completed.

B. TURN-OFF

Turn-Off Delay Interval 1

The equivalent circuit model is shown in Figure 15, and operating waveforms are shown in Figure 16. The applied drive voltage V_{DR} is assumed to fall instantaneously to a negative

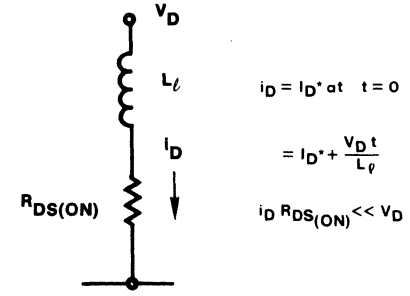


Figure 13. Circuit Model for Turn-On Interval 3, v_D Has Already Collapsed. i_D rises to I_O.

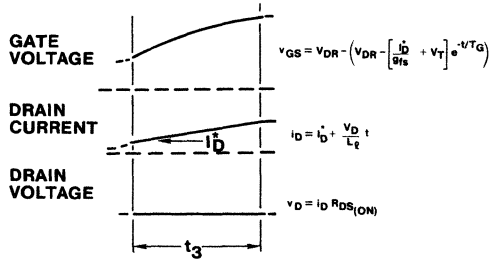


Figure 14. Waveforms for Turn-On Interval 3, v_D Has Already Collapsed. i_D rises to I_O.

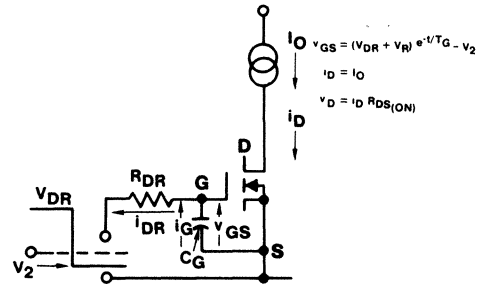


Figure 15. Circuit Model for Turn-Off Delay Interval

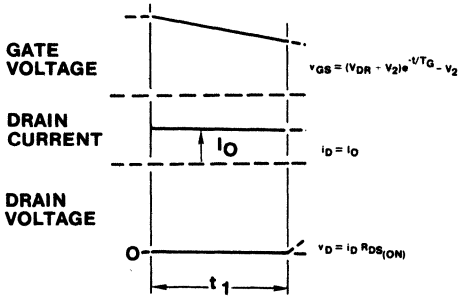


Figure 16. Waveforms for Turn-Off Delay Interval (t_1)

voltage $-V_2$ (this could, of course, be zero, or even positive, representing a small residual positive drive voltage). The voltage appearing between the gate and source terminals falls at a rate determined by the time constant $R_{DR}C_G$, and nothing happens in the drain circuit until the gate voltage falls to $V_T + (I_O/g_{fs})$, which corresponds to the gate voltage needed to sustain the drain current I_O. This point marks the end of the turn-off delay period. The gate voltage during the turn-off delay interval is given by:

$$v_{GS} = (V_{DR} + V_2)e^{-t/T_G} - V_2 \qquad (35)$$

Turn-Off Interval 2

The equivalent circuit model is shown in Figure 17, and typical switching waveforms are shown in Figure 18. The drain voltage rises to V_D whilst the drain current *remains constant* at I_O, and the gate voltage *remains constant* at $(V_T + I_O/g_{fs})$. At first sight this may be surprising; a moment's thought shows it has to be so. Until the drain voltage just exceeds the circuit voltage, V_D, the freewheeling rectifier D (Figure 2) remains reverse biased; the whole of I_O must, therefore, continue to flow into the drain of the HEXFET. So long as the drain current is constant, the gate voltage will also be constant (since these two parameters are inextricably tied to one another by the HEXFET's transfer characteristic), and the current flowing "out of" the resistor R_{DR} is drawn exclusively from the gate-to-drain capacitance.

Since the drain current is constant, the ratio of L_ℓ/R_{DR} has no bearing upon the operation during this period. By similar

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reasoning used to analyze the voltage fall during the third interval of switch-on, the following relationship is derived:

$$v_D = \frac{(I_0/g_{fs} + V_T + V_2)}{C_{GD}R_{DR}} t \qquad (36)$$

Turn-Off Interval 3

The general circuit model for this interval is shown in Figure 19. At the end of the second interval, the drain voltage is just equal to the supply voltage V_D, while the current is equal to the full load value, I_O. The freewheeling rectifier D (Figure 2) is now poised at the point of conduction, ready to receive the load current I_O, and the potential at the "top" of $L\ell$ is now fixed essentially at V_D. In order for the drain current to be commutated into the freewheeling rectifier, it is axiomatic that the drain voltage must increase above V_D. This reflects the fundamental property of inductance $L\ell$; the voltage across it must reverse in order for the current in it to reduce; a voltage-time integral must be developed, equal to I_O x $L\ell$, for the drain current to be returned to zero. This fundamental consideration relates directly to the inductance $L\ell$, and is quite independent of any other circuit considerations. The magnitude of the peak overvoltage developed across the HEXFET will be proportional to the size of the inductance $L\ell$, the magnitude of the current I_O, and the speed of switching.

In most practical circuits, the voltage transient at the drain can easily exceed the voltage rating of the HEXFET. In the absence of an externally connected local voltage clamp, the HEXFET will likely be driven into avalanche, acting, in effect,

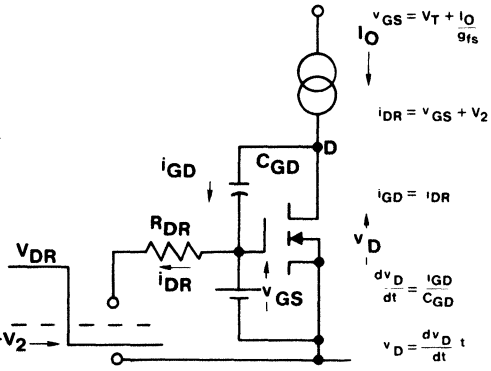


Figure 17. Circuit Model for Turn-Off Interval 2

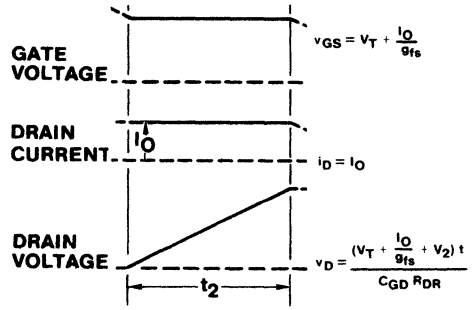


Figure 18. Waveforms for Turn-Off Interval 2

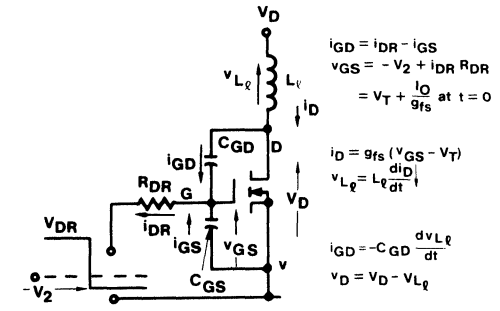


Figure 19. General Circuit Model for Turn-Off Interval 3

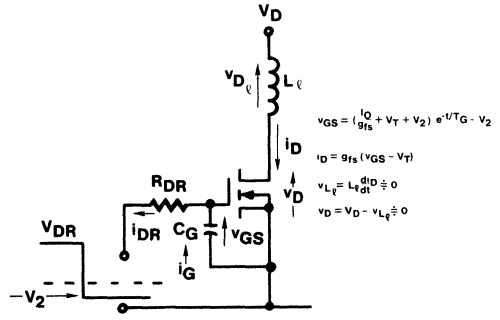


Figure 20. Circuit Model for Turn-Off Interval 3 Small $L\ell/R_{DR}$

as its own voltage clamp, and preventing further substantial increase of voltage. This may or may not be permissible, depending upon whether the HEXFET is rated to handle the avalanche energy. If it cannot do so, then a local external voltage clamp, such as a zener diode, connected physically close to the drain and source terminals will be needed, and this will be functionally equivalent to the HEXFET itself avalanching, save that the energy is absorbed by the clamp, rather than by the HEXFET.

In this third time interval of turn-off, as during the second time interval of turn-on, both the drain current and the drain voltage change. Again, these two events are dynamically intertwined. A change of drain current produces a change of voltage across $L\ell$; this produces a current flow through the "Miller" capacitance C_{GD}; this restrains the rate of decrease of gate voltage, which in turn restrains the original rate of change of drain current.

As we would expect, the form of the analytic solutions depends upon the ratio of $L\ell/R_{DR}$. We will simply state the results, since the derivation follows the same general procedures covered for the second turn-on interval.

Small $L\ell/R_{DR}$

The equivalent circuit model is shown in Figure 20, and operating waveforms are shown in Figure 21.

For small $L\ell/R_{DR}$, equation (6) must be satisfied:

$$v_{GS} = (I_0/g_{fs} + V_T + V_2) e^{-t/T_G} - V_2 \qquad (37)$$

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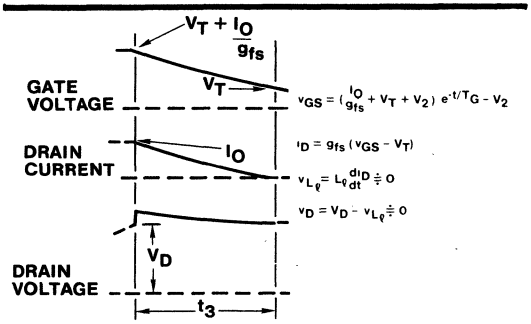


Figure 21. Waveforms for Turn-Off Interval 3 Small L_ℓ/R_{DR}

$$\frac{L_\ell}{R_{DR}} < \frac{C_{GS}^2}{10 C_{GD} g_{fs}}$$

$$i_D = (I_0 + g_{fs}\,[V_T + V_2])\, e^{-t/T_G} - g_{fs}[V_T + V_2] \qquad (38)$$

$$v_D = V_D + \frac{(I_0 + g_{fs}[V_T + V_2])\, e^{-t/T_G}}{T_G} \qquad (39)$$

The interval ends when the drain current i_D falls to zero.

Intermediate L_ℓ/R_{DR}

The general circuit model shown in Figure 19 applies. Either equation (7) or (13) must be satisfied. Operating waveforms for L_ℓ/R_{DR} that satisfy equation (7) are shown in Figure 22(a). Expressions for the gate voltage v_{GS}, the drain current i_D, and the drain voltage v_D are as follows:

$$v_{GS} = \frac{(I_0/g_{fs} + V_T + V_2)}{(T_1 - T_2)} \left\{ T_1 e^{-t/T_1} - T_2 e^{-t/T_2} \right\} - V_2 \qquad (40)$$

$$i_D = \frac{(I_0 + g_{fs}[V_T + V_2])}{(T_1 - T_2)} \left\{ T_1 e^{-t/t_1} - T_2 e^{-t/T_2} \right\} \ldots$$

$$\ldots - g_{fs}[V_T + V_2] \qquad (41)$$

$$v_D = V_D + \frac{(I_0 + g_{fs}[V_T + V_2])\, L_\ell}{(T_1 - T_2)} \left\{ e^{-t/T_2} - e^{-1/T_1} \right\} \qquad (42)$$

where T_1 and T_2 are given by equations (11) and (12), respectively.

Operating waveforms for L_ℓ/R_{DR} given by equation (13) are shown in Figure 22 (b). Expressions for the gate voltage v_{GS}, the drain current i_D, and the drain voltage v_D are as follows:

$$v_{GS} = (I_0/g_{fs} + V_T + V_2) e^{-t/T_3} \left\{ \cos \omega_3 t + \frac{\sin \omega_3 t}{\omega_3 t_3} \right\} - V_2 \qquad (43)$$

$$i_D = (I_0 + g_{fs}[V_T + V_2]) e^{-t/T_3} \left\{ \cos \omega_3 t + \frac{\sin \omega_3 t}{\omega_3 t_3} \right\} \ldots$$

$$\ldots - g_{fs}[V_T + V_2] \qquad (44)$$

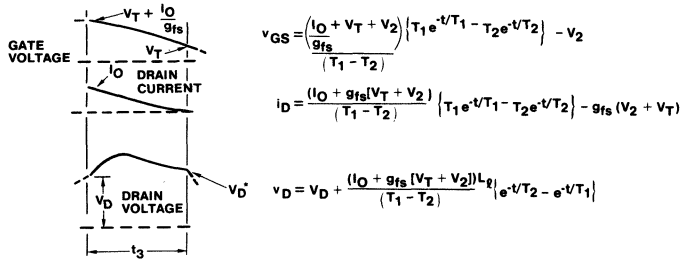


Figure 22(a). Waveforms for Turn-Off Interval 3 Intermediate L_ℓ/R_{DR}

$$\frac{C_{GS}^2}{10 C_{GD} g_{fs}} < \frac{L}{R_{DR}} < \frac{C_{GS}^2}{4 C_{GD} g_{fs}}$$

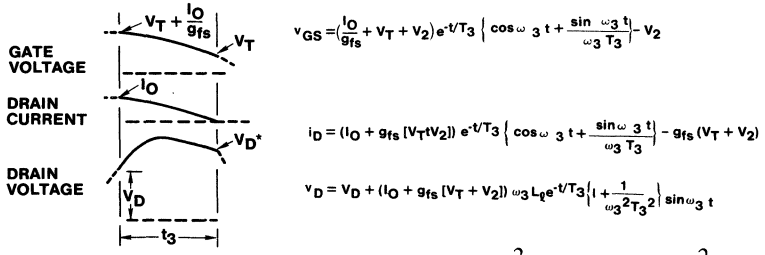


Figure 22(b). Waveforms for Turn-Off Interval 3 Intermediate L_ℓ/R_{DR}

$$\frac{C_{GS}^2}{4 C_{GD} g_{fs}} < \frac{L_\ell}{R_{DR}} < \frac{10 C_{GS}^2}{C_{GD} g_{fs}}$$

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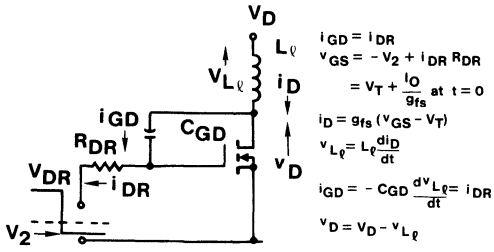


Figure 23. Circuit Model for Turn-Off Interval 3 Large L_ℓ/R_{DR}

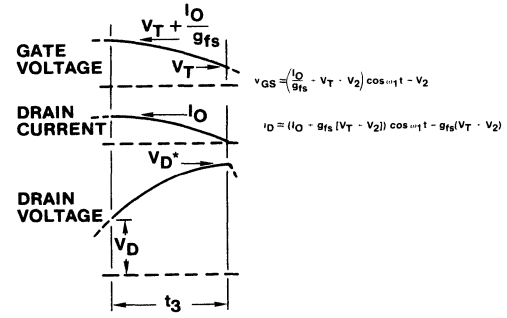


Figure 24. Waveforms for Turn-Off Internal 3 Large L_ℓ/R_{DR}

$$\frac{L_\ell}{R_{DR}} > \frac{10C_{GS}^2}{C_{GD}g_{fs}}$$

$$v_D = V_D + (I_0 + g_{fs}[V_T + V_2])\omega_3 L_\ell e^{-t/T_3} \ldots \left\{1 + \frac{1}{\omega_3^2 T_3^2}\right\} \sin \omega_3 t \qquad (45)$$

where T_3 and ω_3 are given by equations (17) and (18), respectively.

Large L_ℓ/R_{DR}

Large L_ℓ/R_{DR} is defined by equation (29). The circuit model is shown in Figure 23, and operating waveforms are shown in Figure 24. Expressions for the gate voltage v_{GS}, the drain current i_D, and the drain voltage v_D, are as follows:

$$v_{GS} = (I_0/g_{fs} + V_T + V_2)\cos \omega_1 t - V_2 \qquad (46)$$

$$i_D = (I_0 + g_{fs}[V_T + V_2])\cos \omega_1 t - g_{fs}(V_T + V_2) \qquad (47)$$

$$v_D = V_D + (I_0 + g_{fs}[V_T + V_2])\omega_1 L_\ell \sin \omega_1 t \qquad (48)$$

where ω_1 is given by equation (28).

Turn-Off Interval 3a (Clamping of the Drain Voltage)

The expressions just derived assume that the drain voltage will increase to whatever extent the circuit operation dictates. In practice, as already stated, the instantaneous drain voltage is likely to exceed the voltage rating of the HEXFET; this is particularly true for high L_ℓ/R_{DR} ratio.

In this event, either the HEXFET will be driven into avalanche—in effect acting as its own "voltage clamp" and limiting further increase of voltage—or, if the HEXFET is unable to handle this, an external local voltage clamping device would have to be connected.

In either event, at the instant at which the drain voltage becomes equal to the "clamp" voltage, interval 3, as given by the previous equations, comes to an end, and interval 3a—the clamping interval—starts.

Figure 25 shows the equivalent circuit for the "clamping" interval, with an external clamp, and operating waveforms are shown in Figure 26. The drain voltage is assumed to stay constant at the "clamp" level, V_{CLAMP}, while the drain circuit current decays linearly to zero:

$$i_D = I_D^* - \frac{(V_{CLAMP} - V_D)}{L_\ell} t \qquad (49)$$

The period ends when $i_D = 0$. Note that if the HEXFET acts as its own clamp and is driven into avalanche, then equation (49) applies to the HEXFET's drain current; if an external clamp is used, drain current can be assumed to stop flowing at the start of this interval, and equation (49) then applies to the current in the external clamp.

Turn-Off Interval 4

At the end of interval 3 (or 3a) the drain current has fallen to zero, but the drain voltage V_D^*, is greater than the circuit

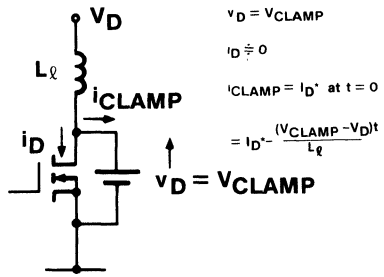


Figure 25. Circuit for Clamping Turn-Off Interval 3a

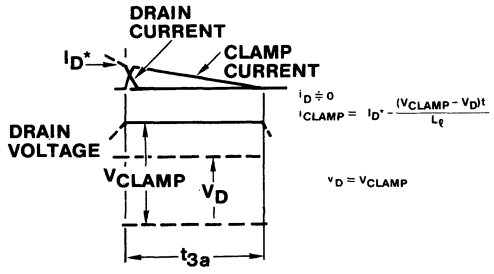


Figure 26. Waveforms for Clamping Turn-Off Interval 3a

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voltage V_D. The drain capacitance C_D then "rings" with the stray circuit inductance L_ℓ, the oscillation being damped by the stray circuit resistance R_ℓ. Figure 27 shows the equivalent circuit for this interval, and Figure 28 shows a typical drain voltage waveform.

$$v_D = V_D + (V_D^* - V_D)e^{-t/T_4} \cos \omega_4 t \quad (50)$$

where

$$T_4 = \frac{2L_\ell}{R_\ell} \quad (51)$$

$$\omega_4 = \frac{\sqrt{4L_\ell C_D - C_D^2 R_e^2}}{2L_\ell C_D} \quad \ell \quad (52)$$

During this interval the gate voltage discharges exponentially with time constant T_G towards a final value of $-V_2$.

VI. A Worked Design Example

Figures 29 through 32 show switching waveforms for a specific design example, obtained from the analytic expressions presented in this paper. Various combinations of $L\ell/R_{DR}$, and amplitude of drive voltage, are considered in order to illustrate the effects of these parameters on the switching performance. The following data is used:

HEXFET type: IRF150

C_{GS}: 2650 pF
C_{GD}: 350 pF
V_T: 3 V
g_{fs}: 8 A/V
V_D: 50 V
I_O: 35A

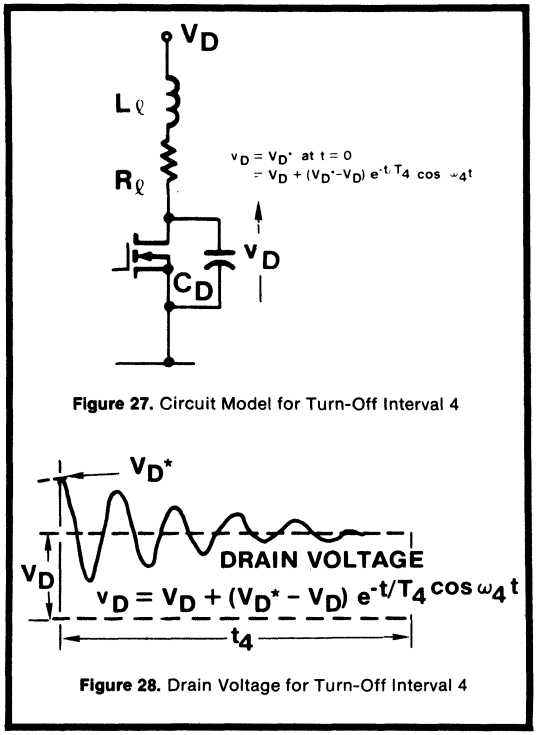


Figure 27. Circuit Model for Turn-Off Interval 4

Figure 28. Drain Voltage for Turn-Off Interval 4

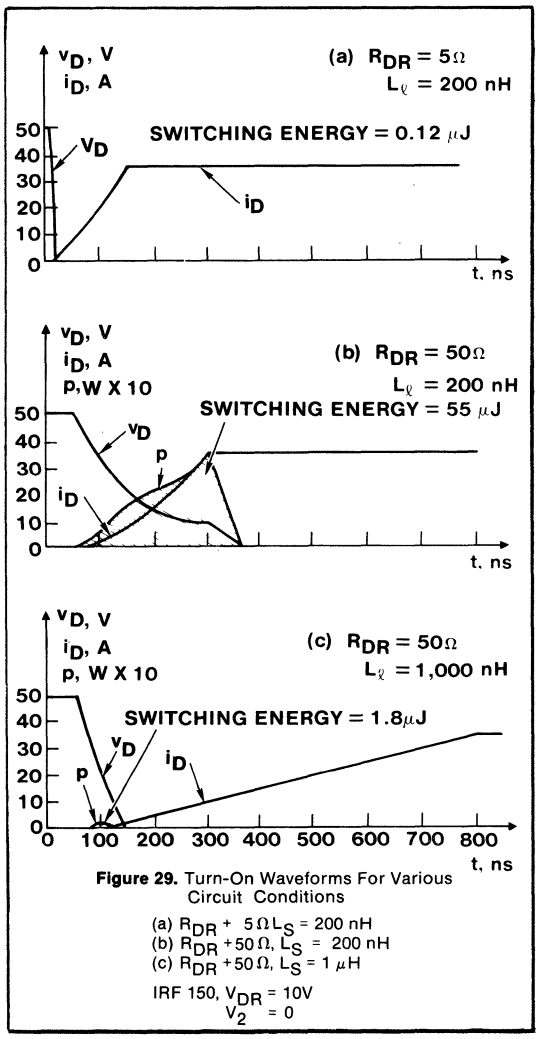


Figure 29. Turn-On Waveforms For Various Circuit Conditions

(a) R_{DR} + 5Ω L_S = 200 nH
(b) R_{DR} +50Ω, L_S = 200 nH
(c) R_{DR} +50Ω, L_S = 1 μH

IRF 150, V_{DR} = 10V
V_2 = 0

Figure 29 shows waveforms calculated for the turn-on interval for: (a) R_{DR} = 5 ohms, $L\ell$ = 200 nH; (b) R_{DR} = 50 ohms, $L\ell$ = 200 nH; and (c) R_{DR} = 50 ohms, $L\ell$ = 1 μH. The drive voltage V_{DR} is 10 volts.

Condition (a) is representative of a fast drive circuit, and a relatively high impedance of $L\ell$. The drain voltage falls rapidly, and most of the current rise time occurs subsequent to the collapse of drain voltage. The switching energy is almost negligible —a mere 0.12 μJ. In Figure 29(b), the inductance is the same, but the drive resistance has increased to 50 ohms. The gate drive circuit is now much slower, and the drain voltage collapses much less rapidly; in fact, the drain current now completes its rise before the drain voltage collapses completely. The total switching time (current rise + voltage fall) increases from 150 ns in Figure 29(a) to 360 ns in Figure 29(b). More significantly, the switching energy increases from 0.12 μJ to 55 μJ.

In Figure 29(c), the drive circuit resistance is still 50 ohms, while the drain inductance $L\ell$ has increased from 200 nH to 1 μH. The speed of the drive circuit is, therefore, the same as in Figure 29(b), but the impedance of $L\ell$ increases by a factor of 5. The voltage drop in the drain circuit is, therefore, once again very significant, and the drain voltage collapses much more

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rapidly. Because of the increased inductance, however, the current rise time is much longer. The switching energy decreases from 55 μJ in Figure 29(b) to 1.8 μJ in Figure 29(c), because of the much faster voltage collapse. It would be wrong to believe, however, that the overall switching losses can be decreased by increasing $L\ell$. The energy saved during turn-on by increasing $L\ell$ is more than offset by increased energy at turn-off. Increasing $L\ell$ to reduce the turn-on losses is counterproductive; it simply postpones the "day of reckoning" to the turn-off interval.

Before studying the details of the turn-off waveforms in Figure 30, it will be instructive to make some basic comparisons between the operation during the turn-on and turn-off intervals.

At turn-on the peak dissipation is drastically effected by the $L\ell/R_{DR}$ ratio, and is very small if this ratio is large. At turn-off, however, $L\ell/R_{DR}$ has no real influence on the peak dissipation, and this is *always* relatively high. This is because the drain current cannot start to decrease *until* the drain voltage has risen all the way to the circuit voltage. The peak dissipation during the voltage rise interval (turn-off interval 2) will, therefore, always be $V_D \times I_O$. While the value of drive resistance, R_{DR}, controls the duration of this period, $L\ell$, has no effect upon it.

The next turn-off interval (t_3), is also one of relatively high power dissipation. Even with no drain inductance, the drain current must decay from I_O to zero with the drain voltage at the full circuit value, V_D. In practice $L\ell$ will never be zero, and the energy stored in this inductance ($1/2\ L\ell I_O^2$) will also be dissipated during this period. It is evident, therefore, that while the turn-on energy depends strongly upon the $L\ell/R_{DR}$ ratio, and can be very small if $L\ell/R_{DR}$ is large, there is no way of avoiding a much more significant turn-off energy. Generally, the larger is $L\ell$, the greater will be the *total* energy dissipation, even though the turn-on dissipation may be very low.

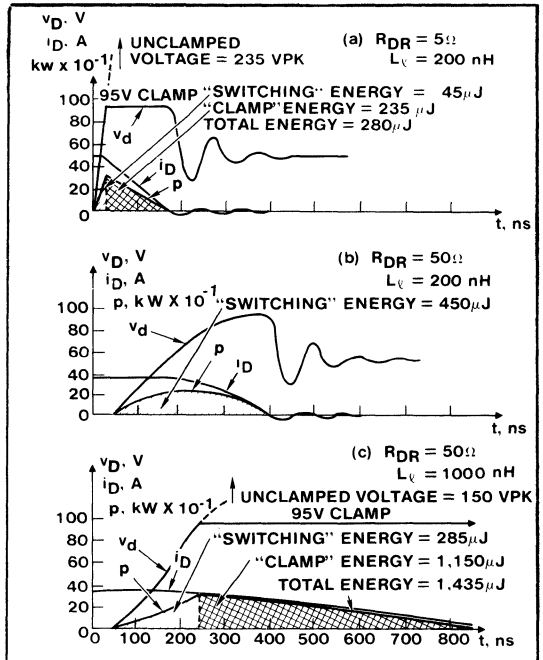


Figure 30. Turn-On Waveforms For Various Circuit Conditions

(a) R_{DR} = 5Ω, L_S = 200 nH
(b) R_{DR} = 50Ω, L_S = 200 nH
(c) R_{DR} = 50Ω, L_S = 1000 nH

IRF 150, V_{DR} = 10V
V_2 = 0

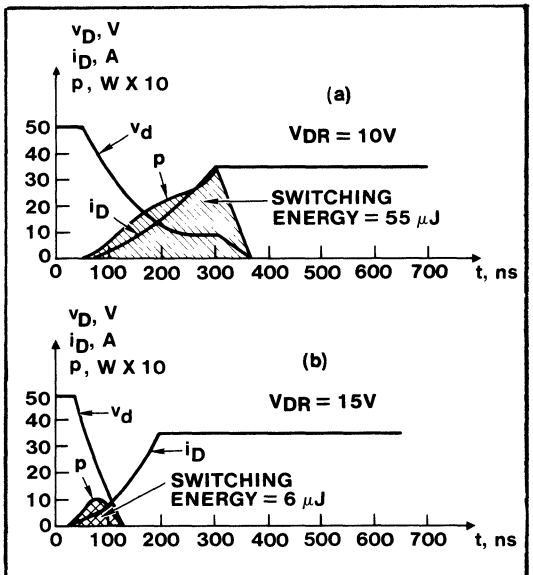


Figure 31. Turn-On Waveforms for:

(a) Drive Voltage V_{DR} = 10V
(b) Drive Voltage V_{DR} = 15V

IRF 150 R_{DR} = 50Ω
L_S = 200nH

Figures 30(a) through (c) show waveforms at turn-off that correspond to the same three sets of values of R_{DR} and $L\ell$ as in Figure 29(a) through (c). The waveforms in Figure 30 (a) are for a fast drive circuit (R_{DR} = 5 ohms). The drain voltage rises rapidly to the clamping level of 95V. Note that in the absence of a clamp the drain voltage would rise to a hypothetical peak of 235V (assuming that this 100V rated HEXFET would take it!). The energy dissipated in the HEXFET during the time the drain voltage rises to the 95V clamp level is referred to in Figure 31 as "switching" energy, and is 45 μJ—more than two orders of magnitude greater than the energy at turn-on for the same values of R_{DR} and $L\ell$ [Figure 29(a)].

Once the 95V clamp level is reached, the current decays approximately linearly, and an additional 235 μJ of energy is dissipated during the clamping period. This energy would be dissipated either in an external clamp, if this is used, or in the HEXFET itself—assuming that it is capable of operating in its avalanche mode.

Note that the energy stored in $L\ell$, $1/2\ L\ell I_O^2$ = 122 μJ, is about half the total energy dissipated during the clamping period. Simple physical reasoning confirms the correctness of this; not only must the energy stored in $L\ell$ be dissipated, but since the supply voltage V_D continues to feed energy to the circuit (i_D continues to be drawn from V_D), this energy also must end up being dissipated during this period.

Figure 30(b) shows waveforms for R_{DR} = 50 ohms, with $L\ell$ the same as for Figure 30(a). The response of the gate drive circuit is much slower, and hence the rate of rise of drain voltage is also much slower —so slow, in fact, that the drain voltage never reaches the clamping level of 95V. In this case, all the switching energy must be dissipated in the device itself, and there is no opportunity for shunting some of this into an external clamp. The total switching time increases from 175 ns [Figure 30(a)] to 400 ns, and the total switching energy increases from 280 to 450 μJ. Once again, the turn-off energy of 450 μJ is much greater than the turn-on energy of 55 μJ for the same value of $L\ell$ and R_{DR} [Figure 29(b)].

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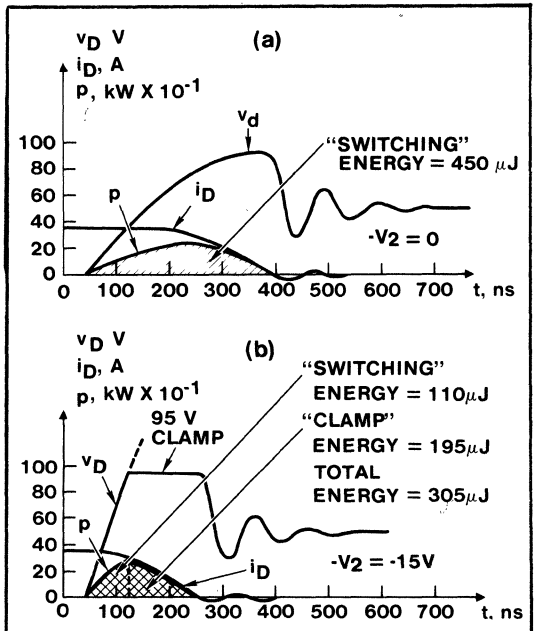


Figure 32. Turn-Off Waveforms for:
(a) "Negative Drive Voltage" ($-V_2$) = 0
(b) "Negative Voltage" ($-V_2$) = 15V

IRF 150 R_{DR} =50Ω
L_S = 200nH

Figure 30(c) shows turn-off waveforms for R_{DR} = 50 ohms, but with $L\ell$ increased to 1 μH. As would be expected, the initial rate of change of drain voltage is the same as in Figure 30(b); until the drain voltage becomes equal to the circuit voltage of 50V, the drain current remains constant at I_O, and $L\ell$ has no effect. Thereafter, however, the drain voltage moves much more rapidly upwards, and has no difficulty in reaching the clamp level of 95V. The total switching time increases to 950 ns, because of the increased value of $L\ell$, and the total switching energy increases from 450 μJ in Figure 30(b) to 1435 μJ in Figure 30(c).

It is interesting to compare the energy reduction at turn-on when $L\ell$ is increased from 200 nH to 1 μH, Figures 29(b) and (c), versus the energy increase at turn-off [Figures 30(b) and (c)]. The energy *reduction* at turn-on is (55 - 1.8) = (53.2 μJ, while the energy *increase* at turn-off is (1435 - 450) = 985 μJ. The net effect of increasing drain circuit inductance is a very substantial increase in the *total* energy dissipation.

The waveforms in Figure 31 show the effect of increasing the applied drive voltage from 10V to 15V, for R_{DR} 50 ohms and $L\ell$ = 200 nH. The total switching time decreases from 360 ns to 160 ns, and the switching energy decreases from 55 μJ to 6 μJ.

Figure 32 shows the same comparison for the turn-off interval. The waveforms in Figure 32(a) are for no applied drive voltage during the turn-off interval, while those in Figure 32(b) are for a negative drive voltage of -15V. The total switching time decreases from 400 to 250 ns, and the switching energy from 450 to 305 μJ. The negative gate drive voltage not only reduces the total switching energy, but also, because it forces the drain voltage to reach the 95V clamping level, it offers the possibility for "dumping" 195 μJ of energy which would otherwise be dissipated in the HEXFET, into an external clamp.

VII. The Effect of Common Source Inductance

So far we have ignored the effect of the common source inductance L_S, shown dashed in Figure 2. This inductance will always be present to some extent; even with careful circuit layout, the user will have to accept, at a minimum, the internal lead inductance within the package of the device. For a TO-3 package, this inductance is in the order of 10 to 15 nH. We will now consider briefly the modifying effect of L_S on the switching operation.

Figure 33 shows the general equivalent circuit which includes L_S. As the drain current i_D starts to increase at turn-on, a voltage will be developed across L_S due to the rate of change of drain current. This voltage is common to the gate circuit, and its polarity is such to reduce the net voltage appearing between the gate and source terminals. Like the "Miller" effect, which provides a negative feedback from the drain to the gate, slowing down the rate of change of current, so the common source inductance also provides a negative feedback, from the source circuit to the gate, also slowing down the change of drain current.

A complete analysis of the switching operation that includes the effect of the common source inductance can be accomplished by means of the procedures already presented. This is beyond the scope of this paper. We will content ourselves instead with an approximate analysis, the main benefit of which is the extreme simplicity of the result.

Referring to the equvialent circuit in Figure 33, it is evident that L_S only has an effect when the drain current is changing, and the HEXFET is in its active region. This restricts the analysis to interval 2 during turn-on, and interval 3 during turn-off.

The loop equation for the gate circuit is:

$$i_{DR}R_{DR} + \frac{i_{GS}}{pC_{GS}} + pL_S i_{GS} + pL_S i_D = V_{DR} \qquad (53)$$

By making the approximation (valid for practical operating conditions) $pL_S i_D \gg pL_S i_{GS}$, equation (53) becomes:

$$i_{DR}R_{DR} + \frac{i_{GS}}{pC_{GS}} + pL_S i_D = V_{DR} \qquad (54)$$

Now

$$i_D = g_{fs}v_{GS} = \frac{g_{fs}i_{GS}}{pC_{GS}} \qquad (55)$$

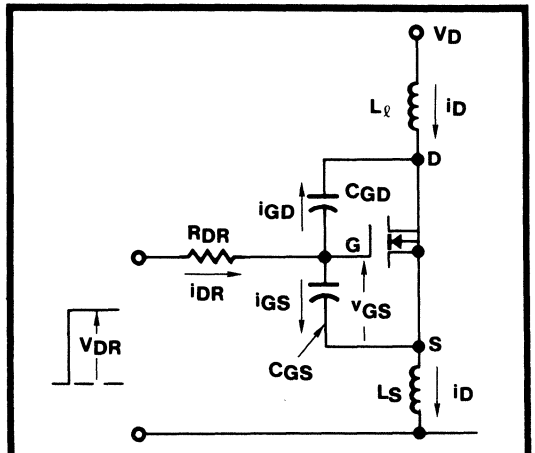


Figure 33. Equivalent Circuit Including the Effect of Common Source Inductance, L_S

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Substituting for i_D into equation (54) gives:

$$i_{DR}R_{DR} + \frac{i_{GS}}{pC_{GS}} + \frac{g_{fs}L_S i_{GS}}{C_{GS}} = V_{DR} \quad (56)$$

It is seen from equation (56) that the effect of L_S, has been to add a resistive voltage drop, equal to R i_{GS}, into the loop equation, where:

$$R' = \frac{g_{fs}L_S}{C_{GS}} \quad (57)$$

Equation (57) quantifies the voltage which subtracts from the gate-to-source voltage, and hence acts to restrict the switching speed. Since $i_{GS} \ll I_{DR}$ [i_{GS} i_{DR} as $L\ell/R_{RD} \rightarrow 0$] we could conservatively represent this voltage drop as $R'i_{DR}$. To be sure this will be "over representing" the modifying effect of L_S, but the result is too simple to resist. The loop equation then becomes:

$$i_{DR}(R_{DR} + R') + \frac{i_{GS}}{pC_{GS}} = V_{DR} \quad (58)$$

We conclude that we can conservatively represent the effect of the source inductance L_S by simply adding an equivalent resistance R', given by equation (57) to the "real" drive circuit resistance, R_{DR}.

The only modification we then have to make to the analytic expressions already obtained is to substitute (R_{DR} + R') for R_{DR}, for turn-on interval 2 and turn-off interval 3. The analytic expressions for all other intervals remains unaltered.

It is interesting to see what a typical value of R' will be. Taking the IRF150, 100V 28A HEXFET, and assuming L_S = 10 nH, R' 30Ω.

According to this simple representation, the modifying effect of L_S will clearly be greatest when the "real" drive circuit resistance is low. This is to be expected. We should bear in mind, however, that this equivalent representation will tend to become progressively more conservative as the real drive circuit resistance becomes lower (assuming that this accompanied by a corresponding increase in $L\ell/R_{DR}$). This is because as the "Miller" effect becomes greater i_{GS} becomes smaller relative to i_{DR} and hence the approximation $i_{GS}R' \doteq i_{DR}R'$ becomes more conservative.

VIII. Conclusions

Our major objective has been to convey an understanding of the switching operation of the HEXFET, by giving a physical insight into the switching mechanism, and into the interaction of the HEXFET with the external circuit, and to provide analytical tools that enable the switching performance to be quantified at the design stage. The major conclusions are as follows:

1. The shapes of the switching waves during the intervals that the drain current and drain voltage simultaneously change are profoundly influenced by the external circuit parameters—specifically the drain circuit inductance and the gate circuit resistance. A given ratio of these parameters substantially determines the geometry of the switching waves, but the actual switching time depends upon specific values.
2. At turn-on, the current rises before the voltage fall is completed, if the ratio of $L\ell/R_{DR}$ is small (assuming a clamped inductive load). The converse is true, if the ratio of $L\ell/R_{DR}$ is large.
3. At turn-off, the drain voltage always rises to the circuit voltage while the drain current remains constant (assuming an inductive load). The rate of rise of drain voltage is controlled by the drive circuit resistance, but it is independent of drain circuit inductance. Once the drain voltage reaches the circuit voltage, the waveshapes then depend upon the ratio of $L\ell/R_{DR}$.
4. The turn-off energy is always greater than the turn-on energy. Increasing the drain circuit inductance decreases turn-on losses, but increases the turn-off losses by a far greater amount. The smaller this inductance, the faster the switching times, and the lower the overall energy losses. It is good design practice, therefore, to keep this inductance as small as possible, by appropriate attention to circuit layout, transformer design, etc.
5. Turn-on time and turn-on energy can be decreased by increasing the applied drive voltage. Turn-off time and turn-off energy can be decreased by applying an increasing negative drive voltage.
6. Common source inductance reduces the switching speed and increases switching energy. It effects the operation during those intervals in which the drain current changes, and the HEXFET is in its active mode (turn-on interval 2, and turn-off interval 3). For these intervals it can be conservatively represented by an equivalent resistance added in series with the drive circuit resistance. □

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2. "Analysis and Characterization of Power MOSFET Switching Interval Performance, " S.M. Clemente, B.R. Pelly. A. Isidori, POWERCON 8, 1981.

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CHAPTER 9
APPLICATION NOTE 942

Simplified HEXFET® Power Dissipation and Junction Temperature Calculation Speeds Heatsink Design

by R. SEVERNS

The reliability and life expectancy of HEXFETs, like that of any power semiconductor, is directly related to the maximum junction temperature the device experiences. It is, therefore, vital for the designer to be able to accurately determine the device power dissipation and the maximum junction temperature. The power dissipation and maximum junction temperature along with the ambient temperature, determine the design of the heatsink.

The first step in this process is to determine the total power dissipation in the device. This is not trivial since while the power dissipation determines the junction temperature, the power dissipation is itself a function of the junction temperature, because the on-resistance increases with temperature. Because of the nonlinear nature of the on-resistance increase, which varies from one device type to another, strictly analytical solutions can be time-consuming.

This application note presents a simple graphical method for determining the total power dissipation and junction temperature for any given heatsink. The method provides a graphic illustration of the conditions that provide a sound and stable thermal design, as well as showing the designer conditions that are to be avoided because they lead to unnecessary thermal runaway.

The total power dissipation (P_T) is the sum of the switching transition loss (P_S), the conduction loss (P_C), a fraction of the gate drive power (P_G), and the loss due to I_{DSS} (P_L), during the switch OFF time.

Switching Transition Loss

Because of the rapid transition times which are possible, P_S for a HEXFET can, in theory, be almost arbitrarily small for switching rates up to several hundred kHz if a sufficiently low impedance gate driver is used. In a practical circuit, however, there are often limitations on the switch transition time, due to transient ringing of parasitic circuits or the capabilities of the rectifier diodes, so that P_S is usually not negligible. Even if the switching time were zero, any practical circuit will have stray capacity in the drain circuit. The energy stored in this capacity while the device is OFF will be dissipated in the switch at turn-on.

Unlike a bipolar switch, the losses during switching for a MOSFET are not increased by quasi-saturation or current tailing. As shown in Figure 1(a), the switching waveforms for an inductive load can usually be closely approximated by two straight lines. The switching loss for each type of transition (turn-on or turn-off) is then:

$$P_S = \frac{(V_{DS(max)} \cdot I_{D(max)})}{2} \tau_s f_s \qquad (1)$$

where f_s is the switching frequency.

The values for $V_{DS(max)}$ and τ_s will probably differ for the turn-on and turn-off transitions due to stray inductance and capacitance. P_S is then the sum of the turn-on and turn-off transition losses.

If the load is resistive, then the switching transitions will be as shown in Figure 1(b) and the losses due to each type of transition can be expressed as:

$$P_S = \frac{(V_{DS(max)} \cdot I_{D(max)})}{6} \tau_s f_s \qquad (2)$$

If, because of load or drive circuit peculiarities, the straight line approximations of Figure 1 are not sufficiently accurate, then the power dissipation can be found from:

$$P_S = f_s \int_0^{\tau_s} V_{DS}(t) \cdot I_D(t)\, dt \qquad (3)$$

Usually a simple piecewise linear approximation for $V_{DS}(t)$ and $I_D(t)$ is sufficient.

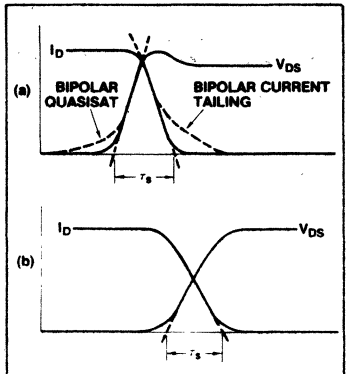


Figure 1. Inductive and Resistive Load Switching Transitions

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When the switching losses are calculated from circuit oscillographs, the foregoing equations are quite accurate, but if the losses are being estimated in advance of breadboarding the circuit, a slightly different procedure is needed.

It is not unusual for $C_{DS} + C_{stray}$ to be large enough to significantly alter the transition time of V_{DS} during turn-off. Figure 2 shows an oscillograph of typical switching waveforms in a power converter. Note that even though the gate turn-on and turn-off times are identical, the transition time at turn-off is noticeably longer than at turn-on. This is due to the finite charging time for the capacitance in the drain circuit by the drain load current.

This capacitance, as shown in Figure 3, includes C_{oss} which is integral to the device, and the stray capacitance in the drain circuit. A TO-3 case, using a thin mica or plastic film insulating washer will add about 200pF to C_{stray}. A 0.062" beryllia washer, on the other hand, will add only about 25pF to C_{stray} and as an additional benefit will provide a lower case-to-heatsink thermal impedance ($R_{\theta CH}$).

P_S can be estimated by using equations (1) or (2) with the anticipated transition times due to the gate drive characteristics in the absence of the output capacitance and then include an additional loss (P_{SC}) due to the drain capacitance.

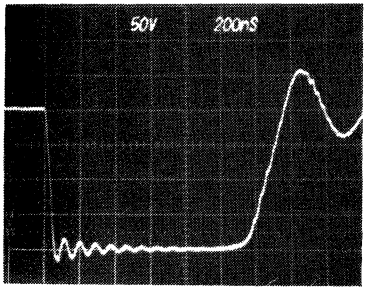


Figure 2. Effect of Drain-Source Capacity

This loss is:

$$P_{SC} = \frac{(C_{DS} + C_{stray})\, V^2_{DS} f_s}{2} \qquad (4)$$

where V_{DS} is the value of V_{DS} at switch turn-on.

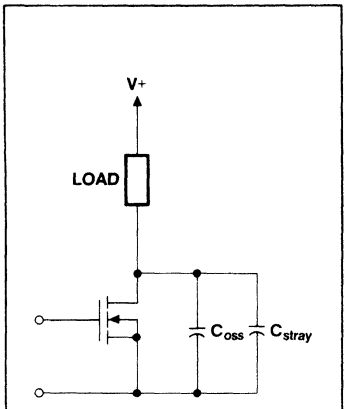


Figure 3. Drain-to-Source Capacitances

Drain-Source Leakage Current Losses

During the switch OFF period, a small temperature-dependent current (I_{DSS}) will flow through the switch.

The loss due to this current is:

$$P_L = I_{DSS} \cdot V_{DS} (1 - D) \qquad (5)$$

where V_{DS} is the drain-source voltage during the OFF time and D is the ON time duty cycle of the switch.

Even for T_J = 150°C, this loss is usually quite small, of the order of ½W or less in a 400V device. There are, however, circumstances where P_L is not insignificant. If due to the drive circuit, $V_{GS} > 0$ during the OFF time, then I_{DSS} can be an order of magnitude larger, and in that case, P_L may well be important. This problem can arise when driving the HEXFET from IC logic.

Normally, with the logic driver in the "0" state, the current into the driver from the HEXFET is minute (nanoamperes or less) and the gate-source voltage is very low. However, if an open collector driver is used with a relatively low value of resistance in the collector to improve the switching speed, the "0" state gate-source voltage may be high enough to significantly increase I_{DSS}.

Due to the considerable variation in I_{DSS} as a function of T_J, V_{GS} and $V_{GS(th)}$ from one device to another, it is difficult to quantify this effect in advance of the actual design. The designer will need to look at the actual circuit to see if there is a problem when the device is being operated in a radiation environment or if V_{GS} is substantially greater than zero during the OFF time.

In a radiation environment, $V_{GS(th)}$ is progressively reduced as the dosage is increased. This can dramatically increase I_{DSS}, and it is recommended that I_{DSS} be reduced by applying a negative V_{GS} during the OFF time.

Dissipation Due to Gate Drive

A portion of the gate drive power (P_{Gi}) will be dissipated internally by the device due to the internal gate resistance. The portion of the total gate drive power (P_G) dissipated in the device depends on the internal gate resistance (R_G), and the external drive source resistance (R_S) and may be expressed as:

$$P_{Gi} = P_G\left(\frac{R_G}{R_S + R_G}\right)$$

$$P_{Gi} = V_{GS}\, Q_G\, f_s\left(\frac{R_G}{R_S + R_G}\right) \qquad (6)$$

R_G is typically 1 to 10Ω. For switching rates below 100kHz, P_{Gi} is very small and may be ignored, but as the switching rate is increased, R_S must be reduced to obtain faster transition times, and P_G is increased due to the faster switching rate. In addition, the amount of V_{GS} overdrive is often increased to further reduce the transition times. The net result is that P_{Gi} may be significant especially for switching frequencies above 500kHz.

Conduction Power Loss

The major power loss in a MOSFET is P_C. The conduction loss is:

$$P_C = I^2_{D(RMS)}\, R_{DS(on)} \qquad (7)$$

Equation (7) is deceptively simple. In many applications, I_D will be a duty cycle modulated triangular or trapezoidal waveform, and the designer must calculate the RMS value of the drain current. $R_{DS(on)}$ is a function of I_D, T_J and V_{GS}, and T_J is itself a function of P_T.

The data sheet provides graphs for determining $R_{DS(on)}$. Figure 4 shows $R_{DS(on)}$ as a function of V_{GS} and I_D at T_J = 25°C, and Figure 5 shows the normalized value of $R_{DS(on)}$ as a function of T_J.

The first step is to determine $I_{D(RMS)}$ and V_{GS} and then the value of $R_{DS(on)}$ at 25°C [$R_{DS(on)25°C}$] can be taken from Figure 4. If T_J is known, then the appropriate multiplier for $R_{DS(on)25°C}$ can be found from Figure 5 and P_C calculated directly from equation (7). Note that Figure 5 is for

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a particular value of I_D and V_{GS}. The curve does not change very much for variations in I_D, but it is strongly affected by changes in V_{GS} when V_{GS} is close to $V_{GS(th)}$. The value of V_{GS} selected for the data sheet curve is well above $V_{GS(th)}$ and as long as the designer uses a value of V_{GS} equal to or greater than the curve value, then little error will occur.

Instead of using Figure 6, an analytical expression for $R_{DS(on)}$ can be used:

$$R_{DS(on)} \cong R_{DS(on)}25°C\left(1+\frac{\alpha}{100}\right)^{T_J-25} \quad (8)$$

The dashed line on Figure 5 is a plot of equation (8) with $\alpha = 0.7$. The fit of the equation is very good above 25° C, but below 25° C the fit becomes quite poor. Figure 5 is for an IRF431 which is a 450V device. Figure 6 shows the normalized $R_{DS(on)}$ curve for an IRF151, a 100V device. Using an α of 0.4, the fit is very good, and the analytic expression for $R_{DS(on)}$ is quite accurate. As the examples in Figure 5 and 6 show, both the shape of the $R_{DS(on)}$ curve and the value for α, vary from one device type to another and for each value of V_{GS}. In order to determine α, it is necessary to have the $R_{DS(on)}$ versus temperature curve, but if one has the curve, then there is no real need for an analytic solution since the graphical solution is simpler and will produce answers of sufficient accuracy. For those who wish an analytic solution using equation (8), Table I is a tabulation of solutions to that equation.

The solution for P_C is not so easy if T_J is not defined. In a typical application, the properties of the heatsink may be defined and the designer must then calculate both P_C and T_J for a variety of load and line conditions. In this case, P_C is in part determined by P_S, P_L and P_G and the solution has to include these losses. Fortunately, there is a simple graphical solution method.

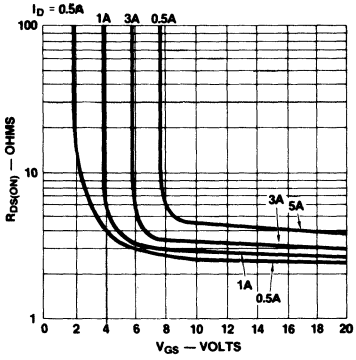


Figure 4. $R_{DS(ON)}$ Dependence on I_D

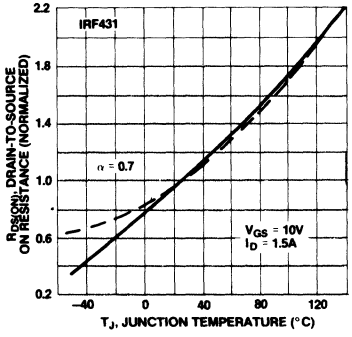


Figure 5. Normalized On-Resistance Vs. Temperature (IRF431)

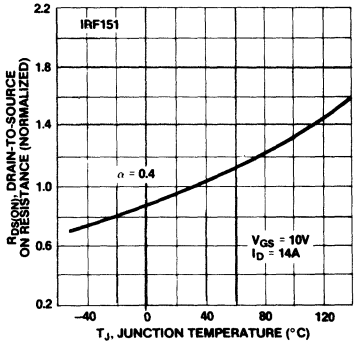


Figure 6. Normalized On-Resistance Vs. Temperature (IRF151)

Table I

		$R_{DS(on)}$ NORMALIZED														
T_J °C T_A = 25° C	ΔT_J °C	α = 0.30	α = 0.35	α = 0.40	α = 0.45	α = 0.50	α = 0.55	α = 0.60	α = 0.65	α = 0.70	α = 0.75	α = 0.80	α = 0.85	α = 0.90	α = 0.95	α = 1.00
-40	-65	0.82	0.80	0.77	0.75	0.72	0.70	0.68	0.66	0.64	0.62	0.60	0.58	0.56	0.54	0.52
-20	-45	0.87	0.85	0.84	0.82	0.80	0.78	0.76	0.75	0.73	0.71	0.70	0.68	0.67	0.65	0.64
0	-25	0.93	0.92	0.91	0.89	0.88	0.87	0.86	0.85	0.84	0.83	0.82	0.81	0.80	0.79	0.78
25	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
40	15	1.05	1.05	1.06	1.07	1.08	1.09	1.09	1.10	1.11	1.12	1.13	1.14	1.14	1.15	1.16
60	35	1.11	1.13	1.15	1.17	1.19	1.21	1.23	1.25	1.28	1.30	1.32	1.34	1.37	1.39	1.42
80	55	1.18	1.21	1.25	1.28	1.32	1.35	1.39	1.43	1.47	1.51	1.55	1.59	1.64	1.68	1.73
100	75	1.25	1.30	1.35	1.40	1.45	1.51	1.57	1.63	1.69	1.75	1.82	1.89	1.96	2.03	2.11
120	95	1.33	1.39	1.46	1.53	1.61	1.68	1.77	1.85	1.94	2.03	2.13	2.23	2.34	2.46	257
140	115	1.41	1.49	1.58	1.68	1.77	1.88	1.99	2.11	2.23	2.36	2.50	2.65	2.80	2.97	3.14
160	135	1.50	1.60	1.71	1.83	1.96	2.10	2.24	2.40	2.56	2.74	2.93	3.14	3.35	3.58	3.83
180	155	1.59	1.72	1.86	2.01	2.17	2.34	2.53	2.73	2.95	3.18	3.44	3.71	4.01	4.33	4.68
200	175	1.69	1.84	2.01	2.19	2.39	2.61	2.85	3.11	3.39	3.70	4.03	4.40	4.80	5.23	5.70

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Graphical Solution for MOSFET Thermal Design

From the earlier discussion:

$$P_T = P_S + P_L + P_G + P_C \quad (9)$$

For convenience, one can lump together the fixed losses*:

$$P_1 = P_S + P_L + P_G \quad (10)$$

Substituting equations (7) and (10) in equation (9):

$$P_T = P_1 + I^2_{D(RMS)}\, R_{DS(on)} \quad (11)$$

From thermal considerations:

$$T_J = T_A + R_{\theta JA}\, P_T \quad (12)$$

and

$$R_{\theta JA} = R_{\theta HA} + R_{\theta CH} + R_{\theta JC} \quad (13)$$

**This example ignores the temperature dependent nature of P_L on the assumption that it is negligible or that the worst case value is used.*

To determine P_C and T_J requires the simultaneous solution of equations (11) and (12). This can be done graphically as shown in Figure 7.

If P_1 and $I_{D(RMS)}$ are presumed constant over the range of T_J the shape of the P_T versus T_J curve is determined by $R_{DS(on)}$. Except for a scale factor and an offset, the curve for P_T is exactly the same as that shown in Figures 5 and 6

The scale factor is:

$$K_1 = I^2_{D(RMS)}\, R_{DS(on)\,25°C} \quad (14)$$

The offset is:

$$K_2 = P_1$$

Then the total power dissipation is:

$$P_T = K_1\, R_{DS(on)normalized} + K_2$$

The curve for equation (12) is simply a straight line with slope of $1/R_{\theta JA}$ and which intersects the T_J axis at $T_J = T_A$.

$$\frac{1}{R_{\theta JA}} = \left(\frac{P_T}{T_J - T_A}\right) \quad (15)$$

The intersection of the two curves is the desired solution. Figure 7 clearly demonstrates the effect of increasing $R_{\theta JA}$. As $R_{\theta JA}$ is increased, both P_T and T_J increase. A point is reached where there may be two intersections of the curves at T_{J2} and T_{J2}'.

T_{J2} represents a point of stable thermal equilibrium and T_{J2}' represents an unstable equilibrium point. That this is so can be seen by inspection of Figure 7 as follows:

1. Stable equilibrium can exist only if the heat input (P_T) from the switch equals the heat dissipated by the sink.
2. For $T_J < T_{J2}'$ P_T exceeds the heat removed by the sink. T_J must therefore rise, increasing P_T, until $T_J = T_{J2}'$ where P_T equals the heat removed.
3. For $T_{J2} < T_J < T_{J2}'$ the heat removed by the sink is greater than P_T and the device must cool down, reducing P_T, until $T_J = T_{J2}'$.
4. If $T_J > T_{J2}'$ then P_T is always greater than the heat removed. P_T and T_J will then increase without limit until the device is destroyed. This is a thermal runaway condition.

As long as the initial temperature is less than T_{J2}' then T_J will converge at T_{J2}. If $R_{\theta JA}$ is further increased to $R_{\theta JA2}$, there is no intersection of the curves and this also represents a condition of thermal runaway, since P_T is always greater than the heat removed by the heatsink.

Design Example 1

Device	= IRF431
$R_{\theta JC}$	= 1.7 deg. C/W
$R_{\theta CH}$	= 0.4 deg. C/W
$R_{\theta HA}$	= 2 deg. C/W and 4 deg. C/W
$I_{D(RMS)}$	= 2.1A
$R_{DS(on)25°C}$	= 1.7Ω (max. $R_{DS(on)}$ at I_D = 3A)
T_A	= 55°C
P_1	= 0

Find T_J and P_T for each value of $R_{\theta HA}$.

$R_{\theta JA}$	= $R_{\theta JC} + R_{\theta CH} + R_{\theta HA}$
$R_{\theta JA1}$	= 4.1 deg. C/W
$R_{\theta JA2}$	= 6.1 deg. C/W

The graphical solution is shown in Figure 8. For $R_{\theta HA}$ = 2 deg. C/W, P_T = 14.5W and T_J = 115° C. For $R_{\theta HA}$ = 4 deg. C/W, there is no intersection and the device will experience thermal runaway.

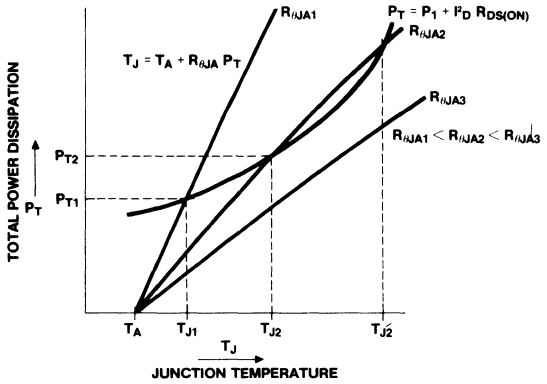


Figure 7. Graphical Representation of the Thermal Equations

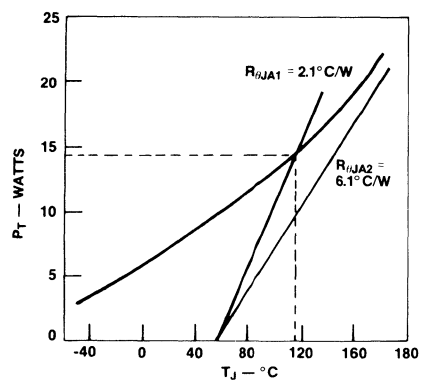


Figure 8. Design Example 1

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Suppose one wishes to set P_I to some value other than zero or to vary I_D. The solution method used in Figure 8 would require the graphs to be redrawn for each new condition. It would be preferable if the normalized ON-resistance versus temperature graph could be used directly without a change of scale for all solutions. The P_T and T_J calculations could then be done directly on the data sheet curves, adding only straight lines. This can be done by normalizing the P_T scale.

At any temperature:

$$P_T = P_I + I^2_{D(RMS)} R_{DS(on)} \quad (16)$$

At 25°C:

$$P_{T(25°C)} = P_I + I^2_{D(RMS)} R_{DS(on)25°C} \quad (17)$$

Reordering equations (16) and (17):

$$P_T - P_I = I^2_{D(RMS)} R_{DS(on)} \quad (18)$$

$$P_{T(25°C)} - P_I = I^2_{D(RMS)} R_{DS(on)25°C} \quad (19)$$

Dividing equation (18) by equation (19):

$$\frac{P_T - P_I}{P_{T(25°C)} - P_I} = \frac{R_{DS(on)}}{R_{DS(on)25°C}} \quad (20)$$

$= R_{DS(on)N}$ = normalized value of $R_{DS(on)}$ as given in the data sheet graph.

If we then define the normalized power P_N:

$$P_N \cong \frac{P_T - P_I}{P_{T(25°C)} - P_I} = R_{DS(on)N} \quad (21)$$

$$P_N = R_{DS(on)N}$$

The vertical scale of the $R_{DS(on)}$ normalized scale is now numerically equal to P_N.

In a similar fashion, the second equation can be normalized:

$$T_J = T_A + R_{\theta JA} P_T \quad (23)$$

Rearranging equation (21):

$$P_T = P_I + P_N [P_{T(25°C)} - P_I] \quad (24)$$

Equation (24) may be simplified to:

$$P_T = P_I + P_N [I^2_{D(RMS)} \cdot R_{DS(on)25°C}] \quad (25)$$

And then combine equations (23) and (25):

$$T_J = T_A + R_{\theta JA} [P_I + P_N \cdot (I^2_{D(RMS)} R_{DS(on)25°C})] \quad (26)$$

Once a graphical solution in terms of P_N is found, T_J may be read out directly and P_T can be calculated from equation (25).

Design Example 2

Refer to Figure 9.

Device	= IRF431
$R_{\theta JC}$	= 1.7 deg. C/W
$R_{\theta CH}$	= 0.4 deg. C/W
$R_{\theta HA}$	= 2 deg. C/W
$R_{DS(on)25°C}$	= 1.7Ω at 2.1A and 1.5Ω at 1.2A
T_A	= 55°C
$I_{D(RMS)}$	= 2.1 and 1.2A
P_I	= 0W and 4W

Find T_J and P_T for each case.

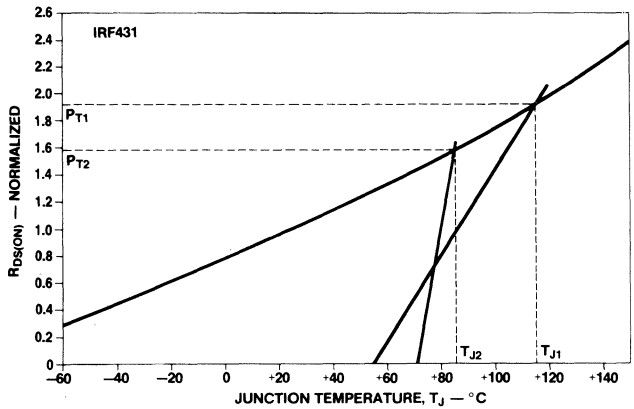


Figure 9. Design Example 2

Solution 1

Step 1:
Locate two points on the graph to plot equation (26):

Point 1: For $P_N = 0$, $T_J = T_A$

Point 2: For $P_N = 1$

$T_J = T_A + R_{\theta JA} I^2_{D(RMS)} R_{DS(on)25°C}$

$T_J = 55° + (4.1)(2.1^2)(1.7) = 86°C$

Step 2:
Draw a straight line through:

$P_N = 0, T_J = 55°C$ and $P_N = 1, T_J = 86°C$

Step 3:
Read T_J directly off, $T_J = 115°C$

$P_N = 1.9$

Step 4:
Calculate P_T

$P_T = P_I + I^2_{D(RMS)} R_{D(on)25°C} P_N$

$P_T = 0 + (2.2^2)(1.7)(1.9)$

$P_T = 14.5W$

Solution 2

$I_{D(RMS)}$ is reduced to 1.2A and P_I is increased to 4W. T_A remains at 55°C.

Step 1:
Find two points for equation (26) with $P_N = 0$ and $P_N = 1$.

Point 1:

$T_{J1} = T_A + R_{\theta JA} P_I$

$T_{J1} = 55 + (4.1)(4)$

$T_{J1} = 71°C$

Point 2:

$T_{J2} = T_A + R_{\theta JA} P_{T(25°C)}$

$T_{J2} = 55 + 4.1 [(1.2^2)(1.5) + 4]$

$T_{J2} = 80°C$

Step 2:
Draw a straight line through:

$P_N = 0, T_J = 71°C$ and $P_N = 1, T_J = 64°C$

Step 3:
Read off $T_J = 85°C$ and $P_N = 1.6$

Step 4:
Calculate P_T

$P_T = 4 + 1.6 [(1.2^2)(1.5)]$

$P_T = 7.5W$

Determination of the Peak Junction Temperature for Pulsed Current Waveforms

The previous discussion and examples were for the average junction temperature. For very long (> 1 sec.), high duty cycle pulses or very short

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(< 10μs) pulses, the peak junction temperature is very nearly equal to the average junction temperature, and the procedure is acceptable. For other operating conditions, the procedure is identical, but the equation (26) must be modified to use the transient thermal impedance, $Z_{\theta JC}$. $Z_{\theta JC}$ is related to $R_{\theta JC}$ by:

$$Z_{\theta JC} = r(t)\ R_{\theta JC} \qquad (27)$$

where r(t) is the normalizing factor taken from the normalized transient thermal impedance curves for the particular device. The appropriate values for the pulse width (t_p) and duty cycle (D) must be used.

Equation (26) can now be modified to:

$$T_J = T_A + (r(t)\ R_{\theta JC} + R_{\theta CA})[P_l + P_N (I^2_{D(RMS)}\ R_{DS(on)25°C})] \qquad (28)$$

The procedure is exactly as shown earlier except that equation (28) is used instead of equation (26).

Summary

The power loss calculation for a power MOSFET differs substantially from the same calculation for a bipolar power transistor primarily because of the $I^2_{D(RMS)}\ R_{DS(on)}$ loss characteristic. The calculation is further complicated by the non-linear behavior of $R_{DS(on)}$ versus T_J. Because the $R_{DS(on)}$ characteristic must be determined experimentally for each device type, a strictly algebraic approach to the loss calculation is very cumbersome. The graphical method shown here is much more rapid and is just as accurate.

APPENDIX

Determining the RMS Value of I_D Waveforms

To accurately determine the conduction losses in a MOSFET, the RMS value for I_D must be known. The current waveforms are rarely simple sinusoids or rectangles, and this can pose some problems in determining the value for I_{RMS}. The following equations and procedure can be used to determine I_{RMS} for any waveform that can be broken up into segments for which the RMS value can be calculated individually.

The RMS value of any waveform is defined as:

$$I_{RMS} = [1/T \int_0^T [I(t)]^2\ dt]^{1/2} \qquad (1)$$

Figure A-1 shows several simple waveforms and the derivation for I_{RMS} using equation (1).

If the actual waveform can be approximated satisfactorily by combining the waveforms in Figure A-1, then the RMS value of the waveform can be calculated from:

$$I_{RMS} = \sqrt{I^2_{RMS(1)} + I^2_{RMS(2)} + \ldots + I^2_{RMS(N)}} \qquad (2)$$

In some applications such as switching regulators, it is possible for the designer to control the wave shape to some extent. This can be very beneficial in reducing the value for I_{RMS} in the switch for a given value of average current (I_{AVG}).

Effect of Waveform Shape on RMS Value

In a switch mode converter, the current waveforms through the inductors, transformer windings, rectifiers and switches will appear as shown in Figure A-2, ranging from a triangle to a rectangle depending on the value of the averaging inductor and the load. For the capacitors, the waveforms will be similar, except that there can be no DC component as shown in Figure A-3. The RMS values of the waveform are given in the figures.

It can be shown that:

$$K = \frac{I_a}{I_b} = f(L/L_c) \qquad (3)$$

where:
L = inductance of the averaging choke.

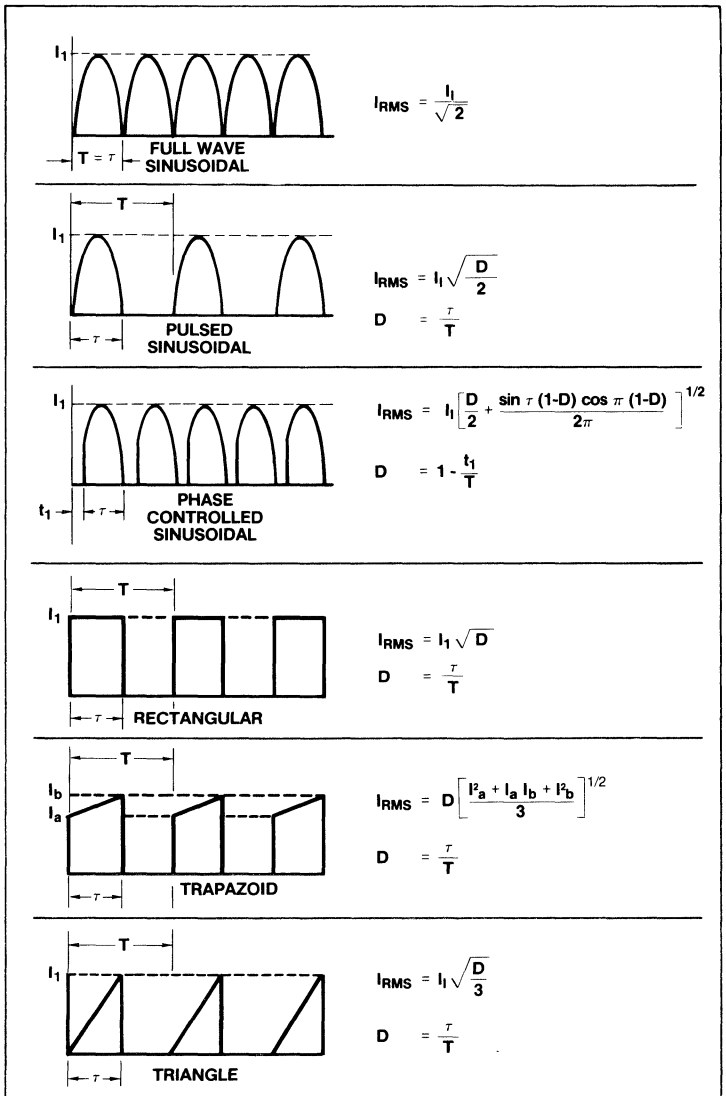


Figure A-1.

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$L_c = 1$ is the critical inductance for a particular input voltage and load power.

As L is increased, K goes from 0 (triangle) to 1 (rectangle). Substituting $K = I_a/I_b$, for the continuous choke current case:

$$I_{RMS} = \frac{2\,I_{(avg)}}{\sqrt{D}}\sqrt{\frac{K^2 + K + 1}{3\,(K+1)^2}} \qquad (4)$$

For constant $I_{(avg)}$ and D, the normalized ($I_{RMS} = 1$ for $K = 1$) I_{RMS} is as shown in Figure A-4. This curve shows that, for triangular current waveforms, the I^2R losses are 32% higher than for rectangular waveforms. It is also apparent that for $I_a/I_b > 0.6$, the additional losses incurred by having $L < \alpha$ is only 2%, so from a practical point of view, L need only be about twice L_c. Increasing the value of I_a/I_b increases the switch turn-on losses but decreases the turn-off losses. Since the turn-off losses frequently dominate, increasing I_a/I_b reduces the total switching loss also.

For the case of discontinuous inductor current ($L < L_c$), $I_a/I_b = 0$ and is no longer relevant, since the waveforms are now triangles. For a given $I_{(avg)}$ the RMS current is:

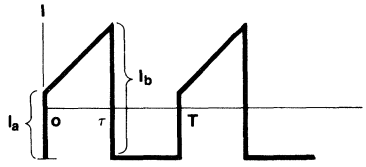
$$I_{RMS} = \frac{2\,I_{(avg)}}{\sqrt{3D}}$$

A plot of equation (4) is given in Figure A-5, where $I_{(avg)}$ is constant and I_{RMS} is normalized to $D = 1$. Obviously, triangular current waveforms with high peak currents and low duty cycles are to be avoided if low losses are desired.

For the case where: $I_a = I_b$:

$$I_{RMS} = \frac{I_{(avg)}}{\sqrt{3D}}$$

the curve in Figure A-5 also applies. It is important to realize that for a given input voltage, current and transformation ratio, there can be a difference in duty cycle which allows one circuit to have lower losses due to the lower value of I_{RMS}.



GENERAL CASE

$$I_{RMS} = \left\{D\left[\frac{I_a^2 + I_a I_b + I_b^2}{3} - \frac{D}{4}(I_a + I_b)^2\right]\right\}^{1/2}$$

$$D = \frac{\tau}{T}$$

SPECIAL CASES

1) $D = 1$

$$I_{RMS} = \frac{I_b - I_a}{\sqrt{12}}$$

2) $I_a = I_b$

$$I_{RMS} = I_a\sqrt{D - D^2}$$

3) $I_a = 0$

$$I_{RMS} = I_b\sqrt{\frac{D}{3} - \frac{D^2}{4}}$$

Figure A-2. RMS Current Through a Capacitor

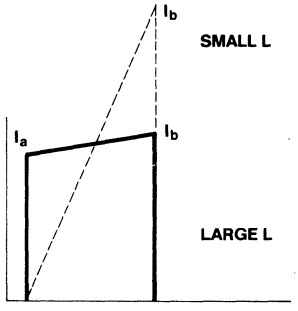


Figure A-3. Current Waveform

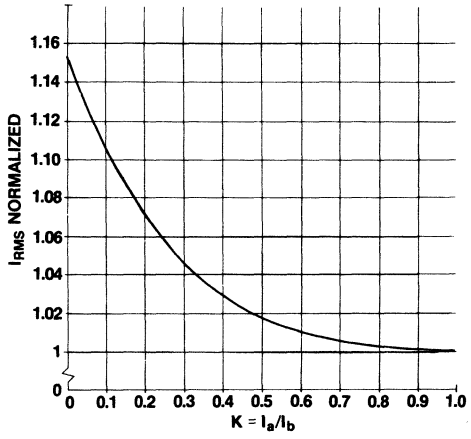


Figure A-4. Variation of I_{RMS} with Squareness Ratio

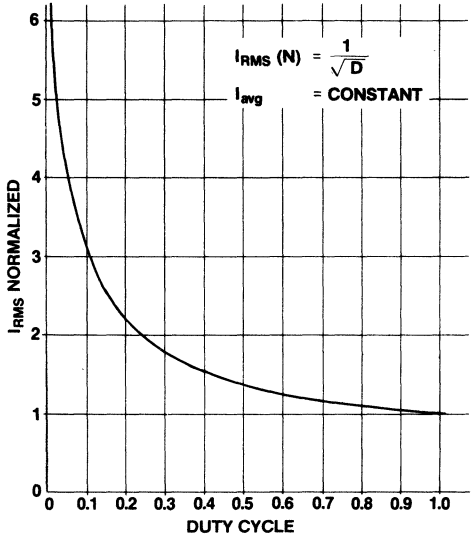


Figure A-5. Variation of I_{RMS} Value with Duty Cycle

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By S. CLEMENTE, B. PELLY, R. RUTTONSHA

Summary

Power MOSFETs are attractive candidates for use in switching power supplies. In order to take full advantage of their unique characteristics, one cannot simply substitute a MOSFET for a bipolar transistor in an existing circuit. More fundamentally, it is necessary to rethink basic concepts, and to shape the circuit around the operating features of the device.

This application note describes a 100kHz, 100W off-line power supply providing a regulated 5V DC output. The circuit is "universal" in the sense that it operates both from 115V and 240V line inputs, without any alteration of circuitry or switching of components. The circuit uses a single 500V-rated power HEXFET in a modification of the classical "forward converter" circuit.

Introduction

DC power supplies are employed today wherever electrical or electronic equipment is in use. Traditional designs that operate from AC input power are based upon the use of a line frequency transformer, a secondary rectifier, an output filter and a dissipative series regulating element; typical overall efficiency is 40% to 50%.

Newer designs are based upon fundamentally more efficient high frequency switching techniques. The line frequency is first rectified to DC, then inverted to high frequency AC, by a transistor switching circuit. The high frequency voltage is fed through an output transformer, rectified and filtered to produce the required DC. Regulation of the output is accomplished by controlling the pulse width of the high frequency voltage wave. This circuit technique gives much better efficiency — typically 75% to 85% — and a dramatic reduction in size — typically 4 or 5 to 1 — because of the much smaller magnetic and filter components associated with the use of high frequency.

Today, most switching power supplies use power bipolar transistors. Switching frequencies are in the range of 20kHz to 40kHz. Although a few designs operate at higher frequency, this undoubtedly means "pushing" the bipolar to the limits of its performance.

Higher operating frequency than the usual 20kHz to 40kHz range is in principle advantageous, because it offers the possibility for further reductions in size of magnetic and filter components, as well as faster response. With the availability of power MOSFETs, the switching component is no longer the frequency limiting element in the system. This new situation has generated considerable interest in where the optimum switching frequency of a power supply now lies, having due regard to the technology of the associated magnetic and filter components. Presently, there is no clear consensus. It is safe to say, however, that the optimum switching frequency is certainly greater than the 20kHz to 40kHz range of the bipolar transistor. Most probably it is at least 100kHz, and perhaps considerably higher.

It would be erroneous, however, to assume that the potential advantage of the power MOSFET is simply one of faster switching speed and higher frequency. In order to utilize all of the characteristics of the power MOSFET to best advantage, the design task is not simply one of pursuing well trodden bipolar transistor circuit techniques, albeit with higher operating frequency. Basic circuit concepts should be rethought; only then can all the potential advantages of the MOSFET be realized.

By the same token, it can be quite erroneous to labor under the notion that because power MOSFETs still are more expensive than bipolars, therefore they are not yet economically competitive. This overlooks the fact that performance advantages, or cost reductions, or both, are achieveable at the system level with these devices, that can more than compensate for their higher costs.

In this application note, we present a switching power supply using a HEXFET that operates at 100kHz — a considerably higher frequency than normally used with bipolar transistors. Attainment of this frequency actually is no particular feat for a power HEXFET, since frequencies much higher are within easy reach. A more vital objective of this application note is to demonstrate that by rethinking basic circuit concepts, results are achievable which, to many circuit designers at first sight, might seem to be unattainable. Specifically, we will show that just a single 500V-rated HEXFET can be used in a circuit that operates from a 265V line input; this compares with the usual 800V minimum rating requirement of a bipolar transistor in a single-ended circuit. We will moreover demonstrate a circuit which has the surprising capability of maintaining a constant DC output voltage over a very wide range of line input voltage — a "universal" power supply — that can operate both from the 115V line

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common in the United States, and from a 220V/240V line common in Europe, without any modification of circuitry or switching of components.

Specific Design Goals

The discussion that follows is addressed to the general circuit concepts involved in using a single power HEXFET in a wide input voltage range switching power supply. A specific implementation of the concepts described is presented; this is a circuit for a 100kHz, 100W, 5V DC power supply that employs a single 500V/3.5A-rated power HEXFET in a TO-220 package.

The performance of this power supply is summarized in Table 1. Variations from these specifications — different output power, different output voltage, different operating frequency, and so on — are obviously possible, without departing from the basic concepts.

Basic Concepts

The Conventional Forward Converter Circuit

The basic single-transistor forward converter circuit is shown in Figure 1. Idealized voltage and current waveforms that describe the operation are shown in Figure 2. During the conduction period of the transistor, current is transferred from the primary DC power source through the output transformer to the output circuit. During the OFF period of the transistor, the magnetizing current in the transformer is returned via the clamping winding to the primary DC source, resetting the flux in the transformer core, prior to the next cycle of operation.

The clamping winding usually has the same number of turns as the primary, which means that the peak voltage developed across the transistor during the OFF period is twice the primary DC supply voltage. For a nominal line input voltage of say 240V, this peak voltage would be about 720V; this is why a transistor voltage rating of at least 800V is required.

The maximum permissible conduction period of the transistor is 50% of the total cycle time. It cannot be longer than this, because there would then be insufficient time for the transformer flux to be reset during the transistor OFF period, and the transformer would be driven into saturation. A 50% duty cycle is approached for the condition of low input voltage and full load; the transistor conduction time automatically decreases from this point as the line input voltage increases or as the output load decreases, under the action of a closed-loop regulator circuit, which acts so as to maintain an essentially constant output voltage.

Modified Circuit

There is no fundamental need to clamp the peak transistor voltage to twice the supply voltage. The device voltage could be clamped to any level that is higher than the DC supply

Table 1. Performance Characteristics of 100kHz "Universal" Power Supply

Minimum Input Voltage	85V RMS, 50-400 Hz
Maximum Input Voltage	265V RMS, 50-400 Hz
Output Voltage	5V DC
Maximum Output Current	20A DC
DC Output Voltage Regulation, For All Conditions of Output Current & Input Voltage	± 0.5%
Maximum Output Ripple Voltage	50mV P-P
Transient Response for a Step Change of 10A Load Current	500mV, settling within 250μs
Full Load Efficiency	74%

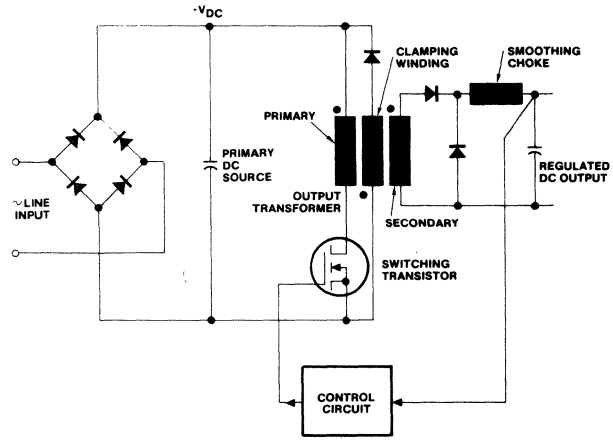


Figure 1. Basic Single-Transistor Forward Converter Circuit

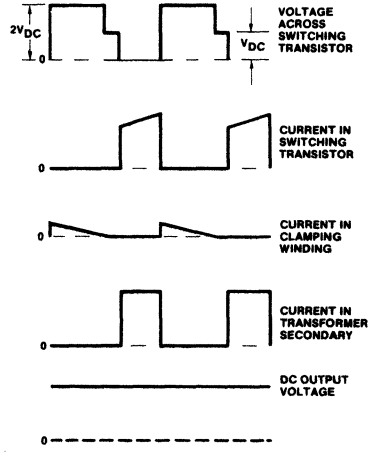


Figure 2. Idealized Waveforms for the Circuit of Figure 1

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voltage, so long as the voltage-time integral developed across the transformer during the OFF period of the transistor is equal and opposite to the voltage-time integral during the conduction period, thereby fully resetting the flux by the end of each cycle.

It is therefore possible, in principle, to reduce the peak transistor voltage, at the expense of reducing the conduction time of the transistor. The penalty is that the peak device current necessarily increases as the conduction time decreases, for a given power output and input voltage level. The idealized waveforms in Figure 3(a) illustrate operation with a 20% duty cycle; for comparison, Figure 3(b) represents operation with a 50% duty cycle, for the same power output and input voltage. The peak transistor current is greater by a factor of 2.5 for the shorter conduction period; the peak transistor voltage, on the other hand, is lower, by a factor of 1.6. This means that for a 240V input, the peak transistor voltage is reduced from the usual 720V to around 450V, permitting a 500V-rated HEXFET to be used.

With a bipolar transistor, operation with a duty cycle substantially less than 50% is undesirable. The gain of a bipolar decreases, and the device becomes increasingly difficult to use as the peak current increases. The transconductance of the power HEXFET, on the other hand, does not decrease with increasing drain current, and it is quite practical to operate a HEXFET with a short duty cycle at relatively high peak current. Higher peak current will, of course, produce greater conduction power dissipation than would be obtained in a circuit operating with a longer conduction time at correspondingly lower current. This is of little concern, however, because the HEXFET is well able to handle the "extra" dissipation; in any event, the dissipation in the switching device is substantially less than that in the output rectifiers. It is an unfortunate fact that the conduction voltage drop in these rectifiers is quite significant for a 5V output, and the circuit losses tend to be dominated by the rectifier losses.

Clamping the Drain Voltage

The drain voltage must be clamped at a level that ensures the output transformer is completely reset during the OFF period of the HEXFET. There are various ways of doing this.

A clamping winding on the output transformer — used in the conventional forward converter with a 50% duty cycle — can, in principle, still be used. The ratio of clamping turns to primary turns would, of course, no longer be 1 to 1. Taking the example considered, for a conduction duty cycle of 0.2, the peak transistor voltage must be at least 1.25X the primary DC source voltage. The clamping winding should therefore have four times the number of primary turns, as shown in Figure 4(a).

This fixes the peak transistor voltage at 1.25X the primary DC source voltage, as illustrated in Figure 4(b). A duty cycle of 0.2 would be set to occur when the line input voltage is lowest, and the output load current is highest. As the line input voltage increases, or the load current decreases, the conduction time of the transistor would decrease, under the action of a closed-loop regulator, so as to keep the DC output voltage at a constant value. The transistor clamping voltage would always be 1.25X the primary DC source voltage, regardless of what that voltage might be. The flux in the transformer is therefore reset before the end of the cycle, except at the condition of minimum line input voltage, and the peak transistor voltage is therefore generally higher than the level that is just sufficient to reset the transformer by the end of the cycle.

A transformer clamping winding, though realizable, creates some practical problems. In the example considered, the peak voltage developed between the primary and clamping windings would be five times the DC source voltage; the insulation between these windings must be sufficient to withstand this voltage. The clamping rectifier also sees a total of five times the DC source voltage and must be rated accordingly. Perhaps the biggest practical difficulty is that

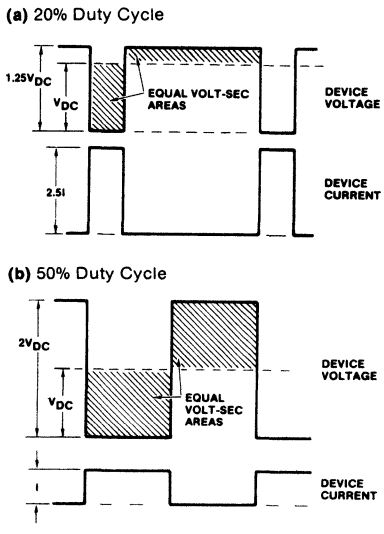


Figure 3. Idealized Waveforms of Device Voltage and Current

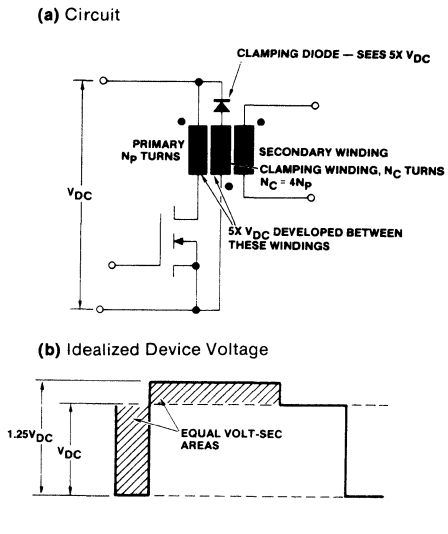


Figure 4. Use of a Transformer Clamping Winding

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substantial leakage inductance and self-capacitance inevitably appears between the primary and clamping windings, and this gives rise to superimposed high frequency oscillations on the current and voltage waves, as shown in Figure 4(c). These oscillations are difficult to eliminate.

A Different Approach

A much more satisfactory approach arises from the basic fact that for minimum voltage stress on the HEXFET, the voltage that appears across the transformer during the device OFF period should have the right amplitude to reset the flux just by the end of this period, independent of the conduction duty cycle. This principle is illustrated by the idealized waveforms in Figure 5. In this example, it is assumed that the minimum duty cycle, which occurs at maximum input voltage, is 0.15.

If this principle is followed, the voltage that appears across the transformer during the reset period by no means bears a fixed relationship to the primary DC source voltage; it increases as the DC source voltage decreases and is inversely proportional to (1-D), where D is the duty cycle. Thus, a transformer clamping winding, in principle, will not do the job.

If the required clamping circuit could be devised, two benefits — in addition to the elimination of the transformer clamping winding — would be realized. First, as already mentioned, the voltage across the HEXFET would be minimized. Second, there would not be a maximum permissible conduction period for the transistor — as there is with a transformer clamping winding — above which the transistor OFF period becomes too short for the transformer flux to be reset. There would therefore no longer be the same minimum line voltage below which the circuit cannot operate.

This is very interesting; it means, for example, that if the circuit is designed so that it operates with a rather short duty cycle, say 0.15 at a line voltage around 265V, then the circuit could be made to stay in regulation and to deliver the same DC output voltage when the line input voltage is as low as say 80V, at which point the conduction duty cycle would be about 0.5. This example is actually represented by the idealized waveforms in Figure 5.

Even this would not theoretically be the limiting range of operation; as a practical matter, however, most integrated circuits that are intended for controlling power supplies of this type have a maximum duty cycle of 0.5. At all events, if we design the circuit according to these principles, we will have a "universal" power supply, capable of delivering the same regulated DC output voltage both from 115V and 220V/240V line inputs, with no modification of circuitry, or switching of components.

A Capacitor-Resistor-Diode Clamp

The desired clamping circuit can be realized in a surprisingly simple manner. The circuit is illustrated in Figure 6. The capacitor C is a "reservoir" capacitor which charges to an essentially steady level of voltage — the necessary transformer resetting voltage. The resistor R dissipates the energy delivered to the clamping circuit from the transformer. Unlike the transformer winding, which returns the energy stored in the transformer to the primary DC source, this is a dissipative clamp.

(c) Practical Oscillograms

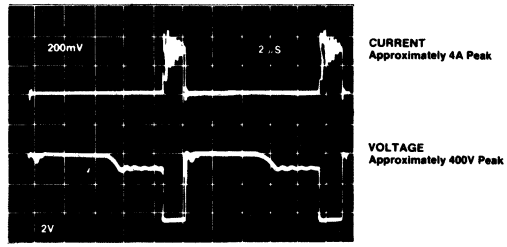


Figure 4. Use of a Transformer Clamping Winding (continued)

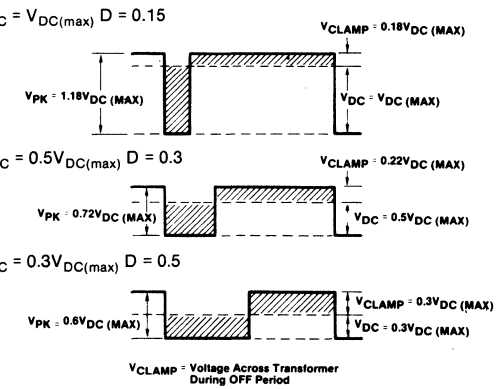


Figure 5. Idealized Waveforms Illustrating Operation when Device Voltage During OFF Period Always has just Correct Amplitude to Reset Transformer by End of this Period.

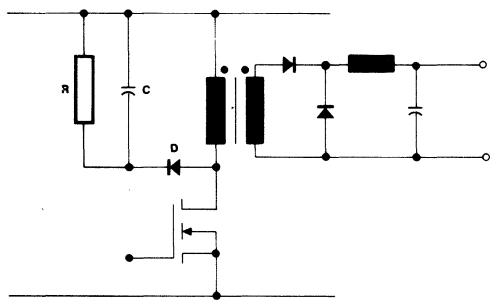


Figure 6. Capacitor-Resistor-Diode Clamp

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From a practical point of view, because of the possibility for operating at high frequency, the transformer can be designed so that the power dissipation in the clamp is kept to a quite acceptable level. In the specific circuit described, the power dissipation in the clamping circuit is quite minimal, and ranges between 2% and 3% of the output power.

The inherent action of this simple clamp can be arranged to be such as to adjust the steady-state voltage across the capacitor to the level required to reset the transformer just by the end of the OFF period, regardless of the level of input voltage. This can be seen by assuming for the moment that the voltage across the capacitor is insufficient to reset the transformer. In this event, the magnetizing current, and the voltage across the capacitor, "ratchet up" during succeeding cycles, until the voltage does become sufficient, at which point an equilibrium condition is attained. This action is illustrated by the idealized waveforms in Figure 7.

This clamp thus provides the required voltage to keep the transformer voltage-time integral within balance, independent (within limits) of the value of the capacitor C or the resistor R. Care must be taken, however, to size the resistor so that minimum energy is stored in the transformer — that is, so that the magnetizing current does not "ratchet up" more than is necessary — otherwise, the losses will be excessive. Assuming that the magnetizing current will always be continuous, and thus that the HEXFET voltage will always be minimized, the "best" design will result from sizing the resistor so that the magnetizing current is just continuous at the highest input voltage level.

The general relationship between the voltage across the clamping resistor, V_R, and the primary DC source voltage, V_{DC}, for a given conduction duty cycle, D, with continuous transformer magnetizing current is:

$$V_R = \frac{D\,V_{DC}}{(1-D)}$$

The required value of the resistor R is therefore given by:

$$R = \frac{\left[\frac{D_{(min)}\,V_{DC(max)}}{1-D_{(min)}}\right]^2}{\left[\tfrac{1}{2}\,L_{(mag)}\,I^2_{(mag)PK} + \tfrac{1}{2}\,L_S\,I^2_{LPK}\right] f}$$

Where $D_{(min)}$ is the minimum full load duty cycle, (obtained when $V_{DC} = V_{DC(max)}$).

$L_{(mag)}$ is the transformer magnetizing inductance.

$I_{(mag)PK}$ is the peak magnetizing current for just-continuous magnetizing current.

L_S is the leakage inductance of the transformer, referred to the primary.

I_{LPK} is the peak full load current in the transformer primary.

f is the frequency.

The ratio of the voltage V_R across R at any other lower value of primary DC voltage V_{DC} is:

$$\frac{V_R}{V_{R(min)}} = \frac{1 - D_{(min)}}{1 - \left[\frac{V_{DC(max)}}{V_{DC}} \cdot D_{(min)}\right]}$$

Considering a specific example, if $D_{(min)} = 0.15$ and $\frac{V_{DC(max)}}{V_{DC}} = 0.3$, then:

$$\frac{V_R}{V_{R(min)}} = \frac{1 - 0.15}{1 - [(0.15)3]} = 1.55$$

The losses in the clamping resistor at 1/3 of the maximum input voltage would then be $1.55^2 = 2.4$X the losses at maximum input voltage.

The maximum power dissipation in the clamp — obtained at the lowest input voltage — can be reduced, at the expense of a small increase in the maximum voltage developed across the HEXFET — obtained at the highest input voltage — by sizing the resistor R so that the magnetizing current becomes discontinuous at some intermediate value of line input voltage. As the input voltage increases above this level, the peak magnetizing current stays constant, while the magnetizing current waveform becomes progressively more discontinuous, and the voltage across the clamp circuit stays constant, because (for a given load current) the energy stored in the transformer is constant. Below the critical intermediate level of line voltage, the transformer magnetizing current becomes continuous, and the clamping voltage rises as the input voltage decreases.

As an example of this design approach, assume that the clamp resistor is sized to give just-continuous conduction at 45% of maximum line voltage. If the minimum duty cycle at maximum input voltage is 0.15, then at maximum input voltage, the peak voltage developed across the transistor will be 1.23, instead of 1.18 times the primary DC source voltage. For a total range of input voltage variation of 3 to 1, the maximum duty cycle would be 0.45, and the ratio of the maximum to minimum voltage across the clamp resistor would be:

$$\frac{V_{R(max)}}{V_{R(min)}} = \frac{1 - (0.15/0.45)}{1 - 0.45} = 1.22$$

The range of maximum to minimum power loss in the clamp resistor at full output power would then be $1.22^2 = 1.49$. Figure 8 illustrates this specific design example.

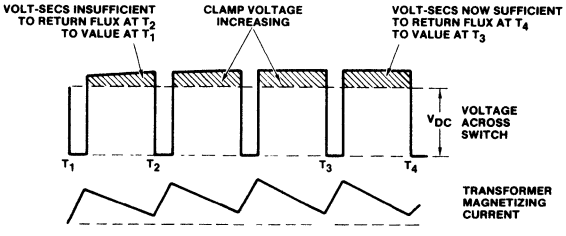


Figure 7. Idealized Waveforms Showing Transformer Magnetizing Current "Ratcheting Up" to Create Sufficient Clamp Voltage to Maintain Equilibrium

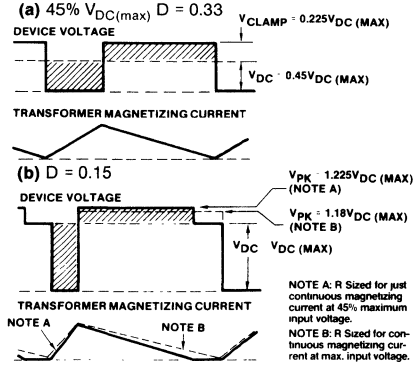


Figure 8. Idealized Waveforms Showing Operation when Clamp Resistor is Sized to Give just Continuous Magnetizing Current at 45% Maximum Input Voltage

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Practical Circuit

Figure 9 shows a complete diagram for a 100W, 100kHz, 5V DC output circuit, which conforms with the performance specifications shown in Table 1. Component details are listed in Table 2.

Table 2. List of Components for Figure 9

Q1	IRF830 HEXFET
IC	Silicon General 3526
B1	IR 3KCB80
C1	500μF, 450V wkg.
C2	0.68μF, 100V
C3	4X 150μF, 6V
C4	22μF, 16V
C5	0.5μF, 25V wkg.
C6	10nF
C7	910pF
C8	0.0068 mfd.
C9	0.005μF
C10	0.1μF
C11	22μF, 25V
R1	1.5K (3X500Ω, 5W)
R2	12Ω 1/4W
R3	6.8kΩ 1/4W
R4	10Ω
R5	12kΩ 1/4W
R6	100Ω potentiometer
R7	33Ω 1/4W
R8	560Ω 1/4W
D1	20FQ030
D2	60HQ100
D3	IR 40SL6
Z1	1N4112 zener diode
Z2	1N4112 zener diode
Z3	4X 1N987B zener diodes in series
L1	Pan Magnetics International E-2481 (Core Arnold A-930157-2, 16 turns, 2 in parallel #14)
T1	Pan Magnetics International E-2478 (Core TDK 26/20. Primary: 20 turns, 3 in parallel #32; Secondary: 3 turns, 0.3mm x 0.8cm copper strip)
T2	Pan Magnetics International E-2479 (Core TDK H5B2T10-20-5. Primary: 6 turns #24; Secondary: 6 turns #24)
T3	Pan Magnetics International E-2480 (Core TDK H5B2T5-10-2.5. Primary: 1 turn; Secondary: 100 turns #32)

Performance Measurements

Oscillograms for various operating conditions are shown in Figures 10 through 20. Figure 10(a) and (b) shows oscillograms of drain voltage and drain current for output currents of 20A and 5A, respectively, with a 85V input. Figure 11(a) and (b) shows corresponding waveforms with 265V input.

Figure 12(a) and (b) shows oscillograms of HEXFET voltage and current during turn-ON for output currents of 20A and 5A, respectively, with 85V input. Note that although the voltage across the HEXFET falls in about 75ns, the rise time of the HEXFET current with a 20A output is over 300ns. This rather long rise time is due to leakage inductance, primarily of the transformer, and does not reflect the switching speed of the HEXFET. Figure 13(a) and (b) shows corresponding oscillograms for the turn-on interval, with 265V input. The rise time of the current is faster, because the higher voltage produces an increased rate-of-rise of current in the circuit inductance.

Figure 14(a) and (b) shows oscillograms of HEXFET voltage and current during turn-OFF for output currents of 20A and 5A, respectively, with 85V input. Transformer leakage inductance does not significantly effect the fall time of the current, because the current in the leakage inductance when switching OFF is diverted into the clamping circuit, and the slow fall time is not "seen" by the HEXFET. Figure 15(a) and (b) shows corresponding oscillograms during turn-OFF, with 265V input.

In Figures 11 and 15, it can be seen that with the maximum line input voltage of 265V, the peak voltage developed across the HEXFET at full load, including the voltage "spike" when switching OFF, is about 440V. This is comfortably within the 500V rating of the device.

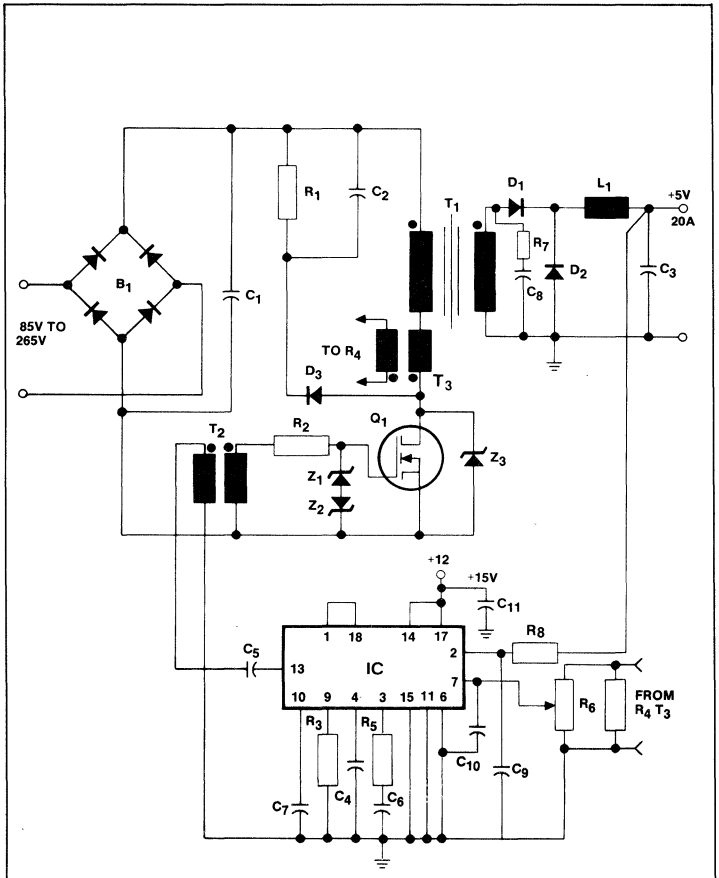
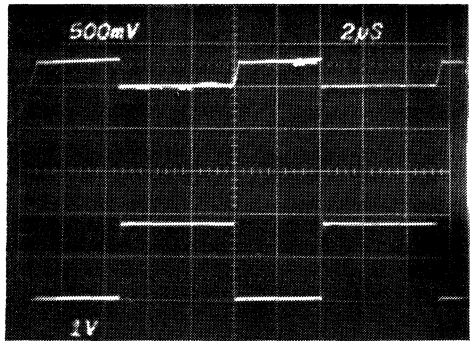
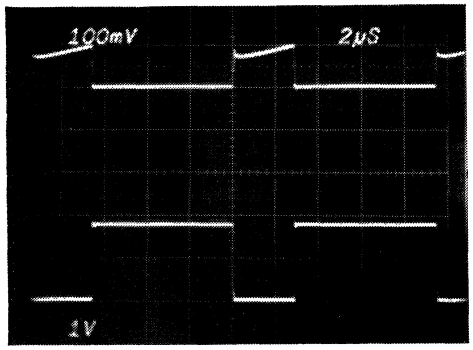


Figure 9. Circuit Diagram of 100kHz, 100W Wide Range Power Supply

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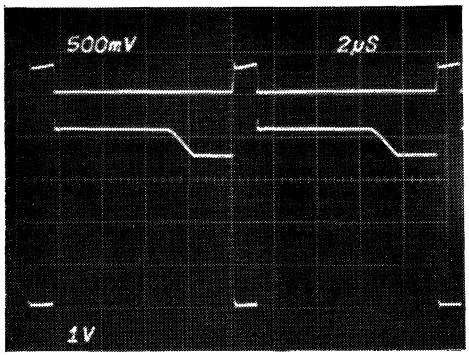


Upper Trace: Drain Current: 5A/division, 2μs/division
Lower Trace: Drain Voltage: 100V/division; Output Current: 20A
(a)

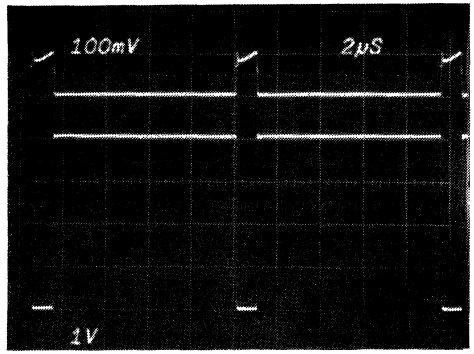


Upper Trace: Drain Current: 1A/division, 2μs/division
Lower Trace: Drain Voltage: 100V/division; Output Current: 5A
(b)

Figure 10. Oscillograms of Drain Voltage and Current, 85V Line Input

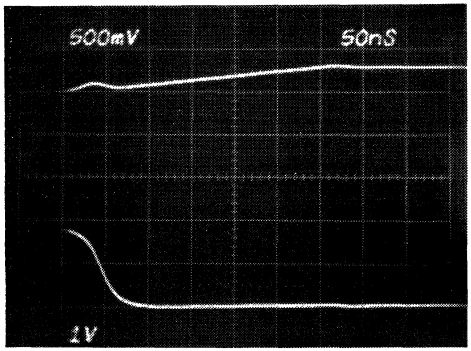


Upper Trace: Drain Current: 5A/division, 2μs/division
Lower Trace: Drain Voltage: 100V/division; Output Current: 20A
(a)

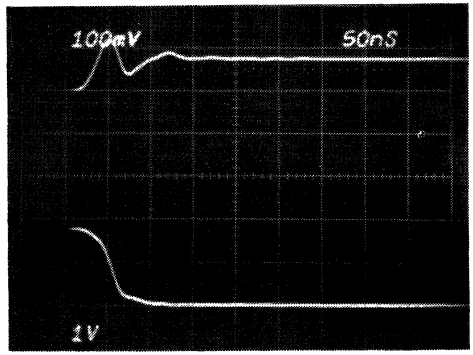


Upper Trace: Drain Current: 1A/division, 2μs/division
Lower Trace: Drain Voltage: 100V/division; Output Current: 5A
(b)

Figure 11. Oscillograms of Drain Voltage and Current, 265V Line Input



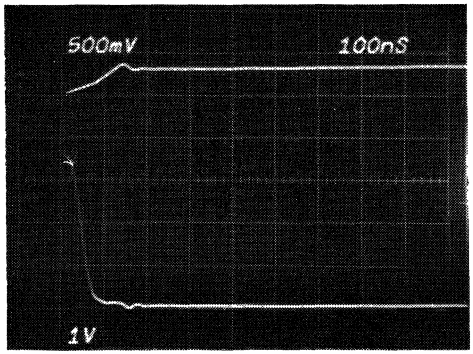
Upper Trace: Drain Current: 5A/division, 50ns/division
Lower Trace: Drain Voltage: 100V/division; Output Current: 20A
(a)



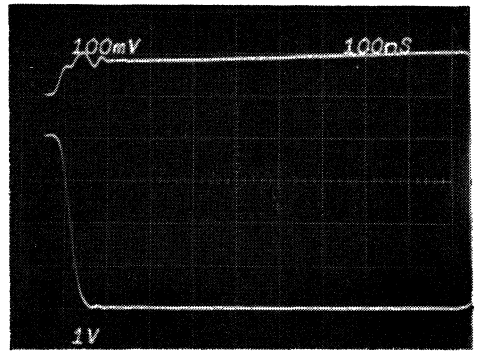
Upper Trace: Drain Current: 1A/division, 50ns/division
Lower Trace: Drain Voltage: 100V/division; Output Current: 5A
(b)

Figure 12. Oscillograms of Drain Voltage and Current During Turn-On, 85V Line Input

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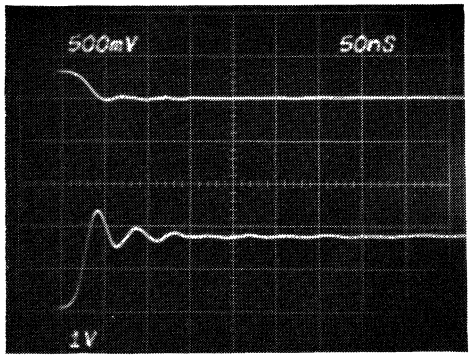


Upper Trace: Drain Current: 5A/division 100ns/division (a)
Lower Trace: Drain Voltage: 100V/division
Output Current: 20A

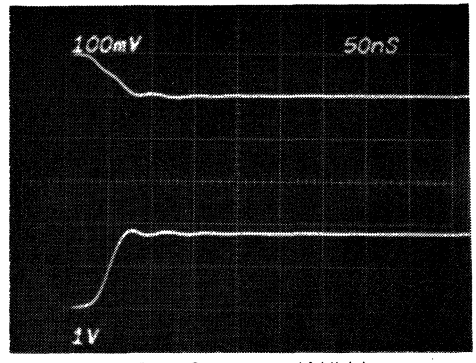


Upper Trace: Drain Current: 1A/division 100ns/division (b)
Lower Trace: Drain Voltage: 100V/division
Output Current: 5A

Figure 13. Oscillograms of Drain Voltage and Current During Turn-On, 265V Line Input

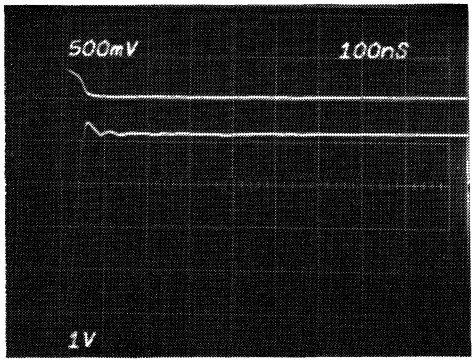


Upper Trace: Drain Current: 5A/division 50ns/division (a)
Lower Trace: Drain Voltage: 100V/division
Output Current: 20A

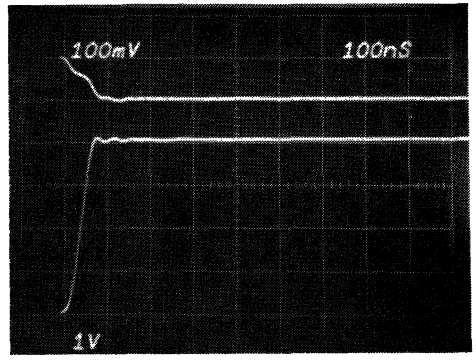


Upper Trace: Drain Current: 1A/division 50ns/division (b)
Lower Trace: Drain Voltage: 100V/division
Output Current: 5A

Figure 14. Oscillograms of Drain Current and Voltage During Turn-Off, 85V Line Input



Upper Trace: Drain Current: 5A/division 100ns/division (a)
Lower Trace: Drain Voltage: 100V/division
Output Current: 20A



Upper Trace: Drain Current: 1A/division 100ns/division (b)
Lower Trace: Drain Voltage: 100V/division
Output Current: 5A

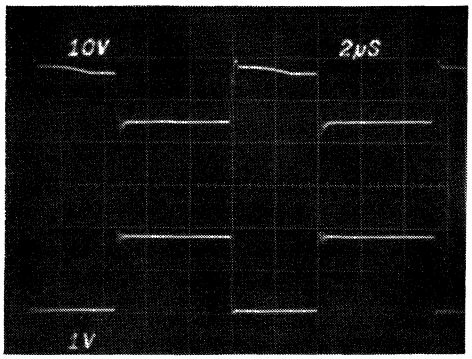
Figure 15. Oscillograms of Drain Current and Voltage During Turn-Off, 265V Line Input

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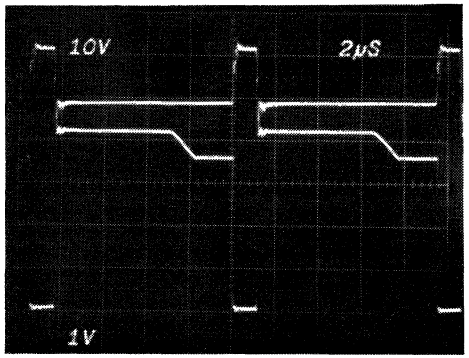
Figure 16(a) and (b) shows oscillograms of the gate-to-source and drain-to-source voltages at line input voltages of 85V and 265V, respectively, with the full load output current of 20A, while Figure 17 shows oscillograms of voltage across the output rectifiers, D_1 and D_2, with 5A output current, for input voltages of 85V and 265V. Note that with 265V input, the voltage across the output freewheeling rectifier, D_2, including the transient commutation spike, is about 75V. An experimental 20A, 100V Schottky rectifier was used in this position. At the time of writing, this particular device is not yet commercially available; the 60A, 100V-rated 60HQ100 Schottky rectifier, though really oversized, is listed in Table 2, since it is commercially available. Alternatively, of course, an appropriate 100V fast recovery rectifier, such as the 40HFL100S02, could be employed. Note that the peak voltage across rectifier D_1, including the commutation "spike", is less than 20V, which means that a 30V-rated Schottky is adequate.

Figure 18(a) and (b) shows the transient response of the output voltage to a step change in output current from 10A to 20A, and vice versa, with 85V input, while Figure 19(a) and (b) shows corresponding oscillograms for 265V input.

Figure 20(a) and (b) shows oscillograms of drain current and drain voltage with a short circuit applied at the output, at input voltages of 85V and 265V, respectively. With 85V input, the peak HEXFET current is regulated to about 3A, by the automatic current limiting facility built into the control circuit, and the corresponding DC output current is just over 20A. With 265V input, however, the peak HEXFET current is about 7A, the short circuit DC output current is about 55A, and the peak HEXFET voltage is almost 500V. The lack of effective current limiting under this condition is due to the fact that the control circuit has a minimum ON conduction time of about 0.8 microseconds, and this is not short enough to keep the current under control under short circuit conditions.



Upper Trace: Gate-Source Voltage: 10V/division 2μs/division
Lower Trace: Drain Voltage: 100V/division
Line Input: 85V
(a)



Upper Trace: Gate-Source Voltage: 10V/division 2μs/division
Lower Trace: Drain Voltage: 100V/division
Line Input: 265V
(b)

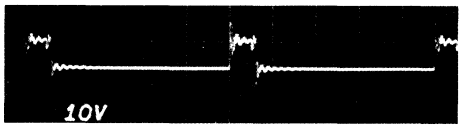
Figure 16. Oscillograms of Gate-Source Voltage and Drain Voltage, 20A Output



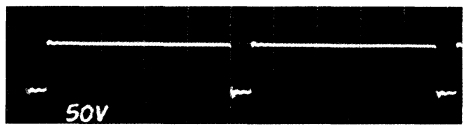
Voltage across D1: 10V/division 2μs/division
Input: 85V
(a)



Voltage across D2: 20V/division 2μs/division
Input: 85V
(b)



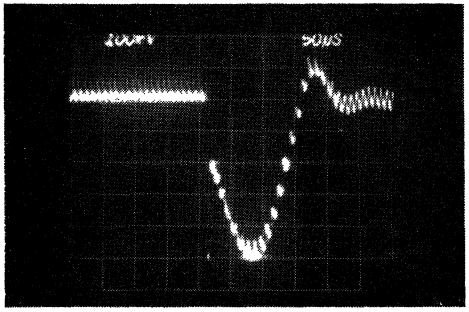
Voltage across D1: 10V/division 2μs/division
Input: 265V
(c)



Voltage across D2: 50V/division 2μs/division
Input: 265V
(d)

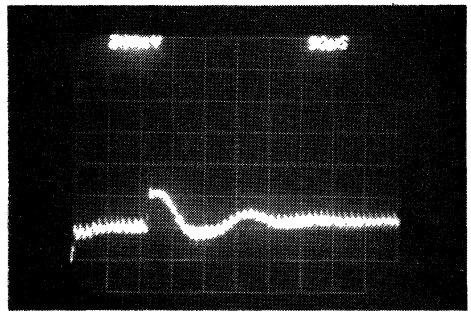
Figure 17. Oscillograms of Voltage Across Output Rectifiers D1 and D2, 5A Output Current

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Output Voltage: 100mV/division
50μs/division
Step Load
Change: 10A to 20A

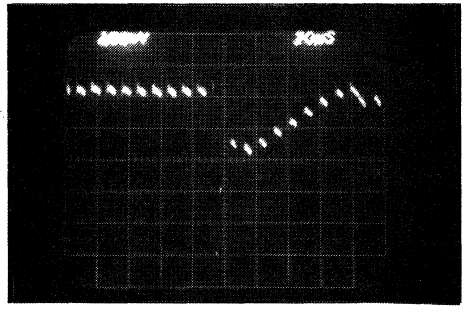
(a)



Output Voltage: 100mV/division
50μs/division
Step Load
Change: 20A to 10A

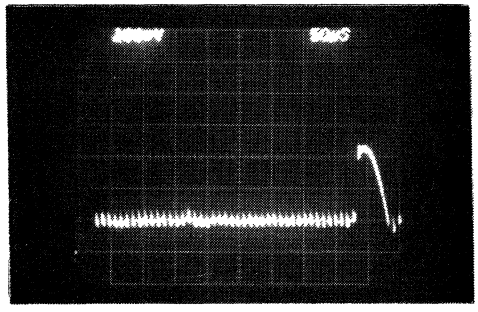
(b)

Figure 18. Oscillograms of DC Output Voltage During Step Change of Output Load Current, 85V Line Input



Output Voltage: 100mV/division
50μs/division
Step Load
Change: 10A to 20A

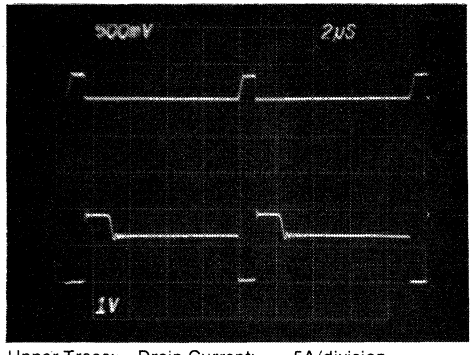
(a)



Output Voltage: 100mV/division
50μs/division
Step Load
Change: 20A to 10A

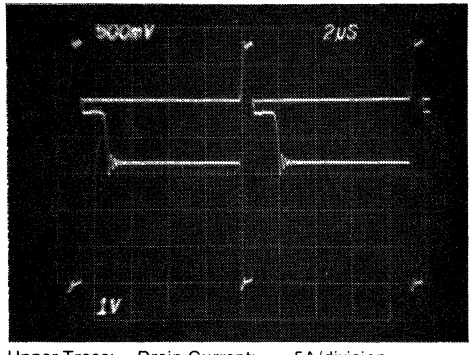
(b)

Figure 19. Oscillograms of DC Output Voltage During Step Change of Output Load Current, 265V Line Input



Upper Trace: Drain Current: 5A/division
2μs/division
Lower Trace: Drain Voltage: 100V/division
Line Input: 85V

(a)



Upper Trace: Drain Current: 5A/division
2μs/division
Lower Trace: Drain Voltage: 100V/division
Line Input: 265V

(b)

Figure 20. Oscillograms of Drain Voltage and Current with Short Circuit at Output

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Attention should be paid to this point in a production design. A solution could be to add a circuit that clamps the "soft start" terminal of the control circuit to ground when the output current exceeds a predetermined level, thereby switching OFF the power supply. Resetting would be done manually once the fault condition has cleared. While this design aspect certainly needs consideration, it is of interest to see that the circuit continues to operate satisfactorily, albeit under high stress, with a short circuit output current close to 3X the rated value.

Generally, our objective has been to demonstrate the feasibility of the basic circuit concepts described, and we have not paid particular attention to design details that can be handled in a rather routine manner, according to the particular requirements of the designer. In this vein, we have taken for granted that 15V DC is available to supply the control circuit. This auxiliary DC supply could be derived from a small line frequency transformer with a rectifier and a relatively coarse voltage regulator. A 12V to 16V range of regulation would be quite satisfactory. Current consumption of the control circuit is 50mA maximum, which equates to a total power dissipation in this auxiliary power supply circuit of a little over 2W at maximum input voltage, and less than 1W at minimum input voltage.

Power Losses and Overall Efficiency

Table 3 shows the power dissipation in the various individual components of the circuit, as well as the overall efficiency, for various levels of output power, at input voltages of 90V and 260V. This data has been obtained through a combination of measurement and estimation.

The DC power delivered from the input bridge rectifier, and the DC output power, are measured directly, and the overall loss in the intervening circuitry is derived from the difference of these two measurements. The loss in the input rectifier, the HEXFET, the output rectifier, and an assumed auxiliary DC control power supply, fed from the input line through a transformer (as discussed above), are estimated individually from a knowledge of the operating voltage and currents for these components. The loss in the clamp circuit is calculated from the measured voltage across the clamp resistor; and the power loss in the output transformer and filter choke is taken as the difference between the total power dissipation, and the sum of the losses in the other components.

The overall full load efficiency arrived at in this way is 76% at 265V input, and 74% at 85V input. It should be added that an EMI filter, required in a practical system, but not included here, would reduce the overall efficiency slightly from the values shown here.

"Wide Range" Versus "Dual Range"

A point of contention may have arisen in the mind of the astute reader. This is that it is a usual design requirement to maintain rated DC output voltage during loss of the input line voltage for one cycle. In order to do this, the input reservoir capacitor, C_1 in Figure 9, must be sized to supply the required energy to the output, while its voltage must not deplete below a level at which control of the output voltage can be maintained. If this capacitor is sized to supply the required energy when operating from a 115V input, as it should be, it will then be grossly oversized for operation from a 240V input, and most likely will be larger and more expensive than the capacitance required by a conventional power supply.

A conventional "dual voltage" power supply can operate either from 115V or 240V input, by means of switching from a voltage doubler circuit when operating at 115V, to a full rectifier bridge circuit when operating at 240V, with the two "doubler" capacitors then connected directly in series across the output of the bridge. Substantially the same primary DC source voltage is thereby maintained for both AC input voltage levels.

Taking the specific case of a 100W supply, the choice would then typically be between the single 500μF 450V capacitor, shown in Figure 21(a), for the wide range power supply, versus two 600μF 200V capacitors, shown in Figure 21(b), for the "dual voltage" supply. The single capacitor in Figure 21(a) has approximately 30% more volume than the combined volume of the two capacitors shown in Figure 20(b); the cost differential is about 11%, or $0.60 extra for the capacitor for the wide range power supply. This could be more than compensated for by the fact that the additional complication of switching from a doubler to a bridge configuration is eliminated, to say nothing of the functional convenience of not having to make any adjustments when operating from 115V or 240V input.

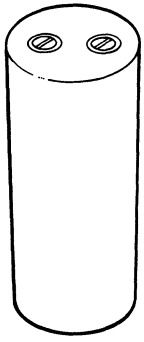
A quite different aspect is that if the wide regulation capability of the circuit is utilized only under the short-term condition of loss of input line voltage for one cycle, then a drastic reduction in the size of the input reservoir capacitance can be made. This is because the voltage across this capacitor can then be allowed to "drift" all the way from, say, 310V down to 120V, during the one-cycle "outage" period.

Table 3. Power Losses and Overall Efficiency Under Various Operating Conditions

Line Input Voltage V	DC Output Voltage V	Power Output W	Total Power Loss W	Estimated Power Loss in Input Rectifier W	Estimated Power Loss in HEXFET W	Power Loss in Clamp Circuit W	Estimated Power Loss in Transformer and Filter Choke W	Estimated Power Loss in Output Rectifier W	Estimated Power Loss in Control Circuit W	Overall Efficiency %
90	5.0	97.26	34.09	4	8.0	2.99	2.7	15.5	0.9	74
	5.0	73.11	24.4	3	4.6	2.60	2.4	10.9	0.9	75
	5.0	48.81	15.94	2	2.3	2.24	1.5	7.0	0.9	75
	5.0	24.40	9.3	1	0.8	2.02	1.28	3.3	0.9	72
260	5.0	96.96	30.22	1.3	5.4	2.02	3.3	15.5	2.7	76
	5.0	72.81	22.74	1.0	3.7	1.54	2.9	10.9	2.7	76
	5.0	48.66	16.69	0.7	2.3	1.29	2.7	7.0	2.7	74
	5.0	24.35	10.98	0.4	1.1	1.18	2.3	3.3	2.7	69

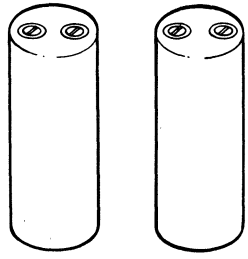
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Capacitor required for wide range power supply when designed to operate from 115V and 240V inputs without modification.



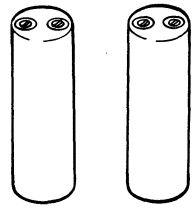
Capacitor Required: 1 X 500μF, 450V
Total Volume: 14.72 cubic inch
Typical Cost: $6.50

Capacitors required for power supply with facility for switching from "voltage doubler" to bridge configurations for 115V and 240V inputs, respectively.



Capacitor Required: 2 X 600μF, 200V
Total Volume: 11.49 cubic inch
Typical Cost: $5.88

Capacitors required for wide range power supply when used with facility for switching from "voltage doubler" to bridge configurations for 115V and 240V inputs, respectively.



Capacitor Required: 2 X 200μF, 200V
Total Volume: 5.23 cubic inch
Typical Cost: $2.64

Figure 21. Input Reservoir Capacitors Required for Various Alternative Designs

With this design approach, it would be necessary to switch from a voltage doubler circuit to a bridge circuit when operating from 115V and 240V inputs, respectively, but the size of the required input capacitors would be reduced as shown in Figure 21(c). The volume of these capacitors is just under 50% of the volume of the capacitors required for a conventional "dual voltage" power supply, and the cost is approximately 45% — an absolute saving in the region of $3.00.

Conclusions

In order to get the most out of a power HEXFET, it is necessary to rethink basic concepts, and to design the circuitry to take maximum advantage of the special operating features of the device. An illustration of this basic precept is the 100kHz, 100W "universal" switching power supply described in this article. The circuit uses a single 500V-rated HEXFET to provide a regulated 5V DC output, over the entire range of line input voltage from 85V to 265V. □

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A Chopper for Motor Speed Control Using Parallel Connected Power HEXFETs®

By S. CLEMENTE, B. PELLY

Summary

Today's MOSFETs are rated at currents as high as 28A continuous and 70A peak, at 100V. They are easily parallelable for higher current operation, and are attractive candidates for controlling the speed of electric motors at currents up to several hundred amperes.

This application note demonstrates an experimental DC to DC chopper circuit using parallel connected power MOSFETs, for speed control of a separately excited DC motor. The circuit operates from a 48V battery, and provides "two-quadrant" operation, with maximum motoring and regenerating currents of 200A and 140A, respectively.

Introduction

Efficient speed control of DC motors operating from DC supplies is today accomplished with switching chopper circuits using forced commutated thyristors or bipolar transistors. Battery operated systems rated at hundreds of amperes are in common use in forklift truck and electrical vehicle controllers. Larger thyristor choppers rated at thousands of amperes, at DC voltages up to 1500V, are in use in high power railway traction applications.

In this type of application power MOSFETs would offer some advantages, like very high gain, very rugged performance, and very fast switching speed. The power MOSFET lends itself readily to paralleling (providing the proper precautions are observed), and a power MOSFET chopper operating at currents of several hundred amperes is technically within grasp.

In this application note, we demonstrate the technical feasibility of a chopper circuit using parallel connected HEXFETs to provide a 200A, 48V output for motor speed control. A particular feature of the circuit is its facility for providing electrical braking of the motor by feeding electrical energy back to the DC source. This is accomplished through the use of the integral body-drain diode of the HEXFET, which acts as a circuit component in its own right, and provides the "freewheeling" and "flyback" functions for the "motoring" and "regenerating" modes.

The Power HEXFET

The basic structure of a HEXFET is illustrated in Figure 1, and the electrical symbol is shown in Figure 2. Current flows from the drain region vertically through the silicon, then horizontally through the channel, then vertically out through the source.

The HEXFET design is based upon vertical D-MOS technology. The closed hexagonal cellular structure with the buried silicon gate allow for optimum utilization of silicon, and yield a rugged, highly reliable device.

A feature of the HEXFET (actually, of all power MOSFETs) is that it inherently has built into it an integral reverse "body-drain" diode. The full electrical symbol for the power MOSFET includes the reverse parallel rectifier shown dashed in Figure 2.

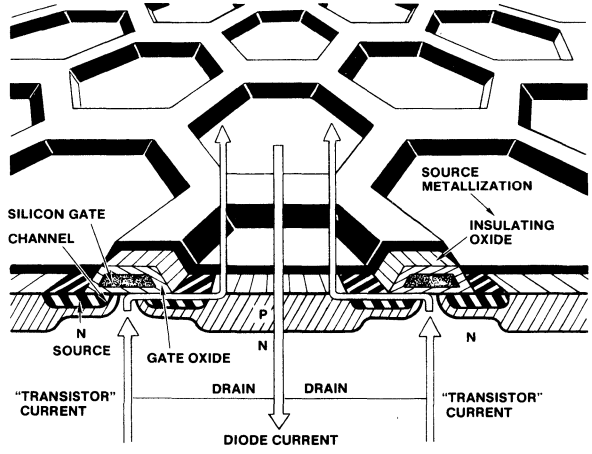


Figure 1. Basic HEXFET Structure

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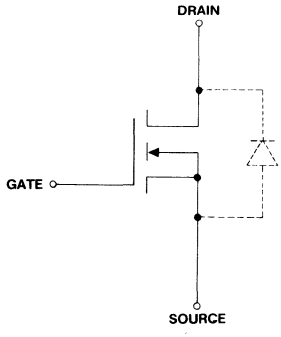


Figure 2. Electrical Symbol for Power HEXFET (MOSFET) including the Body-Drain Diode

The existence of this integral reverse rectifier is explained by reference to Figure 1. Current is free to flow through the middle of each source cell across a forward-biased P-N junction, and out of the drain. The path for this "reverse" current flow is at least comparable in cross-section to that of the "forward" current "transistor" channel. Far from being an inconsequential "parasitic" component, the integral reverse body-drain diode is therefore a real circuit element, with a current handling capability as high as that of the transistor.

The integral reverse body-drain diode may or may not be important in a practical circuit. In some circuits, it is irrelevant, because the circuit operation is such that the voltage across the switching device never changes polarity, and the forward conduction characteristic of the body-drain diode never comes into play. This is the case, for example, in a simple DC to DC chopper circuit for motor control which is not configured for regenerative energy flow, and in which the motor voltage never exceeds the source voltage.

A DC to DC chopper circuit for motor speed control that provides a regenerative braking capability would, however, require rectifiers to be connected across the switching devices, and in this case, the reverse body-drain diode of the HEXFET can be used for this purpose, and, in fact, eliminates the need for additional discrete rectifiers.

Potential Advantages of Power HEXFETs for Motor Drives

The power HEXFET has several unique features which make it a potentially attractive switching component for a chopper drive. These features are briefly discussed below:

High Gain

The HEXFET is a voltage driven device. The gate is isolated electrically from the source by a layer of silicon oxide. The gate draws only minute leakage current, in the order of nanoamperes, and the DC gain — in the conventional sense used for a bipolar transistor is rather meaningless. A more useful parameter is the transconductance. This is the change of drain current brought about by a 1V change of voltage on the gate. The transconductance of the IRF150 HEXFET is typically 10 amps per volt.

Another important advantage is that, unlike the bipolar transistor, the gain of the HEXFET does not decrease with increasing current. This means that the HEXFET is able to handle high peak current, without showing the bipolar transistor's tendency to "pull out of saturation." Typical relationships between gate-to-source voltage and drain current are shown in Figure 3.

Because the gain of the HEXFET is very high, the drive circuitry required is relatively simple. It should be clearly recognized, however, that although the gate consumes virtually no current under "steady" conditions, this is not so under transitional switching conditions. The gate-to-source and gate-to-drain self-capacitances must be charged and discharged appropriately to obtain the desired switching speed, and the drive circuit must have a sufficiently low output impedance to supply the required charging and discharging current. Even once these requirements have been catered for, the fact remains that the drive circuitry required for a HEXFET is considerably simpler than that required for a bipolar transistor.

Ruggedness

One of the outstanding features of the HEXFET is that it does not display the second breakdown phenomenon of the bipolar transistor, and as a result, it has an extremely rugged switching performance.

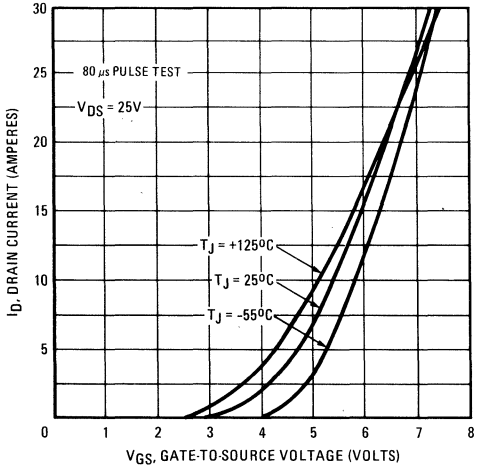


Figure 3. Transfer Characteristics IRF150

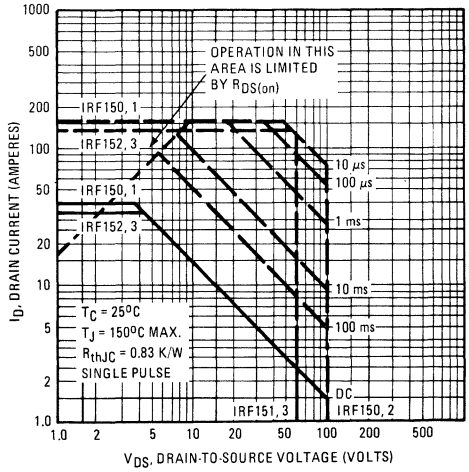


Figure 4. Maximum Safe Operating Area IRF150

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A simple physical explanation accounts for this superiority. If localized, potentially destructive heating occurs within a HEXFET, the carrier mobility in that area decreases. As a result, the device has a positive temperature coefficient and acts in a self-protective manner by forcing currents to be uniformly distributed throughout the silicon. The safe operating area of the IRF150 HEXFET is shown as an example in Figure 4. Note that the safe operating area for 10μs is fully rectangular; this means, in principle, that it is possible to switch 70A at 100V in this device. As a matter of good design practice, of course, one would not operate at this limit.

The absence of second breakdown is, of course, important for this type of application.

Ease of Paralleling

Power HEXFETs are, in principle, easy to parallel, because the positive temperature coefficient forces current sharing among parallel devices. They therefore lend themselves well to the construction of a chopper rated at several hundred amperes, and the problems of paralleling will be much less than those associated with bipolar transistors.

A Basic HEXFET Two-Quadrant Chopper Circuit

Figure 5 shows the basic circuit of a DC to DC chopper that provides continuous speed control in the "motoring" mode of operation (i.e., with the motor receiving power from the DC source), and also provides the facility for the motor to return regenerative energy to the DC source, over the whole speed range. Idealized waveforms that describe the operation are shown in Figure 6, while Figure 7 defines the two operating quadrants of the circuit developed.

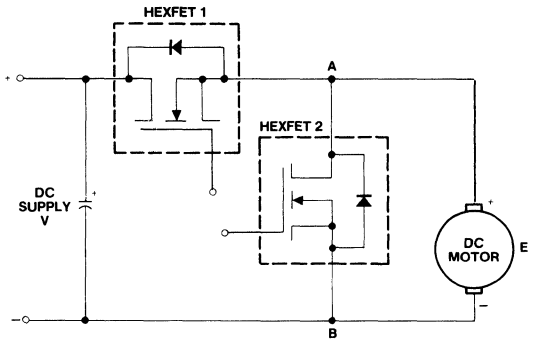


Figure 5. Basic Two Quadrant Chopper Circuit Using HEXFETs

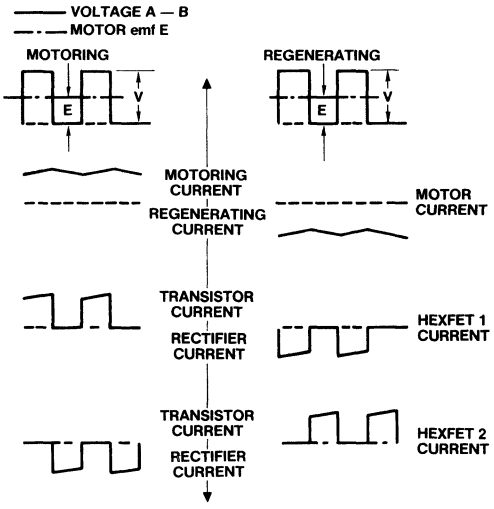


Figure 6. Idealized Operating Waveforms for Figure 5

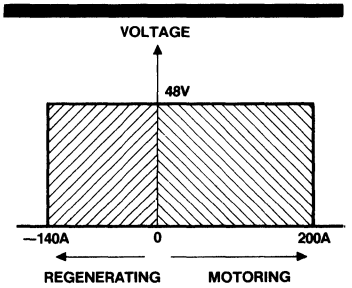


Figure 7. Motoring and Regenerating Operating Quadrants for the Circuit of Figure 5

In the "motoring" mode of operation, HEXFET 1 is switched ON and OFF, at an appropriate repetition rate, and provides control of the average voltage applied to the motor. HEXFET 2 is OFF, but its integral reverse body-drain diode acts as the conventional freewheeling rectifier and carries the freewheeling motor current during the periods when HEXFET 1 is OFF. When the motor is required to act as a generator and return energy to the DC source, HEXFET 2 is chopped ON and OFF, and controls the current fed back from the motor to the supply. In this operating mode, HEXFET 1 is OFF, but its integral reverse rectifier carries the motor current back to the DC source during the intervals when HEXFET 2 is OFF.

In order for the motor to "regenerate," it is necessary for it to have either a shunt or a separately excited field. A series-connected field is not feasible, unless the connections to it are reversed for the regenerative mode of operation, which is not practically convenient.

The major objectives of this application note are to demonstrate the feasibility of operating a group of parallel connected HEXFETs at currents in the order of hundreds of amperes, and of using the reverse body-drain diode of the HEXFET as a circuit element in its own right, in the basic two quadrant chopper circuits shown in Figure 5.

To achieve these objectives, it is

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necessary to consider certain detailed aspects of the operation of the HEXFETs. We do this in the following section.

Use of the HEXFET's Body-Drain Diode

An important consideration when using the HEXFET's integral body-drain diode is its reverse recovery characteristic. This rectifier is a conventional P-N junction device, and therefore it exhibits a classical reverse recovery charge. That is to say, when the rectifier switches OFF, the current through it reverses for a short period, as illustrated in Figure 8.

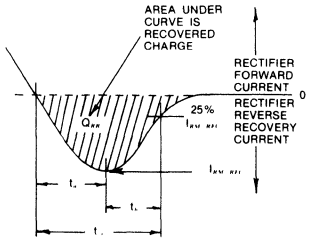


Figure 8. Rectifier Reverse Recovery

The reverse recovery time depends upon the operating conditions. For the IRF150 HEXFET, rated 28A continuous at 100V (the type used here), the reverse recovery time is about 400ns at maximum operating temperature, and about 260ns at 25°C, for an initial peak forward current of 70A, and a di/dt of 100A/μs.

Reverse recovery presents a potential problem when switching any rectifier OFF. The slower the rectifier, the greater the problem. Although the HEXFET's body-drain diode is relatively fast — not as fast as the fastest discrete rectifiers available, but considerably faster than comparably rated general purpose rectifiers — by comparison with the HEXFET itself, it is rather slow. This presents a potential problem in a chopper circuit, as we will now see.

To illustrate the problem, we will consider the motoring mode of operation. The operating condition that is troublesome is when freewheeling current is commutated from the body-drain diode of HEXFET 2 to the transistor of HEXFET 1. The operating sequence is depicted in Figure 9; the theoretical operating waveforms are shown in Figure 10.

Throughout the commutating sequence which, of course, is short by comparison with the overall fundamental operating cycle of the circuit, a constant current, I_M, is assumed to flow through the motor. During the operating period, t_0, the current, I_M, is freewheeling through the rectifier of HEXFET 2. At the start of the operating period, t_1, HEXFET 1 is turned ON, and the load current starts to transfer to the transistor of HEXFET 1. The current, i_1, in HEXFET 1 increases, while the current, i_2, flowing in the rectifier of HEXFET 2 decreases. The sum of i_1 and i_2 is equal to I_M. At the end of period t_1, the current flowing in HEXFET 1 is equal to the motor current, I_M, and the current flowing in the rectifier of HEXFET 2 is instantaneously zero.

Note that during period t_1 (also during the subsequent period t_a), the voltage across HEXFET 1 theoretically is virtually the full source voltage. This is because, as long as the rectifier of HEXFET 2 remains conducting, the voltage across it can be only its conduction voltage; the difference between this relatively small voltage and the total source voltage is developed across HEXFET 1.

This ignores the effect of circuit inductance. In practice, some of the source voltage will be dropped across circuit inductance, and the voltage across HEXFET 1 will be less than the source voltage, by the voltage drop across this inductance. A typical voltage across HEXFET 1 that takes account of the voltage drop across circuit inductance is represented by the dashed wave in Figure 10.

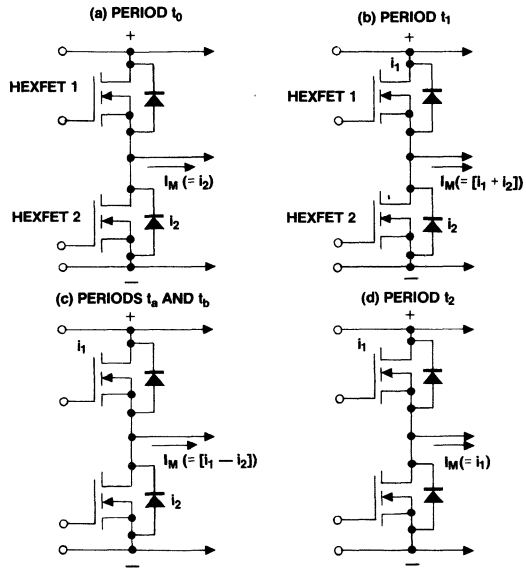


Figure 9. Commutation of Freewheeling Current I_M from the Rectifier of HEXFET 2 to the Transistor of HEXFET 1. HEXFET 1 and HEXFET 2 form a Tandem Series Connected Pair across a DC source.

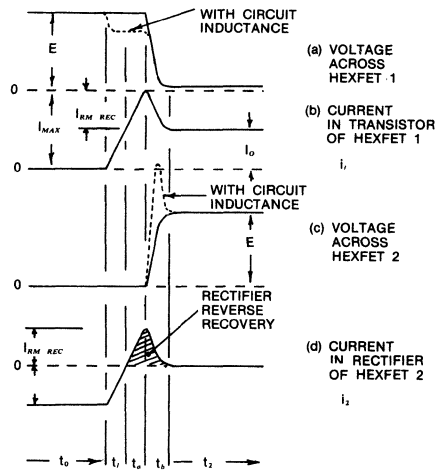


Figure 10. Theoretical Voltage and Current Waveforms for Commutating Sequence Depicted in Figure 9.

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If the rectifier was "perfect," with no recovered charge, the commutation process would be complete at the end of period t_1. In practice, the rectifier current reverses during the recovery periods t_a and t_b. During the period t_a, the reverse current i_2 increases until it reaches its peak value, $I_{RM(rec)}$. The current, i_1, through HEXFET 1 is now the sum of the rectifier reverse current, i_2, and the motor current, I_M, and its peak value, I_{MAX}, is the sum of I_M and $I_{RM(rec)}$. The voltage across HEXFET 1 still theoretically remains high, because the voltage across the rectifier of HEXFET 2 is still relatively low.

During the second part of the recovery period t_b, the rectifier of HEXFET 2 begins to support reverse voltage. The rectifier recovery current i_2 decreases, and the voltage across HEXFET 1 falls to its final conduction level. Note the effect that circuit inductance has in producing an overvoltage transient across the rectifier, as illustrated by the dashed wave in Figure 10.

Certain important points are evident. First, t_1, t_a, and to a lesser extent, t_b, are high dissipation periods. Second, the peak current in HEXFET 1 is the sum of the motor current and the rectifier reverse recovery current, and this peak current occurs at an instant when the voltage across the HEXFET is high. It is important that this peak current does not violate the HEXFET's I_{DM} rating. In fact, if the HEXFET is switched at a speed close to its limiting capability, and no other special precautions are taken, it certainly will do. If the peak current was to substantially exceed this rating, diode failure could occur, as explained in Ref. 1.

Fundamentally, the peak reverse recovery current of the rectifier can be reduced only by slowing down the rate of change of current during the commutation process. This is illustrated in Figure 11. The rate of change of current can be controlled either by inserting inductance into the circuit, or by purposefully slowing down the rate-of-rise of the gate pulse that drives HEXFET 1. A linear inductor inserted in the circuit for the purpose of slowing down the rate of change of current when the HEXFET is switched ON is not attractive, because it produces a transient voltage spike when switching OFF, to say nothing of the fact that it is an added "power circuit" component.

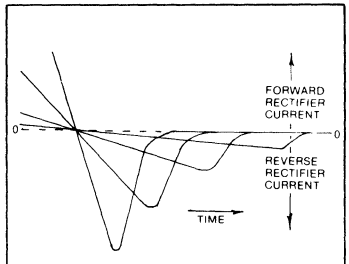


Figure 11. Reducing the Peak Rectifier Reverse Current by Reducing the Rate of Change of Current

The better practical solution is simply to slow down the switching-ON of the HEXFET by slowing down the drive signal. The peak current carried by the HEXFET can be reduced to almost any desired extent, at the expense of prolonging the high dissipation period. This is a necessary compromise in order to keep the peak current within safe limits, and as a practical matter, the switching losses, when averaged over the full operating cycle, are relatively small, for the operating frequencies that will be of interest in this application (normally a few hundred to a few thousand Hz).

Note that it is not necessary (nor desirable) to slow the switching-OFF; hence, the energy dissipation at switch-OFF will be relatively small by comparison with that at switch-ON. As explained in detail in Ref. 1, in this application a substantial dv/dt is likely to be applied across the HEXFET that acts as a diode during its reverse recovery. Since the device is sensitive to dv/dt at that time, a snubber should be added between drain and source, as shown in Figure 21.

Paralleling of HEXFETs

A key question that is fundamental to the successful demonstration of a chopper operating at hundreds of amperes, is the feasibility of multiple paralleling of HEXFETs.

Two questions must be considered: (1) "steady-state" sharing of current, and (2) dynamic sharing of current under the transitional switching conditions.

Steady-State Sharing of Current

During the periods outside of the switching transitions, the current in a parallel group of HEXFETs will distribute itself in the individual devices in inverse proportion to their ON resistance. The device with the lowest ON resistance will carry the highest current. This will, to an extent, be self-compensating, because the power loss in this device will be the highest. It will run hottest, and the increase in ON resistance due to heating will be more than that of the other devices, which will tend to equalize the current.

An analysis of the "worst case" device current in a group of "N" parallel connected devices can be based on the simplifying assumption that (N - 1) devices have the highest limiting value of ON resistance, while just one lone device has the lowest limiting value of ON resistance. The analysis can then be concentrated on the current in this one device.

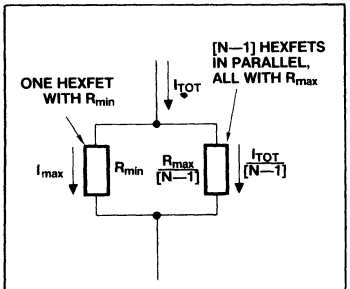


Figure 12. Simplified Equivalent Circuit for Estimating Worst Case Steady-State Current Unbalance

The equivalent electrical circuit shown in Figure 12 simplifies the analysis further by assuming the number of devices is sufficiently large that the current that flows through each of the high resistance devices is approximately $I_{TOT/(N-1)}$. On this assumption, the voltage drop across the lone low resistance device, and hence the current in it, can be calculated.

The ON resistance of each of the "high resistance" devices, at operating temperature, T, is given by:

$$R_{(max)T} = R_{(max)25}\left(1 + [(T_A - 25) + \frac{I^2_{TOT}}{(N-1)^2} R_{(max)T} R_{JA}] K\right)$$

where $R_{(max)25}$ is the limiting maximum value of ON resistance at 25° C, R_{JA} is the total junction-to-ambient thermal resistance in deg. C/W, and K is the per unit change of ON resistance per °C.

$$\therefore R_{(max)T} = \frac{R_{(max)25}\,(1 + [T_A - 25]\,K)}{1 - R_{(max)25}\,\frac{I^2_{TOT}\,R_{JA}\,K}{(N-1)^2}} \quad (1)$$

The voltage drop, V, across the parallel group is:

$$V = \frac{I_{TOT}}{(N-1)} \cdot R_{(max)T} \quad (2)$$

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The resistance of the one low resistance device at its operating temperature is:

$$R_{(min)T} = R_{(min)25}\,(1 + [T_A - 25 + V I_{(max)}\,R_{JA}]\,K)$$

where $R_{(min)25}$ is the limiting minimum value of ON resistance at 25° C, and $I_{(max)}$ is the current in this device.

$$\text{But, } R_{(min)T} = \frac{V}{I_{(max)}}$$

$$\therefore I_{(max)} = \frac{-b + \sqrt{(b^2 + 4aV)}}{2a} \quad (3)$$

where:

$b = R_{(min)25}\,(1 + [T_A - 25]\,K)$

$a = R_{(min)25}\,V\,R_{JA}\,K$

The following example shows the "worst case" degree of current sharing that can be expected, by applying the above relationships to the IRF150 HEXFET, and making the following assumptions:

$R_{(max)25} = 0.045\Omega$

$R_{(min)25} = 0.03\Omega$

$R_{JA} = 3$ deg. C/W

$\frac{I_{TOT}}{(N-1)} = 20A$

$K = 0.006$ per degree C

$T_A = 35°C$

Using the relationships (1), (2), and (3) above, it can be calculated that the "worst case" maximum value of device current is 27A for the hypothetical situation where all devices but one have high limiting ON resistance, of 0.045Ω, and carry 20A each, whereas the remaining one has low limiting ON resistance of 0.03Ω.

Dynamic Sharing of Current Under Switching Conditions

Turn-On

It is necessary to take positive steps to ensure that the current is distributed properly between a group of parallel connected devices during the switching transition. Since the HEXFETs will not all have identical threshold and gain characteristics, some will tend to switch sooner than others, and attempt to take more than their share of the current. Adding to the problem is the fact that circuit inductance associated with each device may be different, and this will also contribute to unbalancing the current under switching conditions. A detailed analysis of these waveforms can be found in Ref. 2. Here we will limit ourselves to a brief qualitative description of the different events that occur during a switching transition.

The problem will be introduced by considering the switching waveforms for the basic chopper circuit, shown in Figure 5, which contains a single HEXFET in each of the "motoring" and "regenerating" positions. We will consider the motoring mode of operation, under which HEXFET 1 is switched ON and OFF, while the motor current (assumed to be smooth, due to the motor inductance) alternates between this HEXFET and the body-drain diode of HEXFET 2, which acts as a freewheeling rectifier.

Figure 13 shows waveforms of drain current, drain-to-source voltage, and gate voltage during the turn-ON interval. We have already seen that in order to limit the peak recovery current of the body diode of HEXFET 2, the gate drive voltage for HEXFET 1 must be applied at a controlled rate. This is the reason that the applied drive pulse is shown increasing at a relatively slow rate.

At time, t_0, the drive pulse starts its rise. At t_1, it reaches the threshold voltage of the HEXFET, and the drain current starts to increase. At this point, two things happen which make the gate-source voltage wave-

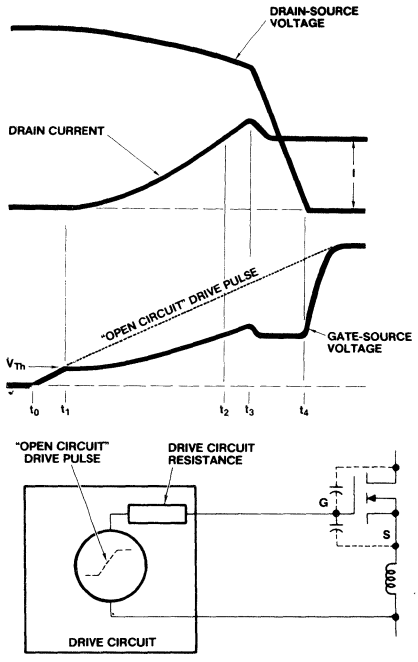


Figure 13. Waveforms at Turn-ON — Single HEXFET

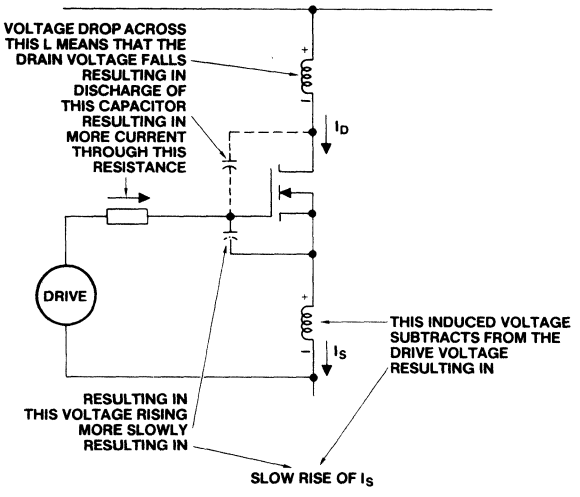


Figure 14. Diagrammatic Representation of Effects When Switching-ON

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form deviate from its original "path." First, inductance in series with the source which is common to the gate circuit develops an induced voltage, as a result of the increasing source current. This voltage counteracts the applied gate drive voltage and slows down the rate-of-rise of voltage appearing directly across the gate and source terminals; this, in turn, slows down the rate-of-rise of the source current. This is a negative feedback effect; increasing current in the source produces a counteractive voltage at the gate, which tends to resist the change of current.

The second factor that influences the gate-source voltage is the so-called "Miller" effect. During the period t_1 to t_2, some voltage is dropped across circuit inductance in series with the drain, and the drain-source voltage starts to fall. The decreasing drain-source voltage is reflected across the drain-gate capacitance, pulling a discharge current through it, and increasing the effective capacitance load on the drive circuit. This, in turn, increases the voltage drop across the impedance of the drive circuit and decreases the rate-of-rise of voltage appearing between the gate and source terminals. This also is a negative feedback effect; increasing current in the drain results in a fall of drain-to-source voltage, which, in turn, slows down the rise of gate-source voltage and tends to resist the increase of drain current. These effects are illustrated diagrammatically in Figure 14.

This state of affairs continues throughout the period t_1 to t_2, while the current in the HEXFET rises to the level of the current, I_M, already flowing in the freewheeling rectifier, and it continues into the next period, t_2 to t_3, while the current increases further, due to the reverse recovery of the freewheeling rectifier.

At time t_3, the freewheeling rectifier starts to support voltage, while the drain current and the drain voltage start to fall. The rate-of-fall of drain voltage is now governed by the Miller effect, and an equilibrium condition is reached, under which the drain voltage falls at just the rate necessary for the voltage between gate and source terminals to satisfy the level of drain current established by the load. This is why the gate-to-source voltage falls as the recovery current of the freewheeling rectifier falls, then stays constant at a level corresponding to the motor current, while the drain voltage is falling.

Finally, at time t_4, the HEXFET is switched fully ON, and the gate-to-source voltage rises rapidly towards the applied "open circuit" value.

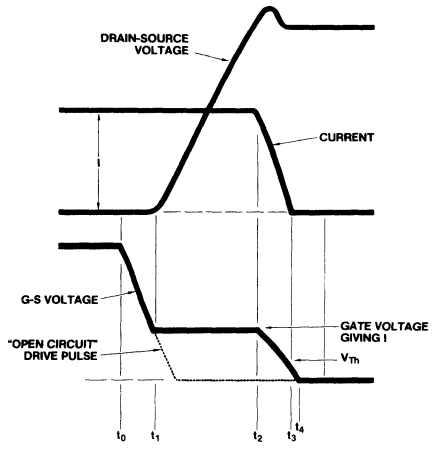


Figure 15. Waveforms at TURN-OFF — Single HEXFET

The gate-to-source voltage waveform for the circuit shown in Figure 5, with just a single device in each position, provides the clue to the difficulties that can be expected with parallel connected devices. The first potential difficulty is that if we apply a common drive signal to all gates in a parallel group, then the first device to turn ON — the one with the lowest threshold voltage — will tend to slow the rise of voltage on the gates of the others, and further delay the turn-ON of these devices. This will be due to the Miller effect. The inductive feedback effect, on the other hand, only influences the gate voltage of its own device (assuming that each source has its own separate inductance).

The second potential difficulty is that if the individual source inductances are unequal, then this will result in dynamic unbalance of current, even if the devices themselves are perfectly matched. Obviously, the solution to this is to ensure that inductances associated with the individual devices are as nearly equal as possible. This can be done by proper attention to the circuit layout.

As examined in detail in Ref. 3, there are several other circuit and device parameters that will contribute to dynamic unbalance. The conclusions presented in the above mentioned paper indicate, however, that the problem is not severe, as long as attention is paid to the following points, in order to ensure satisfactory sharing of current between parallel HEXFETs at turn-ON:

- Threshold voltages should be within determined limits.
- Stray inductances throughout the circuit should be equalized by careful layout.
- Gates should be decoupled with individual resistors, but not more than strictly required, as it will be explained later.

Turn-Off

Similar considerations apply to the dynamic sharing of current during the turn-OFF interval. Figure 15 shows theoretical waveforms for HEXFET 1 in the circuit of Figure 3 during the turn-OFF interval. At t_0, the gate drive starts to fall. At t_1, the gate voltage reaches a level that just sustains the drain current, I. The drain-to-source voltage now starts to rise. The Miller effect governs the rate-of-rise of drain voltage and holds the gate-to-source voltage at a level corresponding to the constant drain current. At t_3, the rise of drain voltage is complete, and the gate voltage starts to fall at a rate determined by the gate-source circuit impedance, while the drain current falls to zero.

Figure 16 shows theoretical waveforms for two parallel connected HEXFETs with their gates connected directly together. For purposes of discussion, the source inductance is assumed to be zero. At t_1, the gate voltage reaches the point at which HEXFET B can no longer sustain its drain current. The load current now

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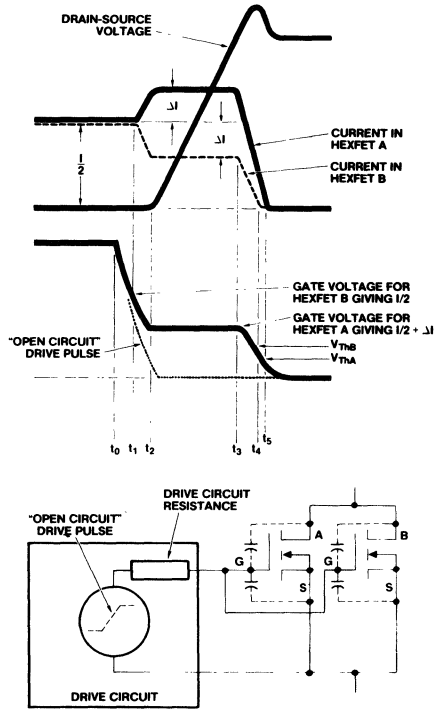


Figure 16. Waveforms at Turn-OFF — Two HEXFETs with Common Gates and Common Sources

redistributes; current in HEXFET B decreases, while that in HEXFET A increases. At t_2, HEXFET B can no longer sustain its current; both HEXFETs now operate in their "linear" region, and the drain voltage starts to rise. The gate-to-source voltage is kept practically constant by the Miller effect, while the currents in the two HEXFETs remain at their separate levels. Clearly, the unbalance of current in this example is significant.

While a turn-off unbalance is potentially a more serious problem, the analysis in Ref. 3 shows that this is not so in practice as long as the devices are turned off with a "hard" (very low impedance) gate drive. This by itself will almost guarantee limited dynamic unbalance at turn-off.

In summary, to achieve good sharing at turn-off the same precautions should be used as for turn-on, with the addition of a "hard" drive.

Figure 17 shows that when using paralleled devices, a low impedance path is generated that may be prone to parasitic self oscillations. For this reason some degree of gate decoupling is needed as necessary to prevent oscillations.

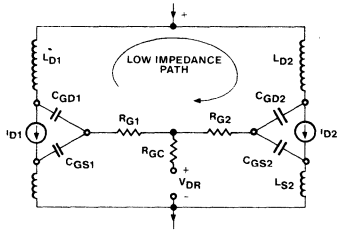


Figure 17. Low Impedance Path for Parasitic Oscillation for Unbalanced Parallel Branches

A Complete Functional Control Scheme for a Two-Quadrant Chopper

A simplified functional diagram of the control and drive circuitry for a two-quadrant HEXFET chopper is shown in Figure 18; this is intended to demonstrate the basic operating principle of the overall chopper system, and differs in some minor details from the actual practical circuitry presented later (Figure 22).

The control system has an outer voltage feedback loop, which compares the motor voltage with a reference voltage and processes the resulting "error" signal to keep the motor voltage essentially equal to the reference value. In a practical system, the voltage control loop could be complemented with a signal proportional to the armature voltage drop, to give a closer regulation of actual motor speed. Alternatively, the voltage feedback signal could be substituted with a signal from a tachogenerator, to give a more precise speed regulation.

An inner control loop regulates the current to the level required to satisfy the load on the motor. The current control loop also determines the chopper switching frequency by regulating the peak-to-peak ripple current between preset upper and lower limits. This it does by switching the HEXFET ON whenever the current falls a given amount below the reference value, and switching the HEXFET OFF whenever the current rises a given amount above it.

The current control loop also provides instantaneous limiting of the peak HEXFET and motor current. This is accomplished simply by setting a maximum limit on the current reference signal and clamping it to this level. Whenever the instantaneous motor current attempts to exceed the maximum current reference by more than the preset peak ripple current, the HEXFET is immediately switched OFF. Thus, the system is completely self-protecting against overcurrent.

Referring to the functional diagram in Figure 18, the voltage reference is compared with the voltage across the motor, and the error signal is amplified through the voltage error amplifier. The output of the voltage error amplifier is the current reference signal. The voltage error signal is also fed into the *motor-regenerate* logic comparator. When the voltage error is positive, the current reference is also positive, and the control circuit is demanding "motoring" current. The output of the *motor-regenerate* logic comparator is high, the *motor* signal has a logic "1" value, while the *regen* signal has a logic "0" value. Switches A and D are closed, while switches B and C are open.

When the current reference is negative, the control circuit is demanding "regenerating" current. The output of the *motor-regenerate* logic comparator is negative, the *regen* signal has a logic "1" value, while the *motor* signal has a logic "0" value. Switches B and C are closed, while A and D are open.

The *motor-regenerate* logic comparator has a built-in hysteresis to

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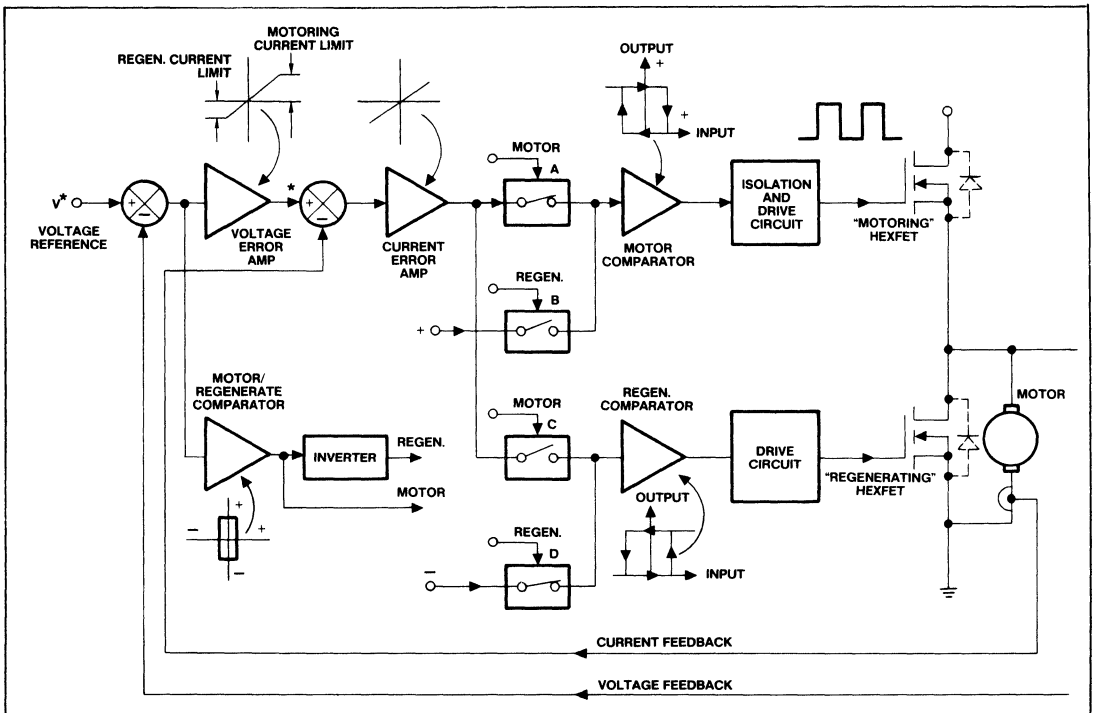


Figure 18. Simplified Control System

prevent unwanted "bouncing" back and forth between the "regeneration" and "motoring" modes of operation, at low current levels.

Consider the "motoring" mode of operation. The positive current reference signal is compared with a signal representing the actual motor current; the difference is amplified through the current error amplifier. The output of this amplifier is fed through switch A, which is closed, to the *motor* comparator. This comparator produces a "0" output signal in response to a positive input signal above a preset threshold level, and a "1" output signal in response to a negative input signal below a certain preset level.

The output signal of the *motor comparator* is isolated and shaped to become the gate drive signal for the "motoring" HEXFET. The "motoring" HEXFET is thereby switched ON when the motor current falls a predetermined amount below the reference and OFF whenever the motor current rises a predetermined amount above the reference value, while the switching frequency automatically adjusts itself to keep the peak-to-peak ripple current constant. The peak-to-peak ripple current and operating frequency can be adjusted by adjusting the hysteresis of the *motor* comparator.

Note that in the motoring mode, switch D is closed, applying a steady negative input to the *regen* comparator, and shutting OFF the gate drive signal to the "regenerating" HEXFET. Theoretical waveforms which illustrate the operation of this scheme in the motoring mode are illustrated in Figure 19.

In the regenerating mode of operation, switches B and C are closed. A continuous positive signal is applied to the input of the *motor* comparator, shutting OFF the drive to the "motoring" HEXFET. The current reference is negative, and the current error signal is fed to the input of the *regen* comparator. This comparator produces a "1" output signal in response to a positive input signal above a certain preset level, and a "0" output signal in response to a negative input signal below a given preset level. The "regenerating" HEXFET is now switched ON whenever the regenerative current from the motor falls a preset amount below the reference value, and OFF whenever the motor current rises a preset amount above the reference value. Theoretical waveforms which illustrate the operation in the regenerating mode are shown in Figure 20.

A 48V, 200A Experimental Chopper

Power Circuit

A schematic diagram of the power circuit of an experimental laboratory chopper is shown in Figure 21. This employs a total of ten IRF150 HEXFETs connected in parallel for the "motoring" switch, and five IRF150 HEXFETs connected in parallel for the "regenerating" switch.

All HEXFETs are mounted on a 22-inch length of aluminum heatsink extrusion, with outer dimensions of 5 inches by 3 inches, with the regenerating HEXFETs being isolated electrically from the heatsink.

The assembly is capable of delivering 200A forward "motoring" current and 140A of "regenerating" current. The "motoring" HEXFETs by themselves actually are capable of carrying about 300A of output current; the 200A limit is set by the current carrying capacity of the five freewheeling body-drain diodes of the "regenerating" HEXFETs.

Control and Drive Circuitry

Figure 22 shows a diagram of the control and drive circuitry. This is

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based upon the functional circuit shown in Figure 18 and requires no additional explanation other than to point out that for practical reasons, some of the signal polarities are opposite to those assumed for the simplified functional circuit of Figure 18.

Test Results

Practical test results are shown in Figures 23 through 27.

Figure 23 shows the current when the motor accelerates from standstill to about half speed. The current limit circuit keeps the peak motor current to just over 200A. The chopping frequency is about 2 kHz.

Figure 24 shows motor current and voltage waveforms when accelerating from half speed to almost full speed, then decelerating back to half speed. The current limit holds the peak motoring current to about 205A, and the peak regenerating current to about 140A.

Figure 25 shows the output voltage and current of the chopper with a passive inductive load. Note the classical linear rise and fall of the current associated with an inductive load.

Figures 26 and 27 show turn-ON and turn-OFF oscillograms respectively for one HEXFET, with the chopper operating with a passive inductive load of 120A. These waveforms generally agree with the foregoing theoretical discussion. Note, however, in Figure 27, that the gate voltage reverses at a switch-OFF; this is due to resonance between the gate capacitance and circuit inductance.

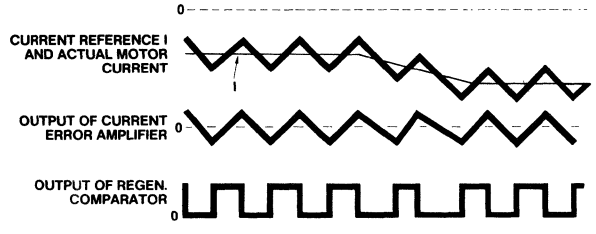


Figure 19. Theoretical Waveforms for the Motoring Mode of Operation

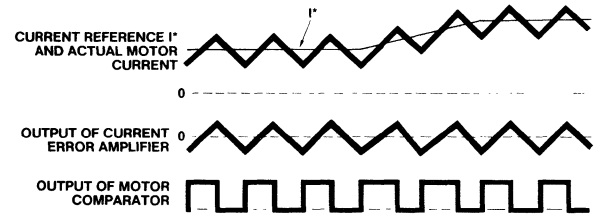


Figure 20. Theoretical Waveforms for the Regenerating Mode of Operation

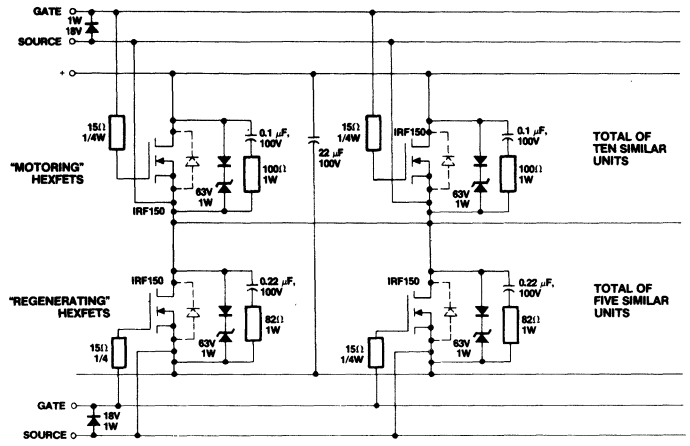


Figure 21. Power Circuit Schematic

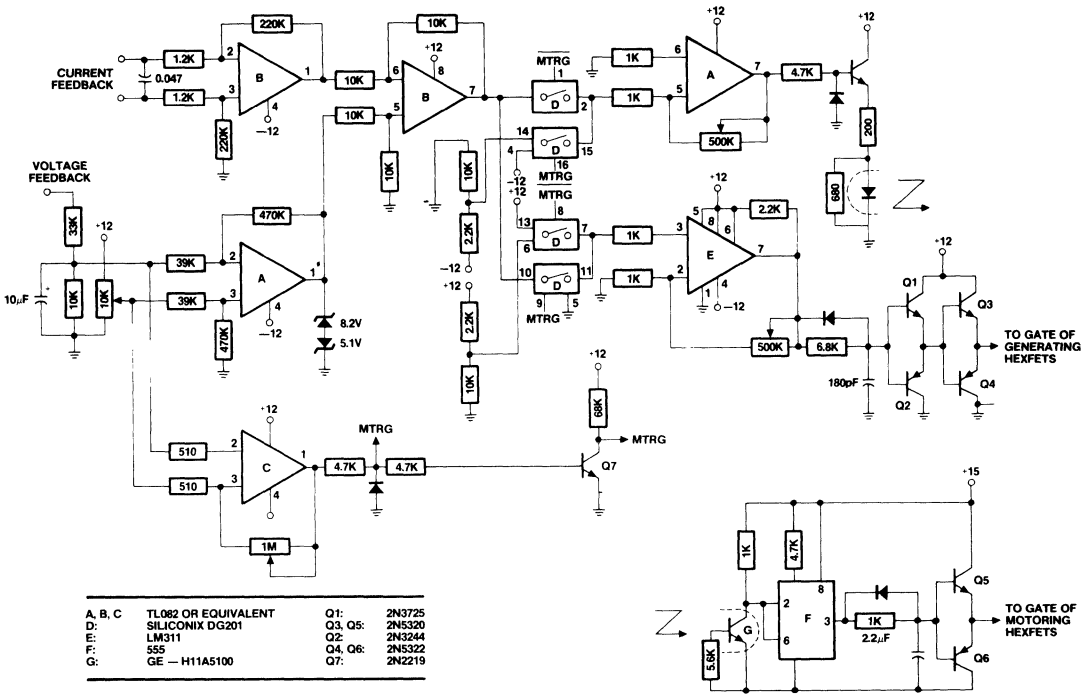
Conclusions

This application note has demonstrated the technical feasibility of a DC-to-DC chopper using parallel connected HEXFETs for motor speed control, operating at the 200A level, and the use of HEXFET's body-drain diode to provide the freewheeling and flyback functions needed for two quadrant operation. The potential attractions of using HEXFETs are simplicity of drive circuitry, ruggedness, speed of response, ease of paralleling and overall compactness.

Power HEXFETs also offer an interesting system advantage in this type of application. Due to the ease of operating at high frequency, a separately excited field winding, with the added motor controlability and superior system performance that this provides, becomes a practical reality. Present-day choppers using bipolar transistors or thyristors generally operate at relatively low frequency (in order to keep them simple), and require a series-connected field winding to keep the motor ripple current to an acceptable level. With the higher chopper frequency made possible by power HEXFETs, on the other hand, the inductance of the motor armature is by itself sufficient to smooth the current, thus allowing the field winding to be disassociated from the armature circuit, and to be independently controlled, offering better system performance and superior control flexibility.

As improvements in circuit design, MOSFET technology, packaging,

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A, B, C	TL082 OR EQUIVALENT	Q1:	2N3725
D:	SILICONIX DG201	Q3, Q5:	2N5320
E:	LM311	Q2:	2N3244
F:	555	Q4, Q6:	2N5322
G:	GE — H11A5100	Q7:	2N2219

Figure 22. Control and Drive Circuit Schematic

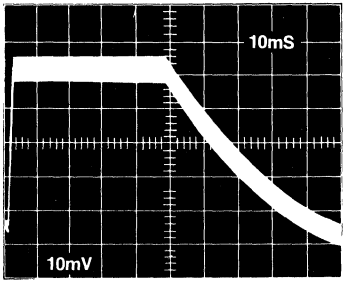


Figure 23. Motor Current under Acceleration. Peak Motor Current = 220A. 40A per division. 10ns per division.

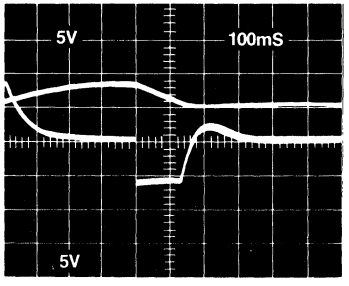


Figure 24. Motor Voltage & Current when Accelerating & Decelerating. Peak Motoring Current = 205A. Peak Regenerating Current = 140A. Top Trace: Voltage 25V per division. Bottom Trace: Current 115A per division.

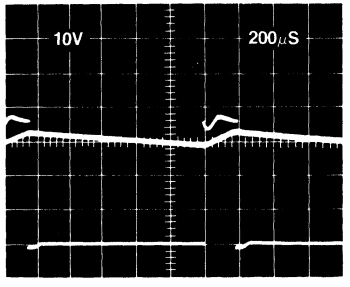


Figure 25. Output Voltage & Current of Chopper into Passive Inductive Load — 220 μs per division. Lower Trace: Voltage 10V per division.

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and device costs all take place, the type of system described in this application note will become economically as well as technically superior to today's chopper systems using bipolar transistors or thyristors. □

References:

1. International Rectifier Application Note AN934A: "The HEXFET Integral Body Diode".
2. International Rectifier Application Note AN947: "Understanding HEXFET Switching Performance".
3. J.B. Forsythe: "Paralleling of Power MOSFETs," IEEE-IAS Conference Record, October 1981.

Acknowledgements

The assistance of H. Murphy and T. Gilmore of Allis Chalmers, and of F. Stich of Siemens Allis, in reviewing and commenting upon this application note, and in providing the motor, is gratefully acknowledged.

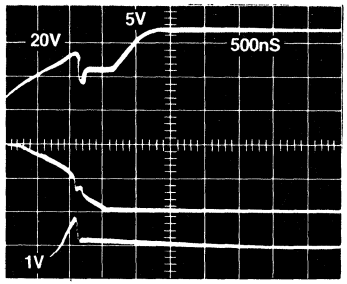


Figure 26. Turn-On Oscillograms for one HEXFET. Total Output Current = 120A. 500ns per division. Top Trace: Gate-Source Voltage 5V per div. Middle Trace: Drain-Source Voltage 20V per div. Lower Trace: Drain Current 10A per div.

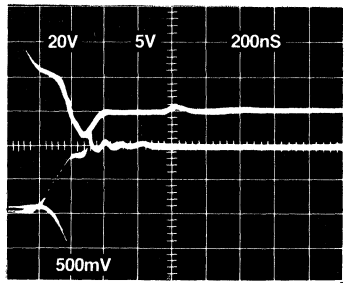


Figure 27. Turn-Off Oscillograms for one HEXFET. Total Output Current = 120A. 200ns per division. Top Trace: Gate-Source Voltage 5V per div. Middle Trace: Drain-Source Voltage 5A per div. Lower Trace: Drain Current 5A per div.

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High Voltage, High Frequency Switching Using a Cascode Connection of HEXFET® and Bipolar Transistor

(HEXFET is the trademark for International Rectifier Power MOSFETs)

By S. CLEMENTE, B. PELLY, R. RUTTONSHA, B. TAYLOR

Summary

A cascode connection of high voltage bipolar transistor and low voltage HEXFET is described. A specific example is considered that is capable of switching 10A at 750V in 200-300 nanoseconds. The use of this combination al "BIMOS" switch is demonstrated in a 10A inverter bridge circuit operating at 25kHz from a dc input voltage up to 750V.

Introduction

Power HEXFETs are now firmly established at voltage ratings up to 500V. Their main attributes are very fast switching speed, permitting switching frequencies of hundreds of kilohertz — very high input impedance, permitting very simple drive circuitry — and absence of second breakdown, permitting reduction or elimination of protection circuitry, and enhanced reliability.

The power HEXFET is a majority carrier device, and its on-state voltage drop is a strong function of voltage rating. A 100V rated HEXFET, for example, has a voltage drop at rated usable current, at rated maximum junction temperature, of about 2.5V, while a 500V rated device has a voltage drop of about 9V, at rated maximum junction temperature.

MOSFETs with voltage ratings above 500V are technically feasible, but voltage drop increases rapidly, as illustrated in Figure 1. An 850V rated MOSFET, for example, would have a voltage drop of about 18V, and a 1000V rated MOSFET would have about a 23V drop. This relationship between voltage drop and voltage rating is presently a barrier to general commercial usage of power MOSFETs at voltage ratings much above 500V.

Circuit designers would nonetheless welcome an 800 to 1000V rated device, with the switching performance and Safe Operating Area of a power HEXFET, but with a voltage drop — and price — that are lower than those of a comparably rated high voltage MOSFET.

This device, if it existed, would open up a range of application possibilities, such as direct off-line (240V) high frequency (20-250kHz) single-ended switching power supplies, and direct off-line (440/480V, 3-phase) high frequency bridge inverter circuits for motor drives, uninterruptable power supplies, and high power (class D) switching amplifiers.

The concept of using a low voltage, fast switching transistor in the emitter of a second high voltage transistor — in a so-called *cascode* connection —to yield a combined high voltage, high speed switch is not new, and has been employed in the past using pairs of bipolar transistors.

With the availability of power HEXFETs, this cascode technique can be looked at with renewed interest, because a high voltage device with HEXFET-like switching performance and relatively low conduction voltage drop can be implemented by combining a high voltage bipolar with a low voltage HEXFET. The best features of each device can be combined to provide operating characteristics that cannot be achieved with either one on its own. This cascode combination of *BI*polar transistor and power *MOS*FET is referred to in this application note as a *BIMOS* switch.

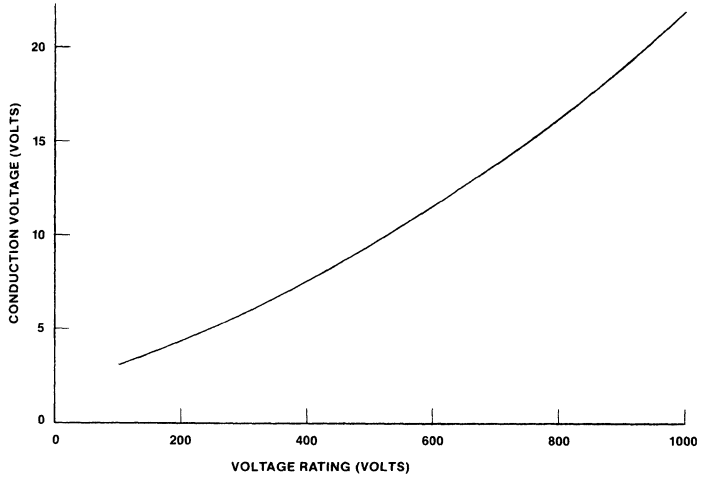


Figure 1. Conduction voltage versus voltage rating of power MOSFET. T_J = 150°C

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Basic Principle of BIMOS Switch

The basic BIMOS switch is shown in Figure 2. It is switched ON and OFF by control of the gate of the HEXFET. When the HEXFET is ON, the bipolar is ON, since it receives base drive current from the bias supply voltage V_B. When the HEXFET is OFF, the bipolar is also OFF, since its emitter is open-circuited.

The voltage developed across the HEXFET when it is OFF is essentially only the bias voltage supply V_B (typically 10 to 15V). The collector-source blocking voltage capability of the combined BIMOS switch is the relatively high V_{CBO} rating of the bipolar, because of the "common base" configuration. In addition, the switching speed of the bipolar is much faster than is achievable in the usual common emitter connection. In essence, this is because the "forcible" opening of the emitter at switch-OFF diverts the collector current in its entirety out of the base.

Since the ON or OFF condition of the BIMOS switch is controlled at the gate of the HEXFET, the input impedance is that of the HEXFET; the externally applied drive current is only that needed to charge and discharge the self capacitance of the HEXFET.

Consideration of a specific example — the 2N6547 bipolar transistor in combination with the IRF131 HEXFET — will illustrate typical performance characteristics. Figure 3 shows the Switching Safe Operating Area of the 2N6547 transistor in common base configuration. Also shown is the Safe Operating Area for the common emitter configuration. Note the substantially wider Safe Operating Area for common base, reflecting the 850V V_{CBO} rating versus the 400V V_{CEO} rating of this device.

Table 1 shows typical switching times of the 2N6547 in the common base connection, for different conduction times, when switching 10A in a 650V circuit. The storage times (180ns to 1000ns) are considerably shorter than for the common emitter connection (typically 2 to 4μs), as are the switching times (40ns to 230ns versus 1 to 1.5μs).

Table 1. Turn-Off Switching Times — 2N6547 (Common Base). Clamped Inductive Load.

On Time	Storage Time	Switching Time
1μs	180ns	40ns
2μs	200ns	50ns
4μs	400ns	85ns
6μs	520ns	120ns
8μs	620ns	160ns
10μs	700ns	170ns
15μs	900ns	210ns
20μs	1000ns	230ns

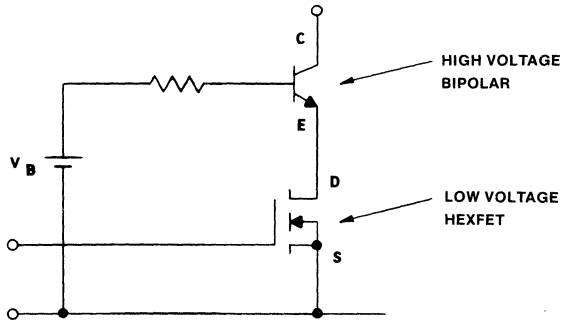


Figure 2. Cascode connection of HEXFET and bipolar

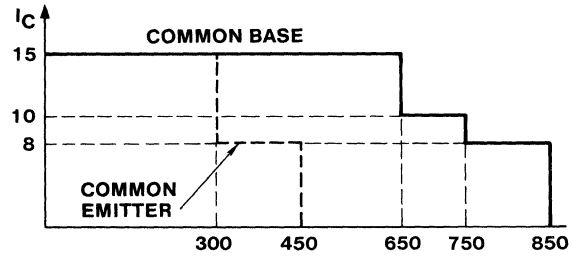


Figure 3. Comparison of common emitter and common base switching SOA of 2N6547 Bipolar

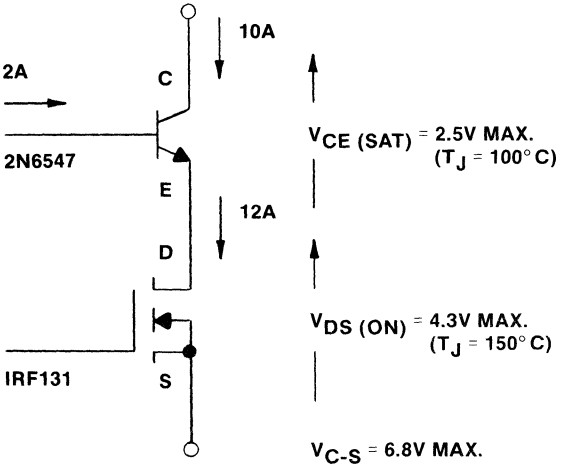


Figure 4. Maximum conduction voltage of BIMOS switch using 2N6547 and IRF131

Test Conditions for Table 1 are: I_C = 10Amps, I_{BI} = 2Amps, $V_{collector}$ = 650V DC

Switching time is the sum of collector voltage rise time and collector current fall time, measured from 10% collector voltage to 10% collector current.

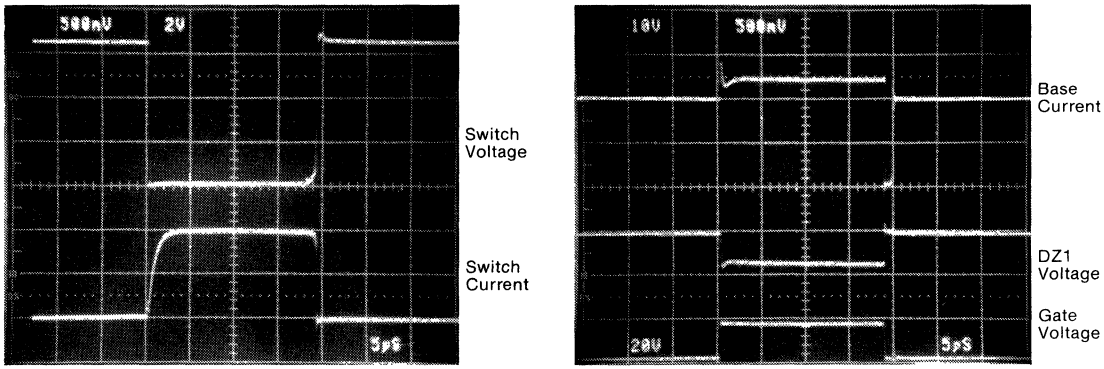
As illustrated in Figure 4, the conduction voltage drop across the BIMOS switch at a load current of 10A (the maximum usable current of the 2N6547) is about *6.8 V*. This compares with about 18V for an equivalent 10A, 850V rated HEXFET.

Circuit Implementation

In practice it will generally be more convenient to replace the fixed voltage supply V_B in Figure 2 with a proportional base drive, derived from a current transformer in the collector circuit. A practical circuit is shown in Figure 5.

The capacitor C1 is charged to the voltage of the zener diode DZ1 when the BIMOS switch is OFF. When the HEXFET is switched ON, base drive for the bipolar is initially derived from C1. Once the collector current is estab-

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(a) Upper: 200V/div 5μs/div
Lower: 5A/div

(b) Upper: 5A/div 5μs/div
Middle: 10V/div Lower: 20V/div

Figure 6. Oscillograms for BIMOS switch of Figure 5 when switching 650V, 10A into resistive/inductive load (65Ω, 50μH) with parallel clamping diode

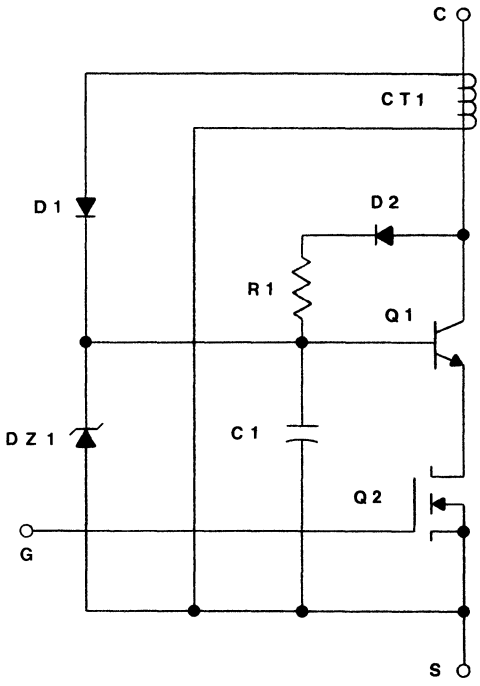


Figure 5. Practical implementation of BIMOS switch
(For component detail see Table 2, page 6.)

lished, CT1 supplies steady base drive current to the bipolar.

With this particular transformer the maximum ON time of the switch when carrying 10A is about 25μs, and the minimum OFF time — required to reset the current transformer — is about 1.5μs. The peak "reset" voltage across the secondary of the current transformer is approximately 135V; this is determined largely by circuit capacitance. Typical operating oscillograms for this basic BIMOS switch are shown in Figures 6 through 10. A brief description of these waveforms follows:

Figure 6(a) shows waveforms of voltage and current when switching 650V, 10A. The load has approximately 65Ω resistance and 50μH series inductance, with a clamping (freewheeling) diode connected across it. The relatively slow rate of rise of current at switch ON is due to the load inductance. Note the rapid fall time of the voltage during turn ON and the rapid rise and fall times of the voltage and current during turn OFF.

Figure 6(b) shows the base current in the bipolar transistor, the voltage across DZ1, and the drive voltage at the gate of the HEXFET. Note the initial "spike" of base current supplied by the capacitor C1. Note also the reverse base current of 10A during the storage period, equal to the 10A collector current, due to the open emitter. The storage time for this 10A collector

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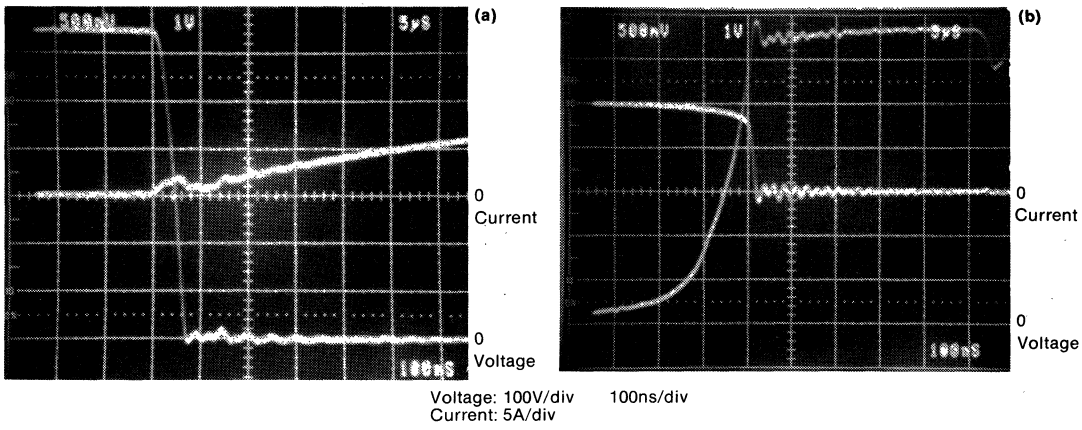


Figure 7. Voltage and current waveforms for BIMOS switch of Figure 5 (a) at turn-ON, and (b) at turn-OFF, when switching 650V, 10A, into resistive/inductive load (65Ω, 50μH) with parallel clamping diode

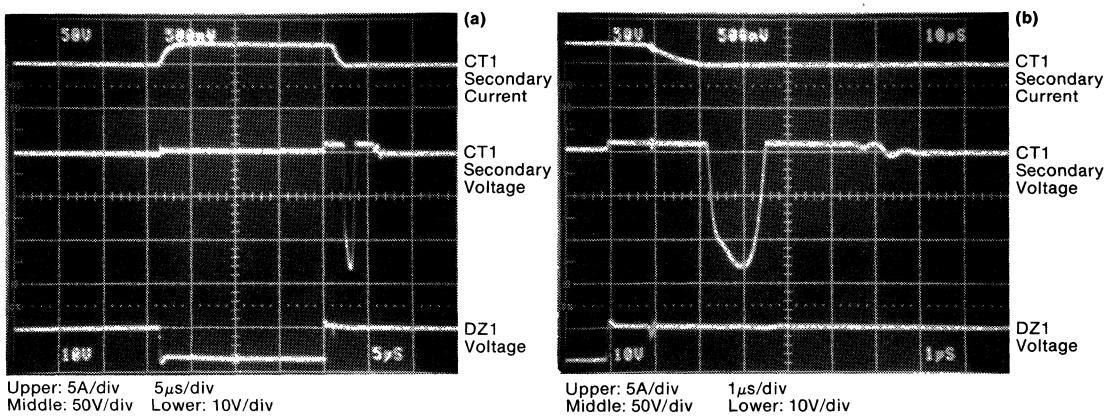


Figure 8. Base drive circuit waveforms for BIMOS switch of Figure 5 when switching 10A (a) 5μs/div (b) expanded to 1μs/div to show details of turn-OFF

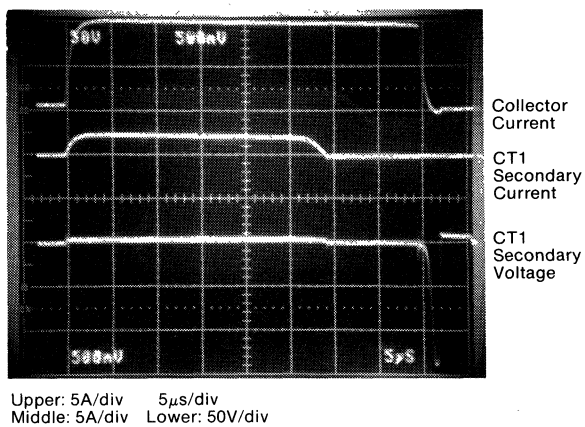


Figure 9. Base drive circuit waveforms for BIMOS switch of Figure 5 with conduction time greater than the 25μs maximum limit permitted by CT1

current level and 18μs conduction time is approximately 1μs.

Figure 7 shows expanded voltage and current waveforms for the BIMOS switch at turn-ON and turn-OFF. The voltage fall time at turn-ON is less than 100ns, and the combined voltage rise time and current fall time at turn-OFF for this 18μs conduction time is about 200 nanoseconds.

Figure 8 shows base drive waveforms for the bipolar. The reset voltage spike across the secondary of CT1 has a peak value of approximately 135V. The reset time is approximately 1.5μs.

Figure 9 shows base drive waveforms for a "forbidden" operating mode when the conduction time is extended beyond the 25μs maximum permitted by this particular current transformer. The transformer starts to saturate after about 28μs, collapsing the base drive to the transistor. Since

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the HEXFET is still switched ON, the emitter of the bipolar is still "grounded." The collector current continues to flow for the relatively long "grounded emitter" storage time of the bipolar — about 12μs. (To add insult to injury, negative base current is zero; this would normally be applied to the grounded emitter configuration to shorten storage time.) The "grounded base" storage time, by contrast, (Figure 6(b)) is about 1μs.

Figure 10 shows the effect on the switching waveforms of changing the voltage of zener diode DZ1 (Figure 5). With a zener voltage of 5V (Figure 10(a)), the fall time of the voltage at turn-ON is relatively slow (100ns), since the capacitor C1 is charged to only 5V, and supplies only a mediocre "spike" of base current at turn-ON. During the storage time at turn-OFF the collector-drain voltage becomes the zener voltage of DZ1 plus the collector-base voltage; this voltage is relatively low, because the zener voltage is relatively low. Dissipation during this period is therefore relatively small.

With a zener voltage of 18V (Figure 10(b)) the fall time of the voltage at turn-ON is reduced to about 50ns, because of the increased charge in C1. The collector-drain voltage at turn-OFF during the storage time is, however, relatively high, because the zener voltage is relatively high, and dissipation during this period is increased.

Judicious selection of the zener voltage will minimize the total switching losses. The 10V zener used in Figure 5 and 11 was judged to be near-optimum.

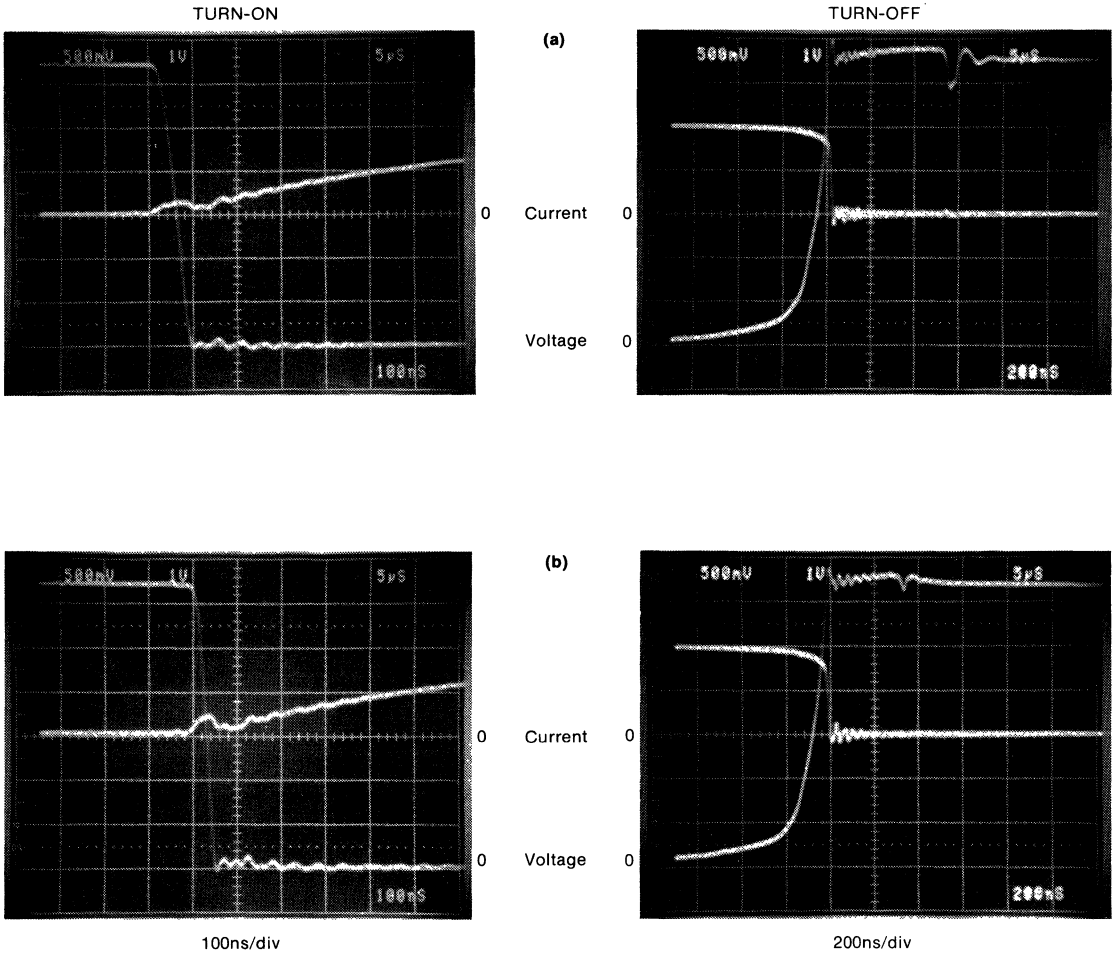


Figure 10. Voltage and current waveforms at turn-ON and turn-OFF for the BIMOS switch of Figure 5 when switching 10A at 650V with DZ1 voltage (a) 5V and (b) 18V

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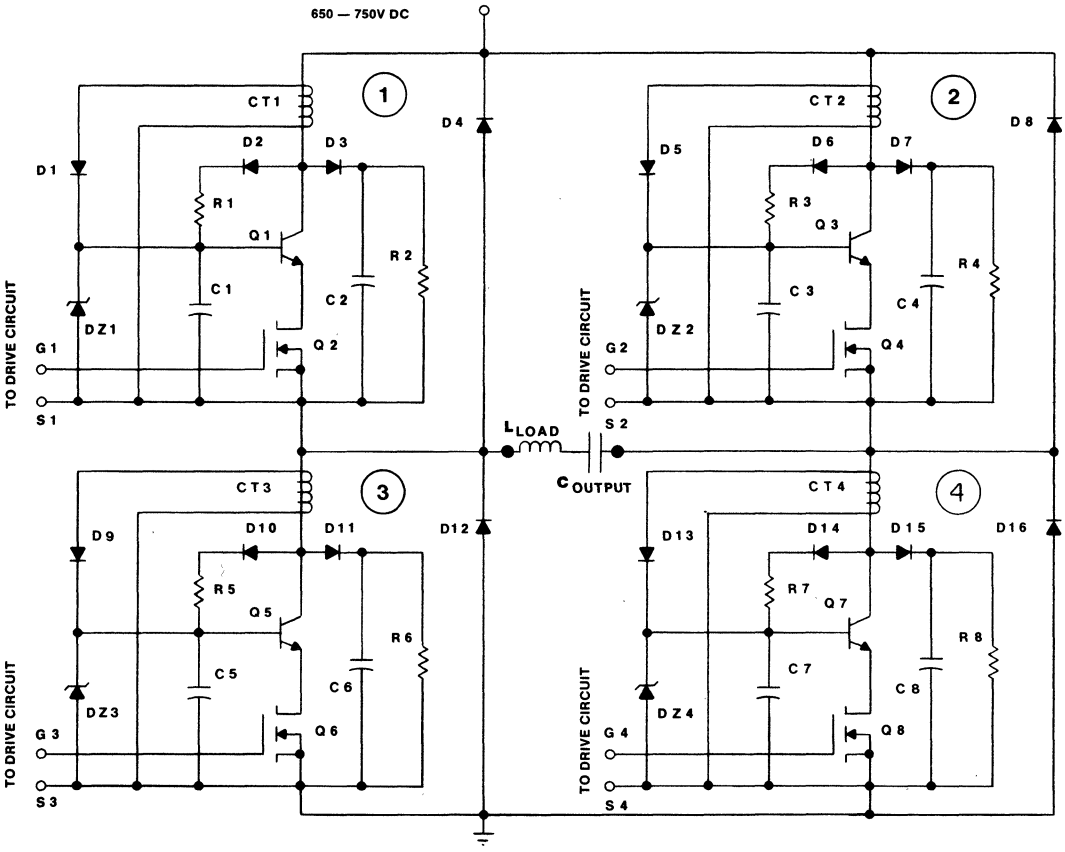


Figure 11. BIMOS bridge circuit

Table 2. Components Listing for Figure 5 and 11.

LIST OF COMPONENTS FOR BIMOS BRIDGE CIRCUIT	
Q_1, Q_3, Q_5, Q_7	IR2N6547
Q_2, Q_4, Q_6, Q_8	IRF131
C_1, C_3, C_5, C_7	0.1μF
C_2, C_4, C_6, C_8	0.068μF, 1000V
R_1, R_3, R_5, R_7	100k ½W
R_2, R_4, R_6, R_8	100k 2W
D_1, D_5, D_9, D_{13}	UES1305
D_2, D_6, D_{10}, D_{14}	IR IN4007
D_3, D_7, D_{11}, D_{15}	Two IR 40SL6 connected in series with sharing resistors
D_4, D_8, D_{12}, D_{16}	12FL100S05
DZ, DZ_2, DZ_3, DZ_4	10V zener diode, 1.5W
CT_1, CT_2, CT_3, CT_4	Primary 2 turns #16 Secondary 10 turns #24 Core TDK H5B2T10-20-5

A BIMOS Bridge Inverter Operating at 650-750V DC, 10A, 25kHz

A major circuit application area for a BIMOS switch is in high frequency bridge inverters operating from 440/480V, 1 or 3-phase lines, for large switching power supplies, motor drives, welding, induction heating, uninterruptible power supplies, high power switching amplifiers, and so on.

The feasibility of a BIMOS switch for this type of application has been demonstrated in an experimental single phase BIMOS bridge circuit operating from 650 to 750V DC at 10A, 25kHz. A diagram of the power circuit is shown in Figure 11. The test results reported in this article are for an inductive load, with a blocking capacitor, C_{OUTPUT}, used to prevent DC load saturation. The experimental control and drive circuitry is shown in Figure 12.

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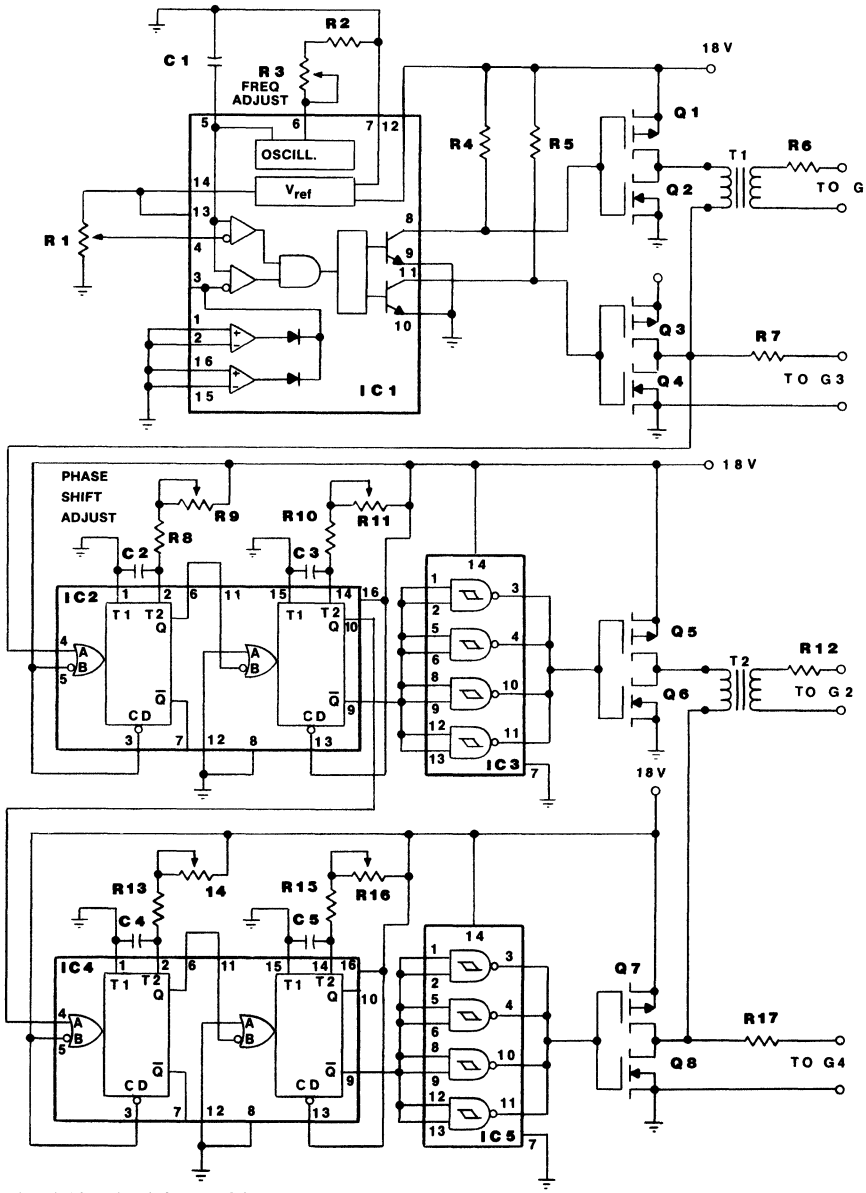


Figure 12. Control and drive circuit for BIMOS bridge

Table 3. Components Listing for Figure 12.

LIST OF COMPONENTS FOR CONTROL AND DRIVE CIRCUIT FOR BIMOS BRIDGE			
Q_1, Q_3, Q_5, Q_7	IRFD9121	R_3	5kΩ, ten turn potentiometer ¼W
Q_2, Q_4, Q_6, Q_8	IRFD111	R_4, R_5	150Ω, 2W
IC_1	Texas Instrument TL494	R_6, R_7, R_{12}, R_{17}	22Ω, ¼W
IC_2, IC_4	MC14528B	R_8, R_{10}, R_{13}, R_{15}	4.7kΩ, ¼W
IC_3, IC_5	MC14093B	R_9	500kΩ, ¼W ten turn potentiometer
C_1	0.01μF	R_{11}, R_{14}, R_{16}	50kΩ, ¼W ten turn potentiometer
C_2	68pF	T_1, T_2	Primary: 40 turns #24
C_3, C_4, C_5	.0068μF		Secondary: 40 turns #24
R_1	5kΩ, ten turn potentiometer		Core TDK H_5B_2T10-20-5
R_2	2.2K ¼W		

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Idealized gating waveforms for the BIMOS switches are shown in Figure 13. Each leg or "pole" of the inverter circuit is gated to deliver a 180° square wave of output voltage (with respect to DC midpoint potential), with a short deadtime when switching from an upper to a lower device, and vice versa, to allow for the storage time of the BIMOS switch. Pulse width control of the output voltage of the bridge is obtained by phase-shifting the gating waveforms applied to the two legs of the bridge. With this gating regime two of the four switches are always gated ON (except during the short crossover dead-time), and the output voltage waveform is always defined by the gating pattern, independent of the load characteristics.

A "simpler" gating regime under which diagonally opposite pairs of switches were simultaneously gated ON for a controllable time, with all gating signals being removed during the intervening periods, was unsatisfactory. This is because substantial oscillation took place between the self capacitance of the switch and the inductance of the load, once inductive current feedback from the load to the DC source was completed, and the BIMOS switches were then left temporarily "floating" with no gating signals applied to them. Operation with this "incorrect" gating regime is illustrated by the oscillograms in Figure 14.

Figures 15 through 24 show waveforms which illustrate the operation of this experimental BIMOS bridge circuit. The dc input voltage for Figures 15 through 23 is 650V, and for Figure 24 it is 750V. A description of these oscillograms follows:

Figure 15(a) shows output voltage and current waveforms with partial-width output voltage pulses, and Figure 15(b) shows corresponding waveforms with almost "full" width output voltage. The peak current for this latter case is approximately 10A.

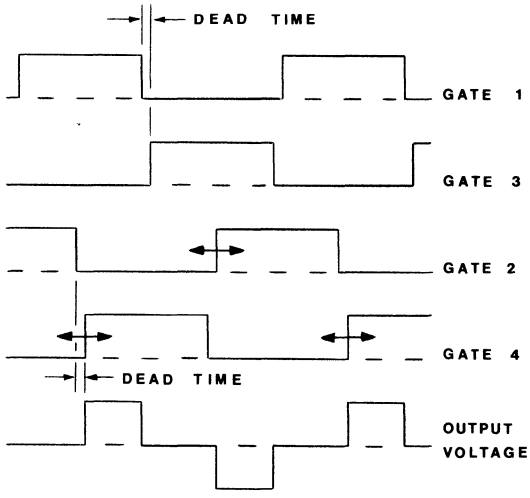


Figure 13. Gating regime for experimental BIMOS bridge

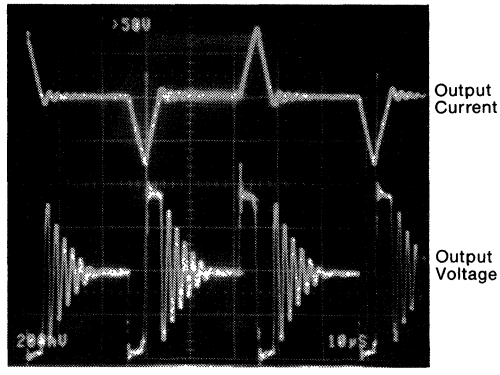
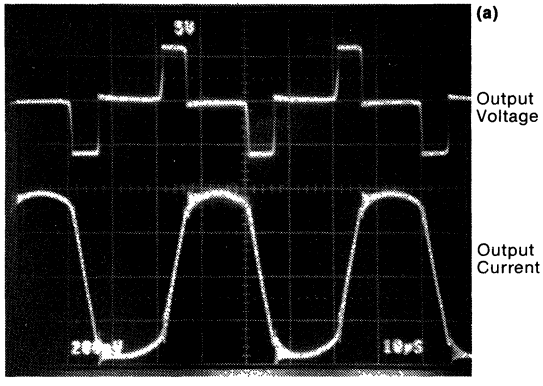
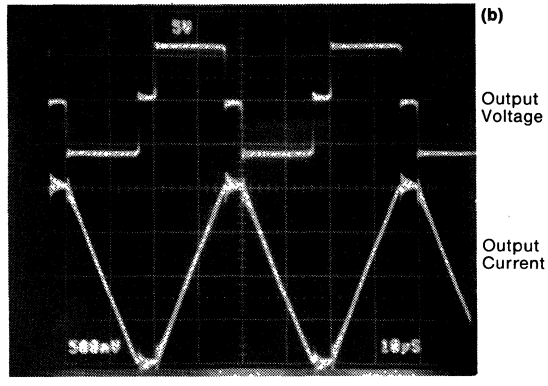


Figure 14. Output current and voltage waveforms with "incorrect" gating regime. Inductive load



Upper: 500V/div 10μs/div
Lower: 2A/div



Upper: 500V/div 10μs/div
Lower: 5A/div

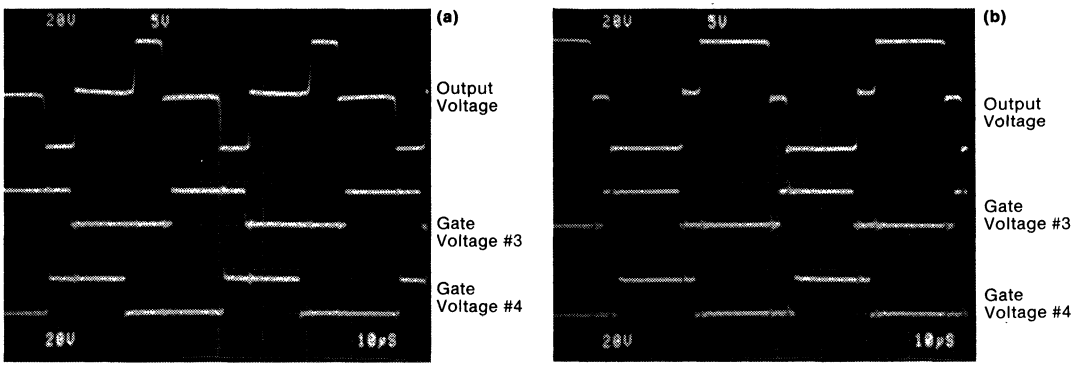
Figure 15. Output voltage and current of BIMOS bridge circuit with 650V DC input
(a) "Partial" output voltage
(b) "Full" output voltage

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Figures 16(a) and (b) show the output voltage and gating pulses for BIMOS switches No's 3 and 4 at partial and full ouput voltage respectively.

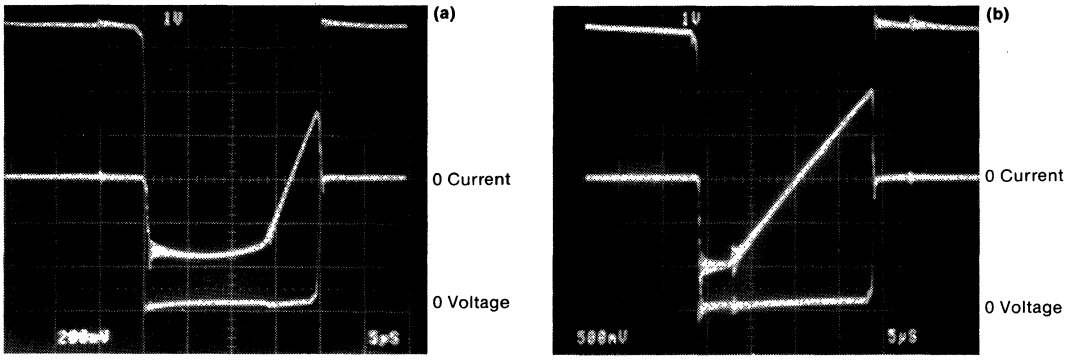
Figure 17 shows voltage and current waveforms for the No. 1 BIMOS switch/feedback diode combination, at partial and full output voltage. Note the relatively long period of "negative" freewheeling current in the feedback diode at partial output because of the relatively short period of the "active" output voltage pulse.

Figure 18 shows an expanded trace of voltage and current for the No. 1 BIMOS switch/feedback diode combination, during the time that the No. 3 switch turns off, forcing inductive load current into the No. 1 feedback diode.



Upper: 500V/div 10μs/div
Middle: 20V/div Lower: 20V/div

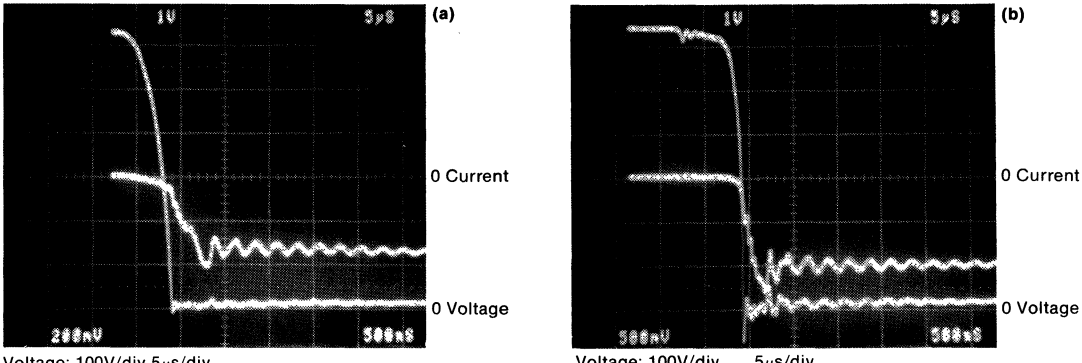
Figure 16. Output voltage and gate drive voltages for BIMOS bridge. 650V DC input. (a) "Partial" output voltage (b) "Full" output voltage



Voltage: 100V/div 500ns/div
Current: 2A/div

Voltage: 100V/div 500ns/div
Current: 5A/div

Figure 17. Voltage and current for BIMOS switch/feetback diode combination. 650V DC input.
(a) "Partial" output voltage (3A peak at switch-off) (b) "Full" output voltage (10A peak at switch-off)

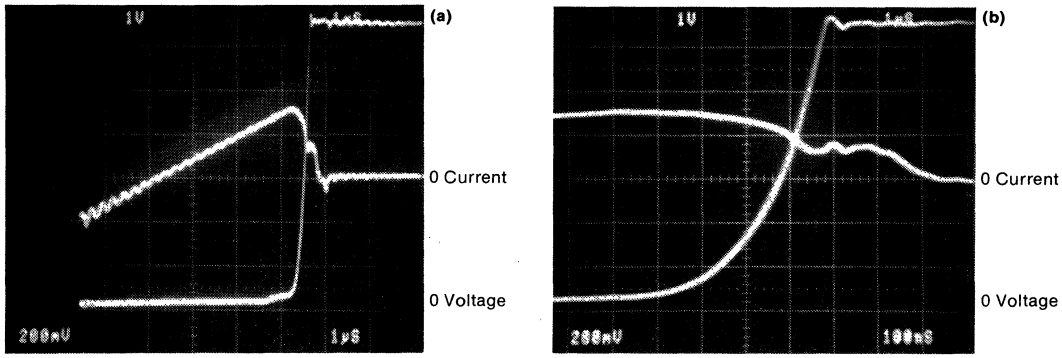


Voltage: 100V/div 5μs/div
Current: 2A/div

Voltage: 100V/div 5μs/div
Current: 5A/div

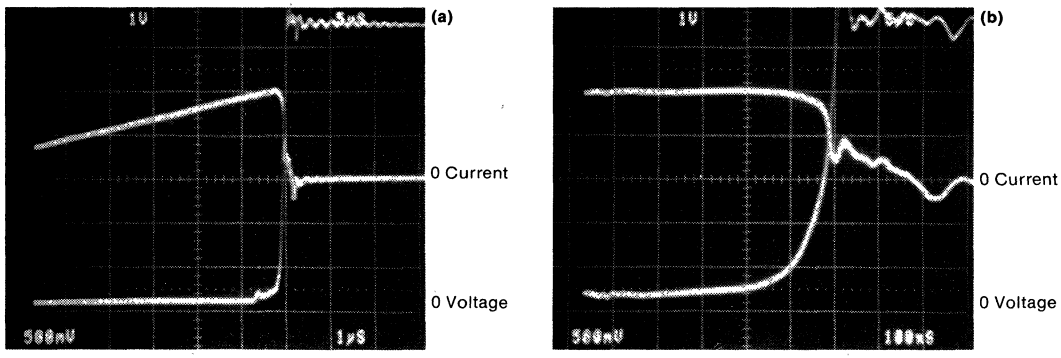
Figure 18. Voltage and current for No. 1 BIMOS switch/feedback diode combination when No.3 turns-off and current commutates into No. 1 feedback diode. 650V DC input.
(a) "Partial" output voltage (3.5A peak at commutation) (b) "Full" output voltage (10A peak at commutation)

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Voltage: 100V/div Current: 2A/div

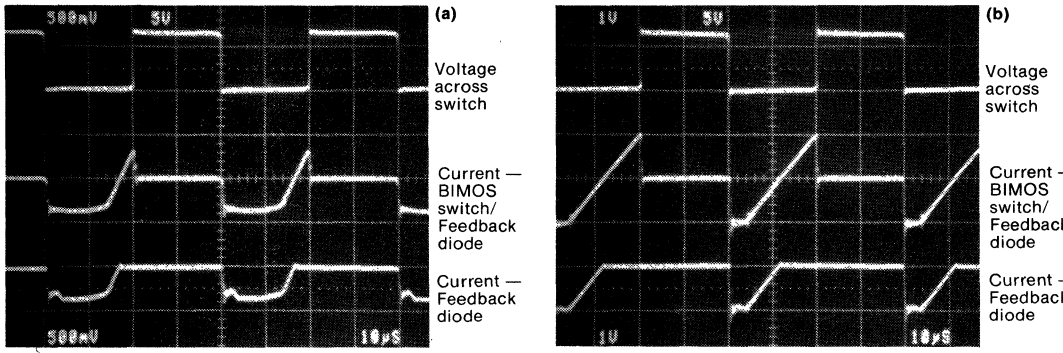
Figure 19. Voltage and current for BIMOS switch at partial output voltage when switching off 3A.
(a) 1μs/div (b) 100ns/div 650V DC input.



Voltage: 100V/div 1μs/div Current: 5A/div

Voltage: 100V/div 100μs/div Current: 5A/div

Figure 20. Voltage and current for BIMOS switch at full output voltage when switching off 10A.
(a) 1μs/div (b) 100ns/div 650V DC input.



Upper: 500V/div 10μs/div
Middle: 5A/div Lower: 5A/div

Upper: 500V/div 10μs/div
Middle: 10A/div Lower: 10A/div

Figure 21. Voltage and current waveforms for BIMOS switch and feedback diode (No. 1) 650V DC input.
(a) "Partial" output voltage (b) "Full" output voltage

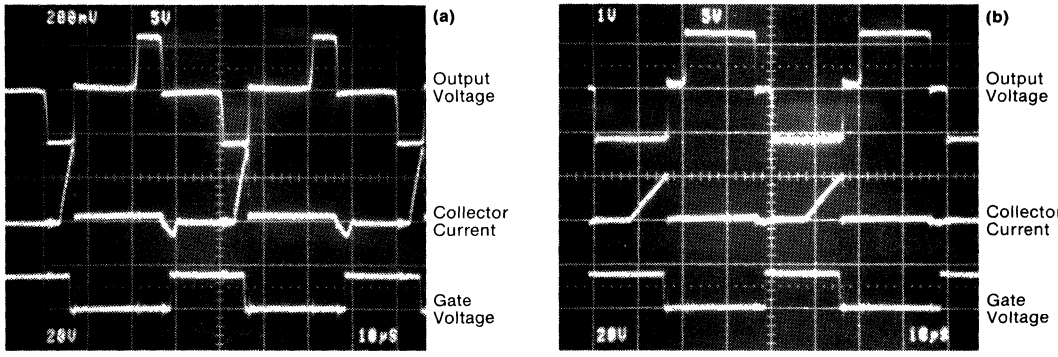
Figure 19 shows voltage and current waveforms for the BIMOS switch at partial output voltage, when turning off 3A. The storage time is approximately 600ns, and the sum of the voltage rise and current fall times is about 500ns.

Figure 20 shows similar waveforms at full output voltage, when turning off 10A. The storage time is about 500ns, and the sum of the voltage rise and current fall times is about 300ns.

Note that the current waveforms in Figures 19 and 20 *include* the current in the clamping circuit D3, C2, R3 (Figure 11). The current fall-times seen in these oscillograms are therefore *greater* than for the BIMOS switch itself.

Figure 21 shows waveforms of voltage and current for the No. 1 BIMOS switch/feedback diode combination, and the waveform of current for the feedback diode by itself. Note the "notch" of current "missing" from the feedback diode current waveform. The "missing" current flows through the base-collector junction of the bipolar transistor, as explained below.

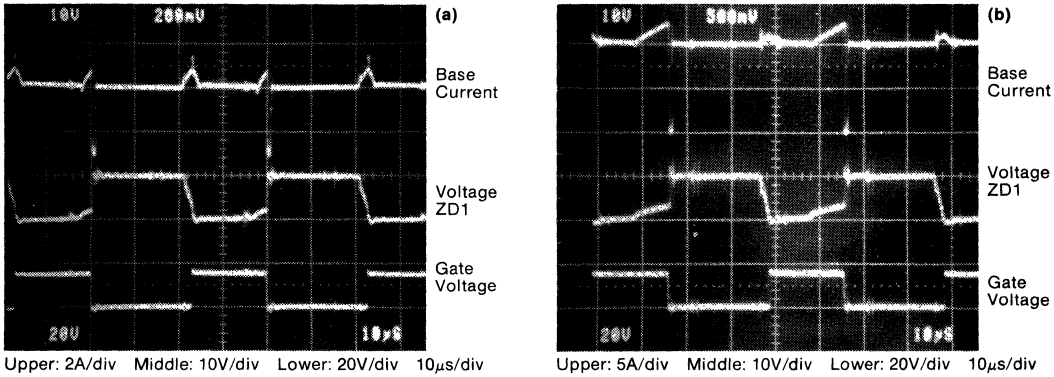
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Upper: 100V/div 10μs/div
Middle: 2A/div Lower: 20V/div

Upper: 500V/div 10μs/div
Middle: 10A/div Lower: 20V/div

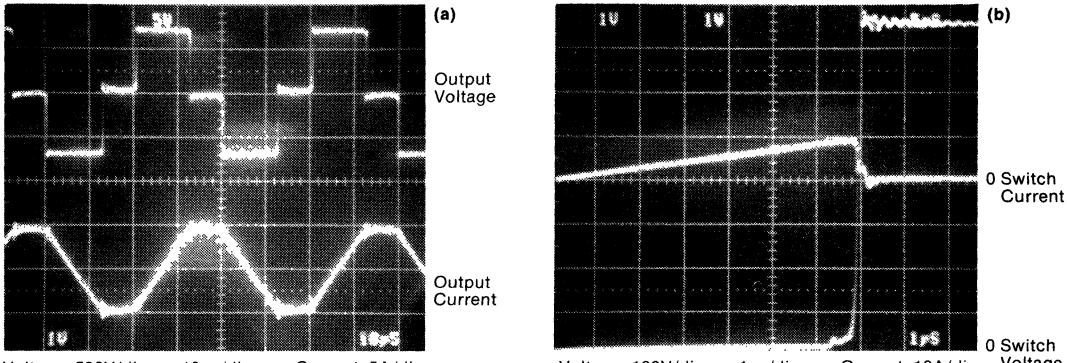
Figure 22. Output voltage, collector current, and gate voltage waveforms. (Switch No. 1) 650V DC input.
(a) "Partial" output voltage (3A peak) (b) "Full" output voltage (10A peak)



Upper: 2A/div Middle: 10V/div Lower: 20V/div 10μs/div

Upper: 5A/div Middle: 10V/div Lower: 20V/div 10μs/div

Figure 23. Base current, zener voltage, and gate voltage waveforms for BIMOS switch. 650V DC input.
(a) "Partial" output voltage (b) "Full" output voltage



Voltage: 500V/div 10μs/div Current: 5A/div

Voltage: 100V/div 1μs/div Current: 10A/div

Figure 24. Waveforms of (a) Output voltage and current and (b) Switch voltage and current at turn-off. 750V DC input

Figure 22 shows waveforms of output voltage, collector current, and gate voltage for BIMOS switch No. 1. Note the negative collector current notches — the "missing" feedback diode current notches referred to above — which occur just after the opposite device in the same inverter leg has turned OFF, but before the No. 1 HEXFET is gated ON. During this period, the inductive load current flows through the bipolar transistor's collector base junction, which is forward biased by the voltage on the capacitor C1. By the time the HEXFET is gated ON, whatever charge still remains on capacitor C1 is rapidly discharged through the HEXFET, and the load current transfers into the feedback diode (D4).

Figure 23 shows waveforms of base current, zener voltage, and gate voltage for BIMOS switch No. 1. The "notch" of base-collector current referred to above can be seen on the base current waveform. This notch of current substantially discharges capacitor C1 by the time the HEXFET is gated ON.

Figure 24 shows waveforms of out-

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Table 4. Comparisons Between Alternative Devices

	BIMOS SWITCH	HIGH VOLTAGE HEXFET	GTO
Maximum voltage capability	1000V	1000V	1800V
Switching speed	Fast 40ns to 250ns fall time 180ns to 1μs storage	Very Fast 50 to 100ns fall time No storage	Moderate 1 to 2μs fall time 1μs storage
Voltage drop	Moderate	High	Low
Snubber energy	Low	Low	High
Relative efficiency	Good at intermediate to high frequency	Good at high frequency. Moderate at low frequency.	Good at low frequency. Poor at high frequency.
Overload capability	Poor	Good	Good
Drive Circuitry	Simple	Simple	Complex
Relative cost	Low/moderate	High	Low

Table 5. Approximate Cost Comparison

	850V 10A BIMOS		850V 10A HEXFET	850-1500V 10A GTO
Basic Device Cost	2N6547	$2.90	$20.00*	$4.00*
	IRF131*	2.00		
Other circuit components	3.60		0.50	0.70
Drive circuitry (isolated)	0.50		0.50	3.00
Total $	9.00		21.00	7.70

*Estimated 10K piece price, 1984

put voltage, output current, and voltage and current for the No. 1 BIMOS switch at turn-OFF, with a DC input voltage of 750V. The peak load current is about 10A. These waveforms are included to demonstrate the solid capability of the BIMOS switch to operate at a voltage close to the V_{CBO} rating of the bipolar — and actually represent a slight excursion beyond the limits of the common base Safe Operating Area shown in Figure 3 for the 2N6547.

Comparison With Alternatives

Alternative candidate devices to the BIMOS switch are (a) a single high voltage HEXFET (or two HEXFETs connected in series, which would have approximately similar characteristics) and (b) a gate turn-off thyristor (GTO).

Each of the three alternatives has its own particular features, and each will find use in the applications in which it best fits. A comparison between the most salient features of a BIMOS switch, a high voltage HEXFET, and a GTO is given in Table 4. Table 5 gives an approximate comparison of component costs; this provides an indication of relative costs, and is not exact. It does not include circuit assembly costs, which will have a modifying effect, but will not greatly alter the relative comparison.

The following general summary can be made:

(a) A high voltage HEXFET (or two HEXFETs connected in series) offers the fastest switching speed, and therefore has the greatest advantage at high frequency (say 200kHz and above). For lower frequency it will generally not be the best choice for applications requiring 850-1000V rating, because voltage drop and cost are relatively high.

(b) The GTO offers the highest voltage capability — up to 1800V — and will generally be the best choice for applications that require device voltage ratings substantially in excess of 1000V, provided that the operating frequency is not too high — say 10 to 15kHz maximum. (It is to be noted, however, that the GTO *can* be operated at higher frequency, perhaps up to 50kHz, by operating at reduced current and/or voltage. But cost per switching volt-ampere then increases significantly.)
Switching speed of the GTO at normal "rated" conditions is relatively slow, and snubber energy is relatively high, Snubber losses per device could typically be 50W for a GTO switching 10A at 700V, at 10kHz — unless a complex "lossless" snubber circuit is used. Drive circuitry for the GTO is also relatively complex.

(c) The BIMOS switch offers higher frequency than the GTO, up 100 or 200kHz, with relatively good efficiency. Its cost is significantly lower than for a high voltage HEXFET, but higher than for a GTO. Several discrete components are needed to make a BIMOS switch, which is a disadvantage, but external drive circuitry is simple.

Another possibility, not included in the above comparison, would be a cascode connection of GTO and low voltage HEXFET. This would offer higher voltage capability than the BIMOS switch, but would have slower switching speed, higher losses, and probably somewhat higher cost. It would have the advantage over the GTO on its own of much simpler external drive circuitry, and improved switching speed.

Conclusion

The BIMOS switch should be considered as a serious candidate for applications requiring device voltage ratings up to 1000V, operating frequency up to one or two hundred kilohertz, and power levels up to tens of kilowatts. □

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Linear Power Amplifier Using Complimentary HEXFETs®

By Peter Wilson

Introduction

The class AB amplifier described in this application note uses a complementary pair of HEXFET devices as the output stage. This feature offers performance improvements over the equivalent bipolar output stage and allows a reduction in the complexity of the driver circuit, the output devices being driven by a single class A driver.

The design described will deliver 60W rms into a 4 ohm load when working from ±30V supplies. The bandwidth is in excess of 100kHz, but may be tailored to the user requirements by making component value changes.

Circuit Description

The amplifier circuit diagram is shown in Figure 1, and the components listing in Table 1. Split power supply rails ($\pm V_{DD}$) are used, giving improved rejection of power supply ripple and allowing the load, R_{load}, to be direct coupled. The output devices Q_5, Q_6, operate in source follower configuration. This offers a twofold advantage; a) the possibility of oscillation in the power output stage is reduced as the voltage gain is less than unity and b) signal feedback through the heatsink on which the devices are assembled is eliminated as the drain terminal, which is electrically connected to the tab on the TO220 package, is at dc voltage.

Symmetrical output is achieved by providing "bootstrapped" drive to the gate of the n-channel device, Q_5, from the output. The use of the bootstrap circuit, C_4, R_8, R_9 also allows the driver transistor, Q_4, to operate at near constant current which improves the linearity of the driver stage. The diode D_1 acts as a clamp for the bootstrap circuit, restricting the positive voltage at the gate of Q_5 to $+V_{DD}$. This allows symmetry to be maintained under overload conditions.

Transistor Q_3 and resistors R_{11}, R_{12}, R_{13} provide gate-source offset voltage for the output devices. R_{12} is variable, allowing adjustment of the output quiescent current for variation in HEXFET threshold voltage. A degree of temperature compensation is built into the circuit as both the bipolar transistor, Q_3, emitter base voltage and the combined threshold voltages of the HEXFETs, Q_5, Q_6 have a temperature coefficient of -0.3%/°C.

The class A driver transistor, Q_4, operates at a bias current determined by resistors R_8, R_9, nominally 5mA. Q_4 is driven by a PNP differential input pair, Q_1, Q_2. The bias current in the input stage is set to 2mA by

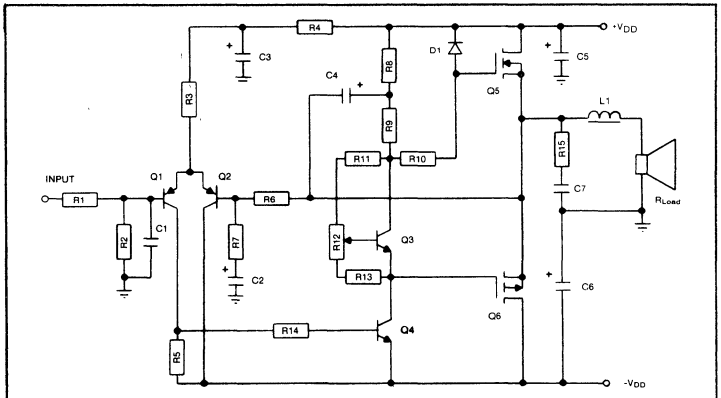


Figure 1. Class AB Amplifier Circuit Diagram

Table 1. Components List

R_1	4.7KΩ	R_9	2.7KΩ	C_1	220pF	Q_1,Q_2,	2N4356,2N5086 or equivalent
R_2	47KΩ	R_{10}	680Ω	C_2	100μF 10V		
R_3	15KΩ	R_{11}	10KΩ	C_3	47μF 40V	Q_3,Q_4,	2N4410,2N5088 or equivalent
R_4	1.2KΩ	R_{12}	1KΩ Pot.	C_4	47μF 40V		
R_5	560Ω	R_{13}	820Ω	C_5	2200μF 40V	Q_5	IRF532
R_6	47KΩ	R_{14}	4.7KΩ	C_6	2200μF 40V	Q_6	IRF9532
R_7	470Ω	R_{15}	10Ω 1W	C_7	68nF	D_1	1N4002
R_8	2.7KΩ	R_{load}	8/4Ω	L_1	3μH aircored		

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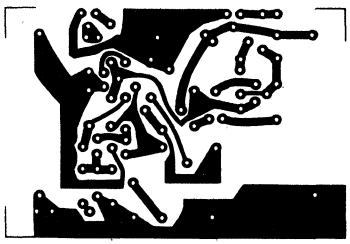
resistor R_3. Negative feedback from the output of the amplifier is fed to the base of Q_2 by resistor R_6. Components R_7, C_2 set the closed loop gain of the amplifier (R_6/R_7) and provide low frequency gain boosting. The additional components R_{15}, C_7 connected between the output node and ground suppress the high frequency response of the output stage, allowing the h.f. performance of the amplifier to be determined by the input circuit. Components R_1, R_2, C_1 at the input of the amplifier define the input impedance (47Kohm) and suppress noise.

The amplifier input stage requires additional power supply ripple suppression which is provided by components R_4, C_3.

Additional circuit components have been added to ensure high frequency stability of the complete amplifier. Placement of the components and component values will depend to some extent on the printed circuit board layout. The following rules should be followed when designing the printed circuit board:

(a) A 'common ground' principle should be adopted, i.e., power supply decoupling capacitors, load and input stage biasing components should all be taken to ground in close proximity, eliminating the effects of common node ground current. Similarly, a "common output node" should be used, the load, feedback resistor and h.f. suppression components being taken from a common point on the pcb.

Copper Side



Component Side

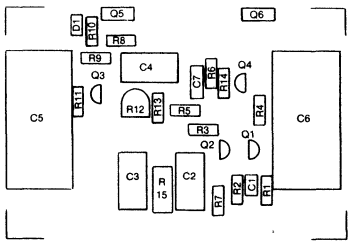


Figure 2. Amplifier Printed Circuit Board Layout

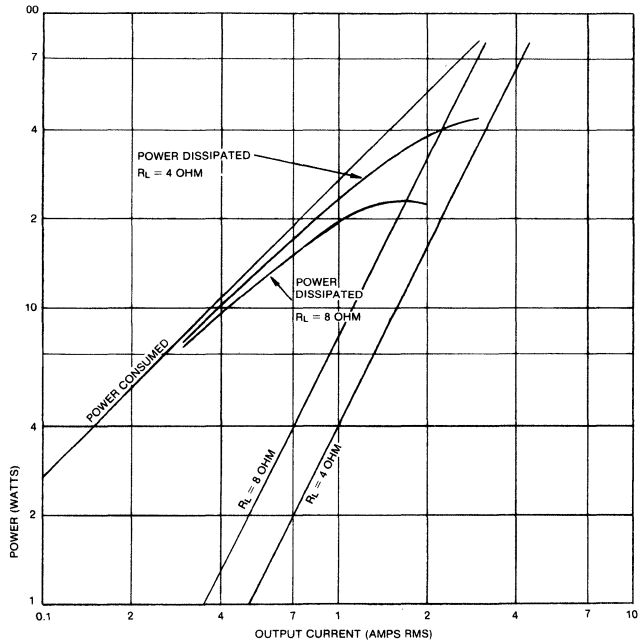


Figure 3. Power Curves for the Amplifier with 4 and 8 Ohm Loads and ±30V Power Supplies

(b) The length of connecting lead to the gate terminals of HEXFETs Q_5, Q_6 should be an absolute minimum to avoid oscillation of the power output stage. A series gate resistor, R_{10}, may be used to suppress oscillation, but too high a resistor value will limit the slew rate. Oscillation of the amplifier caused by capacitive coupling to the base of the driver transistor, Q_4, is suppressed by the addition of a series resistor, R_{14}.

(c) Phase shift in the amplifier when driving a reactive load can lead to high frequency instability. With a capacitive load, the addition of a small, air-cored choke (3μH with an 8 ohm, 2μF load) will restore stability. The final value of the choke is defined by experiment.

Figure 2 shows a printed circuit layout which can be used for the circuit shown in Figure 1. The preceding design rules have been followed.

Amplifier Performance

(a) *Output Power:* To achieve 60W rms into a 4 ohm load, the current in the load is 3.9A rms or 5.5A pk. This information is derived from equations (1) and (2):

$$P_O = I^2_{rms} R_{load} = \frac{V^2_{rms}}{R_{load}} \quad (1)$$

$$I_{rms} = \frac{I_{pk}}{\sqrt{2}} \quad (2)$$

$$V_{rms} = \frac{V_{pk}}{\sqrt{2}} \quad (3)$$

Also from equation (1), the voltage developed across the load at 60W output is 15.5V rms or 22V pk. To sustain a source current of 5.5A, the n-channel HEXFET, IRF532, requires a gate source voltage of 5V. One can conclude that the gate bias voltage to achieve peak power in the positive sense is $V_{pk} + V_{gs} = 27V$. A similar calculation for the negative peak, using the P channel HEXFET, IRF9532, shows that a negative gate bias supply of -28V is required.

Consequently, a ±30V supply will be adequate for a 60W output, provided that the supply voltage does not fall below ±28V when loaded, i.e., the power supply impedance should be better than 1 ohm. The

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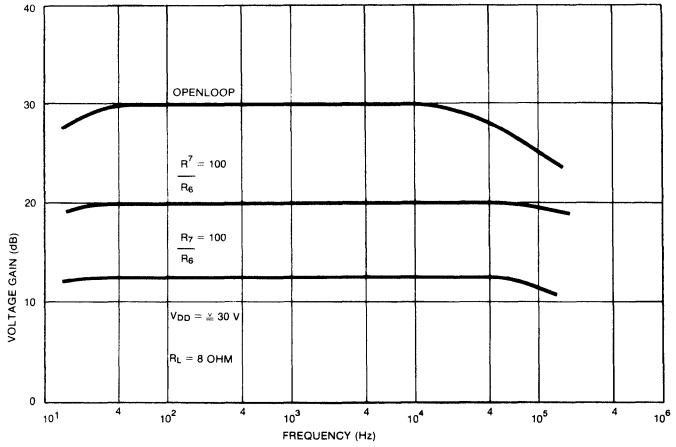


Figure 4. Amplifier Open and Closed Loop Frequency Response Curves

relationship between the power delivered to the load and the power absorbed from the supply is shown in Figure 3, assuming a sinusoidal waveform and a ±30V supply. The curve representing the power delivered to the load can be easily plotted with the help of equation (1) for different values of load current.
The power absorbed from the supply has been plotted with the help of the following relationship:

$$P_S = (V_{avg})(I_{avg})$$

$$= (2V_{DC})\left(\frac{\sqrt{2}}{\pi} I_{rms}\right) \qquad (4)$$

The difference between the two is the power dissipated in the HEXFETs and as it can be seen from Figure 3, it has a peak of approximately 46W. Assuming a maximum ambient temperature of 55°C, the total thermal resistance between the junction of the two HEXFETs and the ambient will have to be less than 2°C/W. Considering that the IRF532 and IRF9532 have a thermal resistance between junction and case of 1.67°C/W each, the maximum case temperature will have to be less than 110°C and the thermal resistance of the heatsink will have to be less than 1.16°C/W to ambient.

(b) *Frequency Response:* Open loop and closed loop frequency response curves for the amplifier are shown in Figure 4. The open loop gain, measured with gate and source connections to the HEXFETs broken, is 30db, -3db points occurring at 15 Hz and 60kHz. Closed loop curves are shown for amplifier gains of 100 (R_7 = 470 ohm) and 20 (R_7 = 2.2K ohm). In both instances the curves remain flat to within +1db between 15 Hz and 100kHz with an 8 ohm load. The slew rate of the amplifier, measured with a 2V pk-pk square wave input is 13V/μs positive going and 16V/μs negative going. The discrepancy could be balanced out by addition of a series gate resistor for Q_6.

(c) *Total Harmonic Distortion:* The fidelity of the amplifier is shown in the distortion curves, Figure 5, and is limited by the loop gain. Reduction of the closed loop gain from 100 to 20 produces a significant improvement in distortion figure. The output stage quiescent current was adjusted to 100mA and can influence the distortion measurement significantly if allowed to fall below 50mA.

(d) *Quiescent Operating Conditions:* The dependence of the quiescent current in the output stage and of the output offset voltage on power supply voltage are illustrated in Table 2. The quiescent current is set by first adjusting the potentiometer, R_{12}. for minimum offset voltage - turned fully anticlockwise if the pcb layout in Figure 2 is used - and applying the power supply voltage, the positive supply passing through an ammeter with 1A f.s.d. R_{12} is then adjusted until the meter reading is 100mA with ±30V supplies. The meter should be removed from circuit before applying an input signal to the amplifier.

Power Supply Requirement

A simple line derived power supply suitable for the class AB amplifier is illustrated in Figure 6. The ±30V supplies are taken from the center-tapped secondary of the line transformer.
The 2200μF supply decoupling capacitors, C_5, C_6, (Figure 1) which

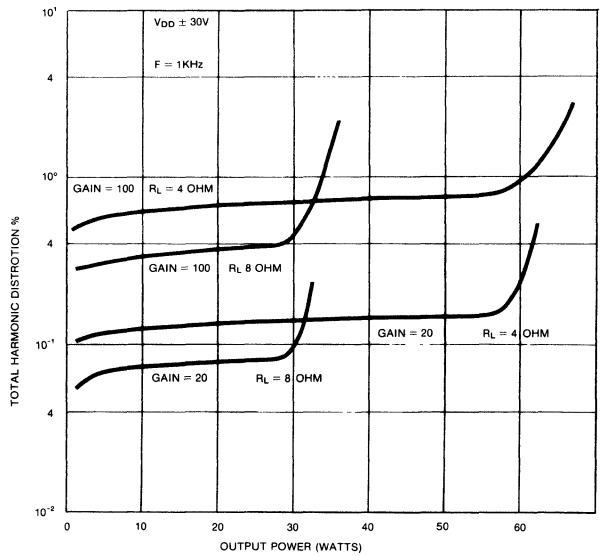


Figure 5. Amplifier Total Harmonic Distortion Curves

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should be mounted as close as possible to the amplifier output stage, reduce the supply frequency ripple to 5.5V pk-pk at full load.

Setting up Procedure and Faultfinding

It is unlikely that any experienced experimenter will have difficulty in achieving satisfactory results when building an amplifier to this design. The printed circuit board shown in Figure 2 is intended to assist in this respect. The major problems anticipated are those associated with the faulty assembly of components and damage to the HEXFETs through handling or circuit oscillation.

The following troubleshooting checklist is offered as a guide to the experimenter:

1. When assembling the printed circuit board, mount the passive components first, ensuring the correct polarity of electrolytic capacitors. Then solder in the transistors Q_1 - Q_4 checking for correct pin identification. Finally, mount the HEXFETs, avoiding static discharge by shorting the pins together to ground and using a grounded soldering iron. Check the assembled board for correct component placement. A component side overlay as shown in Figure 2 is useful for this purpose. Check the copper side of the board for solder bridges between tracks, and remove them. Check for dry solder joints visually and electrically using a resistance meter and rework, if necessary.

2. Power can now be applied to the amplifier and the output stage quiescent current set to between 50 and 100mA. The potentiometer, R_{12} is first adjusted for minimum offset (fully anticlockwise on the pcb layout in Figure 2). An ammeter is connected in series with the positive supply and selected to read 1A f.s.d R_{12} is adjusted until the ammeter reads between 50mA and 100mA. Quiescent current setting can be performed without the load connected. If, however, a loudspeaker load is connected in circuit, it can be protected by a fuse from dc overload. With the quiescent current set, the output offset voltage can be confirmed to be less than 100mV. Excessive and erratic variation in quiescent current as R_{12} is adjusted are indicative of circuit oscillation or faulty wiring. The solutions described in "Circuit Description" (series gate resistors, minimized gate wiring and common earthing) should be adopted. Also, supply decoupling capacitors should be mounted in close proximity to the amplifier output stage and load ground point. Quiescent current setting should be performed with the HEXFETs mounted on their heatsink to avoid overdissipation.

3. With the quiescent current set, the ammeter should be removed from the positive supply and a signal can be applied to the amplifier input. Signal requirements for full rated output are:

gain = 100:
$R_L = 4\ \Omega$, $V_{in} = 150$mV rms
$R_L = 8\ \Omega$, $V_{in} = 160$mV rms
gain = 20:
$R_L = 4\ \Omega$, $V_{in} = 770$mV rms
$R_L = 8\ \Omega$, $V_{in} = 800$mV rms

"Clipping" of the output waveform when operating at rated power indicates poor supply regulation and can be remedied by reducing the input signal amplitude and derating the amplifier. Alternatively, a lower impedance supply should be used. The frequency response of the amplifier can be checked over the frequency range 15 Hz - 100kHz with the aid of an audio test set or signal generator and oscilloscope. Distortion of the output waveform at high frequency is indicative of a reactive load and adjustment of the output choke will be required to restore the waveform. The high frequency response may be tailored with a compensation capacitor in parallel with R_6. The low frequency response is controlled by components R_7,C_2.

4. Hum pickup will be more likely to occur in a high gain circuit. Pickup at the high impedance input is minimized by use of a shielded cable, grounded at the signal source. Supply frequency ripple injected through the supply to the input stage of the amplifier can be detected across capacitor, C_3. This is attenuated by the common mode rejection ratio of Q_1, Q_2 before being amplified. However, if this is the source of hum, adjustment to the values of C_3, R_5 can be made to suppress the signal amplitude.

5. In the event of the output stage being destroyed, either through short circuit load or h.f. oscillation, both HEXFETs should be replaced. It is

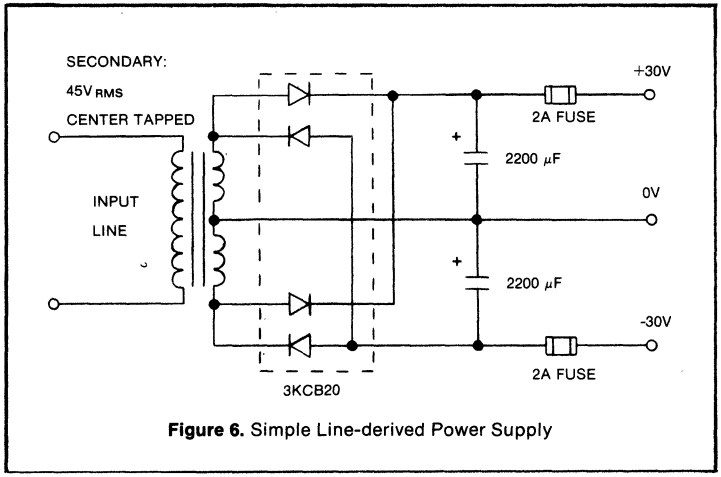


Figure 6. Simple Line-derived Power Supply

Table 2. Variation in Output offset voltage and Output quiescent current with supply voltage

Supply Voltage $\pm V_{DD}$ V	Output Offset V_{OS} mV	Output Quiescent Current I_q mA
35	-40	135
30	-20	100
25	+4	75
20	+30	54

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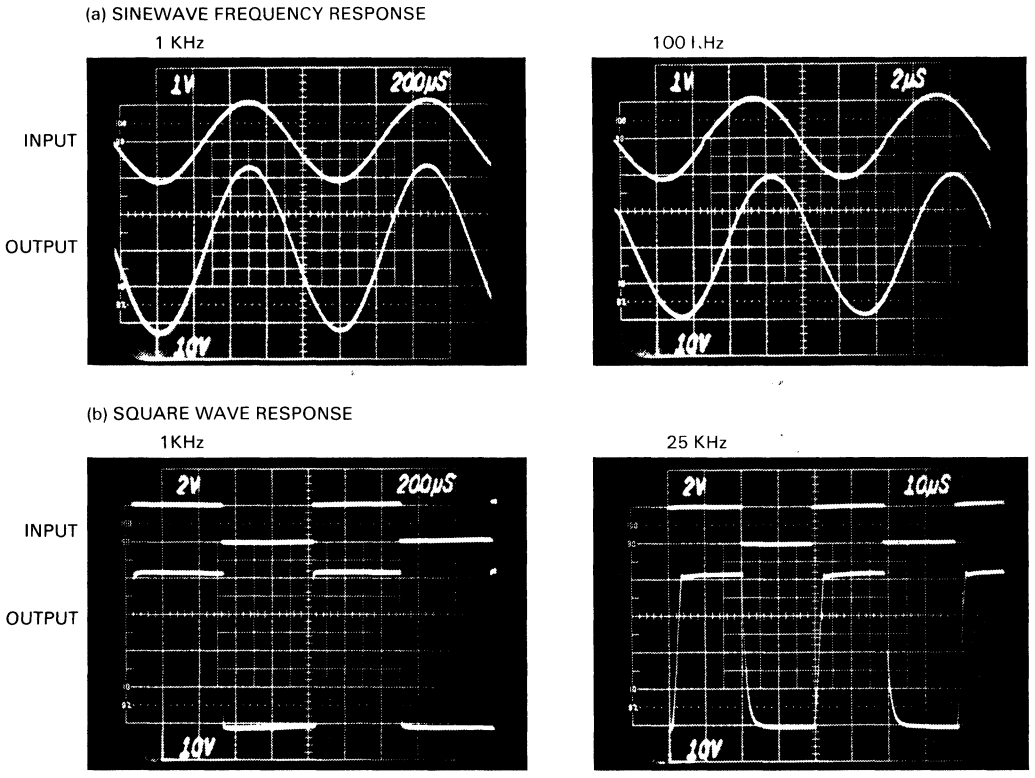


Figure 7. Amplifier Waveforms illustrating Frequency Response

unlikely, however, that other circuit components will have been affected. The setup procedure should, of course, be repeated with the new devices in circuit.

Performance Summary

Using a complementary pair of HEXFETs, IRF532 and IRF9532 and with a ±30V supply, the following performance can be achieved:

Maximum rms output power:

60W into 4Ω
32W into 8Ω

Bandwidth:

15 Hz to 100kHz ±1db

Total harmonic distortion (1kHz):

0.15% at 60W into 4Ω
0.08% at 32W into 8Ω

Voltage gain:

Adjustable, ×100 to ×20

Input impedance: 47KΩ

Figure 7 illustrates the amplifier response to 1kHz and 100kHz sine-wave input signals and also the square wave response at 1kHz and 25kHz.□

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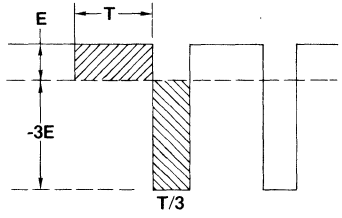
Transformer-Isolated HEXFET® Driver Provides very large duty cycle ratios

(HEXFET is the trademark for International Rectifier Power MOSFETs)

By P. WOOD

Transformer coupling of low level signals to power switches offers several advantages such as impedance matching, DC isolation and either step up or step down capability.

Unfortunately, transformers can deliver only AC signals since the core flux must be reset each half cycle. This "constant volt seconds" property of transformers results in large voltage swings if a narrow reset pulse, i.e., a large duty cycle is required (Figure 1).



NOTE: VOLT-SECONDS PRODUCT IN SHADED AREAS MUST BE EQUAL. THIS CAUSES RESET VOLTAGE TO BE 3 TIMES APPLIED VOLTAGE E.

Figure 1. Constant-Volt-Seconds Characteristics of Transformers

For this reason, transformers in semiconductor drive circuits are limited to 50% duty cycle or roughly equal pulse widths positive and negative because of drive voltage limitations of the semiconductors themselves.

For large duty cycle ratios designers must choose an alternative to the transformer, such as an optical coupler to provide the necessary drive isolation.

These devices have poor noise immunity, high impedance output and require additional floating power sources which add complexity.

When a power HEXFET is used for the power switch, the high output impedance of optical couplers is less of a problem because the HEXFET power MOSFET does not require drive current in the ON or OFF states. Switching speed, however, is seriously comprised by C_{iss} if a high impedance driver is used.

The circuit in Figure 2 provides a low impedance answer during the switching intervals, and a duty cycle ratio of 1-99%; furthermore, it can have any desired voltage ratio, and provides electrical isolation!

In Figure 2, Q2 is a power HEXFET providing the switching function for a switching power supply, motor drive or other application requiring isolation between the low level logic and high power output. Q1 is a low power HEXFET such as the IRFD1Z1, which is used to control the drive signals to Q2, and T1 is a small 1:1 driver transformer providing electrical isolation from, and coupling to, the low level circuitry.

The waveforms in Figure 3 explain the circuit operation. Waveform A is the desired logic signal to be switched by Q2. When this voltage is applied to the primary of T1 the waveform is supported by changing core flux until saturation occurs as shown in waveform B. At this time the winding voltages fall to zero and remain so until

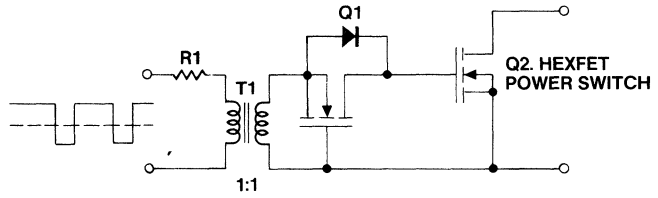


Figure 2. Wide Duty Cycle HEXFET Driver Circuit

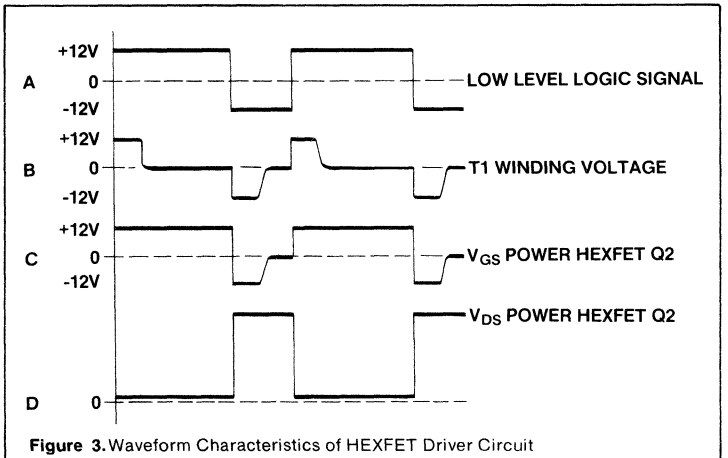


Figure 3. Waveform Characteristics of HEXFET Driver Circuit

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the core flux is reversed by the negative-going portion of waveform A. Saturation will again occur if the negative-applied pulse exceeds the volt-seconds capability of the core.

During the positive portion of the secondary waveform, which, of course, has the same form as the primary, the intrinsic diode of Q1 is in forward conduction and Q2 receives a positive gate drive voltage with a source impedance of R1 plus the intrinsic diode forward impedance. In a practical circuit this can be less than 10 Ohms total, with a consequent turn-on time of around 75nsec.

When T1 saturates, the intrinsic diode of Q1 isolates the collapse of voltage at the winding from the gate of the power HEXFET and the input capacitance C_{iss} of the power switch holds the gate bias at the fully enhanced condition for a time limited only by the gate leakage current of Q2 as indicated in Figure 3c.

When waveform A goes 12 volts negative Q1 will become fully enhanced; and the main switch Q2 will now be turned off at approximately -12V at a source impedance R1 + $R_{DS(ON)}$ of Q2. This will again be less than 10 Ohms and will yield a turn-off time less than 100nsec.

When T1 again saturates, during the negative half cycle, its winding voltages fall to zero and Q1 turns off. As T1 voltage collapses, the gate of Q2 also follows this voltage and remains at zero bias. The drain voltage of the power HEXFET Q2 appears in Figure 3d, showing that it is indeed a mirror image of waveform A, the desired low level logic signal. Note that because T1 need only support a 12V signal, for 1 μsec or less, it is very small — and inexpensive.

There are many circuits where power HEXFETs are replacing bipolar transistors, and this one illustrates an important feature of HEXFETs not shared by bipolars, namely the insignificant gate currents required to achieve full conduction — so small, in fact, that the ON or OFF bias levels can be stored in the gate-to-source capacitance!

A few examples of possible circuit applications are shown in Figures 4, 5, and 6.

It should be noted with reference to Figure 3b that the gate-source voltage of Q2 in the OFF state returns to zero when T1 saturates. For most applications, the noise immunity provided by the threshold voltage of Q2 is sufficient ($2V<V_{TH}<4V$). In some applications it may be desirable to provide more noise immunity. This can be achieved merely by adding another small N-Channel HEXFET (typically an IRFD1Z1) as shown in Figure 7.

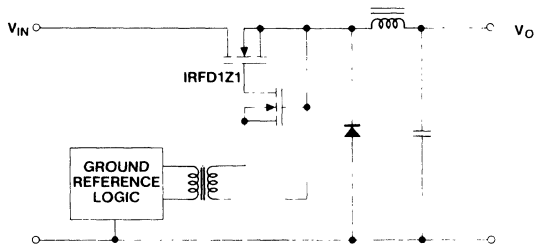


Figure 4. Single Switch Regulators

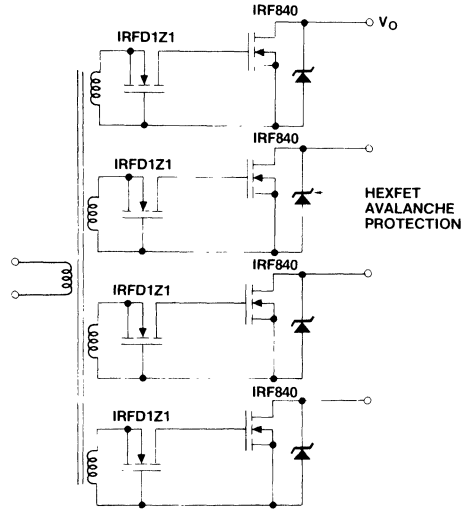


Figure 5. High Voltage, High Power HEXFET Switch (500V, 8A per Section)

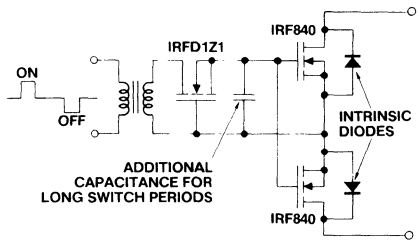


Figure 6. Bi-directional AC Switch using HEXFETs

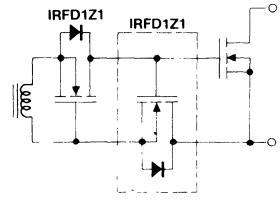


Figure 7. HEXFET Driver Circuit with additional Noise Immunity

The circuit now provides -12V to the power MOSFET *after the transformer saturates,* and this reverse bias remains until the next positive half cycle of drive. Thus, a minimum of 14V noise immunity is provided which should be adequate for all applications. Cost of the HEXFETs used in Figure 7 is minimal, and these are available in 4-pin HEXDIP packages, which can be stacked side by side in standard DIP sockets.

Conclusion

As described in this application note, the circuit in Figure 7 offers a simple and inexpensive way to drive HEXFETs. It is especially useful where isolated drives with variable ON-OFF ratios are needed, and which are difficult to accomplish with conventional transformers or optical isolators. □

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Custom Assembly of HEXFET® Dice

Introduction

This application note describes the HEXFET transistors available from International Rectifier in die form. These power MOS field effect transistor dice feature the same high reliability planar technology used for the IRF series of TO-3, TO-220, TO-39 and HEX-Dip packaged HEXFETs. The same advanced MOS processing techniques, silicon gate structure, and efficient hexagonal source pattern are available in die form for hybrid assembly. As the name implies, the HEXFET consists of an hexagonal cell structure which results in a packing density of over 500,000 cells per square inch. Use of a silicon-gate design and state-of-the-art MOS processing techniques result in an extremely reliable device which is highly reproducible in various die sizes. Hybrid packaging of such die results in substantial savings in weight and volume compared to standard packaging.

Die Characteristics

Six HEXFET die sizes presently available from International Rectifier are summarized in Table 1. These are termed HEX-Z (43 mil x 35 mil), HEX-1 (91 mil x 69 mil), HEX-2 (137 mil x 87 mil), HEX-3 (175 mil x 115 mil), HEX-4 (227 mil x 170 mil), and HEX-5 (257 mil x 257 mil). The majority of die sizes are available in eight voltage ranges, with the exception of the P-Channel devices (see Table 2), at corresponding on-resistances. All die sizes have one gate and one source bonding pad as shown in Figures 1 through 6. Each HEXFET die is individually probed at room ambient temperature to the electrical specifications shown in Tables 2 and 3.

Because of limitations when electrically probing in wafer form, some of the generic specifications of the equivalent packaged device cannot be tested and guaranteed in die form. These are power dissipation, P_D, safe operating area, SOA, thermal resistance, R_{thJC}, on-resistance at rated current, $R_{DS(on)}$, and inductive current, I_{LM}. (On-resistance at I_D = 1A is tested and guaranteed according to Tables 2 and 3. These parameters are dependent upon the user's assembly technique. However, the following characteristics are guaranteed by design to meet the specifications of the equivalent part: g_{fs}, C_{iss}, C_{oss}, C_{rss}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f, and $T_{J(max)}$. Consult the appropriate data sheet from each table.

Following electrical probing, the dice are inked for identification and scribed. The dice are mechanically separated, 100% visually inspected, and packed for shipment.

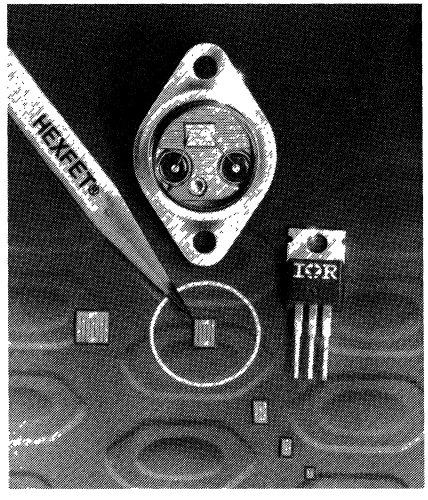
Dimensional Tolerances (Table 1.)

Bonding Pad L or W:
< 0.025 in., Tolerance = ±0.0005 in.
⩾ 0.025 in., Tolerance = ±0.001 in.

Overall Die L or W:
< 0.050 in., Tolerance = ±0.004 in.
⩾ 0.050 in., Tolerance = ±0.008 in.

Table 1. HEXFET Die Dimension Summary with Photo Showing Size Relationship (HEX-4 circled)

HEXFET DIE DIMENSIONS		HEX-Z	HEX-1	HEX-2	HEX-3	HEX-4	HEX-5
L	inch	0.043	0.091	0.137	0.175	0.227	0.257
	mm	1.09	2.31	3.48	4.45	5.77	6.53
W	inch	0.035	0.069	0.087	0.115	0.170	0.257
	mm	0.89	1.75	2.21	2.92	4.32	6.53
L_{Gate}	inch	0.006	0.012	0.024	0.029	0.040	0.050
	mm	0.15	0.30	0.61	0.74	1.02	1.27
W_{Gate}	inch	0.006	0.014	0.031	0.038	0.060	0.070
	mm	0.15	0.36	0.79	0.97	1.52	1.78
L_{Source}	inch	0.006	0.012	0.023	0.029	0.040	0.050
	mm	0.15	0.30	0.58	0.74	1.02	1.27
W_{Source}	inch	0.006	0.014	0.029	0.040	0.060	0.070
	mm	0.15	0.36	0.74	1.42	1.52	1.70
$T_{hickness}$	inch	0.016	0.016	0.016	0.016	0.016	0.016
	mm	0.41	0.41	0.41	0.41	0.41	0.41
Number of Gate Fingers		1	1	2	2	4	6



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Table 2. Electrical Probe Specifications for N-Channel HEXFET Power MOSFET Die

HEXFET DIE SIZE	PART NUMBER	MAXIMUM RATED V_{DS}	$R_{DS(on)}$ @ I_D = 1A, V_{GS} = 10V		I_{DSS} @ RATED V_{DS} MAXIMUM	I_{GSS} @ V_{GS} = 20V MAXIMUM	$V_{GS(TH)}$ @ I_D = 1mA, V_{DS} = V_{GS}		DATA SHEET FOR CORRESPONDING PACKAGED DEVICE
			TYP	MAX			MIN	MAX	
HEX-Z N	IRFC1Z0	100V	2.2 Ω	2.4 Ω	0.5mA	100nA	2.0V	4.0V	PD-9.380
	IRFC1Z1	60V	2.2 Ω	2.4 Ω	0.5mA	100nA	2.0V	4.0V	PD-9.380
	IRFC1Z2	100V	2.8 Ω	3.2 Ω	0.5mA	100nA	2.0V	4.0V	PD-9.380
	IRFC1Z3	60V	2.8 Ω	3.2 Ω	0.5mA	100nA	2.0V	4.0V	PD-9.380
HEX-1 N	IRFC110	100V	0.5 Ω	0.6 Ω	0.5mA	100nA	2.0V	4.0V	PD-9.325
	IRFC111	60V	0.5 Ω	0.6 Ω	0.5mA	100nA	2.0V	4.0V	PD-9.325
	IRFC112	100V	0.6 Ω	0.8 Ω	0.5mA	100nA	2.0V	4.0V	PD-9.325
	IRFC113	60V	0.6 Ω	0.8 Ω	0.5mA	100nA	2.0V	4.0V	PD-9.325
	IRFC210	200V	1.0 Ω	1.5 Ω	0.5mA	100nA	2.0V	4.0V	PD-9.326
	IRFC211	150V	1.0 Ω	1.5 Ω	0.5mA	100nA	2.0V	4.0V	PD-9.326
	IRFC212	200V	1.5 Ω	2.4 Ω	0.5mA	100nA	2.0V	4.0V	PD-9.326
	IRFC213	150V	1.5 Ω	2.4 Ω	0.5mA	100nA	2.0V	4.0V	PD-9.326
	IRFC310	400V	3.3 Ω	3.6 Ω	0.5mA	100nA	2.0V	4.0V	PD-9.327
	IRFC311	350V	3.3 Ω	3.6 Ω	0.5mA	100nA	2.0V	4.0V	PD-9.327
	IRFC312	400V	3.6 Ω	5.0 Ω	0.5mA	100nA	2.0V	4.0V	PD-9.327
	IRFC313	350V	3.6 Ω	5.0 Ω	0.5mA	100nA	2.0V	4.0V	PD-9.327
HEX-2 N	IRFC120	100V	0.25 Ω	0.3 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.312
	IRFC121	60V	0.25 Ω	0.3 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.312
	IRFC122	100V	0.3 Ω	0.4 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.312
	IRFC123	60V	0.3 Ω	0.4 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.312
	IRFC220	200V	0.5 Ω	0.8 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.316
	IRFC221	150V	0.5 Ω	0.8 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.316
	IRFC222	200V	0.8 Ω	1.2 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.316
	IRFC223	150V	0.8 Ω	1.2 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.316
	IRFC320	400V	1.5 Ω	1.8 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.134
	IRFC321	350V	1.5 Ω	1.8 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.134
	IRFC322	400V	1.8 Ω	2.5 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.134
	IRFC323	350V	1.8 Ω	2.5 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.134
	IRFC420	500V	2.5 Ω	3.0 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.323
	IRFC421	450V	2.5 Ω	3.0 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.323
	IRFC422	500V	3.0 Ω	4.0 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.323
	IRFC423	450V	3.0 Ω	4.0 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.323
HEX-3 N	IRFC130	100V	0.14 Ω	0.18 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.303
	IRFC131	60V	0.14 Ω	0.18 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.303
	IRFC132	100V	0.2 Ω	0.25 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.303
	IRFC133	60V	0.2 Ω	0.25 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.303
	IRFC230	200V	0.25 Ω	0.4 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.306
	IRFC231	150V	0.25 Ω	0.4 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.306
	IRFC232	200V	0.4 Ω	0.6 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.306
	IRFC233	150V	0.4 Ω	0.6 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.306
	IRFC330	400V	0.8 Ω	1.0 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.302
	IRFC331	350V	0.8 Ω	1.0 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.302
	IRFC332	400V	1.0 Ω	1.5 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.302
	IRFC333	350V	1.0 Ω	1.5 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.302
	IRFC430	500V	1.3 Ω	1.5 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.310
	IRFC431	450V	1.3 Ω	1.5 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.310
	IRFC432	500V	1.5 Ω	2.0 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.310
	IRFC433	450V	1.5 Ω	2.0 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.310
HEX-4 N	IRFC140	100V	0.07 Ω	0.085Ω	1.0mA	100nA	2.0V	4.0V	PD-9.369
	IRFC141	60V	0.07 Ω	0.085Ω	1.0mA	100nA	2.0V	4.0V	PD-9.369
	IRFC142	100V	0.09 Ω	0.11 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.369
	IRFC143	60V	0.09 Ω	0.11 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.369
	IRFC240	200V	0.14 Ω	0.18 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.370
	IRFC241	150V	0.14 Ω	0.18 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.370
	IRFC242	200V	0.20 Ω	0.22 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.370
	IRFC243	150V	0.20 Ω	0.22 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.370
	IRFC340	400V	0.47 Ω	0.55 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.371
	IRFC341	350V	0.47 Ω	0.55 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.371
	IRFC342	400V	0.68 Ω	0.80 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.371
	IRFC343	350V	0.68 Ω	0.80 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.371
	IRFC440	500V	0.8 Ω	0.85 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.372
	IRFC441	450V	0.8 Ω	0.85 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.372
	IRFC442	500V	1.0 Ω	1.1 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.372
	IRFC443	450V	1.0 Ω	1.1 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.372
HEX-5 N	IRFC150	100V	0.045Ω	0.055Ω	1.0mA	100nA	2.0V	4.0V	PD-9.305
	IRFC151	60V	0.045Ω	0.055Ω	1.0mA	100nA	2.0V	4.0V	PD-9.305
	IRFC152	100V	0.06 Ω	0.08 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.305
	IRFC153	60V	0.06 Ω	0.08 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.305
	IRFC250	200V	0.07 Ω	0.085Ω	1.0mA	100nA	2.0V	4.0V	PD-9.321
	IRFC251	150V	0.07 Ω	0.085Ω	1.0mA	100nA	2.0V	4.0V	PD-9.321
	IRFC252	200V	0.09 Ω	0.12 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.321
	IRFC253	150V	0.09 Ω	0.12 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.321
	IRFC350	400V	0.25 Ω	0.3 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.304
	IRFC351	350V	0.25 Ω	0.3 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.304
	IRFC352	400V	0.3 Ω	0.4 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.304
	IRFC353	350V	0.3 Ω	0.4 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.304
	IRFC450	500V	0.3 Ω	0.4 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.322
	IRFC451	450V	0.3 Ω	0.4 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.322
	IRFC452	500V	0.4 Ω	0.5 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.322
	IRFC453	450V	0.4 Ω	0.5 Ω	1.0mA	100nA	2.0V	4.0V	PD-9.322

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Table 3. Electrical Probe Specifications for P-Channel HEXFET Power MOSFET Die

HEXFET DIE SIZE	PART NUMBER	MAXIMUM RATED V_{DS}	$R_{DS}(on)$ @ I_D = 1A V_{GS} = 10V		I_{DSS} @ RATED V_{DS}	I_{GSS} @ V_{GS} = 20V	$V_{GS}(TH)$ @ I_D = 1mA, V_{DS} = V_{GS}		DATA SHEET FOR CORRESPONDING PACKAGED DEVICE
			TYP	MAX	MAXIMUM	MAXIMUM	MIN	MAX	
HEX-1 P	IRFC9110	-100V	1.0 Ω	1.2Ω	-0.5mA	-100nA	-2.0V	-4.0V	PD-9.381
	IRFC9111	-60V	1.0 Ω	1.2Ω	-0.5mA	-100nA	-2.0V	-4.0V	PD-9.381
	IRFC9112	-100V	1.2 Ω	1.6Ω	-0.5mA	-100nA	-2.0V	-4.0V	PD-9.381
	IRFC9113	-60V	1.2 Ω	1.6Ω	-0.5mA	-100nA	-2.0V	-4.0V	PD-9.381
	IRFC9210	-200V	2.3 Ω	3.0Ω	-0.5mA	-100nA	-2.0V	-4.0V	PD-9.350
	IRFC9211	-150V	2.3 Ω	3.0Ω	-0.5mA	-100nA	-2.0V	-4.0V	PD-9.350
	IRFC9212	-200V	3.5 Ω	4.5Ω	-0.5mA	-100nA	-2.0V	-4.0V	PD-9.350
	IRFC9213	-150V	3.5 Ω	4.5Ω	-0.5mA	-100nA	-2.0V	-4.0V	PD-9.350
HEX-2 P	IRFC9120	-100V	0.5 Ω	0.6Ω	-1.0mA	-100nA	-2.0V	-4.0V	PD-9.319
	IRFC9121	-60V	0.5 Ω	0.6Ω	-1.0mA	-100nA	-2.0V	-4.0V	PD-9.319
	IRFC9122	-100V	0.6 Ω	0.8Ω	-1.0mA	-100nA	-2.0V	-4.0V	PD-9.319
	IRFC9123	-60V	0.6 Ω	0.8Ω	-1.0mA	-100nA	-2.0V	-4.0V	PD-9.319
	IRFC9220	-200V	1.0 Ω	1.5Ω	-1.0mA	-100nA	-2.0V	-4.0V	PD-9.351
	IRFC9221	-150V	1.0 Ω	1.5Ω	-1.0mA	-100nA	-2.0V	-4.0V	PD-9.351
	IRFC9222	-200V	1.5 Ω	2.4Ω	-1.0mA	-100nA	-2.0V	-4.0V	PD-9.351
	IRFC9223	-150V	1.5 Ω	2.4Ω	-1.0mA	-100nA	-2.0V	-4.0V	PD-9.351
HEX-3 P	IRFC9130	-100V	0.25Ω	0.3Ω	-1.0mA	-100nA	-2.0V	-4.0V	PD-9.318
	IRFC9131	-60V	0.25Ω	0.3Ω	-1.0mA	-100nA	-2.0V	-4.0V	PD-9.318
	IRFC9132	-100V	0.3 Ω	0.4Ω	-1.0mA	-100nA	-2.0V	-4.0V	PD-9.318
	IRFC9133	-60V	0.3 Ω	0.4Ω	-1.0mA	-100nA	-2.0V	-4.0V	PD-9.318
	IRFC9230	-200V	0.5 Ω	0.8Ω	-1.0mA	-100nA	-2.0V	-4.0V	PD-9.349
	IRFC9231	-150V	0.5 Ω	0.8Ω	-1.0mA	-100nA	-2.0V	-4.0V	PD-9.349
	IRFC9232	-200V	0.8 Ω	1.2Ω	-1.0mA	-100nA	-2.0V	-4.0V	PD-9.349
	IRFC9233	-150V	0.8 Ω	1.2Ω	-1.0mA	-100nA	-2.0V	-4.0V	PD-9.349

Handling and Shipping

HEXFET dice from International Rectifier are shipped in anti-static chip trays and sealed in plastic containers for protection during shipment. Once opened, the dice must be stored in a dry, inert atmosphere such as nitrogen prior to assembly. Dice should be handled with DuPont Teflon-tipped vacuum pencils to prevent mechanical damage. Any nonconformance to the electrical or visual inspection specifications in this brochure must be reported in writing to International Rectifier within 60 days after shipment of the lot by International Rectifier. International Rectifier assumes no responsibilities for die which have been subjected to further processing such as mountdown, wire bonding, or encapsulation. In the interest of product improvement, the right is reserved to make design or processing changes without notification.

The anti-static chip trays are designed to avoid the build-up of static charge. International Rectifier HEXFETs have large gate capacitances and thick oxide layers relative to low level MOS devices. Though significantly more rugged than such low level devices, reasonable precautions should be observed during handling and assembly to prevent exceeding the ±20V maximum gate-source voltage. The chip tray capacities are 400, 180, 140, 96, 35 and 16 die per tray for HEX-Z, HEX-1, HEX-2, HEX-3, HEX-4 and HEX-5 dice, respectively.

Visual Inspection of Die

International Rectifier HEXFET die are designed to meet the visual inspection criteria of Mil-Standard 750B, Method 2072 with the exception of the specific criteria listed below. HEXFET dice are visually screened to a 1.0% AQL level. Mil-Standard 750B, Method 2072 shall apply except as follows (the paragraph numbers refer to Method 2072):

PAR. 3.1. All inspection is at 30X magnification.

PAR. 3.1.1.3 Localized areas of discoloration are generally harmless films which are present in varying degrees from lot to lot and are not cause for rejection.

PAR. 3.1.3.d A die having attached portions of the adjacent die up to 10% of additional length is acceptable, provided the die still fits the chip tray cavity.

PAR. 3.2.3.1 Ink, chemical stains, and other foreign material attached to the surface of the HEXFET die are isolated by a vapox (silicon dioxide) layer, except for the aluminum bonding pads, and are not cause for rejection.

Die Mounting

The HEXFET dice have chromium-nickel-silver drain metallization which is suitable for solder preform mounting using solders such as 95/5 PbSn or 92.5/2.5/5 Pb AgIn solder. Any of the commonly used header or substrate materials such as copper, nickel-plated copper, and gold-plated molybdenum, beryllia, and alumina are acceptable. The substrate must be freed of oxides prior to assembly either by chemical cleaning or H_2 prefiring techniques. The HEXFET dice should be cleaned prior to mountdown in deionized water cascade (one minute) followed by isopropyl alcohol agitated bath (twice, one minute each) and then 70°C nitrogen chamber drying. Mounting is generally accomplished in a profiled belt furnace. The furnace zone settings will depend upon hybrid mass density, jigging, and belt speed. The HEXFET die temperature must not exceed 400°C, nor be in the range of 350 to 400°C for greater than one minute. A clean furnace of hydrogen atmosphere is recommended, although nitrogen atmosphere or forming gas (nitrogen-hydrogen, 85% - 15%) is acceptable.

Wire Bonding

Electrical connection to the gate and source aluminum bonding pads is by ultrasonic wirebonding with annealed 99% Al, 1% Si wire having an elongation of 10%. The maximum recommended wire diameter for HEX-Z, HEX-1, HEX-2, HEX-3, HEX-4 and HEX-5 is 2 mil, 4 mil, 8 mil, 10 mil, 20 mil and 20 mil, respectively. Caution must be exercised during wire bonding to insure that the bonding footprint remains within

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the bonding pad area; otherwise, device failure can result. Likewise, wire bond equipment settings should be optimized and a wire pull test performed (e.g., see Method 2037, Mil-Standard 750B) to monitor wire bond strength uniformity. Destructive sample testing and 100% non-destructive testing is recommended. Rebonding of wire bond rejects can be performed although decreased yield can be expected from such reworks. Using process controls as described above, final assembly yields of 80% to 95% can be achieved.

Encapsulation

Prior to encapsulation, the die/assembly must be kept in a moisture-free environment, as I_{GSS} particularly is sensitive to surface moisture. If the final package is non-hermetic, a high grade electronic coating such as Dow Corning RTV3140 or equivalent should be applied. If the package is hermetic, the coating is optional. Cleaning of the die in a freon vapor degreaser prior to coating is recommended. Immediately prior to encapsulation, a 150°C, two-hour bake should be performed to remove any surface moisture. Capping of hermetic packages should be performed in a dry, nitrogen atmosphere.

Conclusion

The use of power MOSFET dice for hybrid assemblies can result in significant reduction in overall package size. In addition, the high gain characteristics of the HEXFET can allow further miniaturization by eliminating complex drive circuitry. Several HEXFET dice can readily be mounted on the same heatsink to form circuit configurations or to parallel devices. The HEXFET operational advantages, thereby, can be realized in very compact, custom package configurations. □

All dimensions shown in $\frac{\text{inches}}{\text{mm}}$

HEXFET DIE and BONDING PAD DIMENSIONS

(Not shown to scale)

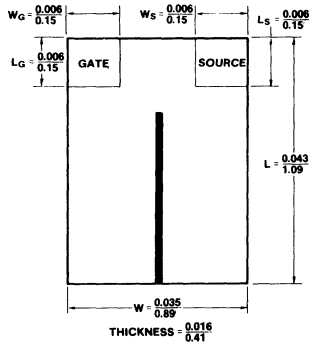


Figure 1. HEX-Z

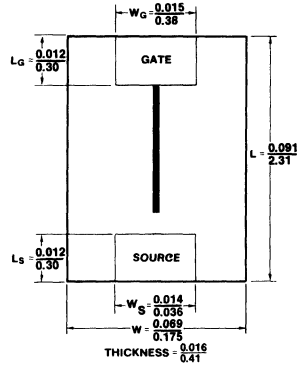


Figure 2. HEX-1

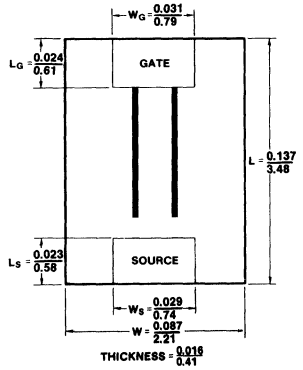


Figure 3. HEX-2

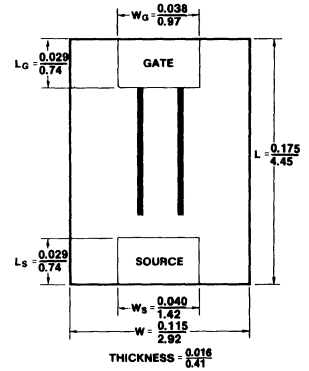


Figure 4. HEX-3

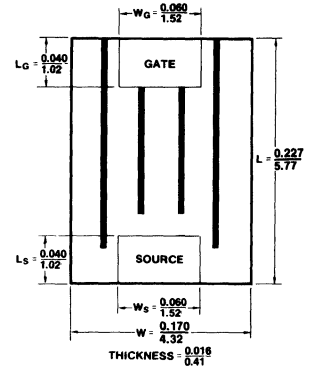


Figure 5. HEX-4

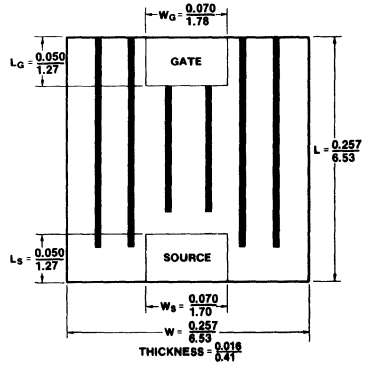


Figure 6. HEX-5

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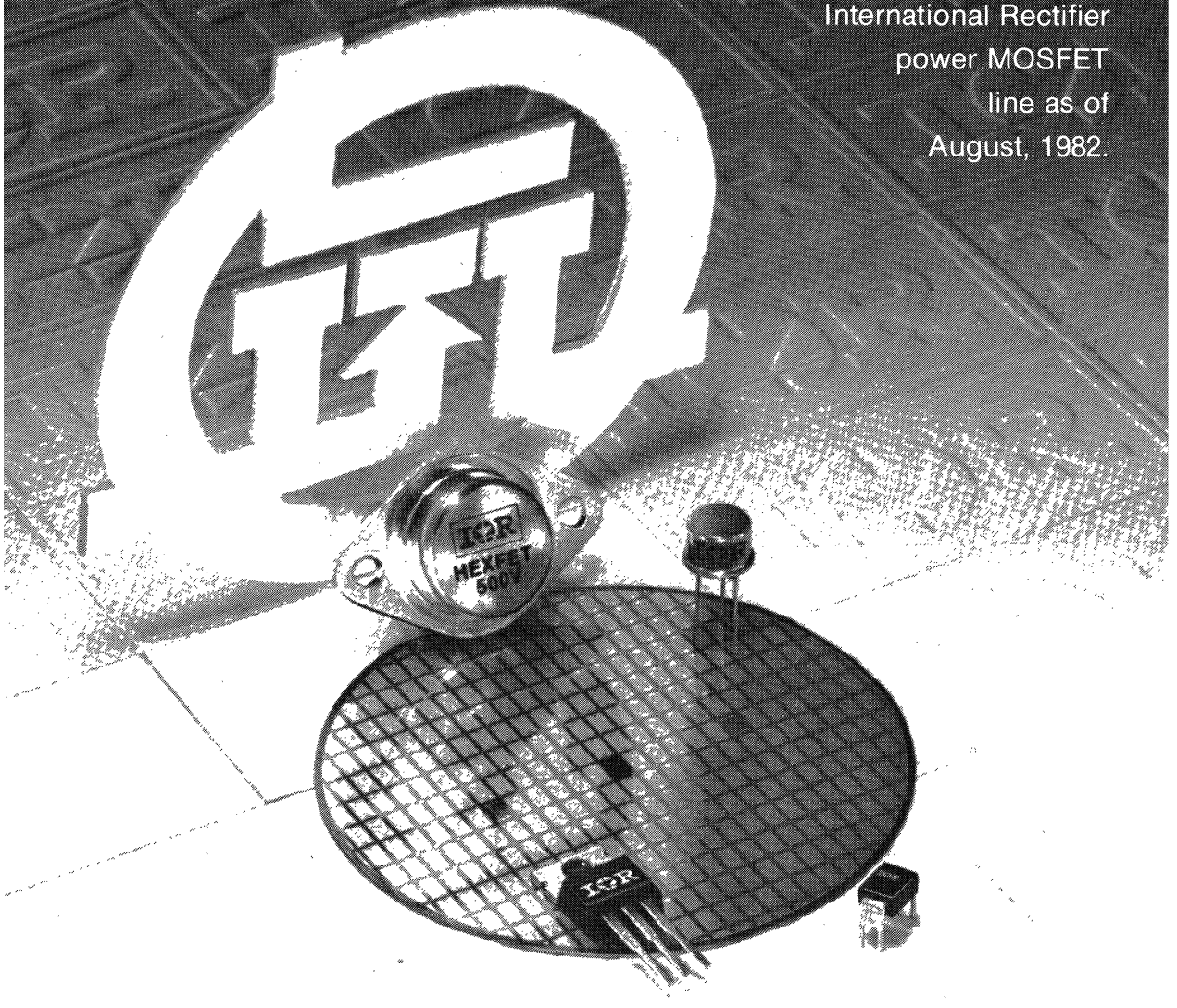
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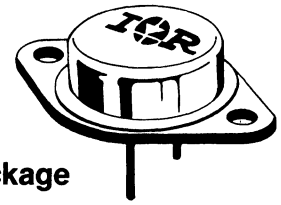
IOR HEXFET® PRODUCT DATA

The HEXFET devices detailed in the following pages represent the International Rectifier power MOSFET line as of August, 1982.



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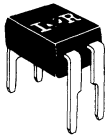
HEXFET SELECTOR GUIDE
BY PACKAGE, VOLTAGE RANGE AND "ON" RESISTANCE



TO-3 Package

VOLTAGE RANGE	SERIES NUMBER	"ON" RESISTANCE	PAGE NUMBER
60V-100V	IRF120	0.3 Ohms	D-69
	IRF130	0.18 Ohms	D-75
	IRF140	0.085 Ohms	D-81
	IRF150	0.055 Ohms	D-87
	IRF9130*	0.3 Ohms	D-263
	2N6755	0.25 Ohms	D-1
	2N6756**	0.18 Ohms	D-1
	2N6763	0.08 Ohms	D-17
	2N6764**	0.055 Ohms	D-17
150V-200V	IRF220	0.8 Ohms	D-93
	IRF230	0.4 Ohms	D-99
	IRF240	0.18 Ohms	D-105
	IRF250	0.085 Ohms	D-111
	IRF9230*	0.8 Ohms	D-269
	2N6757	0.6 Ohms	D-5
	2N6758**	0.4 Ohms	D-5
	2N6765	0.12 Ohms	D-21
	2N6766**	0.085 Ohms	D-21
350V-400V	IRF320	1.8 Ohms	D-117
	IRF330	1.0 Ohms	D-123
	IRF340	0.55 Ohms	D-129
	IRF350	0.3 Ohms	D-135
	2N6759	1.5 Ohms	D-9
	2N6760**	1.0 Ohms	D-9
	2N6767	0.4 Ohms	D-25
	2N6768	0.3 Ohms	D-25
450V-500V	IRF420	3.0 Ohms	D-141
	IRF430	1.5 Ohms	D-147
	IRF440	0.85 Ohms	D-153
	IRF450	0.4 Ohms	D-159
	2N6761	2.0 Ohms	D-13
	2N6762	1.5 Ohms	D-13
	2N6769	0.5 Ohms	D-29
	2N6770	0.4 Ohms	D-29

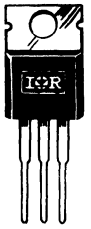
*P-Channel **Available to JAN/JANTX/JANTXV



HD-1 Package
4-PIN HEXDIP™

VOLTAGE RANGE	SERIES NUMBER	"ON" RESISTANCE	PAGE NUMBER
60V-100V	IRFD110	0.6 Ohms	D-39
	IRFD1Z0	2.4 Ohms	D-33
	IRFD9120*	0.6 Ohms	D-45

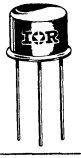
*P-Channel



TO-220AB Package

VOLTAGE RANGE	SERIES NUMBER	"ON" RESISTANCE	PAGE NUMBER
60V-100V	IRF510	.6 Ohms	D-165
	IRF520	0.3 Ohms	D-171
	IRF530	0.18 Ohms	D-177
	IRF540	0.085 Ohms	D-183
	IRF9520*	0.6 Ohms	D-275
	IRF9530*	0.3 Ohms	D-281
150V-200V	IRF610	1.5 Ohms	D-189
	IRF620	0.8 Ohms	D-195
	IRF630	0.4 Ohms	D-201
	IRF640	0.18 Ohms	D-207
	IRF9610*	3.0 Ohms	D-287
	IRF9620*	1.5 Ohms	D-293
	IRF9630*	0.8 Ohms	D-299
350V-400V	IRF710	3.6 Ohms	D-213
	IRF720	1.8 Ohms	D-219
	IRF730	1.0 Ohms	D-225
	IRF740	0.55 Ohms	D-231
450V-500V	IRF820	3.0 Ohms	D-237
	IRF830	1.5 Ohms	D-243
	IRF840	0.85 Ohms	D-249

*P-Channel



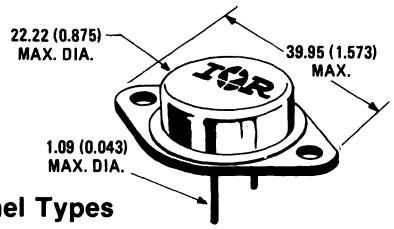
TO-39 Package

VOLTAGE RANGE	SERIES NUMBER	"ON" RESISTANCE	PAGE NUMBER
60V-100V	IRFF110	0.6 Ohms	D-51
	IRFF120	0.3 Ohms	D-57
	IRFF130	0.18 Ohms	D-63

NOTE: This Selector Guide lists only the first part number within a series of devices. Refer to appropriate listings for the complete HEXFET product line.

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INDEX TO TO-3 PACKAGED HEXFETs BY VOLTAGE RATING



JEDEC Types

Listed within the TO-3 packaged HEXFETs are 16 JEDEC registered devices, sequentially numbered from 2N6755 to 2N6770. The IRF part number immediately following each JEDEC number is the International Rectifier HEXFET equivalent.

Contact the factory for current JEDEC information

★ JAN, JANTX, JANTXV Types.

The JEDEC numbered devices identified with a star are available to JAN, JANTX, JANTXV specifications.

N-Channel Types

Electrical Characteristics at 25°C unless noted otherwise.

	V_{DS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	Part Numbers	I_D Continuous Drain Current (Amps) 100°C Case	I_D Continuous Drain Current (Amps) 25°C Case	I_{DM} Pulsed Drain Current (Amps)	P_D Max. Power Dissipation (Watts)	Page
	500	0.4	2N6770	7.75	12.0	25	150	D-29
	500	0.4	IRF450	8.0	13.0	52	150	D-159
	500	0.5	IRF452	7.0	12.0	48	150	D-159
	500	0.85	IRF440	5.0	8.0	32	125	D-153
	500	1.1	IRF442	4.0	7.0	28	125	D-153
	500	1.5	2N6762	3.0	4.5	7	75	D-13
	500	1.5	IRF430	3.0	4.5	18	75	D-147
	500	2.0	IRF432	2.5	4.0	16	75	D-147
	500	3.0	IRF420	1.5	2.5	10	40	D-141
	500	4.0	IRF422	1.0	2.0	8	40	D-141
	450	0.4	IRF451	8.0	13.0	52	150	D-159
	450	0.5	2N6769	7.0	11.0	20	150	D-29
	450	0.5	IRF453	7.0	12.0	48	150	D-159
	450	0.85	IRF441	5.0	8.0	32	125	D-153
	450	1.1	IRF443	4.0	7.0	28	125	D-153
	450	1.5	IRF431	3.0	4.5	18	75	D-147
	450	2.0	2N6761	2.5	4.0	6	75	D-13
	450	2.0	IRF433	2.5	4.0	16	75	D-147
	450	3.0	IRF421	1.5	2.5	10	40	D-141
	450	4.0	IRF423	1.0	2.0	8	40	D-141
	400	0.3	2N6768	9.0	14.0	25	150	D-25
	400	0.3	IRF350	9.0	15.0	60	150	D-135
	400	0.4	IRF352	8.0	13.0	52	150	D-135
	400	0.55	IRF340	6.0	10.0	40	125	D-129
	400	0.8	IRF342	5.0	8.0	32	125	D-129
★	400	1.0	2N6760	3.5	5.5	8	75	D-9
	400	1.0	IRF330	3.5	5.5	22	75	D-123
	400	1.5	IRF332	3.0	4.5	18	75	D-123
	400	1.8	IRF320	2.0	3.0	12	40	D-117
	400	2.5	IRF322	1.5	2.5	10	40	D-117
	350	0.3	IRF351	9.0	15.0	60	150	D-135
	350	0.4	2N6767	7.75	12.0	20	150	D-25
	350	0.4	IRF353	8.0	13.0	52	150	D-135
	350	0.55	IRF341	6.0	10.0	40	125	D-129
	350	0.8	IRF343	5.0	8.0	32	125	D-129
	350	1.0	IRF331	3.5	5.5	22	75	D-123
	350	1.5	2N6759	3.0	4.5	7	75	D-9
	350	1.5	IRF333	3.5	4.5	18	75	D-123
	350	1.8	IRF321	2.0	3.0	12	40	D-117
	350	2.5	IRF323	1.5	2.5	10	40	D-117
★	200	0.085	2N6766	19.0	30.0	60	150	D-21
	200	0.085	IRF250	19.0	30.0	120	150	D-111
	200	0.12	IRF252	16.0	25.0	100	150	D-111
	200	0.18	IRF240	11.0	18.0	72	125	D-105
	200	0.22	IRF242	10.0	16.0	64	125	D-105
★	200	0.4	2N6758	6.0	9.0	15	75	D-5
	200	0.4	IRF230	6.0	9.0	36	75	D-99
	200	0.6	IRF232	5.0	8.0	32	75	D-99
	200	0.8	IRF220	3.0	5.0	20	40	D-93
	200	1.2	IRF222	2.5	4.0	16	40	D-93
	150	0.085	IRF251	19.0	30.0	120	150	D-111
	150	0.12	2N6765	16.0	25.0	50	150	D-21
	150	0.12	IRF253	16.0	25.0	100	150	D-111
	150	0.18	IRF241	11.0	18.0	72	125	D-105
	150	0.22	IRF243	10.0	16.0	64	125	D-105
	150	0.4	IRF231	6.0	9.0	36	75	D-99
	150	0.6	2N6757	5.0	8.0	12	75	D-5
	150	0.6	IRF233	5.0	8.0	32	75	D-99
	150	0.8	IRF221	3.0	5.0	20	40	D-93
	150	1.2	IRF223	2.5	4.0	16	40	D-93
★	100	0.055	2N6764	24.0	38.0	70	150	D-17
	100	0.055	IRF150	25.0	40.0	160	150	D-87
	100	0.08	IRF152	20.0	33.0	132	150	D-87
	100	0.085	IRF140	17.0	27.0	108	125	D-81
	100	0.11	IRF142	15.0	24.0	96	125	D-81
★	100	0.18	2N6756	9.0	14.0	30	75	D-1
	100	0.18	IRF130	9.0	14.0	56	75	D-75
	100	0.25	IRF132	8.0	12.0	48	75	D-75
	100	0.3	IRF120	5.0	8.0	32	40	D-69
	100	0.4	IRF122	4.0	7.0	28	40	D-69
	60	0.055	IRF151	25.0	40.0	160	150	D-87
	60	0.08	2N6763	20.0	31.0	60	150	D-17
	60	0.08	IRF153	20.0	33.0	132	150	D-87
	60	0.085	IRF141	17.0	27.0	108	125	D-81
	60	0.11	IRF143	15.0	24.0	96	125	D-81
	60	0.18	IRF131	9.0	14.0	56	75	D-75
	60	0.25	2N6755	8.0	12.0	25	75	D-1
	60	0.25	IRF133	8.0	12.0	48	75	D-75
	60	0.3	IRF121	5.0	8.0	32	40	D-69
	60	0.4	IRF123	4.0	7.0	28	40	D-69

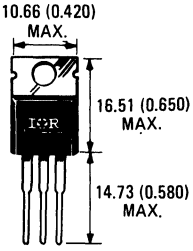
P-Channel Types

V_{DS} Drain Source Voltage (Volts)	$R_{DS(ON)}$ On-State Resistance (Ohms)	Part Numbers	I_D Continuous Drain Current (Amps) 100°C Case	I_D Continuous Drain Current (Amps) 25°C Case	I_{DM} Pulsed Drain Current (Amps)	P_D Max. Power Dissipation (Watts)	Page
-200	0.8	IRF9230	-4.0	-6.5	-26	75	D-269
-200	1.2	IRF9232	-3.5	-5.5	-22	75	D-269
-150	0.8	IRF9231	-4.0	-6.5	-26	75	D-269
-150	1.2	IRF9233	-3.5	-5.5	-22	75	D-269
-100	0.3	IRF9130	-7.5	-12.0	-48	75	D-263
-100	0.4	IRF9132	-6.5	-10.0	-40	75	D-263
-60	0.3	IRF9131	-7.5	-12.0	-48	75	D-263
-60	0.4	IRF9133	-6.5	-10.0	-40	75	D-263

Dimensions in Millimeters and (Inches)

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INDEX TO TO-220AB PACKAGED HEXFETs BY VOLTAGE RATING



TO-220AB plastic packaged HEXFETs offer a complete range of smaller, lower cost power MOSFETs ideally suited for commercial applications. Leads are on standard 100 mil centers for convenience in PC Board design. Savings in assembly costs can be realized because these devices can be installed by working from only one side of the board.

International Rectifier's advancements in construction techniques, materials and in-process production and quality control inspection ensure the high reliability of both the HEXFET die and the finished TO-220AB packaged HEXFET.

N-Channel Types

Electrical Characteristics at 25°C unless noted otherwise

V_{DS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	Part Numbers	I_D Continuous Drain Current (Amps) 100°C Case	25°C Case	I_{DM} Pulsed Drain Current (Amps)	P_D Max. Power Dissipation (Watts)	Page
500	0.85	IRF840	5.0	8.0	32	125	D-249
500	1.1	IRF842	4.0	7.0	28	125	D-249
500	1.5	IRF830	3.0	4.5	18	75	D-243
500	2.0	IRF832	2.5	4.0	16	75	D-243
500	3.0	IRF820	1.5	2.5	10	40	D-237
500	4.0	IRF822	1.0	2.0	8	40	D-237
450	0.85	IRF841	5.0	8.0	32	125	D-249
450	1.1	IRF843	4.0	7.0	28	125	D-249
450	1.5	IRF831	3.0	4.5	18	75	D-243
450	2.0	IRF833	2.5	4.0	16	75	D-243
450	3.0	IRF821	1.5	2.5	10	40	D-237
450	4.0	IRF823	1.0	2.0	8	40	D-237
400	0.55	IRF740	6.0	10.0	40	125	D-231
400	0.80	IRF742	5.0	8.0	32	125	D-231
400	1.0	IRF730	3.5	5.5	22	75	D-225
400	1.5	IRF732	3.0	4.5	18	75	D-225
400	1.8	IRF720	2.0	3.0	12	40	D-219
400	2.5	IRF722	1.5	2.5	10	40	D-219
400	3.6	IRF710	1.0	1.5	6	20	D-213
400	5.0	IRF712	0.8	1.3	5	20	D-213
350	0.55	IRF741	6.0	10.0	40	125	D-231
350	0.8	IRF743	5.0	8.0	32	125	D-231
350	1.0	IRF731	3.5	5.5	22	75	D-225
350	1.5	IRF733	3.0	4.5	18	75	D-225
350	1.8	IRF721	2.0	3.0	12	40	D-219
350	2.5	IRF723	1.5	2.5	10	40	D-219
350	3.6	IRF711	1.0	1.5	6	20	D-213
350	5.0	IRF713	0.8	1.3	5	20	D-213
200	0.18	IRF640	11.0	18.0	72	125	D-207
200	0.22	IRF642	10.0	16.0	64	125	D-207
200	0.4	IRF630	6.0	9.0	36	75	D-201
200	0.6	IRF632	5.0	8.0	32	75	D-201
200	0.8	IRF620	3.0	5.0	20	40	D-195
200	1.2	IRF622	2.5	4.0	16	40	D-195
200	1.5	IRF610	1.5	2.5	10	20	D-189
200	2.4	IRF612	1.25	2.0	8	20	D-189
150	0.18	IRF641	11.0	18.0	72	125	D-207
150	0.22	IRF643	10.0	16.0	64	125	D-207
150	0.4	IRF631	6.0	9.0	36	75	D-201
150	0.6	IRF633	5.0	8.0	32	75	D-201
150	0.8	IRF621	3.0	5.0	20	40	D-195
150	1.2	IRF623	2.5	4.0	16	40	D-195
150	1.5	IRF611	1.5	2.5	10	20	D-189
150	2.4	IRF613	1.25	2.0	8	20	D-189
100	0.085	IRF540	17.0	27.0	108	125	D-183
100	0.11	IRF542	15.0	24.0	96	125	D-183
100	0.18	IRF530	9.0	14.0	56	75	D-177
100	0.25	IRF532	8.0	12.0	48	75	D-177
100	0.3	IRF520	5.0	8.0	32	40	D-171
100	0.4	IRF522	4.0	7.0	28	40	D-171
100	0.6	IRF510	2.5	4.0	16	20	D-165
100	0.8	IRF512	2.0	3.5	14	20	D-165
60	0.085	IRF541	17.0	27.0	108	125	D-183
60	0.11	IRF543	15.0	24.0	96	125	D-183
60	0.18	IRF531	9.0	14.0	56	75	D-177
60	0.25	IRF533	8.0	12.0	48	75	D-177
60	0.3	IRF521	5.0	8.0	32	40	D-171
60	0.4	IRF523	4.0	7.0	28	40	D-171
60	0.6	IRF511	2.5	4.0	16	20	D-165
60	0.8	IRF513	2.0	3.5	14	20	D-165

P-Channel Types

V_{DS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	Part Numbers	I_D Continuous Drain Current (Amps) 100°C Case	25°C Case	I_{DM} Pulsed Drain Current (Amps)	P_D Max Power Dissipation (Watts)	Page
-200	0.8	IRF9630	-4.0	-6.5	-26	75	D-299
-200	1.2	IRF9632	-3.5	-5.5	-22	75	D-299
-200	1.5	IRF9620	-2.0	-3.5	-14	40	D-293
-200	2.4	IRF9622	-1.5	-3.0	-12	40	D-293
-200	3.0	IRF9610	-1.0	-1.75	-7	20	D-287
-200	4.5	IRF9612	-0.9	-1.5	-6	20	D-287
-150	0.8	IRF9631	-4.0	-6.5	-26	75	D-299
-150	1.2	IRF9633	-3.5	-5.5	-22	75	D-299
-150	1.5	IRF9621	-2.0	-3.5	-14	40	D-293
-150	2.4	IRF9623	-1.5	-3.0	-12	40	D-293
-150	3.0	IRF9611	-1.0	-1.75	-7	20	D-287
-150	4.5	IRF9613	-0.9	-1.5	-6	20	D-287
-100	0.3	IRF9530	-7.5	-12.0	-48	75	D-281
-100	0.4	IRF9532	-6.5	-10.0	-40	75	D-281
-100	0.6	IRF9520	-4.0	-6.0	-24	40	D-275
-100	0.8	IRF9522	-3.5	-5.0	-20	40	D-275
-60	0.3	IRF9531	-7.5	-12.0	-48	75	D-281
-60	0.4	IRF9533	-6.5	-10.0	-40	75	D-281
-60	0.6	IRF9521	-4.0	-6.0	-24	40	D-275
-60	0.8	IRF9523	-3.5	-5.0	-20	40	D-275

Characteristics common to all TO-3 and TO-220AB HEXFETs.

T_J = -55°C to + 150°C Operating

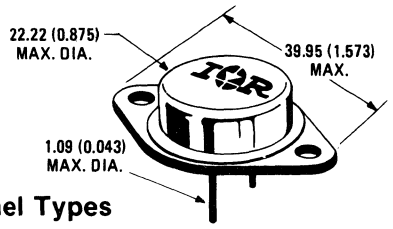
$V_{GS(th)}$ Gate Threshold = 2.0 to 4.0 Volts
See Data Sheets for conditions

Lead Temperature = 300°C for 10 Seconds Max

Dimensions in Millimeters and (Inches)

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NUMERICAL INDEX TO TO-3 PACKAGED HEXFETs.



JEDEC Types

Listed within the TO-3 packaged HEXFETs are 16 JEDEC registered devices, sequentially numbered from 2N6755 to 2N6770. The IRF part number immediately following each JEDEC number is the International Rectifier HEXFET equivalent.

Contact the factory for current JEDEC information

★ JAN, JANTX, JANTXV Types.

The JEDEC numbered devices identified with a star are available to JAN, JANTX, JANTXV specifications.

N-Channel Types

Electrical Characteristics at 25°C unless noted otherwise

Part Numbers	V_{DS}, Drain Source Voltage (Volts)	R_{DS} (on), On-State, Resistance (Ohms)	I_D, Continuous Drain Current 100°C Case	I_D, Continuous Drain Current 25°C Case	I_{DM}, Pulse Drain Current (Amps)	P_D, Max. Power Dissipation (Watts)	Page
IRF120	100	0.3	5.0	8.0	32	40	D-69
IRF121	60	0.3	5.0	8.0	32	40	
IRF122	100	0.4	4.0	7.0	28	40	
IRF123	60	0.4	4.0	7.0	28	40	
IRF130	100	0.18	9.0	14.0	56	75	D-75
IRF131	60	0.18	9.0	14.0	56	75	
IRF132	100	0.25	8.0	12.0	48	75	
IRF133	60	0.25	8.0	12.0	48	75	
IRF140	100	0.085	17.0	27.0	108	125	D-81
IRF141	60	0.085	17.0	27.0	108	125	
IRF142	100	0.11	15.0	24.0	96	125	
IRF143	60	0.11	15.0	24.0	96	125	
IRF150	100	0.055	25.0	40.0	160	150	D-87
IRF151	60	0.055	25.0	40.0	160	150	
IRF152	100	0.08	20.0	33.0	132	150	
IRF153	60	0.08	20.0	33.0	132	150	
IRF220	200	0.8	3.0	5.0	20	40	D-93
IRF221	150	0.8	3.0	5.0	20	40	
IRF222	200	1.2	2.5	4.0	16	40	
IRF223	150	1.2	2.5	4.0	16	40	
IRF230	200	0.4	6.0	9.0	36	75	D-99
IRF231	150	0.4	6.0	9.0	36	75	
IRF232	200	0.6	5.0	8.0	32	75	
IRF233	150	0.6	5.0	8.0	32	75	
IRF240	200	0.18	11.0	18.0	72	125	D-105
IRF241	150	0.18	11.0	18.0	72	125	
IRF242	200	0.22	10.0	16.0	64	125	
IRF243	200	0.22	10.0	16.0	64	125	
IRF250	200	0.085	19.0	30.0	120	150	D-111
IRF251	150	0.085	19.0	30.0	120	150	
IRF252	200	0.120	16.0	25.0	100	150	
IRF253	150	0.120	16.0	25.0	100	150	
IRF320	400	1.8	2.0	3.0	12	40	D-117
IRF321	350	1.8	2.0	3.0	12	40	
IRF322	400	2.5	1.5	2.5	10	40	
IRF323	350	2.5	1.5	2.5	10	40	
IRF330	400	1.0	3.5	5.5	22	75	D-123
IRF331	350	1.0	3.5	5.5	22	75	
IRF332	400	1.5	3.0	4.5	18	75	
IRF333	350	1.5	3.0	4.5	18	75	
IRF340	400	0.55	6.0	10.0	40	125	D-129
IRF341	350	0.55	6.0	10.0	40	125	
IRF342	400	0.8	5.0	8.0	32	125	
IRF343	350	0.8	5.0	8.0	32	125	
IRF350	400	0.3	9.0	15.0	60	150	D-135
IRF351	350	0.3	9.0	15.0	60	150	
IRF352	400	0.4	8.0	13.0	52	150	
IRF353	350	0.4	8.0	13.0	52	150	
IRF420	500	0.3	1.5	2.5	10	40	D-141
IRF421	450	0.3	1.5	2.5	10	40	
IRF422	500	2.0	1.0	2.0	8	40	
IRF423	450	2.0	1.0	2.0	8	40	
IRF430	500	1.5	3.0	4.5	18	75	D-147
IRF431	450	1.5	3.0	4.5	18	75	
IRF432	500	2.0	2.5	4.0	16	75	
IRF433	450	2.0	2.5	4.0	16	75	
IRF440	500	0.85	5.0	8.0	32	125	D-153
IRF441	450	0.85	5.0	8.0	32	125	
IRF442	500	1.1	4.0	7.0	28	125	
IRF443	450	1.1	4.0	7.0	28	125	
IRF450	500	0.4	8.0	13.0	52	150	D-159
IRF451	450	0.4	8.0	13.0	52	150	
IRF452	500	0.5	7.0	12.0	48	150	
IRF453	450	0.5	7.0	12.0	48	150	
2N6755	60	0.25	8.0	12.0	25	75	D-1
★2N6756	100	0.18	9.0	14.0	30	75	D-1
2N6757	150	0.6	5.0	8.0	12	75	D-5
★2N6758	200	0.4	6.0	9.0	15	75	D-5
2N6759	350	1.5	3.0	4.5	7	75	D-9
★2N6760	400	1.0	3.5	5.5	8	75	D-9
2N6761	450	2.0	2.5	4.0	6	75	D-13
2N6762	500	1.5	3.0	4.5	7	75	D-13
2N6763	60	0.08	20.0	31.0	60	150	D-17
★2N6764	100	0.055	24.0	38.0	70	150	D-17
2N6765	150	0.12	16.0	25.0	50	150	D-21
★2N6766	200	0.085	19.0	30.0	60	150	D-21
2N6767	350	0.4	7.75	12.0	20	150	D-25
2N6768	400	0.3	9.0	14.0	25	150	D-25
2N6769	450	0.5	7.0	11.0	20	150	D-29
★2N6770	500	0.4	7.75	12.0	25	150	D-29

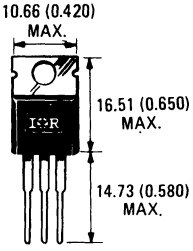
★ JAN, JANTX, JANTXV Types

P-Channel Types

Part Numbers	V_{DS}, Drain Source Voltage (Volts)	R_{DS} (on), On-State, Resistance (Ohms)	I_D, Continuous Drain Current 100°C Case	I_D, Continuous Drain Current 25°C Case	I_{DM}, Pulse Drain Current (Amps)	P_D, Max. Power Dissipation (Watts)	Page
IRF9130	-100	0.3	-7.5	-12.0	-48	75	D-263
IRF9131	-60	0.3	-7.5	-12.0	-48	75	
IRF9132	-100	0.4	-6.5	-10.0	-40	75	
IRF9133	-60	0.4	-6.5	-10.0	-40	75	
IRF9230	-200	0.8	-4.0	-6.5	-26	75	D-269
IRF9231	-150	0.8	-4.0	-6.5	-26	75	
IRF9232	-200	1.2	-3.5	-5.5	-22	75	
IRF9233	-150	1.2	-3.5	-5.5	-22	75	

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NUMERICAL INDEX TO TO-220AB PACKAGED HEXFETs.



TO-220AB plastic packaged HEXFETs offer a complete range of smaller, lower cost power MOSFETs ideally suited for commercial applications Leads are on standard 100 mil centers for convenience in PC Board design. Savings in assembly costs can be realized because these devices can be installed by working from only one side of the board.

International Rectifier's advancements in construction techniques, materials and in-process production and quality control inspection ensure the high reliability of both the HEXFET die and the finished TO-220AB packaged HEXFET

N-Channel Types

Electrical Characteristics at 25°C unless noted otherwise

Part Numbers	V_{DS}, Drain Source Voltage (Volts)	R_{DS} (on), On-State, Resistance (Ohms)	I_D, Continuous Drain Current 100°C Case	I_D, Continuous Drain Current 25°C Case	I_{DM}, Pulse Drain Current (Amps)	P_D, Max. Power Dissipation (Watts)	Page
IRF510	100	0.6	2.5	4.0	16	20	D-165
IRF511	60	0.6	2.5	4.0	16	20	
IRF512	100	0.8	2.0	3.5	14	20	
IRF513	60	0.8	2.0	3.5	14	20	
IRF520	100	0.3	5.0	8.0	32	40	D-171
IRF521	60	0.3	5.0	8.0	32	40	
IRF522	100	0.4	4.0	7.0	28	40	
IRF523	60	0.4	4.0	7.0	28	40	
IRF530	100	0.18	9.0	14.0	56	75	D-177
IRF531	60	0.18	9.0	14.0	56	75	
IRF532	100	0.25	8.0	12.0	48	75	
IRF533	60	0.25	8.0	12.0	48	75	
IRF540	100	0.085	17.0	27.0	108	125	D-183
IRF541	60	0.085	17.0	27.0	108	125	
IRF542	100	0.11	15.0	24.0	96	125	
IRF543	60	0.11	15.0	24.0	96	125	
IRF610	200	1.5	1.5	2.5	10	20	D-189
IRF611	150	1.5	1.5	2.5	10	20	
IRF612	200	2.4	1.25	2.0	8	20	
IRF613	150	2.4	1.25	2.0	8	20	
IRF620	200	0.8	3.0	5.0	20	40	D-195
IRF621	150	0.8	3.0	5.0	20	40	
IRF622	200	1.2	2.5	4.0	16	40	
IRF623	150	1.2	2.5	4.0	16	40	
IRF630	200	0.4	6.0	9.0	36	75	D-201
IRF631	150	0.4	6.0	9.0	36	75	
IRF632	200	0.6	5.0	8.0	32	75	
IRF633	150	0.6	5.0	8.0	32	75	
IRF640	200	0.18	11.0	18.0	72	125	D-207
IRF641	150	0.18	11.0	18.0	72	125	
IRF642	200	0.22	10.0	16.0	64	125	
IRF643	150	0.22	10.0	16.0	64	125	
IRF710	400	3.6	1.0	1.5	6	20	D-213
IRF711	350	3.6	1.0	1.5	6	20	
IRF712	400	5.0	0.8	1.3	5	20	
IRF713	350	5.0	0.8	1.3	5	20	
IRF720	400	1.8	2.0	3.0	12	40	D-219
IRF721	350	1.8	2.0	3.0	12	40	
IRF722	400	2.5	1.5	2.5	10	40	
IRF723	350	2.5	1.5	2.5	10	40	
IRF730	400	1.0	3.5	5.5	22	75	D-225
IRF731	350	1.0	3.5	5.5	22	75	
IRF732	400	1.5	3.0	4.5	18	75	
IRF733	350	1.5	3.0	4.5	18	75	
IRF740	400	0.55	6.0	10.0	40	125	D-231
IRF741	350	0.55	6.0	10.0	40	125	
IRF742	400	0.8	5.0	8.0	32	125	
IRF743	350	0.8	5.0	8.0	32	125	

Part Numbers	V_{DS}, Drain Source Voltage (Volts)	R_{DS} (on), On-State, Resistance (Ohms)	I_D, Continuous Drain Current 100°C Case	I_D, Continuous Drain Current 25°C Case	I_{DM}, Pulse Drain Current (Amps)	P_D, Max. Power Dissipation (Watts)	Page
IRF820	500	3.0	1.5	2.5	10	40	D-237
IRF821	450	3.0	1.5	2.5	10	40	
IRF822	500	4.0	1.0	2.0	8	40	
IRF823	450	4.0	1.0	2.0	8	40	
IRF830	500	1.5	3.0	4.5	18	75	D-243
IRF831	450	1.5	3.0	4.5	18	75	
IRF832	500	2.0	2.5	4.0	16	75	
IRF833	450	2.0	2.5	4.0	16	75	
IRF840	500	0.85	5.0	8.0	32	125	D-249
IRF841	450	0.85	5.0	8.0	32	125	
IRF842	500	1.1	4.0	7.0	28	125	
IRF843	450	1.1	4.0	7.0	28	125	

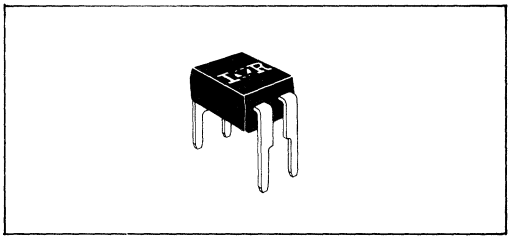
P-Channel Types

Part Numbers	V_{DS}, Drain Source Voltage (Volts)	R_{DS} (on), On-State, Resistance (Ohms)	I_D, Continuous Drain Current 100°C Case	I_D, Continuous Drain Current 25°C Case	I_{DM}, Pulse Drain Current (Amps)	P_D, Max. Power Dissipation (Watts)	Page
IRF9520	-100	0.6	-4.0	-6.0	-24	40	D-275
IRF9521	-60	0.6	-4.0	-6.0	-24	40	
IRF9522	-100	0.8	-3.5	-5.0	-20	40	
IRF9523	-60	0.8	-3.5	-5.0	-20	40	
IRF9530	-100	0.3	-7.5	-12.0	-48	75	D-281
IRF9531	-60	0.3	-7.5	-12.0	-48	75	
IRF9532	-100	0.4	-6.5	-10.0	-40	75	
IRF9533	-60	0.4	-6.5	-10.0	-40	75	
IRF9610	-200	3.0	-1.0	-1.75	-7	20	D-287
IRF9611	-150	3.0	-1.0	-1.75	-7	20	
IRF9612	-200	4.5	-0.9	-1.5	-6	20	
IRF9613	-150	4.5	-0.9	-1.5	-6	20	
IRF9620	-200	1.5	-2.0	-3.5	-14	40	D-293
IRF9621	-150	1.5	-2.0	-3.5	-14	40	
IRF9622	-200	2.4	-1.5	-3.0	-12	40	
IRF9623	-150	2.4	-1.5	-3.0	-12	40	
IRF9630	-200	0.8	-4.0	-6.5	-26	75	D-299
IRF9631	-150	0.8	-4.0	-6.5	-26	75	
IRF9632	-200	1.2	-3.5	-5.5	-22	75	
IRF9633	-150	1.2	-3.5	-5.5	-22	75	

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Dual In-Line HEXDIPs

HEXDIPs combine automatic insertion efficiency, a 1 watt heat sink tab with the HEXFET high performance, quality, and reliability. These space saving HEXDIPs are end-stackable in rows of any length on 100 mil centers. The low profile N and P-Channel HEXDIPs can be used on boards for cages with 0.5" board spacing.



Electrical Characteristics at 25° C unless noted otherwise

Part Numbers	V_{DS} Drain Source Voltage (Volts)	$R_{DS(on)}$, On-State Resistance (Ohms)	I_D Continuous Drain Current 25° C Case	I_{DM} Pulse Drain Current (Amps)	P_D Max. Power Dissipation (Watts)	Page
4-Pin, N-Channel Types						
IRFD1Z0	100	2.4	0.5	2.0	1.0	D-33
IRFD1Z1	60	2.4	0.5	2.0	1.0	
IRFD1Z2	100	3.2	0.4	1.5	1.0	
IRFD1Z3	60	3.2	0.4	1.5	1.0	
IRFD110	100	0.6	1.0	4.0	1.0	D-39
IRFD111	60	0.6	1.0	4.0	1.0	
IRFD112	100	0.8	0.8	3.0	1.0	
IRFD113	60	0.8	0.8	3.0	1.0	
4-Pin, P-Channel Types						
IRFD9120	-100	0.6	-1.0	-4.0	1.0	D-45
IRFD9121	-60	0.6	-1.0	-4.0	1.0	
IRFD9122	-100	0.8	-0.8	-3.0	1.0	
IRFD9123	-60	0.8	-0.8	-3.0	1.0	

TO-39 Packaged HEXFETs.

HEXFET power MOSFETs in TO-39 packages offer the industry's lowest on-state resistance and best power ratios in this case style.



Used as switching devices, these hermetically sealed TO-39 HEXFETs are suitable for interfacing logic signals in hostile environment applications such as military, instrumentation, process controls and on-site computer systems. Because the HEXFET process yields on-state resistances that are approximately 30 percent lower than MOSFET technologies, signal integrity is high and component losses are low.

Electrical Characteristics at 25° C unless noted otherwise

Part Numbers	V_{DS} Drain Source Voltage (Volts)	$R_{DS(on)}$, On-State Resistance (Ohms)	I_D Continuous Drain Current 25° C Case	I_{DM} Pulse Drain Current (Amps)	P_D Max. Power Dissipation (Watts)	Page
IRFF110	100	0.6	3.5	14	15	D-51
IRFF111	60	0.6	3.5	14	15	
IRFF112	100	0.8	3.0	12	15	
IRFF113	60	0.8	3.0	12	15	
IRFF120	100	0.3	6.0	24	20	D-57
IRFF121	60	0.3	6.0	24	20	
IRFF122	100	0.4	5.0	20	20	
IRFF123	60	0.4	5.0	20	20	
IRFF130	100	0.18	8.0	32	25	D-63
IRFF131	60	0.18	8.0	32	25	
IRFF132	100	0.25	7.0	28	25	
IRFF133	60	0.25	7.0	28	25	

TO-220AB N and P-Channel Complementary Pairs.

Broad bandwidth and linearity make these complementary HEXFET pairs ideal for high-quality amplifiers in audio, ultrasonic, radar/sonar and general purpose applications. Using these HEXFETs in complementary output stages allows two devices to share load current equally and provide identical characteristics and low harmonic distortion.

As presented in the table at right, each part number covers two TO-220AB devices. Example: IRF5522 consists of one N-Channel device marked N F5522 and one P-Channel device marked P F5522.

Electrical Characteristics at 25° C unless noted otherwise

Part Numbers	Device Types Included	V_{DS} Drain Source Voltage (Volts)	I_{DM} Pulsed Drain Current (Amps)	P_D Max. Power Dissipation (Watts)	Page
IRF5522	N-Channel	+100	+12	40	D-255
	P-Channel	-100	-12	40	
IRF5523	N-Channel	+60	+12	40	D-255
	P-Channel	-60	-12	40	
IRF5532	N-Channel	+100	+25	75	D-259
	P-Channel	-100	-25	75	
IRF5533	N-Channel	+60	+25	75	D-259
	P-Channel	-60	-25	75	

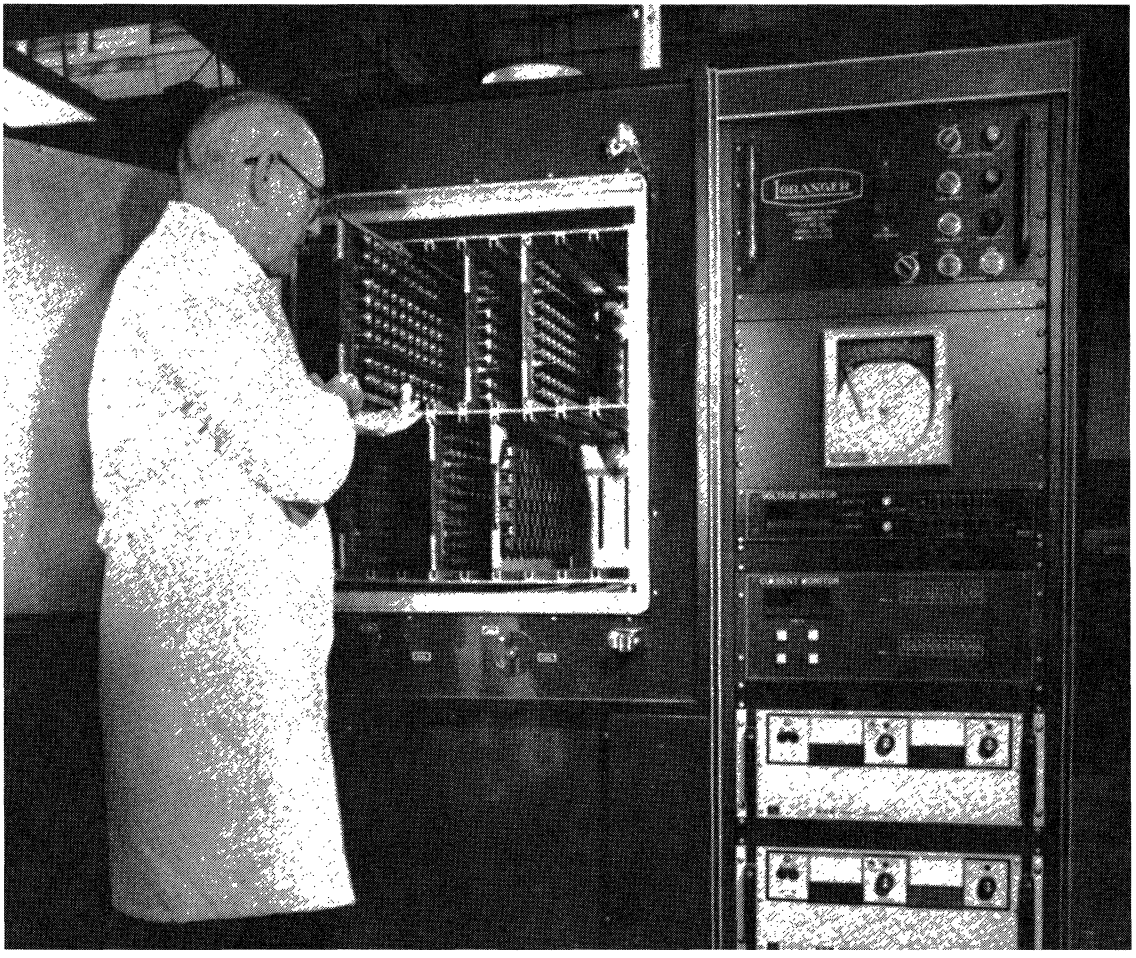
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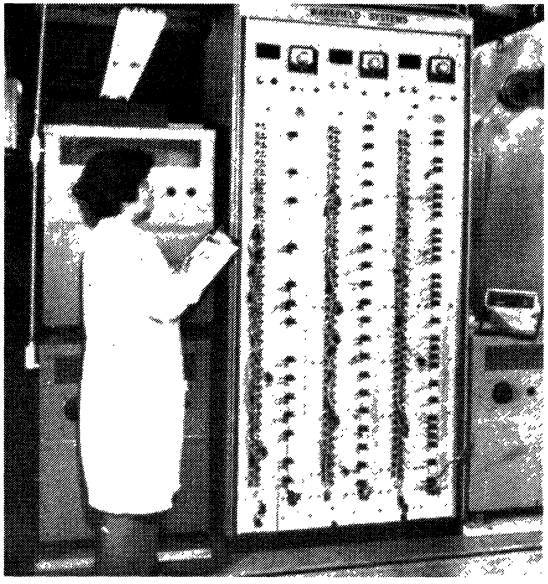
JAN, JANTX, JANTXV and C.E.C.C. Test Capabilities.

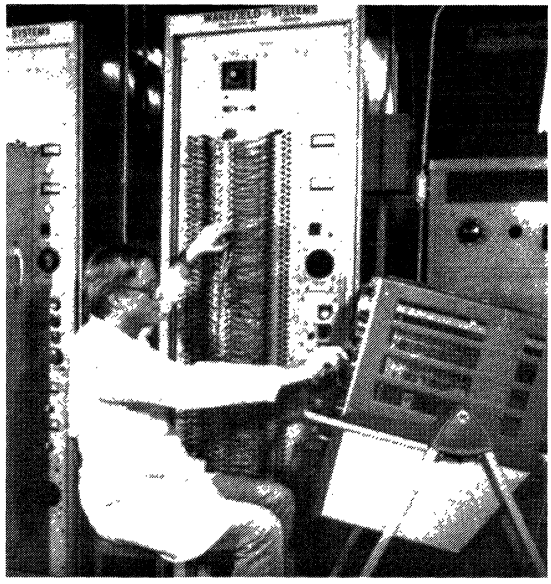
International Rectifier supplies HEXFETs which meet the high reliability requirements of the Military, DOE and NASA. The manufacturing facilities and test lab of International Rectifier at El Segundo, CA, have been surveyed by DESC to Appendix D of MIL-S-19500F and have been approved to produce the JAN, JANTX and JANTXV devices listed on the pages that follow. The IR facilities at Oxted, England have been approved to produce the C.E.C.C. devices listed.

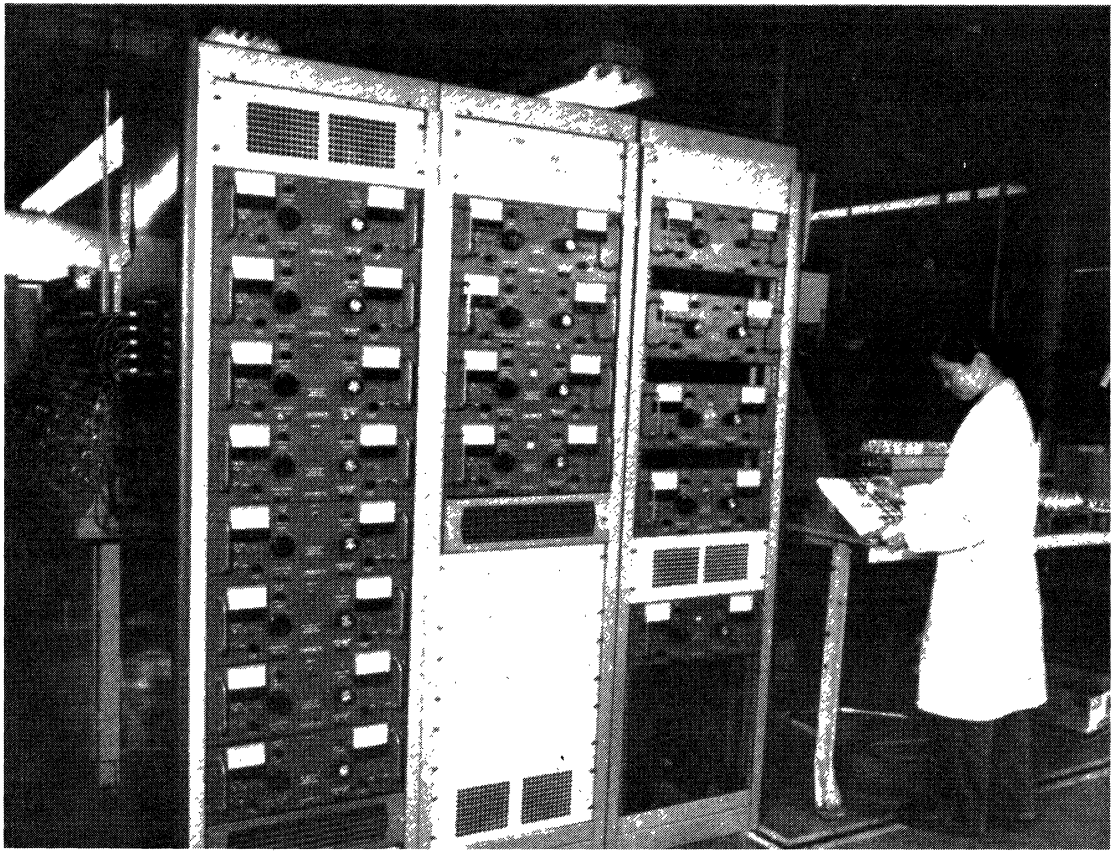
High reliability tests available include such screens as pre-cap visual, oven bake, temperature cycling, hermetic seal, constant acceleration, burn-in with delta limits, and tests such as salt atmosphere, altitude, moisture resistance, vibration, shock, thermal resistance and life tests.



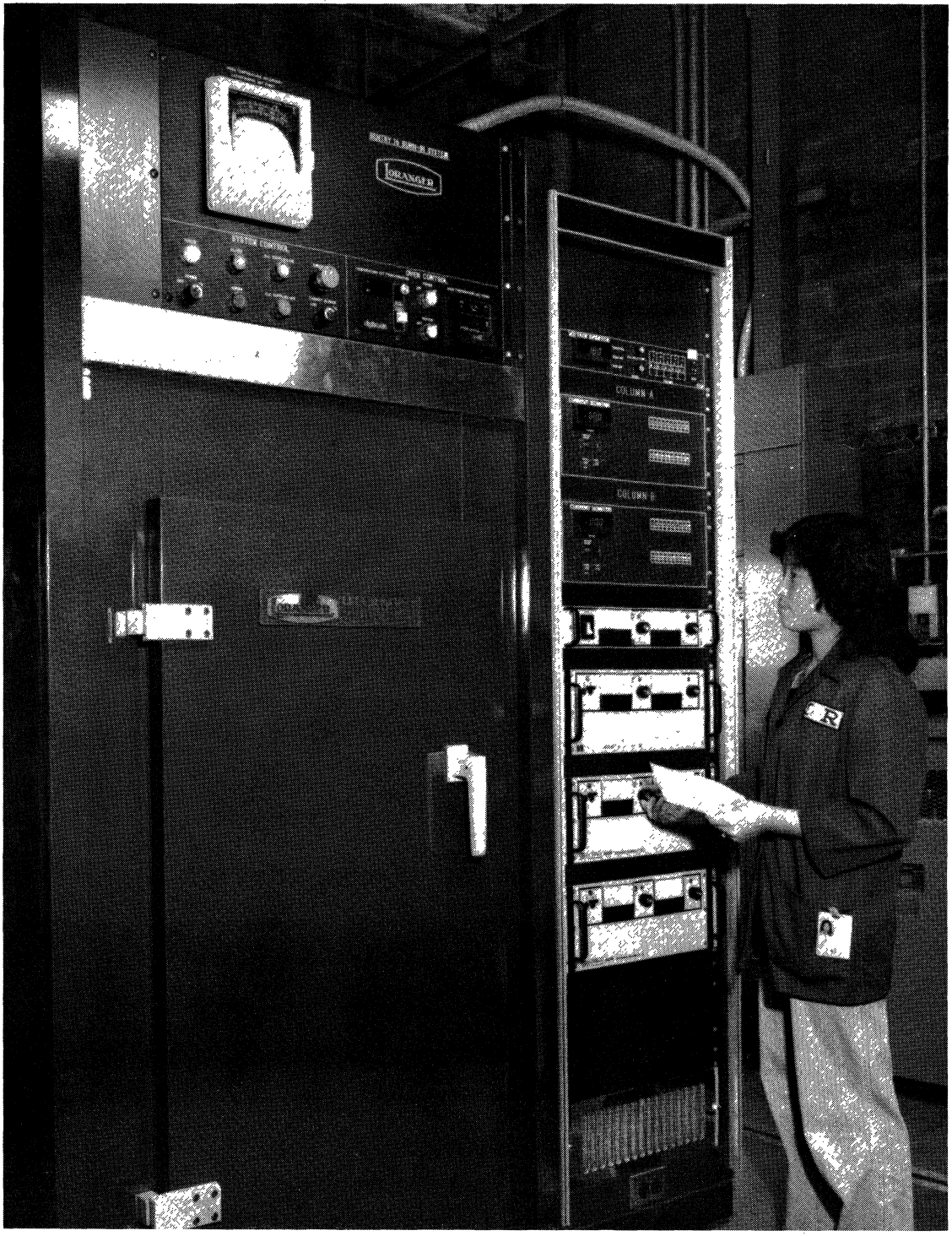
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MIL QUALIFIED HEXFETs

JAN, JANTX, JANTXV HEXFET POWER MOSFETs

Part Number	Cross Reference	JAN	JANTX	JANTXV	Voltage	Current (25°C)	MIL Spec	Qualification
2N6756	IRF130	Yes	Yes	Yes	100V	14.0 A	MIL-S-19500/542A	19500-488-81
2N6758	IRF230	Yes	Yes	Yes	200V	9.0 A	MIL-S-19500/542A	19500-488-81
2N6760	IRF330	Yes	Yes	Yes	400V	5.5 A	MIL-S-19500/542A	19500-488-81
2N6762	IRF430	Yes	Yes	Yes	500V	4.5 A	MIL-S-19500/542A	*
2N6764	IRF150	Yes	Yes	Yes	100V	38.0 A	MIL-S-19500/543A	19500-490-81
2N6766	IRF250	Yes	Yes	Yes	200V	30.0 A	MIL-S-19500/543A	19500-490-81
2N6768	IRF350	Yes	Yes	Yes	400V	14.0 A	MIL-S-19500/543A	*
2N6770	IRF450	Yes	Yes	Yes	500V	12.0 A	MIL-S-19500/543A	*

*Qualification testing completed as of September, 1982. Consult factory for qualification approval status.

C.E.C.C. POWER HEXFET REGISTRATIONS AND APPROVALS

C.E.C.C. Part Number	Approval Number
IRF120 CECC	50-012-012
IRF120 CECC SA	50-012-012
IRF120 CECC SB	50-012-012
IRF120 CECC SC	50-012-012
IRF120 CECC SD	50-012-012
IRF123 CECC	50-012-012
IRF130 CECC	50-012-013
IRF130 CECC SA	50-012-013
IRF130 CECC SB	50-012-013
IRF130 CECC SC	50-012-013
IRF130 CECC SD	50-012-013
IRF133 CECC	50-012-013
IRF150 CECC	50-012-014
IRF150 CECC SA	50-012-014
IRF150 CECC SB	50-012-014
IRF150 CECC SC	50-012-014
IRF150 CECC SD	50-012-014
IRF153 CECC	50-012-014
IRF220 CECC	50-012-012
IRF220 CECC SA	50-012-012
IRF220 CECC SB	50-012-012
IRF220 CECC SC	50-012-012
IRF220 CECC SD	50-012-012
IRF223 CECC	50-012-012
IRF230 CECC	50-012-013
IRF230 CECC SA	50-012-013

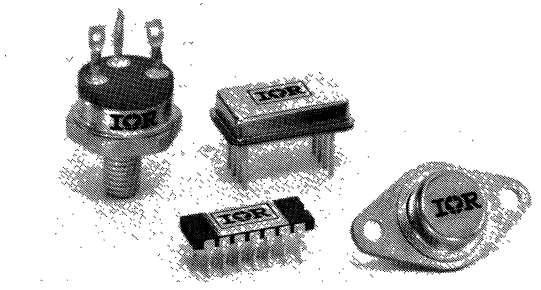
C.E.C.C. Part Number	Approval Number
IRF230 CECC SB	50-012-013
IRF230 CECC SC	50-012-013
IRF230 CECC SD	50-012-013
IRF233 CECC	50-012-013
IRF250 CECC	50-012-014
IRF250 CECC SA	50-012-014
IRF250 CECC SB	50-012-014
IRF250 CECC SC	50-012-014
IRF250 CECC SD	50-012-014
IRF253 CECC	50-012-014
IRF320 CECC	50-012-012
IRF320 CECC SA	50-012-012
IRF320 CECC SB	50-012-012
IRF320 CECC SC	50-012-012
IRF320 CECC SD	50-012-012
IRF323 CECC	50-012-012
IRF330 CECC	50-012-013
IRF330 CECC SA	50-012-013
IRF330 CECC SB	50-012-013
IRF330 CECC SC	50-012-013
IRF330 CECC SD	50-012-013
IRF333 CECC	50-012-013
IRF350 CECC	50-012-014
IRF350 CECC SA	50-012-014
IRF350 CECC SB	50-012-014
IRF350 CECC SC	50-012-014

C.E.C.C. Part Number	Approval Number
IRF350 CECC SD	50-012-014
IRF353 CECC	50-012-014
IRF420 CECC	50-012-012
IRF420 CECC SA	50-012-012
IRF420 CECC SB	50-012-012
IRF420 CECC SC	50-012-012
IRF420 CECC SD	50-012-012
IRF423 CECC	50-012-012
IRF430 CECC	50-012-013
IRF430 CECC SA	50-012-013
IRF430 CECC SB	50-012-013
IRF430 CECC SC	50-012-013
IRF430 CECC SD	50-012-013
IRF433 CECC	50-012-013
IRF450 CECC	50-012-014
IRF450 CECC SA	50-012-014
IRF450 CECC SB	50-012-014
IRF450 CECC SC	50-012-014
IRF450 CECC SD	50-012-014
IRF453 CECC	50-012-014
IRF9130 CECC	50-012-015
IRF9130 CECC SA	50-012-015
IRF9130 SECC SB	50-012-015
IRF9130 SECC SC	50-012-015
IRF9130 SECC SD	50-012-015
IRF9133 SECC	50-012-015

CUSTOM HEXFET PACKAGING

Military and hi-rel requirements often dictate special packages which optimize mechanical or thermal designs and result in weight and/or space savings.

In addition to the T03 and T039 hermetic packages shown in the catalog, HEXFETs can be obtained on special order in such industry standard packages as T061, T066, 14-pin ceramic side braze, etc. Consult sales representative for more information.



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Radiation Resistance of HEXFETs®

(HEXFET is the trademark for International Rectifier Power MOSFETs)

This report presents test results that demonstrate the radiation hardness of HEXFETs in Space and Military applications.

The effects of ionizing and neutron radiation on HEXFETs are important in this type of duty, and it is necessary for the circuit designer to know what parameters are effected and by how much. Armed with this information, HEXFET circuitry can be designed to circumvent the effects of radiation, and provide reliable operation even in the most "hostile" environments.

Ionizing Radiation

The main effect of ionizing radiation is to introduce charges into the gate oxide which produce a shift in the gate-to-source threshold voltage. $V_{GS(th)}$ of N-Channel HEXFETs decreases with increasing total dose, while $V_{GS(th)}$ of P-Channel HEXFETs increases with increasing total dose. This change of threshold voltage is essentially independent of dose rate, and depends only on total dose.

HEXFET gate drive circuitry for switching applications can be designed to nullify these threshold voltage shifts by overriding them with appropriate biasing levels.

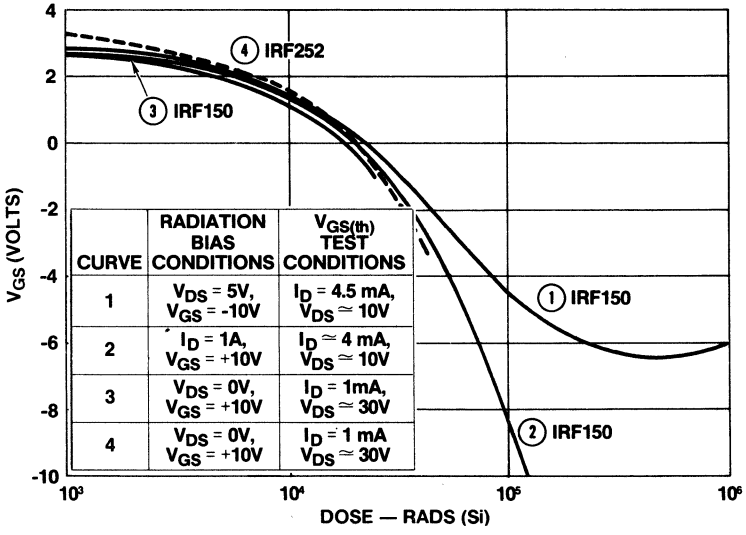
Figure 1 shows typical variation of gate-to-source threshold voltage with total dose for IRF150 and IRF252 HEXFETs, for various biasing conditions. The threshold voltage is tested with a fixed applied drain-to-source voltage. (The commonly used test condition of the gate tied to the drain can be misleading for high dose levels, because as V_{GS} decreases, V_{DS} and hence I_{DS} also tend to zero, giving and "artificial" threshold voltage reading that always remains positive.)

For the biased OFF (V_{GS} = -10V) test, (curve 1) the threshold voltage reaches about -6V at 2 x 10^5 rads, then stays practically constant at this value with further increase in radiation. The applied gate voltage of -10V ensures that the HEXFET remains fully OFF, even after 1 megarad of exposure.

The variation of threshold voltage is about the same for the biased ON (I_D = 1A, curve 2) and biased OFF V_{GS} = -10V, curve 1) test conditions, for doses up to about 30k rads. Thereafter threshold voltage decreases much more rapidly for the biased ON condition, reaching -10V at about 120k rads. This relatively rapid shift of threshold voltage for the biased ON condition must be considered and accounted for in linear applications, by providing a sufficient dynamic range of control of gate voltage. Figure 2 shows similar relationships between threshold voltage and dose rate for the IRF130 HEXFET.

In a practical switching application, the HEXFET is switched ON and OFF at the switching frequency, and the above static biasing conditions are not directly applicable. It could be expected from the above results, though, that a negative gate bias of say -10V during the OFF period would ensure correct switch OFF for total doses up to 1 megarad. This was verified by measuring the change in threshold voltage of an IRF150 HEXFET in a switching circuit after a 1 megarad dose. The operating frequency was 50kHz, and the gate was switched between ±12.0V. Peak drain current was about 2.5A, and peak drain voltage about 25V. The threshold voltage after 1 megarad was -4.4V — a shift that actually was *less* than for the above static biasing conditions.

Figure 3 shows the shift of thresh-



CURVE	RADIATION BIAS CONDITIONS	$V_{GS(th)}$ TEST CONDITIONS
1	V_{DS} = 5V, V_{GS} = -10V	I_D = 4.5 mA, $V_{DS} \simeq$ 10V
2	I_D = 1A, V_{GS} = +10V	$I_D \simeq$ 4 mA, $V_{DS} \simeq$ 10V
3	V_{DS} = 0V, V_{GS} = +10V	I_D = 1mA, $V_{DS} \simeq$ 30V
4	V_{DS} = 0V, V_{GS} = +10V	I_D = 1 mA $V_{DS} \simeq$ 30V

Figure 1. Typical Gate Threshold Voltage vs. Total Gamma (CO^{60}) Dose. IRF150 & IRF252.

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old voltage with radiation dose for a P-Channel HEXFET — the IRF9132. In this case, threshold voltage increases with increasing dose — that is, the P-Channel HEXFET becomes more biased OFF as dose increases.

Figure 4 shows the effect on drain-source leakage current of total radiation dose, for various N-Channel HEXFET types. Notice, as would be expected, that with $V_{GS} = 0$ the leakage current increases quite rapidly when a dose level is reached at which the threshold voltage approaches zero. Also to be expected, the increase of I_{DSS} with increasing dose can be largely nullified simply by applying a negative bias voltage to the gate, as shown for the IRF252 in Figure 4.

Figure 5 shows the relationship between drain-source leakage current and total dose for the IRF9132 P-Channel HEXFET. For this device the leakage current tends to saturate at a dose of about 100k rads, and does not increase further.

Table 1 shows typical values of on-resistance ($R_{DS(on)}$) and input capacitance (C_{iss}) for IRF150 and IRF130 HEXFETs, before and after 1 megarad of radiation. These results demonstrate that gamma radiation has no practical effect on these parameters.

Neutron Radiation

The effect of neutron radiation is to produce an increase in the HEXFET's on-resistance. The increase of on-resistance depends on the resistivity of the silicon — and hence the voltage rating of the HEXFET. It is almost negligible for a 100V rated HEXFET, but can be appreciable for a 400V rated device at high neutron fluence.

Figure 6 shows typical measured relationships between on-resistance and neutron fluence level for 100V and 400V rated HEXFETs. On-resistance of the 100V hardly increases up to a fluence of 2×10^{13} neutr/cm^2, while at 10^{14} neutr/cm^2 it shows about a 30% increase. The 400V HEXFET's on-resistance increases by about 25% at 2×10^{13} neutr/cm^2, and by about 150% at 10^{14} neutr/cm^2.

The increase of on-resistance caused by neutron radiation will result in increased conduction losses in switching applications, but will have little practical effect in linear applications. It can be allowed for at the design stage by appropriate choice of the HEXFET/heatsink combination.

Conclusion

The primary effect of ionizing radiation on HEXFETs is to cause a decrease in the threshold voltage of

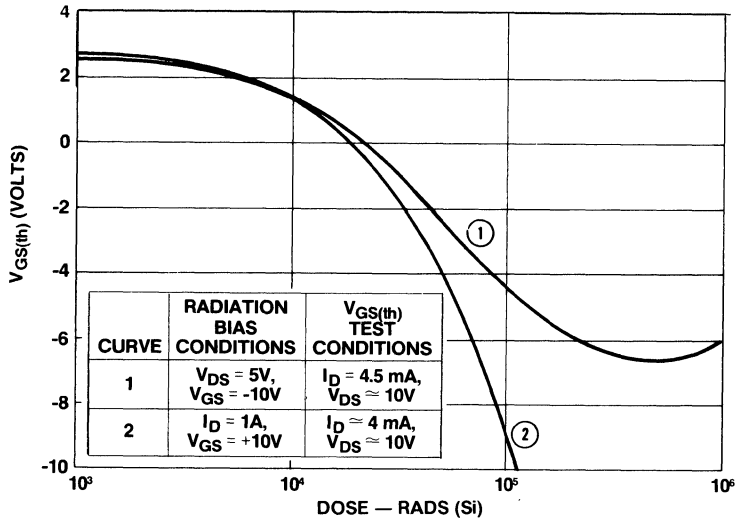


Figure 2. Gate Threshold Voltage vs. Total Gamma (CO^{60}) Dose. IRF130.

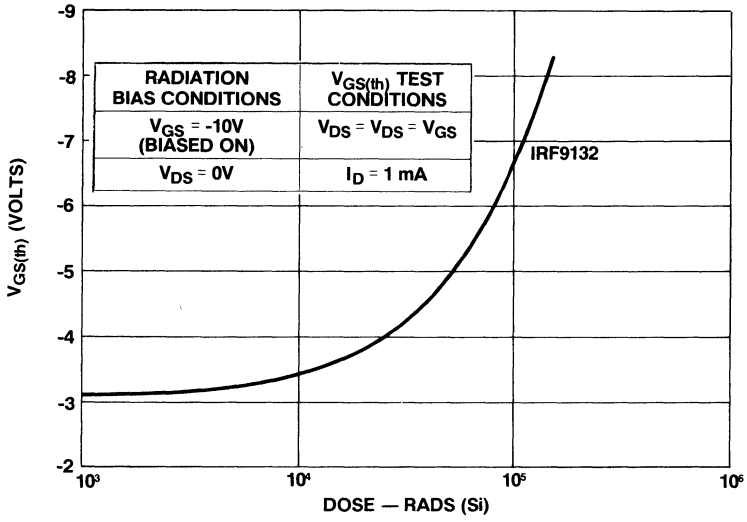


Figure 3. Typical Gate Threshold Voltage vs. Total Dose (150KV) X-ray. IRF9132.

TABLE 1: $R_{DS(on)}$ and C_{iss} before and after 1 megarad ionizing (Co^{60}) radiation.

IRF150				IRF130			
$R_{DS(on)}$ ohms		C_{iss} pF		$R_{DS(on)}$ ohms		C_{iss} pF	
Before	After	Before	After	Before	After	Before	After
0.38	0.35	2480	2500	0.127	0.111	515	520
0.34	0.34	2500	2530	0.128	0.135	510	540
0.33	0.31	2500	2590	0.127	0.106	673	710

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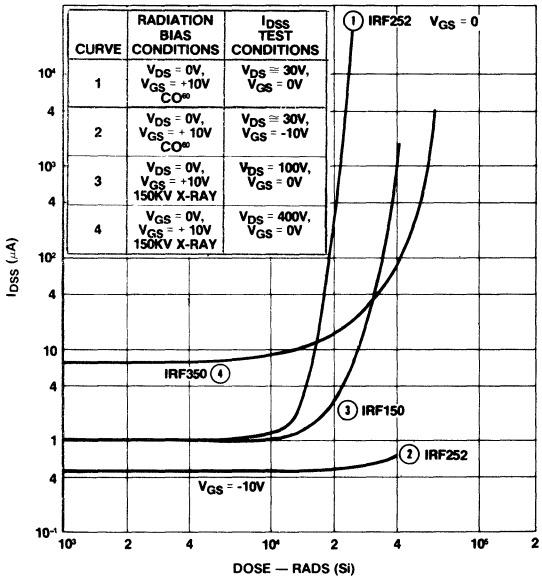


Figure 4. Typical Drain-Source Leakage Current vs. Total Dose. IRF150, IRF252 & IRF350.

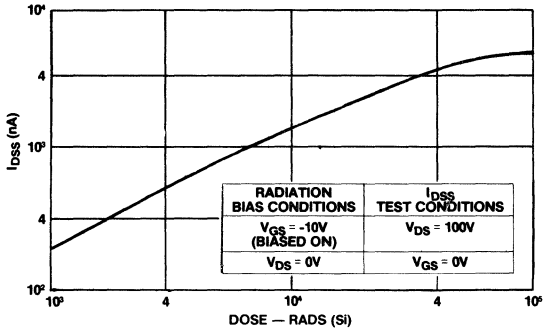


Figure 5. Typical Drain-Source Leakage Current vs. Total Dose (150KV X-ray). IRF9132.

N-Channel types and an increase for P-Channel types. The amount of change of threshold voltage is a function of the biasing conditions, particularly at radiation doses which are sufficient to change the polarity of the threshold voltage (N-Channel HEXFETs) — typically -10V — allows reliable switching operation at doses up to at least 1 megarad (Si).

The primary effect of neutron radiation is to cause an increase in on-resistance. This is almost negligible for low voltage (100V) HEXFETs, but can be significant at higher neutron fluence levels for higher voltage types. By allowing for the increase of on-resistance at the design stage, predictable and reliable operation of HEXFETs in a neutron radiation environment can be readily achieved.□

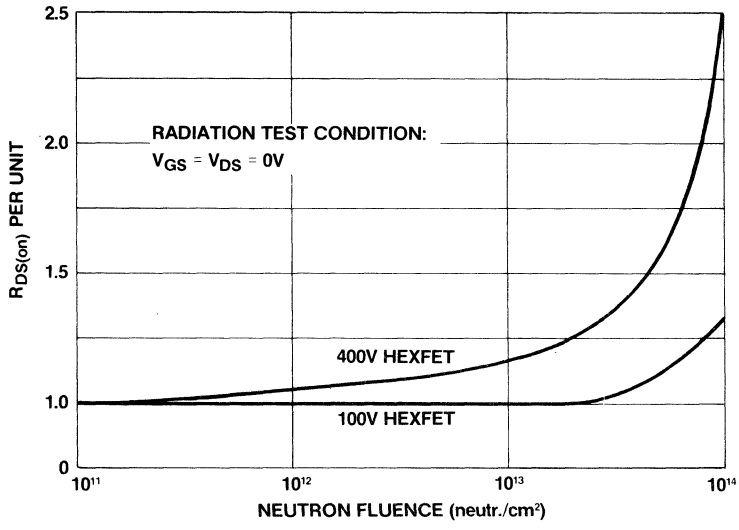


Figure 6. On-resistance vs. Neutron Fluence Level.

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Life, Power-Age, Environmental and Military Test Capabilities

1. Life Tests and Power-Age Capabilities

International Rectifier has complete facilities to provide life tests and power-age on all devices which they manufacture.

A. High temperature storage life testing up to 200°C.

B. Voltage temperature stress tests at both ambient and elevated conditions.

C. Free air operation life. Test capability, 1000 positions for power transistors, and 1500 positions for power diodes.

D. HTRB test capabilities. Several thousands of positions for V_{GS} and for V_{DS} burn-in.

E. Computerized readout equipment.

2. Environmental Test Capabilities

TEST	CAPABILITY
Acceleration, Sustained (Centrifuge)	50-30,000g (Standard)
Altitude (Barometric Pressure, Reduced)	450,000 Ft. Simulated Altitude with T_A=25°C Capability
Moisture Resistance	25-85°C 85% RH
Salt Atmosphere/Spray	25°C to 71°C, up to 20% Salt Solution by Weight
Seal-Gross, Fine Leak	1 X 10^{-8} atm cc/sec, Fluorocarbons, Mineral Oils, FC-43, Hydrostatic Pressure: 0 - 100psig
Symbolization (Resistance to Solvents)	
Shock (Mechanical)	Pulse Shape - Approximately Half-sine 500 - 1500g at 0.5 - 1.0 msec
Solderability	Up to 280°C
Temperature Cycling	-65° C to 200° C
Terminal Strength (Lead Integrity)	Lead Fatigue, Tension, Stud Torque, Terminal Torque
Thermal Shock	-65°C to 200°C
Vibration, Fatigue	60Hz, 5 - 20g
Vibration, Variable	5 - 2000 Hz as Limited by 1 inch DA and 60 inches/second Velocity; 0-20g (Standard)

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3. Military Test Standard Capabilities

TEST CATEGORY	MIL-STD-202	MIL-STD-750
Barometric Pressure (reduced)	Method 105 All Conditions	Method 1001 All Conditions
Moisture Resistance	Method 106	Method 1021
Resistance to Solvents	Method 215	Method 1022
Salt Atmosphere	Method 101 All Conditions	Method 1041
Seal, Gross Leak	Method 112B, Conditions A,B & D	Method 1071 Conditions C,D & F
Seal, Fine Leak	Only Method 112B, Condition C Procedure IIIA	Method 1071, Condition H
Solderability	Method 208	Method 2026
Soldering Heat	Method 210 All Conditions	Method 2031
Temperature Cycling	Method 102 All Conditions	Method 1051 All Conditions
Terminal Strength	Method 211 All Conditions	Method 2036 All Conditions
Terminal Shock (Glass Strain)	Method 107 All Conditions	Method 1056 All Conditions
Acceleration, Sustained (Centrifuge)	Method 212 All Conditions	Method 2006
Shock (Mechanical)	Method 213 Conditions D,E & F	Method 2016
Vibration, Fatigue	Method 201	Method 2046
Vibration, Variable Frequency	Method 204	Method 2056

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HEXFET DEVICE CHARACTERISTICS AND RATINGS

The HEXFET devices listed in this DATABOOK represent the International Rectifier power MOSFET line as of August, 1982. Some changes to earlier published Data Sheets have been made. Therefore the data presented here supersedes all previous specifications.

Reference is made to all previous Data Sheets in the upper corner of each page beginning a specific series. This will permit holders of previous materials to compare the current data with that appearing on the earlier Data Sheets, if necessary.

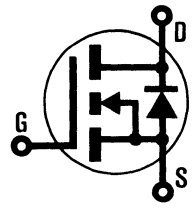
In the interest of product improvement, International Rectifier reserves the right to change specifications at any time without notice.

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS 2N6755
2N6756

JEDEC REGISTERED N-CHANNEL POWER MOSFETs



2N6756 AVAILABLE AS JAN, JANTX AND JANTXV QUALIFIED PER MIL-S-19500/542A

100 Volt, 0.18 Ohm HEXFET

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

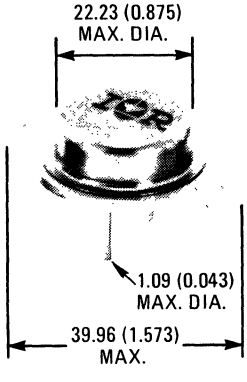
Features:

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

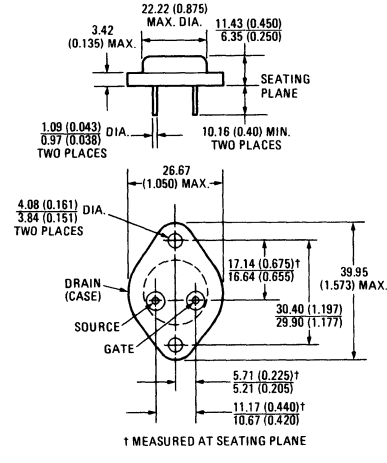
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
2N6755	60V	0.25Ω	12A
2N6756	100V	0.18Ω	14A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



† MEASURED AT SEATING PLANE

Conforms to JEDEC Outline TO-204AA (TO-3)
Dimensions in Millimeters and (Inches)

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Absolute Maximum Ratings

Parameter		2N6755	2N6756	Units
V_{DS}	Drain – Source Voltage	60*	100*	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 1 MΩ)	60*	100*	V
I_D @ T_C = 25°C	Continuous Drain Current	12*	14*	A
I_D @ T_C = 100°C	Continuous Drain Current	8.0*	9.0*	A
I_{DM}	Pulsed Drain Current	25	30	A
V_{GS}	Gate – Source Voltage	±20*		V
P_D @ T_C = 25°C	Max. Power Dissipation	75* (See Fig. 11)		W
P_D @ T_C = 100°C	Max. Power Dissipation	30* (See Fig. 11)		W
	Linear Derating Factor	0.6* (See Fig. 11)		W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH		A
		25	30	
T_J T_{stg}	Operating and Storage Temperature Range	-55* to 150*		°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)		°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6755	60	–	–	V	V_{GS} = 0
		2N6756	100	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6755	–	–	3.0*	V	V_{GS} = 10V, I_D = 12A
		2N6756	–	–	2.52*	V	V_{GS} = 10V, I_D = 14A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6755	–	0.20	0.25*	Ω	V_{GS} = 10V, I_D = 8A
		2N6756	–	0.14	0.18*	Ω	V_{GS} = 10V, I_D = 9A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6755	–	–	0.45*	Ω	V_{GS} = 10V, I_D = 8A, T_C = 125°C
		2N6756	–	–	0.33*	Ω	V_{GS} = 10V, I_D = 9A, T_C = 125°C
g_{fs}	Forward Transconductance ①	ALL	4.0*	5.5	12.0*	S (℧)	V_{DS} = 15V, I_D = 9A
C_{iss}	Input Capacitance	ALL	350*	600	800*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	150*	300	500*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	50*	100	150*	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	–	–	30*	ns	$V_{DD} \cong$ 36V, I_D = 9A, Z_o = 15Ω
t_r	Rise Time	ALL	–	–	75*	ns	(See Figs. 13 and 14)
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	–	–	40*	ns	(MOSFET switching times are essentially
t_f	Fall Time	ALL	–	–	45*	ns	independent of operating temperature.)

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67*	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6755	–	–	12*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		2N6756	–	–	14*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6755	–	–	25	A	
		2N6756	–	–	30		
V_{SD}	Diode Forward Voltage ①	2N6755	0.85*	–	1.7*	V	T_C = 25°C, I_S = 12A, V_{GS} = 0
		2N6756	0.90*	–	1.8*	V	T_C = 25°C, I_S = 14A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	300	–	ns	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.0	–	μC	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

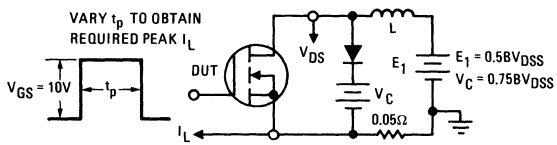


Fig. 1 – Clamped Inductive Test Circuit

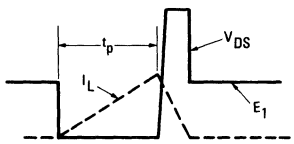


Fig. 2 – Clamped Inductive Waveforms

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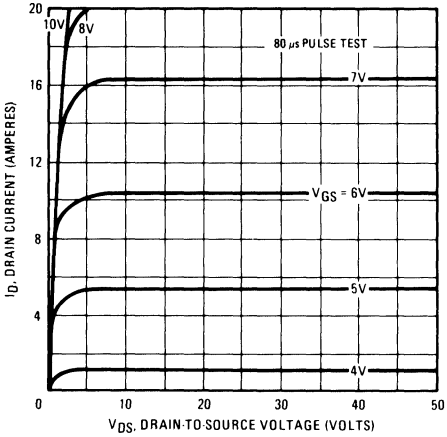


Fig. 3 — Typical Output Characteristics

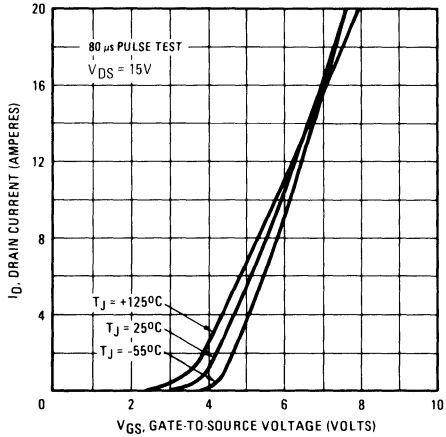


Fig. 4 — Typical Transfer Characteristics

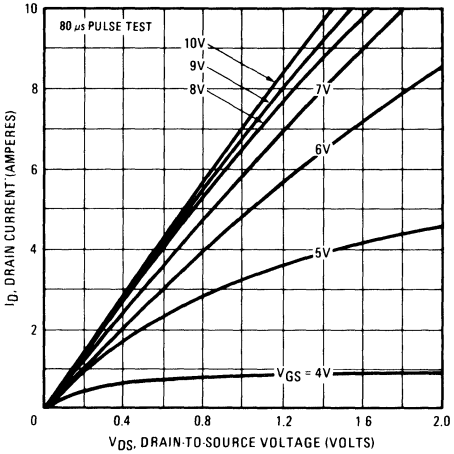


Fig. 5— Typical Saturation Characteristics (2N6755)

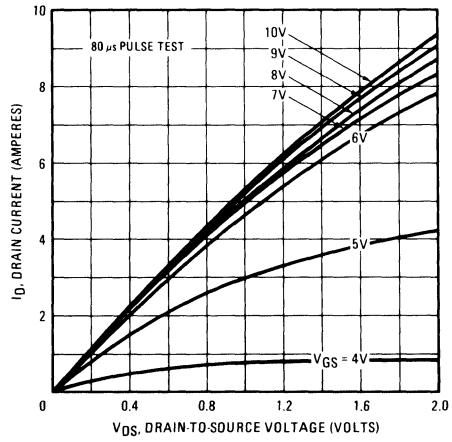


Fig. 6— Typical Saturation Characteristics (2N6756)

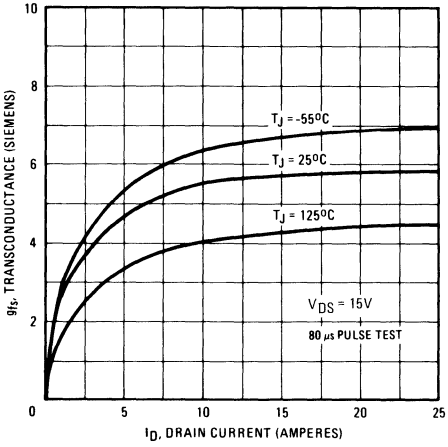


Fig. 7 — Typical Transconductance Vs. Drain Current

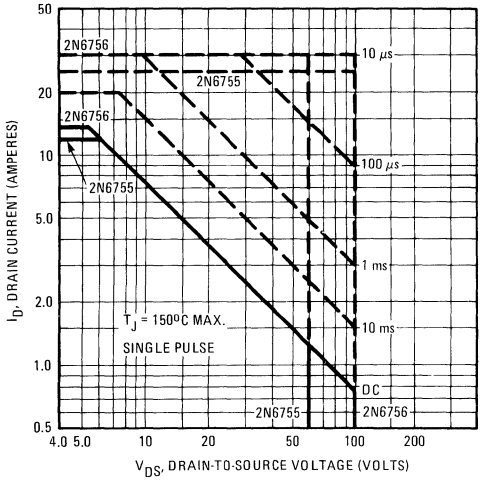


Fig. 8 — Maximum Safe Operating Area

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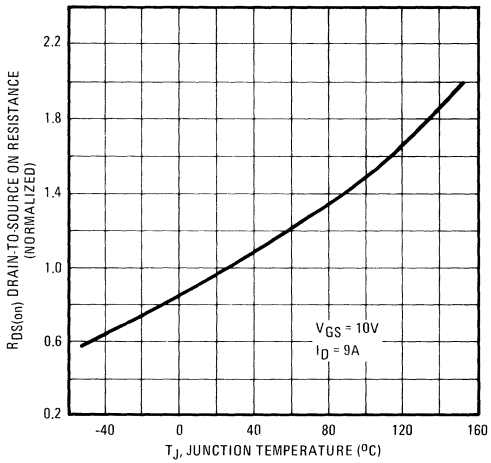


Fig. 9 — Normalized Typical On-Resistance Vs. Temperature

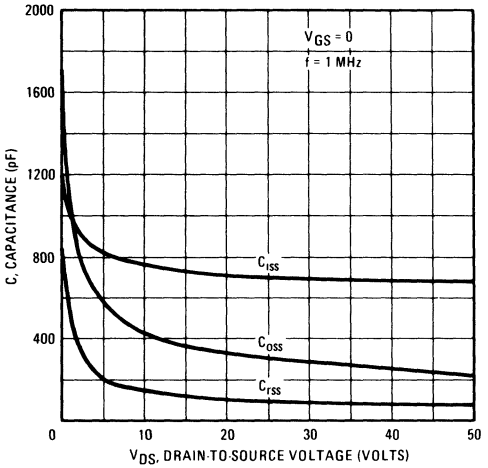


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

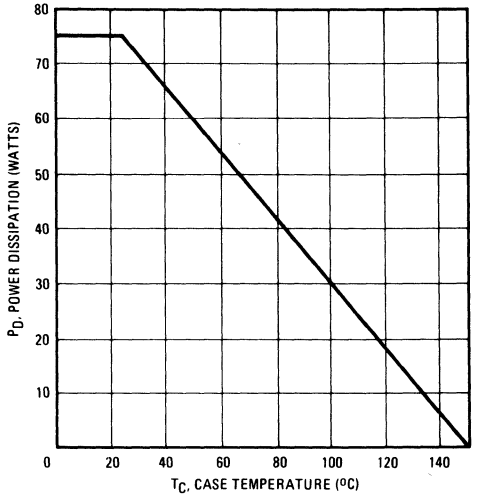


Fig. 11 — Power Vs. Temperature Derating Curve

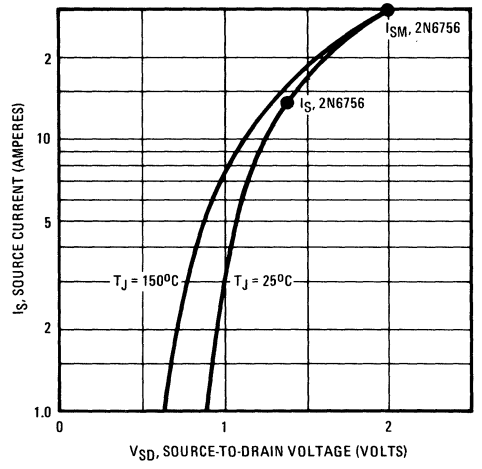


Fig. 12 — Typical Body-Drain Diode Forward Voltage

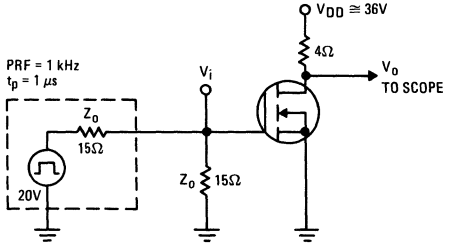


Fig. 13 — Switching Time Test Circuit

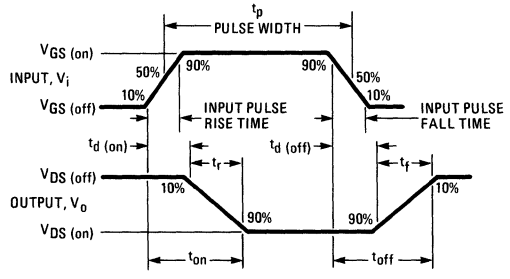


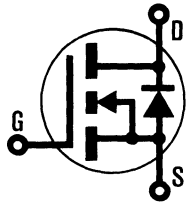
Fig. 14 — Switching Time Waveforms

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS 2N6757 2N6758

JEDEC REGISTERED N-CHANNEL POWER MOSFETs



2N6758 AVAILABLE AS JAN, JANTX AND JANTXV QUALIFIED PER MIL-S-19500/542A

200 Volt, 0.4 Ohm HEXFET

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

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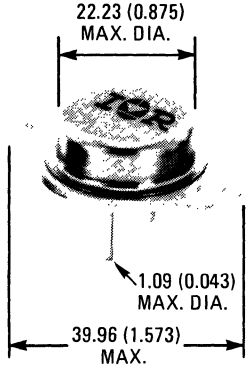
Features:

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

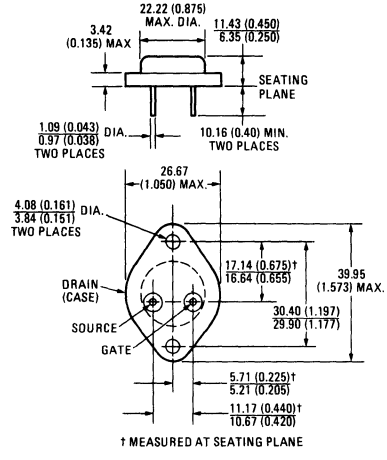
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
2N6757	150V	0.6Ω	8A
2N6758	200V	0.4Ω	9A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Conforms to JEDEC Outline TO-204AA (TO-3)
Dimensions in Millimeters and (Inches)

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Absolute Maximum Ratings

Parameter		2N6757	2N6758	Units
V_{DS}	Drain – Source Voltage	150*	200*	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 1 MΩ)	150*	200*	V
I_D @ T_C = 25°C	Continuous Drain Current	8.0*	9.0*	A
I_D @ T_C = 100°C	Continuous Drain Current	5.0*	6.0*	A
I_{DM}	Pulsed Drain Current	12	15	A
V_{GS}	Gate – Source Voltage	±20*		V
P_D @ T_C = 25°C	Max. Power Dissipation	75* (See Fig. 11)		W
P_D @ T_C = 100°C	Max. Power Dissipation	30* (See Fig. 11)		W
	Linear Derating Factor	0.6* (See Fig. 11)		W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH		A
		12	15	
T_J T_{stg}	Operating and Storage Temperature Range	-55* to 150*		°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)		°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6757	150	–	–	V	V_{GS} = 0
		2N6758	200	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6757	–	–	4.8*	V	V_{GS} = 10V, I_D = 8A
		2N6758	–	–	3.6*	V	V_{GS} = 10V, I_D = 9A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6757	–	0.4	0.6*	Ω	V_{GS} = 10V, I_D = 5A
		2N6758	–	0.25	0.4*	Ω	V_{GS} = 10V, I_D = 6A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6757	–	–	1.13*	Ω	V_{GS} = 10V, I_D = 5A, T_C = 125°C
		2N6758	–	–	0.75*	Ω	V_{GS} = 10V, I_D = 6A, T_C = 125°C
g_{fs}	Forward Transconductance ①	ALL	3.0*	5.0	9.0*	S (℧)	V_{DS} = 15V, I_D = 6A
C_{iss}	Input Capacitance	ALL	350*	600	800*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	100*	250	450*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	40*	80	150*	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30*	ns	V_{DD} ≅ 90V, I_D = 6A, Z_o = 15Ω (See Figs. 13 and 14) (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	50*	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	50*	ns	
t_f	Fall Time	ALL	–	–	40*	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67*	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6757	–	–	8.0*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		2N6758	–	–	9.0*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6757	–	–	12	A	
		2N6758	–	–	15		
V_{SD}	Diode Forward Voltage ①	2N6757	0.75*	–	1.50*	V	T_C = 25°C, I_S = 8A, V_{GS} = 0
		2N6758	0.80*	–	1.60*	V	T_C = 25°C, I_S = 9A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	650	–	ns	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	10	–	μC	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

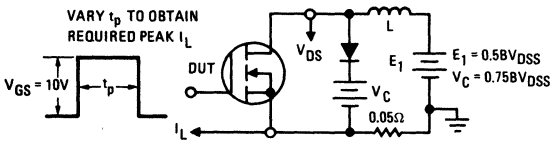


Fig. 1 – Clamped Inductive Test Circuit

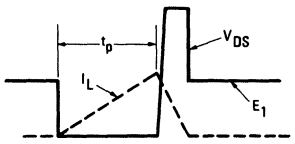


Fig. 2 – Clamped Inductive Waveforms

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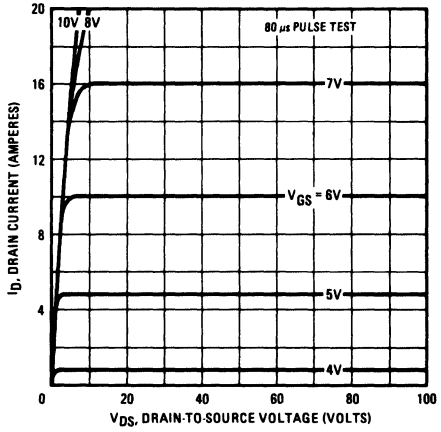


Fig. 3 – Typical Output Characteristics

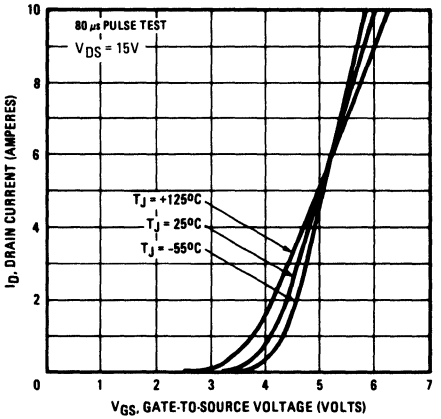


Fig. 4 – Typical Transfer Characteristics

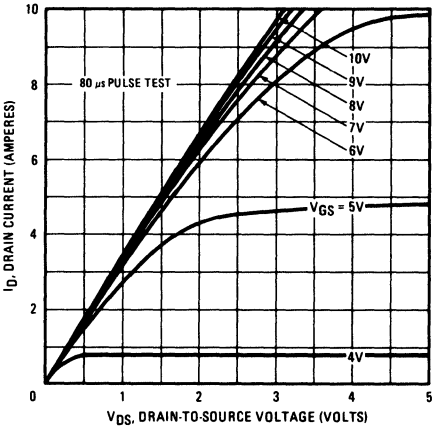


Fig. 5– Typical Saturation Characteristics (2N6757)

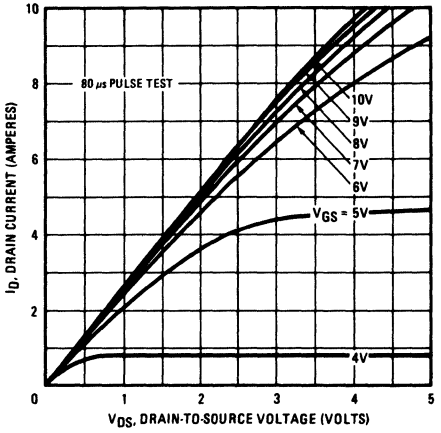


Fig. 6– Typical Saturation Characteristics (2N6758)

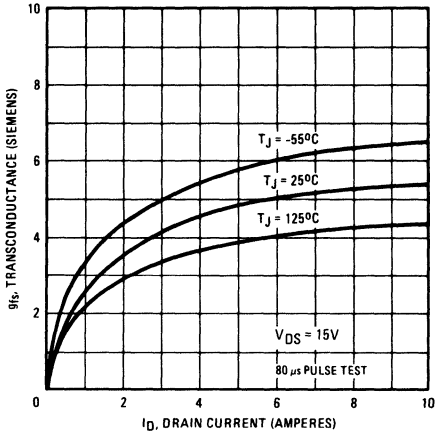


Fig. 7 – Typical Transconductance Vs. Drain Current

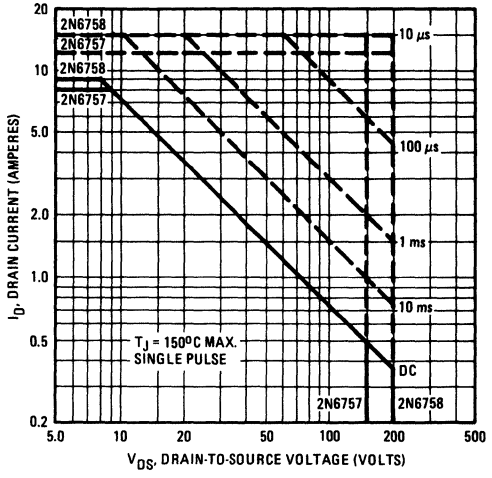


Fig. 8 – Maximum Safe Operating Area

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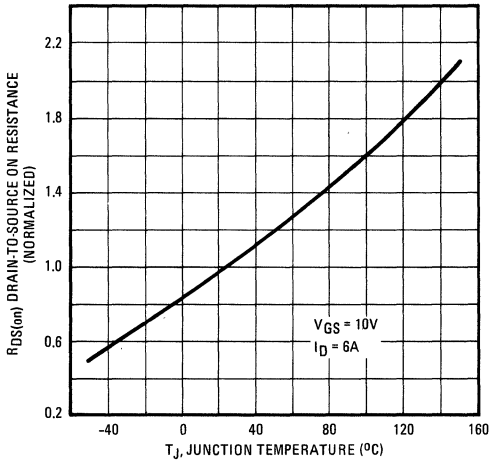


Fig. 9 — Normalized Typical On-Resistance Vs. Temperature

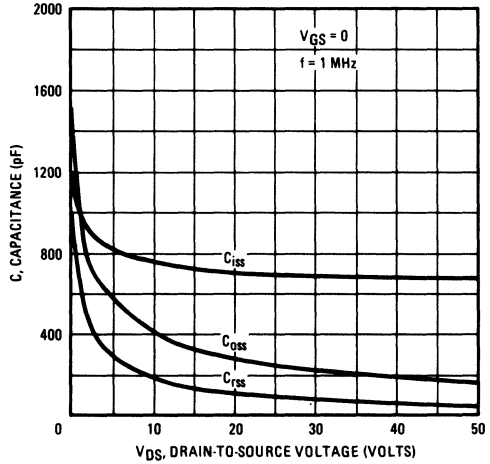


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

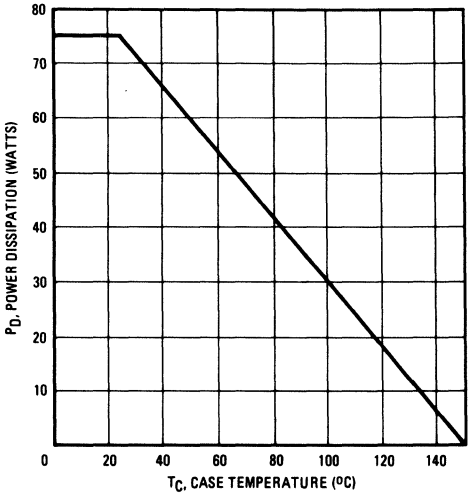


Fig. 11 — Power Vs. Temperature Derating Curve

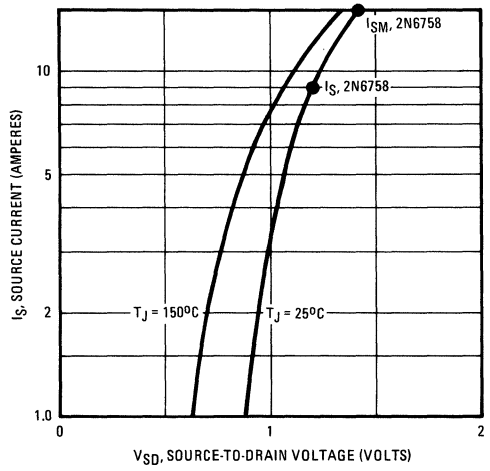


Fig. 12 — Typical Body-Drain Diode Forward Voltage

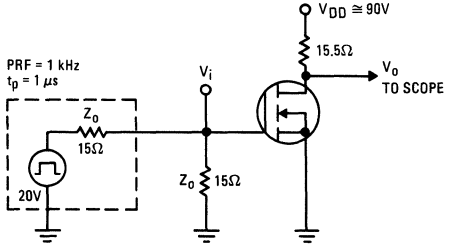


Fig. 13 — Switching Time Test Circuit

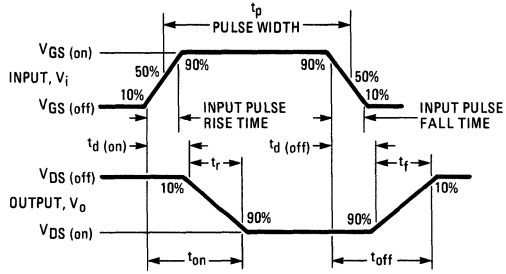


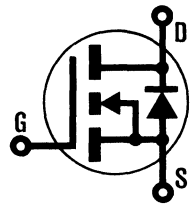
Fig. 14 — Switching Time Waveforms

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS 2N6759 2N6760

JEDEC REGISTERED N-CHANNEL POWER MOSFETs



2N6760 AVAILABLE AS JAN, JANTX AND JANTXV QUALIFIED PER MIL-S-19500/542A

400 Volt, 1.0 Ohm HEXFET

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

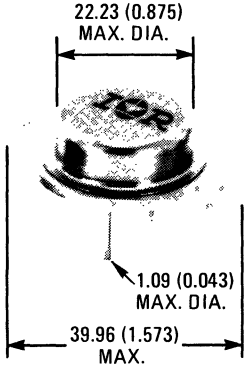
Features:

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

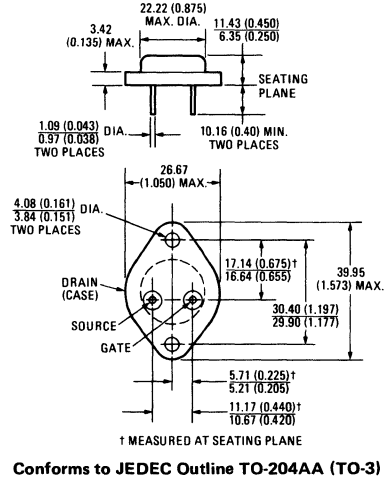
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
2N6759	350V	1.5Ω	4.5A
2N6760	400V	1.0Ω	5.5A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



† MEASURED AT SEATING PLANE

Conforms to JEDEC Outline TO-204AA (TO-3)
Dimensions in Millimeters and (Inches)

Downloaded from Arrow.com.

Absolute Maximum Ratings

Parameter		2N6759	2N6760	Units
V_{DS}	Drain – Source Voltage	350*	400*	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 1 MΩ)	350*	400*	V
I_D @ T_C = 25°C	Continuous Drain Current	4.5*	5.5*	A
I_D @ T_C = 100°C	Continuous Drain Current	3.0*	3.5*	A
I_{DM}	Pulsed Drain Current	7.0	8.0	A
V_{GS}	Gate – Source Voltage	±20*		V
P_D @ T_C = 25°C	Max. Power Dissipation	75* (See Fig. 11)		W
P_D @ T_C = 100°C	Max. Power Dissipation	30* (See Fig. 11)		W
	Linear Derating Factor	0.6* (See Fig. 11)		W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH		A
		7.0	8.0	
T_J T_{stg}	Operating and Storage Temperature Range	-55* to 150*		°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)		°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6759	350	–	–	V	V_{GS} = 0
		2N6760	400	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6759	–	–	7.0*	V	V_{GS} = 10V, I_D = 4.5A
		2N6760	–	–	6.7*	V	V_{GS} = 10V, I_D = 5.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6759	–	1.0	1.5*	Ω	V_{GS} = 10V, I_D = 3A
		2N6760	–	0.8	1.0*	Ω	V_{GS} = 10V, I_D = 3.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6759	–	–	3.3*	Ω	V_{GS} = 10V, I_D = 3A, T_C = 125°C
		2N6760	–	–	2.2*	Ω	V_{GS} = 10V, I_D = 3.5A, T_C = 125°C
g_{fs}	Forward Transconductance ①	ALL	3.0*	4.5	9.0*	S (℧)	V_{DS} = 15V, I_D = 3.5A
C_{iss}	Input Capacitance	ALL	350*	600	800*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	50*	150	300*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	20*	40	80*	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	–	–	30*	ns	V_{DD} ≅ 175V, I_D = 3.5A, Z_o = 15Ω
t_r	Rise Time	ALL	–	–	35*	ns	(See Figs. 13 and 14)
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	–	–	55*	ns	(MOSFET switching times are essentially
t_f	Fall Time	ALL	–	–	35*	ns	independent of operating temperature.)

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67*	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6759	–	–	4.5*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		2N6760	–	–	5.5*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6759	–	–	7.0	A	
		2N6760	–	–	8.0		
V_{SD}	Diode Forward Voltage ①	2N6759	0.70*	–	1.4*	V	T_C = 25°C, I_S = 4.5A, V_{GS} = 0
		2N6760	0.75*	–	1.5*	V	T_C = 25°C, I_S = 5.5A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	550	–	ns	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	8.0	–	μC	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

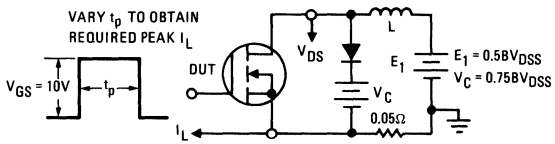


Fig. 1 – Clamped Inductive Test Circuit

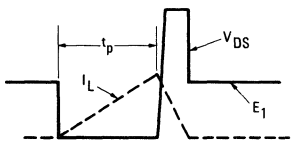


Fig. 2 – Clamped Inductive Waveforms

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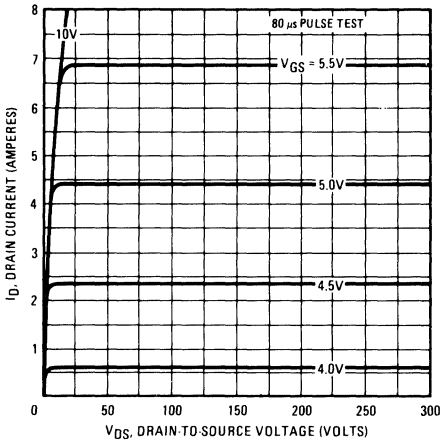


Fig. 3 — Typical Output Characteristics

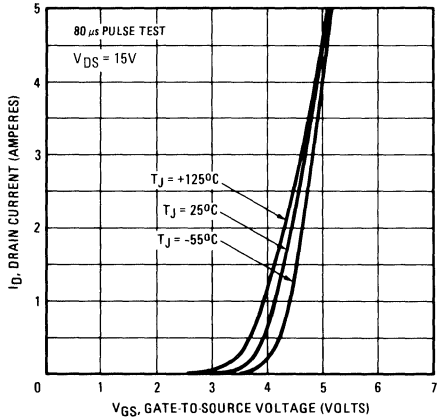


Fig. 4 — Typical Transfer Characteristics

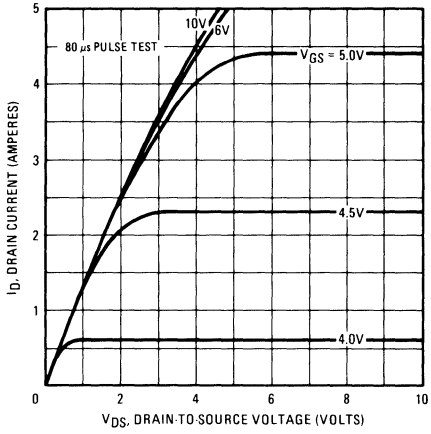


Fig. 5— Typical Saturation Characteristics (2N6759)

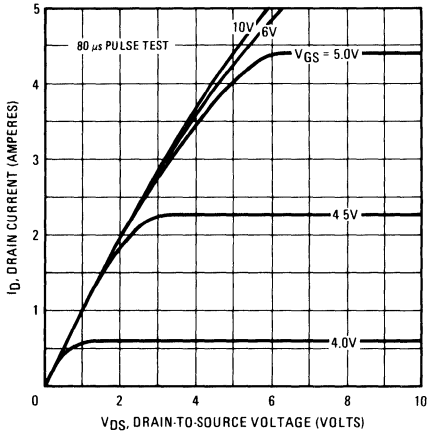


Fig. 6— Typical Saturation Characteristics (2N6760)

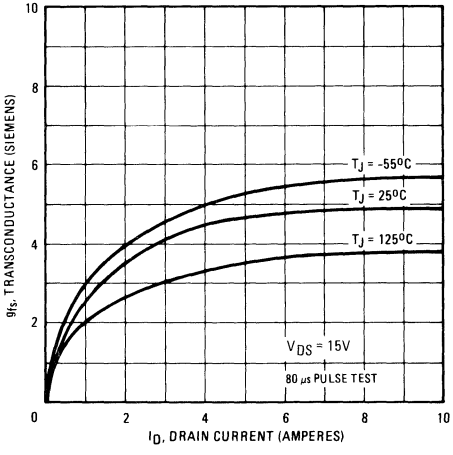


Fig. 7 — Typical Transconductance Vs. Drain Current

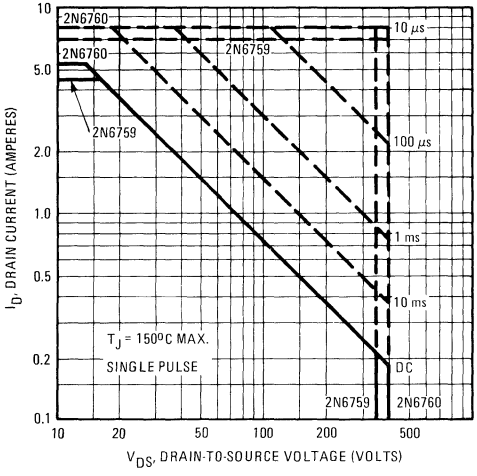


Fig. 8 — Maximum Safe Operating Area

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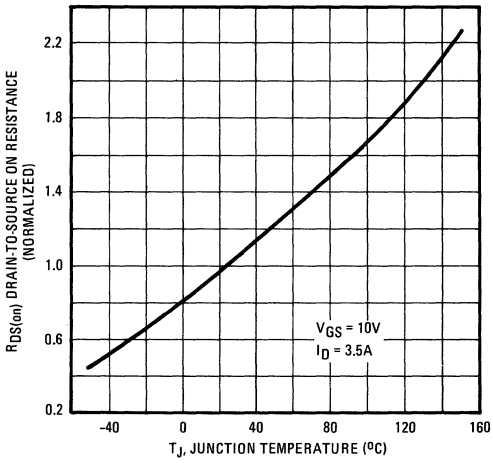


Fig. 9 — Normalized Typical On-Resistance Vs. Temperature

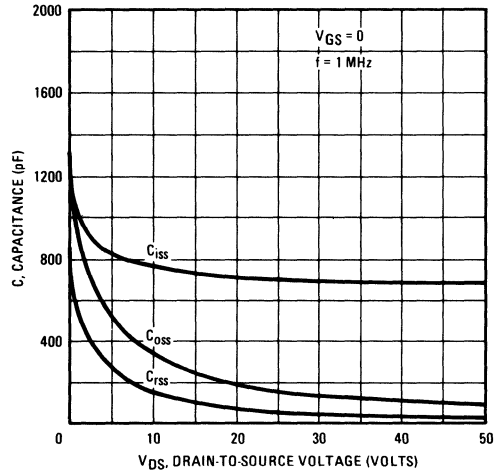


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

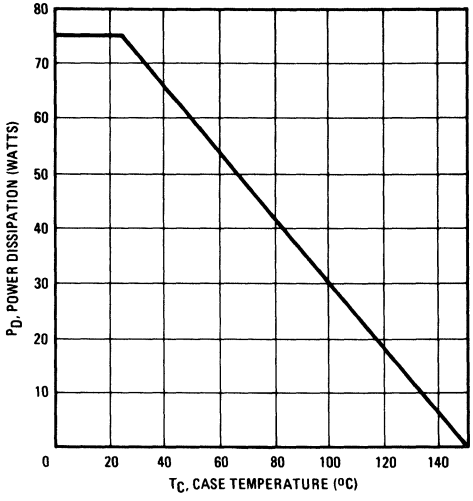


Fig. 11 — Power Vs. Temperature Derating Curve

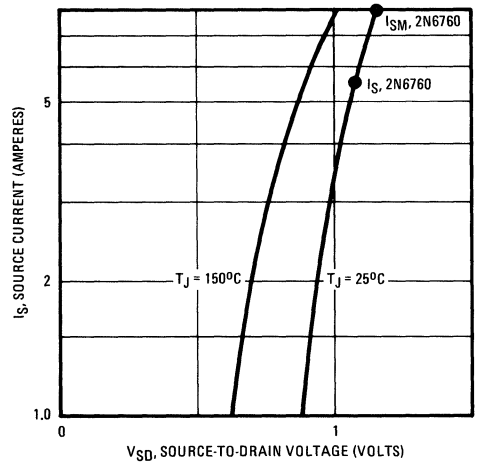


Fig. 12 — Typical Body-Drain Diode Forward Voltage

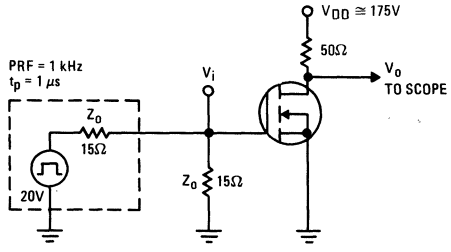


Fig. 13 — Switching Time Test Circuit

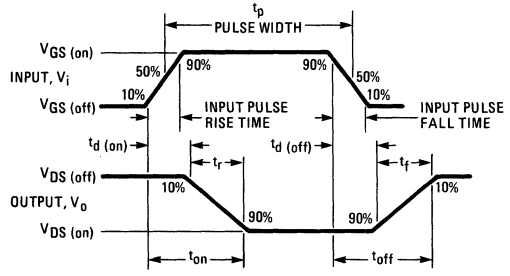


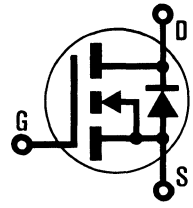
Fig. 14 — Switching Time Waveforms

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS 2N6761 2N6762

JEDEC REGISTERED N-CHANNEL POWER MOSFETs



500 Volt, 1.5 Ohm HEXFET

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

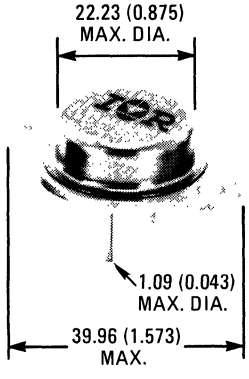
Features:

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

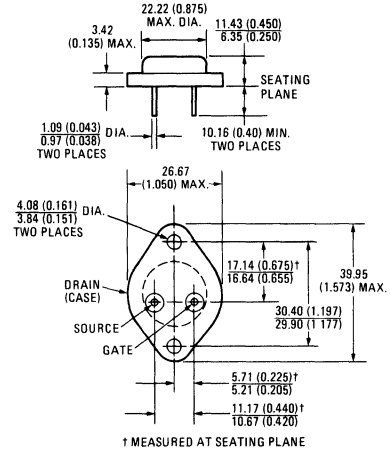
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
2N6761	450V	2.0Ω	4.0A
2N6762	500V	1.5Ω	4.5A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



† MEASURED AT SEATING PLANE

Conforms to JEDEC Outline TO-204AA (TO-3)
Dimensions in Millimeters and (Inches)

Downloaded from Arrow.com.

Absolute Maximum Ratings

Parameter		2N6761	2N6762	Units
V_{DS}	Drain – Source Voltage	450*	500*	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 1 MΩ)	450*	500*	V
I_D @ T_C = 25°C	Continuous Drain Current	4.0*	4.5*	A
I_D @ T_C = 100°C	Continuous Drain Current	2.5*	3.0*	A
I_{DM}	Pulsed Drain Current	6.0	7.0	A
V_{GS}	Gate – Source Voltage	±20*		V
P_D @ T_C = 25°C	Max. Power Dissipation	75* (See Fig. 11)		W
P_D @ T_C = 100°C	Max. Power Dissipation	30* (See Fig. 11)		W
	Linear Derating Factor	0.6* (See Fig. 11)		W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH		A
		6.0	7.0	
T_J T_{stg}	Operating and Storage Temperature Range	-55* to 150*		°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)		°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6761	450	–	–	V	V_{GS} = 0
		2N6762	500	–	–	V	I_D = 4.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = 0.8 x Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 25°C to 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6761	–	–	8.0*	V	V_{GS} = 10V, I_D = 4A
		2N6762	–	–	7.7*	V	V_{GS} = 10V, I_D = 4.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6761	–	1.5	2.0*	Ω	V_{GS} = 10V, I_D = 2.5A
		2N6762	–	1.3	1.5*	Ω	V_{GS} = 10V, I_D = 3.0A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6761	–	–	4.4*	Ω	V_{GS} = 10V, I_D = 2.5A, T_C = 125°C
		2N6762	–	–	3.3*	Ω	V_{GS} = 10V, I_D = 3.0A, T_C = 125°C
g_{fs}	Forward Transconductance ①	ALL	2.5*	3.5	7.5*	S (℧)	V_{DS} = 16V, I_D = 3A
C_{iss}	Input Capacitance	ALL	350*	600	800*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	25*	100	200*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	15*	30	60*	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	–	–	30*	ns	$V_{DD} \cong$ 225V, I_D = 3A, Z_o = 15Ω (See Figs. 13 and 14) (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	30*	ns	
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	–	–	55*	ns	
t_f	Fall Time	ALL	–	–	30*	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67*	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6761	–	–	4.0*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		2N6762	–	–	4.5*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6761	–	–	6.0	A	
		2N6762	–	–	7.0		
V_{SD}	Diode Forward Voltage ①	2N6761	0.65*	–	1.3*	V	T_C = 25°C, I_S = 4A, V_{GS} = 0
		2N6762	0.7*	–	1.4*	V	T_C = 25°C, I_S =4.5A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	500	–	ns	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	7.0	–	μC	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

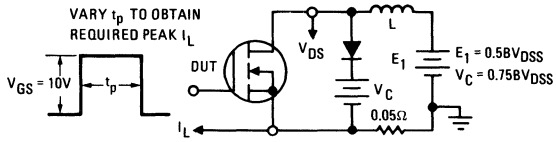


Fig. 1 — Clamped Inductive Test Circuit

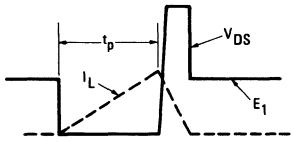


Fig. 2 — Clamped Inductive Waveforms

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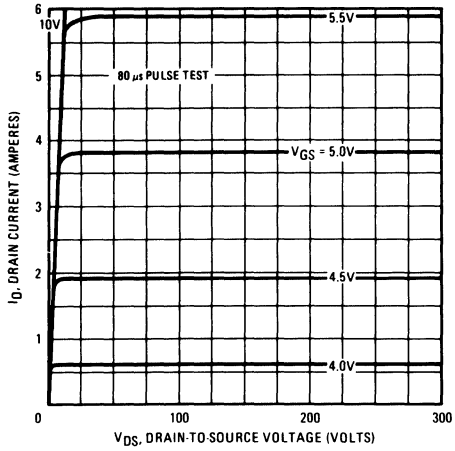


Fig. 3 — Typical Output Characteristics

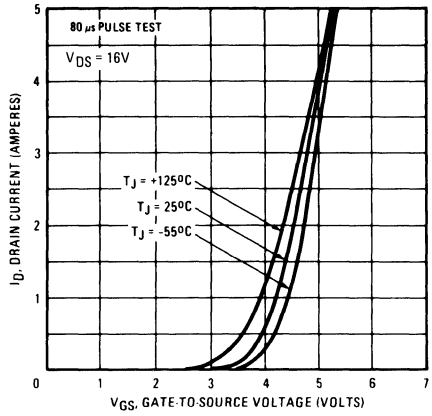


Fig. 4 — Typical Transfer Characteristics

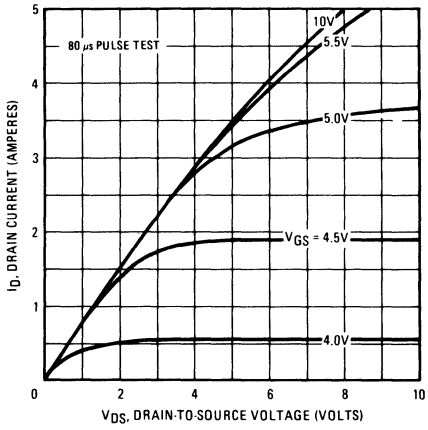


Fig. 5— Typical Saturation Characteristics (2N6761)

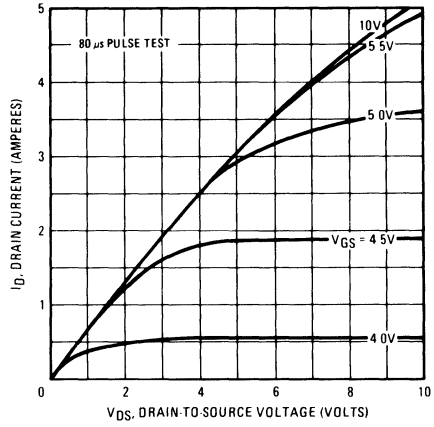


Fig. 6— Typical Saturation Characteristics (2N6762)

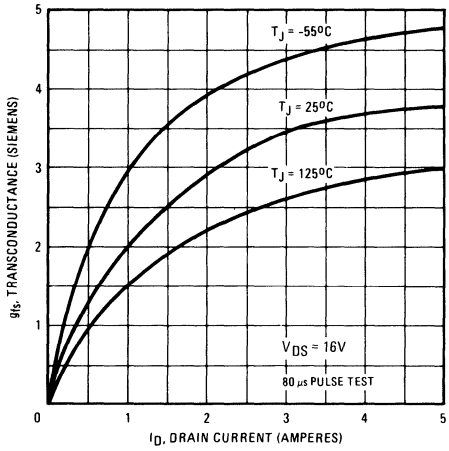


Fig. 7 — Typical Transconductance Vs. Drain Current

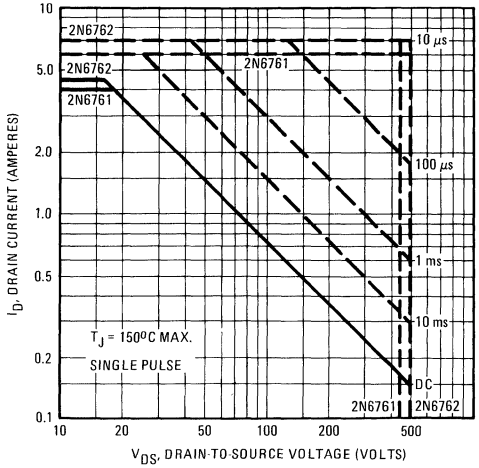


Fig. 8 — Maximum Safe Operating Area

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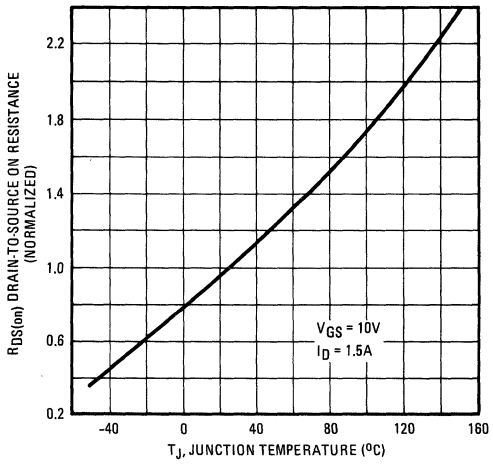


Fig. 9 — Normalized Typical On-Resistance Vs. Temperature

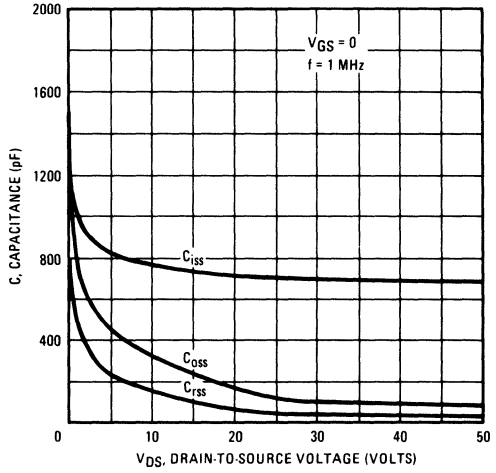


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

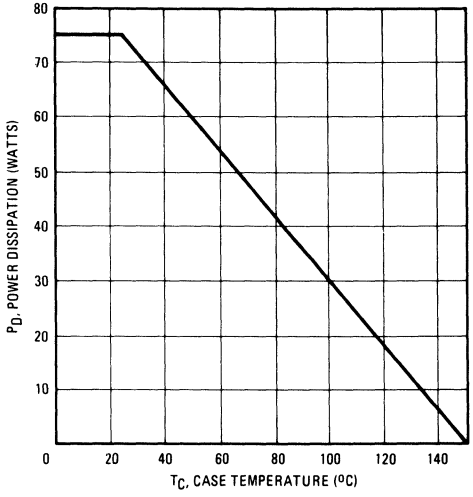


Fig. 11 — Power Vs. Temperature Derating Curve

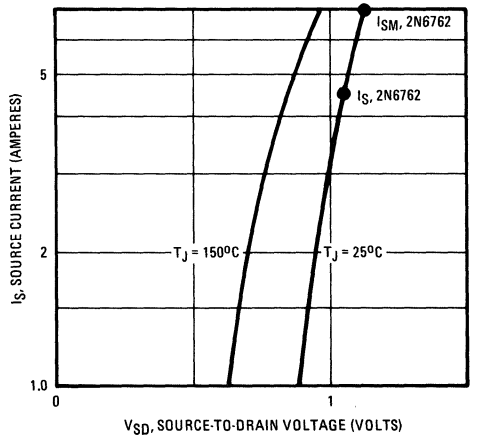


Fig. 12 — Typical Body-Drain Diode Forward Voltage

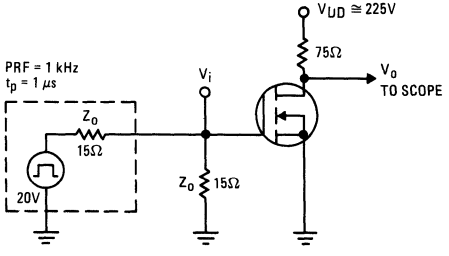


Fig. 13 — Switching Time Test Circuit

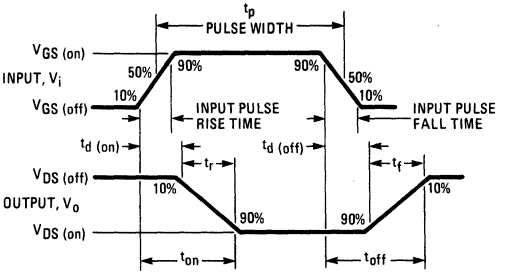


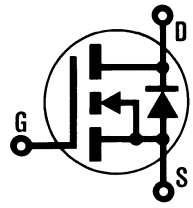
Fig. 14 — Switching Time Waveforms

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS 2N6763 2N6764

JEDEC REGISTERED N-CHANNEL POWER MOSFETs



2N6764 AVAILABLE AS JAN, JANTX AND JANTXV QUALIFIED PER MIL-S-19500/543A

100 Volt, 0.055 Ohm HEXFET

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

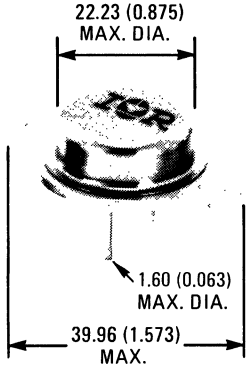
Features:

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

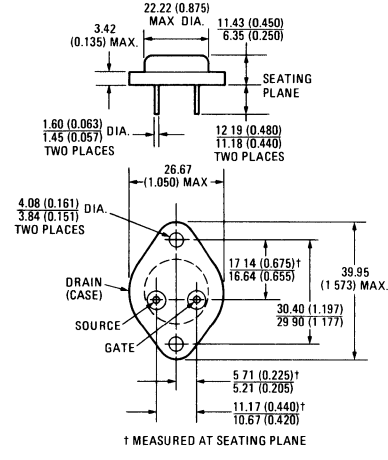
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
2N6763	60V	0.08Ω	31A
2N6764	100V	0.055Ω	38A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



† MEASURED AT SEATING PLANE

Conforms to JEDEC Outline TO-204AE (Modified TO-3)
Dimensions in Millimeters and (Inches)

Downloaded from Arrow.com.

Absolute Maximum Ratings

Parameter		2N6763	2N6764	Units
V_{DS}	Drain – Source Voltage	60*	100*	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 1 MΩ)	60*	100*	V
I_D @ T_C = 25°C	Continuous Drain Current	31*	38*	A
I_D @ T_C = 100°C	Continuous Drain Current	20*	24*	A
I_{DM}	Pulsed Drain Current	60	70	A
V_{GS}	Gate – Source Voltage	±20*		V
P_D @ T_C = 25°C	Max. Power Dissipation	150* (See Fig. 11)		W
P_D @ T_C = 100°C	Max. Power Dissipation	60* (See Fig. 11)		W
	Linear Derating Factor	1.2* (See Fig. 11)		W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH 60 | 70		A
T_J T_{stg}	Operating and Storage Temperature Range	-55* to 150*		°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)		°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6763	60	–	–	V	V_{GS} = 0
		2N6764	100	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6763	–	–	2.48*	V	V_{GS} = 10V I_D = 31A
		2N6764	–	–	2.09*	V	V_{GS} = 10V, I_D = 38A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6763	–	0.06	0.08*	Ω	V_{GS} = 10V, I_D = 20A
		2N6764	–	0.045	0.055*	Ω	V_{GS} = 10V, I_D = 24A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6763	–	–	0.136*	Ω	V_{GS} = 10V, I_D = 20A, T_C = 125°C
		2N6764	–	–	0.094*	Ω	V_{GS} = 10V, I_D = 24A, T_C = 125°C
g_{fs}	Forward Transconductance ①	ALL	9.0*	12.5	27*	S (℧)	V_{DS} = 15V, I_D = 24A
C_{iss}	Input Capacitance	ALL	1000*	2000	3000*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	500*	1000	1500*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	150*	350	500*	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	35*	ns	V_{DD} ≅ 24V, I_D = 24A, Z_o = 4.7Ω
t_r	Rise Time	ALL	–	–	100*	ns	(See Figs. 13 and 14)
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	125*	ns	(MOSFET switching times are essentially
t_f	Fall Time	ALL	–	–	100*	ns	independent of operating temperature.)

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	0.83*	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6763	–	–	31*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		2N6764	–	–	38*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6763	–	–	60	A	
		2N6764	–	–	70		
V_{SD}	Diode Forward Voltage ①	2N6763	0.90*	–	1.8*	V	T_C = 25°C, I_S = 31A, V_{GS} = 0
		2N6764	0.95*	–	1.9*	V	T_C = 25°C, I_S = 38A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	500	–	ns	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	10	–	μC	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

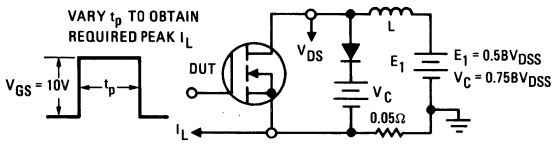


Fig. 1 – Clamped Inductive Test Circuit

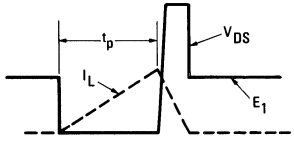


Fig. 2 – Clamped Inductive Waveforms

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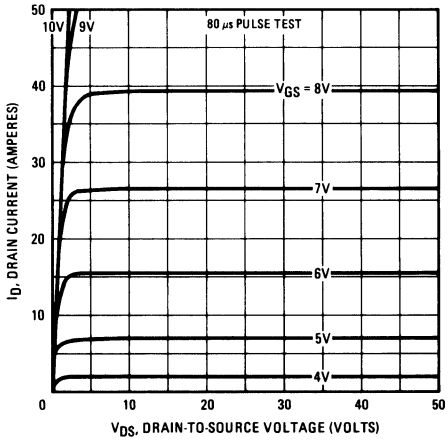


Fig. 3 — Typical Output Characteristics

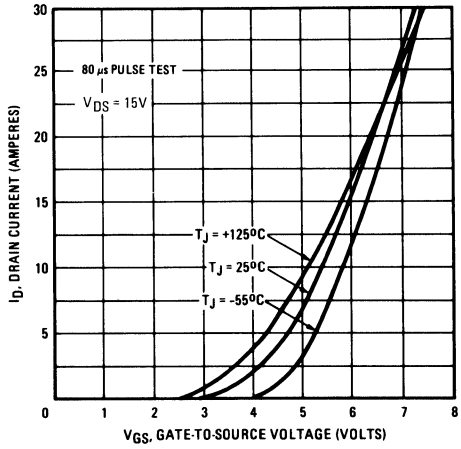


Fig. 4 — Typical Transfer Characteristics

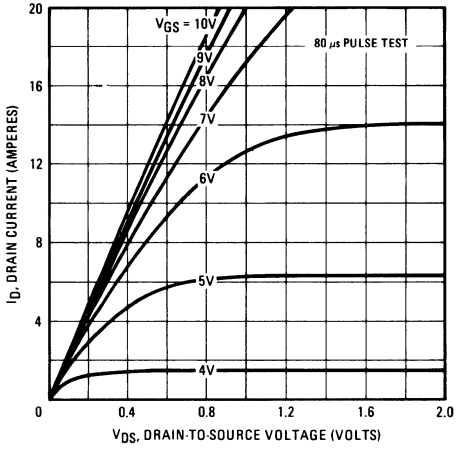


Fig. 5— Typical Saturation Characteristics (2N6763)

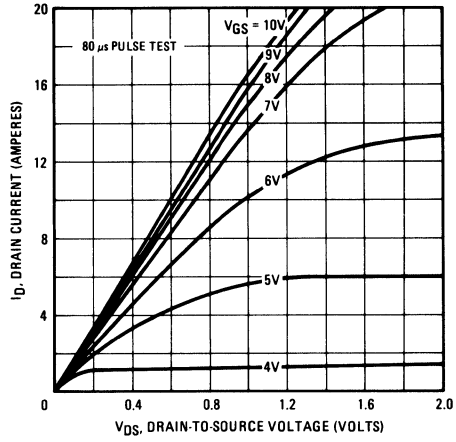


Fig. 6— Typical Saturation Characteristics (2N6764)

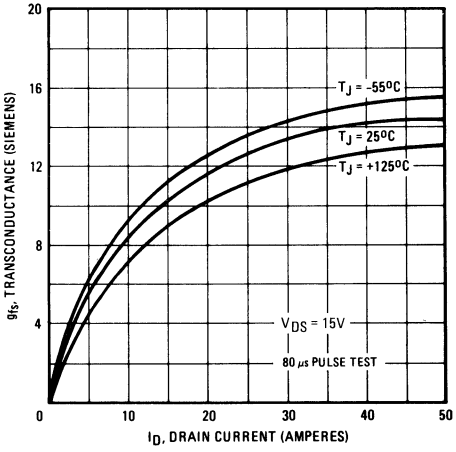


Fig. 7 — Typical Transconductance Vs. Drain Current

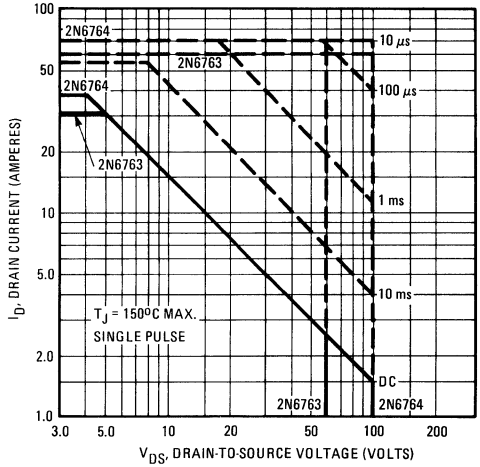


Fig. 8 — Maximum Safe Operating Area

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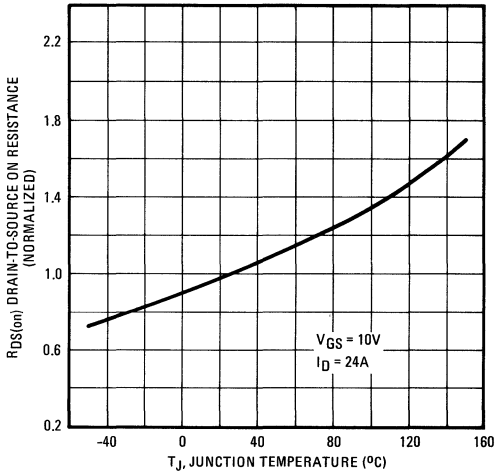


Fig. 9 — Normalized Typical On-Resistance Vs. Temperature

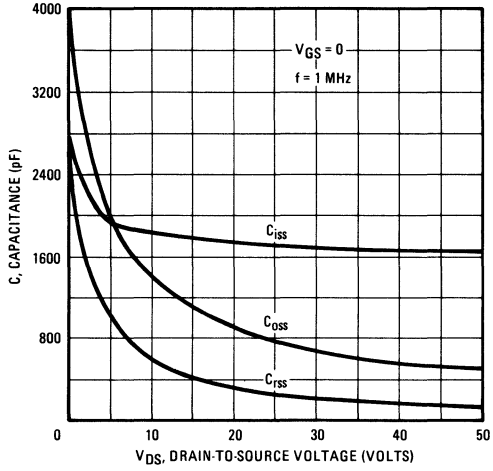


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

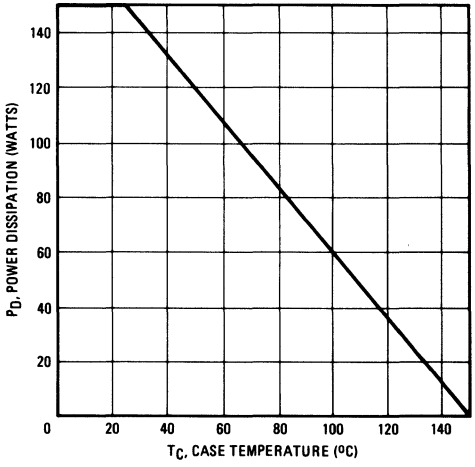


Fig. 11 — Power Vs. Temperature Derating Curve

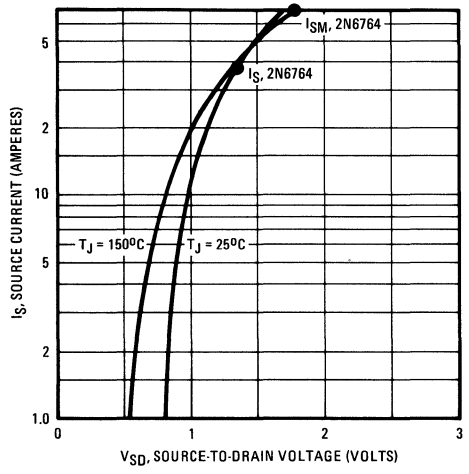


Fig. 12 — Typical Body-Drain Diode Forward Voltage

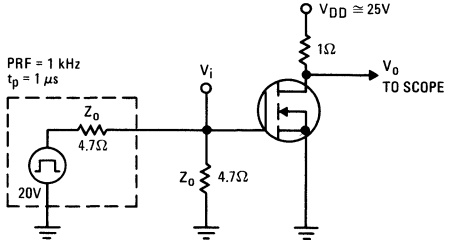


Fig. 13 — Switching Time Test Circuit

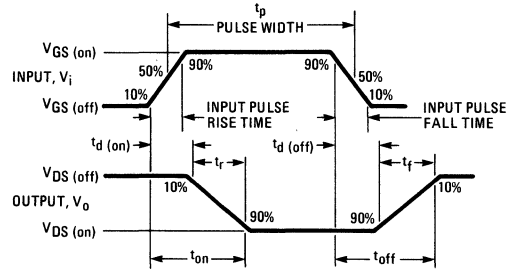


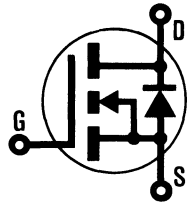
Fig. 14 — Switching Time Waveforms

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS 2N6765 2N6766

JEDEC REGISTERED N-CHANNEL POWER MOSFETs



2N6766 AVAILABLE AS JAN, JANTX AND JANTXV QUALIFIED PER MIL-S-19500/543A

200 Volt, 0.085 Ohm HEXFET

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

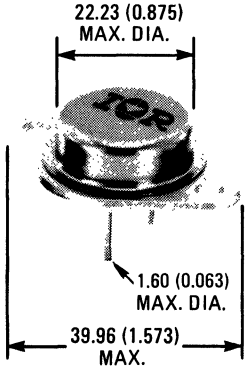
Features:

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

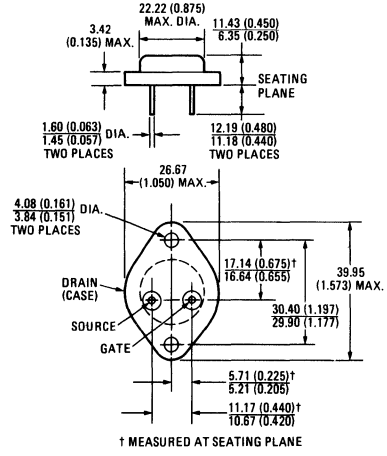
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
2N6765	150V	0.120Ω	25A
2N6766	200V	0.085Ω	30A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



† MEASURED AT SEATING PLANE

Conforms to JEDEC Outline TO-204AE (Modified TO-3)
Dimensions in Millimeters and (Inches)

Downloaded from Arrow.com.

Absolute Maximum Ratings

Parameter		2N6765	2N6766	Units
V_{DS}	Drain – Source Voltage	150*	200*	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 1 MΩ)	150*	200*	V
I_D @ T_C = 25°C	Continuous Drain Current	25*	30*	A
I_D @ T_C = 100°C	Continuous Drain Current	16*	19*	A
I_{DM}	Pulsed Drain Current	50	60	A
V_{GS}	Gate – Source Voltage	±20*		V
P_D @ T_C = 25°C	Max. Power Dissipation	150* (See Fig. 11)		W
P_D @ T_C = 100°C	Max. Power Dissipation	60* (See Fig. 11)		W
	Linear Derating Factor	1.2* (See Fig. 11)		W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH 50 | 60		A
T_J T_{stg}	Operating and Storage Temperature Range	-55* to 150*		°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)		°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6765	150	–	–	V	V_{GS} = 0
		2N6766	200	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6765	–	–	3.0*	V	V_{GS} = 10V, I_D = 25A
		2N6766	–	–	2.7*	V	V_{GS} = 10V, I_D = 30A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6765	–	0.09	0.12*	Ω	V_{GS} = 10V, I_D = 16A
		2N6766	–	0.07	0.085*	Ω	V_{GS} = 10V, I_D = 19A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6765	–	–	0.216*	Ω	V_{GS} = 10V, I_D = 16A, T_C = 125°C
		2N6766	–	–	0.153*	Ω	V_{GS} = 10V, I_D = 19A, T_C = 125°C
g_{fs}	Forward Transconductance ①	ALL	9.0*	15.5	27*	S (℧)	V_{DS} = 15V, I_D = 19A
C_{iss}	Input Capacitance	ALL	1000*	2000	3000*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	450*	800	1200*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	150*	300	500*	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	35*	ns	V_{DD} ≅ 95V, I_D = 19A, Z_o = 4.7Ω
t_r	Rise Time	ALL	–	–	100*	ns	(See Figs. 13 and 14)
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	125*	ns	(MOSFET switching times are essentially
t_f	Fall Time	ALL	–	–	100*	ns	independent of operating temperature.)

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	0.83*	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6765	–	–	25*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		2N6766	–	–	30*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6765	–	–	50	A	
		2N6766	–	–	60		
V_{SD}	Diode Forward Voltage ①	2N6765	0.85*	–	1.7*	V	T_C = 25°C, I_S = 25A, V_{GS} = 0
		2N6766	0.9*	–	1.8*	V	T_C = 25°C, I_S = 30A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	500	–	ns	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	10	–	μC	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

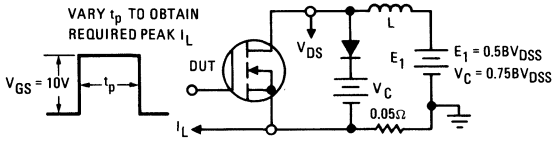


Fig. 1 – Clamped Inductive Test Circuit

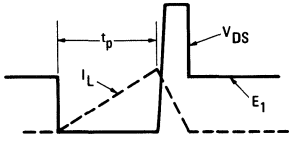


Fig. 2 – Clamped Inductive Waveforms

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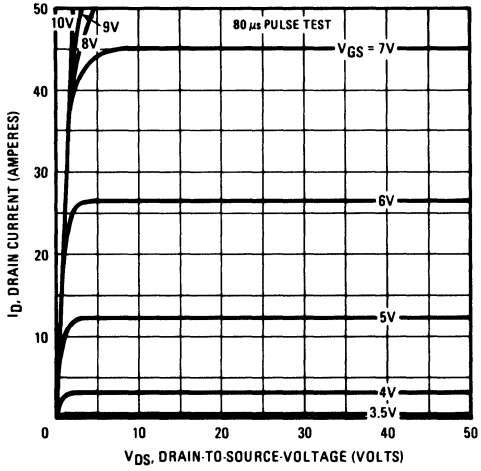


Fig. 3 — Typical Output Characteristics

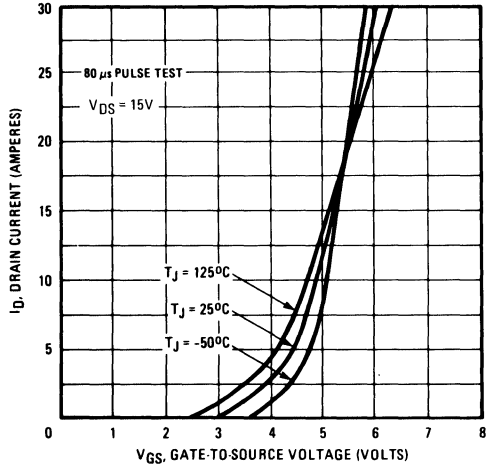


Fig. 4 — Typical Transfer Characteristics

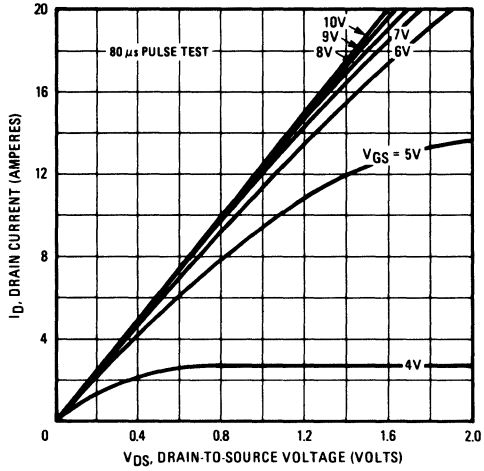


Fig. 5— Typical Saturation Characteristics (2N6765)

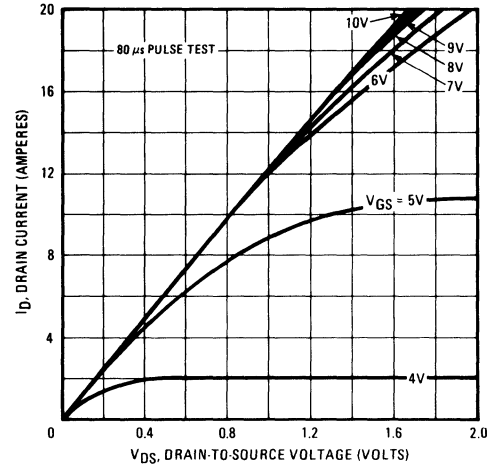


Fig. 6— Typical Saturation Characteristics (2N6766)

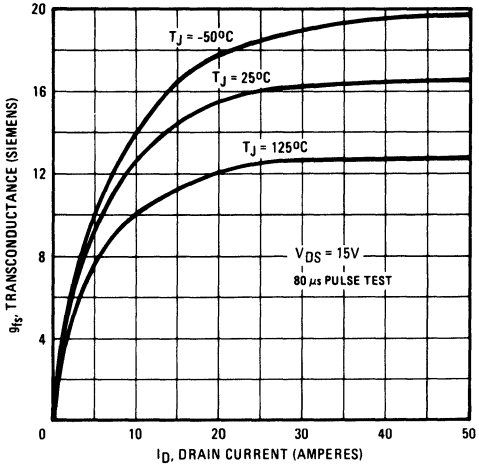


Fig. 7 — Typical Transconductance Vs. Drain Current

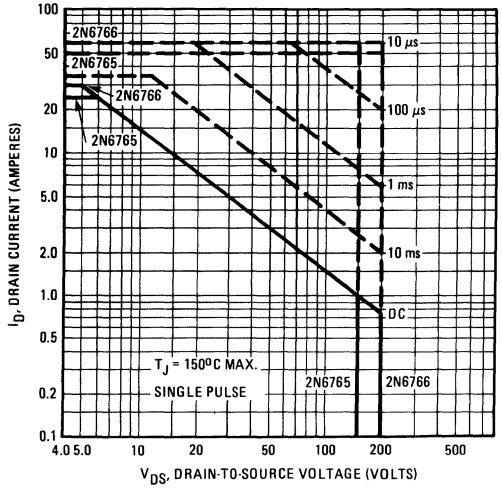


Fig. 8 — Maximum Safe Operating Area

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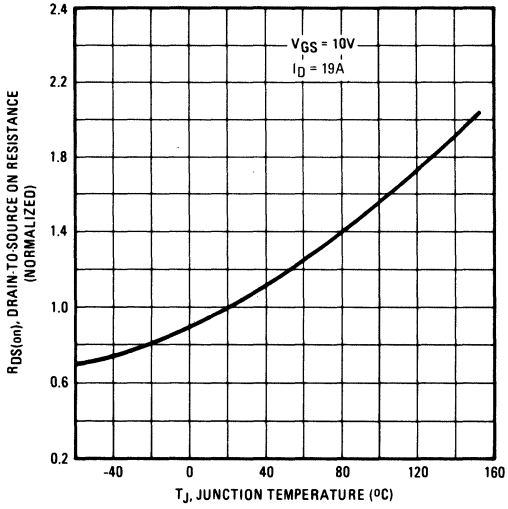


Fig. 9 — Normalized Typical On-Resistance Vs. Temperature

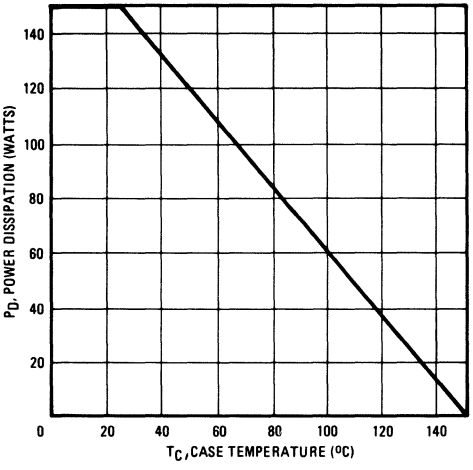


Fig. 11 — Power Vs. Temperature Derating Curve

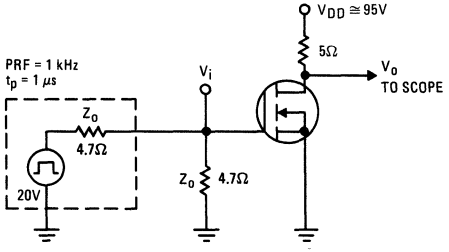


Fig. 13 — Switching Time Test Circuit

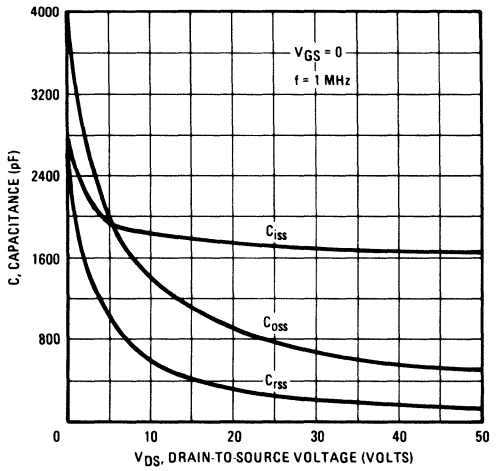


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

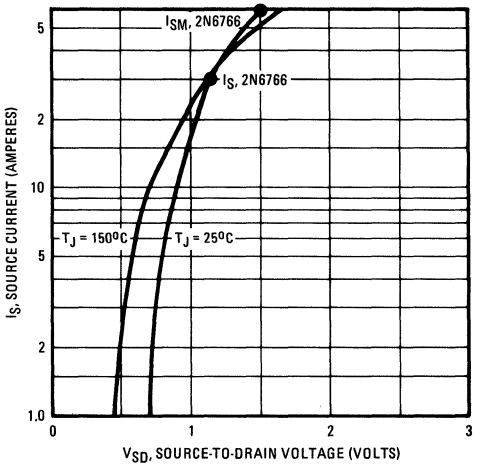


Fig. 12 — Typical Body-Drain Diode Forward Voltage

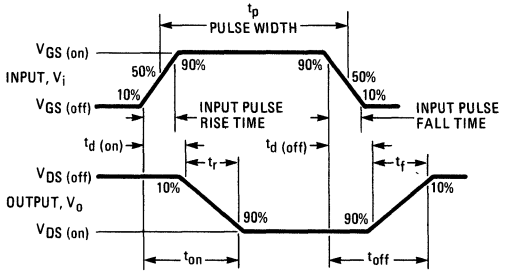


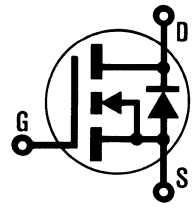
Fig. 14 — Switching Time Waveforms

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS 2N6767 2N6768

JEDEC REGISTERED N-CHANNEL POWER MOSFETs



400 Volt, 0.3 Ohm HEXFET

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

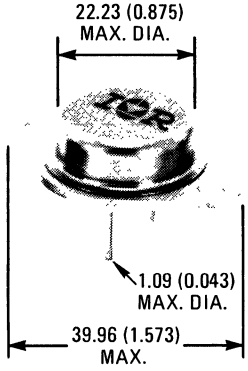
Features:

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

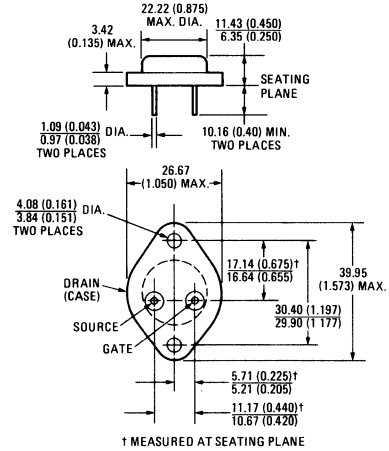
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
2N6767	350V	0.4Ω	12A
2N6768	400V	0.3Ω	14A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



† MEASURED AT SEATING PLANE

Conforms to JEDEC Outline TO-204AA (TO-3)
Dimensions in Millimeters and (Inches)

Downloaded from Arrow.com.

Absolute Maximum Ratings

Parameter		2N6767	2N6768	Units
V_{DS}	Drain – Source Voltage	350*	400*	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 1 MΩ)	350*	400*	V
I_D @ T_C = 25°C	Continuous Drain Current	12*	14*	A
I_D @ T_C = 100°C	Continuous Drain Current	7.75*	9.0*	A
I_{DM}	Pulsed Drain Current	20	25	A
V_{GS}	Gate – Source Voltage	±20*		V
P_D @ T_C = 25°C	Max. Power Dissipation	150* (See Fig. 11)		W
P_D @ T_C = 100°C	Max. Power Dissipation	60* (See Fig. 11)		W
	Linear Derating Factor	1.2* (See Fig. 11)		W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH		A
		20	25	
T_J T_{stg}	Operating and Storage Temperature Range	-55* to 150*		°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)		°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6767	350	–	–	V	V_{GS} = 0
		2N6768	400	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6767	–	–	5.4*	V	V_{GS} = 10V, I_D = 12A
		2N6768	–	–	5.6*	V	V_{GS} = 10V, I_D = 14A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6767	–	0.3	0.4*	Ω	V_{GS} = 10V, I_D = 7.75A
		2N6768	–	0.25	0.3*	Ω	V_{GS} = 10V, I_D = 9.0A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6767	–	–	0.88*	Ω	V_{GS} = 10V, I_D = 7.75A, T_C = 125°C
		2N6768	–	–	0.66*	Ω	V_{GS} = 10V, I_D = 9.0A, T_C = 125°C
g_{fs}	Forward Transconductance ①	ALL	8.0*	11.0	24*	S (℧)	V_{DS} = 15V, I_D = 9.0A
C_{iss}	Input Capacitance	ALL	1000*	2000	3000*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	200*	400	600*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	50*	100	200*	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	35*	ns	V_{DD} ≅ 180V, I_D = 9.0A, Z_o = 4.7Ω
t_r	Rise Time	ALL	–	–	65*	ns	(See Figs. 13 and 14)
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	150*	ns	(MOSFET switching times are essentially
t_f	Fall Time	ALL	–	–	75*	ns	independent of operating temperature.)

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	0.83*	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6767	–	–	12*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		2N6768	–	–	14*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6767	–	–	20	A	
		2N6768	–	–	25		
V_{SD}	Diode Forward Voltage ①	2N6767	0.8*	–	1.6*	V	T_C = 25°C, I_S = 12A, V_{GS} = 0
		2N6768	0.85*	–	1.7*	V	T_C = 25°C, I_S = 14A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	1000	–	ns	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	25	–	μC	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

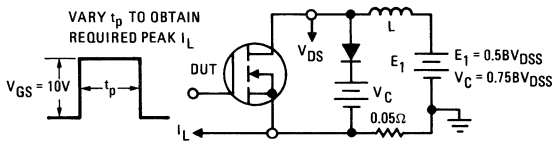


Fig. 1 – Clamped Inductive Test Circuit

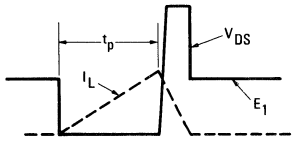


Fig. 2 – Clamped Inductive Waveforms

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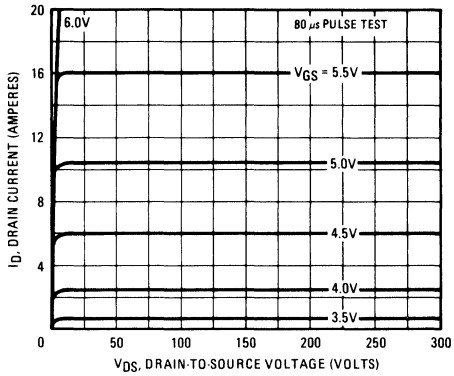


Fig. 3 — Typical Output Characteristics

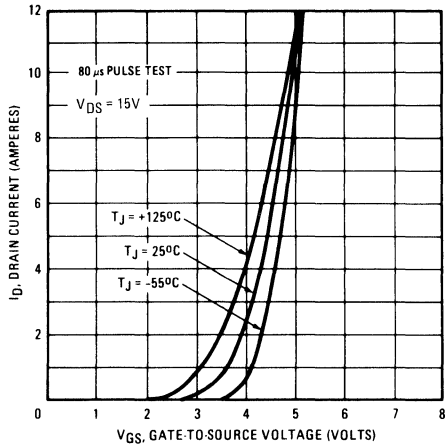


Fig. 4 — Typical Transfer Characteristics

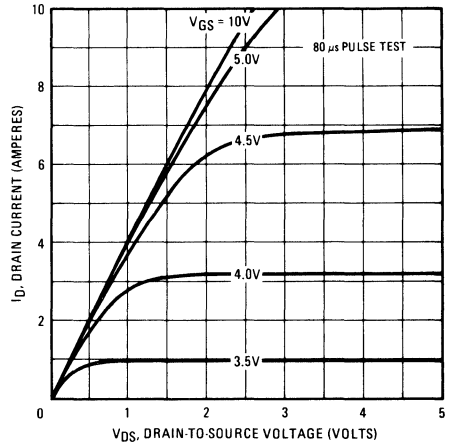


Fig. 5— Typical Saturation Characteristics (2N6767)

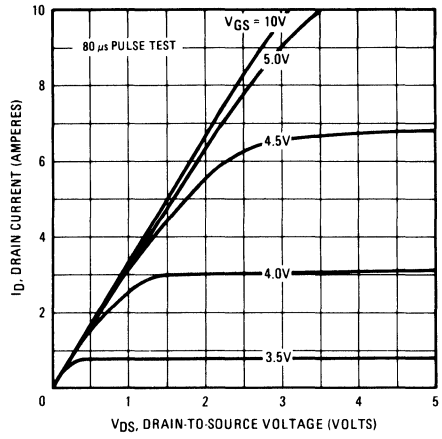


Fig. 6— Typical Saturation Characteristics (2N6768)

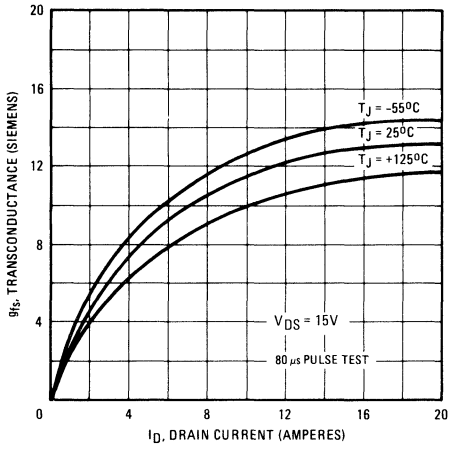


Fig. 7 — Typical Transconductance Vs. Drain Current

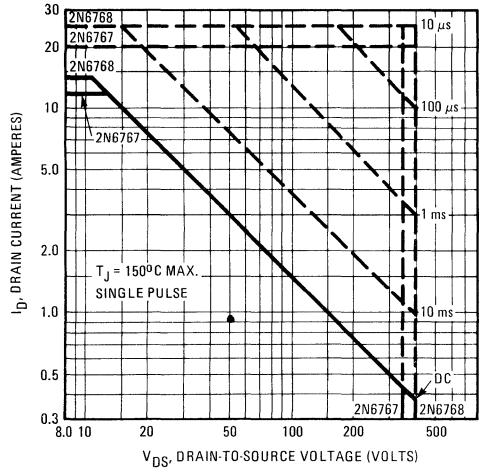


Fig. 8 — Maximum Safe Operating Area

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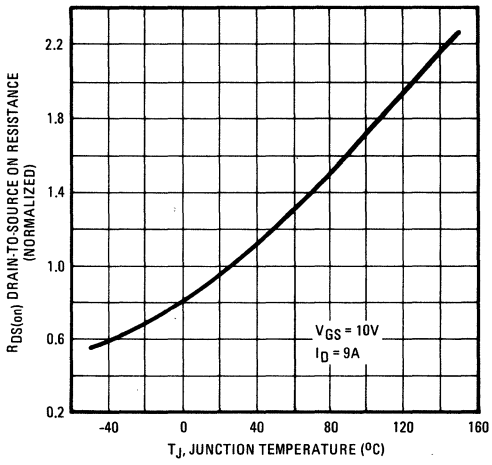


Fig. 9 — Normalized Typical On-Resistance Vs. Temperature

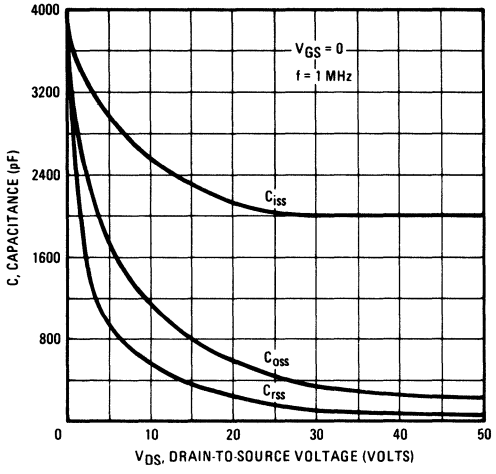


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

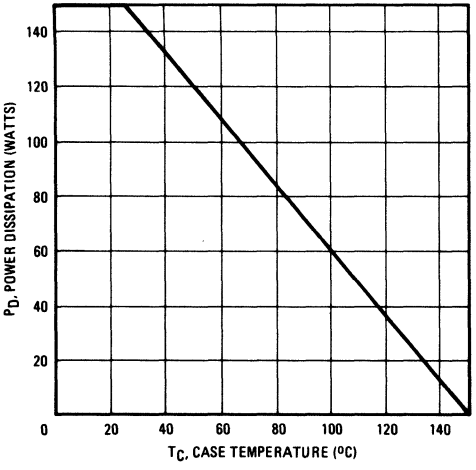


Fig. 11 — Power Vs. Temperature Derating Curve

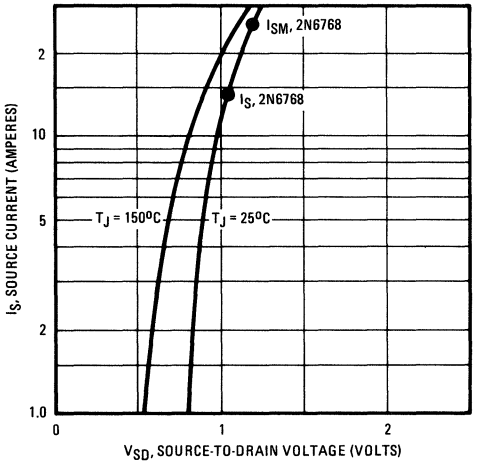


Fig. 12 — Typical Body-Drain Diode Forward Voltage

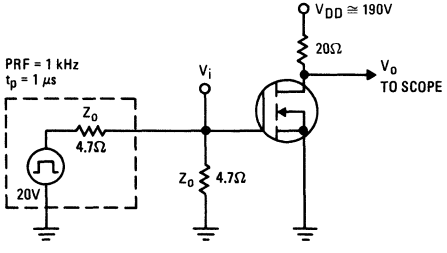


Fig. 13 — Switching Time Test Circuit

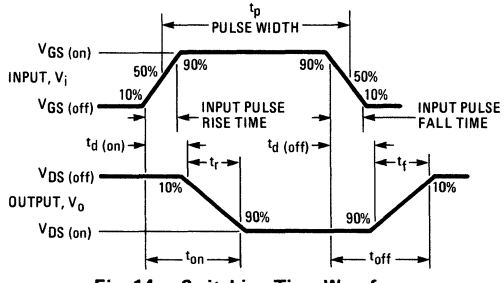


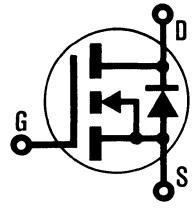
Fig. 14 — Switching Time Waveforms

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HEXFET® TRANSISTORS 2N6769 2N6770

JEDEC REGISTERED N-CHANNEL POWER MOSFETs



500 Volt, 0.4 Ohm HEXFET

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

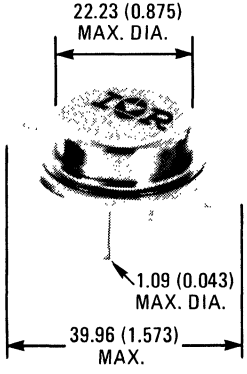
Features:

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

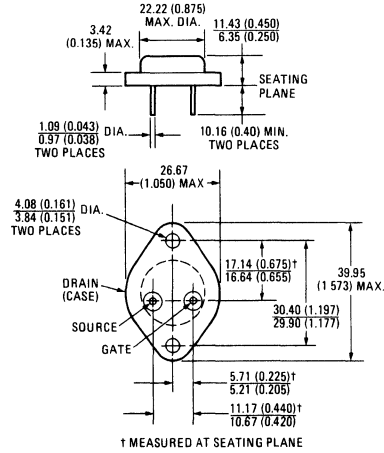
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
2N6769	450V	0.5Ω	11A
2N6770	500V	0.4Ω	12A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



† MEASURED AT SEATING PLANE

Conforms to JEDEC Outline TO-204AA (TO-3)
Dimensions in Millimeters and (Inches)

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Absolute Maximum Ratings

Parameter		2N6769	2N6770	Units
V_{DS}	Drain – Source Voltage	450*	500*	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 1 MΩ)	450*	500*	V
I_D @ T_C = 25°C	Continuous Drain Current	11*	12*	A
I_D @ T_C = 100°C	Continuous Drain Current	7.0*	7.75*	A
I_{DM}	Pulsed Drain Current	20	25	A
V_{GS}	Gate – Source Voltage	±20*		V
P_D @ T_C = 25°C	Max. Power Dissipation	150* (See Fig. 11)		W
P_D @ T_C = 100°C	Max. Power Dissipation	60* (See Fig. 11)		W
	Linear Derating Factor	1.2* (See Fig. 11)		W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH		A
		20	25	
T_J T_{stg}	Operating and Storage Temperature Range	-55* to 150*		°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)		°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6769	450	–	–	V	V_{GS} = 0
		2N6770	500	–	–	V	I_D = 4.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = 0.8 x Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 25°C to 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6769	–	–	6.0*	V	
		2N6770	–	–	6.0*	V	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6769	–	0.4	0.5*	Ω	V_{GS} = 10V, I_D = 7.0A
		2N6770	–	0.3	0.4*	Ω	V_{GS} = 10V, I_D = 7.75A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6769	–	–	1.1*	Ω	V_{GS} = 10V, I_D = 7.0A, T_C = 125°C
		2N6770	–	–	0.88*	Ω	V_{GS} = 10V, I_D = 7.75A, T_C = 125°C
g_{fs}	Forward Transconductance ①	ALL	8.0*	12.0	24*	S (℧)	V_{DS} = 15V, I_D = 7.75A
C_{iss}	Input Capacitance	ALL	1000*	2000	3000*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	200*	400	600*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	50*	100	200*	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	–	–	35*	ns	$V_{DD} \cong$ 210V, I_D = 7.75A, Z_o = 4.7Ω
t_r	Rise Time	ALL	–	–	50*	ns	(See Figs. 13 and 14)
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	–	–	150*	ns	(MOSFET switching times are essentially
t_f	Fall Time	ALL	–	–	70*	ns	independent of operating temperature.)

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	0.83*	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6769	–	–	11*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		2N6770	–	–	12*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6769	–	–	20	A	
		2N6770	–	–	25		
V_{SD}	Diode Forward Voltage ①	2N6769	0.75*	–	1.5*	V	T_C = 25°C, I_S = 11A, V_{GS} = 0
		2N6770	0.80*	–	1.6*	V	T_C = 25°C, I_S = 12A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	400	–	ns	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	10	–	μC	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

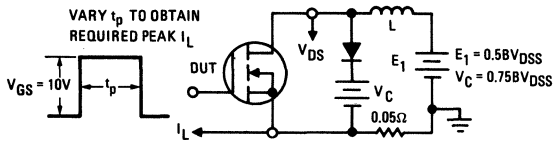


Fig. 1 – Clamped Inductive Test Circuit

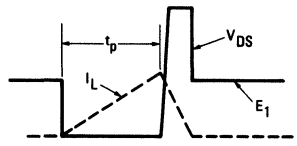


Fig. 2 – Clamped Inductive Waveforms

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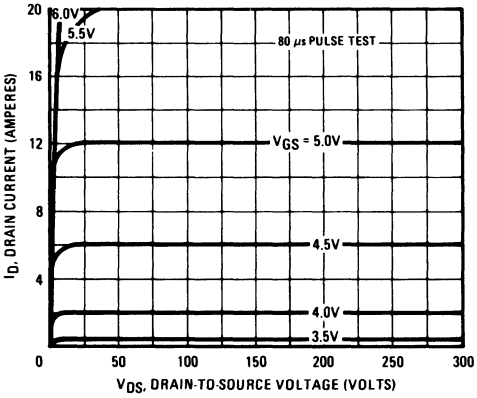


Fig. 3 — Typical Output Characteristics

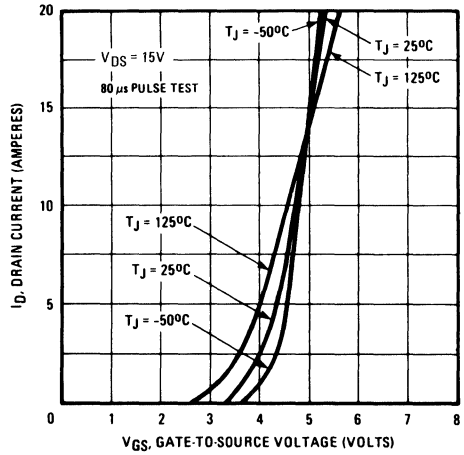


Fig. 4 — Typical Transfer Characteristics

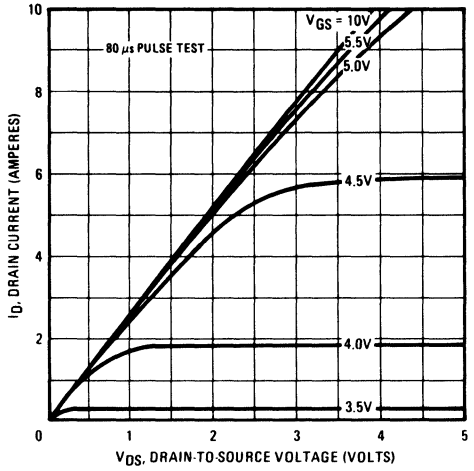


Fig. 5— Typical Saturation Characteristics (2N6769)

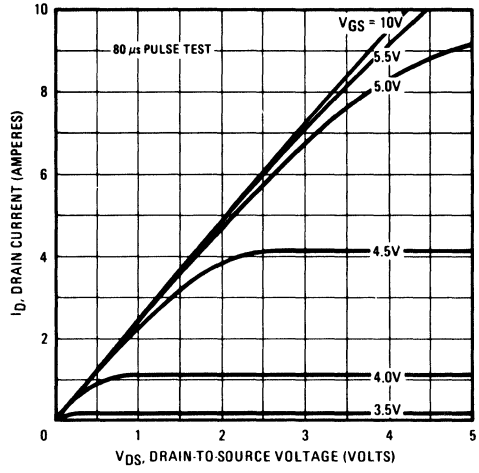


Fig. 6— Typical Saturation Characteristics (2N6770)

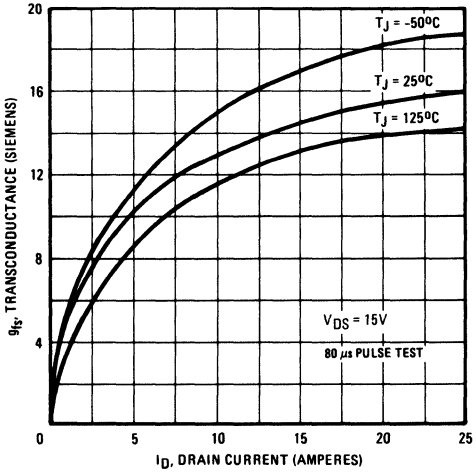


Fig. 7 — Typical Transconductance Vs. Drain Current

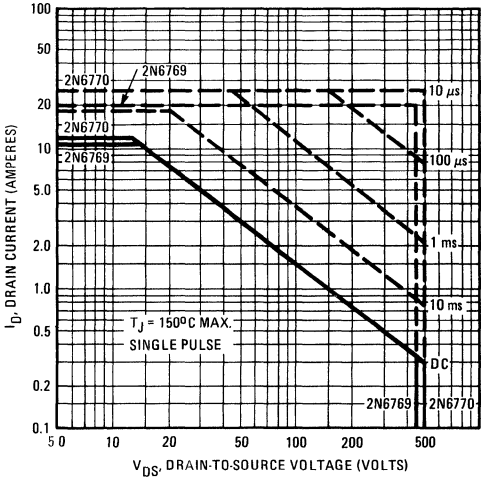


Fig. 8 — Maximum Safe Operating Area

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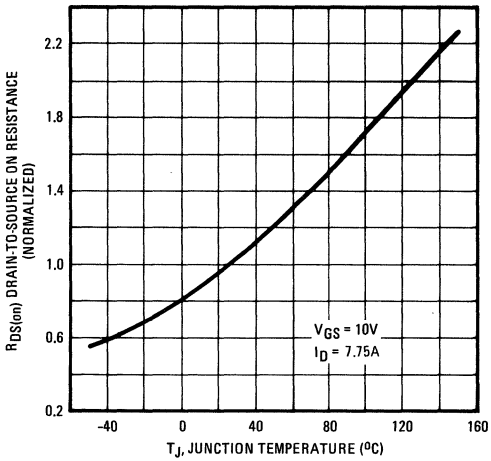


Fig. 9 — Normalized Typical On-Resistance Vs. Temperature

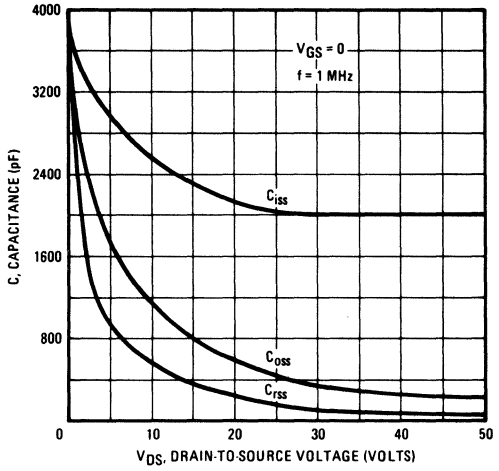


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

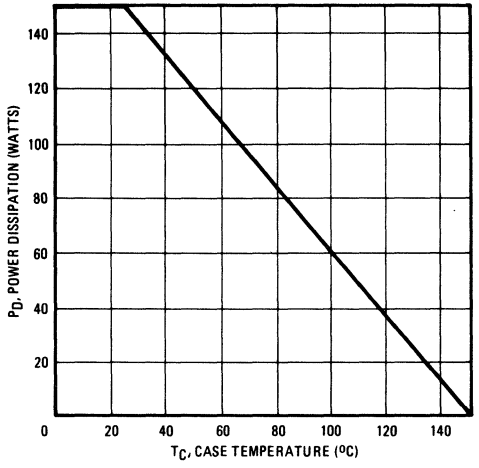


Fig. 11 — Power Vs. Temperature Derating Curve

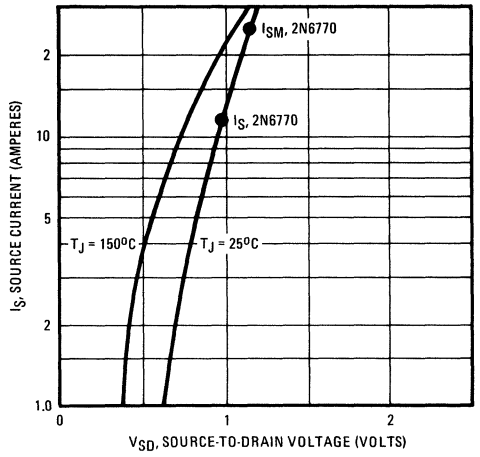


Fig. 12 — Typical Body-Drain Diode Forward Voltage

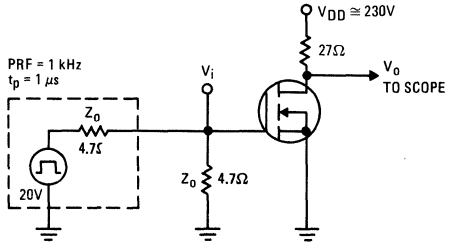


Fig. 13 — Switching Time Test Circuit

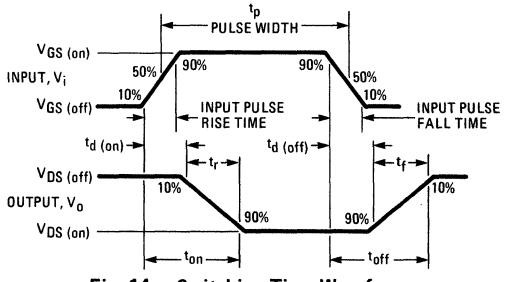


Fig. 14 — Switching Time Waveforms

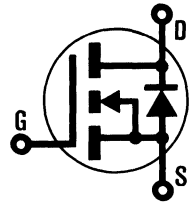
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HEXFET® TRANSISTORS IRFD1Z0

N-CHANNEL HEXDIP™

1-WATT RATED POWER MOSFETs
IN A 4-PIN, DUAL IN-LINE PACKAGE



IRFD1Z1
IRFD1Z2
IRFD1Z3

100 Volt, 2.4 Ohm, 1-Watt HEXDIP

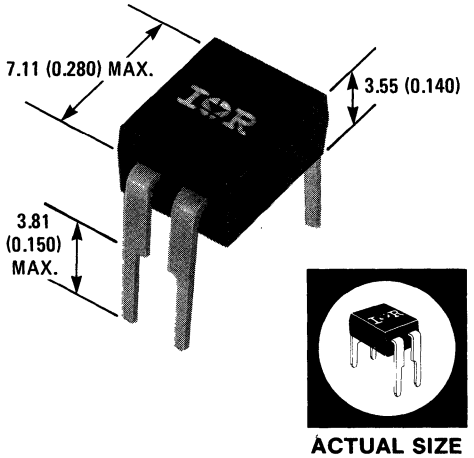
HEXFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. Efficient geometry and unique processing of the HEXFET design achieve a very low on-state resistance combined with high transconductance and great device ruggedness. HEXFETs feature all of the established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

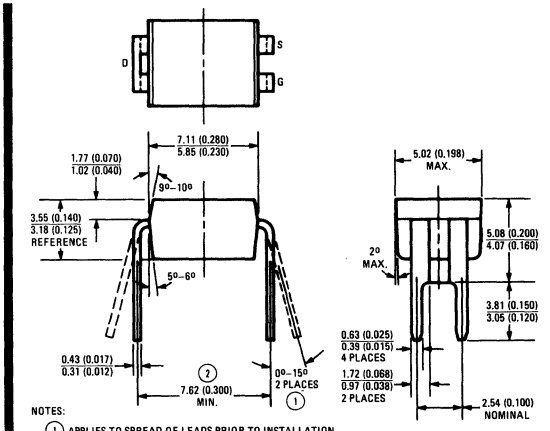
The HEXDIP 4-pin, Dual In-Line Package brings the advantages of HEXFETs to high volume applications where automatic PC Board insertion is desirable, such as circuit boards for computers, printers, telecommunications equipment and consumer products. Their compatibility with automatic insertion equipment, low-profile and end-stackable features, represent the state-of-the-art in power device packaging.

- For Automatic Insertion
- Compact, End-Stackable
- Fast Switching
- Low Drive Current
- Easily Paralleled
- No Second Breakdown
- Excellent Temperature Stability

Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFD1Z0	100V	2.4Ω	0.5A
IRFD1Z1	60V	2.4Ω	0.5A
IRFD1Z2	100V	3.2Ω	0.4A
IRFD1Z3	60V	3.2Ω	0.4A





Case Style HD-1 (Similar to JEDEC Outline MO-001)
Dimensions in Millimeters and (Inches)

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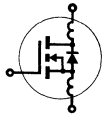
Absolute Maximum Ratings

Parameter		IRFD1Z0	IRFD1Z1	IRFD1Z2	IRFD1Z3	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	0.5	0.5	0.4	0.4	A
I_{DM}	Pulsed Drain Current	2.0	2.0	1.5	1.5	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	1.0 (See Fig. 13)				W
	Linear Derating Factor	0.008 (See Fig. 13)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 14 and 15) L = 100μH				A
		2.0	2.0	1.5	1.5	
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFD1Z0 IRFD1Z2	100	—	—	V	V_{GS} = 0V
		IRFD1Z1 IRFD1Z3	60	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	−500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFD1Z0 IRFD1Z1	0.5	—	—	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRFD1Z2 IRFD1Z3	0.4	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFD1Z0 IRFD1Z1	—	2.2	2.4	Ω	V_{GS} = 10V, I_D = 0.25A
		IRFD1Z2 IRFD1Z3	—	2.8	3.2	Ω	
g_{fs}	Forward Transconductance ②	ALL	—	0.35	—	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 0.25A
C_{iss}	Input Capacitance	ALL	—	50	70	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 9
C_{oss}	Output Capacitance	ALL	—	20	30	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	5.0	10	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	10	20	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 0.25A, Z_0 = 50Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	15	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	15	25	ns	
t_f	Fall Time	ALL	—	10	20	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	2.0	3.0	nC	V_{GS} = 10V, I_D = 1.2A, V_{DS} = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	1.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	1.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	4.0	—	nH	Measured from the drain lead, 2.0mm (0.08 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	6.0	—	nH	Measured from the source lead, 2.0mm (0.08 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJA}	Junction-to-Ambient	ALL	—	—	120	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFD1Z0 IRFD1Z1	—	—	0.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRFD1Z2 IRFD1Z3	—	—	0.4	A	
I_{SM}	Pulse Source Current (Body Diode)	IRFD1Z0 IRFD1Z1	—	—	2.0	A	
		IRFD1Z2 IRFD1Z3	—	—	1.5	A	
V_{SD}	Diode Forward Voltage ②	IRFD1Z0 IRFD1Z1	—	—	1.4	V	T_C = 25°C, I_S = 0.5A, V_{GS} = 0V
		IRFD1Z2 IRFD1Z3	—	—	1.3	V	T_C = 25°C, I_S = 0.4A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	100	—	ns	T_J = 150°C, I_F = 0.5A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	0.2	—	μC	T_J = 150°C, I_F = 0.5A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

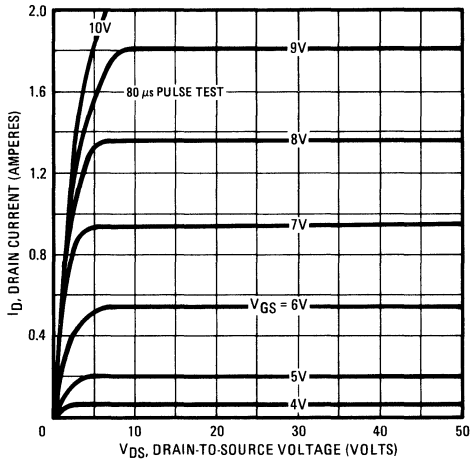


Fig. 1 — Typical Output Characteristics

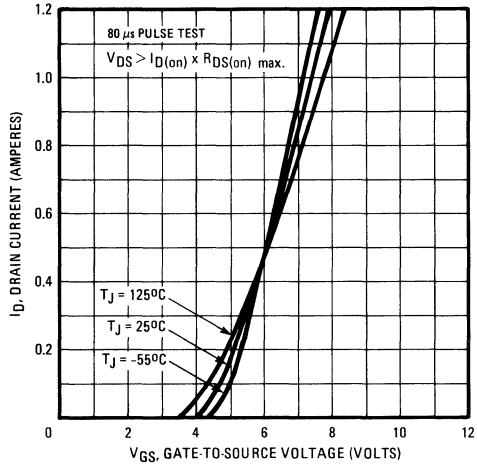


Fig. 2 — Typical Transfer Characteristics

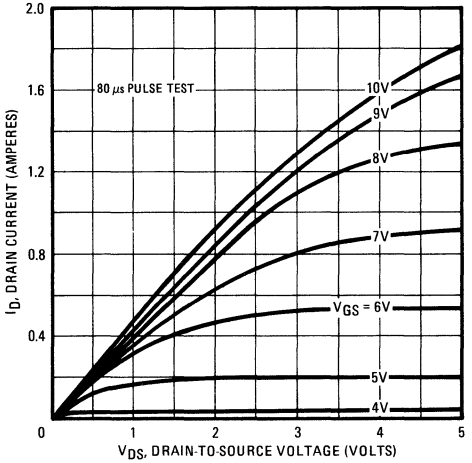


Fig. 3 — Typical Saturation Characteristics

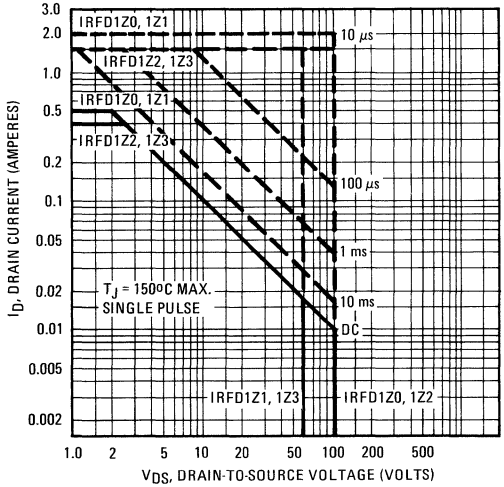


Fig. 4 — Maximum Safe Operating Area

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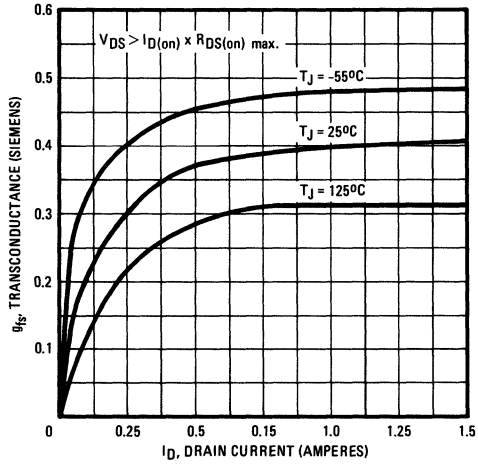


Fig. 5 — Typical Transconductance Vs. Drain Current

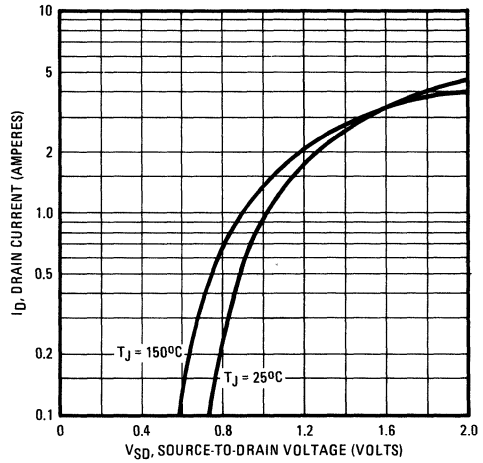


Fig. 6 — Typical Source-Drain Diode Forward Voltage

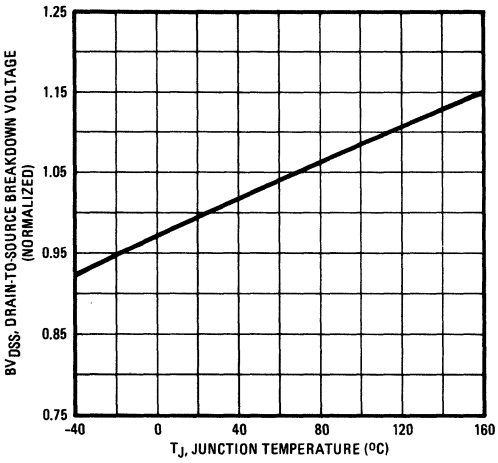


Fig. 7 — Breakdown Voltage Vs. Temperature

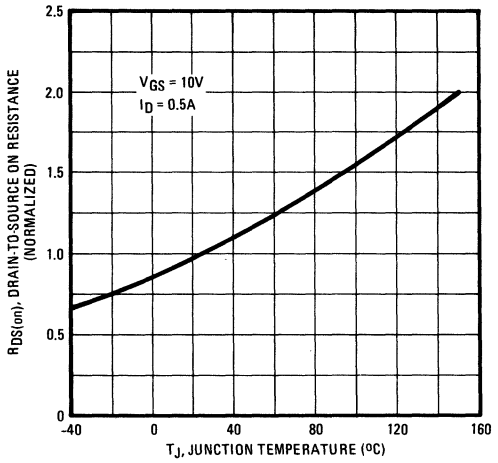


Fig. 8 — Normalized On-Resistance Vs. Temperature

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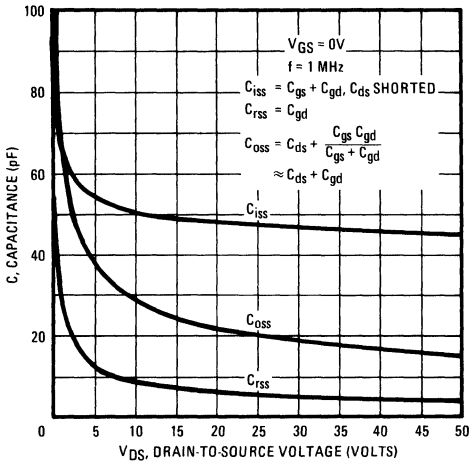


Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

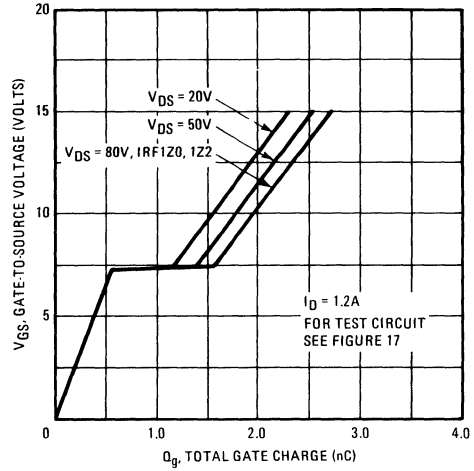


Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

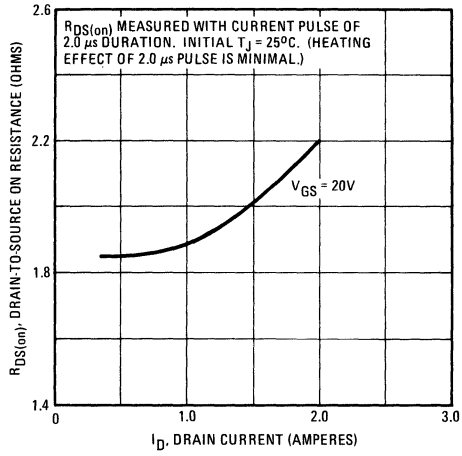


Fig. 11 — Typical On-Resistance Vs. Drain Current

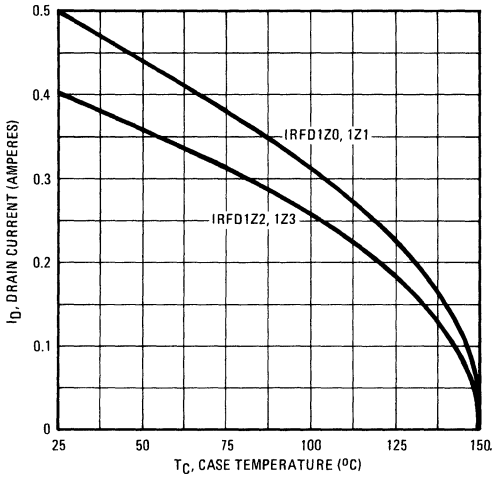


Fig. 12 — Maximum Drain Current Vs. Case Temperature

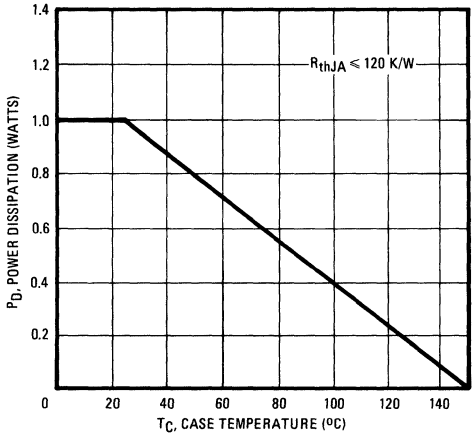


Fig. 13 — Power Vs. Temperature Derating Curve

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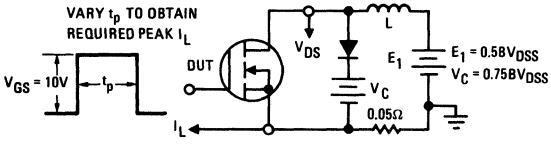


Fig. 14 — Clamped Inductive Test Circuit

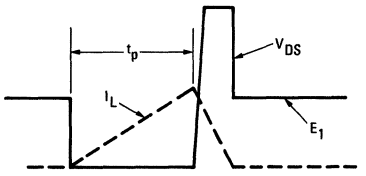


Fig. 15 — Clamped Inductive Waveforms

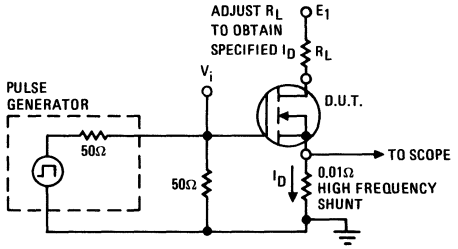


Fig. 16 — Switching Time Test Circuit

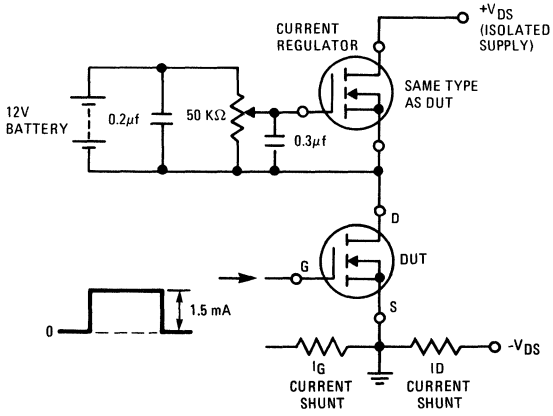


Fig. 17 — Gate Charge Test Circuit

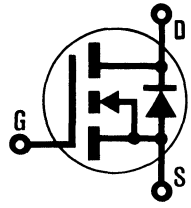
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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS IRFD110

N-CHANNEL HEXDIP™

1-WATT RATED POWER MOSFETs
IN A 4-PIN, DUAL-IN-LINE PACKAGE



IRFD111
IRFD112
IRFD113

100 VOLT, 0.6 Ohm, 1-Watt HEXDIP

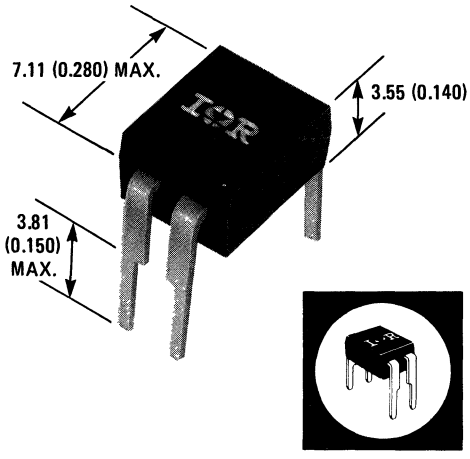
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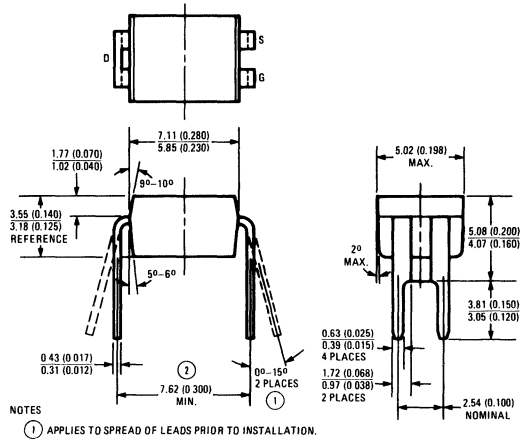
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- For Automatic Insertion
- Compact, End Stackable
- Fast Switching
- Low Drive Current
- Easily Paralleled
- No Second Breakdown
- Excellent Temperature Stability

Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFD110	100V	0.6Ω	1.0A
IRFD111	60V	0.6Ω	1.0A
IRFD112	100V	0.8Ω	0.8A
IRFD113	60V	0.8Ω	0.8A





Case Style HD-1 (Similar to JEDEC Outline MO-001)
Nominal Dimensions in Millimeters and (Inches)

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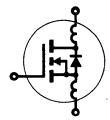
Absolute Maximum Ratings

Parameter		IRFD110	IRFD111	IRFD112	IRFD113	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	1.0	1.0	0.8	0.8	A
I_{DM}	Pulsed Drain Current	4.0	4.0	3.0	3.0	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	1.0 (See Fig. 13)				W
	Linear Derating Factor	0.008 (See Fig. 13)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 14 and 15) L = 100μH				A
		4.0	4.0	3.0	3.0	
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFD110 IRFD112	100	—	—	V	V_{GS} = 0V
		IRFD111 IRFD113	60	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFD110 IRFD111	1.0	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		IRFD112 IRFD113	0.8	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFD110 IRFD111	—	0.5	0.6	Ω	V_{GS} = 10V, I_D = 0.8A
		IRFD112 IRFD113	—	0.6	0.8	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.8	1.2	—	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 0.8A
C_{iss}	Input Capacitance	ALL	—	135	200	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 9
C_{oss}	Output Capacitance	ALL	—	80	100	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	20	25	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	10	20	ns	$V_{DD} \simeq 0.5\ BV_{DSS}$, I_D = 0.8A, Z_o = 50Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	15	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	15	25	ns	
t_f	Fall Time	ALL	—	10	20	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	5.0	7.0	nC	V_{GS} = 10V, I_D = 4.0A, V_{DS} = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	2.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	7.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	4.0	—	nH	Measured from the drain lead, 2.0mm (0.08 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	6.0	—	nH	Measured from the source lead, 2.0mm (0.08 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJA}	Junction-to-Ambient	ALL	—	—	120	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFD110 IRFD111	–	–	1.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFD112 IRFD113	–	–	0.8	A	
I_{SM}	Pulse Source Current (Body Diode)	IRFD110 IRFD111	–	–	4.0	A	
		IRFD112 IRFD113	–	–	3.0	A	
V_{SD}	Diode Forward Voltage ②	IRFD110 IRFD111	–	–	2.5	V	T_C = 25°C, I_S = 1.0A, V_{GS} = 0V
		IRFD112 IRFD113	–	–	2.0	V	T_C = 25°C, I_S = 0.8A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	100	–	ns	T_J = 150°C, I_F = 1.0A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	0.2	–	μC	T_J = 150°C, I_F = 1.0A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

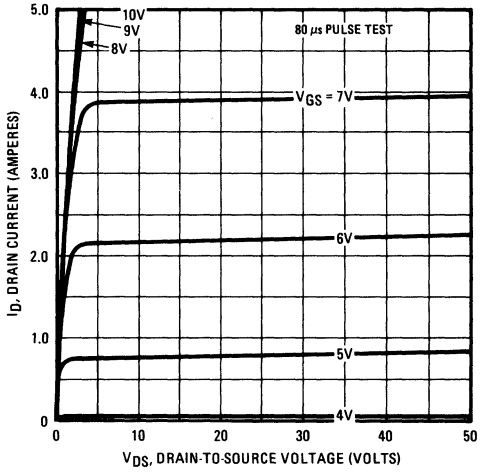


Fig. 1 – Typical Output Characteristics

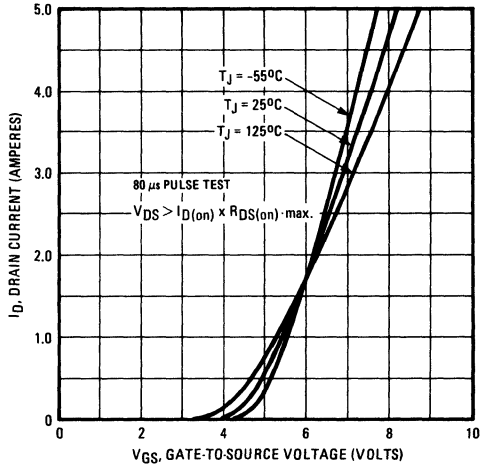


Fig. 2 – Typical Transfer Characteristics

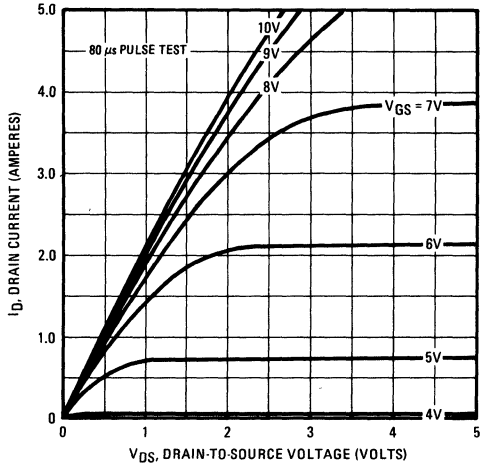


Fig. 3 – Typical Saturation Characteristics

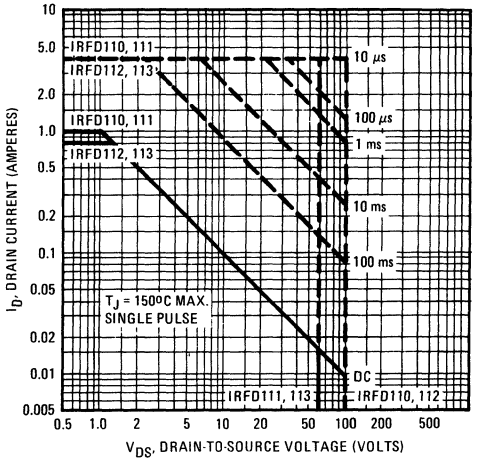


Fig. 4 – Maximum Safe Operating Area

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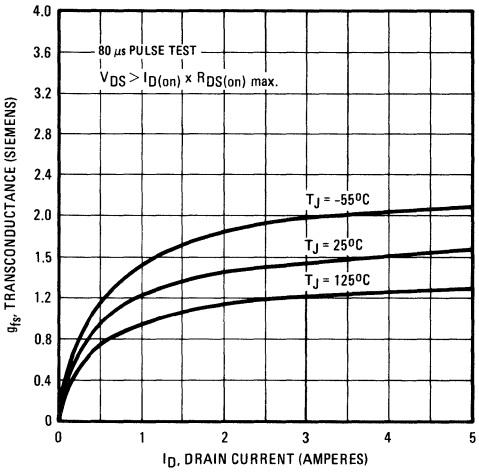


Fig. 5 — Typical Transconductance Vs. Drain Current

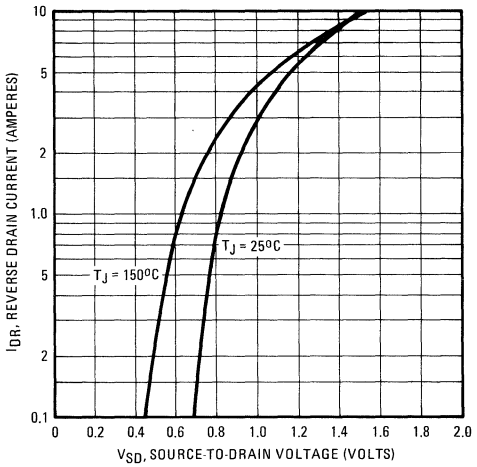


Fig. 6 — Typical Source-Drain Diode Forward Voltage

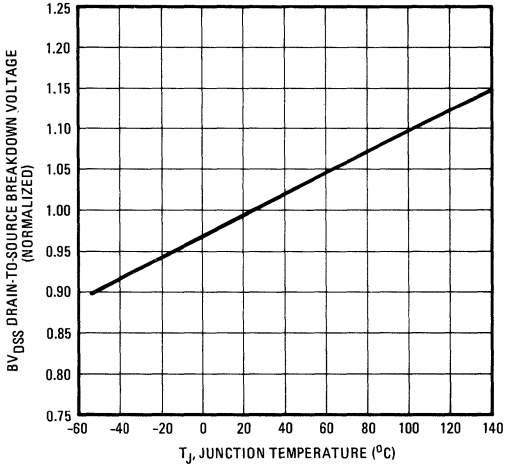


Fig. 7 — Breakdown Voltage Vs. Temperature

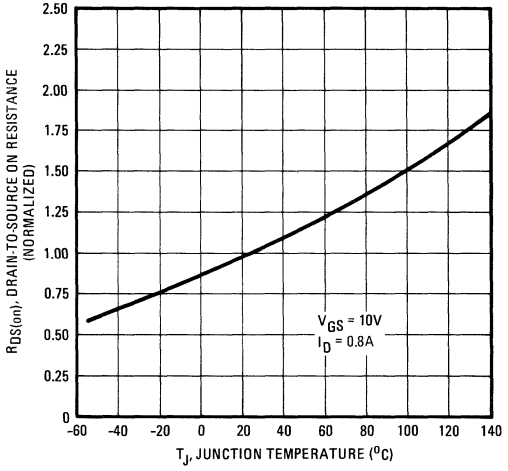


Fig. 8 — Normalized On-Resistance Vs. Temperature

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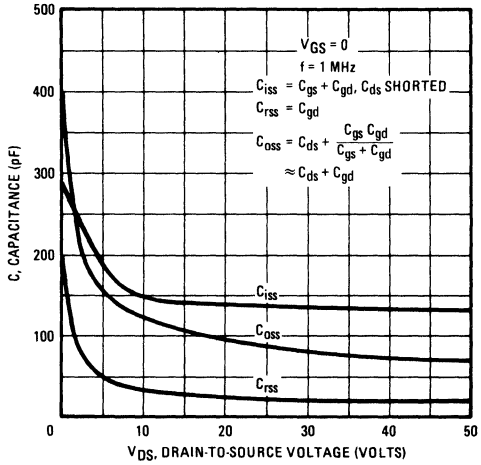


Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

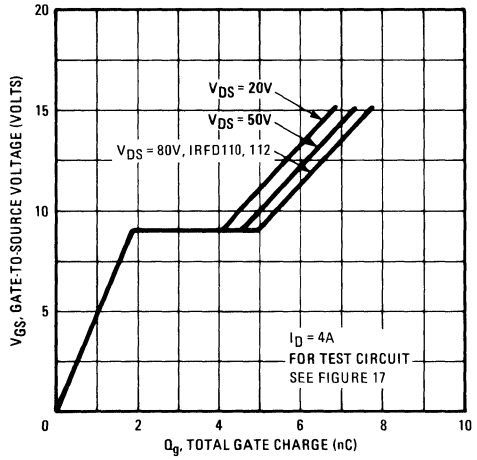


Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

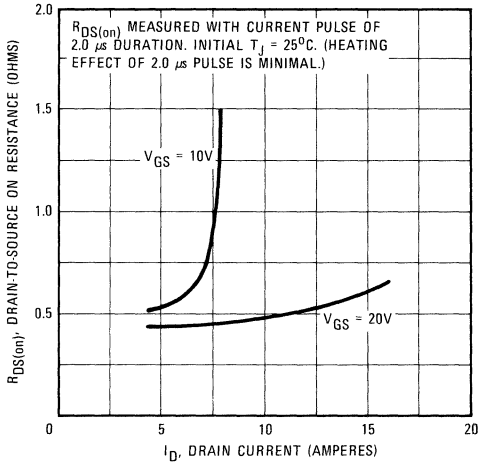


Fig. 11 — Typical On-Resistance Vs. Drain Current

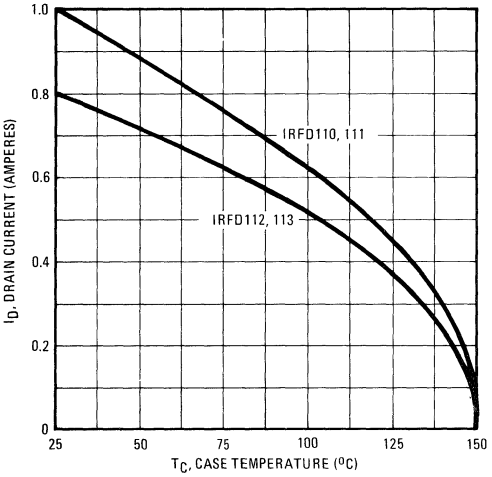


Fig. 12 — Maximum Drain Current Vs. Case Temperature

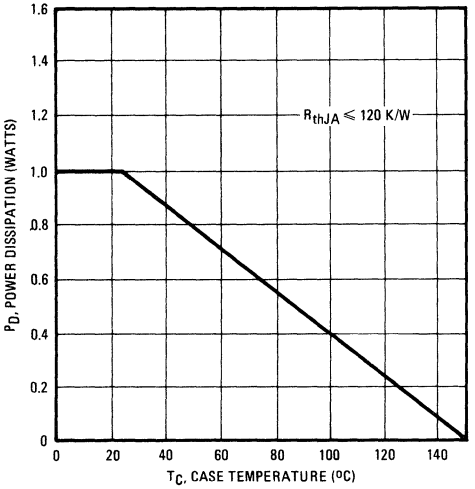


Fig. 13 — Power Vs. Temperature Derating Curve

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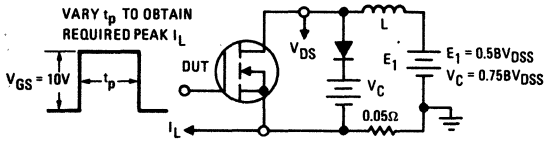


Fig. 14 — Clamped Inductive Test Circuit

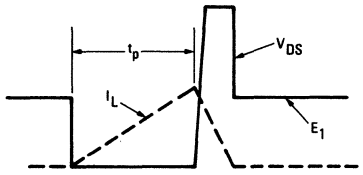


Fig. 15 — Clamped Inductive Waveforms

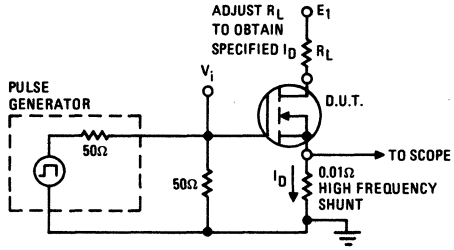


Fig. 16 — Switching Time Test Circuit

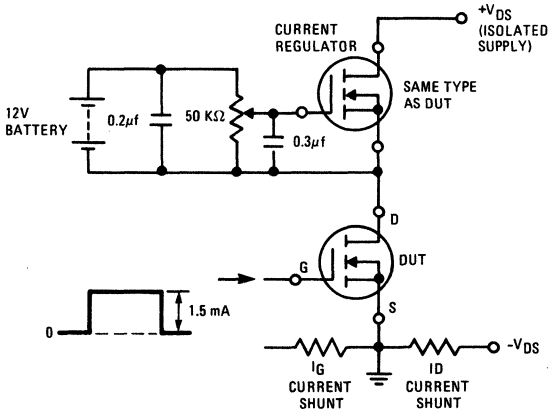


Fig. 17 — Gate Charge Test Circuit

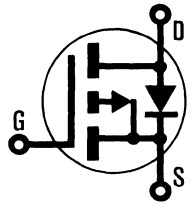
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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS

P-CHANNEL HEXDIP™

1-WATT RATED POWER MOSFETs
IN A 4-PIN, DUAL IN-LINE PACKAGE



IRFD9120
IRFD9121
IRFD9122
IRFD9123

−100 VOLT, 0.6 Ohm, 1-Watt HEXDIP

HEXFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. Efficient geometry and unique processing of the HEXFET design achieve a very low on-state resistance combined with high transconductance and great device ruggedness. HEXFETs feature all of the established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

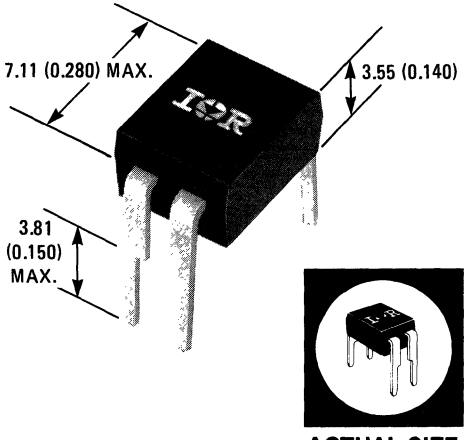
The P-Channel HEXDIPs are designed for applications which require the convenience of reverse polarity operation or the simplification of complementary circuit configurations. For example, the P-Channel IRFD9121 type is essentially the electrical complement to the N-Channel IRFD111 type HEXDIP.

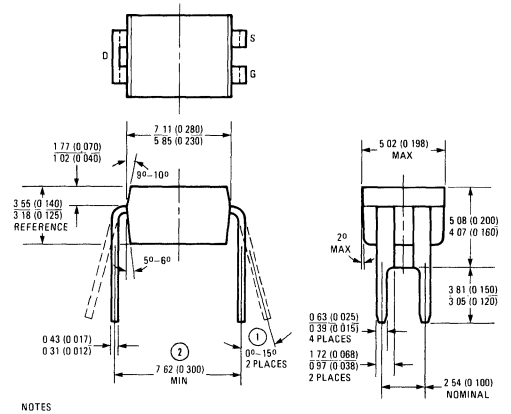
The HEXDIP 4-pin Dual In-Line Package brings the advantages of HEXFETs to high volume applications where automatic PC Board insertion is desirable, such as circuit boards for computers, printers, telecommunications equipment and consumer products. Their compatibility with automatic insertion equipment, low-profile and end-stackable features represent the state-of-the-art in power device packaging.

- P-Channel Versatility
- For Automatic Insertion
- Compact, End Stackable
- Fast Switching
- Low Drive Current
- Easily Paralleled
- No Second Breakdown
- Excellent Temperature Stability

Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFD9120	−100V	0.6Ω	−1.0A
IRFD9121	−60V	0.6Ω	−1.0A
IRFD9122	−100V	0.8Ω	−0.8A
IRFD9123	−60V	0.8Ω	−0.8A





NOTES
(1) APPLIES TO SPREAD OF LEADS PRIOR TO INSTALLATION
(2) APPLIES TO INSTALLED LEAD CENTERS

Case Style HD-1 (Similar to JEDEC Outline MO-001)
Nominal Dimensions in Millimeters and (Inches)

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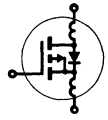
Absolute Maximum Ratings

Parameter		IRFD9120	IRFD9121	IRFD9122	IRFD9123	Units
V_{DS}	Drain - Source Voltage ①	-100	-60	-100	-60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	-100	-60	-100	-60	V
I_D @ T_C = 25°C	Continuous Drain Current	-1.0	-1.0	-0.8	-0.8	A
I_{DM}	Pulsed Drain Current	-4.0	-4.0	-3.0	-3.0	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	1.0 (See Fig. 13)				W
	Linear Derating Factor	0.008 (See Fig. 13)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 14 and 15) L = 100μH				A
		-4.0	-4.0	-3.0	-3.0	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFD9120 IRFD9122	-100	–	–	V	V_{GS} = 0V
		IRFD9121 IRFD9123	-60	–	–	V	I_D = -250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	-2.0	–	-4.0	V	V_{DS} = V_{GS}, I_D = -250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	-500	nA	V_{GS} = -20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	500	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	-250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	-1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFD9120 IRFD9121	-1.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = -10V
		IRFD9122 IRFD9123	-0.8	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFD9120 IRFD9121	–	0.5	0.6	Ω	V_{GS} = -10V, I_D = -0.8A
		IRFD9122 IRFD9123	–	0.6	0.8	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.8	1.2	–	S(℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = -0.8A
C_{iss}	Input Capacitance	ALL	–	300	450	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1.0 MHz See Fig. 9
C_{oss}	Output Capacitance	ALL	–	200	350	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	50	100	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	25	50	ns	V_{DD} = 0.5 BV_{DSS}, I_D = -0.8A, Z_o = 50Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	50	100	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	50	100	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	16	20	nC	V_{GS} = -10V, I_D = -4.0A, V_{DS} = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	9.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	7.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	4.0	–	nH	Measured from the drain lead, 2.0mm (0.08 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	6.0	–	nH	Measured from the source lead, 2.0mm (0.08 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJA}	Junction-to-Ambient	ALL	–	–	120	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFD9120 IRFD9121	—	—	-1.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFD9122 IRFD9123	—	—	-0.8	A	
I_{SM}	Pulse Source Current (Body Diode)	IRFD9120 IRFD9121	—	—	-4.0	A	
		IRFD9122 IRFD9123	—	—	-3.0	A	
V_{SD}	Diode Forward Voltage ②	IRFD9120 IRFD9121	—	—	-6.3	V	T_C = 25°C, I_S = -1.0A, V_{GS} = 0V
		IRFD9122 IRFD9123	—	—	6.0	V	T_C = 25°C, I_S = -0.8A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	150	—	ns	T_J = 150°C, I_F = -4.0A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	0.9	—	μC	T_J = 150°C, I_F = -4.0A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

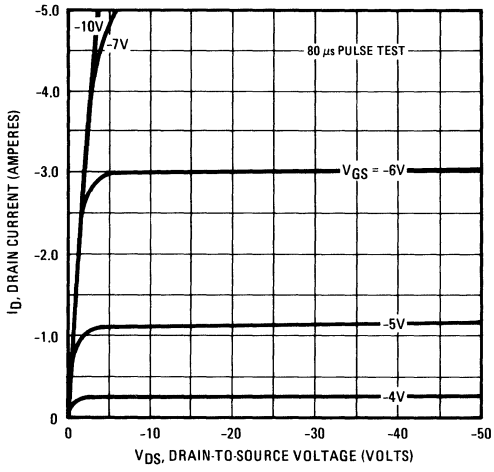


Fig. 1 — Typical Output Characteristics

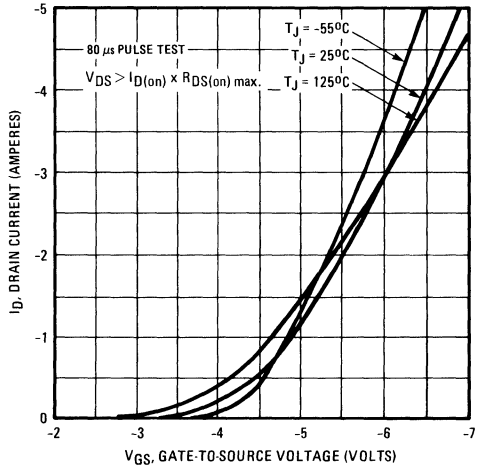


Fig. 2 — Typical Transfer Characteristics

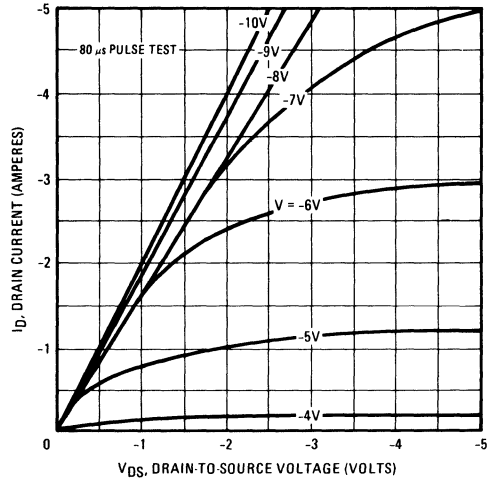


Fig. 3 — Typical Saturation Characteristics

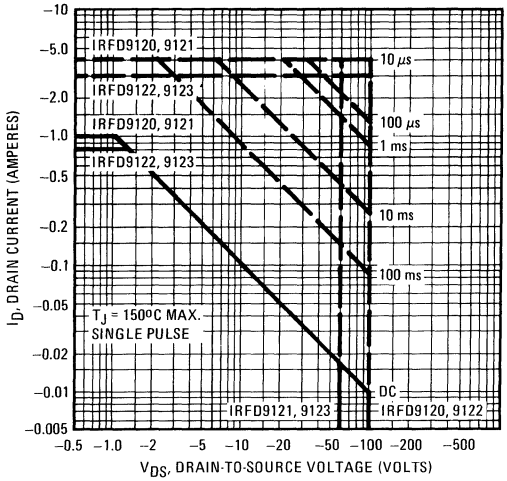


Fig. 4 — Maximum Safe Operating Area

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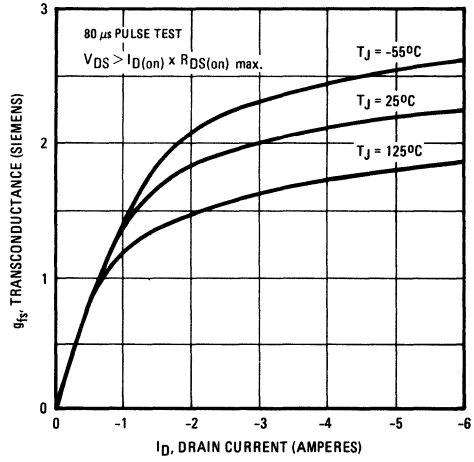


Fig. 5 — Typical Transconductance Vs. Drain Current

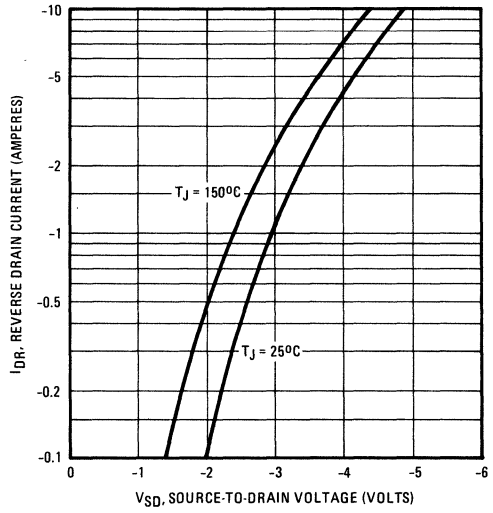


Fig. 6 — Typical Source-Drain Diode Forward Voltage

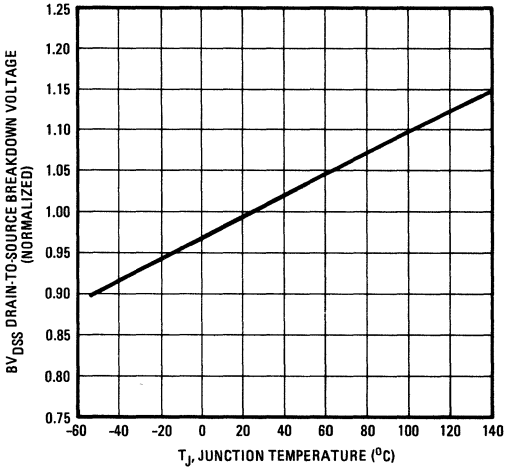


Fig. 7 — Breakdown Voltage Vs. Temperature

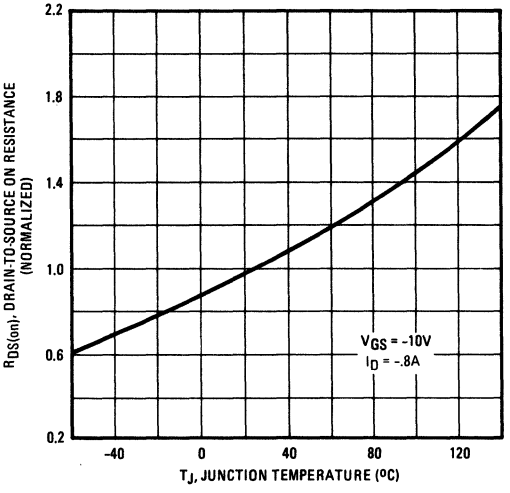


Fig. 8 — Normalized On-Resistance Vs. Temperature

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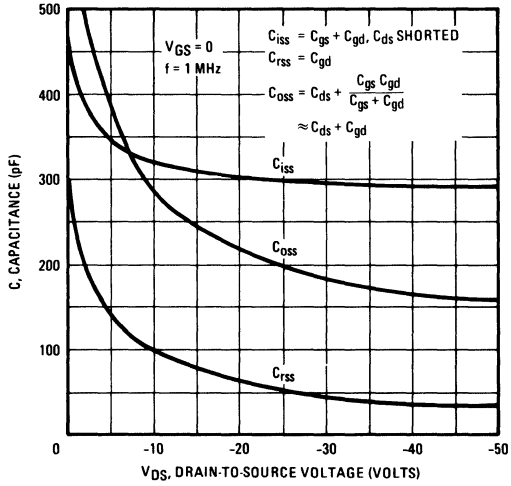


Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

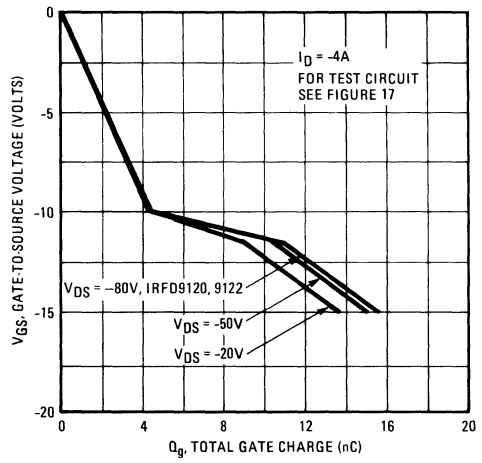


Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

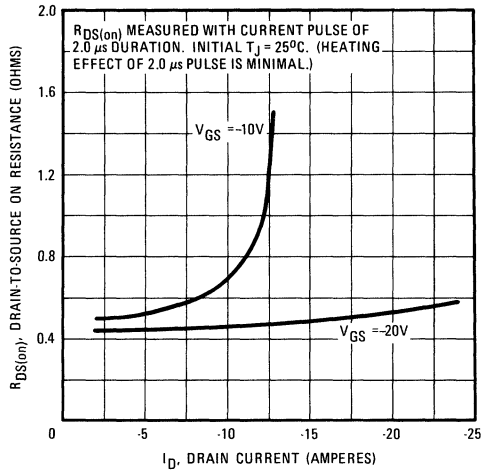


Fig. 11 — Typical On-Resistance Vs. Drain Current

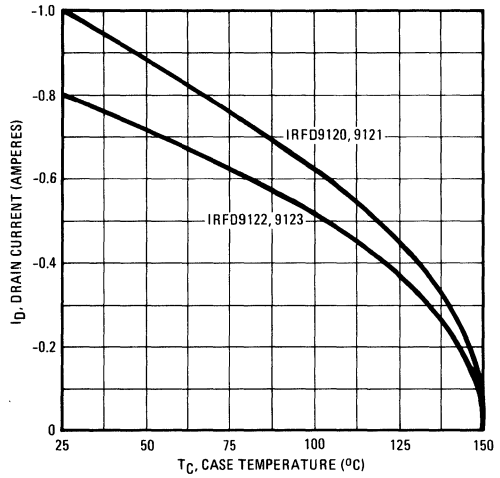


Fig. 12 — Maximum Drain Current Vs. Case Temperature

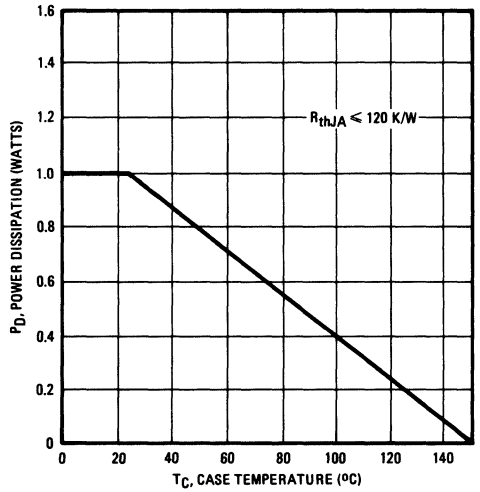


Fig. 13 — Power Vs. Temperature Derating Curve

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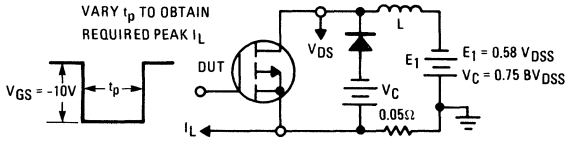


Fig. 14 — Clamped Inductive Test Circuit

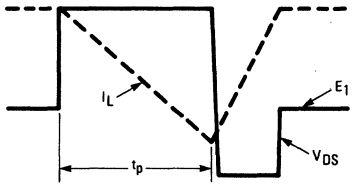


Fig. 15 — Clamped Inductive Waveforms

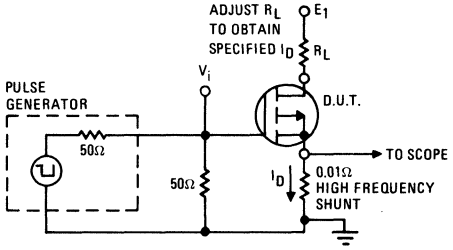


Fig. 16 — Switching Time Test Circuit

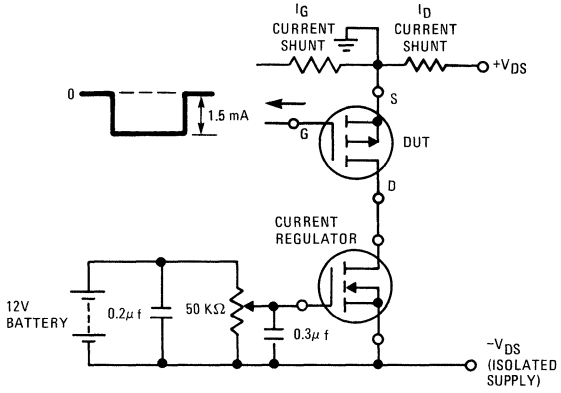


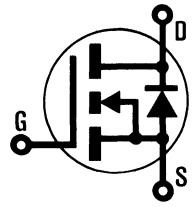
Fig. 17 — Gate Charge Test Circuit

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS IRFF110

N-CHANNEL POWER MOSFETs TO-39 PACKAGE



IRFF111
IRFF112
IRFF113

100 Volt, 0.60 Ohm HEXFET®

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

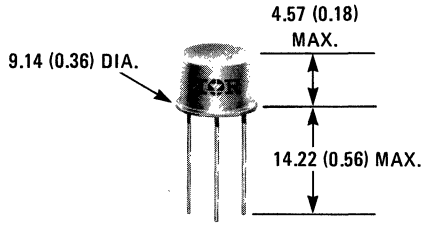
Features:

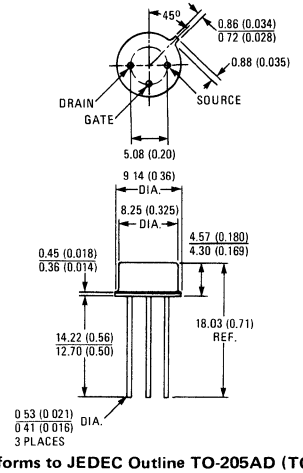
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFF110	100V	0.6Ω	3.5A
IRFF111	60V	0.6Ω	3.5A
IRFF112	100V	0.8Ω	3.0A
IRFF113	60V	0.8Ω	3.0A

CASE STYLE AND DIMENSIONS





Conforms to JEDEC Outline TO-205AD (TO-39)
All Dimensions in Millimeters and (Inches)

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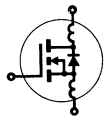
Absolute Maximum Ratings

Parameter		IRFF110	IRFF111	IRFF112	IRFF113	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	3.5	3.5	3.0	3.0	A
I_{DM}	Pulsed Drain Current ③	14	14	12	12	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	15 (See Fig. 14)				W
	Linear Derating Factor	0.12 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		14	14	12	12	
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFF110 IRFF112	100	–	–	V	V_{GS} = 0V
		IRFF111 IRFF113	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFF110 IRFF111	3.5	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		IRFF112 IRFF113	3.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFF110 IRFF111	–	0.5	0.6	Ω	V_{GS} = 10V, I_D = 1.5A
		IRFF112 IRFF113	–	0.6	0.8	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	1.5	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 1.5A
C_{iss}	Input Capacitance	ALL	–	135	200	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	80	100	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	20	25	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	10	20	ns	$V_{DD} \simeq 0.5\ BV_{DSS}$, I_D = 1.5A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	15	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	15	25	ns	
t_f	Fall Time	ALL	–	10	20	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	5.0	7.5	nC	V_{GS} = 10V, I_D = 8.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	2.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	3.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 5 mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	ALL	–	15	–	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	8.33	K/W	
R_{thJA}	Junction-to-Ambient	ALL	–	–	175	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFF110 IRFF111	—	—	3.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFF112 IRFF113	—	—	3.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF110 IRFF111	—	—	14	A	
		IRFF112 IRFF113	—	—	12	A	
V_{SD}	Diode Forward Voltage ②	IRFF110 IRFF111	—	—	2.5	V	T_C = 25°C, I_S = 3.5A, V_{GS} = 0V
		IRFF112 IRFF113	—	—	2.0	V	T_C = 25°C, I_S = 3.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	200	—	ns	T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	1.0	—	μC	T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

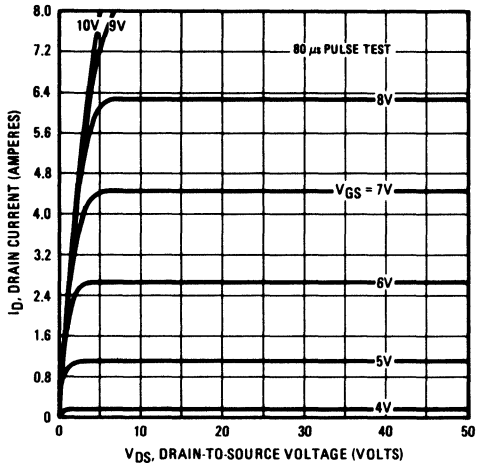


Fig. 1 — Typical Output Characteristics

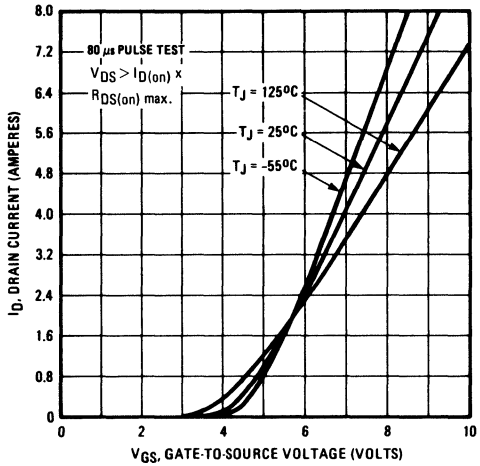


Fig. 2 — Typical Transfer Characteristics

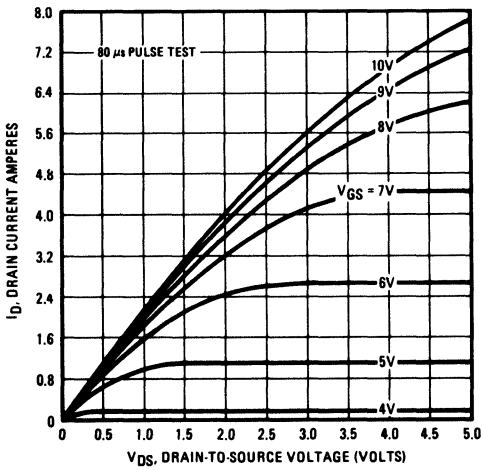


Fig. 3 — Typical Saturation Characteristics

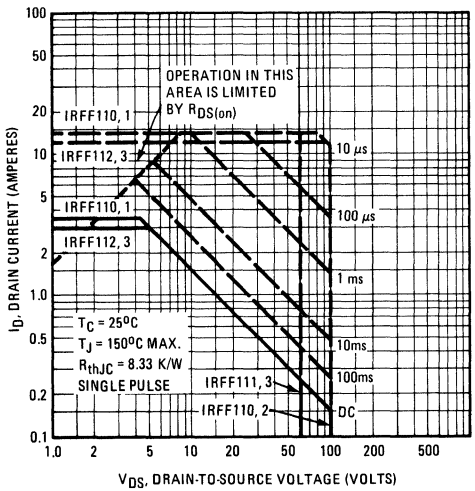


Fig. 4 — Maximum Safe Operating Area

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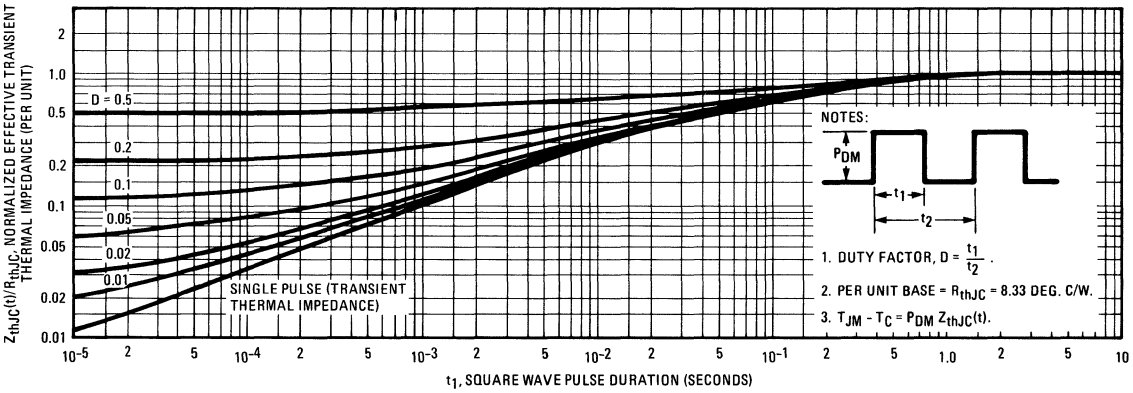


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

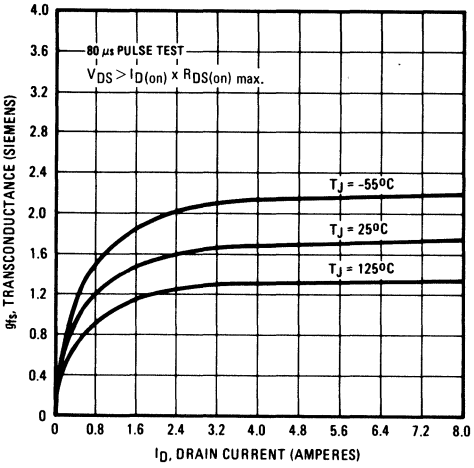


Fig. 6 — Typical Transconductance Vs. Drain Current

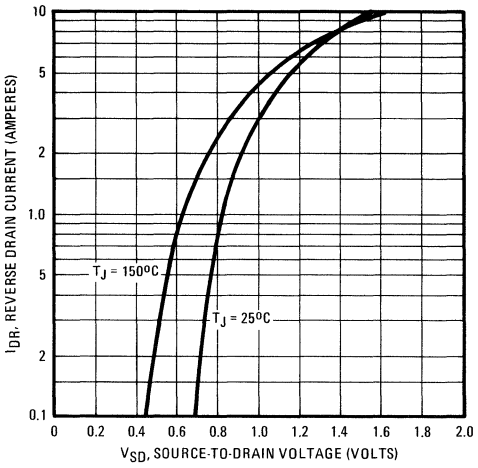


Fig. 7 — Typical Source-Drain Diode Forward Voltage

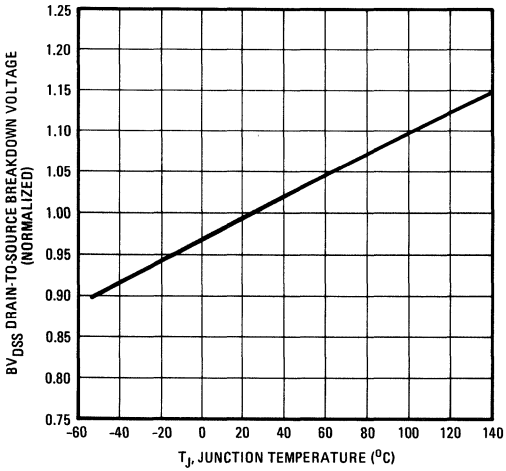


Fig. 8 — Breakdown Voltage Vs. Temperature

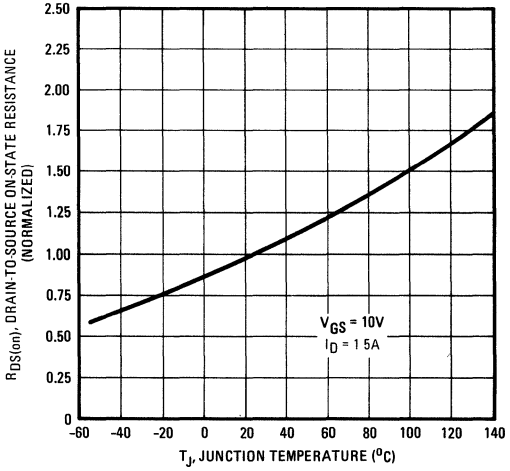


Fig. 9 — Normalized On-Resistance Vs. Temperature

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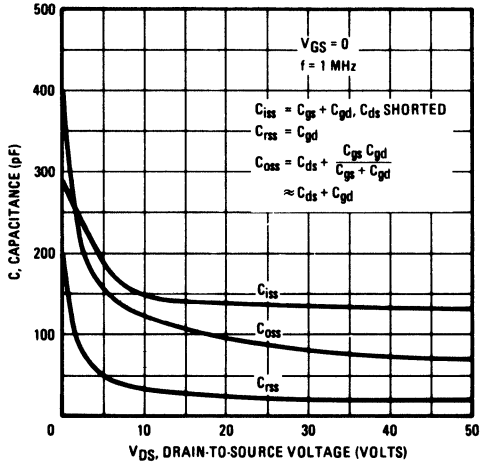


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

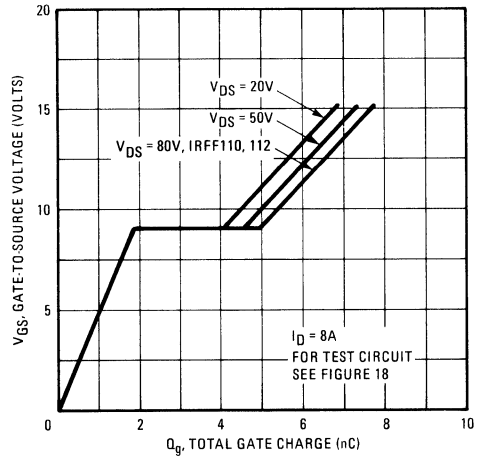


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

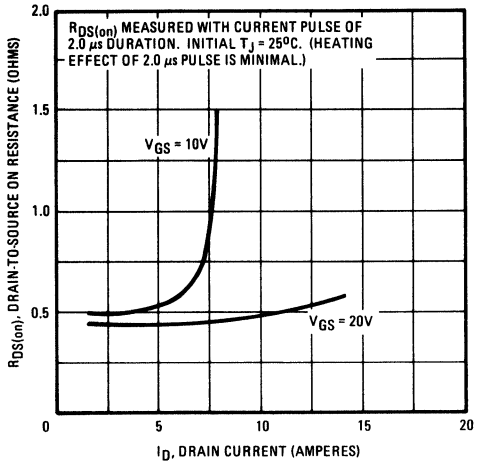


Fig. 12 — Typical On-Resistance Vs. Drain Current

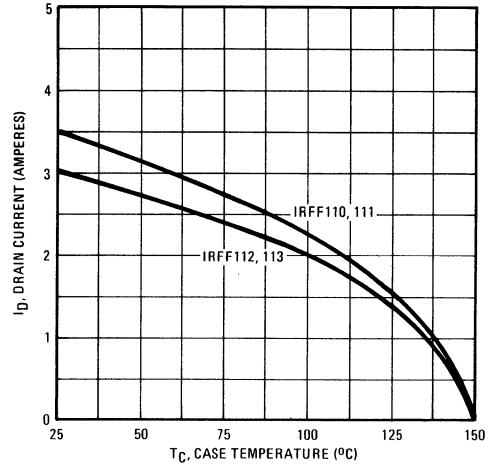


Fig. 13 — Maximum Drain Current Vs. Case Temperature

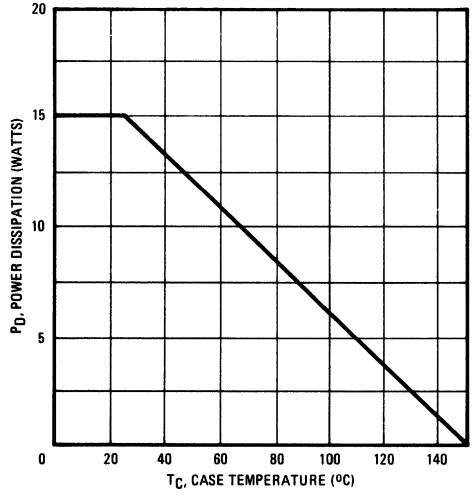


Fig. 14 — Power Vs. Temperature Derating Curve

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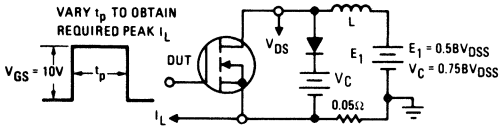


Fig. 15 – Clamped Inductive Test Circuit

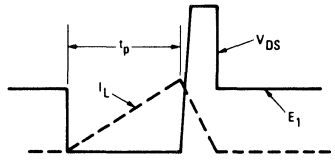


Fig. 16 – Clamped Inductive Waveforms

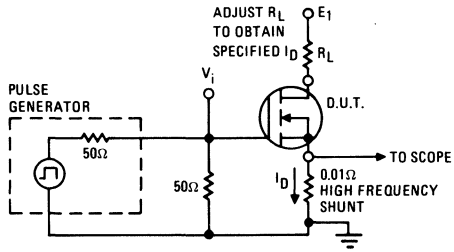


Fig. 17 – Switching Time Test Circuit

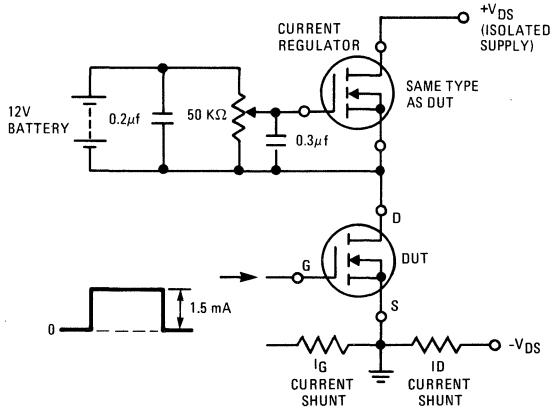


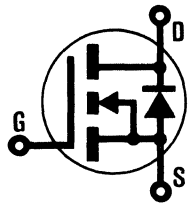
Fig. 18 – Gate Charge Test Circuit

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS IRFF120

N-CHANNEL POWER MOSFETs TO-39 PACKAGE



IRFF121
IRFF122
IRFF123

100 Volt, 0.30 Ohm HEXFET®

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

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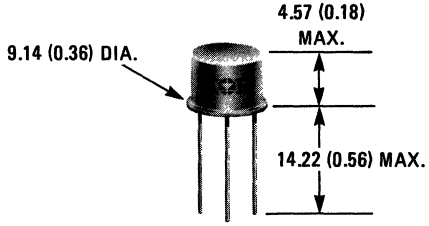
Features:

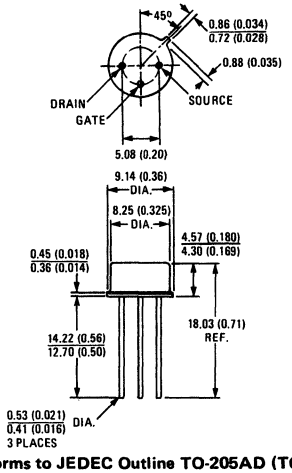
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFF120	100V	0.30Ω	6.0A
IRFF121	60V	0.30Ω	6.0A
IRFF122	100V	0.40Ω	5.0A
IRFF123	60V	0.40Ω	5.0A

CASE STYLE AND DIMENSIONS





Conforms to JEDEC Outline TO-205AD (TO-39)
All Dimensions in Millimeters and (Inches)

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IRFF120, IRFF121, IRFF122, IRFF123 Devices

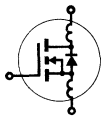
Absolute Maximum Ratings

Parameter		IRFF120	IRFF121	IRFF122	IRFF123	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	6.0	6.0	5.0	5.0	A
I_{DM}	Pulsed Drain Current ③	24	24	20	20	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	20 (See Fig. 14)				W
	Linear Derating Factor	0.16 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		24	24	20	20	
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFF120 IRFF122	100	—	—	V	V_{GS} = 0V
		IRFF121 IRFF123	60	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFF120 IRFF121	6.0	—	—	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRFF122 IRFF123	5.0	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFF120 IRFF121	—	0.25	0.30	Ω	V_{GS} = 10V, I_D = 3.0A
		IRFF122 IRFF123	—	0.30	0.40	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.5	2.9	—	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 3.0A
C_{iss}	Input Capacitance	ALL	—	450	600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	200	400	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	50	100	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	20	40	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 3.0A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	37	70	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	50	100	ns	
t_f	Fall Time	ALL	—	35	70	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	10	15	nC	V_{GS} = 10V, I_D = 10A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	6.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	4.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5 mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	6.25	K/W	
R_{thJA}	Junction-to-Ambient	ALL	—	—	175	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFF120 IRFF121	–	–	6.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFF122 IRFF123	–	–	5.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF120 IRFF121	–	–	24	A	
		IRFF122 IRFF123	–	–	20	A	
V_{SD}	Diode Forward Voltage ②	IRFF120 IRFF121	–	–	2.5	V	T_C = 25°C, I_S = 6.0A, V_{GS} = 0V
		IRFF122 IRFF123	–	–	2.3	V	T_C = 25°C, I_S = 5.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	230	–	ns	T_J = 150°C, I_F = 6.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	1.2	–	μC	T_J = 150°C, I_F = 6.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

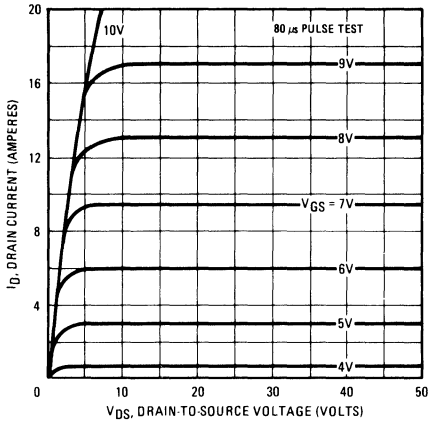


Fig. 1 — Typical Output Characteristics

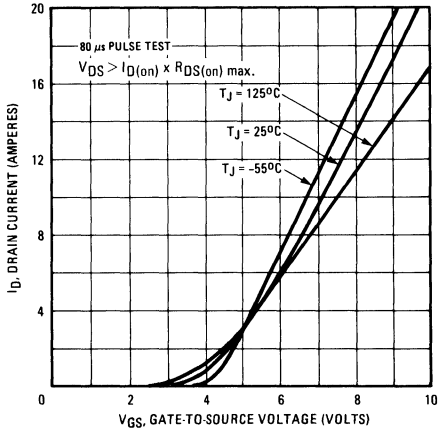


Fig. 2 — Typical Transfer Characteristics

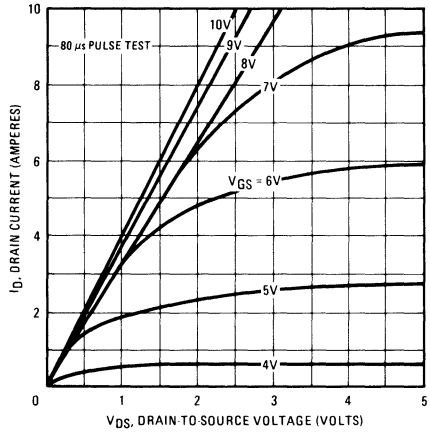


Fig. 3 — Typical Saturation Characteristics

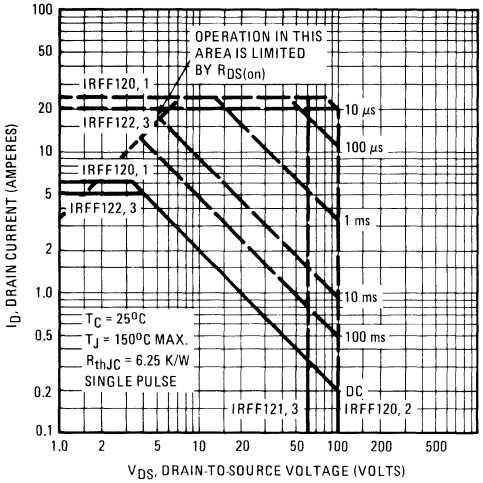


Fig. 4 — Maximum Safe Operating Area

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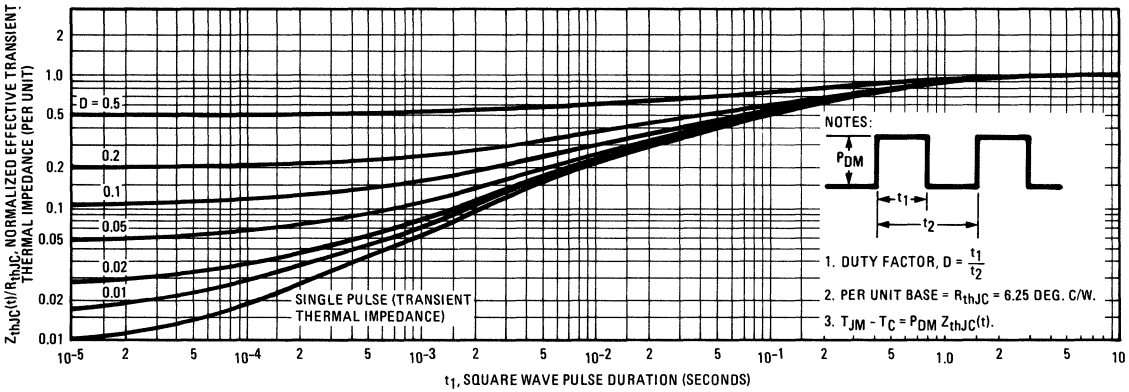


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

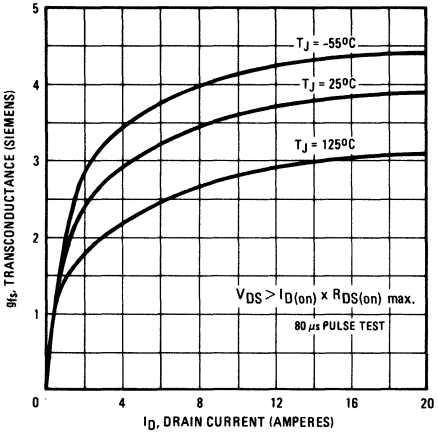


Fig. 6 — Typical Transconductance Vs. Drain Current

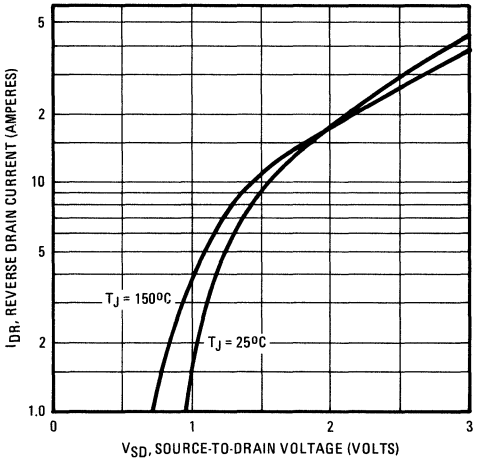


Fig. 7 — Typical Source-Drain Diode Forward Voltage

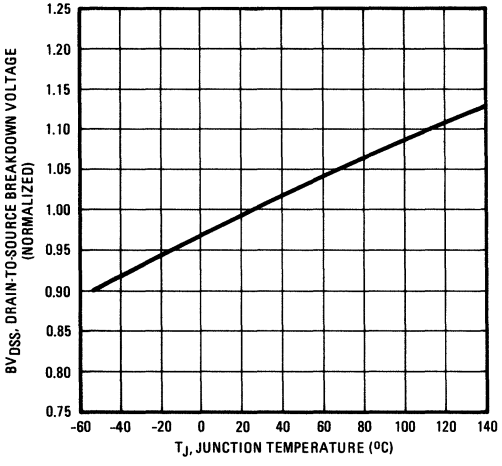


Fig. 8 — Breakdown Voltage Vs. Temperature

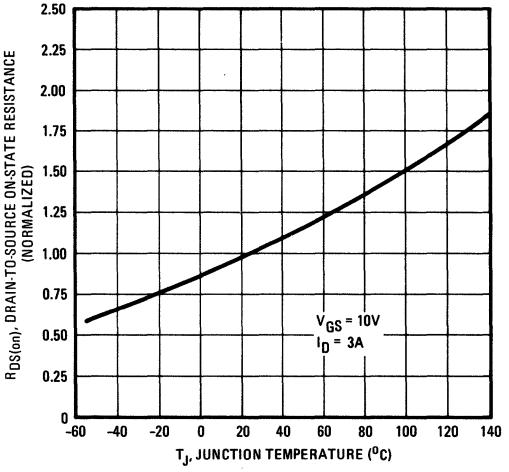


Fig. 9 — Normalized On-Resistance Vs. Temperature

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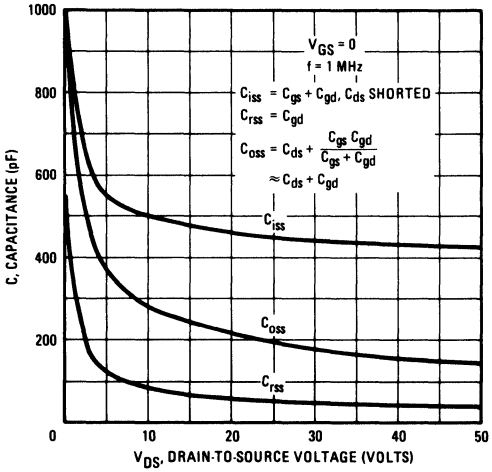


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

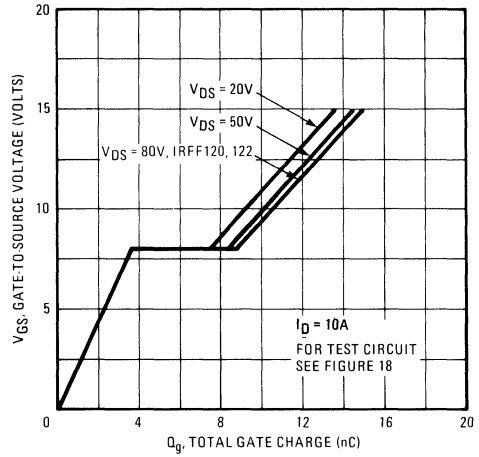


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

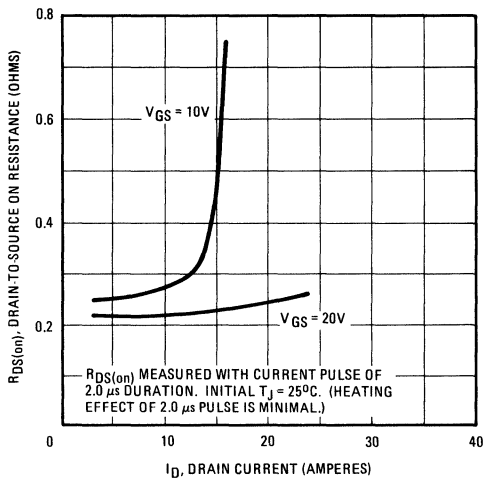


Fig. 12 — Typical On-Resistance Vs. Drain Current

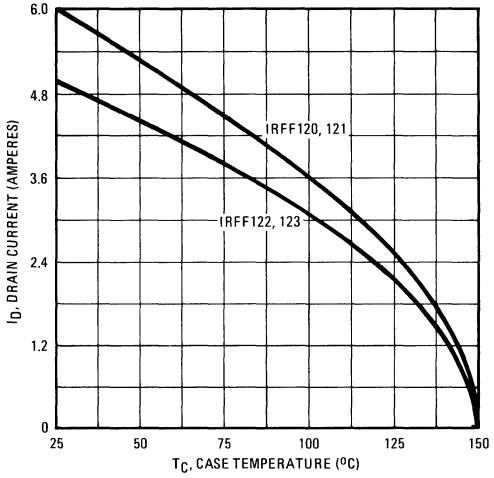


Fig. 13 — Maximum Drain Current Vs. Case Temperature

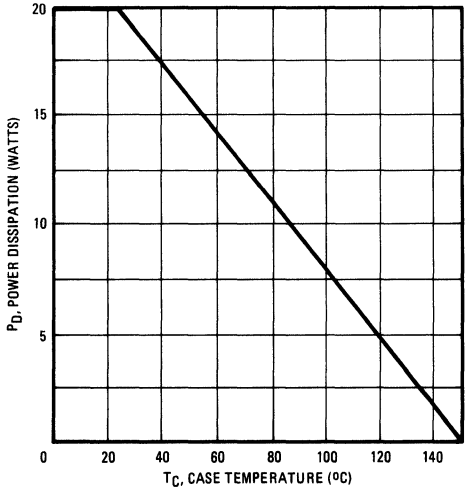


Fig. 14 — Power Vs. Temperature Derating Curve

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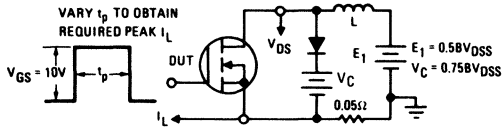


Fig. 15 — Clamped Inductive Test Circuit

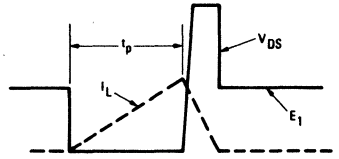


Fig. 16 — Clamped Inductive Waveforms

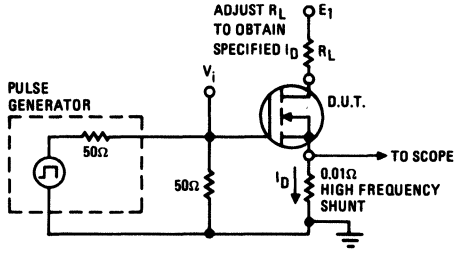


Fig. 17 — Switching Time Test Circuit

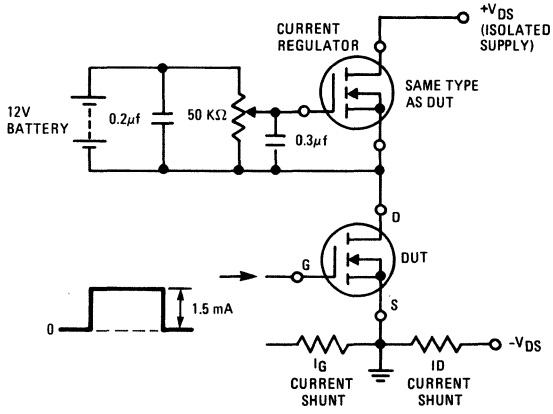


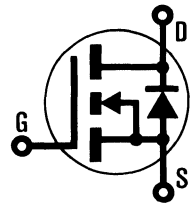
Fig. 18 — Gate Charge Test Circuit

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS IRFF130

N-CHANNEL POWER MOSFETs TO-39 PACKAGE



IRFF131
IRFF132
IRFF133

100 Volt, 0.18 Ohm HEXFET®

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

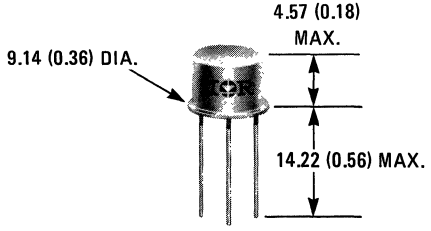
Features:

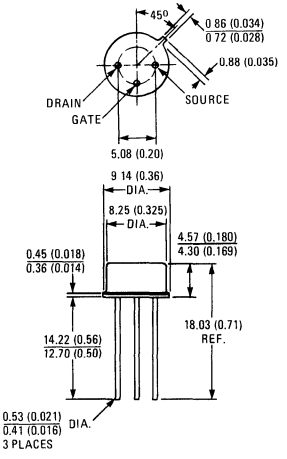
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFF130	100V	0.18Ω	8.0A
IRFF131	60V	0.18Ω	8.0A
IRFF132	100V	0.25Ω	7.0A
IRFF133	60V	0.25Ω	7.0A

CASE STYLE AND DIMENSIONS





Conforms to JEDEC Outline TO-205AD (TO-39)
All Dimensions in Millimeters and (Inches)

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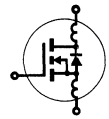
Absolute Maximum Ratings

Parameter		IRFF130	IRFF131	IRFF132	IRFF133	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_{DM}	Pulsed Drain Current ③	32	32	28	28	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	25 (See Fig. 14)				W
	Linear Derating Factor	0.2 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		32	32	28	28	
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFF130 IRFF132	100	–	–	V	V_{GS} = 0V
		IRFF131 IRFF133	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	−100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFF130 IRFF131	8.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRFF132 IRFF133	7.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFF130 IRFF131	–	0.14	0.18	Ω	V_{GS} = 10V, I_D = 4.0A
		IRFF132 IRFF133	–	0.20	0.25	Ω	
g_{fs}	Forward Transconductance ②	ALL	4.0	5.5	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 4.0A
C_{iss}	Input Capacitance	ALL	–	600	800	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	300	500	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	100	150	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	30	50	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 4.0A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	80	150	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	80	150	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	18	30	nC	V_{GS} = 10V, I_D = 18A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	9.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	9.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 5 mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	ALL	–	15	–	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	5.0	K/W	
R_{thJA}	Junction-to-Ambient	ALL	–	–	175	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFF130 IRFF131	–	–	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFF132 IRFF133	–	–	7.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF130 IRFF131	–	–	32	A	
		IRFF132 IRFF133	–	–	28	A	
V_{SD}	Diode Forward Voltage ②	IRFF130 IRFF131	–	–	2.5	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
		IRFF132 IRFF133	–	–	2.3	V	T_C = 25°C, I_S = 7.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	300	–	ns	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	1.5	–	μC	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

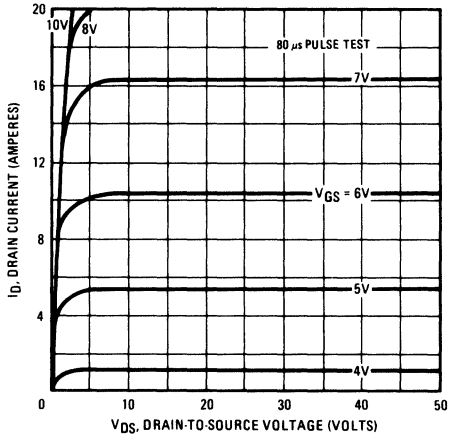


Fig. 1 – Typical Output Characteristics

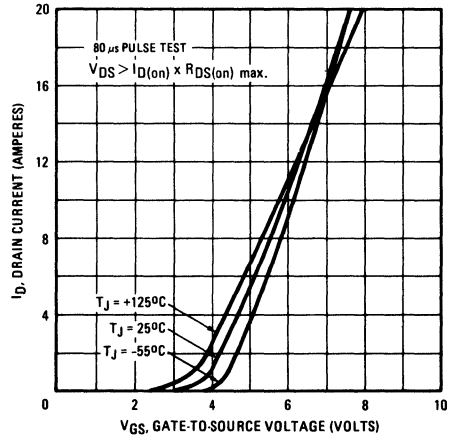


Fig. 2 – Typical Transfer Characteristics

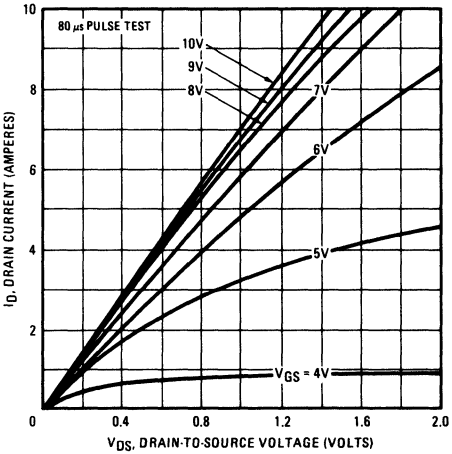


Fig. 3 – Typical Saturation Characteristics

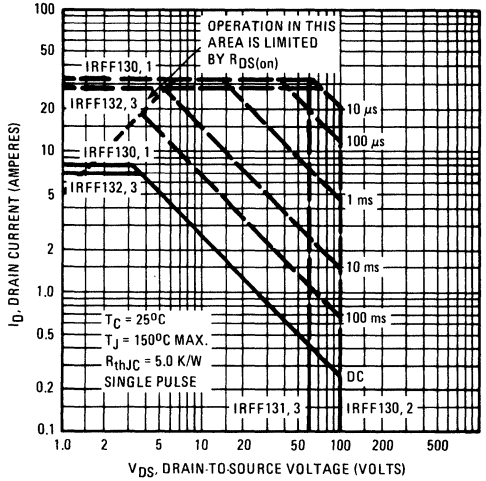


Fig. 4 – Maximum Safe Operating Area

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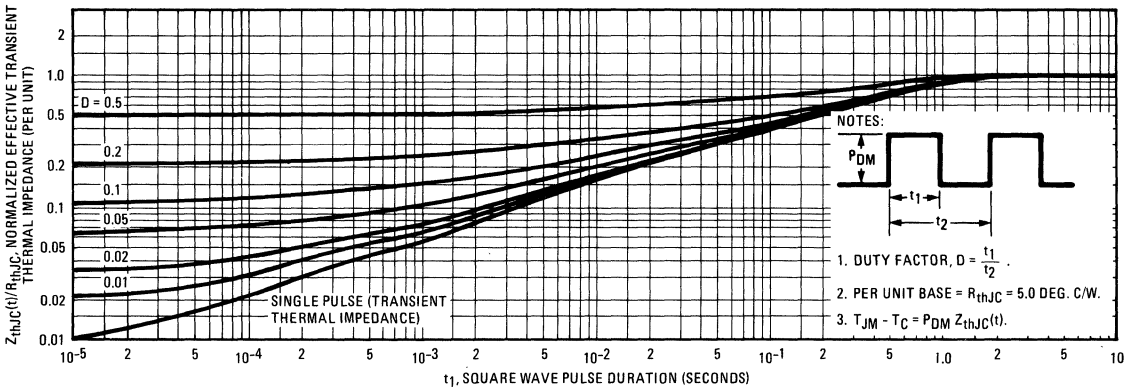


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

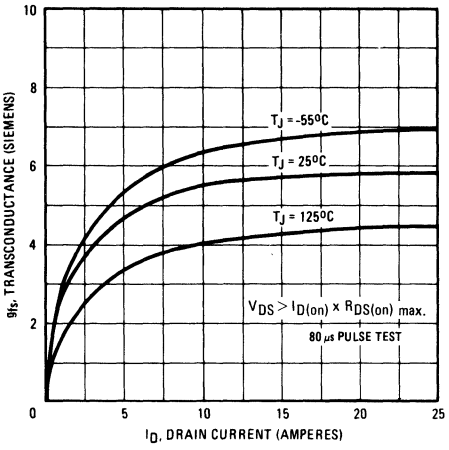


Fig. 6 — Typical Transconductance Vs. Drain Current

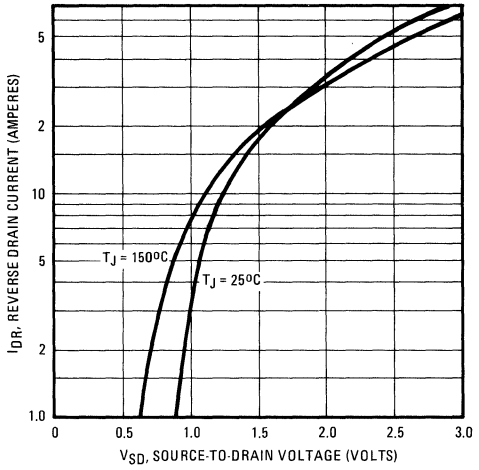


Fig. 7 — Typical Source-Drain Diode Forward Voltage

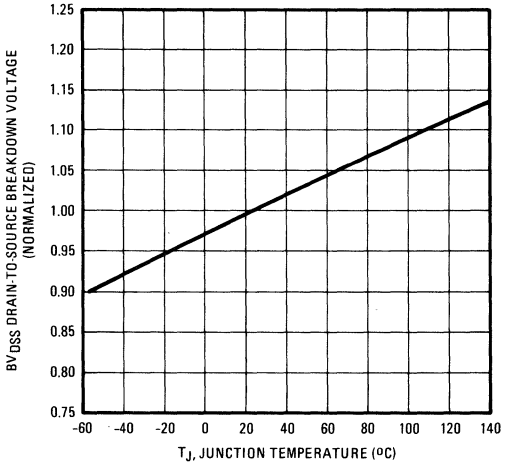


Fig. 8 — Breakdown Voltage Vs. Temperature

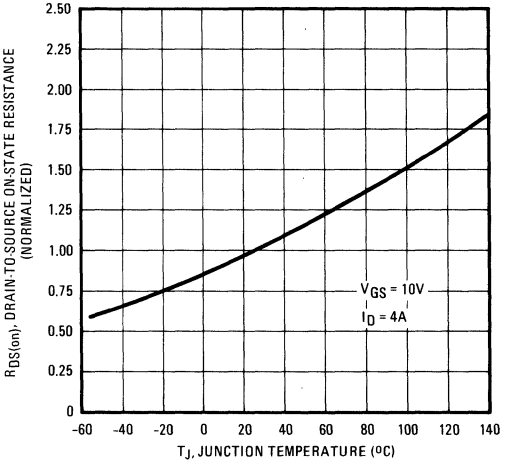


Fig. 9 — Normalized On-Resistance Vs. Temperature

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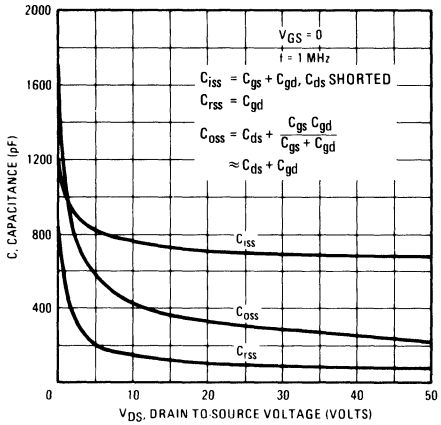


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

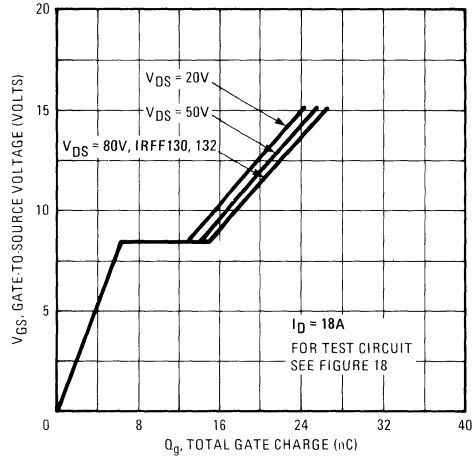


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

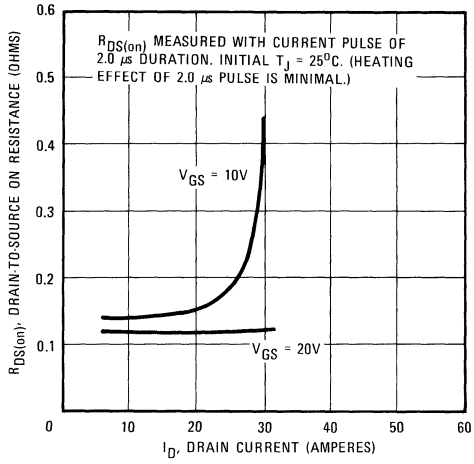


Fig. 12 — Typical On-Resistance Vs. Drain Current

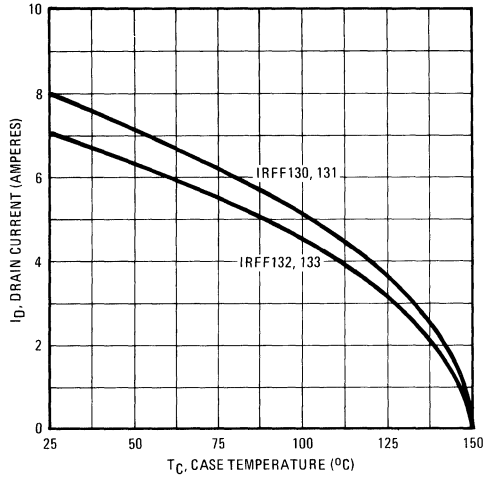


Fig. 13 — Maximum Drain Current Vs. Case Temperature

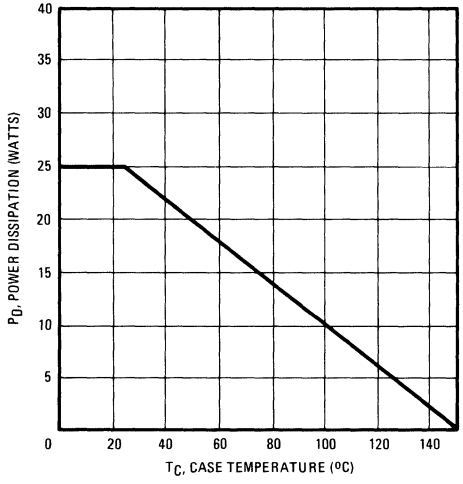


Fig. 14 — Power Vs. Temperature Derating Curve

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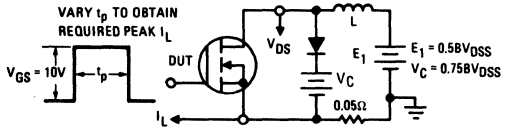


Fig. 15 – Clamped Inductive Test Circuit

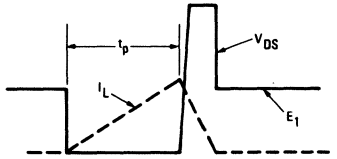


Fig. 16 – Clamped Inductive Waveforms

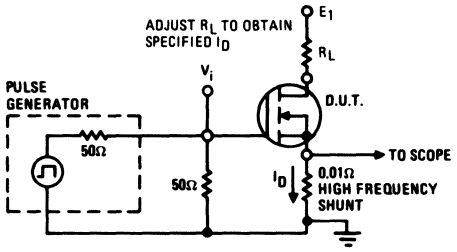


Fig. 17 – Switching Time Test Circuit

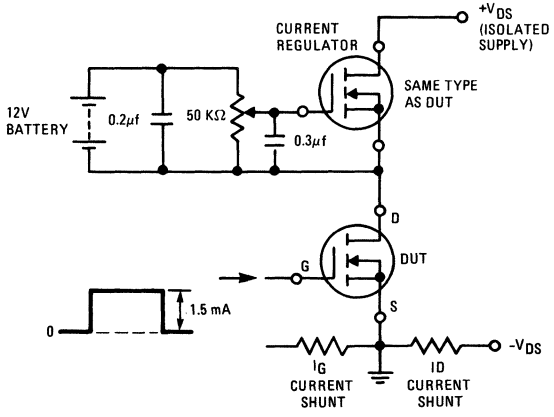
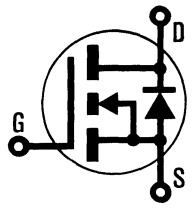


Fig. 18 – Gate Charge Test Circuit

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS IRF120 IRF121 IRF122 IRF123



N-Channel

100 Volt, 0.3 Ohm HEXFET

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

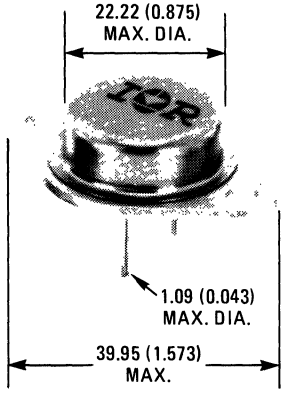
Features:

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

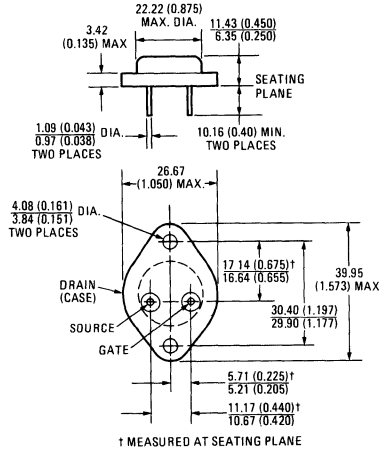
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF120	100V	0.30Ω	8.0A
IRF121	60V	0.30Ω	8.0A
IRF122	100V	0.40Ω	7.0A
IRF123	60V	0.40Ω	7.0A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



† MEASURED AT SEATING PLANE

Conforms to JEDEC Outline TO-204AA (TO-3)
Dimensions in Millimeters and (Inches)

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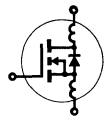
Absolute Maximum Ratings

	Parameter	IRF120	IRF121	IRF122	IRF123	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_D @ T_C = 100°C	Continuous Drain Current	5.0	5.0	4.0	4.0	A
I_{DM}	Pulsed Drain Current ③	32	32	28	28	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 32	32	28	28	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF120 IRF122	100	–	–	V	V_{GS} = 0V
		IRF121 IRF123	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF120 IRF121	8.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF122 IRF123	7.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF120 IRF121	–	0.25	0.30	Ω	V_{GS} = 10V, I_D = 4.0A
		IRF122 IRF123	–	0.30	0.40	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.5	2.9	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 4.0A
C_{iss}	Input Capacitance	ALL	–	450	600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	200	400	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	50	100	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 4.0A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	35	70	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	35	70	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	10	15	nC	V_{GS} = 10V, I_D = 10A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	6.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	4.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	3.12	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF120 IRF121	–	–	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF122 IRF123	–	–	7.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF120 IRF121	–	–	32	A	
		IRF122 IRF123	–	–	28	A	
V_{SD}	Diode Forward Voltage ②	IRF120 IRF121	–	–	2.5	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
		IRF122 IRF123	–	–	2.3	V	T_C = 25°C, I_S = 7.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	280	–	ns	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	1.6	–	μC	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

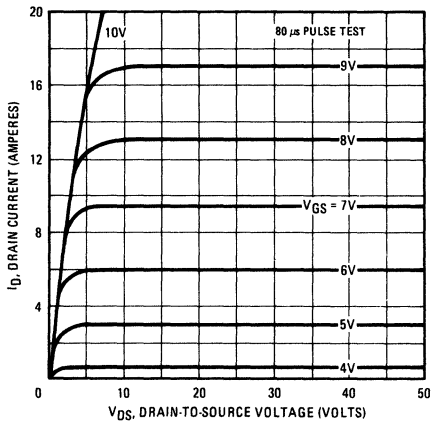


Fig. 1 — Typical Output Characteristics

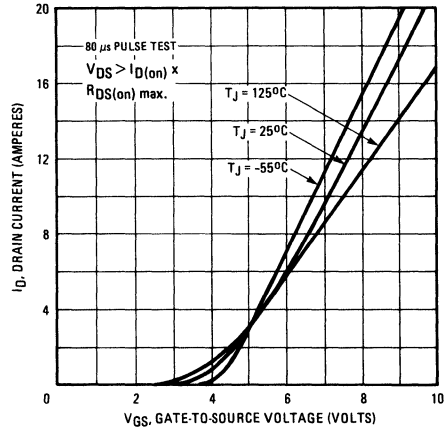


Fig. 2 — Typical Transfer Characteristics

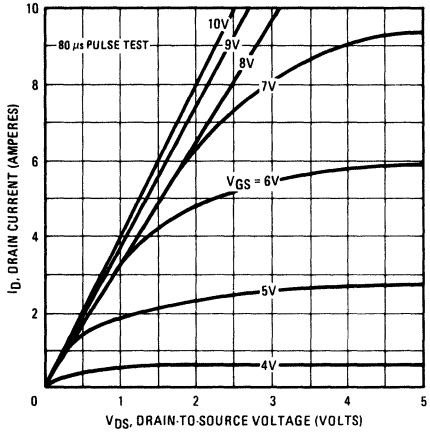


Fig. 3 — Typical Saturation Characteristics

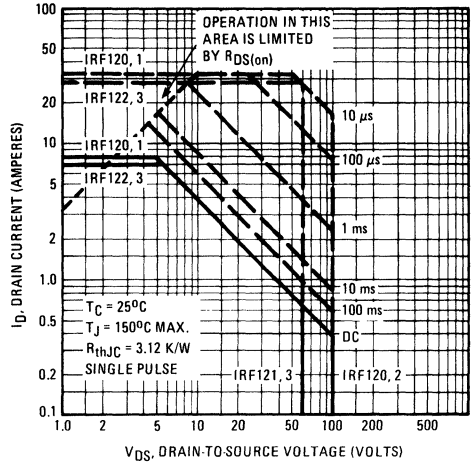


Fig. 4 — Maximum Safe Operating Area

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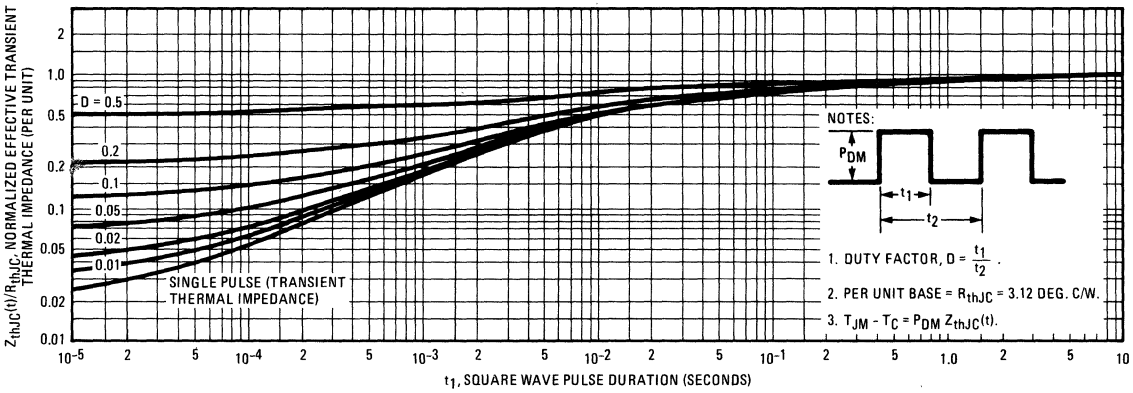


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

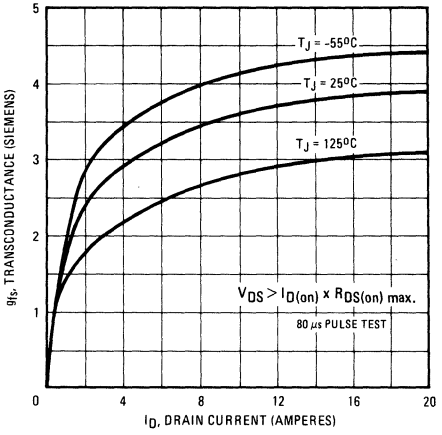


Fig. 6 — Typical Transconductance Vs. Drain Current

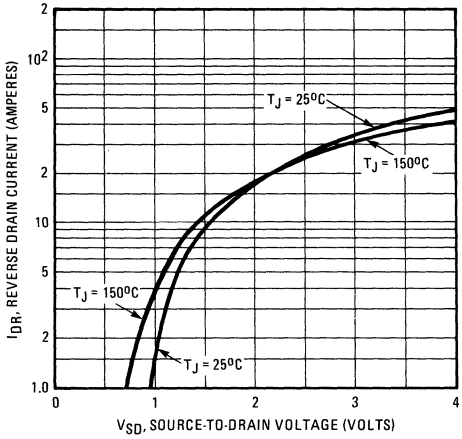


Fig. 7 — Typical Source-Drain Diode Forward Voltage

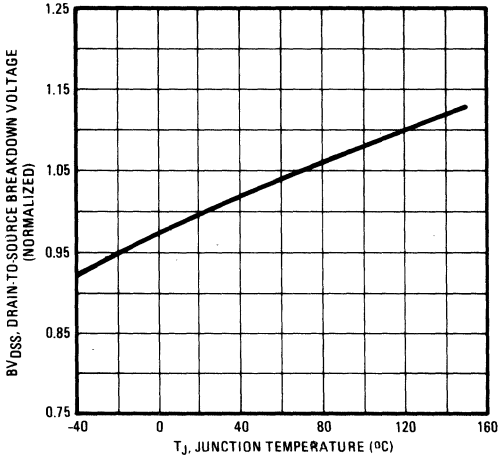


Fig. 8 — Breakdown Voltage Vs. Temperature

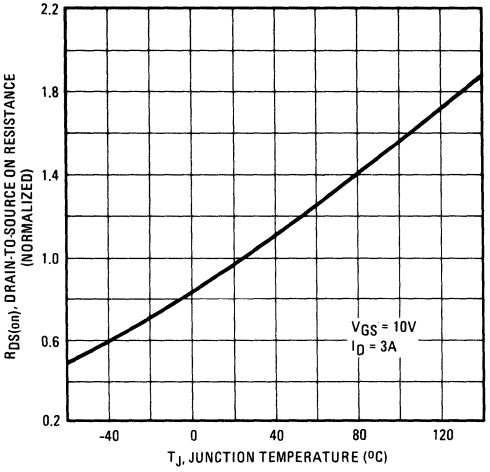


Fig. 9 — Normalized On-Resistance Vs. Temperature

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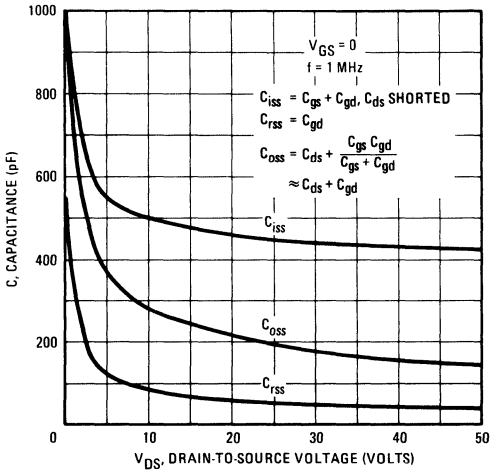


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

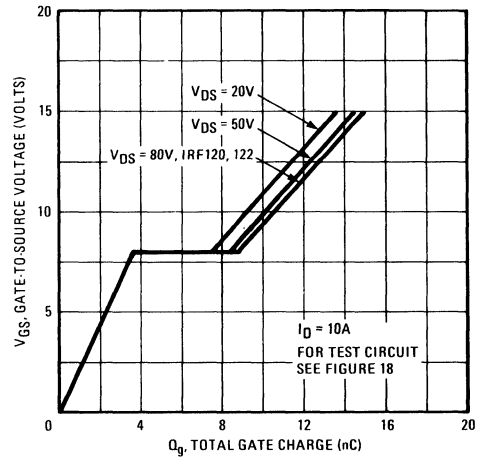


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

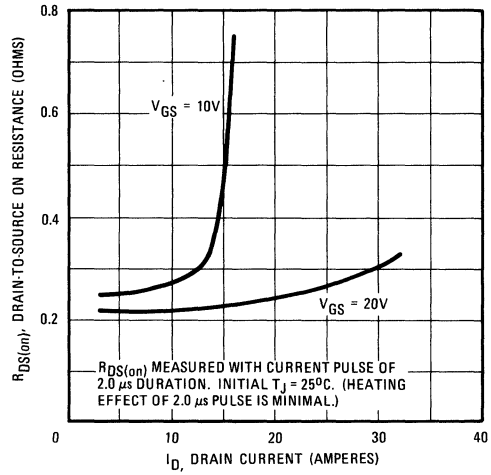


Fig. 12 — Typical On-Resistance Vs. Drain Current

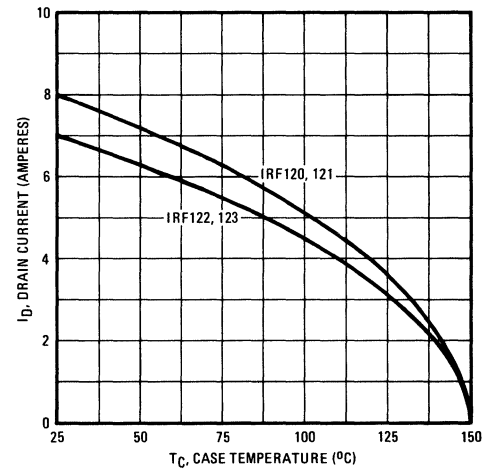


Fig. 13 — Maximum Drain Current Vs. Case Temperature

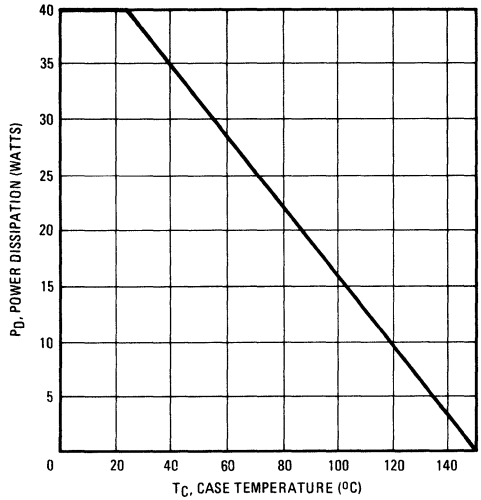


Fig. 14 — Power Vs. Temperature Derating Curve

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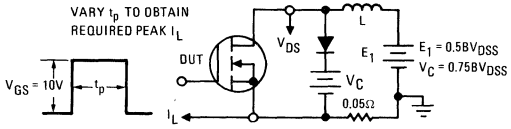


Fig. 15 — Clamped Inductive Test Circuit

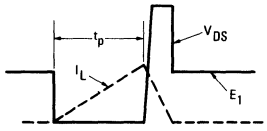


Fig. 16 — Clamped Inductive Waveforms

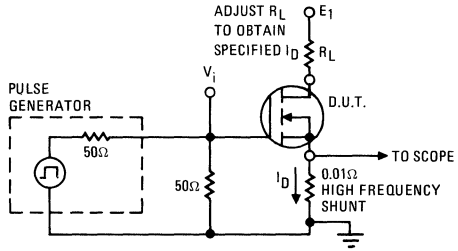


Fig. 17 — Switching Time Test Circuit

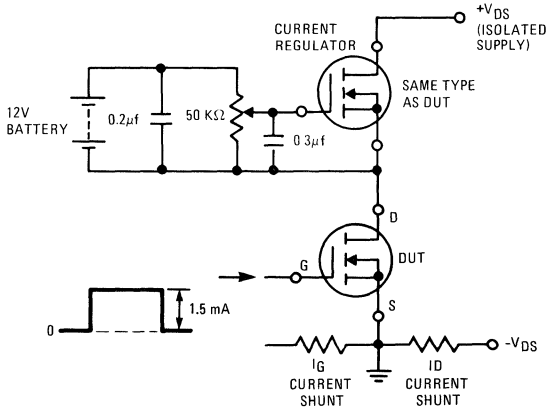
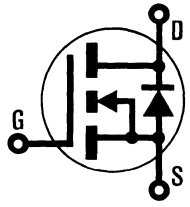


Fig. 18 — Gate Charge Test Circuit

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS IRF130 IRF131 IRF132 IRF133



N-Channel

100 Volt, 0.18 Ohm HEXFET

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

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They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

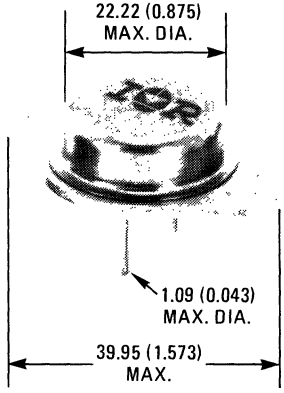
Features:

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

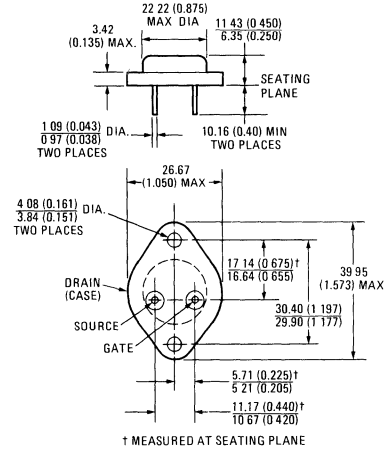
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF130	100V	0.18Ω	14A
IRF131	60V	0.18Ω	14A
IRF132	100V	0.25Ω	12A
IRF133	60V	0.25Ω	12A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



† MEASURED AT SEATING PLANE

Conforms to JEDEC Outline TO-204AA (TO-3)
Dimensions in Millimeters and (Inches)

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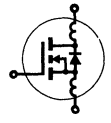
Absolute Maximum Ratings

Parameter		IRF130	IRF131	IRF132	IRF133	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	14	14	12	12	A
I_D @ T_C = 100°C	Continuous Drain Current	9.0	9.0	8.0	8.0	A
I_{DM}	Pulsed Drain Current ③	56	56	48	48	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		56	56	48	48	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF130 IRF132	100	–	–	V	V_{GS} = 0V
		IRF131 IRF133	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF130 IRF131	14	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF132 IRF133	12	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF130 IRF131	–	0.14	0.18	Ω	V_{GS} = 10V, I_D = 8.0A
		IRF132 IRF133	–	0.20	0.25	Ω	
g_{fs}	Forward Transconductance ②	ALL	4.0	5.5	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 8.0A
C_{iss}	Input Capacitance	ALL	–	600	800	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	300	500	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	100	150	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} ≈ 36V, I_D = 8.0A, Z_o = 15Ω See Fig. 17
t_r	Rise Time	ALL	–	–	75	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	40	ns	(MOSFET switching times are essentially independent of operating temperature.)
t_f	Fall Time	ALL	–	–	45	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	18	30	nC	V_{GS} = 10V, I_D = 18A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	9.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	9.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF130 IRF131	—	—	14	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF132 IRF133	—	—	12	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF130 IRF131	—	—	56	A	
		IRF132 IRF133	—	—	48	A	
V_{SD}	Diode Forward Voltage ②	IRF130 IRF131	—	—	2.5	V	T_C = 25°C, I_S = 14A, V_{GS} = 0V
		IRF132 IRF133	—	—	2.3	V	T_C = 25°C, I_S = 12A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	360	—	ns	T_J = 150°C, I_F = 14A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	2.1	—	μC	T_J = 150°C, I_F = 14A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

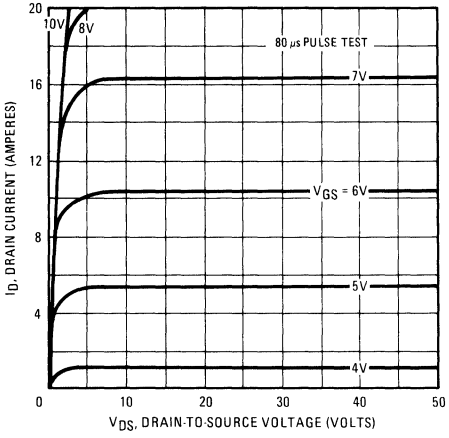


Fig. 1 — Typical Output Characteristics

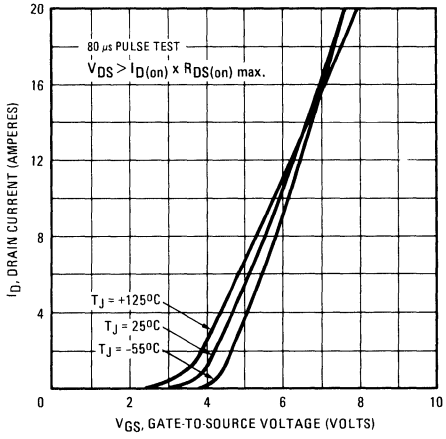


Fig. 2 — Typical Transfer Characteristics

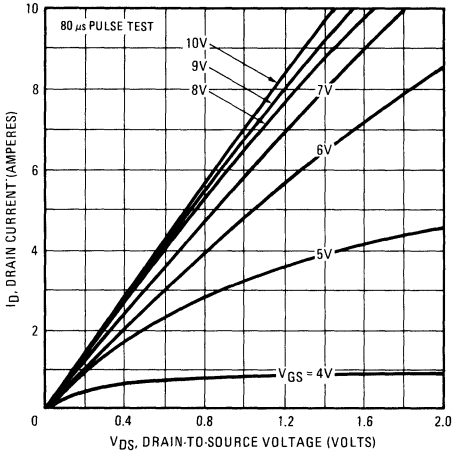


Fig. 3 — Typical Saturation Characteristics

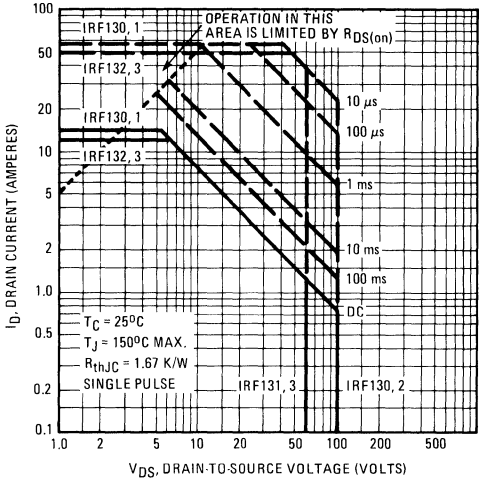


Fig. 4 — Maximum Safe Operating Area

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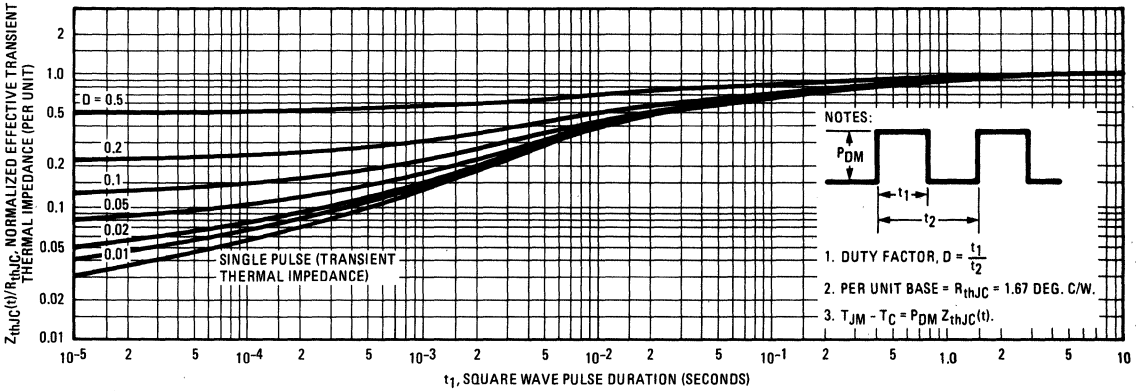


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

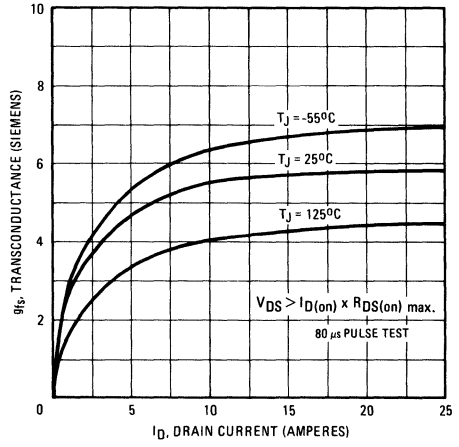


Fig. 6 — Typical Transconductance Vs. Drain Current

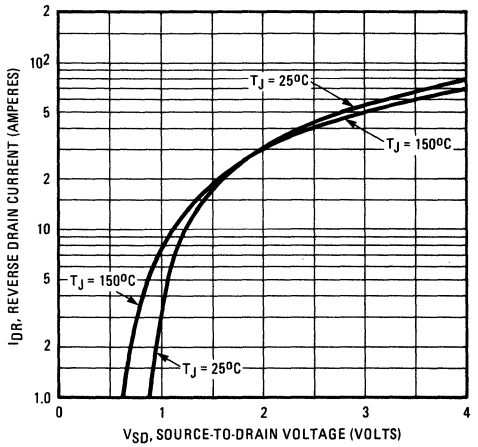


Fig. 7 — Typical Source-Drain Diode Forward Voltage

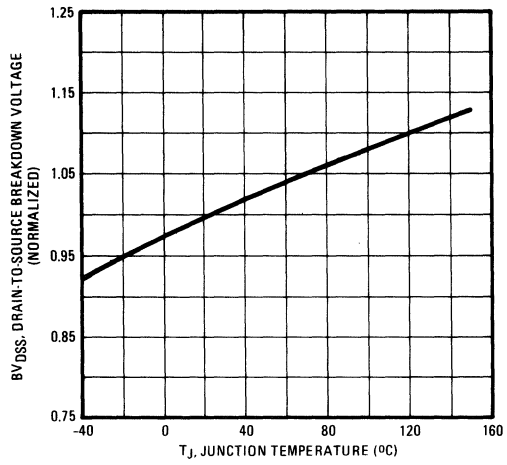


Fig. 8 — Breakdown Voltage Vs. Temperature

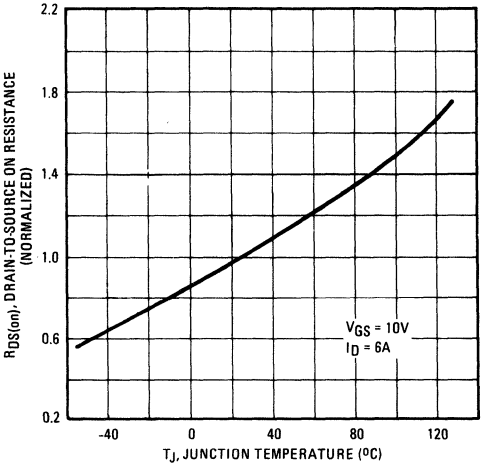


Fig. 9 — Normalized On-Resistance Vs. Temperature

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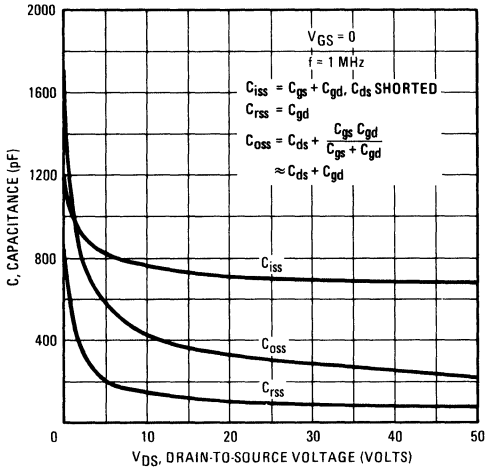


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

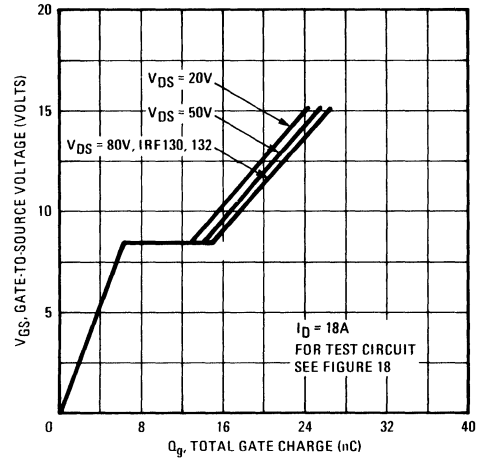


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

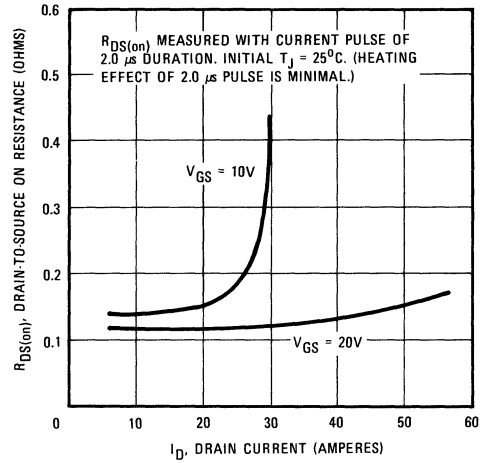


Fig. 12 — Typical On-Resistance Vs. Drain Current

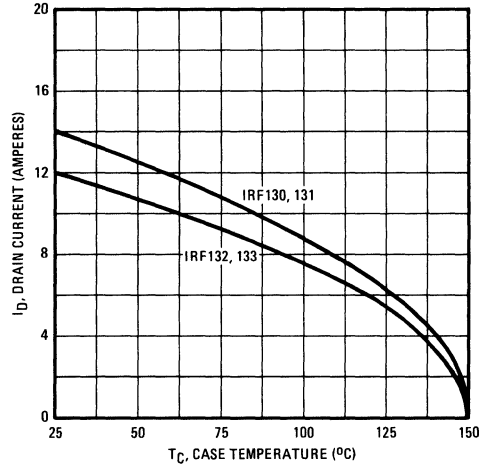


Fig. 13 — Maximum Drain Current Vs. Case Temperature

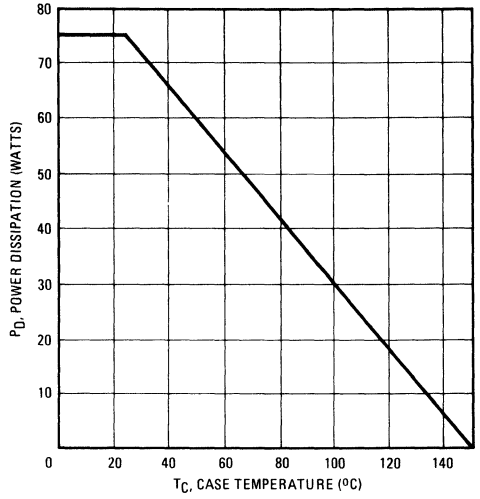


Fig. 14 — Power Vs. Temperature Derating Curve

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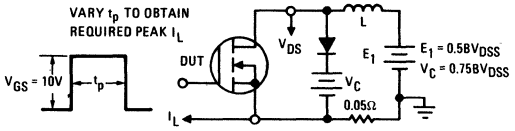


Fig. 15 — Clamped Inductive Test Circuit

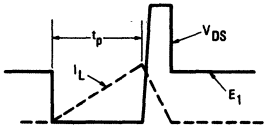


Fig. 16 — Clamped Inductive Waveforms

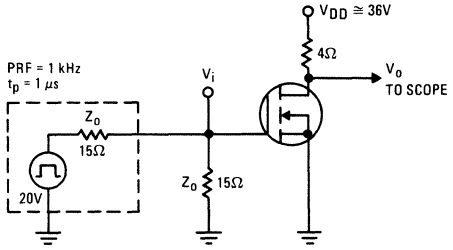


Fig. 17 — Switching Time Test Circuit

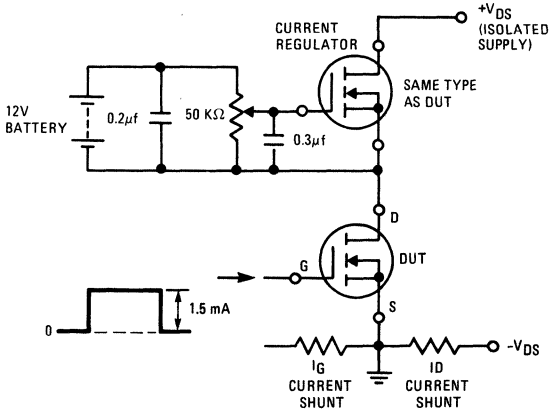


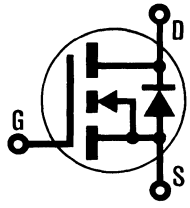
Fig. 18 — Gate Charge Test Circuit

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS IRF140 IRF141 IRF142 IRF143

N-CHANNEL POWER MOSFETs



100 Volt, 0.085 Ohm HEXFET

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

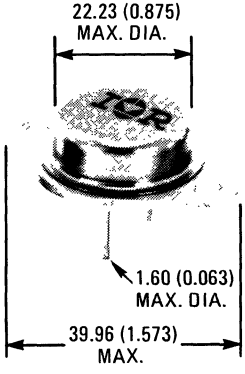
Features:

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

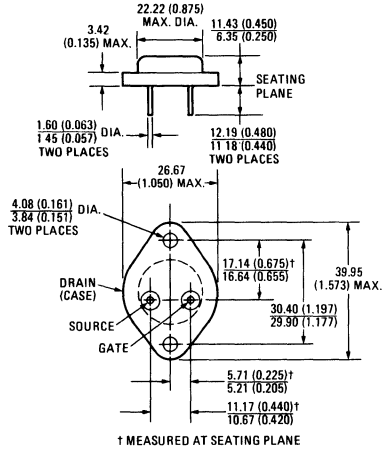
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF140	100V	0.085Ω	27A
IRF141	60V	0.085Ω	27A
IRF142	100V	0.11Ω	24A
IRF143	60V	0.11Ω	24A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



† MEASURED AT SEATING PLANE

Conforms to JEDEC Outline TO-204AA (TO-3)
Dimensions in Millimeters and (Inches)

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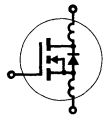
Absolute Maximum Ratings

Parameter		IRF140	IRF141	IRF142	IRF143	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	27	27	24	24	A
I_D @ T_C = 100°C	Continuous Drain Current	17	17	15	15	A
I_{DM}	Pulsed Drain Current ③	108	108	96	96	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		108	108	96	96	
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF140 IRF142	100	—	—	V	V_{GS} = 0V
		IRF141 IRF143	60	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	−100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF140 IRF141	27	—	—	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF142 IRF143	24	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF140 IRF141	—	0.07	0.085	Ω	V_{GS} = 10V, I_D = 15A
		IRF142 IRF143	—	0.09	0.11	Ω	
g_{fs}	Forward Transconductance ②	ALL	6.0	10	—	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 15A
C_{iss}	Input Capacitance	ALL	—	1275	1600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	550	800	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	160	300	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	16	30	ns	V_{DD} ≈ 30V, I_D = 15A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	27	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	38	80	ns	
t_f	Fall Time	ALL	—	14	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	38	60	nC	V_{GS} = 10V, I_D = 34A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	17	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	21	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	1.0	K/W	
R_{thCS}	Case-to-Sink	ALL	—	0.1	—	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF140 IRF141	—	—	27	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF142 IRF143	—	—	24	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF140 IRF141	—	—	108	A	
		IRF142 IRF143	—	—	96	A	
V_{SD}	Diode Forward Voltage ②	IRF140 IRF141	—	—	2.5	V	T_C = 25°C, I_S = 27A, V_{GS} = 0V
		IRF142 IRF143	—	—	2.3	V	T_C = 25°C, I_S = 24A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	500	—	ns	T_J = 150°C, I_F = 27A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	2.9	—	μC	T_J = 150°C, I_F = 27A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

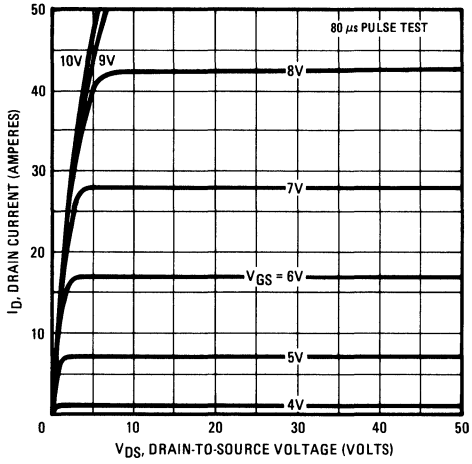


Fig. 1 — Typical Output Characteristics

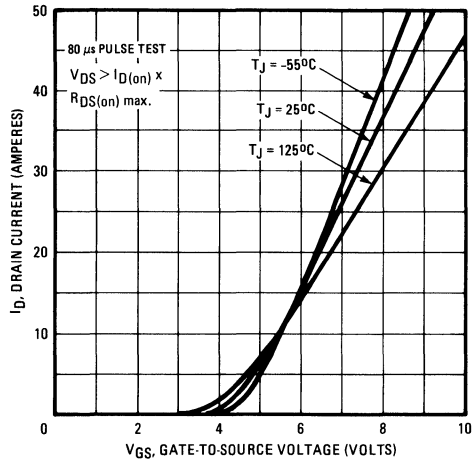


Fig. 2 — Typical Transfer Characteristics

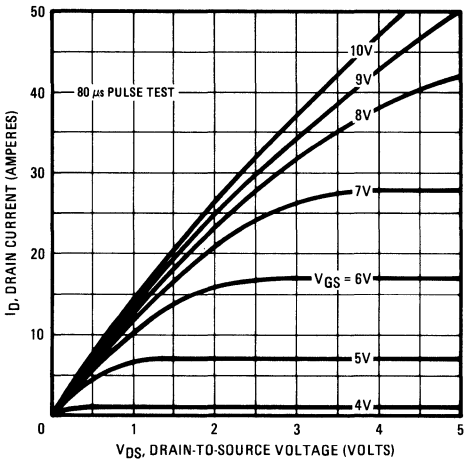


Fig. 3 — Typical Saturation Characteristics

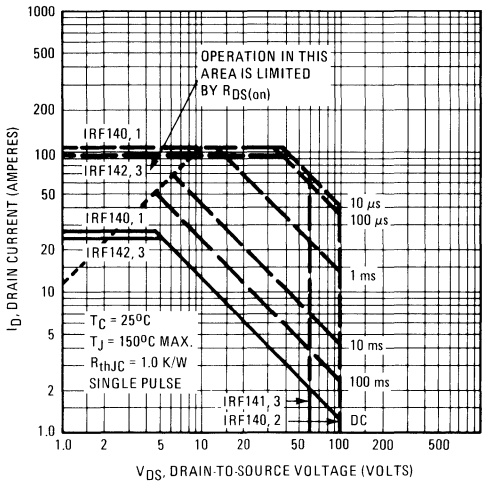


Fig. 4 — Maximum Safe Operating Area

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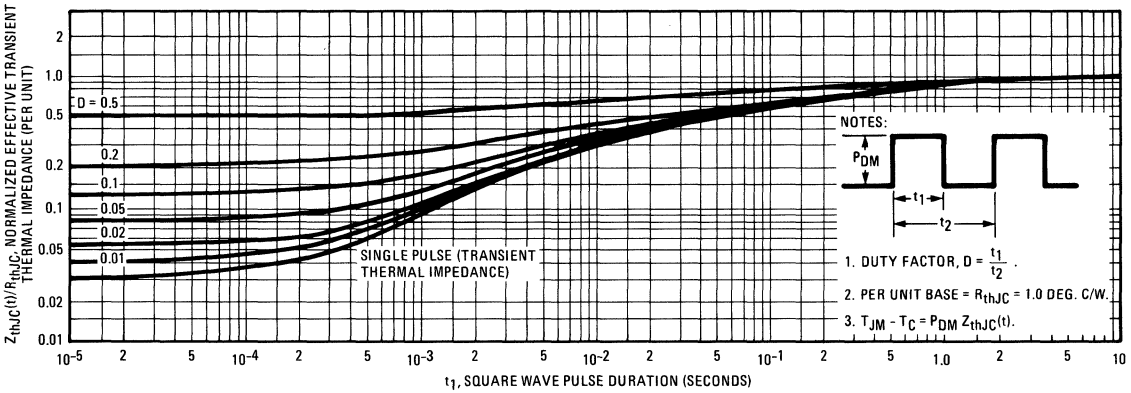


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

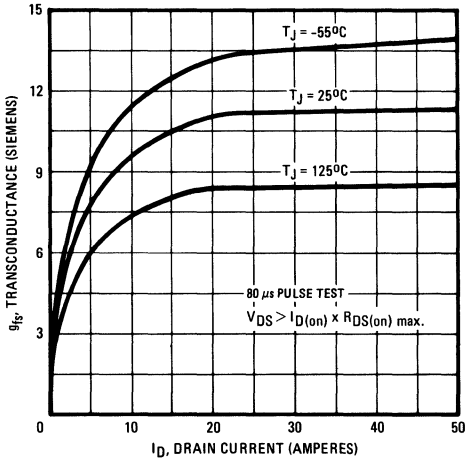


Fig. 6 — Typical Transconductance Vs. Drain Current

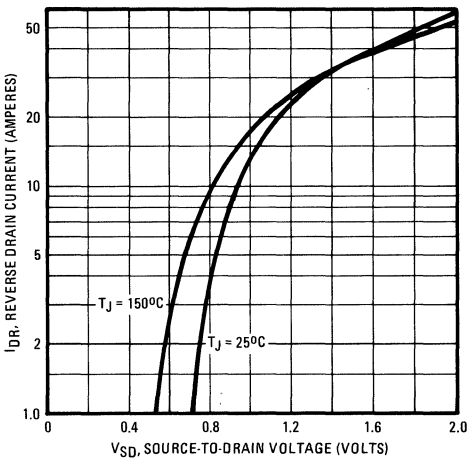


Fig. 7 — Typical Source-Drain Diode Forward Voltage

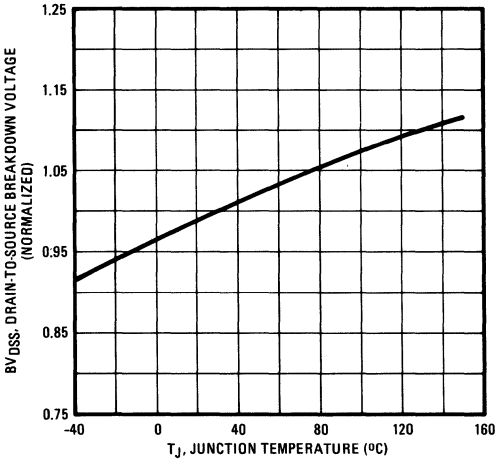


Fig. 8 — Breakdown Voltage Vs. Temperature

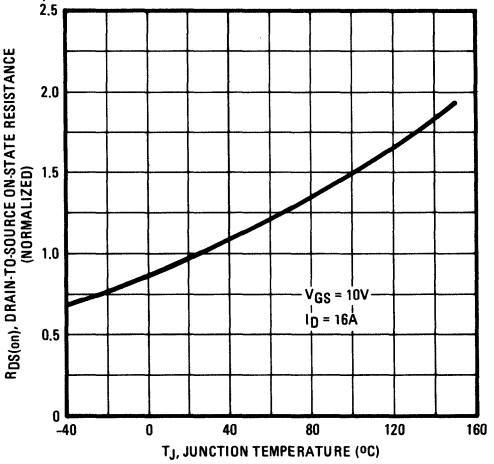


Fig. 9 — Normalized On-Resistance Vs. Temperature

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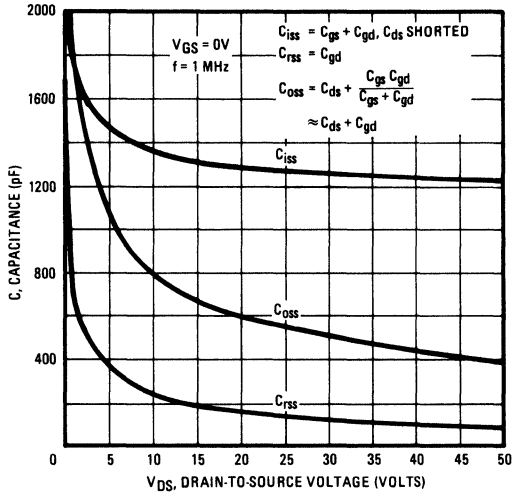


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

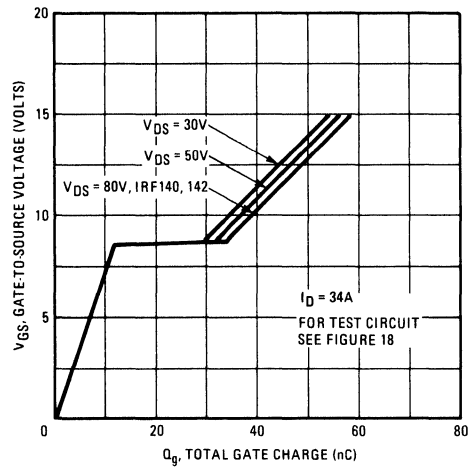


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

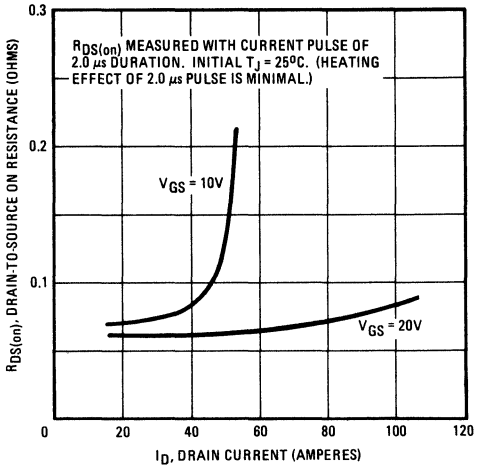


Fig. 12 — Typical On-Resistance Vs. Drain Current

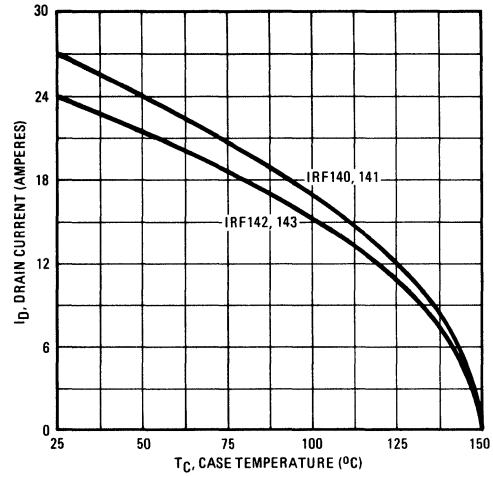


Fig. 13 — Maximum Drain Current Vs. Case Temperature

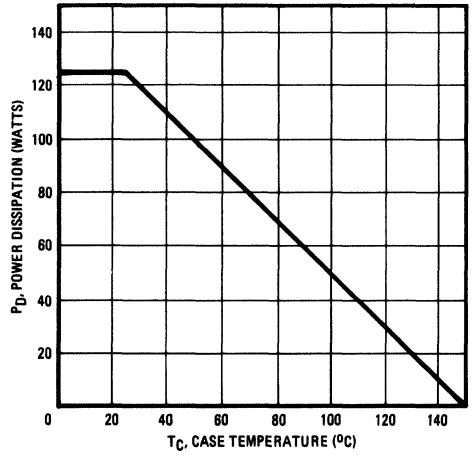


Fig. 14 — Power Vs. Temperature Derating Curve

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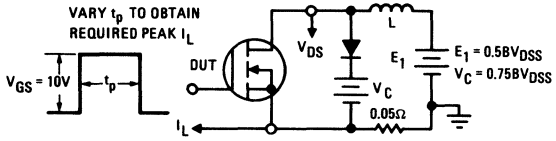


Fig. 15 — Clamped Inductive Test Circuit

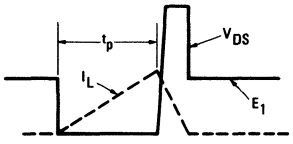


Fig. 16 — Clamped Inductive Waveforms

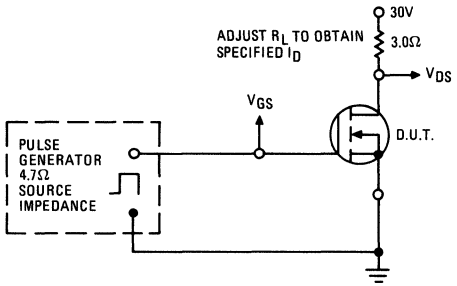


Fig. 17 — Switching Time Test Circuit

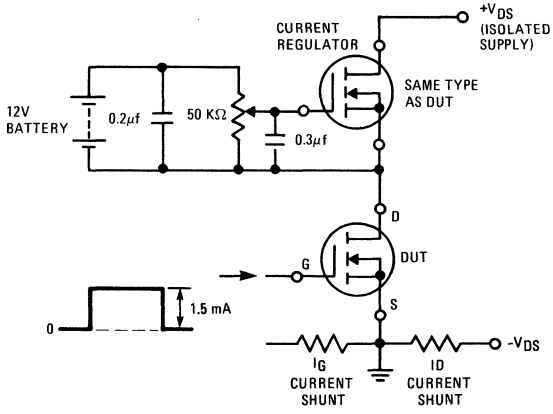
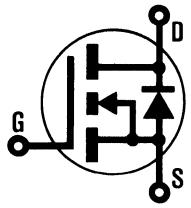


Fig. 18 — Gate Charge Test Circuit

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS IRF150 IRF151 IRF152 IRF153



N-Channel

100 Volt, 0.055 Ohm HEXFET

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

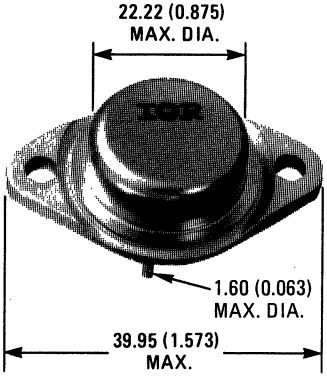
Features:

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

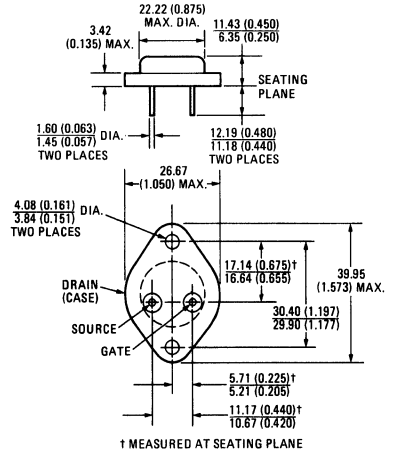
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF150	100V	0.055Ω	40A
IRF151	60V	0.055Ω	40A
IRF152	100V	0.08Ω	33A
IRF153	60V	0.08Ω	33A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



† MEASURED AT SEATING PLANE

Conforms to JEDEC Outline TO-204AE (Modified TO-3)
Dimensions in Millimeters and (Inches)

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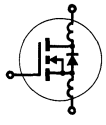
Absolute Maximum Ratings

Parameter		IRF150	IRF151	IRF152	IRF153	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	40	40	33	33	A
I_D @ T_C = 100°C	Continuous Drain Current	25	25	20	20	A
I_{DM}	Pulsed Drain Current ③	160	160	132	132	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	150 (See Fig. 14)				W
	Linear Derating Factor	1.2 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	160	(See Fig. 15 and 16) L = 100μH 160	132	132	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF150 IRF152	100	–	–	V	V_{GS} = 0V
		IRF151 IRF153	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF150 IRF151	40	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF152 IRF153	33	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF150 IRF151	–	0.045	0.055	Ω	V_{GS} = 10V, I_D = 20A
		IRF152 IRF153	–	0.06	0.08	Ω	
g_{fs}	Forward Transconductance ②	ALL	9.0	11	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 20A
C_{iss}	Input Capacitance	ALL	–	2000	3000	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	1000	1500	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	350	500	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	35	ns	V_{DD} = 24V, I_D = 20A, Z_o = 4.7Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	100	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	125	ns	
t_f	Fall Time	ALL	–	–	100	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	63	120	nC	V_{GS} = 10V, I_D = 50A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	27	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	36	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	0.83	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF150 IRF151	–	–	40	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF152 IRF153	–	–	33	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF150 IRF151	–	–	160	A	
		IRF152 IRF153	–	–	132	A	
V_{SD}	Diode Forward Voltage ②	IRF150 IRF151	–	–	2.5	V	T_C = 25°C, I_S = 40A, V_{GS} = 0V
		IRF152 IRF153	–	–	2.3	V	T_C = 25°C, I_S = 33A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	600	–	ns	T_J = 150°C, I_F = 40A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	3.3	–	μC	T_J = 150°C, I_F = 40A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

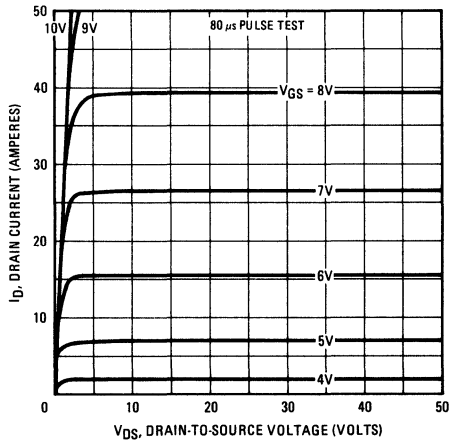


Fig. 1 — Typical Output Characteristics

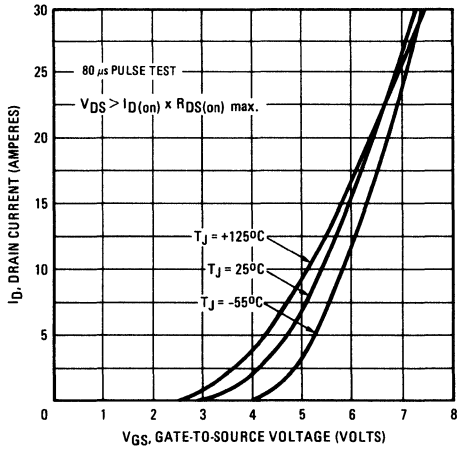


Fig. 2 — Typical Transfer Characteristics

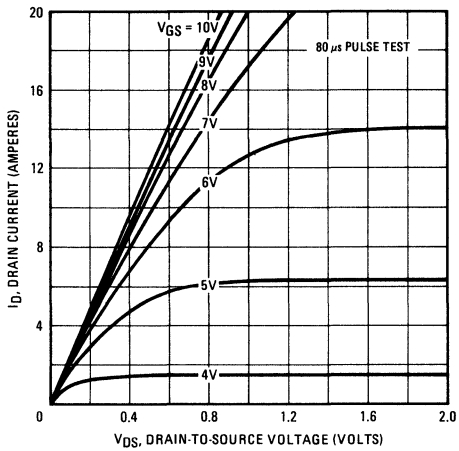


Fig. 3 — Typical Saturation Characteristics

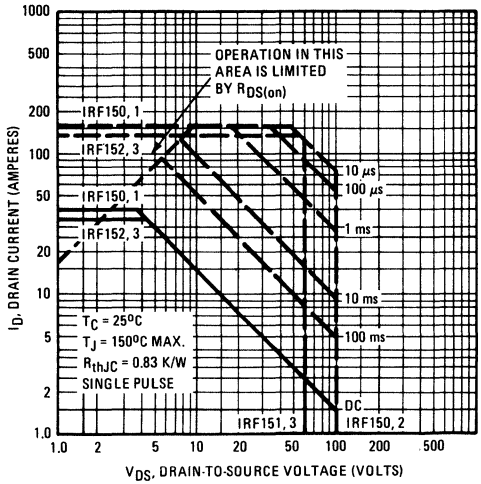


Fig. 4 — Maximum Safe Operating Area

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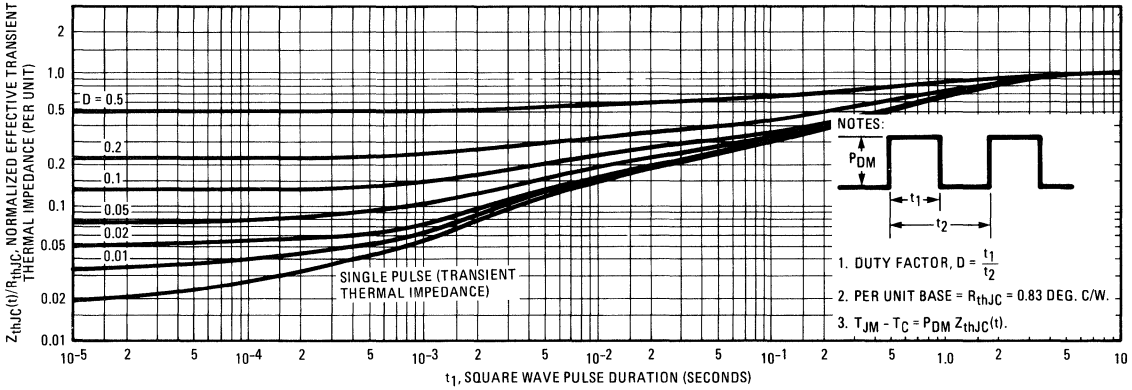


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

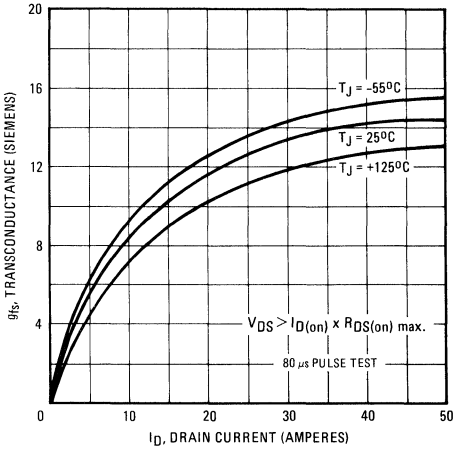


Fig. 6 — Typical Transconductance Vs. Drain Current

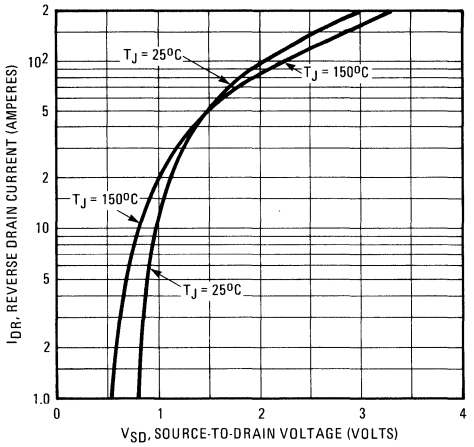


Fig. 7 — Typical Source-Drain Diode Forward Voltage

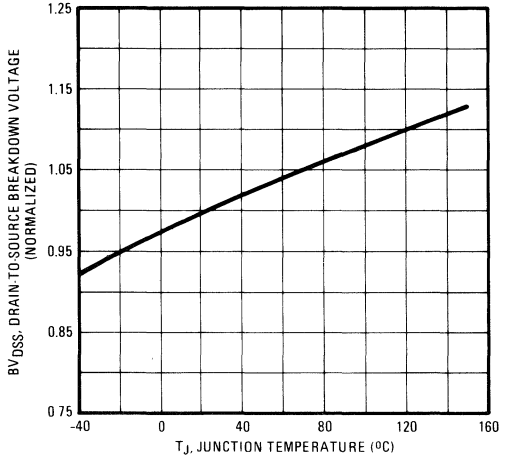


Fig. 8 — Breakdown Voltage Vs. Temperature

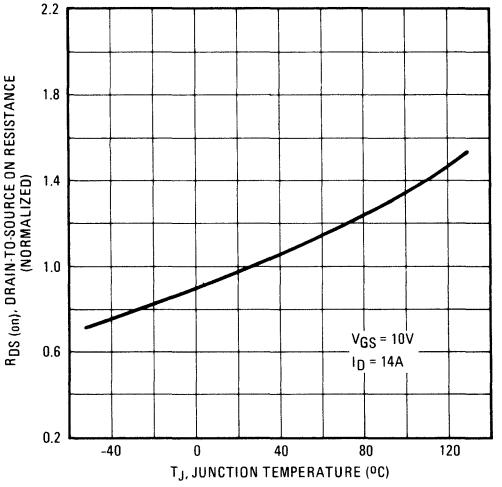


Fig. 9 — Normalized On-Resistance Vs. Temperature

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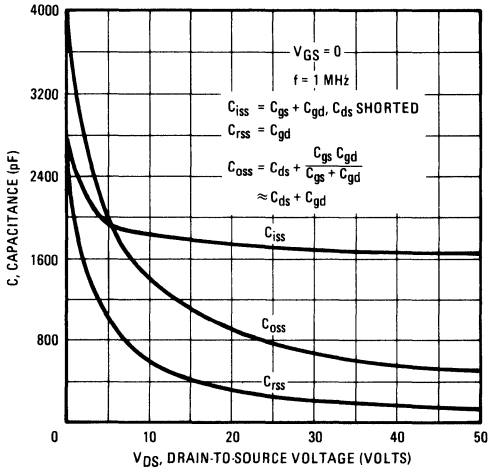


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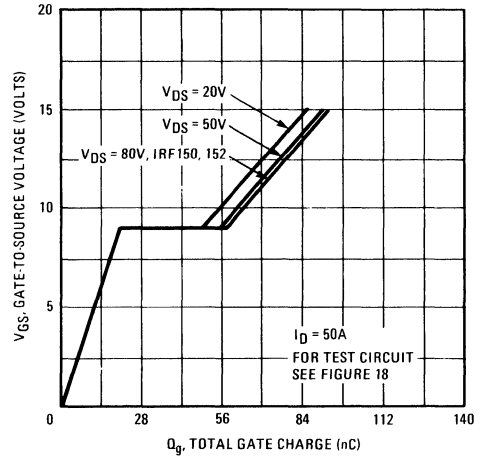


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

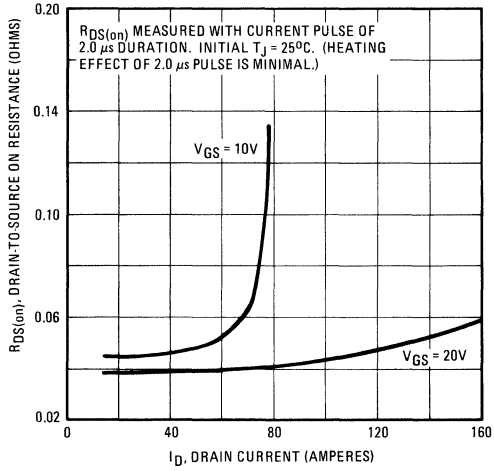


Fig. 12 — Typical On-Resistance Vs. Drain Current

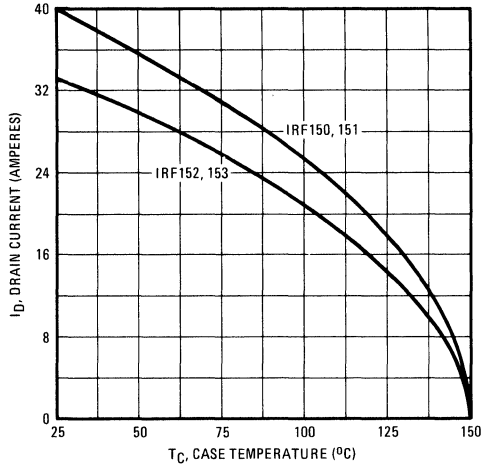


Fig. 13 — Maximum Drain Current Vs. Case Temperature

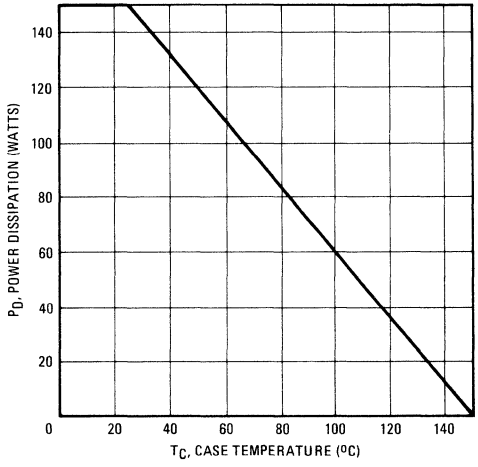


Fig. 14 — Power Vs. Temperature Derating Curve

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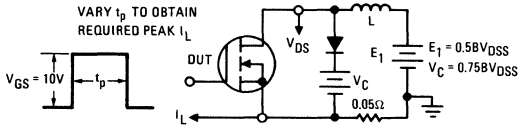


Fig. 15 — Clamped Inductive Test Circuit

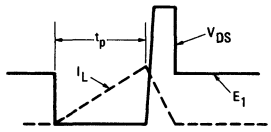


Fig. 16 — Clamped Inductive Waveforms

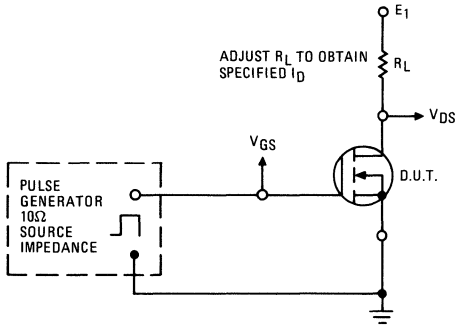


Fig. 17 — Switching Time Test Circuit

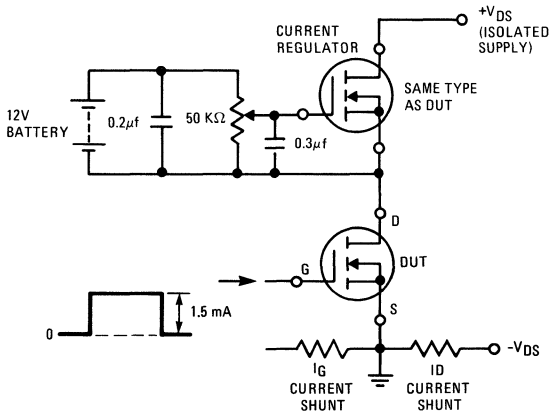
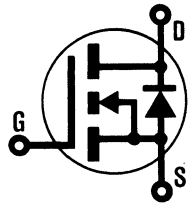


Fig. 18 — Gate Charge Test Circuit

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N-Channel

200 Volt, 0.8 Ohm HEXFET

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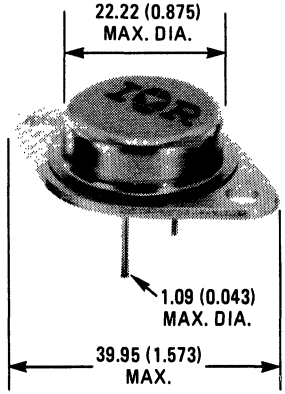
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- No Second Breakdown
- Excellent Temperature Stability

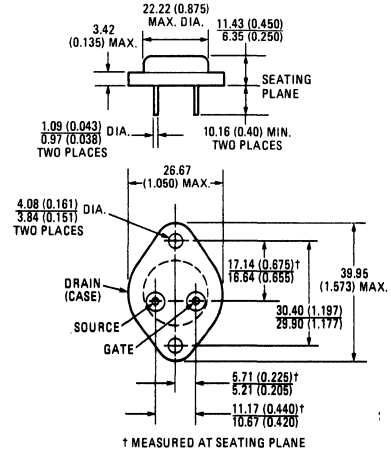
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF220	200V	0.8Ω	5.0A
IRF221	150V	0.8Ω	5.0A
IRF222	200V	1.2Ω	4.0A
IRF223	150V	1.2Ω	4.0A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Conforms to JEDEC Outline TO-204AA (TO-3)
Dimensions in Millimeters and (Inches)

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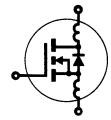
Absolute Maximum Ratings

Parameter		IRF220	IRF221	IRF222	IRF223	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	5.0	5.0	4.0	4.0	A
I_D @ T_C = 100°C	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_{DM}	Pulsed Drain Current ③	20	20	16	16	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		20	20	16	16	
T_J T_{stg}	Operating Junction and Storage Temperature Range	−50 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF220 IRF222	200	–	–	V	V_{GS} = 0V
		IRF221 IRF223	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF220 IRF221	5.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF222 IRF223	4.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF220 IRF221	–	0.5	0.8	Ω	V_{GS} = 10V, I_D = 2.5A
		IRF222 IRF223	–	0.8	1.2	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.3	2.5	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 2.5A
C_{iss}	Input Capacitance	ALL	–	450	600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	150	300	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	40	80	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 2.5A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	30	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	30	60	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	11	15	nC	V_{GS} = 10V, I_D = 6.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	5.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	6.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	3.12	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF220 IRF221	–	–	5.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF222 IRF223	–	–	4.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF220 IRF221	–	–	20	A	
		IRF222 IRF223	–	–	16	A	
V_{SD}	Diode Forward Voltage ②	IRF220 IRF221	–	–	2.0	V	T_C = 25°C, I_S = 5.0A, V_{GS} = 0V
		IRF222 IRF223	–	–	1.8	V	T_C = 25°C, I_S = 4.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	350	–	ns	T_J = 150°C, I_F = 5.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	2.3	–	μC	T_J = 150°C, I_F = 5.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

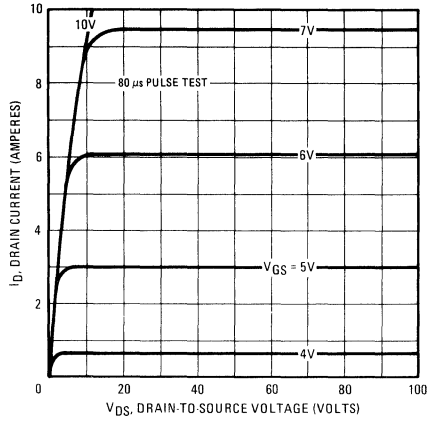


Fig. 1 – Typical Output Characteristics

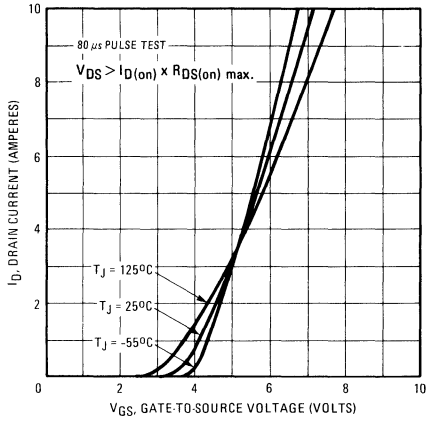


Fig. 2 – Typical Transfer Characteristics

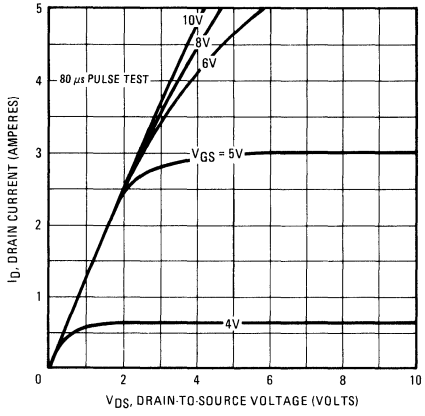


Fig. 3 – Typical Saturation Characteristics

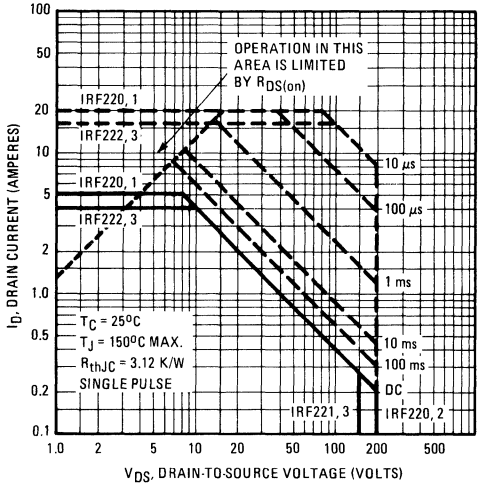


Fig. 4 – Maximum Safe Operating Area

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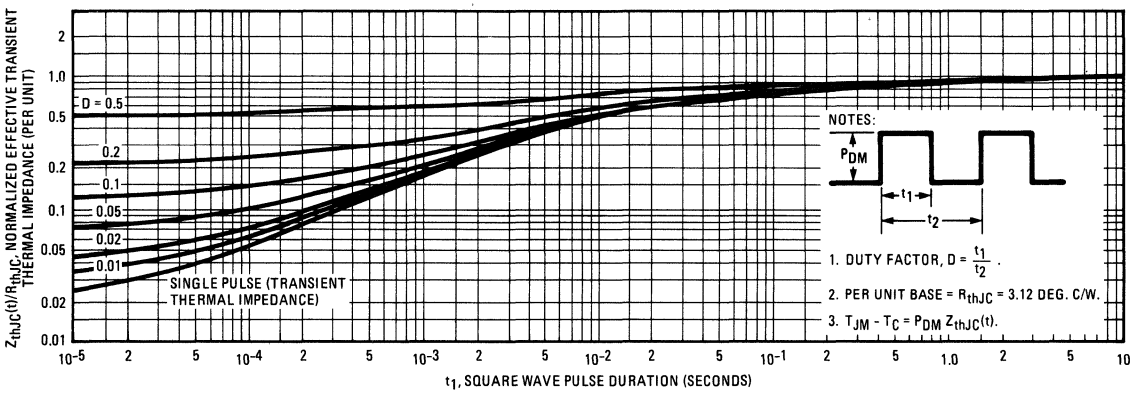


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

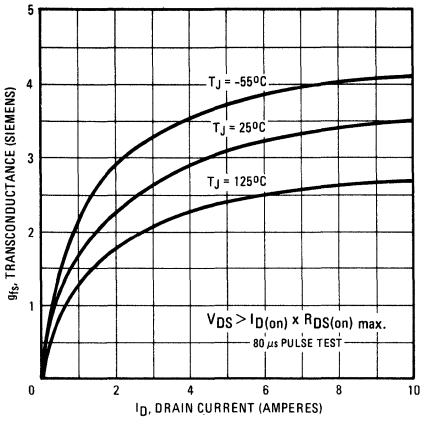


Fig. 6 — Typical Transconductance Vs. Drain Current

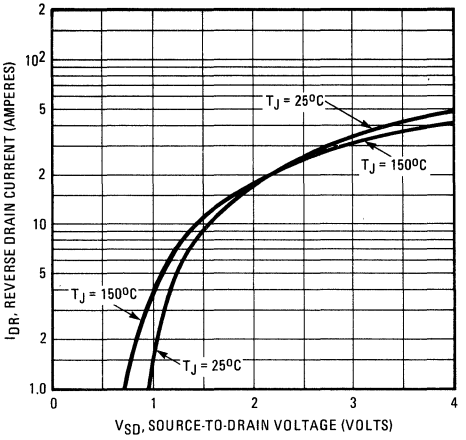


Fig. 7 — Typical Source-Drain Diode Forward Voltage

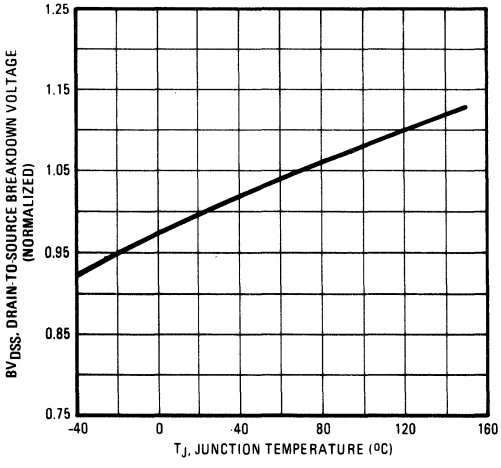


Fig. 8 — Breakdown Voltage Vs. Temperature

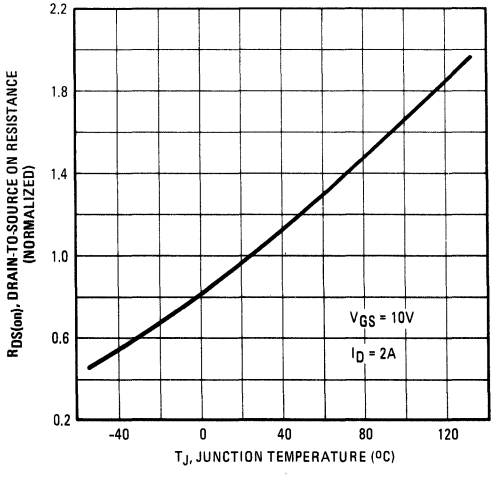


Fig. 9 — Normalized On-Resistance Vs. Temperature

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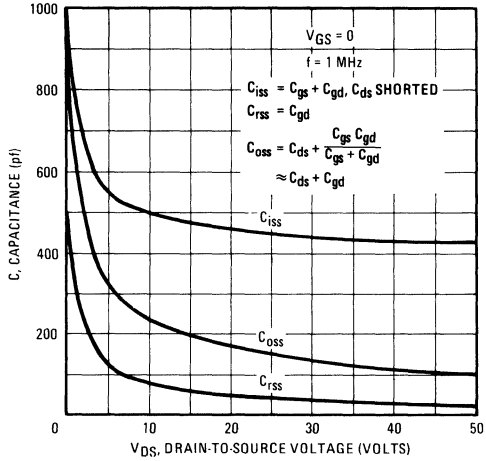


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

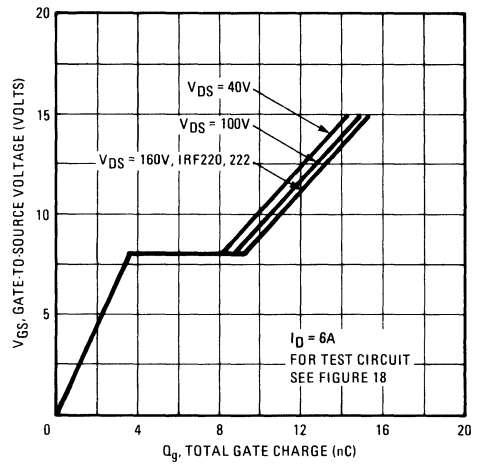


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

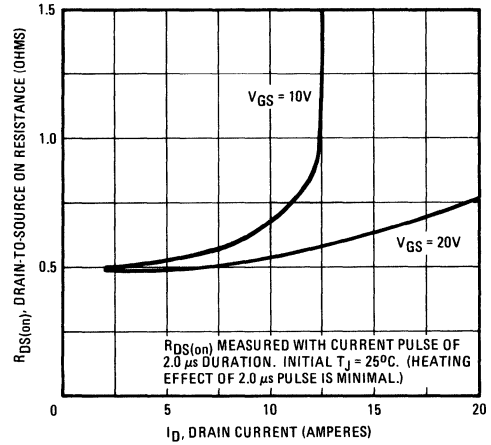


Fig. 12 — Typical On-Resistance Vs. Drain Current

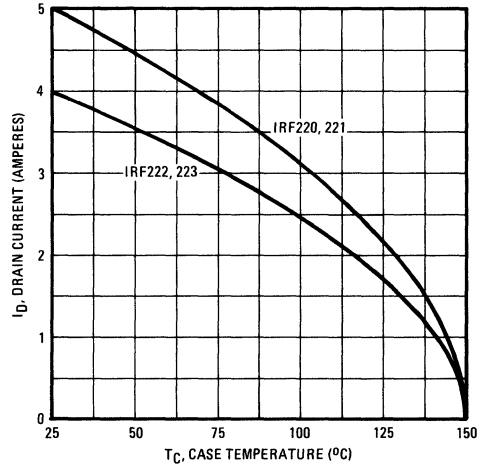


Fig. 13 — Maximum Drain Current Vs. Case Temperature

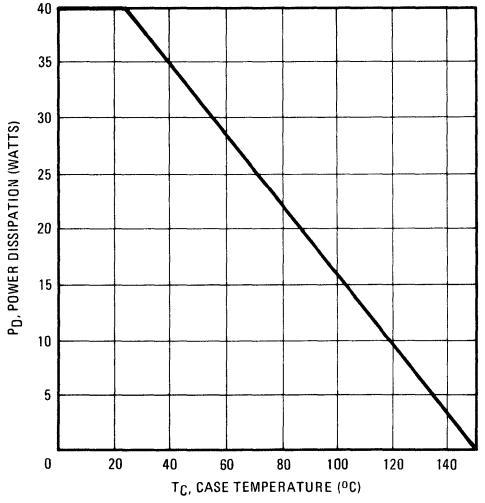


Fig. 14 — Power Vs. Temperature Derating Curve

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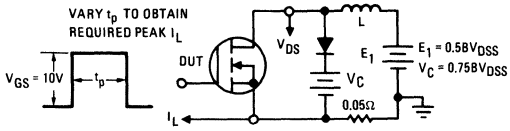


Fig. 15 — Clamped Inductive Test Circuit

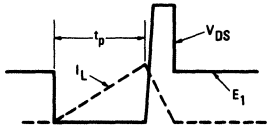


Fig. 16 — Clamped Inductive Waveforms

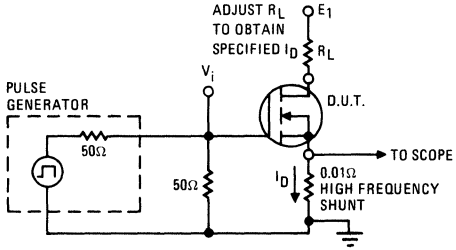


Fig. 17 — Switching Time Test Circuit

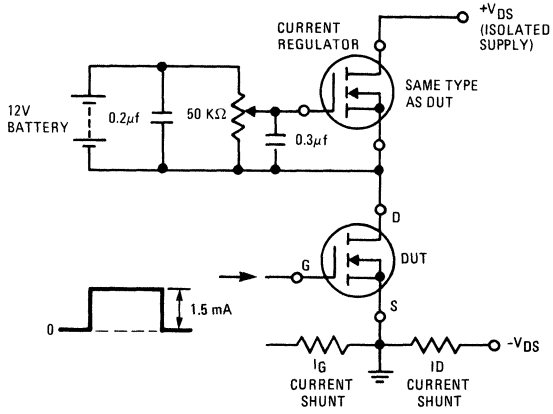
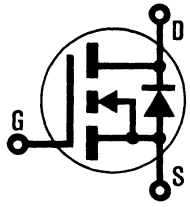


Fig. 18 — Gate Charge Test Circuit

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS IRF230 IRF231 IRF232 IRF233



N-Channel

200 Volt, 0.4 Ohm HEXFET

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

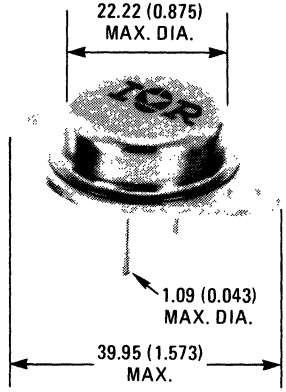
Features:

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

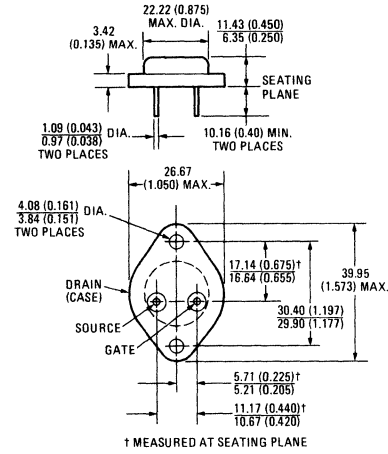
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF230	200V	0.4Ω	9.0A
IRF231	150V	0.4Ω	9.0A
IRF232	200V	0.6Ω	8.0A
IRF233	150V	0.6Ω	8.0A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Conforms to JEDEC Outline TO-204AA (TO-3)
Dimensions in Millimeters and (Inches)

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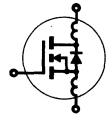
Absolute Maximum Ratings

Parameter		IRF230	IRF231	IRF232	IRF233	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	9.0	9.0	8.0	8.0	A
I_D @ T_C = 100°C	Continuous Drain Current	6.0	6.0	5.0	5.0	A
I_{DM}	Pulsed Drain Current ③	36	36	32	32	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		36	36	32	32	
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF230 IRF232	200	–	–	V	V_{GS} = 0V
		IRF231 IRF233	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	−100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF230 IRF231	9.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF232 IRF233	8.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF230 IRF231	–	0.25	0.4	Ω	V_{GS} = 10V, I_D = 5.0A
		IRF232 IRF233	–	0.4	0.6	Ω	
g_{fs}	Forward Transconductance ②	ALL	3.0	4.8	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 5.0A
C_{iss}	Input Capacitance	ALL	–	600	800	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	250	450	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	80	150	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} ≈ 90V, I_D = 5.0A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	50	ns	
t_f	Fall Time	ALL	–	–	40	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	19	30	nC	V_{GS} = 10V, I_D = 12A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	10	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	9.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF230 IRF231	–	–	9.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF232 IRF233	–	–	8.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF230 IRF231	–	–	36	A	
		IRF232 IRF233	–	–	32	A	
V_{SD}	Diode Forward Voltage ②	IRF230 IRF231	–	–	2.0	V	T_C = 25°C, I_S = 9.0A, V_{GS} = 0V
		IRF232 IRF233	–	–	1.8	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	450	–	ns	T_J = 150°C, I_F = 9.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	3.0	–	μC	T_J = 150°C, I_F = 9.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

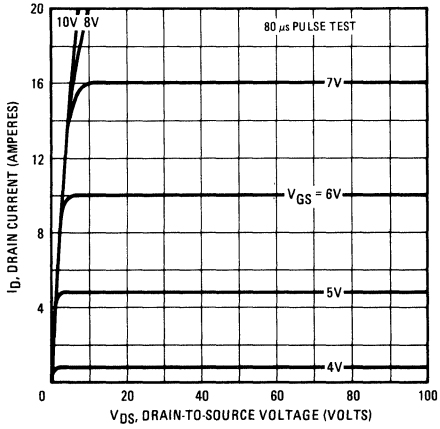


Fig. 1 — Typical Output Characteristics

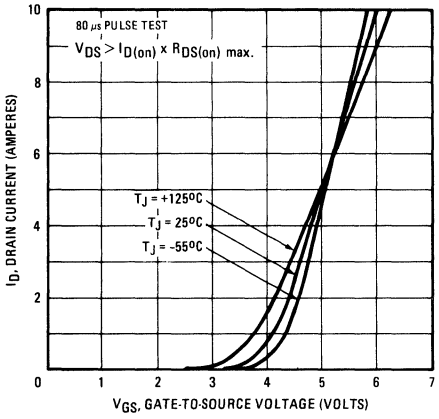


Fig. 2 — Typical Transfer Characteristics

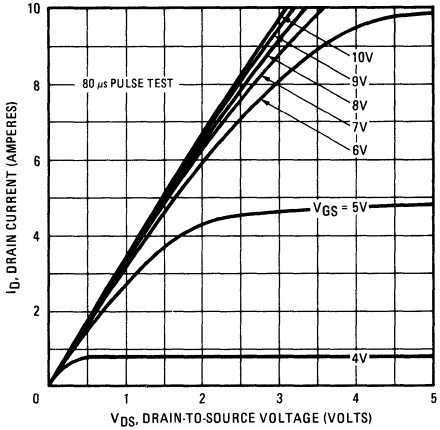


Fig. 3 — Typical Saturation Characteristics

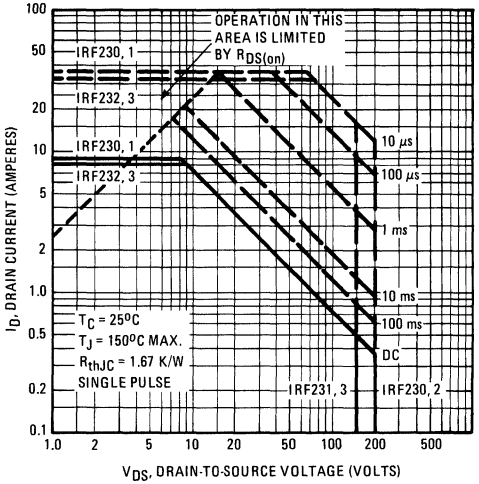


Fig. 4 — Maximum Safe Operating Area

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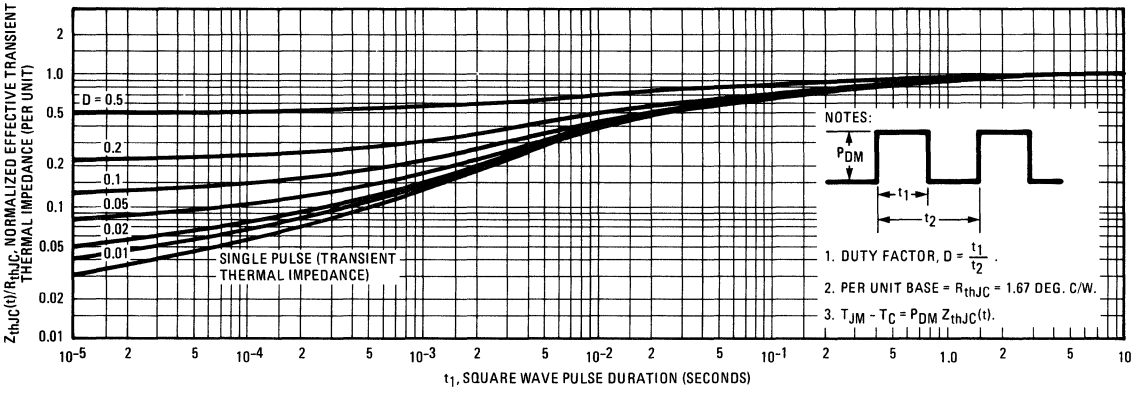


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

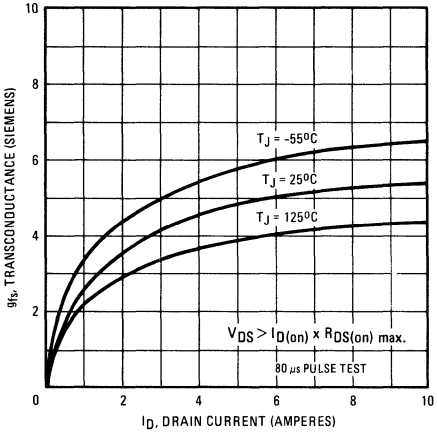


Fig. 6 — Typical Transconductance Vs. Drain Current

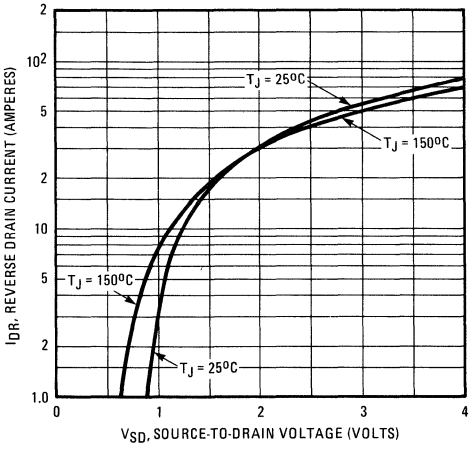


Fig. 7 — Typical Source-Drain Diode Forward Voltage

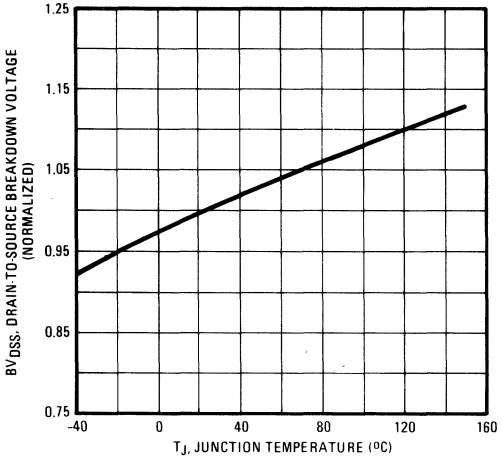


Fig. 8 — Breakdown Voltage Vs. Temperature

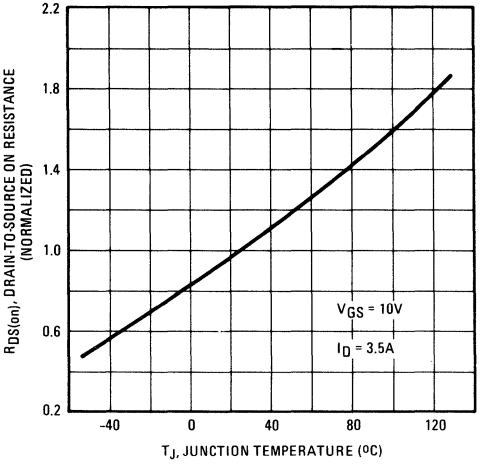


Fig. 9 — Normalized On-Resistance Vs. Temperature

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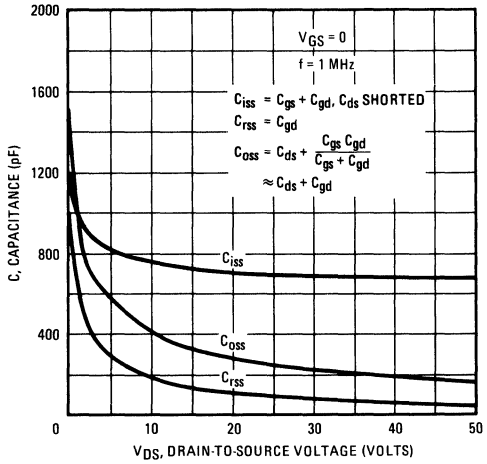


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

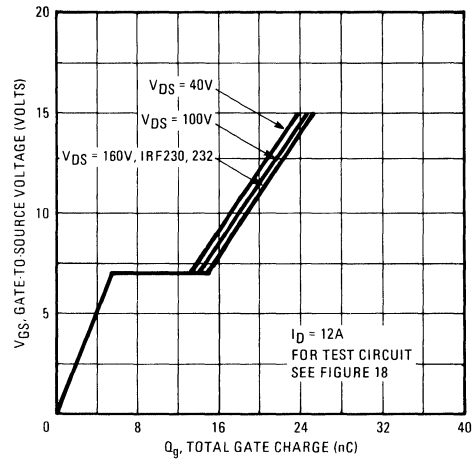


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

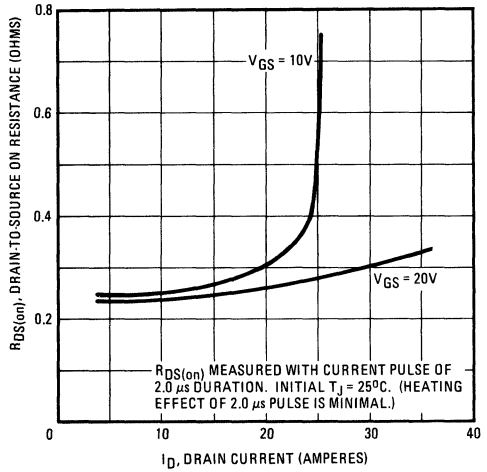


Fig. 12 — Typical On-Resistance Vs. Drain Current

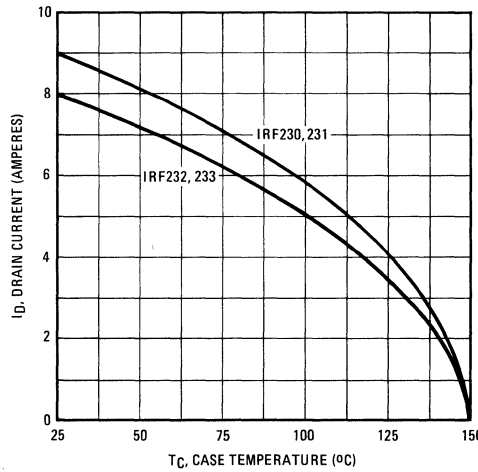


Fig. 13 — Maximum Drain Current Vs. Case Temperature

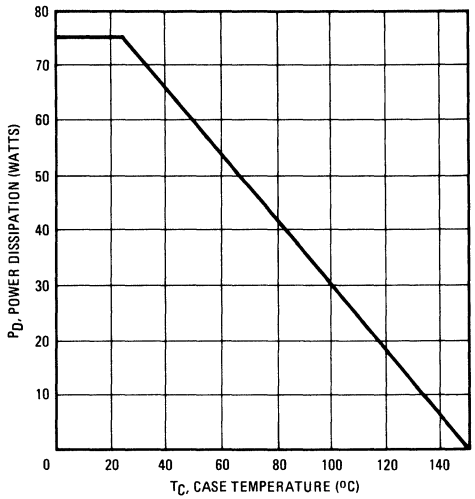


Fig. 14 — Power Vs. Temperature Derating Curve

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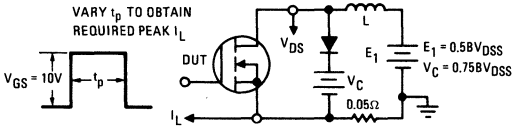


Fig. 15 — Clamped Inductive Test Circuit

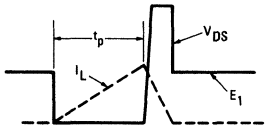


Fig. 16 — Clamped Inductive Waveforms

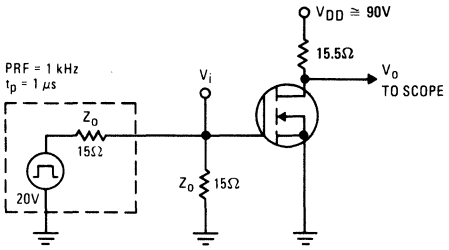


Fig. 17 — Switching Time Test Circuit

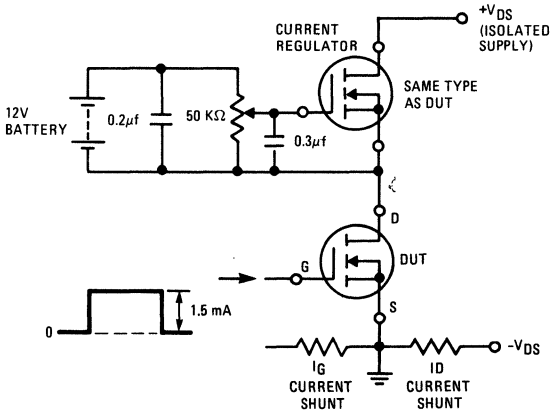


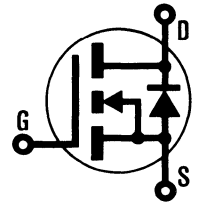
Fig. 18 — Gate Charge Test Circuit

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS IRF240 IRF241 IRF242 IRF243

N-CHANNEL POWER MOSFETs



200 Volt, 0.2 Ohm HEXFET

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

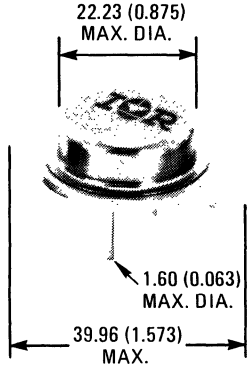
Features:

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

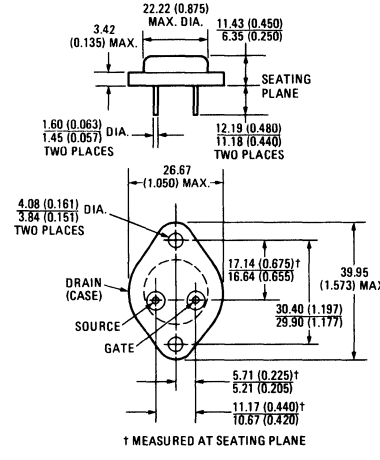
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF240	200V	0.18Ω	18A
IRF241	150V	0.18Ω	18A
IRF242	200V	0.22Ω	16A
IRF243	150V	0.22Ω	16A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



† MEASURED AT SEATING PLANE

Conforms to JEDEC Outline TO-204AA (TO-3)
Dimensions in Millimeters and (Inches)

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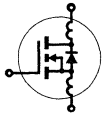
Absolute Maximum Ratings

Parameter		IRF240	IRF241	IRF242	IRF243	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	18	18	16	16	A
I_D @ T_C = 100°C	Continuous Drain Current	11	11	10	10	A
I_{DM}	Pulsed Drain Current ③	72	72	64	64	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		72	72	64	64	
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF240 IRF242	200	–	–	V	V_{GS} = 0V
		IRF241 IRF243	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF240 IRF241	18	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		IRF242 IRF243	16	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF240 IRF241	–	0.14	0.18	Ω	V_{GS} = 10V, I_D = 10A
		IRF242 IRF243	–	0.20	0.22	Ω	
g_{fs}	Forward Transconductance ②	ALL	6.0	9.0	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 10A
C_{iss}	Input Capacitance	ALL	–	1275	1600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	500	750	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	160	300	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	16	30	ns	V_{DD} ≈ 75V, I_D = 10A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	27	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	40	80	ns	
t_f	Fall Time	ALL	–	31	60	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	43	60	nC	V_{GS} = 10V, I_D = 22A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	16	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	27	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.0	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF240 IRF241	–	–	18	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF242 IRF243	–	–	16	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF240 IRF241	–	–	72	A	
		IRF242 IRF243	–	–	64	A	
V_{SD}	Diode Forward Voltage ②	IRF240 IRF241	–	–	2.0	V	T_C = 25°C, I_S = 18A, V_{GS} = 0V
		IRF242 IRF243	–	–	1.9	V	T_C = 25°C, I_S = 16A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	650	–	ns	T_J = 150°C, I_F = 18A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.1	–	μC	T_J = 150°C, I_F = 18A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

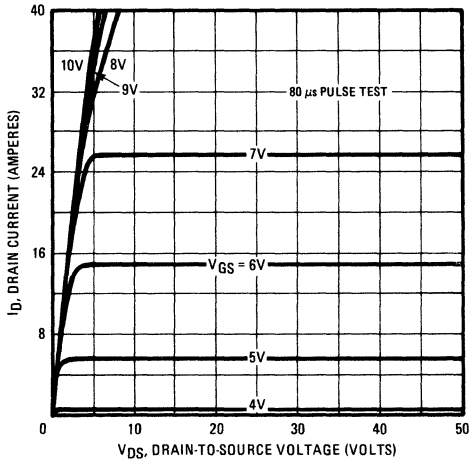


Fig. 1 — Typical Output Characteristics

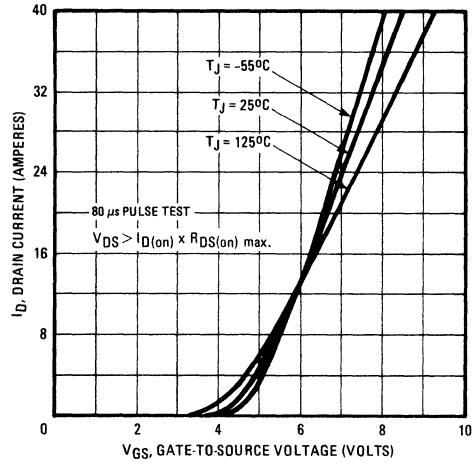


Fig. 2 — Typical Transfer Characteristics

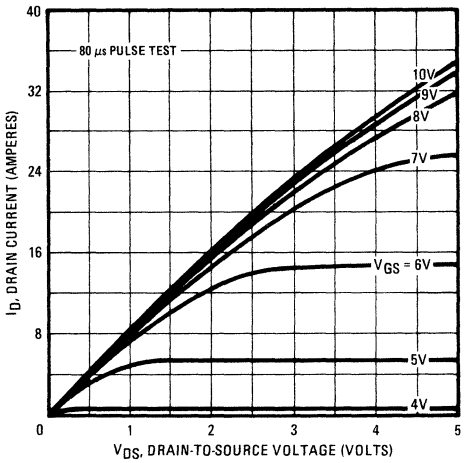


Fig. 3 — Typical Saturation Characteristics

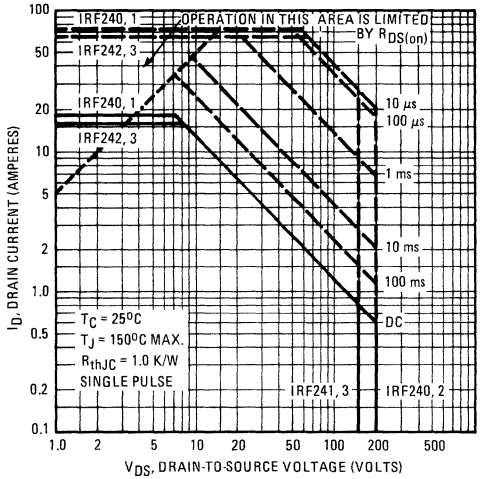


Fig. 4 — Maximum Safe Operating Area

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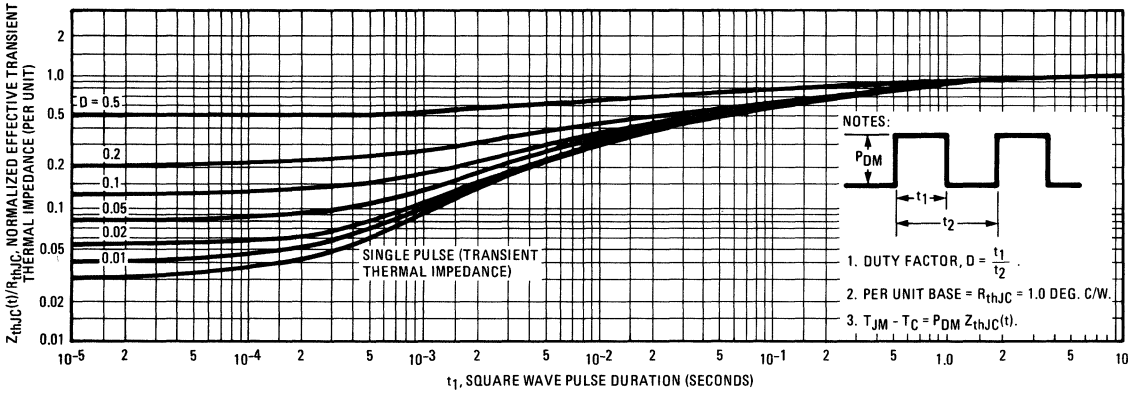


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

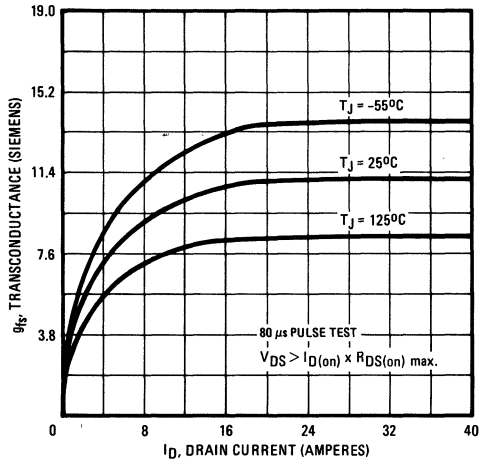


Fig. 6 — Typical Transconductance Vs. Drain Current

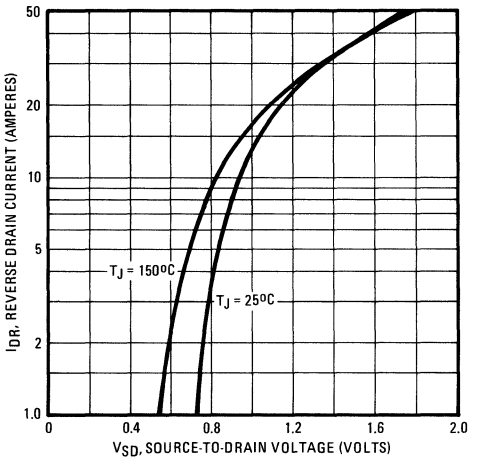


Fig. 7 — Typical Source-Drain Diode Forward Voltage

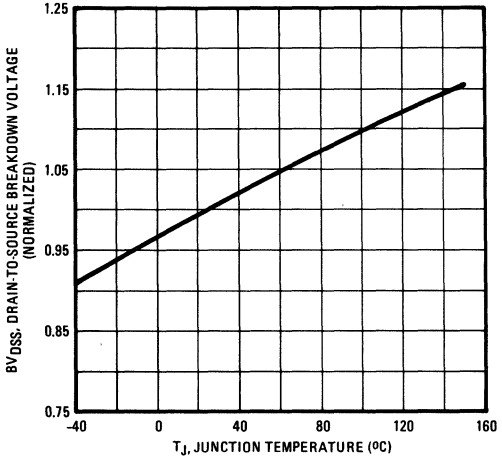


Fig. 8 — Breakdown Voltage Vs. Temperature

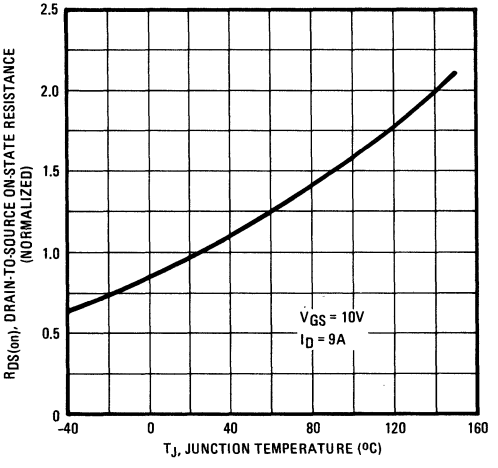


Fig. 9 — Normalized On-Resistance Vs. Temperature

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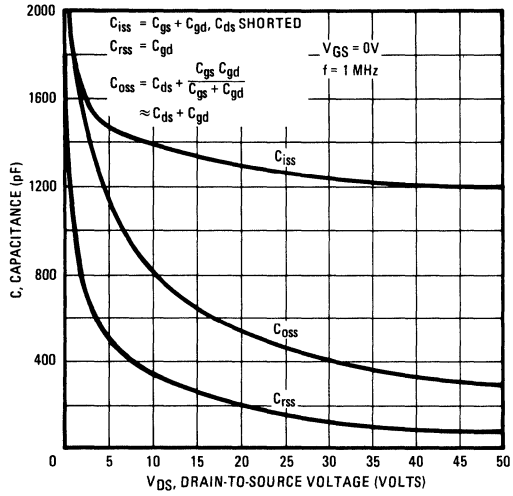


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

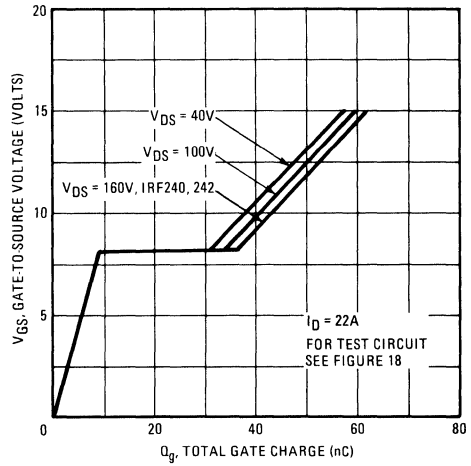


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

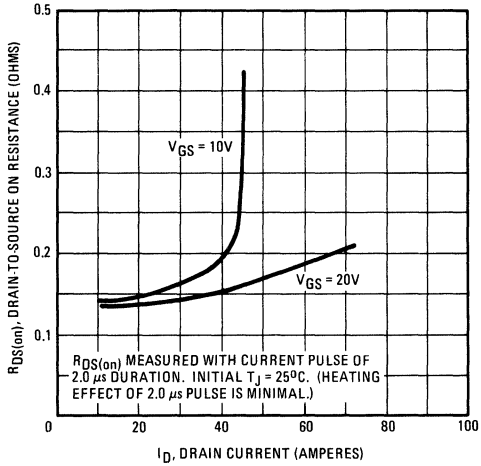


Fig. 12 — Typical On-Resistance Vs. Drain Current

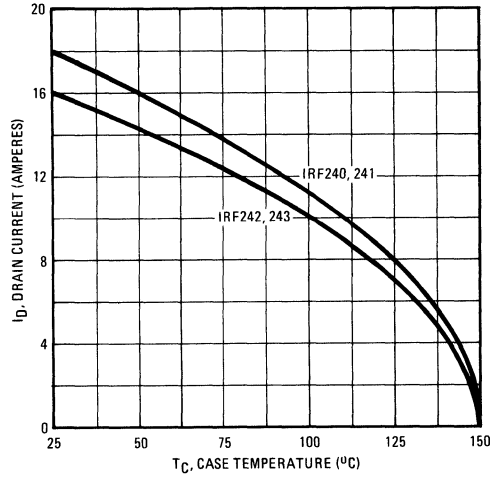


Fig. 13 — Maximum Drain Current Vs. Case Temperature

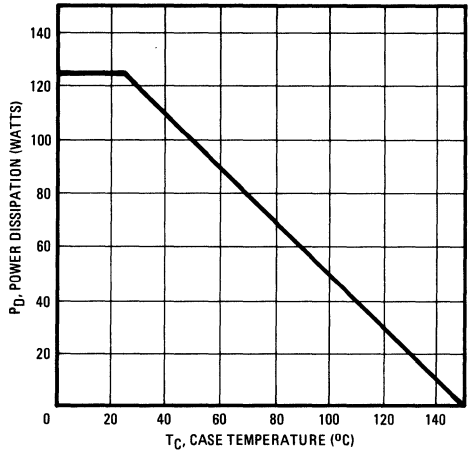


Fig. 14 — Power Vs. Temperature Derating Curve

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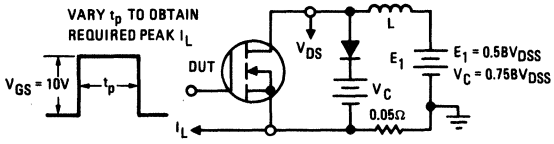


Fig. 15 – Clamped Inductive Test Circuit

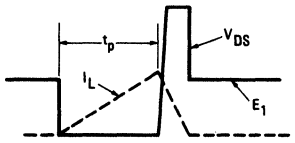


Fig. 16 – Clamped Inductive Waveforms

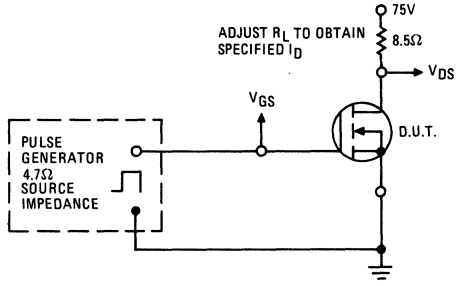


Fig. 17 – Switching Time Test Circuit

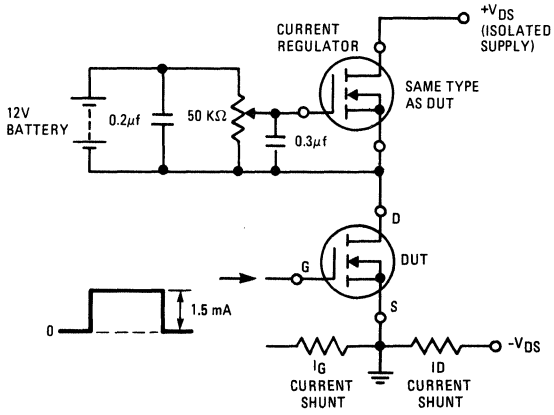


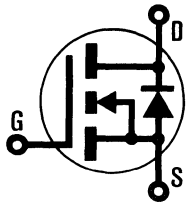
Fig. 18 – Gate Charge Test Circuit

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS

IRF250
IRF251
IRF252
IRF253



N-Channel

200 Volt, 0.085 Ohm HEXFET

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

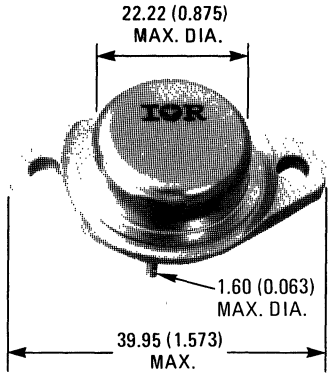
Features:

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

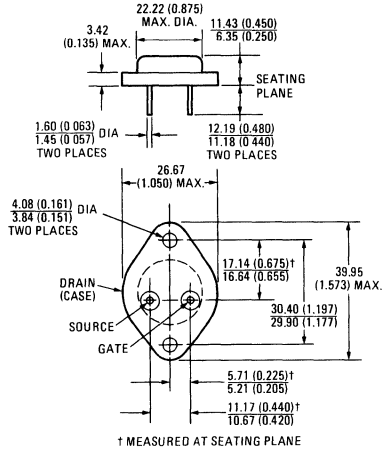
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF250	200V	0.085Ω	30A
IRF251	150V	0.085Ω	30A
IRF252	200V	0.120Ω	25A
IRF253	150V	0.120Ω	25A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Conforms to JEDEC Outline TO-204AE (Modified TO-3)
Dimensions in Millimeters and (Inches)

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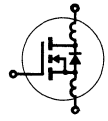
Absolute Maximum Ratings

Parameter		IRF250	IRF251	IRF252	IRF253	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	30	30	25	25	A
I_D @ T_C = 100°C	Continuous Drain Current	19	19	16	16	A
I_{DM}	Pulsed Drain Current ③	120	120	100	100	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	150 (See Fig. 14)				W
	Linear Derating Factor	1.2 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 120	120	100	100	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF250 IRF252	200	–	–	V	V_{GS} = 0V
		IRF251 IRF253	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF250 IRF251	30	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF252 IRF253	25	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF250 IRF251	–	0.07	0.085	Ω	V_{GS} = 10V, I_D = 16A
		IRF252 IRF253	–	0.09	0.120	Ω	
g_{fs}	Forward Transconductance ②	ALL	8.0	14	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 16A
C_{iss}	Input Capacitance	ALL	–	2000	3000	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	800	1200	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	300	500	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	35	ns	V_{DD} ≅ 95V, I_D = 16A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	100	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	125	ns	
t_f	Fall Time	ALL	–	–	100	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	79	120	nC	V_{GS} = 10V, I_D = 38A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	37	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	42	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	0.83	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF250 IRF251	–	–	30	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF252 IRF253	–	–	25	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF250 IRF251	–	–	120	A	
		IRF252 IRF253	–	–	100	A	
V_{SD}	Diode Forward Voltage ②	IRF250 IRF251	–	–	2.0	V	T_C = 25°C, I_S = 30A, V_{GS} = 0V
		IRF252 IRF253	–	–	1.8	V	T_C = 25°C, I_S = 25A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	750	–	ns	T_J = 150°C, I_F = 30A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.7	–	μC	T_J = 150°C, I_F = 30A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

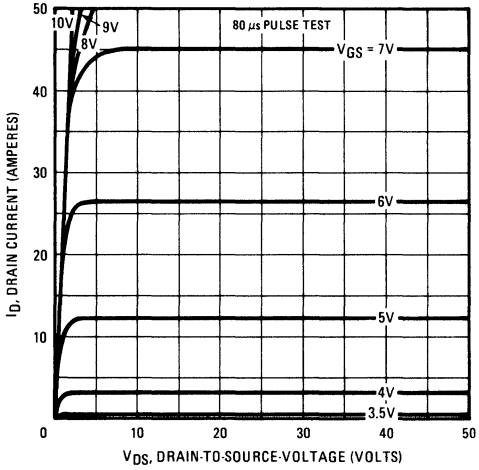


Fig. 1 — Typical Output Characteristics

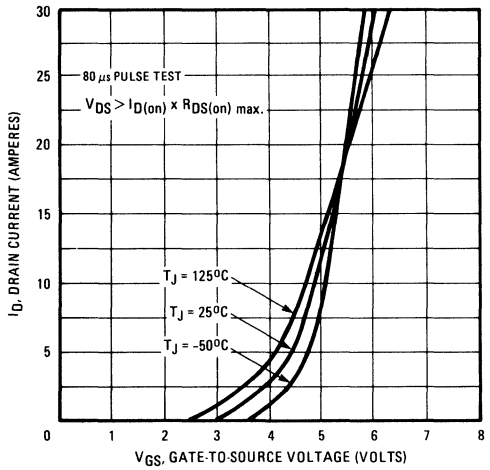


Fig. 2 — Typical Transfer Characteristics

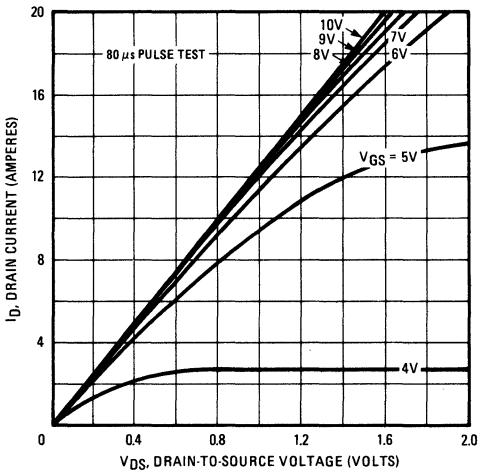


Fig. 3 — Typical Saturation Characteristics

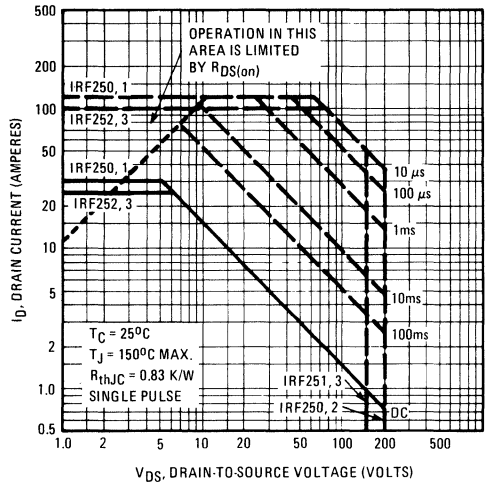


Fig. 4 — Maximum Safe Operating Area

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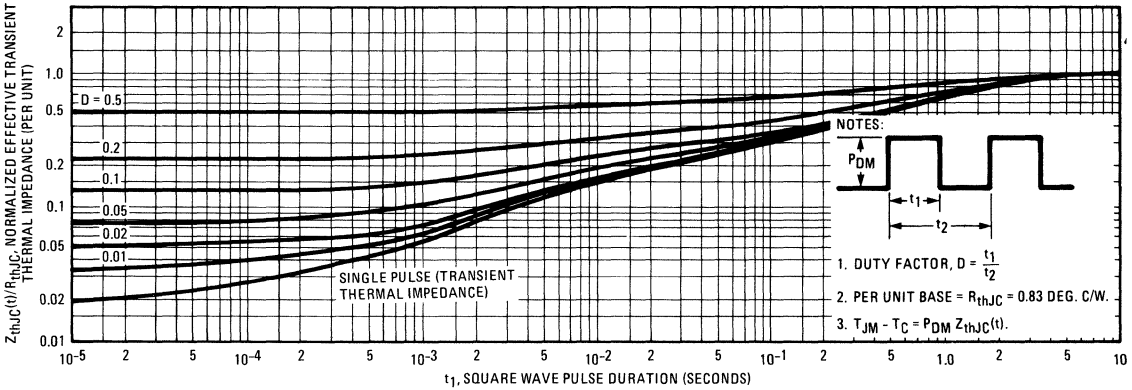


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

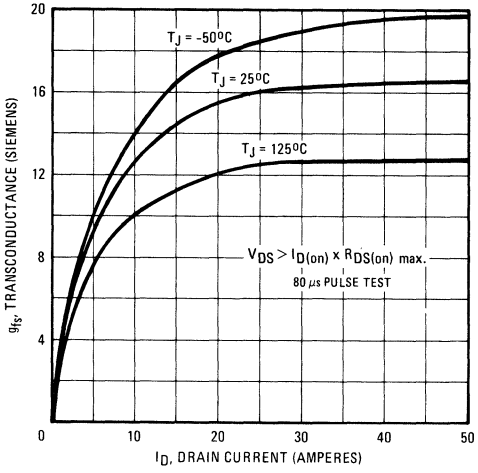


Fig. 6 — Typical Transconductance Vs. Drain Current

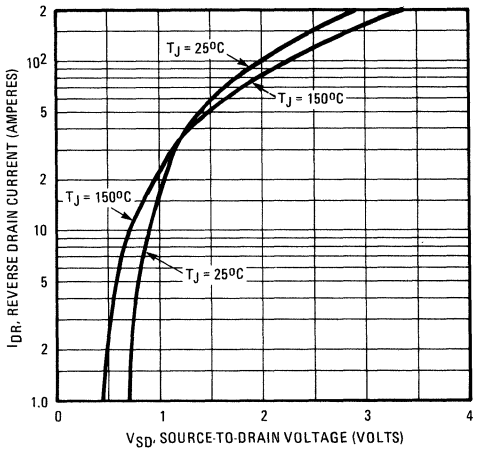


Fig. 7 — Typical Source-Drain Diode Forward Voltage

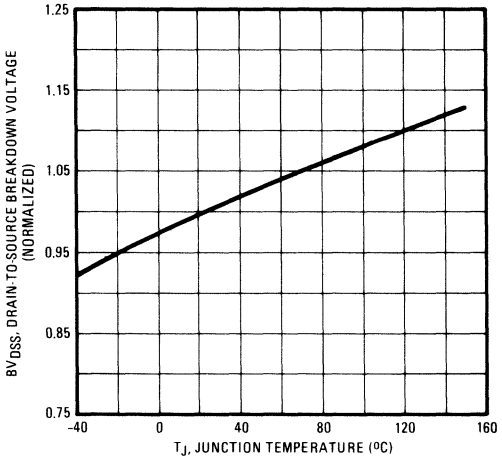


Fig. 8 — Breakdown Voltage Vs. Temperature

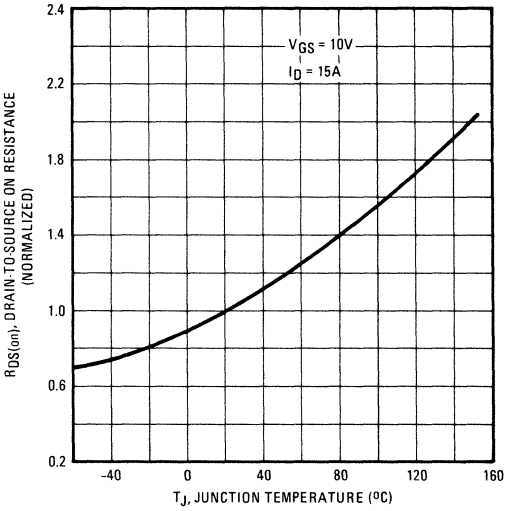


Fig. 9 — Normalized On-Resistance Vs. Temperature

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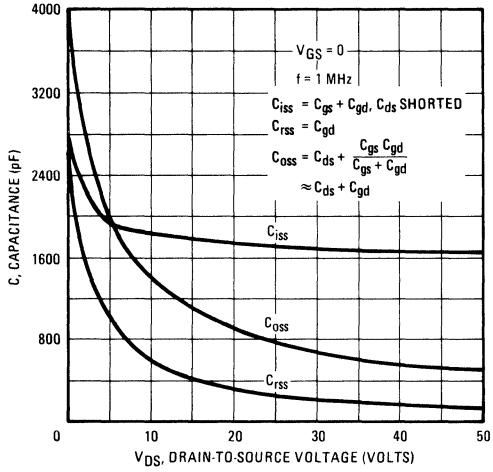


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

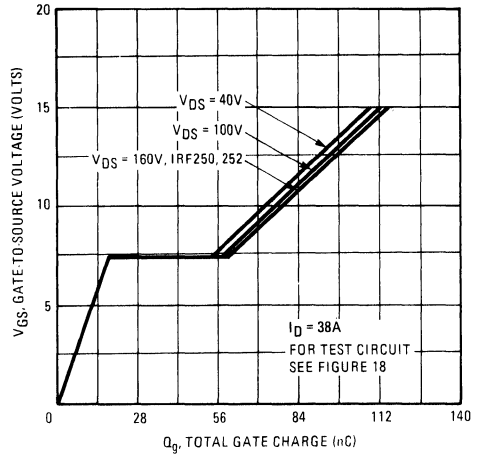


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

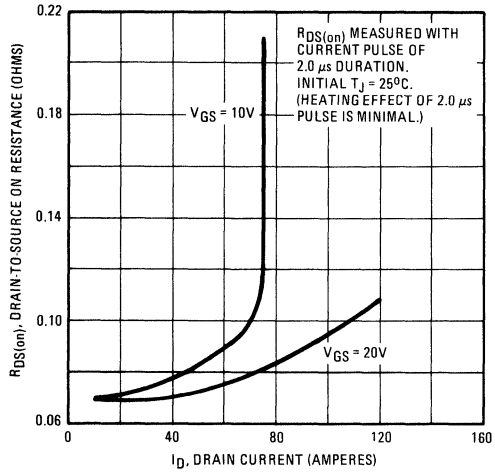


Fig. 12 — Typical On-Resistance Vs. Drain Current

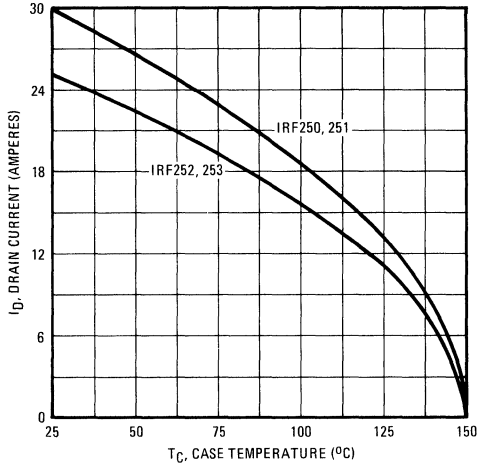


Fig. 13 — Maximum Drain Current Vs. Case Temperature

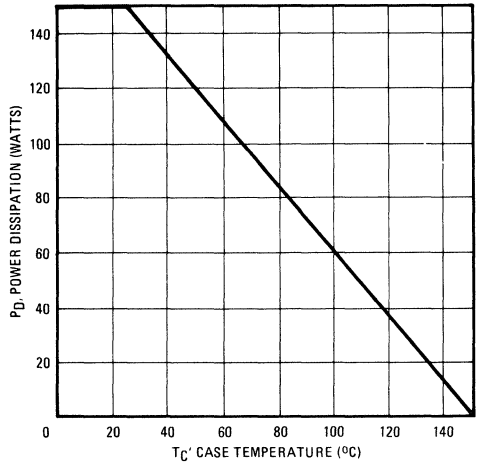


Fig. 14 — Power Vs. Temperature Derating Curve

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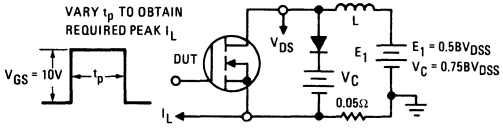


Fig. 15 – Clamped Inductive Test Circuit

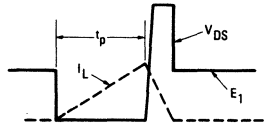


Fig. 16 – Clamped Inductive Waveforms

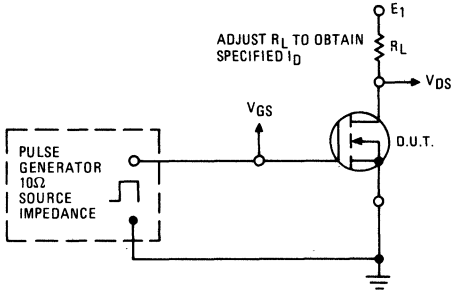


Fig. 17 – Switching Time Test Circuit

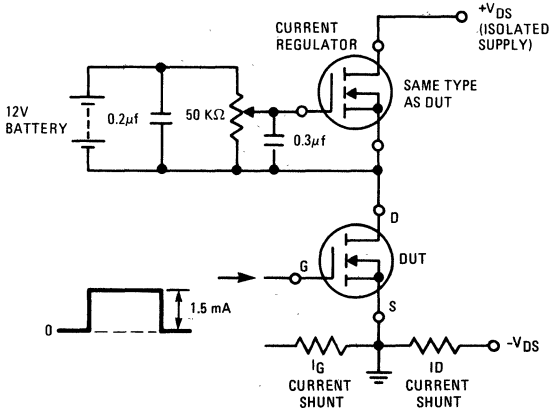


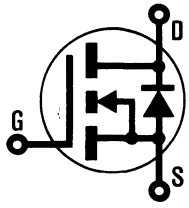
Fig. 18 – Gate Charge Test Circuit

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS

IRF320
IRF321
IRF322
IRF323



N-Channel

400 Volt, 1.8 Ohm HEXFET

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

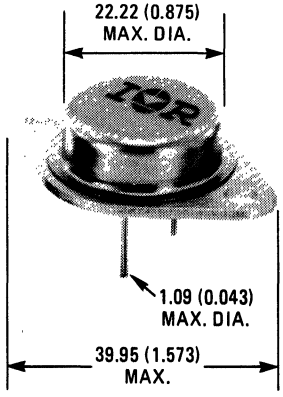
Features:

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

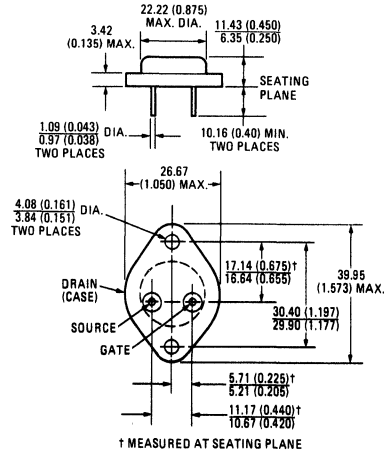
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF320	400V	1.8Ω	3.0A
IRF321	350V	1.8Ω	3.0A
IRF322	400V	2.5Ω	2.5A
IRF323	350V	2.5Ω	2.5A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



† MEASURED AT SEATING PLANE

Conforms to JEDEC Outline TO-204AA (TO-3)
Dimensions in Millimeters and (Inches)

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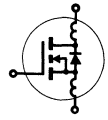
Absolute Maximum Ratings

Parameter		IRF320	IRF321	IRF322	IRF323	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_D @ T_C = 100°C	Continuous Drain Current	2.0	2.0	1.5	1.5	A
I_{DM}	Pulsed Drain Current ③	12	12	10	10	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		12	12	10	10	
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF320 IRF322	400	—	—	V	V_{GS} = 0V
		IRF321 IRF323	350	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF320 IRF321	3.0	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		IRF322 IRF323	2.5	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF320 IRF321	—	1.5	1.8	Ω	V_{GS} = 10V, I_D = 1.5A
		IRF322 IRF323	—	1.8	2.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	2.0	—	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 1.5A
C_{iss}	Input Capacitance	ALL	—	450	600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	100	200	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	20	40	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	20	40	ns	$V_{DD} \approx 0.5\ BV_{DSS}$, I_D = 1.5A, Z_0 = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	25	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	50	100	ns	
t_f	Fall Time	ALL	—	25	50	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	12	15	nC	V_{GS} = 10V, I_D = 4.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	6.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	6.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	3.12	K/W	
R_{thCS}	Case-to-Sink	ALL	—	0.1	—	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF320 IRF321	—	—	3.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF322 IRF323	—	—	2.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF320 IRF321	—	—	12	A	
		IRF322 IRF323	—	—	10	A	
V_{SD}	Diode Forward Voltage ②	IRF320 IRF321	—	—	1.6	V	T_C = 25°C, I_S = 3.0A, V_{GS} = 0V
		IRF322 IRF323	—	—	1.5	V	T_C = 25°C, I_S = 2.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	450	—	ns	T_J = 150°C, I_F = 3.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	3.1	—	μC	T_J = 150°C, I_F = 3.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2% ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

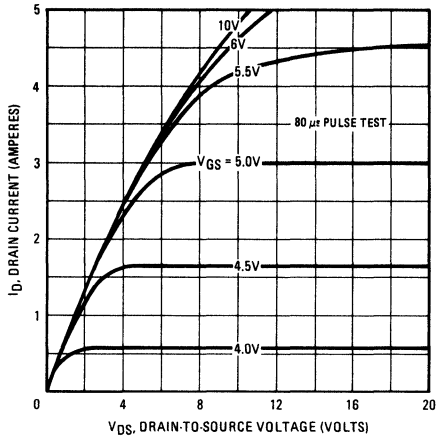


Fig. 1 — Typical Output Characteristics

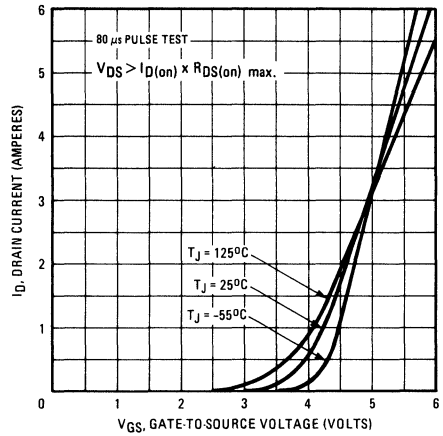


Fig. 2 — Typical Transfer Characteristics

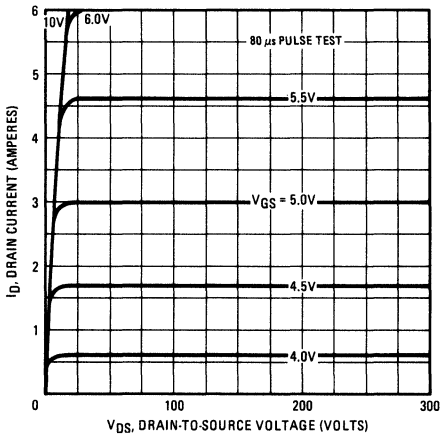


Fig. 3 — Typical Saturation Characteristics

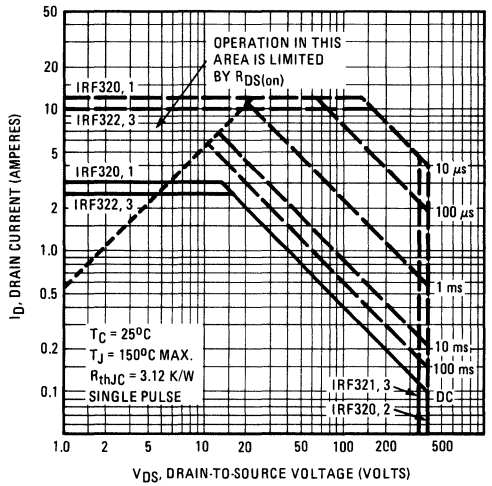


Fig. 4 — Maximum Safe Operating Area

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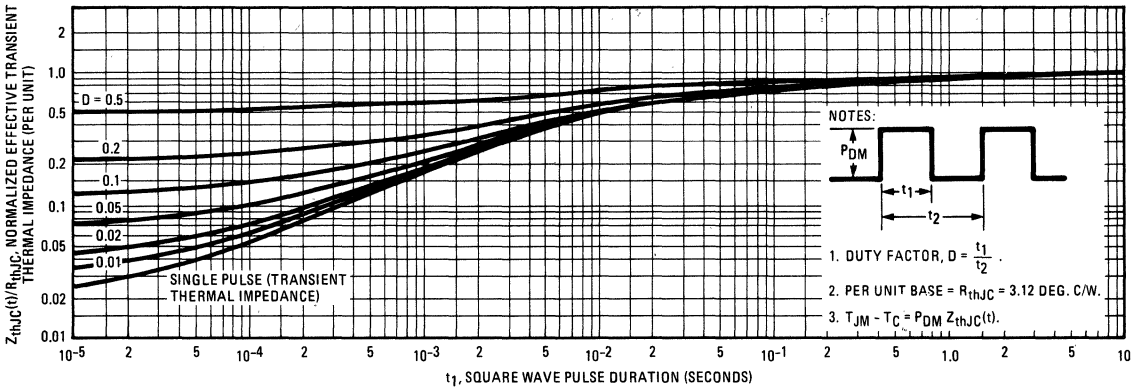


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

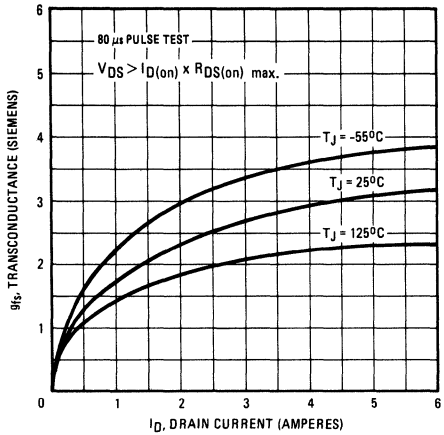


Fig. 6 — Typical Transconductance Vs. Drain Current

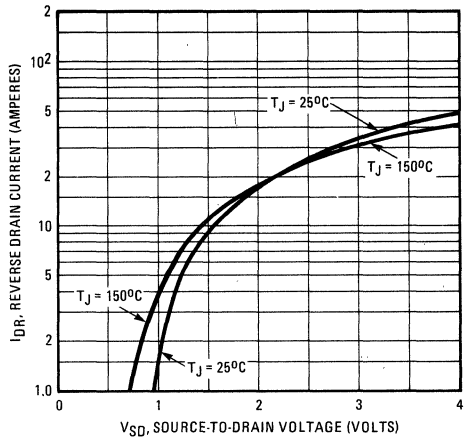


Fig. 7 — Typical Source-Drain Diode Forward Voltage

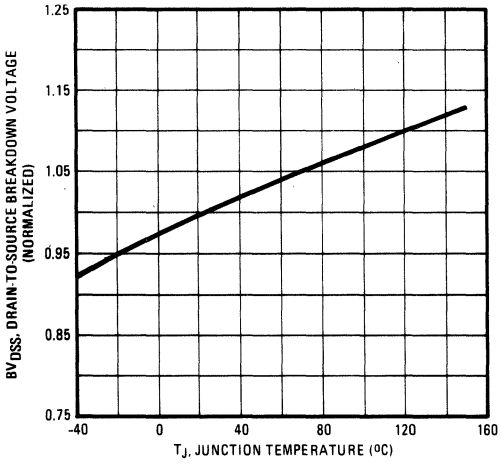


Fig. 8 — Breakdown Voltage Vs. Temperature

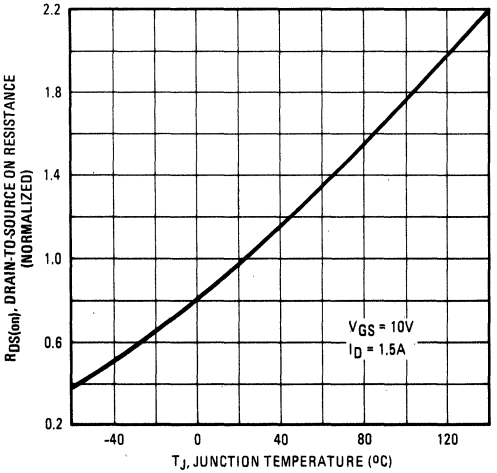


Fig. 9 — Normalized On-Resistance Vs. Temperature

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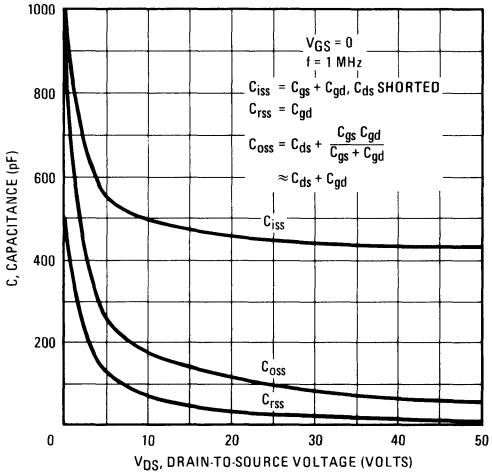


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

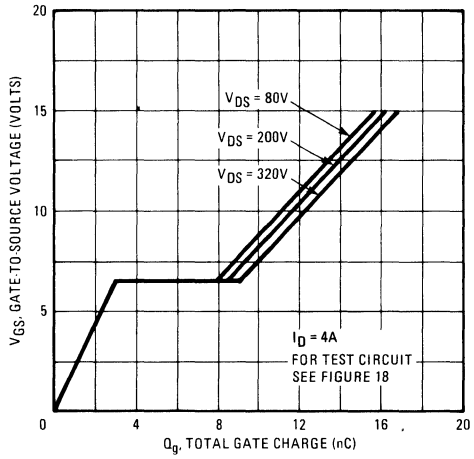


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

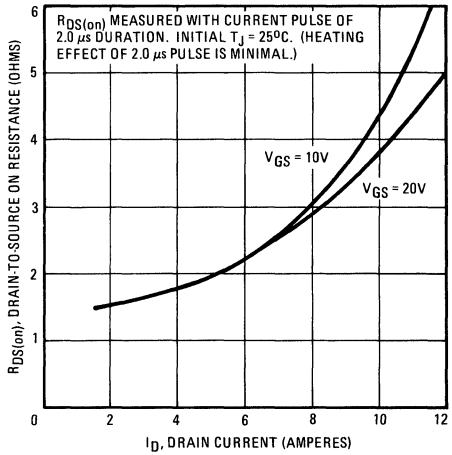


Fig. 12 — Typical On-Resistance Vs. Drain Current

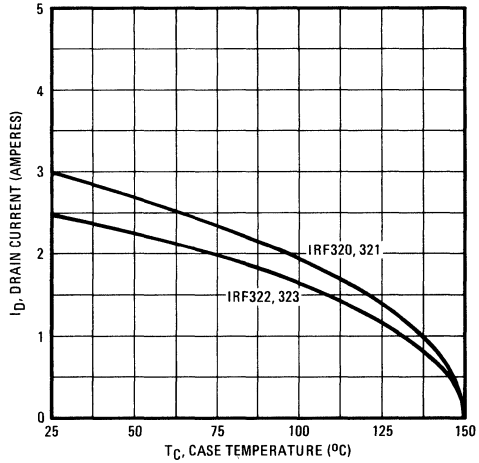


Fig. 13 — Maximum Drain Current Vs. Case Temperature

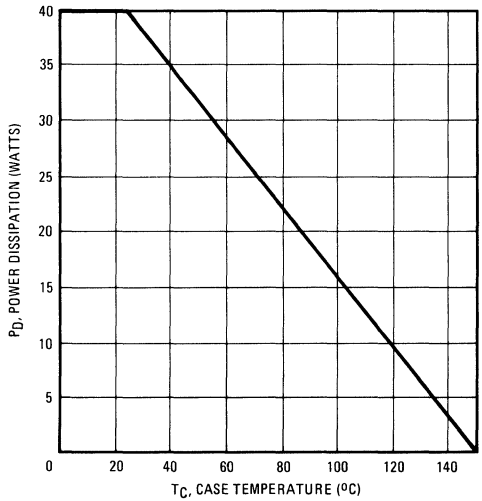


Fig. 14 — Power Vs. Temperature Derating Curve

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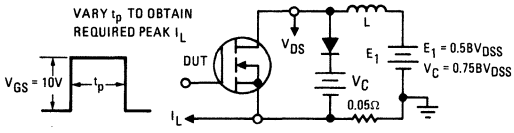


Fig. 15 — Clamped Inductive Test Circuit

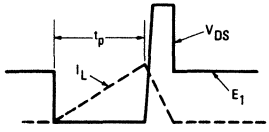


Fig. 16 — Clamped Inductive Waveforms

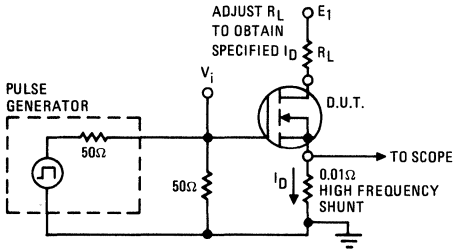


Fig. 17 — Switching Time Test Circuit

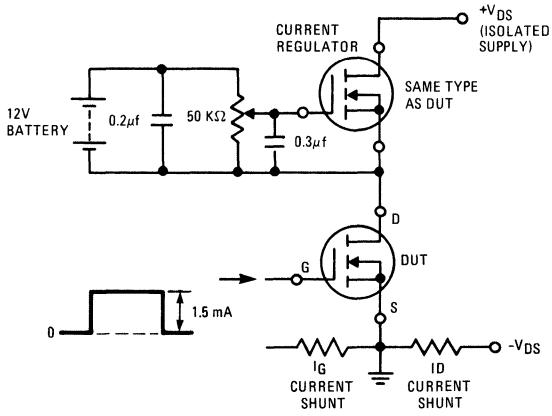


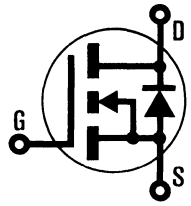
Fig. 18 — Gate Charge Test Circuit

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS

IRF330
IRF331
IRF332
IRF333



N-Channel

400 Volt, 1.0 Ohm HEXFET

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

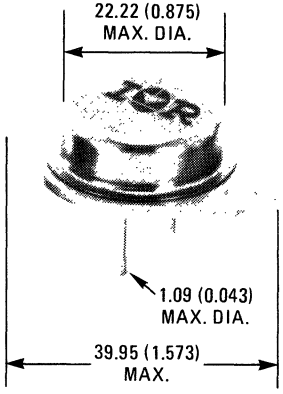
Features:

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

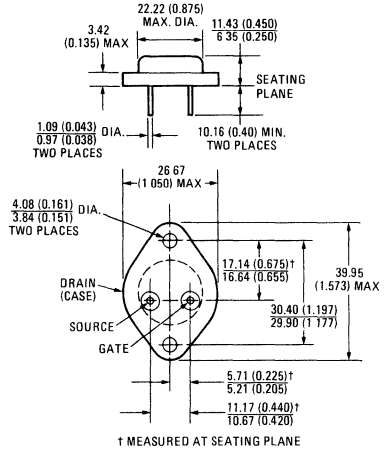
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF330	400V	1.0Ω	5.5A
IRF331	350V	1.0Ω	5.5A
IRF332	400V	1.5Ω	4.5A
IRF333	350V	1.5Ω	4.5A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



† MEASURED AT SEATING PLANE

Conforms to JEDEC Outline TO-204AA (TO-3)
Dimensions in Millimeters and (Inches)

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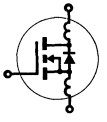
Absolute Maximum Ratings

Parameter		IRF330	IRF331	IRF332	IRF333	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	5.5	5.5	4.5	4.5	A
I_D @ T_C = 100°C	Continuous Drain Current	3.5	3.5	3.0	3.0	A
I_{DM}	Pulsed Drain Current ③	22	22	18	18	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		22	22	18	18	
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF330 IRF332	400	—	—	V	V_{GS} = 0V
		IRF331 IRF333	350	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	−100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF330 IRF331	5.5	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		IRF332 IRF333	4.5	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF330 IRF331	—	0.8	1.0	Ω	V_{GS} = 10V, I_D = 3.0A
		IRF332 IRF333	—	1.0	1.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	3.0	4.0	—	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 3.0A
C_{iss}	Input Capacitance	ALL	—	700	900	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	150	300	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	40	80	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	—	30	ns	V_{DD} = 175V, I_D = 3.0A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	—	35	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	—	55	ns	
t_f	Fall Time	ALL	—	—	35	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	18	30	nC	V_{GS} = 10V, I_D = 7.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	11	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	7.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	1.67	K/W	
R_{thCS}	Case-to-Sink	ALL	—	0.1	—	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF330 IRF331	–	–	5.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF332 IRF333	–	–	4.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF330 IRF331	–	–	22	A	
		IRF332 IRF333	–	–	18	A	
V_{SD}	Diode Forward Voltage ②	IRF330 IRF331	–	–	1.6	V	T_C = 25°C, I_S = 5.5A, V_{GS} = 0V
		IRF332 IRF333	–	–	1.5	V	T_C = 25°C, I_S = 4.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	600	–	ns	T_J = 150°C, I_F = 5.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.0	–	μC	T_J = 150°C, I_F = 5.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

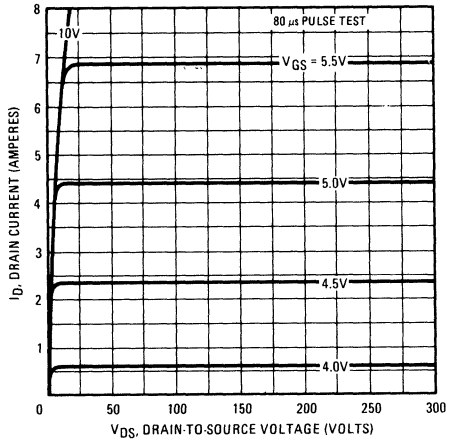


Fig. 1 — Typical Output Characteristics

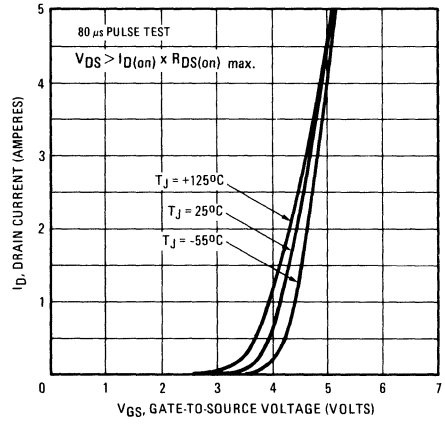


Fig. 2 — Typical Transfer Characteristics

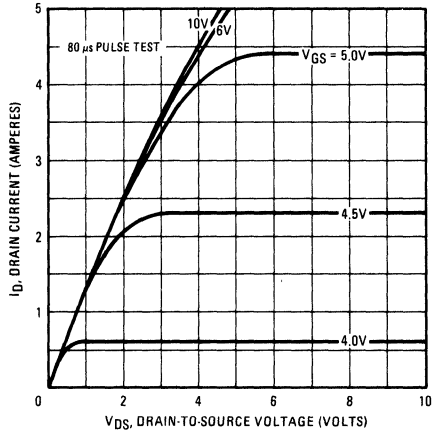


Fig. 3 — Typical Saturation Characteristics

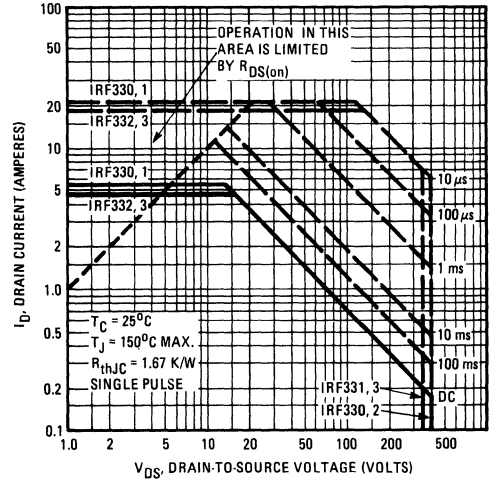


Fig. 4 — Maximum Safe Operating Area

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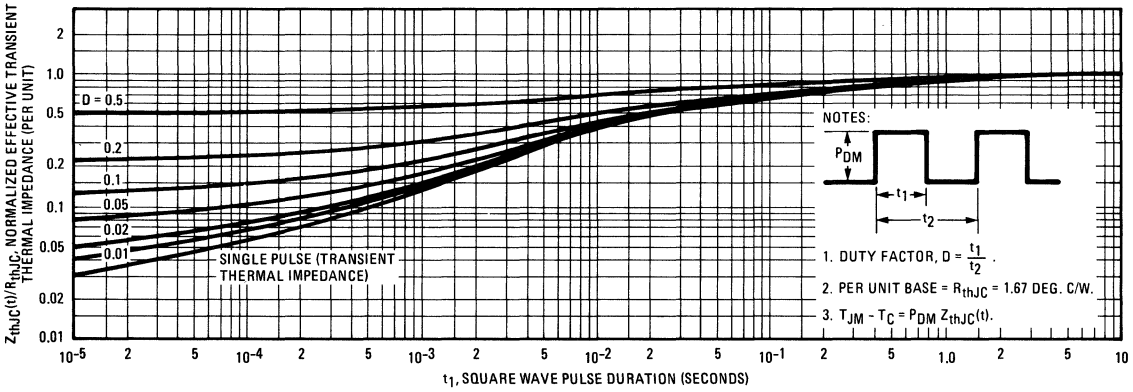


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

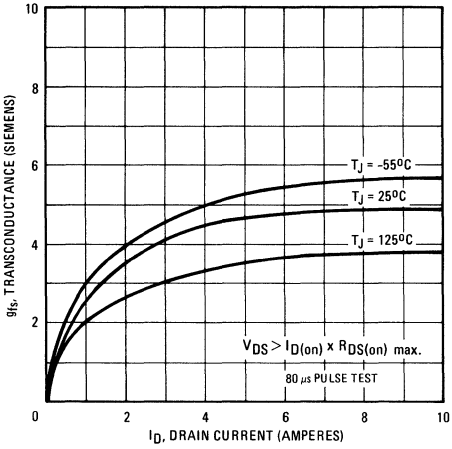


Fig. 6 — Typical Transconductance Vs. Drain Current

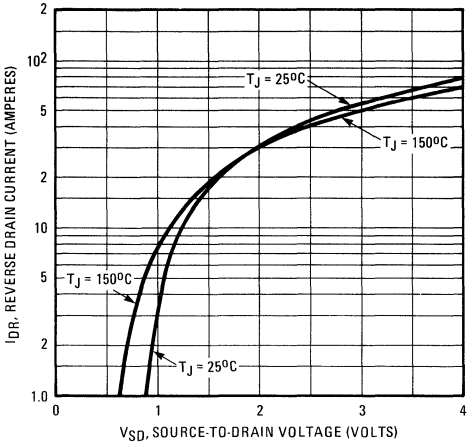


Fig. 7 — Typical Source-Drain Diode Forward Voltage

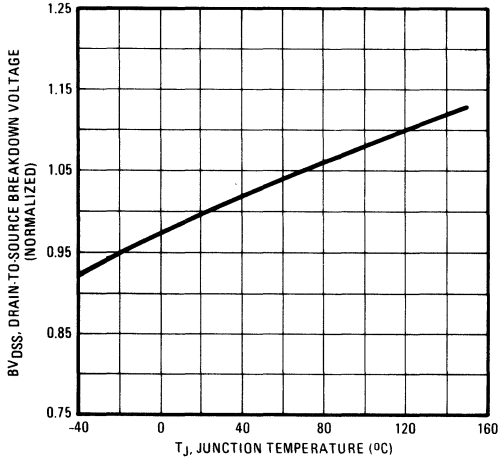


Fig. 8 — Breakdown Voltage Vs. Temperature

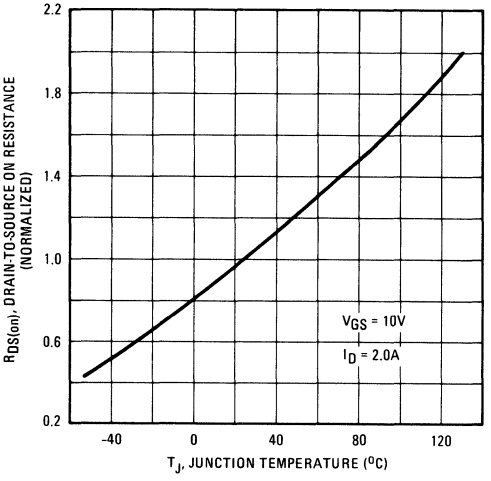


Fig. 9 — Normalized On-Resistance Vs. Temperature

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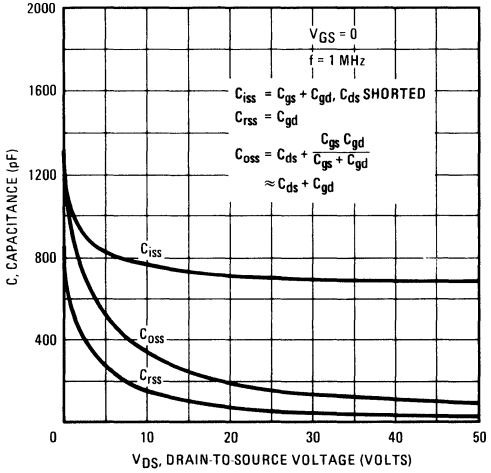


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

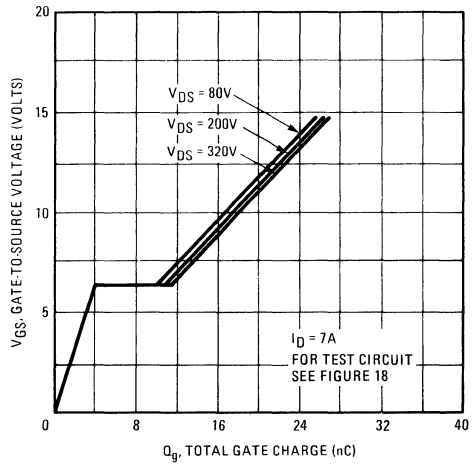


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

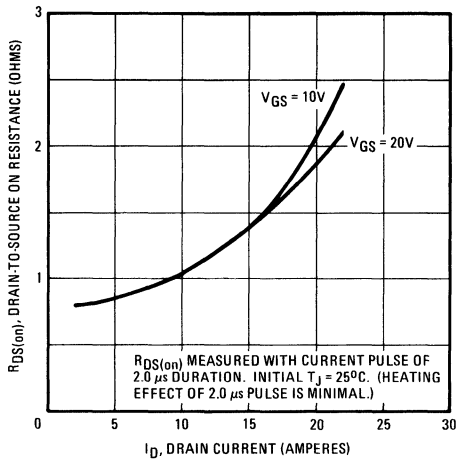


Fig. 12 — Typical On-Resistance Vs. Drain Current

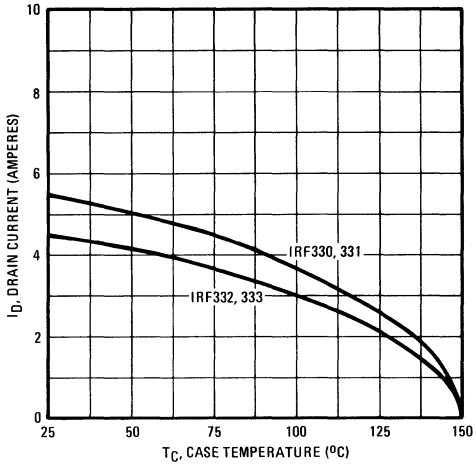


Fig. 13 — Maximum Drain Current Vs. Case Temperature

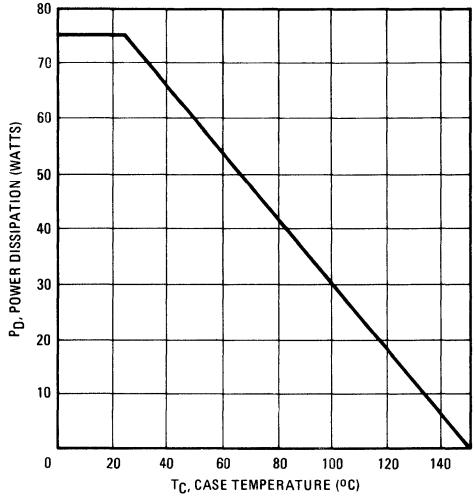


Fig. 14 — Power Vs. Temperature Derating Curve

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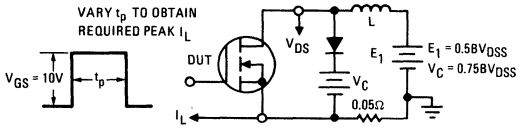


Fig. 15 — Clamped Inductive Test Circuit

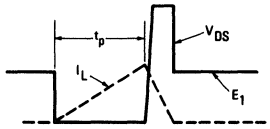


Fig. 16 — Clamped Inductive Waveforms

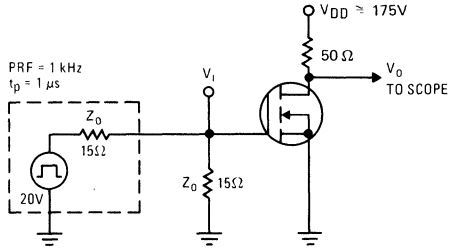


Fig. 17 — Switching Time Test Circuit

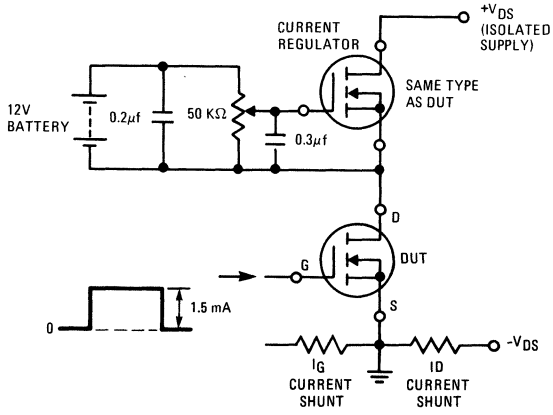


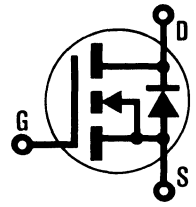
Fig. 18 — Gate Charge Test Circuit

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS IRF340 IRF341 IRF342 IRF343

N-CHANNEL POWER MOSFETs



400 Volt, 0.55 Ohm HEXFET

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

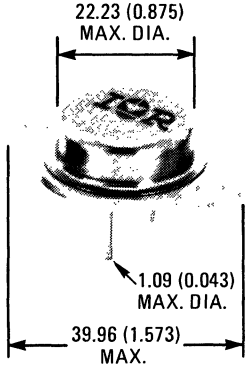
Features:

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

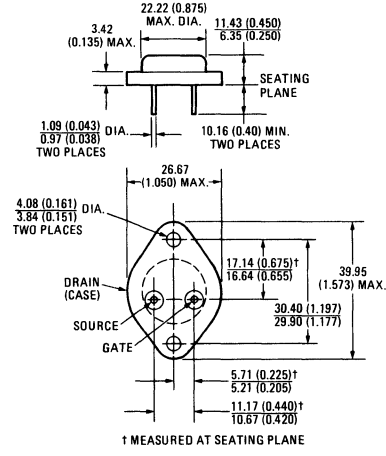
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF340	400V	0.55Ω	10A
IRF341	350V	0.55Ω	10A
IRF342	400V	0.80Ω	8.0A
IRF343	350V	0.80Ω	8.0A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



† MEASURED AT SEATING PLANE

Conforms to JEDEC Outline TO-204AA (TO-3)
Dimensions in Millimeters and (Inches)

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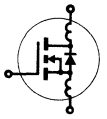
Absolute Maximum Ratings

Parameter		IRF340	IRF341	IRF342	IRF343	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	10	10	8.0	8.0	A
I_D @ T_C = 100°C	Continuous Drain Current	6.0	6.0	5.0	5.0	A
I_{DM}	Pulsed Drain Current ③	40	40	32	32	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		40	40	32	32	
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF340 IRF342	400	–	–	V	V_{GS} = 0V
		IRF341 IRF343	350	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF340 IRF341	10	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF342 IRF343	8.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF340 IRF341	–	0.47	0.55	Ω	V_{GS} = 10V, I_D = 5.0A
		IRF342 IRF343	–	0.68	0.80	Ω	
g_{fs}	Forward Transconductance ②	ALL	4.0	7.0	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 5.0A
C_{iss}	Input Capacitance	ALL	–	1250	1600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	300	450	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	80	150	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	17	35	ns	V_{DD} ≈ 175V, I_D = 5.0A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	5.0	15	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	45	90	ns	
t_f	Fall Time	ALL	–	16	35	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	41	60	nC	V_{GS} = 10V, I_D = 12A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	18	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	23	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.0	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF340 IRF341	–	–	10	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF342 IRF343	–	–	8.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF340 IRF341	–	–	40	A	
		IRF342 IRF343	–	–	32	A	
V_{SD}	Diode Forward Voltage ②	IRF340 IRF341	–	–	2.0	V	T_C = 25°C, I_S = 10A, V_{GS} = 0V
		IRF342 IRF343	–	–	1.9	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	800	–	ns	T_J = 150°C, I_F = 10A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	5.7	–	μC	T_J = 150°C, I_F = 10A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

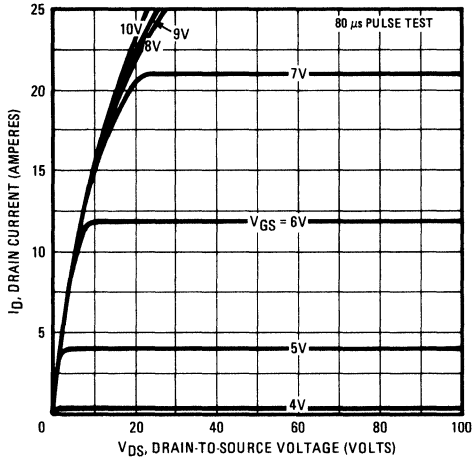


Fig. 1 – Typical Output Characteristics

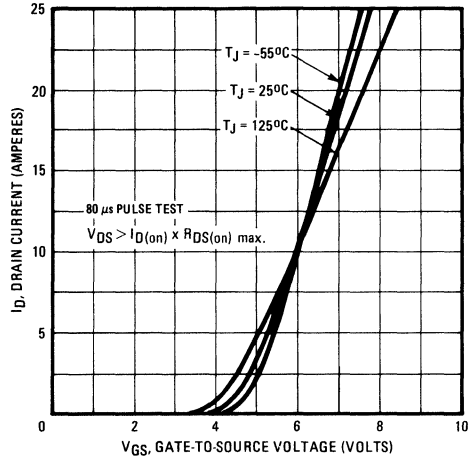


Fig. 2 – Typical Transfer Characteristics

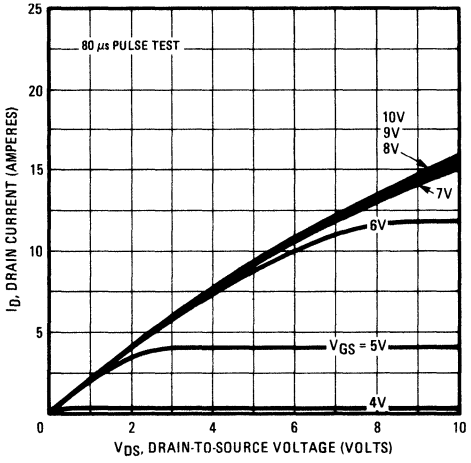


Fig. 3 – Typical Saturation Characteristics

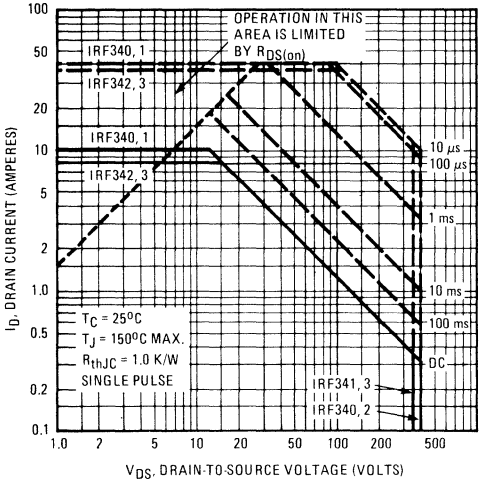


Fig. 4 – Maximum Safe Operating Area

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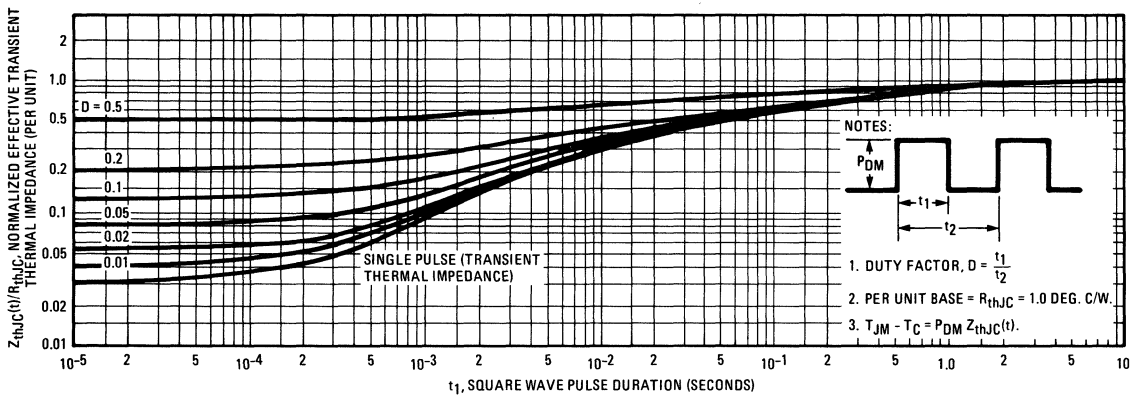


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

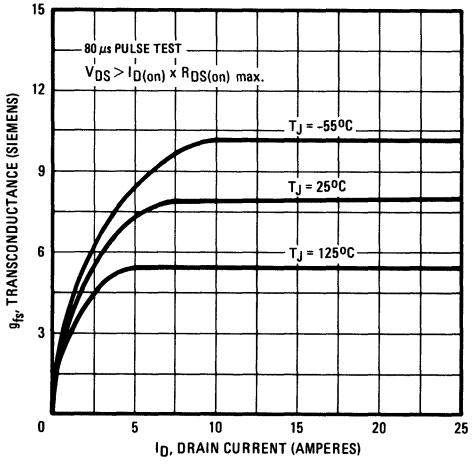


Fig. 6 — Typical Transconductance Vs. Drain Current

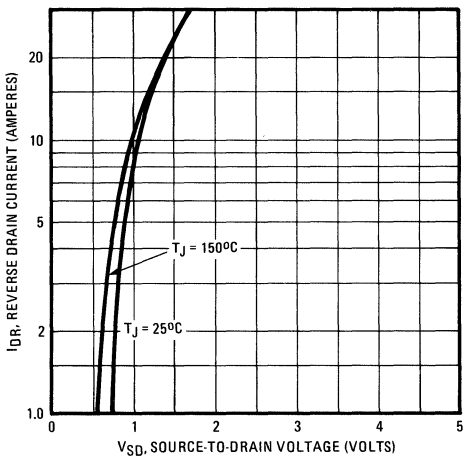


Fig. 7 — Typical Source-Drain Diode Forward Voltage

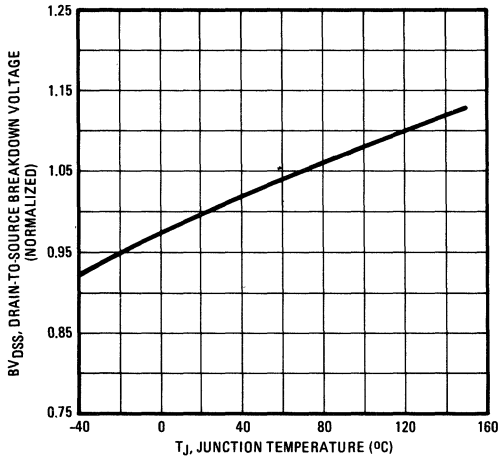


Fig. 8 — Breakdown Voltage Vs. Temperature

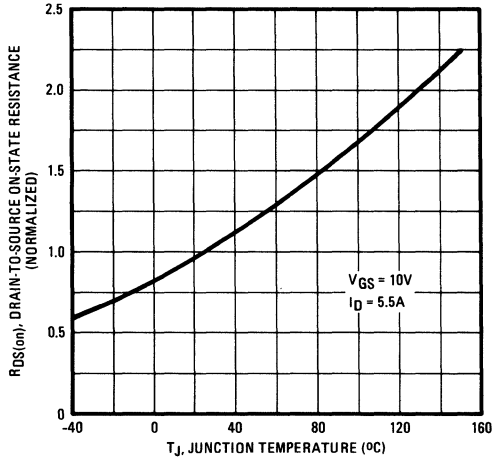


Fig. 9 — Normalized On-Resistance Vs. Temperature

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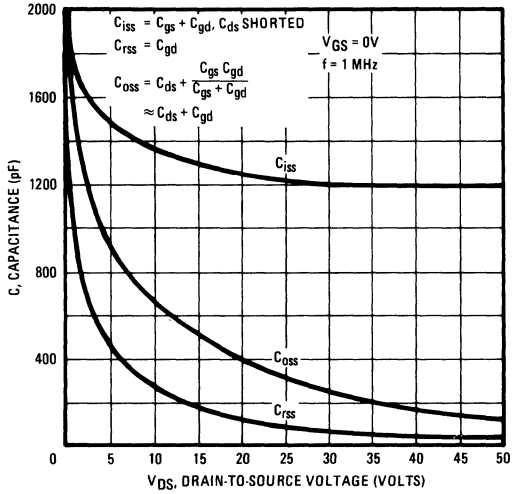


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

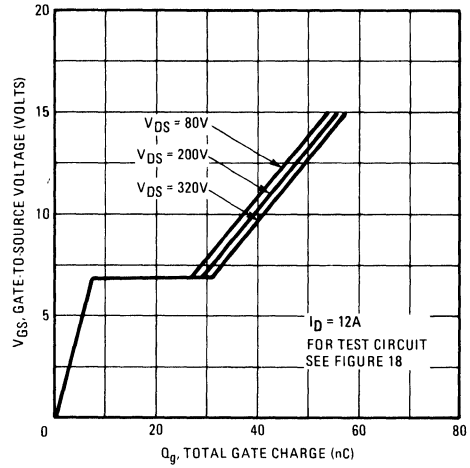


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

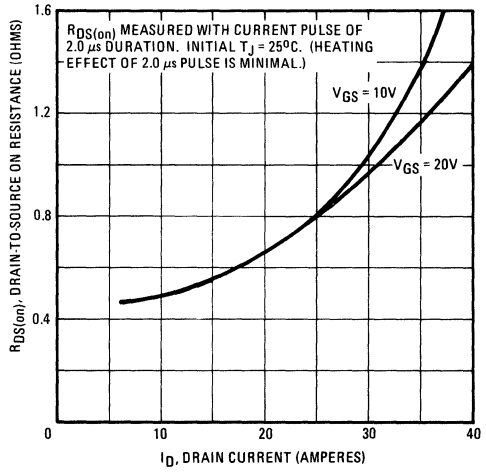


Fig. 12 — Typical On-Resistance Vs. Drain Current

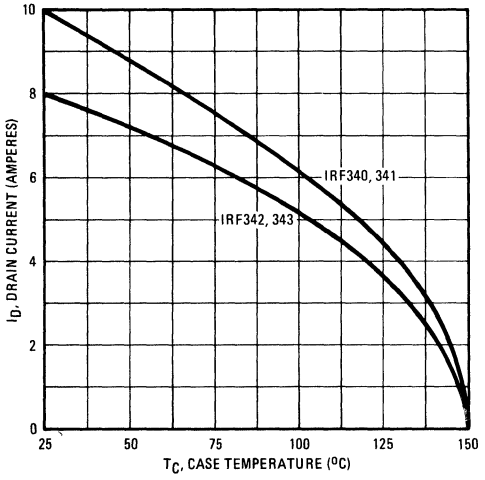


Fig. 13 — Maximum Drain Current Vs. Case Temperature

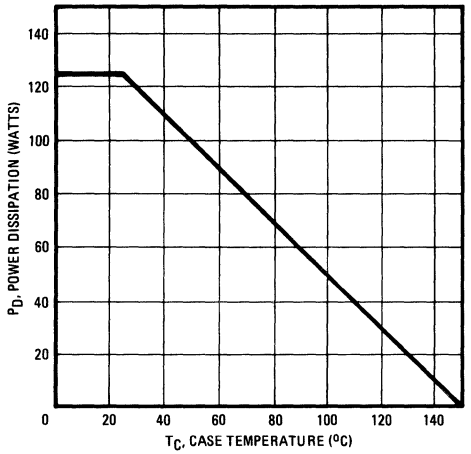


Fig. 14 — Power Vs. Temperature Derating Curve

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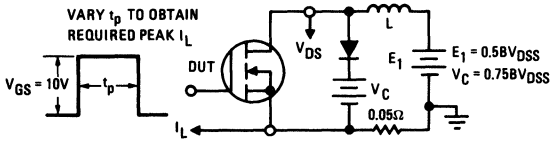


Fig. 15 — Clamped Inductive Test Circuit

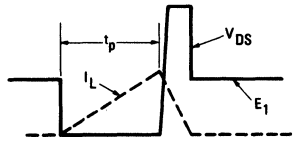


Fig. 16 — Clamped Inductive Waveforms

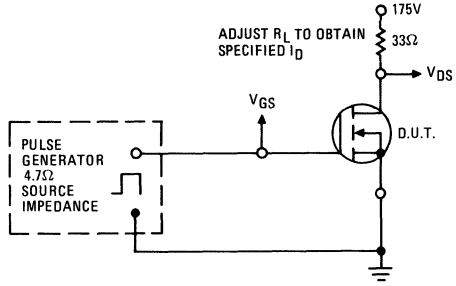


Fig. 17 — Switching Time Test Circuit

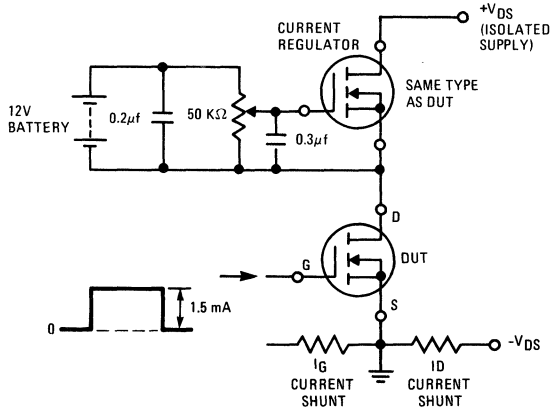


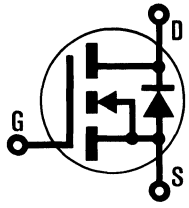
Fig. 18 — Gate Charge Test Circuit

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS

IRF350
IRF351
IRF352
IRF353



N-Channel

400 Volt, 0.3 Ohm HEXFET

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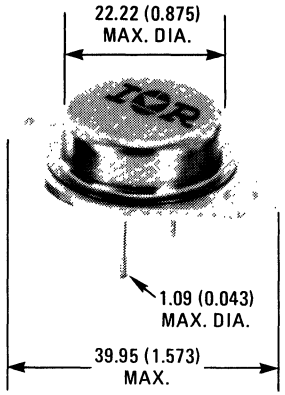
Features:

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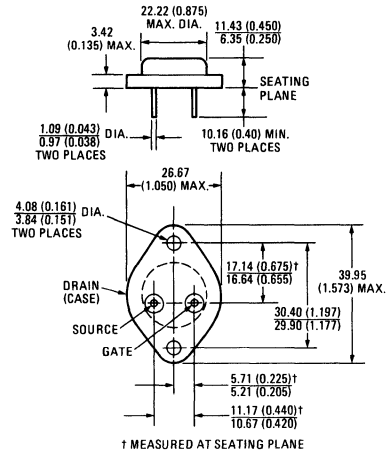
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF350	400V	0.3Ω	15A
IRF351	350V	0.3Ω	15A
IRF352	400V	0.4Ω	13A
IRF353	350V	0.4Ω	13A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



† MEASURED AT SEATING PLANE

Conforms to JEDEC Outline TO-204AA (TO-3)
Dimensions in Millimeters and (Inches)

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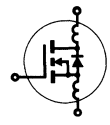
Absolute Maximum Ratings

Parameter		IRF350	IRF351	IRF352	IRF353	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	15	15	13	13	A
I_D @ T_C = 100°C	Continuous Drain Current	9.0	9.0	8.0	8.0	A
I_{DM}	Pulsed Drain Current ③	60	60	52	52	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	150 (See Fig. 14)				W
	Linear Derating Factor	1.2 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	60	(See Fig. 15 and 16) L = 100μH 60	52	52	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF350 IRF352	400	–	–	V	V_{GS} = 0V
		IRF351 IRF353	350	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	−100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF350 IRF351	15	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF352 IRF353	13	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF350 IRF351	–	0.25	0.3	Ω	V_{GS} = 10V, I_D = 8.0A
		IRF352 IRF353	–	0.3	0.4	Ω	
g_{fs}	Forward Transconductance ②	ALL	8.0	10	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 8.0A
C_{iss}	Input Capacitance	ALL	–	2000	3000	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	400	600	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	100	200	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	35	ns	V_{DD} ≈ 180V, I_D = 8.0A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	65	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	150	ns	
t_f	Fall Time	ALL	–	–	75	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	79	120	nC	V_{GS} = 10V, I_D = 18A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	38	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	41	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	0.83	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF350 IRF351	–	–	15	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF352 IRF353	–	–	13	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF350 IRF351	–	–	60	A	
		IRF352 IRF353	–	–	52	A	
V_{SD}	Diode Forward Voltage ②	IRF350 IRF351	–	–	1.6	V	T_C = 25°C, I_S = 15A, V_{GS} = 0V
		IRF352 IRF353	–	–	1.5	V	T_C = 25°C, I_S = 13A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	1000	–	ns	T_J = 150°C, I_F = 15A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	6.6	–	μC	T_J = 150°C, I_F = 15A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

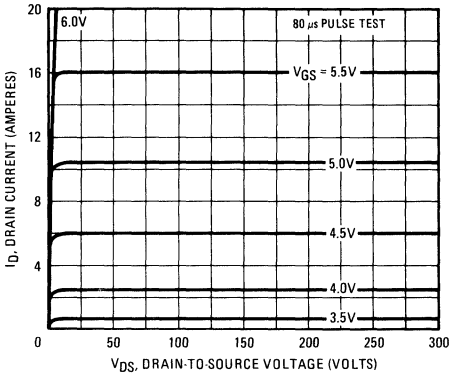


Fig. 1 — Typical Output Characteristics

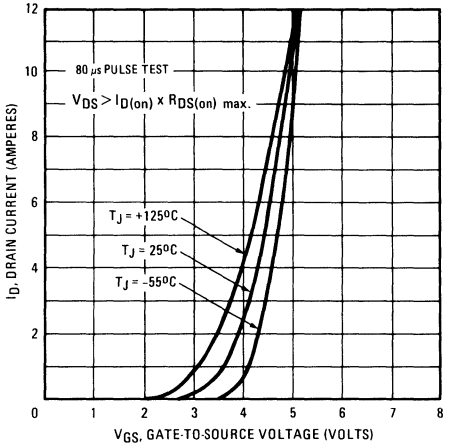


Fig. 2 — Typical Transfer Characteristics

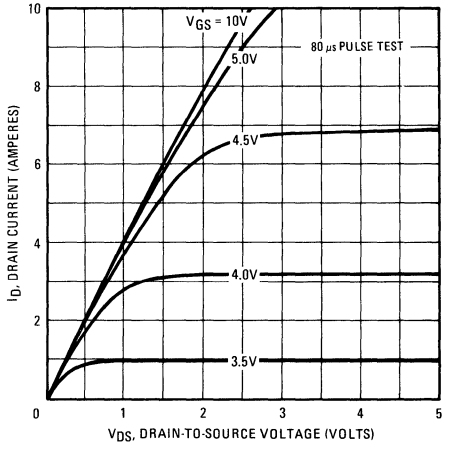


Fig. 3 — Typical Saturation Characteristics

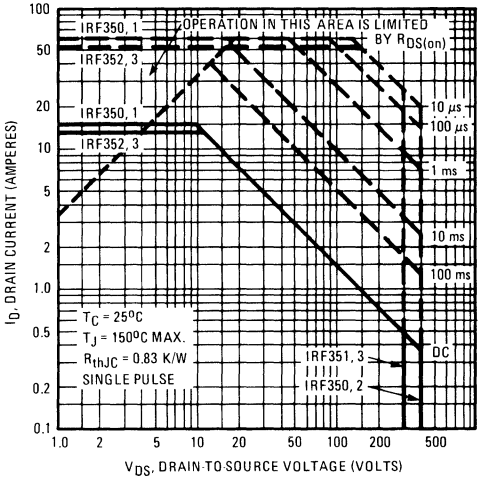


Fig. 4 — Maximum Safe Operating Area

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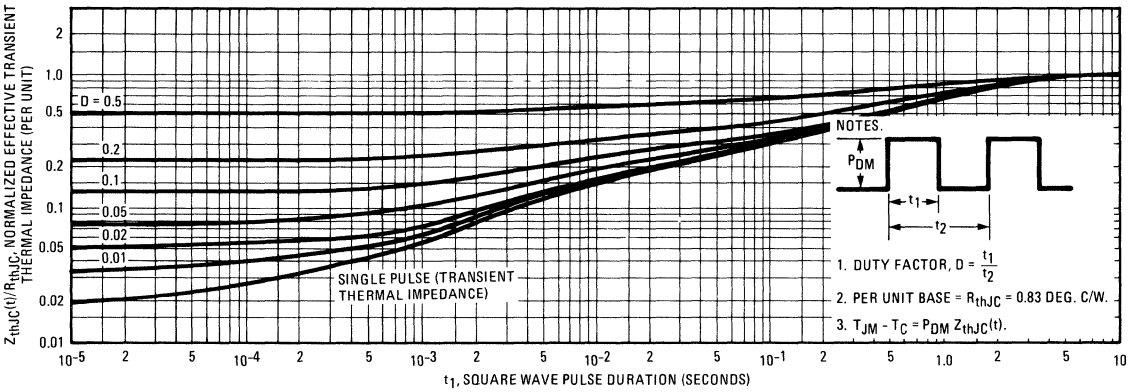


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

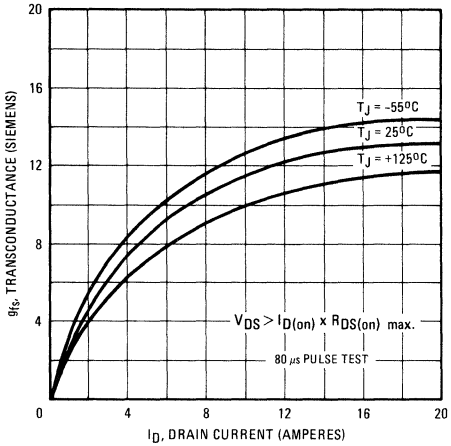


Fig. 6 — Typical Transconductance Vs. Drain Current

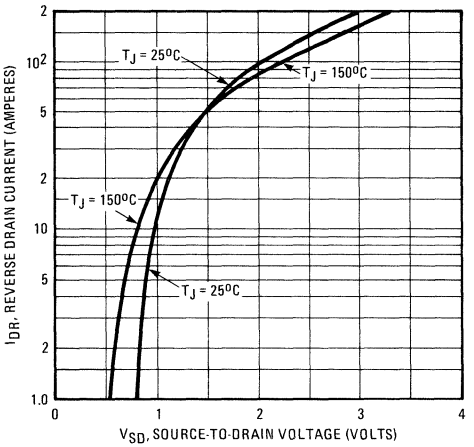


Fig. 7 — Typical Source-Drain Diode Forward Voltage

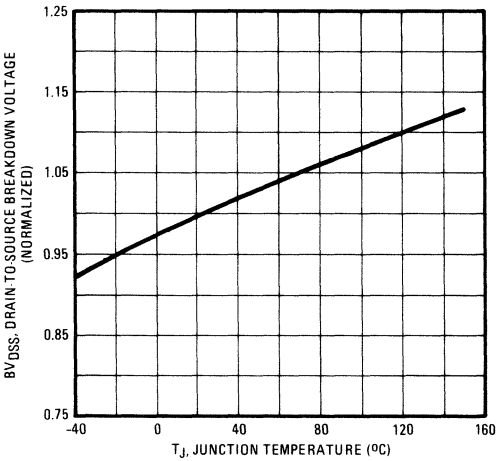


Fig. 8 — Breakdown Voltage Vs. Temperature

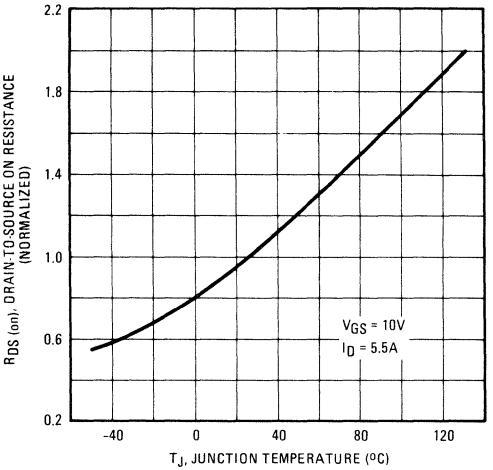


Fig. 9 — Normalized On-Resistance Vs. Temperature

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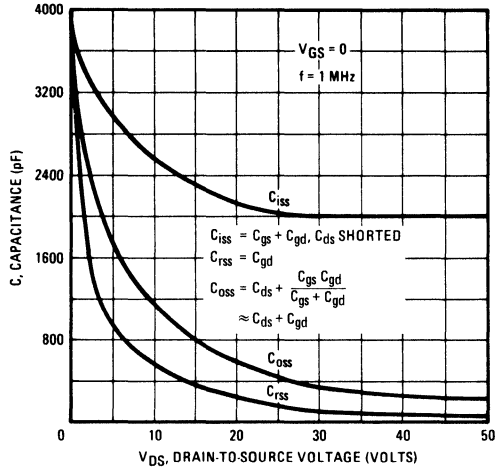


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

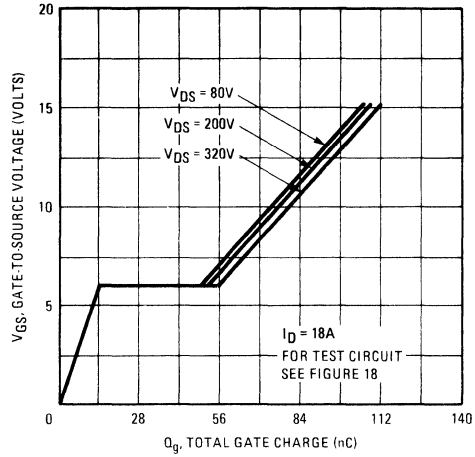


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

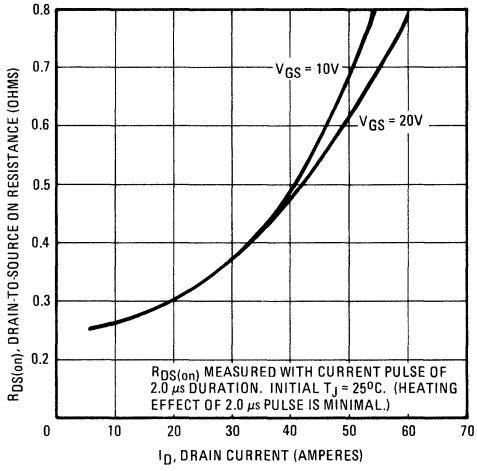


Fig. 12 — Typical On-Resistance Vs. Drain Current

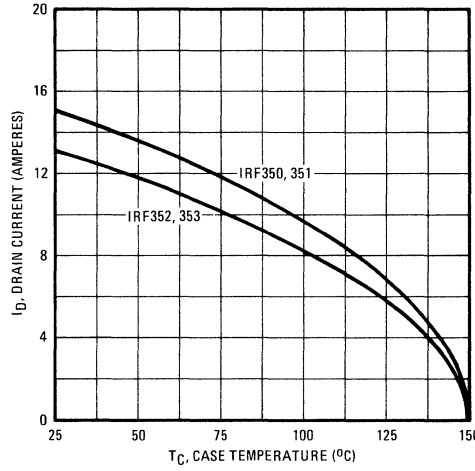


Fig. 13 — Maximum Drain Current Vs. Case Temperature

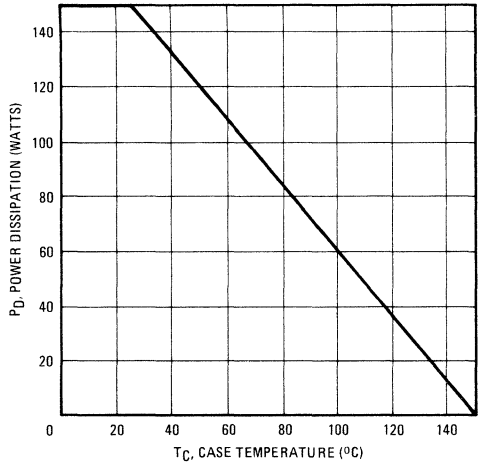


Fig. 14 — Power Vs. Temperature Derating Curve

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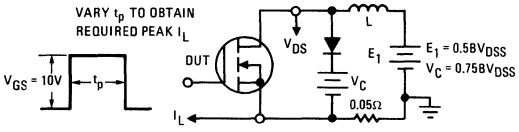


Fig. 15 — Clamped Inductive Test Circuit

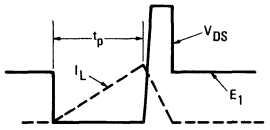


Fig. 16 — Clamped Inductive Waveforms

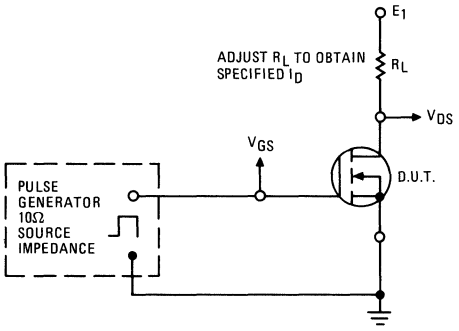


Fig. 17 — Switching Time Test Circuit

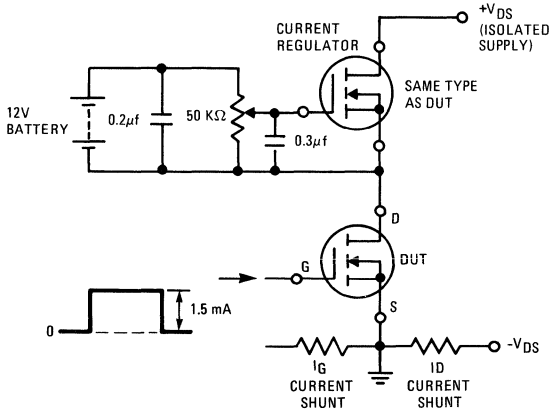


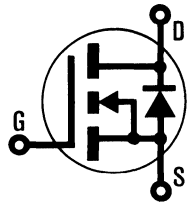
Fig. 18 — Gate Charge Test Circuit

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS

IRF420
IRF421
IRF422
IRF423



N-Channel

500 Volt, 3.0 Ohm HEXFET

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

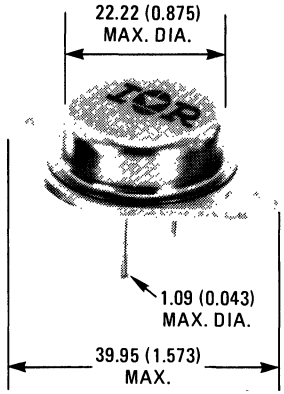
Features:

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

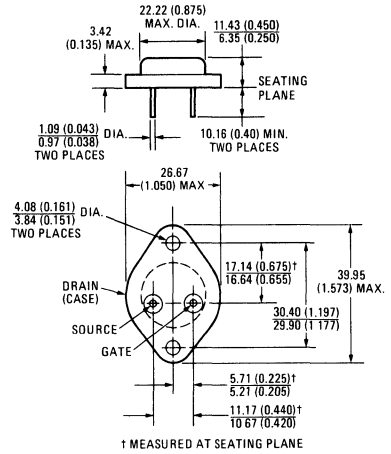
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF420	500V	3.0Ω	2.5A
IRF421	450V	3.0Ω	2.5A
IRF422	500V	4.0Ω	2.0A
IRF423	450V	4.0Ω	2.0A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Conforms to JEDEC Outline TO-204AA (TO-3)
Dimensions in Inches and (Millimeters)

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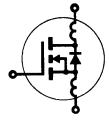
Absolute Maximum Ratings

Parameter		IRF420	IRF421	IRF422	IRF423	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	2.5	2.5	2.0	2.0	A
I_D @ T_C = 100°C	Continuous Drain Current	1.5	1.5	1.0	1.0	A
I_{DM}	Pulsed Drain Current ③	10	10	8.0	8.0	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		10	10	8.0	8.0	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF420 IRF422	500	–	–	V	V_{GS} = 0V
		IRF421 IRF423	450	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF420 IRF421	2.5	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF422 IRF423	2.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF420 IRF421	–	2.5	3.0	Ω	V_{GS} = 10V, I_D = 1.0A
		IRF422 IRF423	–	3.0	4.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	1.75	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 1.0A
C_{iss}	Input Capacitance	ALL	–	300	400	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	75	150	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	20	40	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	30	60	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 1.0A, Z_O = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	25	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	30	60	ns	
t_f	Fall Time	ALL	–	15	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	11	15	nC	V_{GS} = 10V, I_D = 3.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	5.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	6.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	3.12	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF420 IRF421	–	–	2.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF422 IRF423	–	–	2.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF420 IRF421	–	–	10	A	
		IRF422 IRF423	–	–	8.0	A	
V_{SD}	Diode Forward Voltage ②	IRF420 IRF421	–	–	1.4	V	T_C = 25°C, I_S = 2.5A, V_{GS} = 0V
		IRF422 IRF423	–	–	1.3	V	T_C = 25°C, I_S = 2.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	600	–	ns	T_J = 150°C, I_F = 2.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	3.5	–	μC	T_J = 150°C, I_F = 2.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

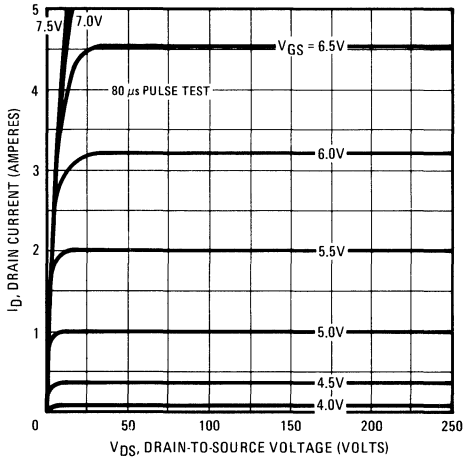


Fig. 1 — Typical Output Characteristics

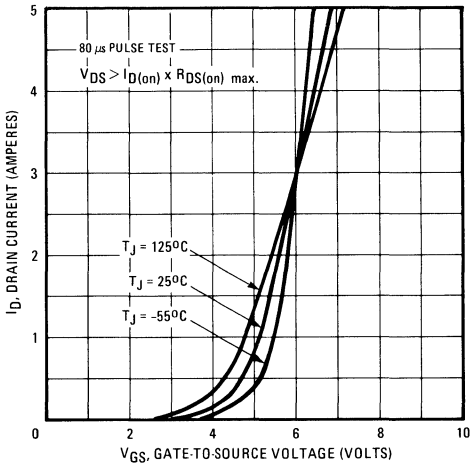


Fig. 2 — Typical Transfer Characteristics

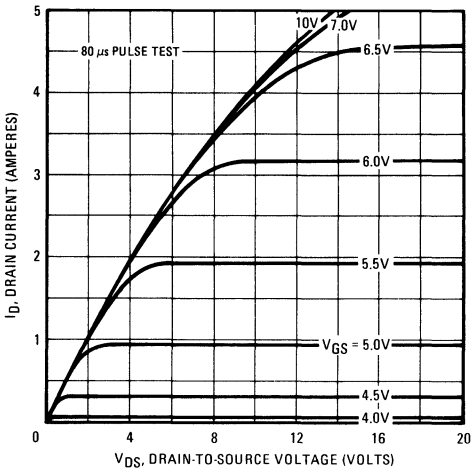


Fig. 3 — Typical Saturation Characteristics

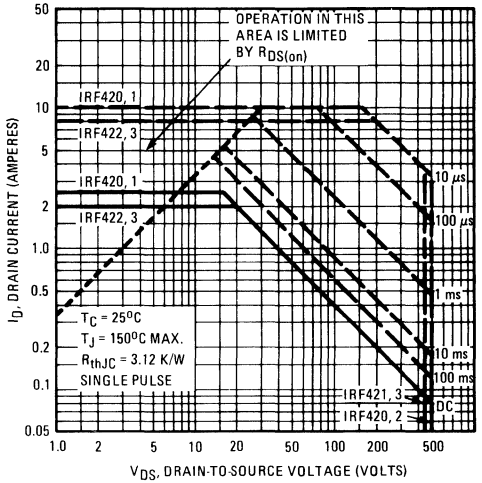


Fig. 4 — Maximum Safe Operating Area

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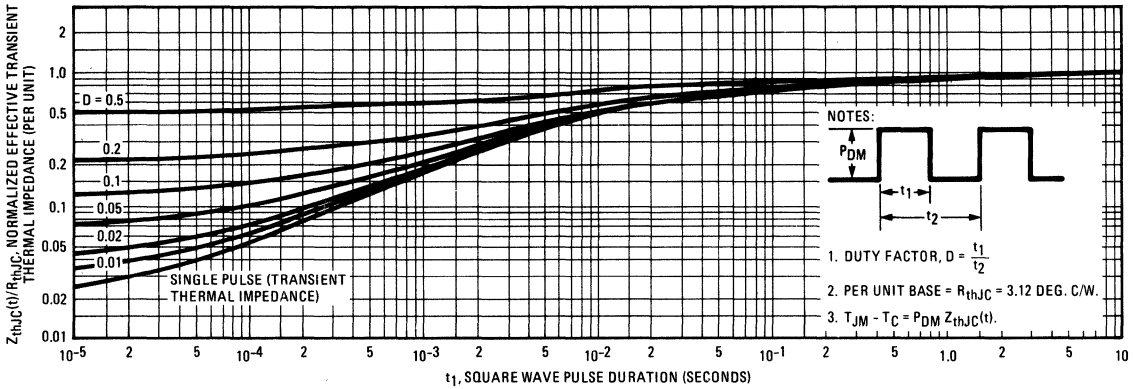


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

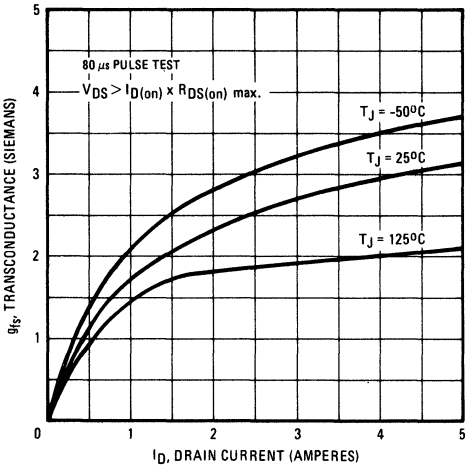


Fig. 6 — Typical Transconductance Vs. Drain Current

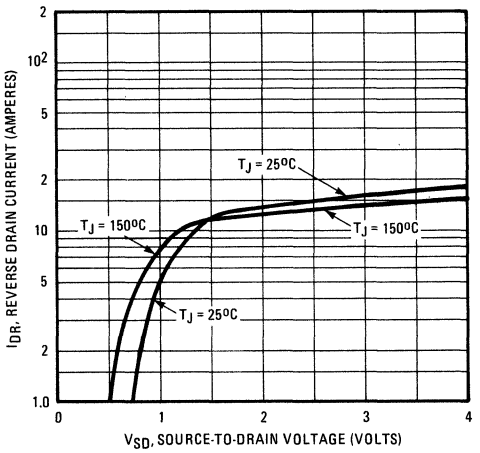


Fig. 7 — Typical Source-Drain Diode Forward Voltage

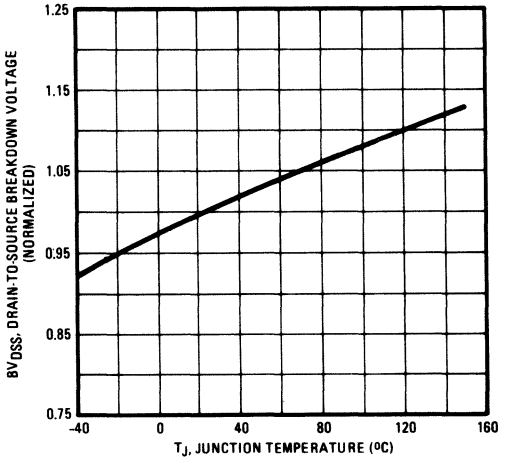


Fig. 8 — Breakdown Voltage Vs. Temperature

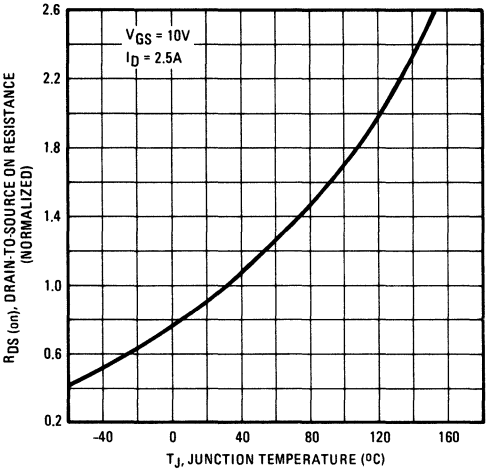


Fig. 9 — Normalized On-Resistance Vs. Temperature

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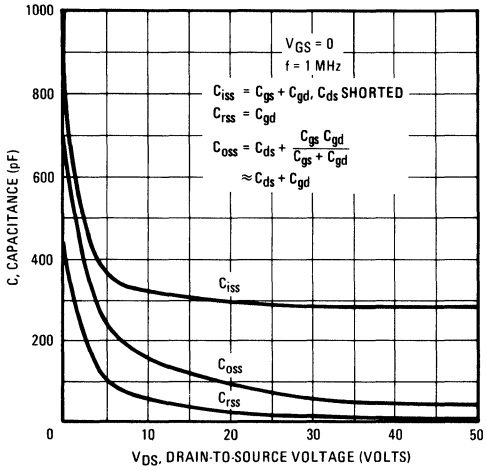


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

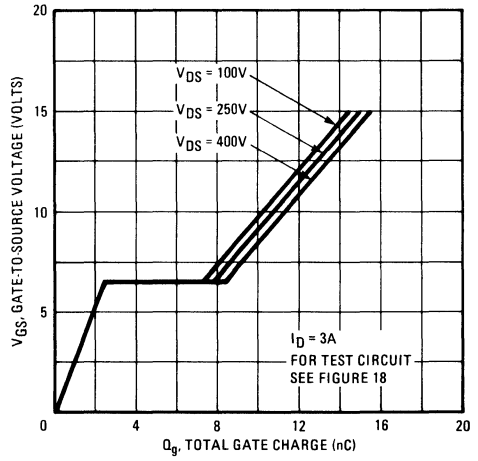


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

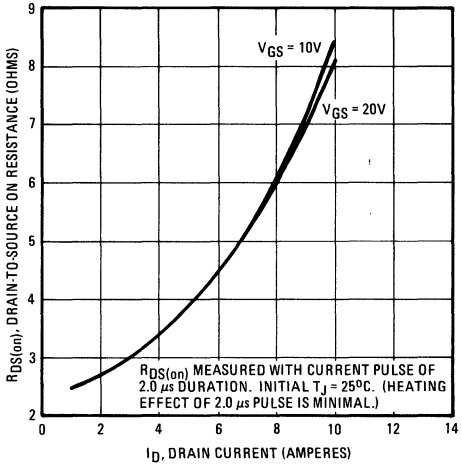


Fig. 12 — Typical On-Resistance Vs. Drain Current

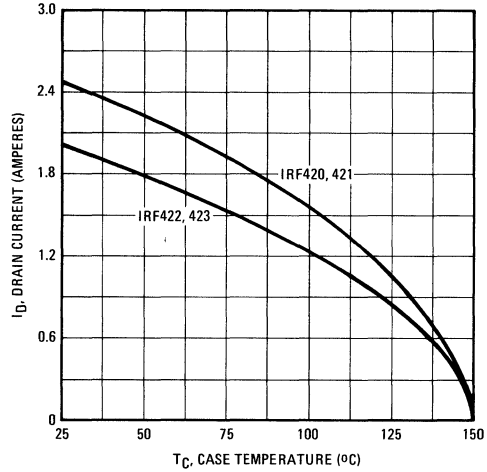


Fig. 13 — Maximum Drain Current Vs. Case Temperature

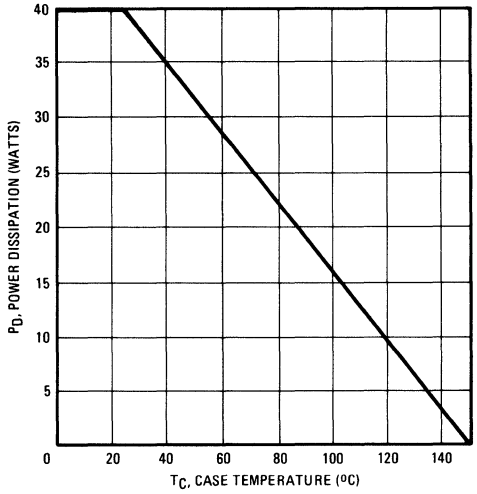


Fig. 14 — Power Vs. Temperature Derating Curve

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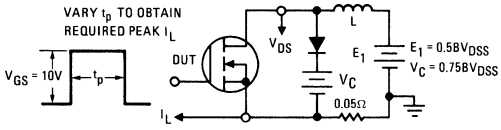


Fig. 15 — Clamped Inductive Test Circuit

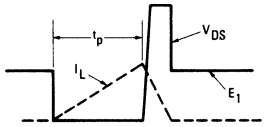


Fig. 16 — Clamped Inductive Waveforms

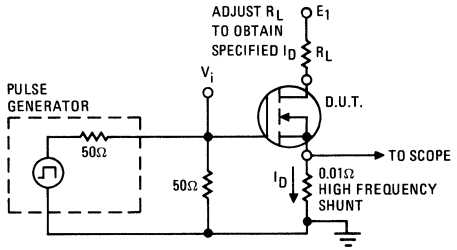


Fig. 17 — Switching Time Test Circuit

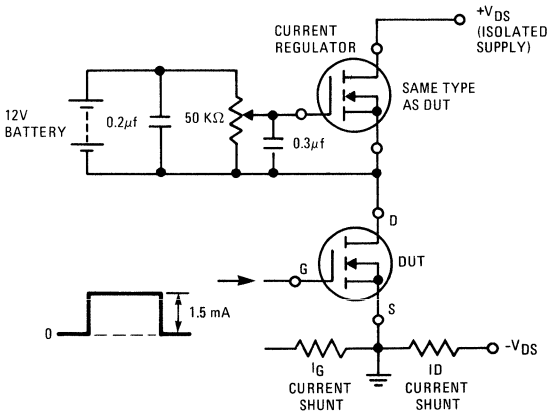


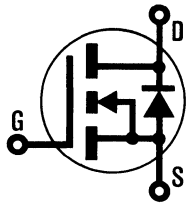
Fig. 18 — Gate Charge Test Circuit

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS

IRF430
IRF431
IRF432
IRF433



N-Channel

500 Volt, 1.5 Ohm HEXFET

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

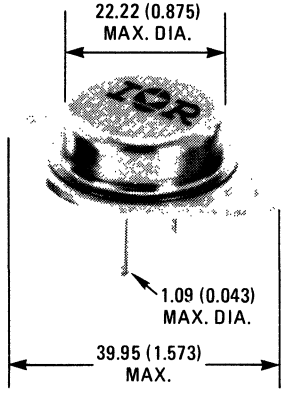
Features:

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

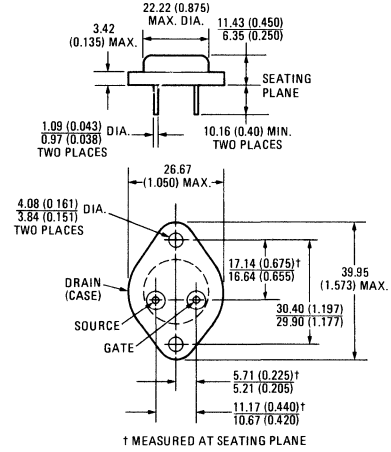
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF430	500V	1.5Ω	4.5A
IRF431	450V	1.5Ω	4.5A
IRF432	500V	2.0Ω	4.0A
IRF433	450V	2.0Ω	4.0A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



† MEASURED AT SEATING PLANE

Conforms to JEDEC Outline TO-204AA (TO-3)
Dimensions in Millimeters and (Inches)

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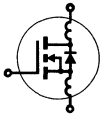
Absolute Maximum Ratings

Parameter		IRF430	IRF431	IRF432	IRF433	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	4.5	4.5	4.0	4.0	A
I_D @ T_C = 100°C	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_{DM}	Pulsed Drain Current ③	18	18	16	16	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		18	18	16	16	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF430 IRF432	500	–	–	V	V_{GS} = 0V
		IRF431 IRF433	450	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF430 IRF431	4.5	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF432 IRF433	4.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF430 IRF431	–	1.3	1.5	Ω	V_{GS} = 10V, I_D = 2.5A
		IRF432 IRF433	–	1.5	2.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	2.5	3.2	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 2.5A
C_{iss}	Input Capacitance	ALL	–	600	800	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	100	200	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	30	60	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} ≈ 225V, I_D = 2.5A, Z_O = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	30	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	55	ns	
t_f	Fall Time	ALL	–	–	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	22	30	nC	V_{GS} = 10V, I_D = 6.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	11	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	11	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF430 IRF431	–	–	4.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF432 IRF433	–	–	4.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF430 IRF431	–	–	18	A	
		IRF432 IRF433	–	–	16	A	
V_{SD}	Diode Forward Voltage ②	IRF430 IRF431	–	–	1.4	V	T_C = 25°C, I_S = 4.5A, V_{GS} = 0V
		IRF432 IRF433	–	–	1.3	V	T_C = 25°C, I_S = 4.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	800	–	ns	T_J = 150°C, I_F = 4.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.6	–	μC	T_J = 150°C, I_F = 4.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

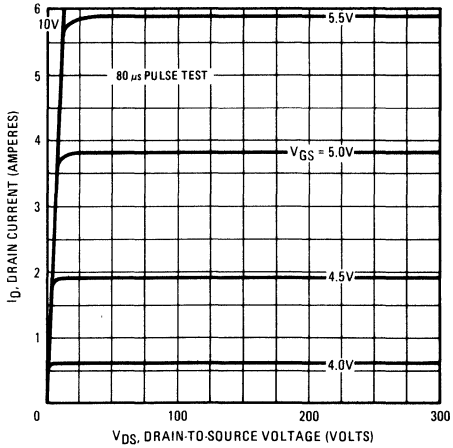


Fig. 1 – Typical Output Characteristics

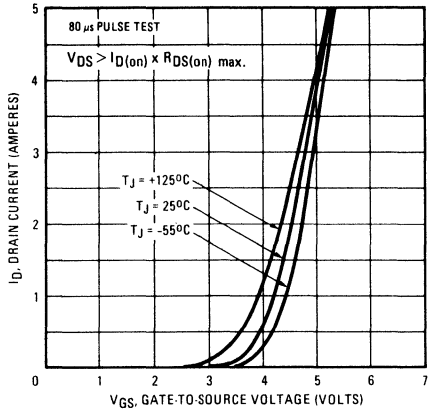


Fig. 2 – Typical Transfer Characteristics

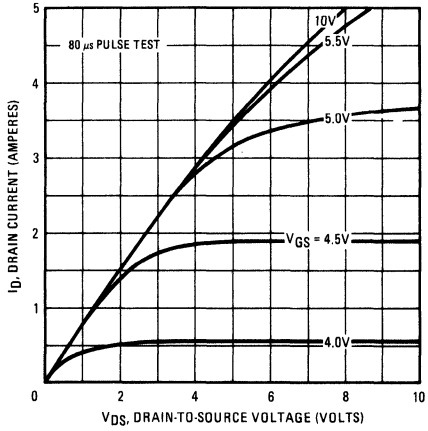


Fig. 3 – Typical Saturation Characteristics

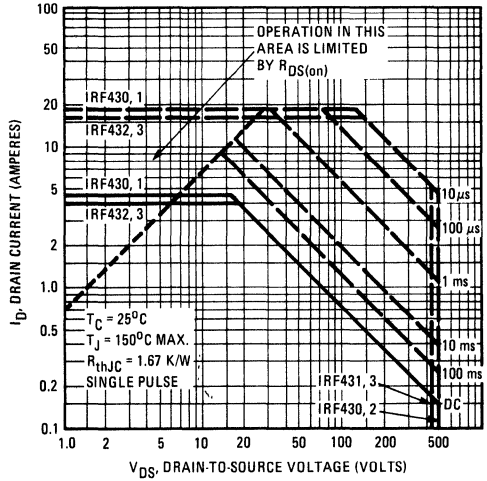


Fig. 4 – Maximum Safe Operating Area

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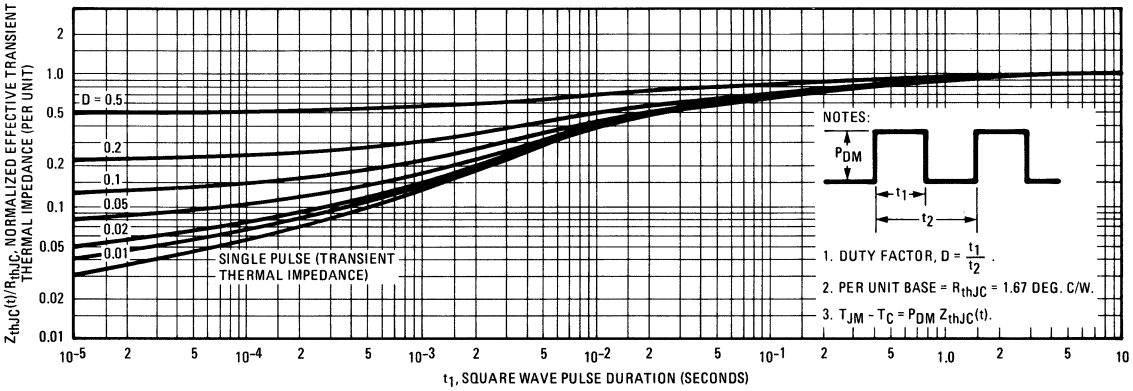


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

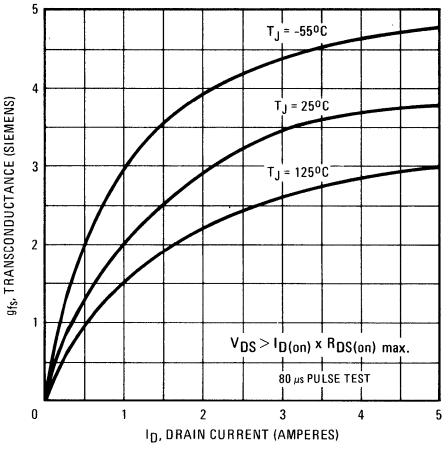


Fig. 6 — Typical Transconductance Vs. Drain Current

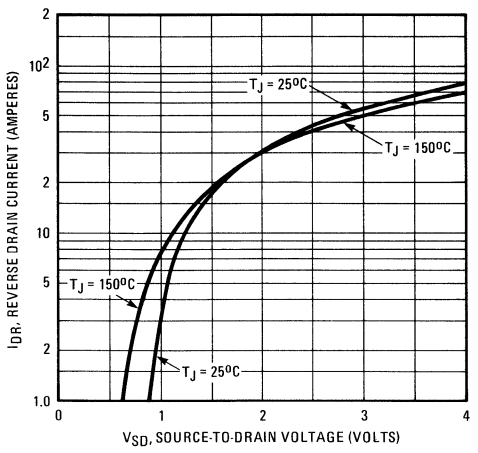


Fig. 7 — Typical Source-Drain Diode Forward Voltage

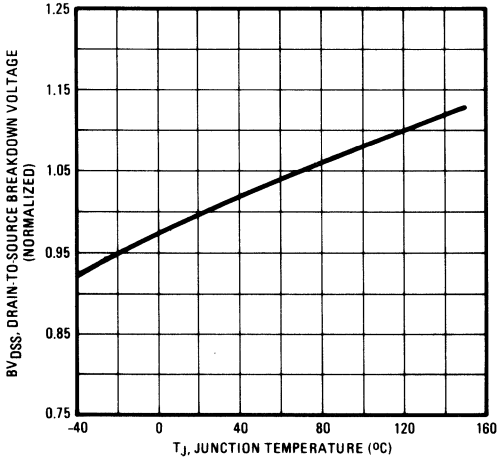


Fig. 8 — Breakdown Voltage Vs. Temperature

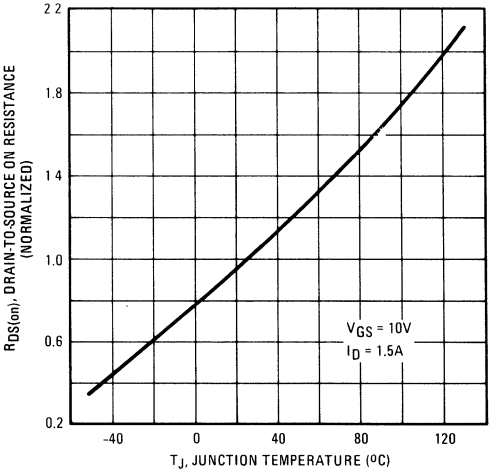


Fig. 9 — Normalized On-Resistance Vs. Temperature

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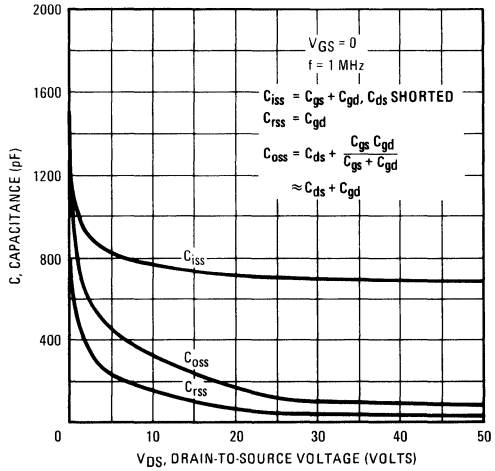


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

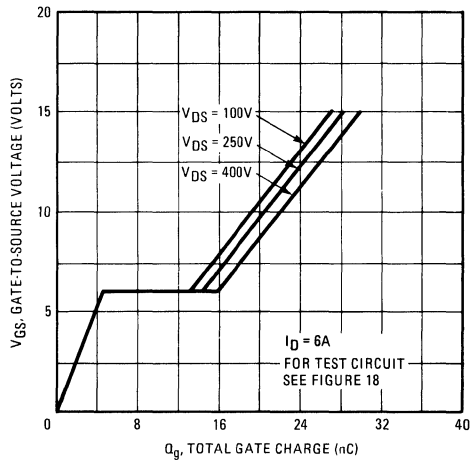


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

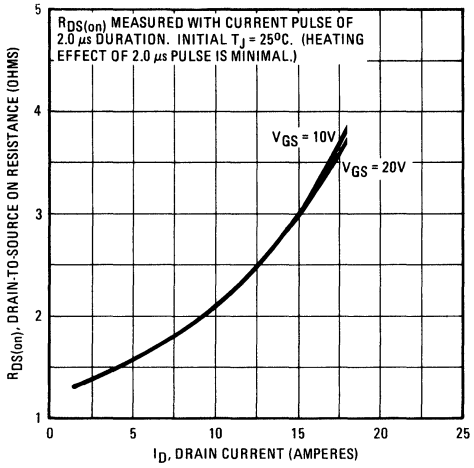


Fig. 12 — Typical On-Resistance Vs. Drain Current

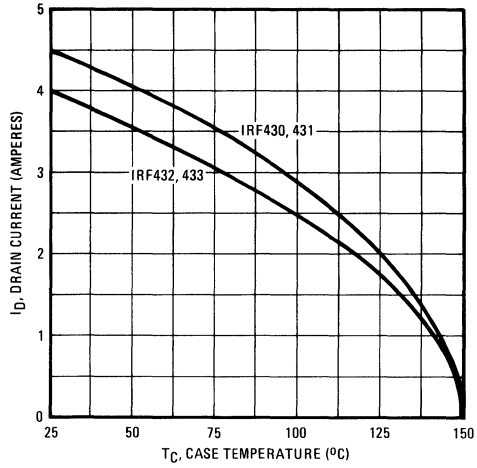


Fig. 13 — Maximum Drain Current Vs. Case Temperature

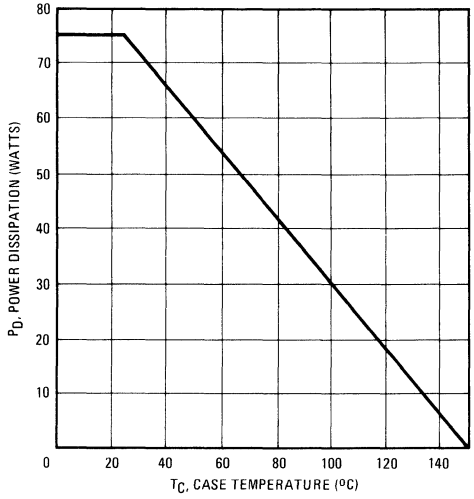


Fig. 14 — Power Vs. Temperature Derating Curve

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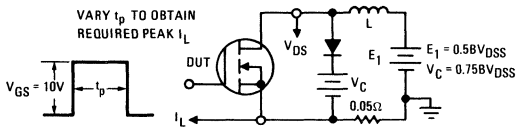


Fig. 15 — Clamped Inductive Test Circuit

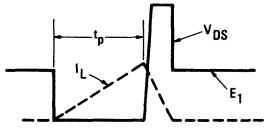


Fig. 16 — Clamped Inductive Waveforms

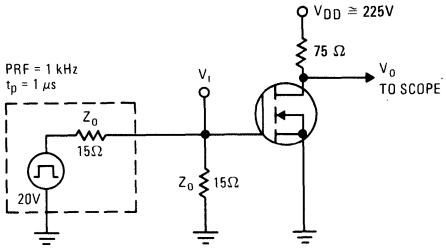


Fig. 17 — Switching Time Test Circuit

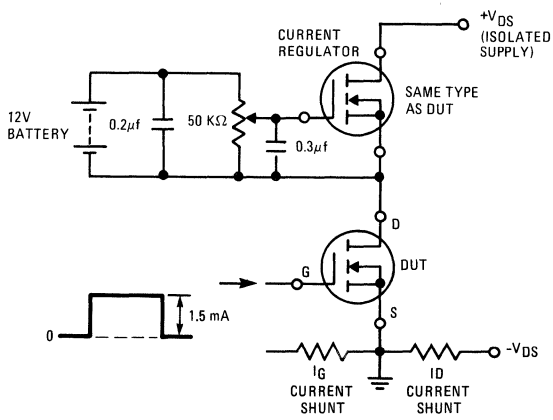


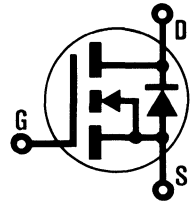
Fig. 18 — Gate Charge Test Circuit

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HEXFET® TRANSISTORS IRF440 IRF441 IRF442 IRF443

N-CHANNEL POWER MOSFETs



500 Volt, 0.85 Ohm HEXFET

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

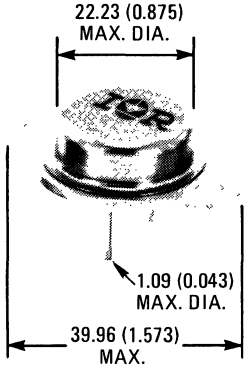
Features:

- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

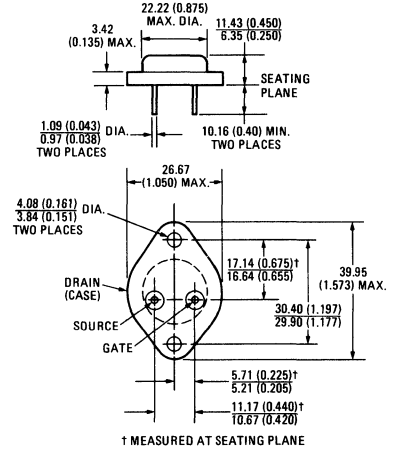
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF440	500V	0.85Ω	8.0A
IRF441	450V	0.85Ω	8.0A
IRF442	500V	1.10Ω	7.0A
IRF443	450V	1.10Ω	7.0A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



† MEASURED AT SEATING PLANE

Conforms to JEDEC Outline TO-204AA (TO-3)
Dimensions in Millimeters and (Inches)

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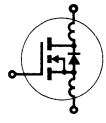
Absolute Maximum Ratings

Parameter		IRF440	IRF441	IRF442	IRF443	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_D @ T_C = 100°C	Continuous Drain Current	5.0	5.0	4.0	4.0	A
I_{DM}	Pulsed Drain Current ③	32	32	28	28	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		32	32	28	28	
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF440 IRF442	500	–	–	V	V_{GS} = 0V
		IRF441 IRF443	450	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	−100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF440 IRF441	8.0	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		IRF442 IRF443	7.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF440 IRF441	–	0.8	0.85	Ω	V_{GS} = 10V, I_D = 4.0A
		IRF442 IRF443	–	1.0	1.1	Ω	
g_{fs}	Forward Transconductance ②	ALL	4.0	6.5	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 4.0A
C_{iss}	Input Capacitance	ALL	–	1225	1600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	200	350	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	85	150	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	17	35	ns	$V_{DD} \approx$ 200V, I_D = 4.0A, Z_0 = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	5	15	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	42	90	ns	
t_f	Fall Time	ALL	–	14	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	42	60	nC	V_{GS} = 10V, I_D = 10A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	20	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	22	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.0	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF440 IRF441	–	–	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF442 IRF443	–	–	7.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF440 IRF441	–	–	32	A	
		IRF442 IRF443	–	–	28	A	
V_{SD}	Diode Forward Voltage ②	IRF440 IRF441	–	–	2.0	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
		IRF442 IRF443	–	–	1.9	V	T_C = 25°C, I_S = 7.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	1100	–	ns	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	6.4	–	μC	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

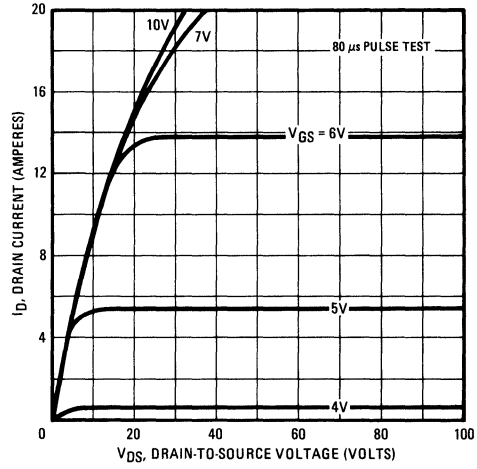


Fig. 1 – Typical Output Characteristics

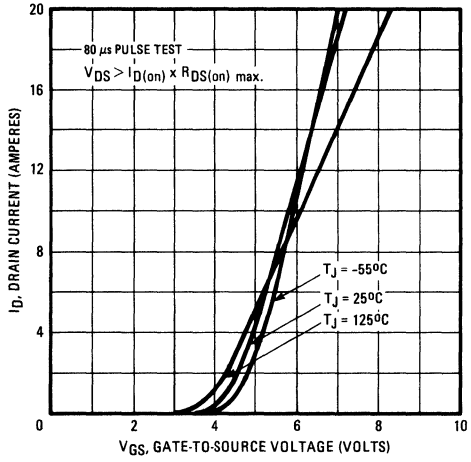


Fig. 2 – Typical Transfer Characteristics

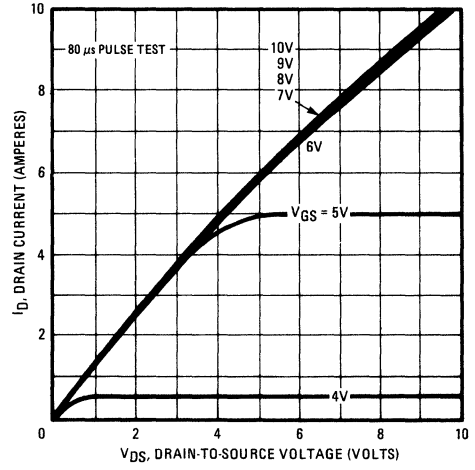


Fig. 3 – Typical Saturation Characteristics

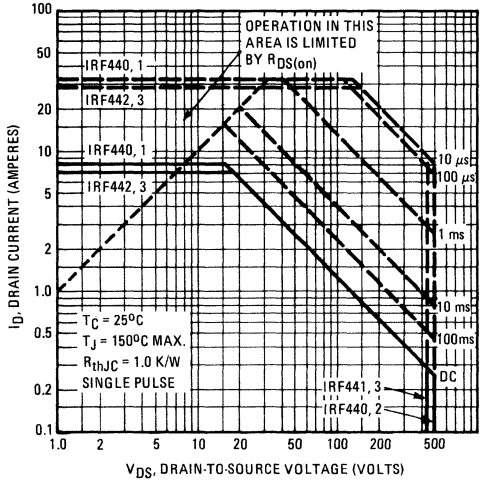


Fig. 4 – Maximum Safe Operating Area

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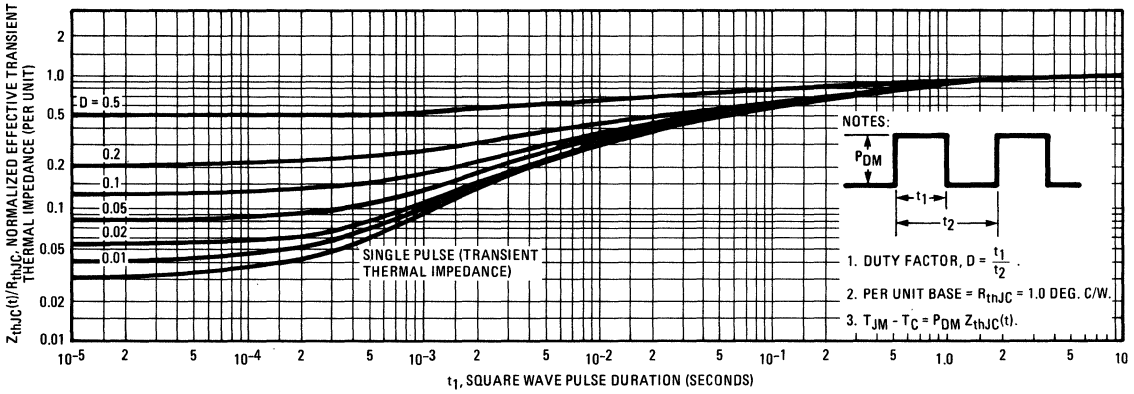


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

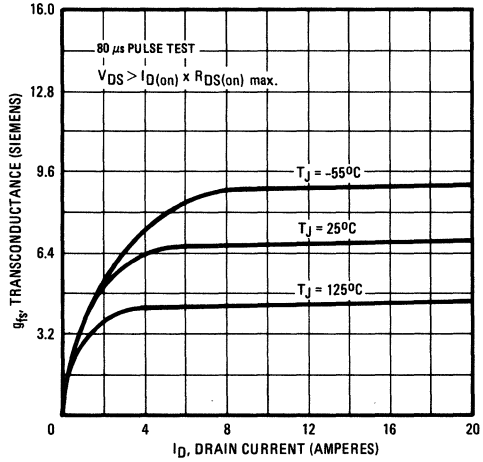


Fig. 6 — Typical Transconductance Vs. Drain Current

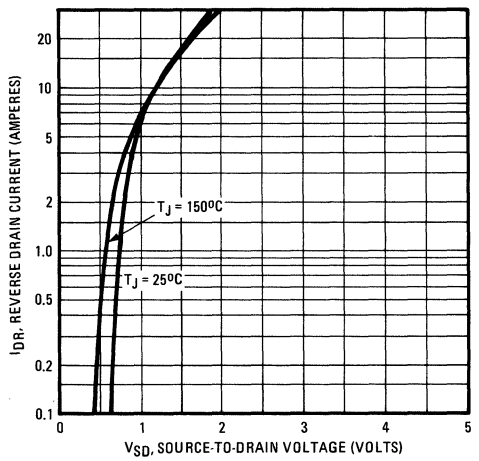


Fig. 7 — Typical Source-Drain Diode Forward Voltage

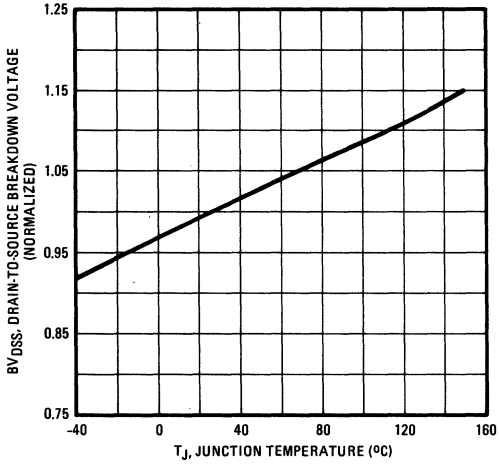


Fig. 8 — Breakdown Voltage Vs. Temperature

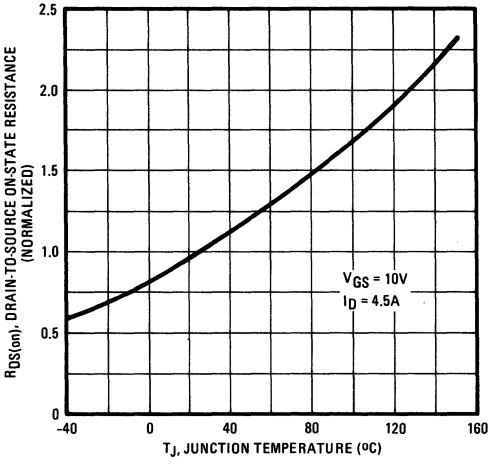


Fig. 9 — Normalized On-Resistance Vs. Temperature

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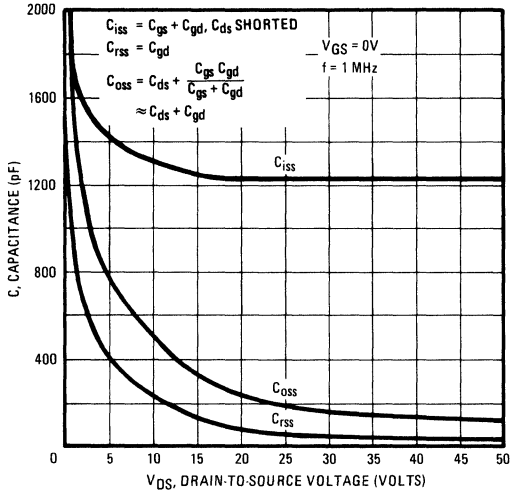


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

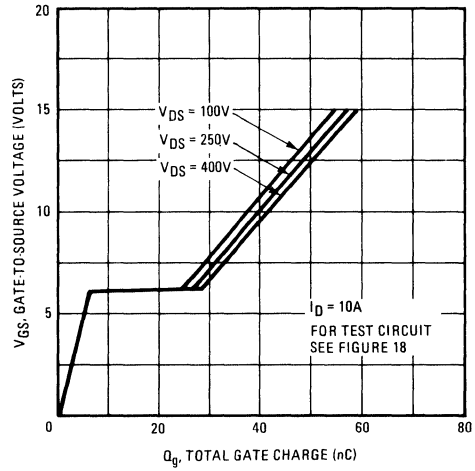


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

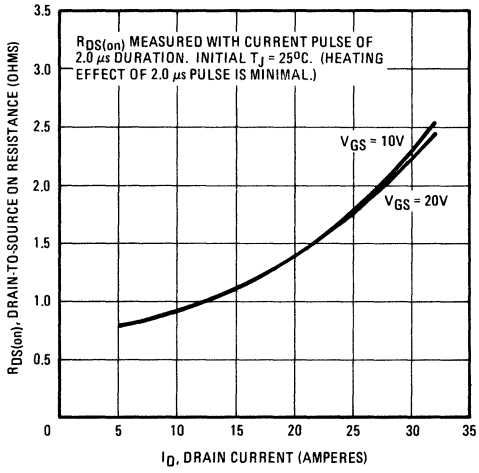


Fig. 12 — Typical On-Resistance Vs. Drain Current

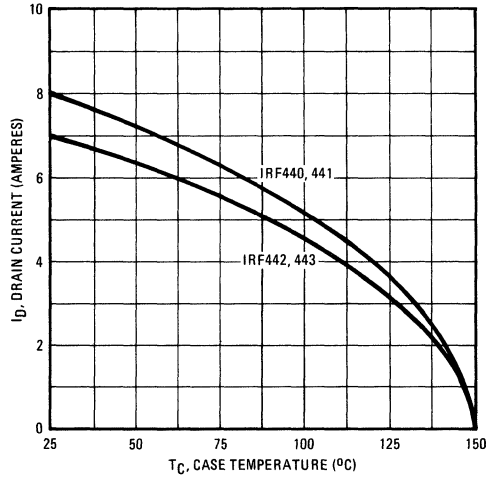


Fig. 13 — Maximum Drain Current Vs. Case Temperature

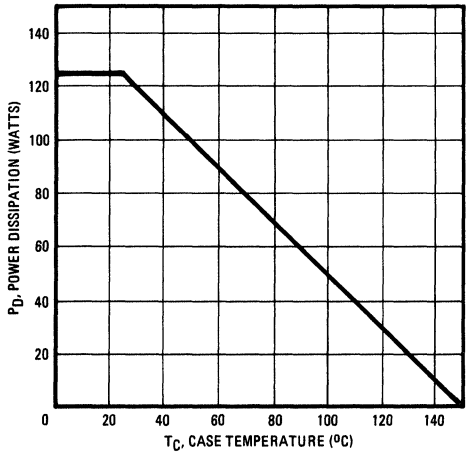


Fig. 14 — Power Vs. Temperature Derating Curve

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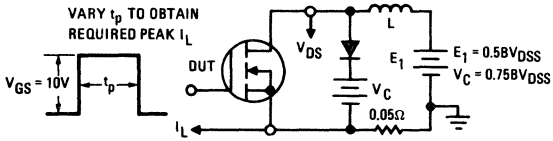


Fig. 15 — Clamped Inductive Test Circuit

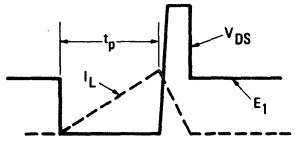


Fig. 16 — Clamped Inductive Waveforms

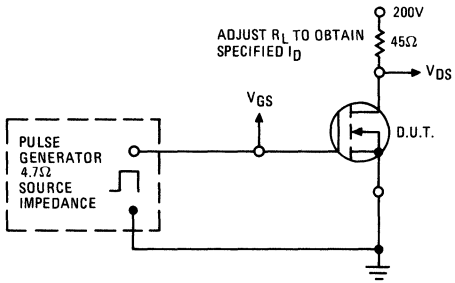


Fig. 17 — Switching Time Test Circuit

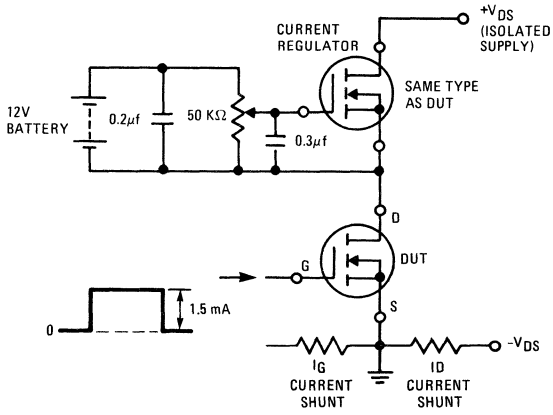


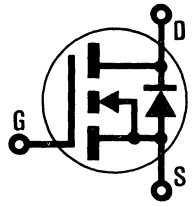
Fig. 18 — Gate Charge Test Circuit

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS

IRF450
IRF451
IRF452
IRF453



N-Channel

500 Volt, 0.4 Ohm HEXFET

The HEXFET® Technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

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They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

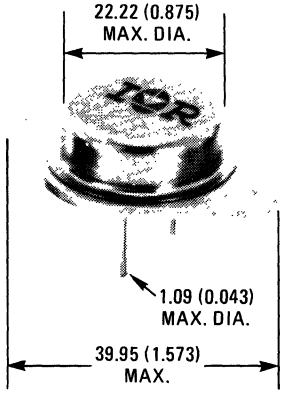
Features:

- Fast Switching
- Low Drive Current
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- No Second Breakdown
- Excellent Temperature Stability

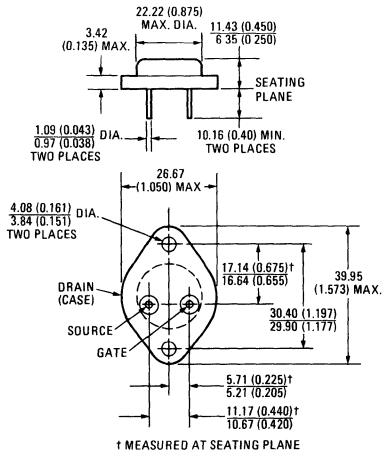
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF450	500V	0.4Ω	13A
IRF451	450V	0.4Ω	13A
IRF452	500V	0.5Ω	12A
IRF453	450V	0.5Ω	12A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Conforms to JEDEC Outline TO-204AA (TO-3)
Dimensions in Millimeters and (Inches)

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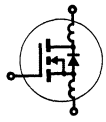
Absolute Maximum Ratings

Parameter		IRF450	IRF451	IRF452	IRF453	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	13	13	12	12	A
I_D @ T_C = 100°C	Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_{DM}	Pulsed Drain Current ③	52	52	48	48	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	150 (See Fig. 14)				W
	Linear Derating Factor	1.2 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 14 and 15) L = 100μH				A
		52	52	48	48	
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF450 IRF452	500	–	–	V	V_{GS} = 0V
		IRF451 IRF453	450	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF450 IRF451	13	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF452 IRF453	12	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF450 IRF451	–	0.3	0.4	Ω	V_{GS} = 10V, I_D = 7.0A
		IRF452 IRF453	–	0.4	0.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	6.0	11	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 7.0A
C_{iss}	Input Capacitance	ALL	–	2000	3000	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	400	600	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	100	200	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	35	ns	V_{DD} ≃ 210V, I_D = 7.0A, Z_O = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	150	ns	
t_f	Fall Time	ALL	–	–	70	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	82	120	nC	V_{GS} = 10V, I_D = 16A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	40	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	42	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	.83	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

Downloaded from Arrow.com.

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF450 IRF451	–	–	13	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF452 IRF453	–	–	12	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF450 IRF451	–	–	52	A	
		IRF452 IRF453	–	–	48	A	
V_{SD}	Diode Forward Voltage ②	IRF450 IRF451	–	–	1.4	V	T_C = 25°C, I_S = 13A, V_{GS} = 0V
		IRF452 IRF453	–	–	1.3	V	T_C = 25°C, I_S = 12A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	1300	–	ns	T_J = 150°C, I_F = 13A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	7.4	–	μC	T_J = 150°C, I_F = 13A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

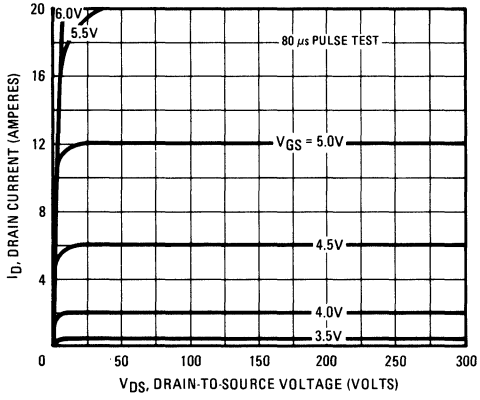


Fig. 1 — Typical Output Characteristics

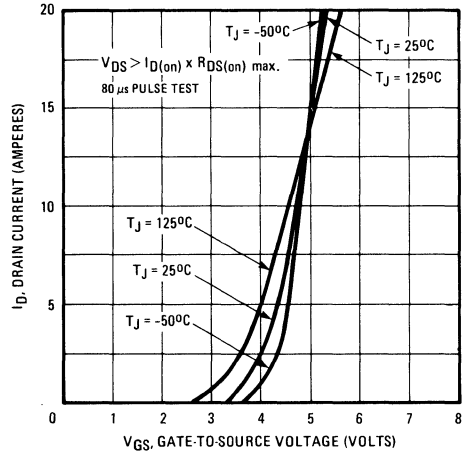


Fig. 2 — Typical Transfer Characteristics

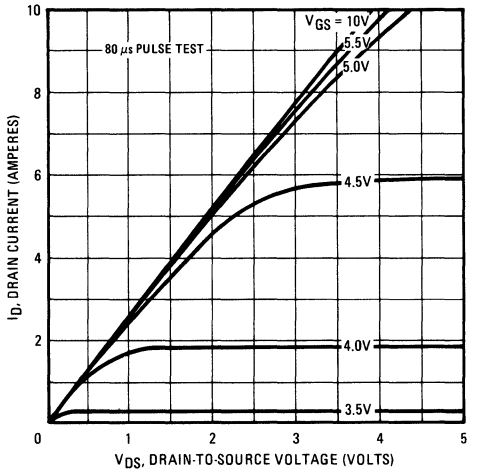


Fig. 3 — Typical Saturation Characteristics

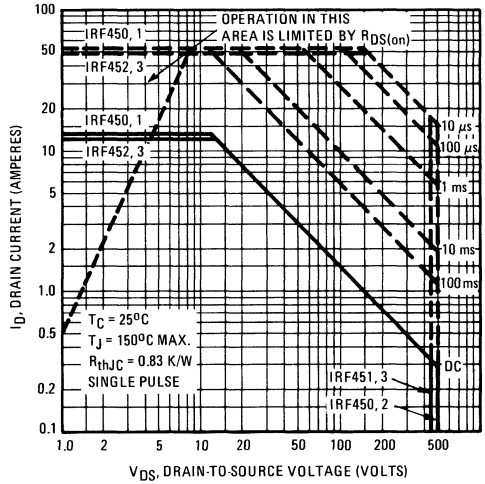


Fig. 4 — Maximum Safe Operating Area

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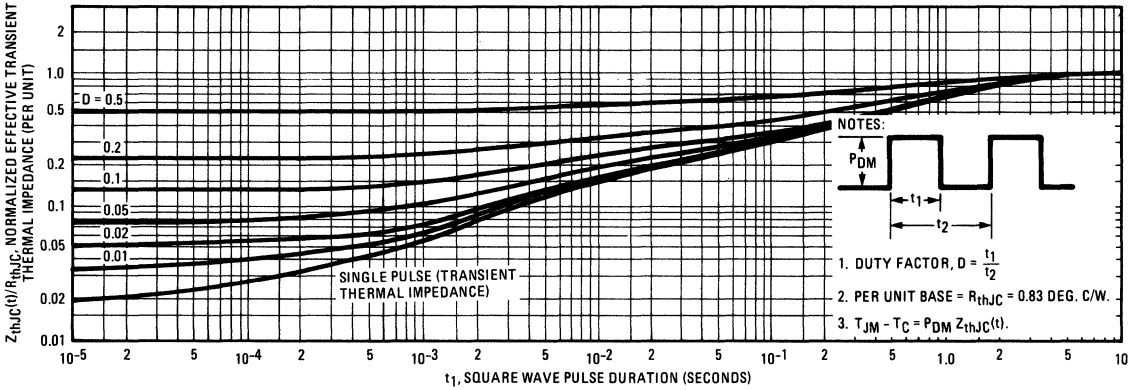


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

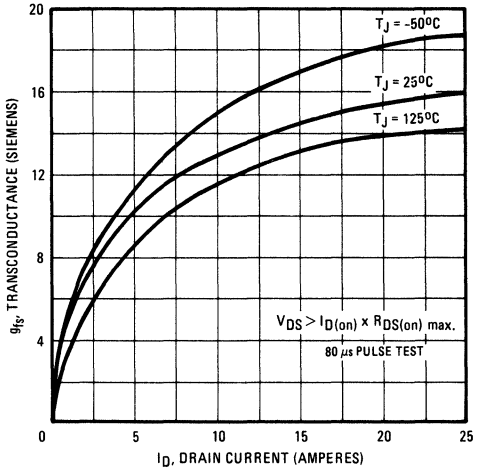


Fig. 6 — Typical Transconductance Vs. Drain Current

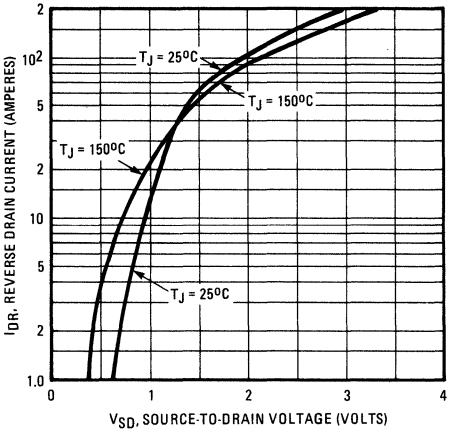


Fig. 7 — Typical Source-Drain Diode Forward Voltage

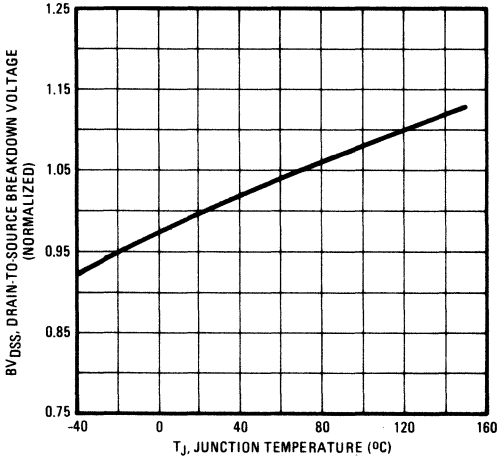


Fig. 8 — Breakdown Voltage Vs. Temperature

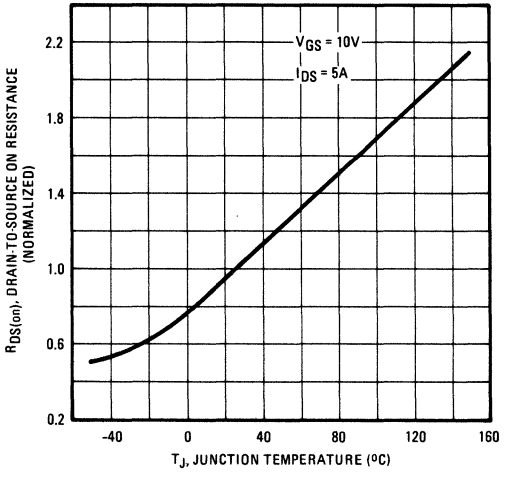


Fig. 9 — Normalized On-Resistance Vs. Temperature

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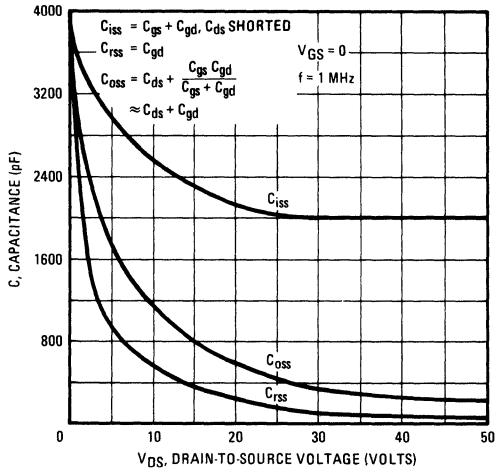


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

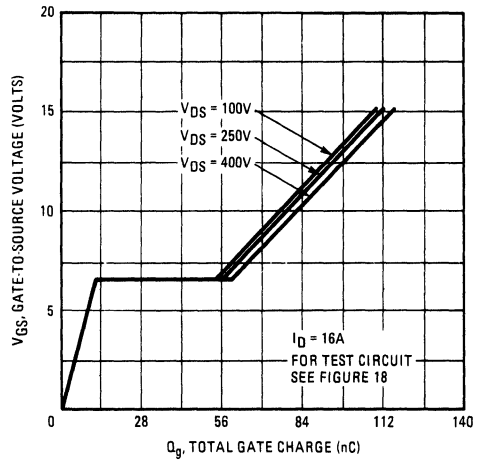


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

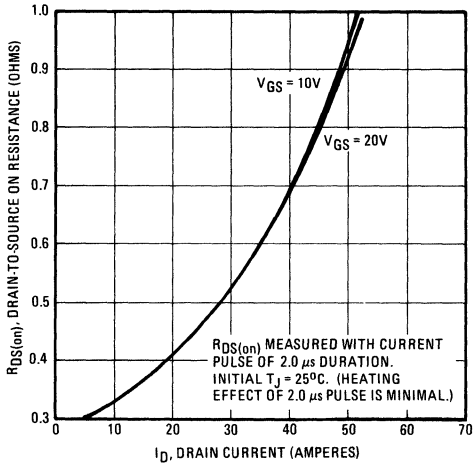


Fig. 12 — Typical On-Resistance Vs. Drain Current

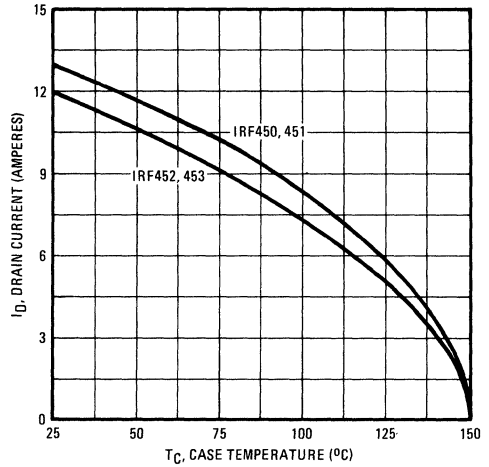


Fig. 13 — Maximum Drain Current Vs. Case Temperature

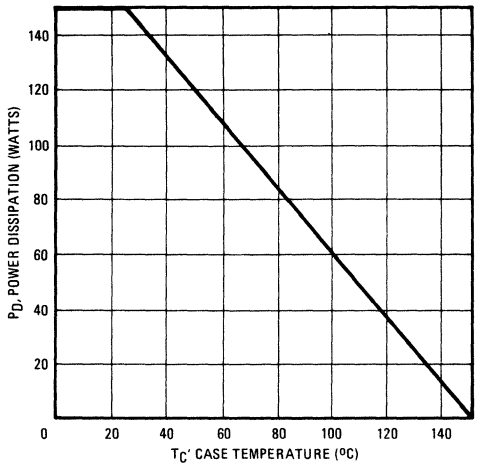


Fig. 14 — Power Vs. Temperature Derating Curve

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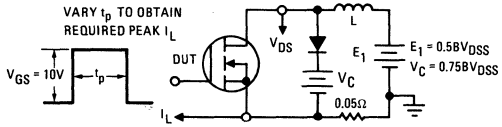


Fig. 15 — Clamped Inductive Test Circuit

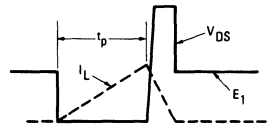


Fig. 16 — Clamped Inductive Waveforms

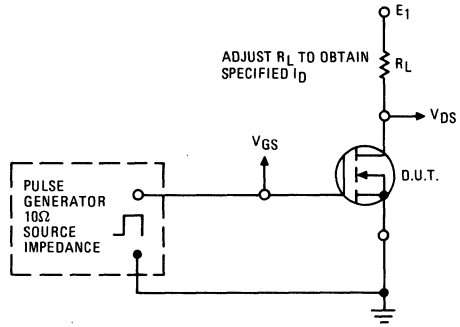


Fig. 17 — Switching Time Test Circuit

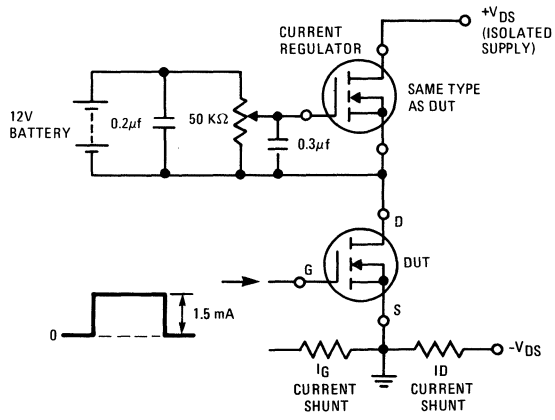


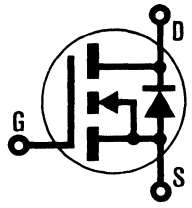
Fig. 18 — Gate Charge Test Circuit

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS

IRF510
IRF511
IRF512
IRF513



N-Channel

100 Volt, 0.6 Ohm HEXFET TO-220AB Plastic Package

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

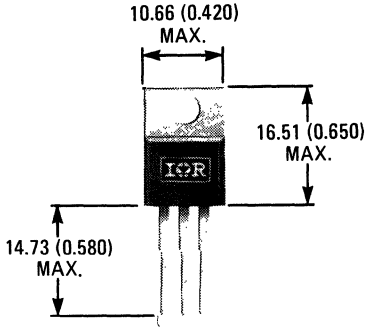
Features:

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

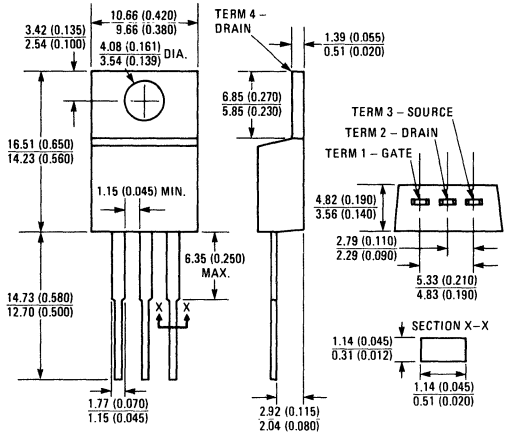
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF510	100V	0.6Ω	4.0A
IRF511	60V	0.6Ω	4.0A
IRF512	100V	0.8Ω	3.5A
IRF513	60V	0.8Ω	3.5A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Case Style TO-220AB
Dimensions in Millimeters and (Inches)

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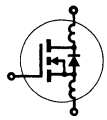
Absolute Maximum Ratings

Parameter		IRF510	IRF511	IRF512	IRF513	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	4.0	4.0	3.5	3.5	A
I_D @ T_C = 100°C	Continuous Drain Current	2.5	2.5	2.0	2.0	A
I_{DM}	Pulsed Drain Current ③	16	16	14	14	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	20 (See Fig. 14)				W
	Linear Derating Factor	0.16 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		16	16	14	14	
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF510 IRF512	100	–	–	V	V_{GS} = 0V
		IRF511 IRF513	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF510 IRF511	4.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF512 IRF513	3.5	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF510 IRF511	–	0.5	0.6	Ω	V_{GS} = 10V, I_D = 2.0A
		IRF512 IRF513	–	0.6	0.8	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	1.5	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 2.0A
C_{iss}	Input Capacitance	ALL	–	135	150	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	80	100	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	20	25	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	10	20	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 2.0A, Z_0 = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	15	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	15	25	ns	
t_f	Fall Time	ALL	–	10	20	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	5.0	7.5	nC	V_{GS} = 10V, I_D = 8.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	2.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	3.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	6.4	K/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF510 IRF511	–	–	4.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF512 IRF513	–	–	3.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF510 IRF511	–	–	16	A	
		IRF512 IRF513	–	–	14	A	
V_{SD}	Diode Forward Voltage ②	IRF510 IRF511	–	–	2.5	V	T_C = 25°C, I_S = 4.0A, V_{GS} = 0V
		IRF512 IRF513	–	–	2.0	V	T_C = 25°C, I_S = 3.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	230	–	ns	T_J = 150°C, I_F = 4.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	1.4	–	μC	T_J = 150°C, I_F = 4.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

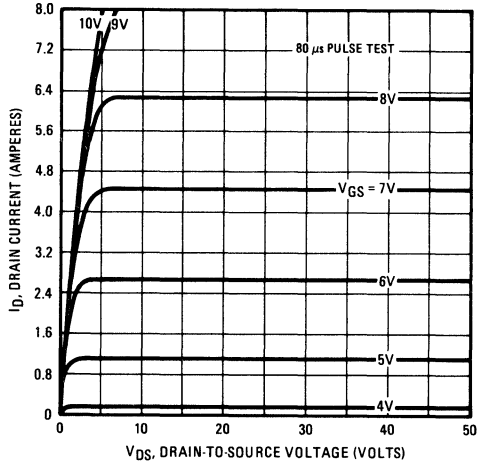


Fig. 1 — Typical Output Characteristics

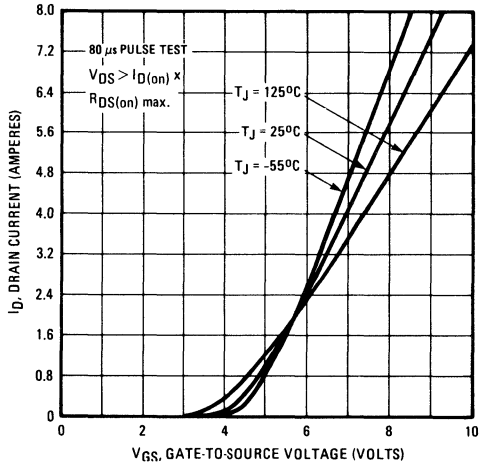


Fig. 2 — Typical Transfer Characteristics

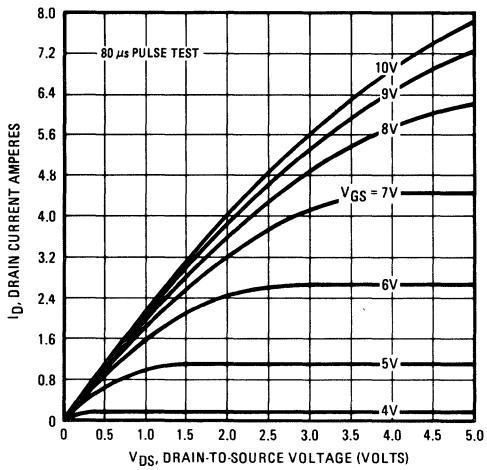


Fig. 3 — Typical Saturation Characteristics

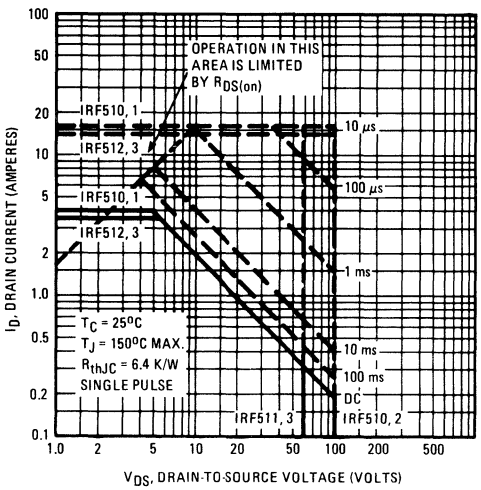


Fig. 4 — Maximum Safe Operating Area

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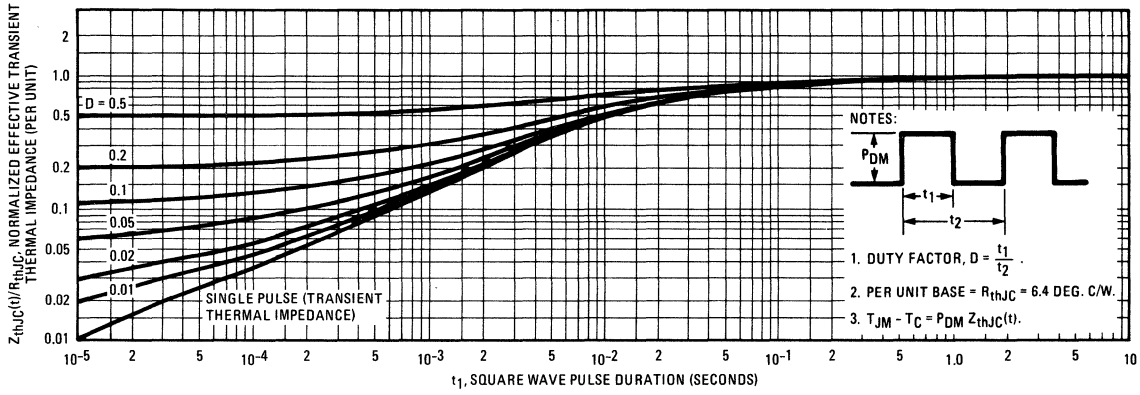


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

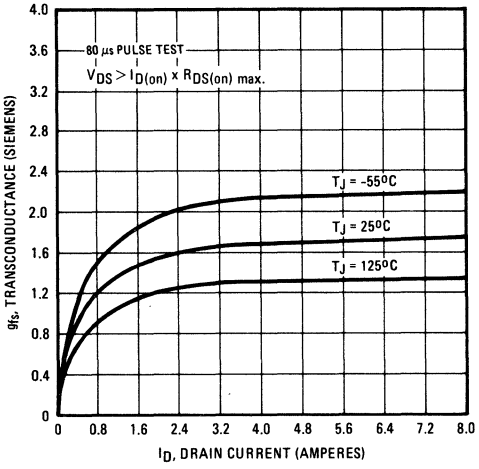


Fig. 6 – Typical Transconductance Vs. Drain Current

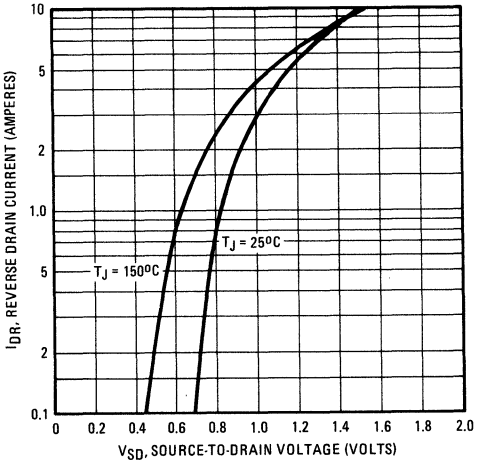


Fig. 7 – Typical Source-Drain Diode Forward Voltage

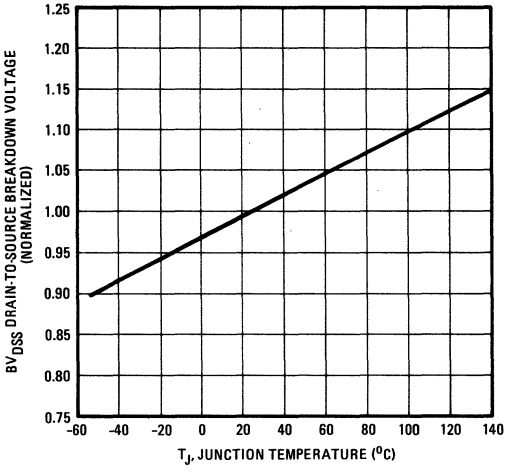


Fig. 8 – Breakdown Voltage Vs. Temperature

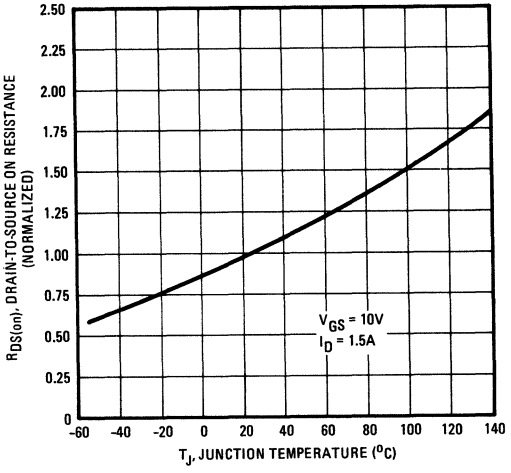


Fig. 9 – Normalized On-Resistance Vs. Temperature

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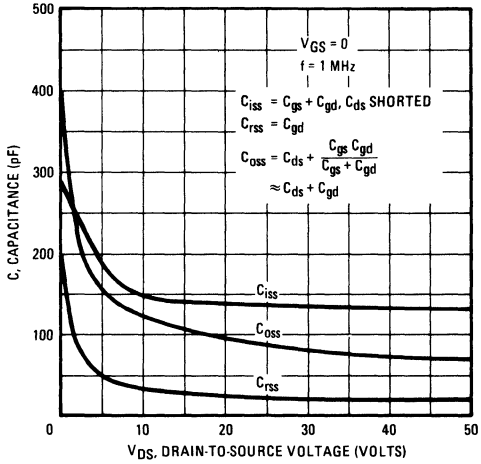


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

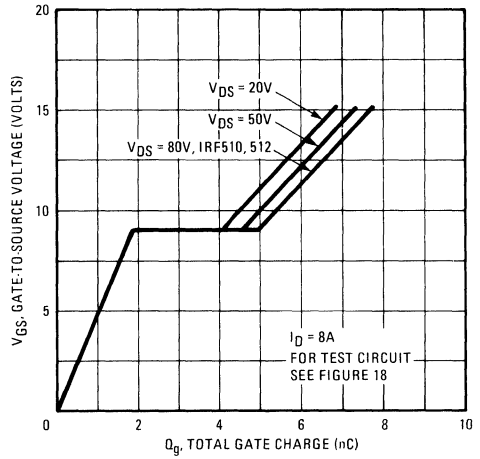


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

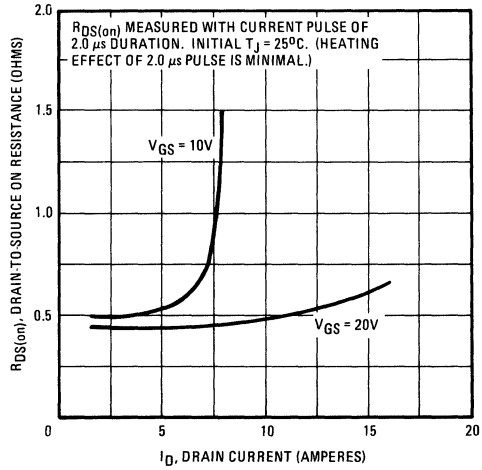


Fig. 12 — Typical On-Resistance Vs. Drain Current

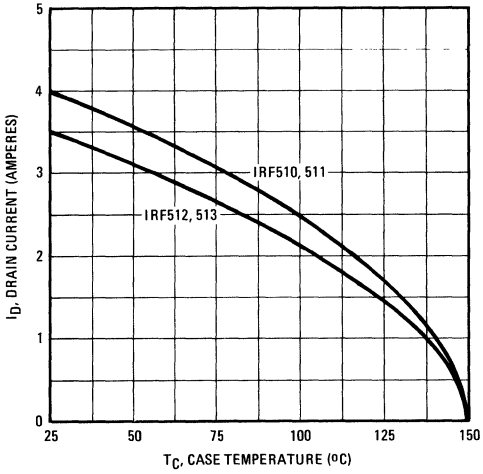


Fig. 13 — Maximum Drain Current Vs. Case Temperature

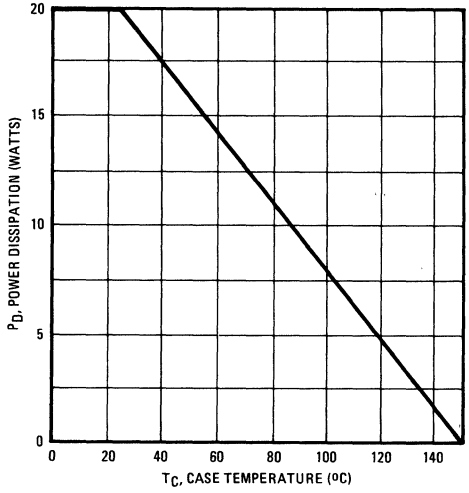


Fig. 14 — Power Vs. Temperature Derating Curve

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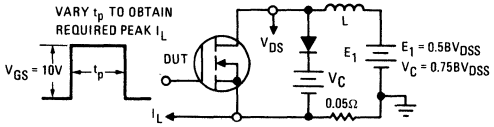


Fig. 15 — Clamped Inductive Test Circuit

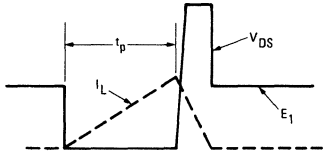


Fig. 16 — Clamped Inductive Waveforms

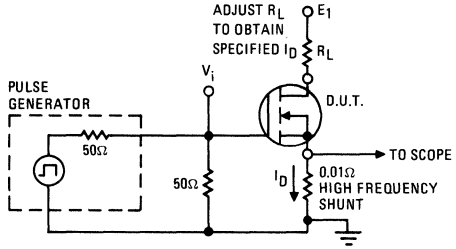


Fig. 17 — Switching Time Test Circuit

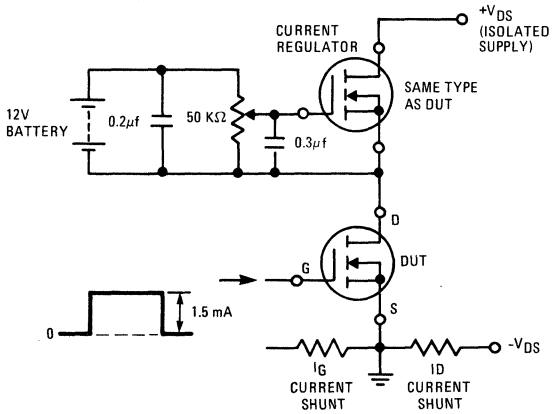


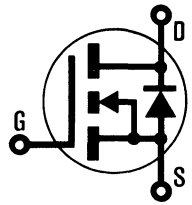
Fig. 18 — Gate Charge Test Circuit

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS

IRF520
IRF521
IRF522
IRF523



N-Channel

100 Volt, 0.3 Ohm HEXFET TO-220AB Plastic Package

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

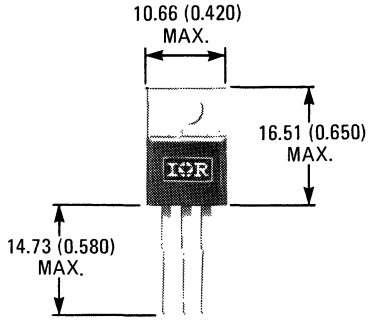
Features:

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

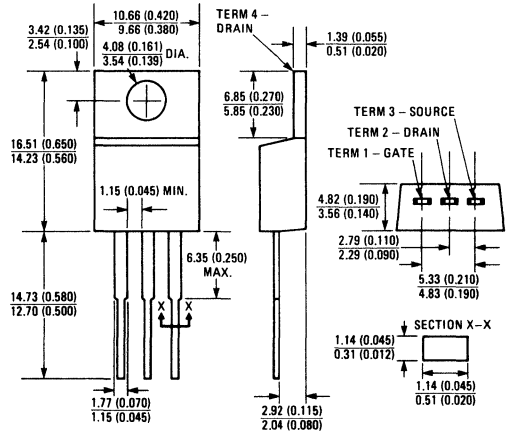
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF520	100V	0.30Ω	8.0A
IRF521	60V	0.30Ω	8.0A
IRF522	100V	0.40Ω	7.0A
IRF523	60V	0.40Ω	7.0A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Case Style TO-220AB
Dimensions in Millimeters and (Inches)

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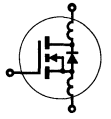
Absolute Maximum Ratings

Parameter		IRF520	IRF521	IRF522	IRF523	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_D @ T_C = 100°C	Continuous Drain Current	5.0	5.0	4.0	4.0	A
I_{DM}	Pulsed Drain Current ③	32	32	28	28	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	32	(See Fig. 15 and 16) L = 100μH 32	28	28	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF520 IRF522	100	–	–	V	V_{GS} = 0V
		IRF521 IRF523	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF520 IRF521	8.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF522 IRF523	7.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF520 IRF521	–	0.25	0.30	Ω	V_{GS} = 10V, I_D = 4.0A
		IRF522 IRF523	–	0.30	0.40	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.5	2.9	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 4.0A
C_{iss}	Input Capacitance	ALL	–	450	600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	200	400	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	50	100	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} ≅ 0.5 BV_{DSS}, I_D = 4.0A, Z_0 = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	35	70	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	35	70	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	10	15	nC	V_{GS} = 15V, I_D = 10A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	6.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	4.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	3.12	K/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF520 IRF521	–	–	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF522 IRF523	–	–	7.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF520 IRF521	–	–	32	A	
		IRF522 IRF523	–	–	28	A	
V_{SD}	Diode Forward Voltage ②	IRF520 IRF521	–	–	2.5	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
		IRF522 IRF523	–	–	2.3	V	T_C = 25°C, I_S = 7.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	280	–	ns	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	1.6	–	μC	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

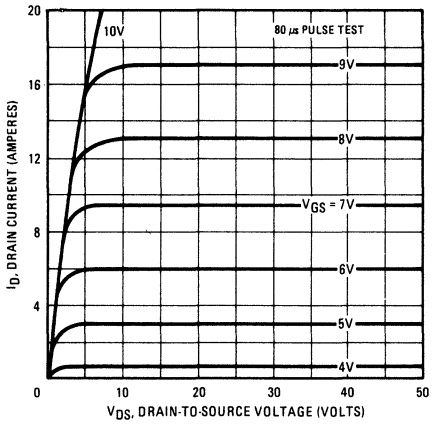


Fig. 1 – Typical Output Characteristics

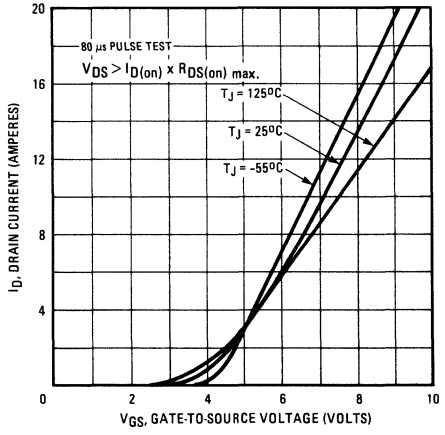


Fig. 2 – Typical Transfer Characteristics

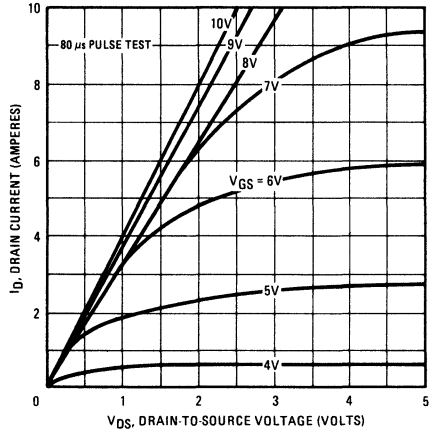


Fig. 3 – Typical Saturation Characteristics

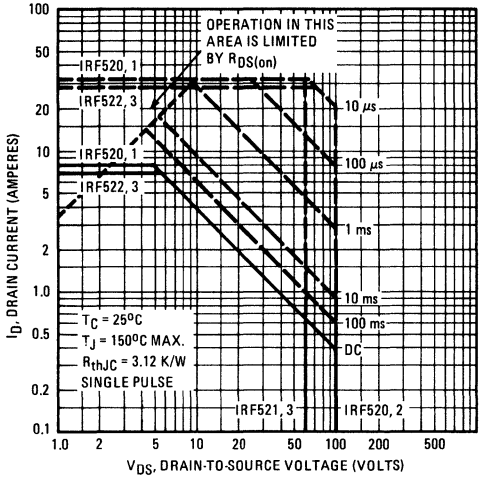


Fig. 4 – Maximum Safe Operating Area

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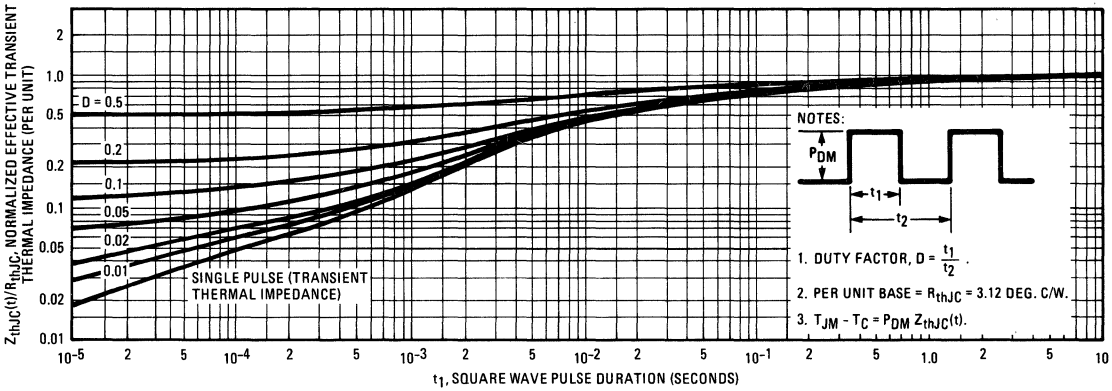


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

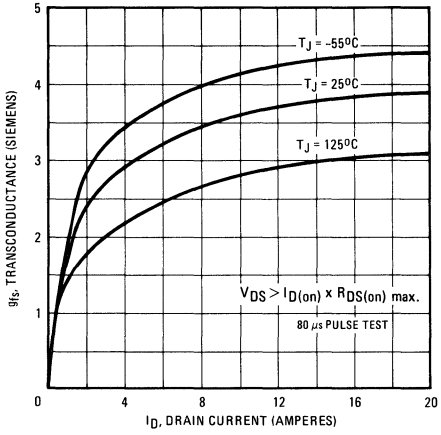


Fig. 6 — Typical Transconductance Vs. Drain Current

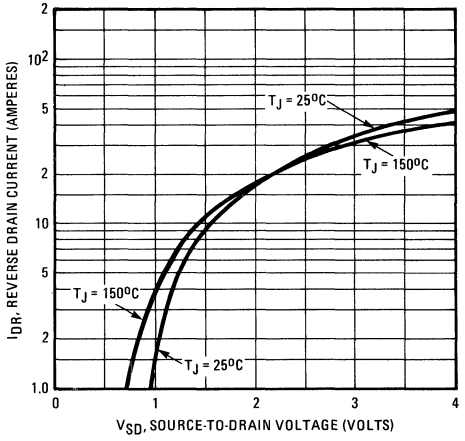


Fig. 7 — Typical Source-Drain Diode Forward Voltage

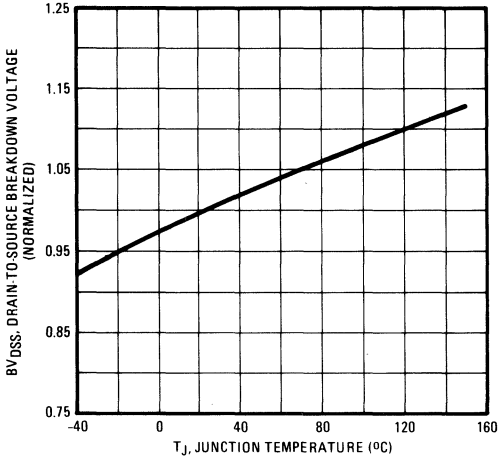


Fig. 8 — Breakdown Voltage Vs. Temperature

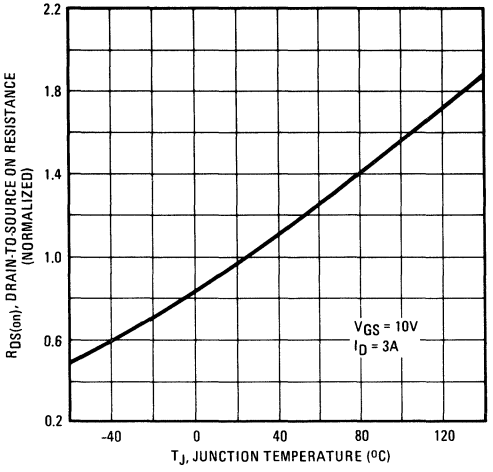


Fig. 9 — Normalized On-Resistance Vs. Temperature

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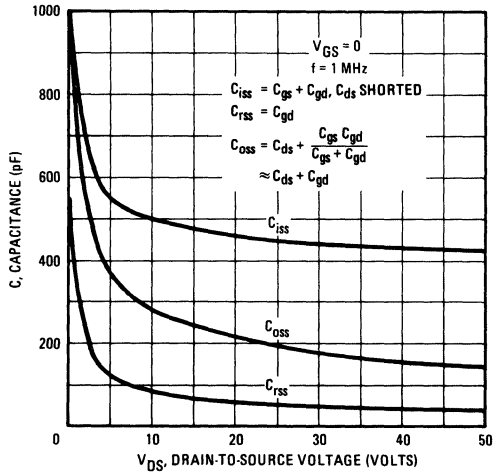


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

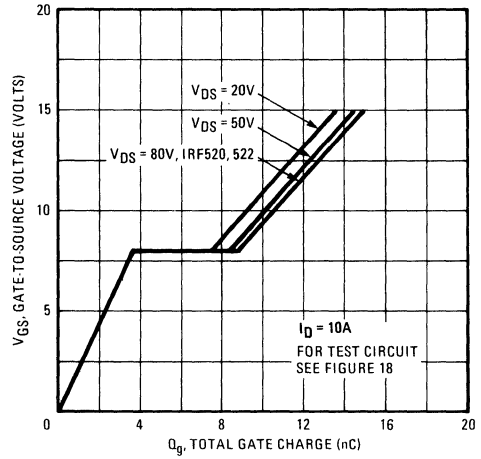


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

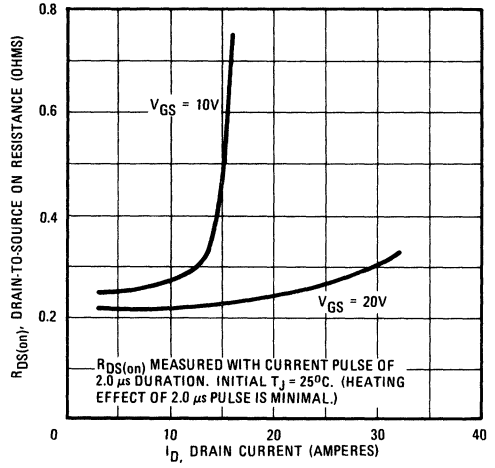


Fig. 12 — Typical On-Resistance Vs. Drain Current

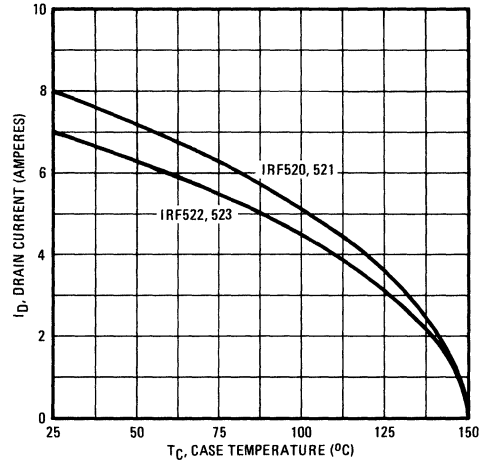


Fig. 13 — Maximum Drain Current Vs. Case Temperature

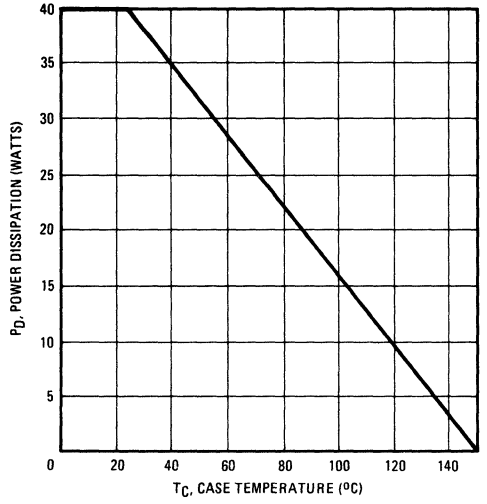


Fig. 14 — Power Vs. Temperature Derating Curve

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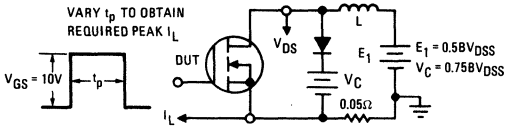


Fig. 15 — Clamped Inductive Test Circuit

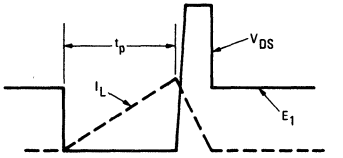


Fig. 16 — Clamped Inductive Waveforms

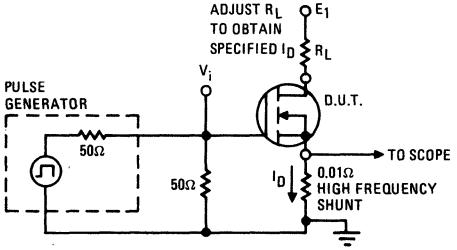


Fig. 17 — Switching Time Test Circuit

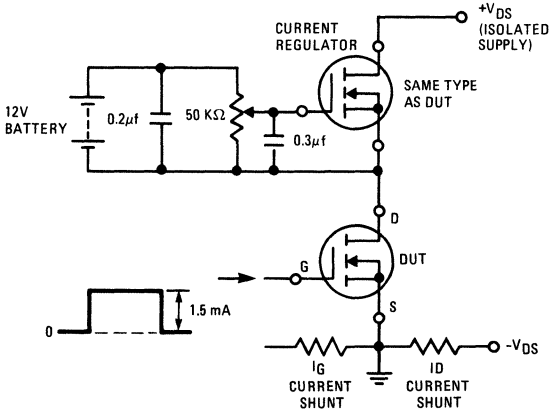


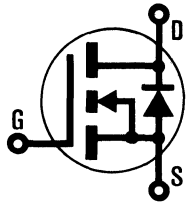
Fig. 18 — Gate Charge Test Circuit

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS

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N-Channel

100 Volt, 0.18 Ohm HEXFET TO-220AB Plastic Package

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They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

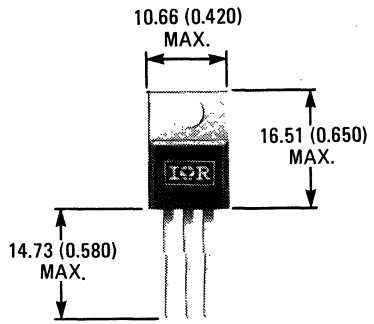
Features:

- Compact Plastic Package
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- No Second Breakdown
- Excellent Temperature Stability

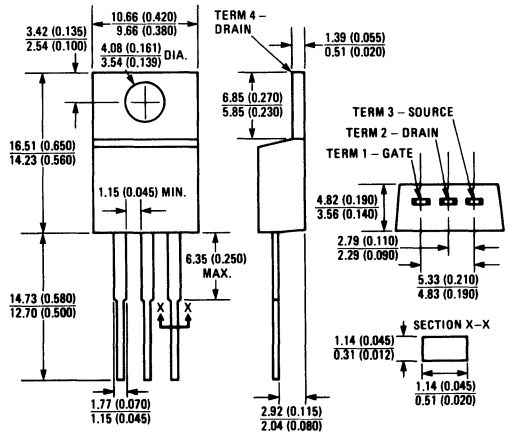
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF530	100V	0.18Ω	14A
IRF531	60V	0.18Ω	14A
IRF532	100V	0.25Ω	12A
IRF533	60V	0.25Ω	12A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Case Style TO-220AB
Dimensions in Millimeters and (Inches)

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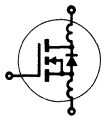
Absolute Maximum Ratings

Parameter		IRF530	IRF531	IRF532	IRF533	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	14	14	12	12	A
I_D @ T_C = 100°C	Continuous Drain Current	9.0	9.0	8.0	8.0	A
I_{DM}	Pulsed Drain Current ③	56	56	48	48	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		56	56	48	48	
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF530 IRF532	100	—	—	V	V_{GS} = 0V
		IRF531 IRF533	60	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	−500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF530 IRF531	14	—	—	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF532 IRF533	12	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF530 IRF531	—	0.14	0.18	Ω	V_{GS} = 10V, I_D = 8.0A
		IRF532 IRF533	—	0.20	0.25	Ω	
g_{fs}	Forward Transconductance ②	ALL	4.0	5.5	—	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 8.0A
C_{iss}	Input Capacitance	ALL	—	600	800	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	300	500	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	100	150	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	—	30	ns	V_{DD} ≈ 36V, I_D = 8.0A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	—	75	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	—	40	ns	
t_f	Fall Time	ALL	—	—	45	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	18	30	nC	V_{GS} = 10V, I_D = 18A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	9.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	9.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.
			—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	1.67	K/W	
R_{thCS}	Case-to-Sink	ALL	—	1.0	—	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF530 IRF531	–	–	14	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF532 IRF533	–	–	12	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF530 IRF531	–	–	56	A	
		IRF532 IRF533	–	–	48	A	
V_{SD}	Diode Forward Voltage ②	IRF530 IRF531	–	–	2.5	V	T_C = 25°C, I_S = 14A, V_{GS} = 0V
		IRF532 IRF533	–	–	2.3	V	T_C = 25°C, I_S = 12A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	360	–	ns	T_J = 150°C, I_F = 14A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	2.1	–	μC	T_J = 150°C, I_F = 14A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

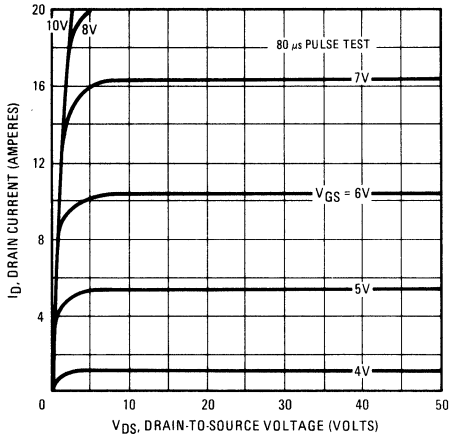


Fig. 1 — Typical Output Characteristics

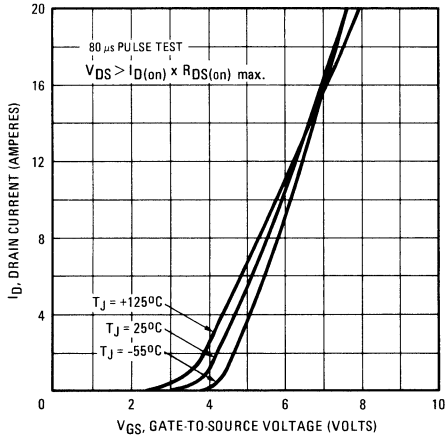


Fig. 2 — Typical Transfer Characteristics

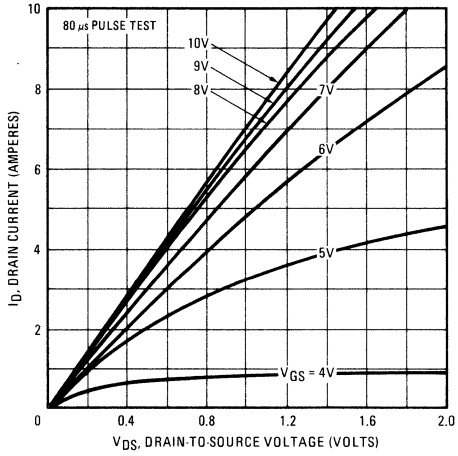


Fig. 3 — Typical Saturation Characteristics

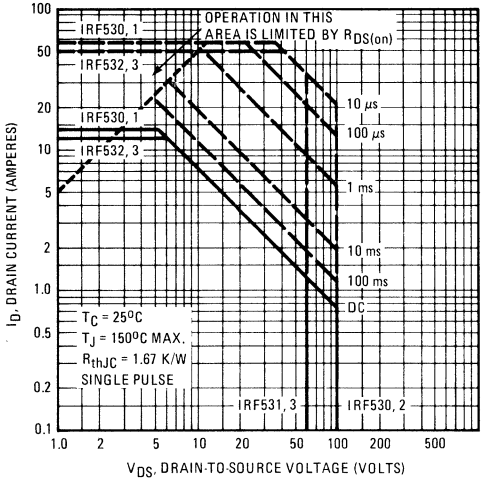


Fig. 4 — Maximum Safe Operating Area

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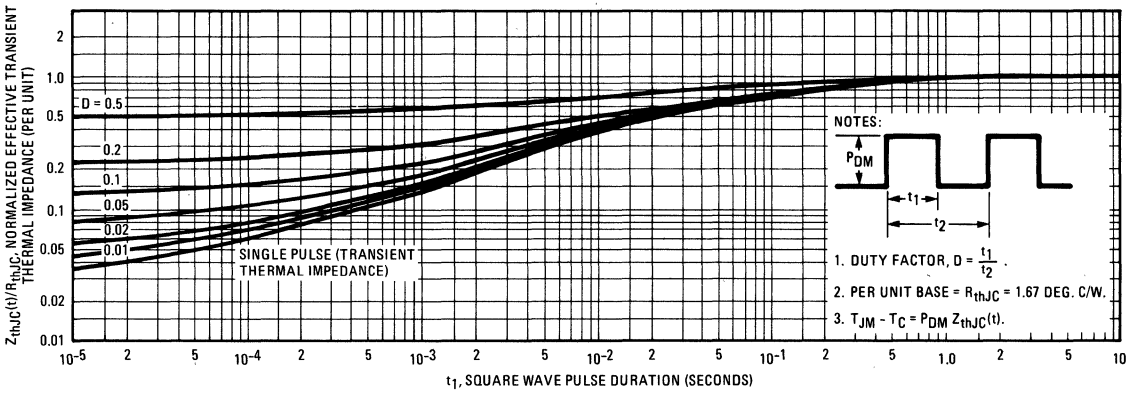


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

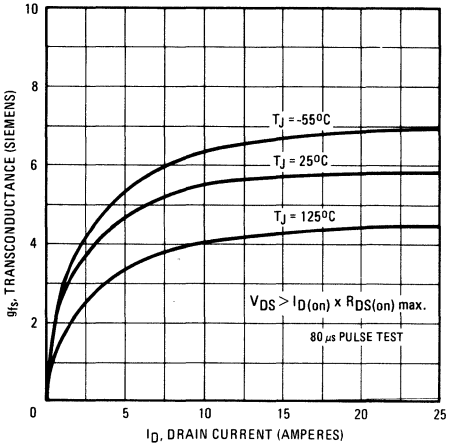


Fig. 6 — Typical Transconductance Vs. Drain Current

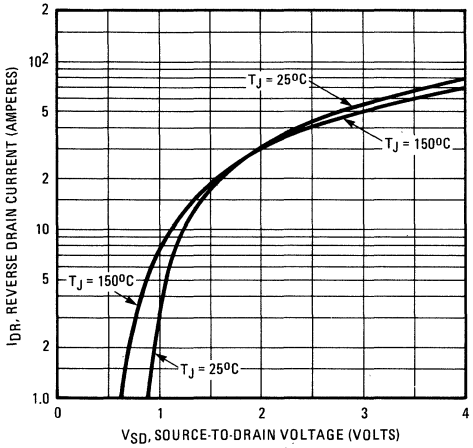


Fig. 7 — Typical Source-Drain Diode Forward Voltage

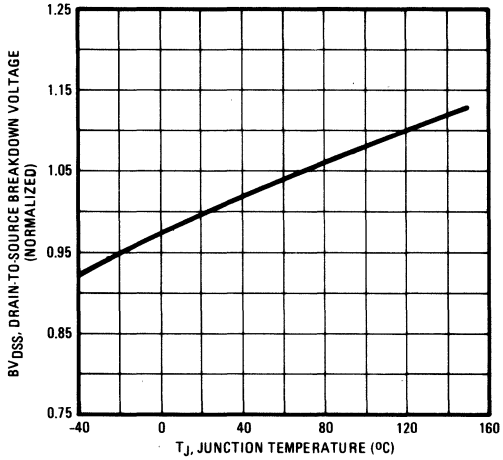


Fig. 8 — Breakdown Voltage Vs. Temperature

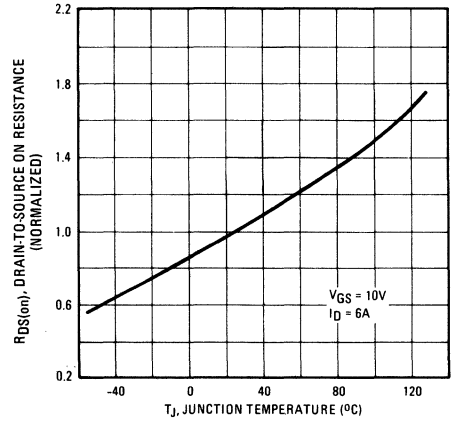


Fig. 9 — Normalized On-Resistance Vs. Temperature

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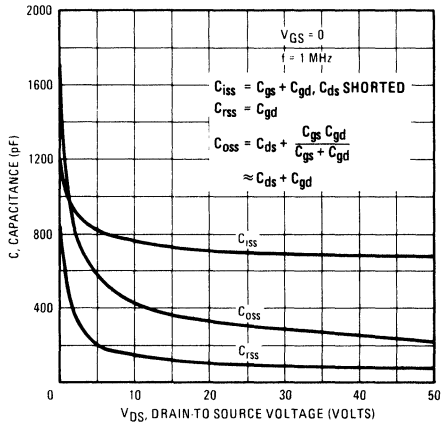


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

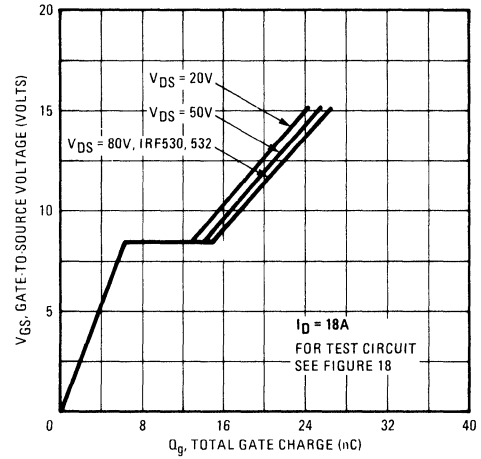


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

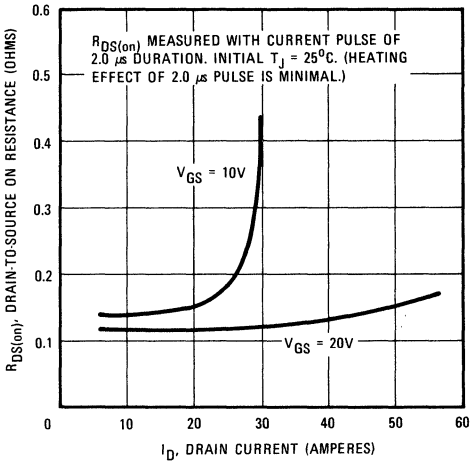


Fig. 12 — Typical On-Resistance Vs. Drain Current

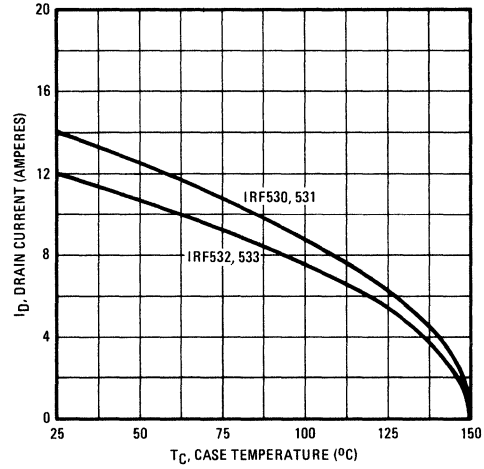


Fig. 13 — Maximum Drain Current Vs. Case Temperature

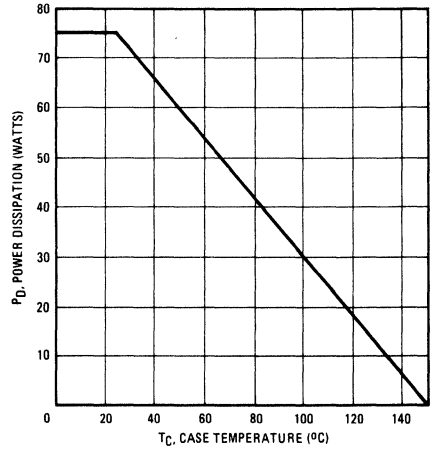


Fig. 14 — Power Vs. Temperature Derating Curve

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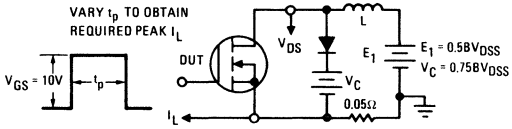


Fig. 15 — Clamped Inductive Test Circuit

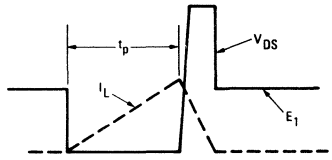


Fig. 16 — Clamped Inductive Waveforms

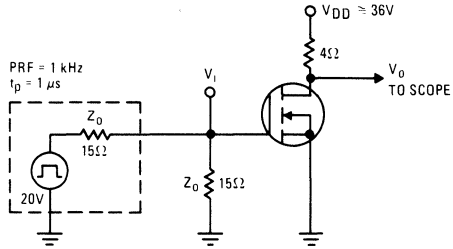


Fig. 17 — Switching Time Test Circuit

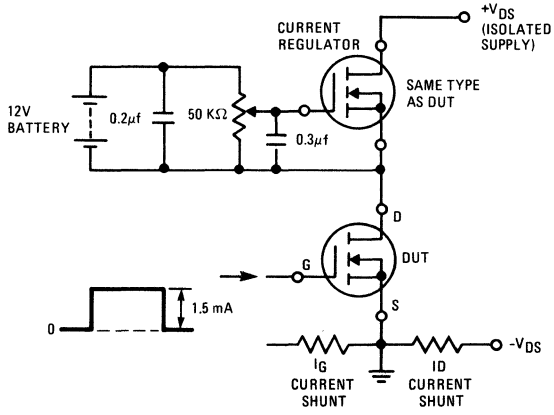


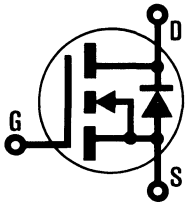
Fig. 18 — Gate Charge Test Circuit

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS

N-CHANNEL POWER MOSFETs



IRF540
IRF541
IRF542
IRF543

100 Volt, 0.085 Ohm HEXFET TO-220AB Plastic Package

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

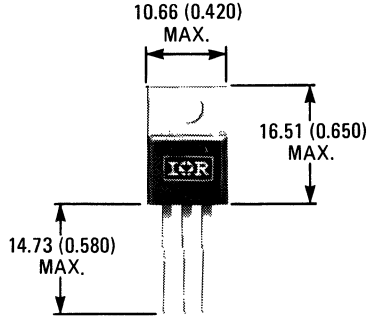
Features:

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

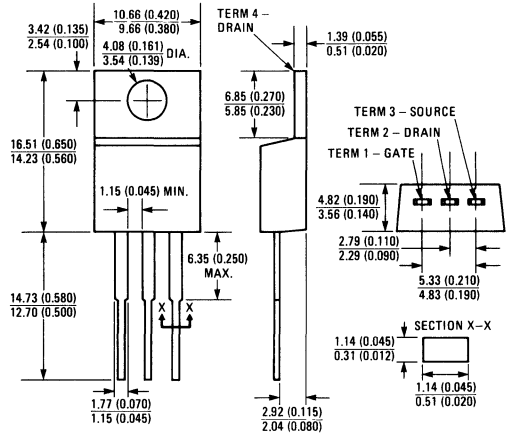
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF540	100V	0.085Ω	27A
IRF541	60V	0.085Ω	27A
IRF542	100V	0.11Ω	24A
IRF543	60V	0.11Ω	24A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Case Style TO-220AB
Dimensions in Millimeters and (Inches)

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IRF540, IRF541, IRF542, IRF543 Devices

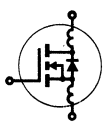
Absolute Maximum Ratings

Parameter		IRF540	IRF541	IRF542	IRF543	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	27	27	24	24	A
I_D @ T_C = 100°C	Continuous Drain Current	17	17	15	15	A
I_{DM}	Pulsed Drain Current ③	108	108	96	96	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		108	108	96	96	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF540 IRF542	100	–	–	V	V_{GS} = 0V
		IRF541 IRF543	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF540 IRF541	27	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF542 IRF543	24	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF540 IRF541	–	0.07	0.085	Ω	V_{GS} = 10V, I_D = 15A
		IRF542 IRF543	–	0.09	0.11	Ω	
g_{fs}	Forward Transconductance ②	ALL	6.0	10	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 15A
C_{iss}	Input Capacitance	ALL	–	1275	1600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	550	800	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	160	300	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	16	30	ns	V_{DD} ≅ 30V, I_D = 15A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	27	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	38	80	ns	
t_f	Fall Time	ALL	–	14	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	38	60	nC	V_{GS} = 10V, I_D = 34A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	17	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	21	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.0	K/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF540 IRF541	–	–	27	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF542 IRF543	–	–	24	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF540 IRF541	–	–	108	A	
		IRF542 IRF543	–	–	96	A	
V_{SD}	Diode Forward Voltage ②	IRF540 IRF541	–	–	2.5	V	T_C = 25°C, I_S = 27A, V_{GS} = 0V
		IRF542 IRF543	–	–	2.3	V	T_C = 25°C, I_S = 24A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	500	–	ns	T_J = 150°C, I_F = 27A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	2.9	–	μC	T_J = 150°C, I_F = 27A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

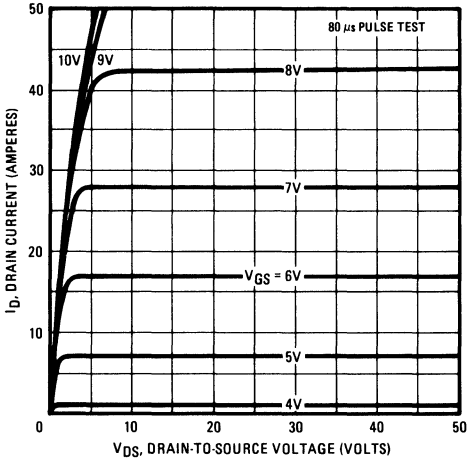


Fig. 1 – Typical Output Characteristics

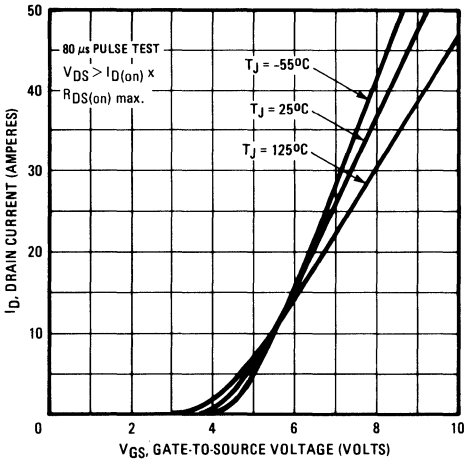


Fig. 2 – Typical Transfer Characteristics

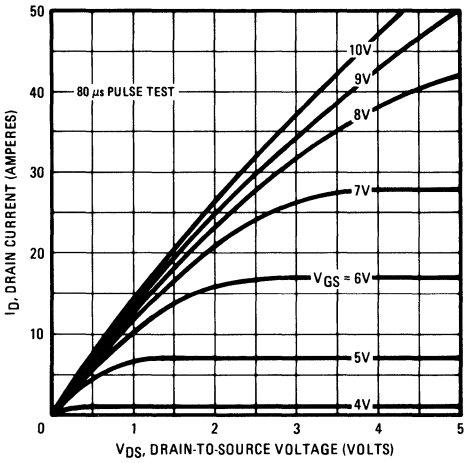


Fig. 3 – Typical Saturation Characteristics

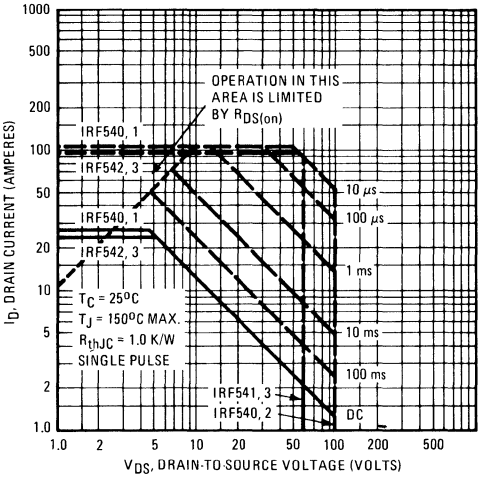


Fig. 4 – Maximum Safe Operating Area

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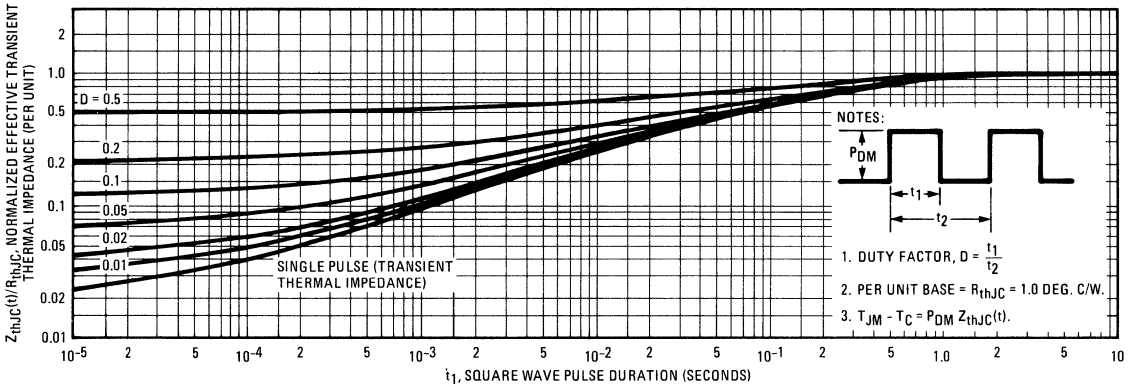


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

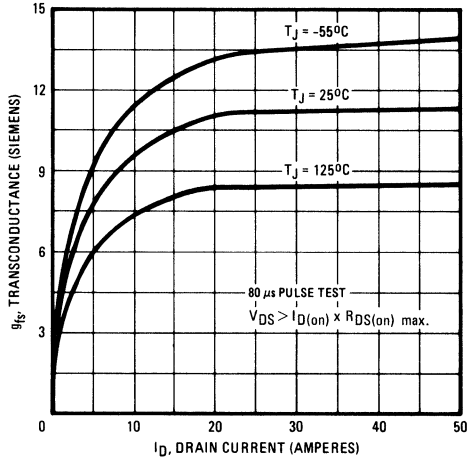


Fig. 6 — Typical Transconductance Vs. Drain Current

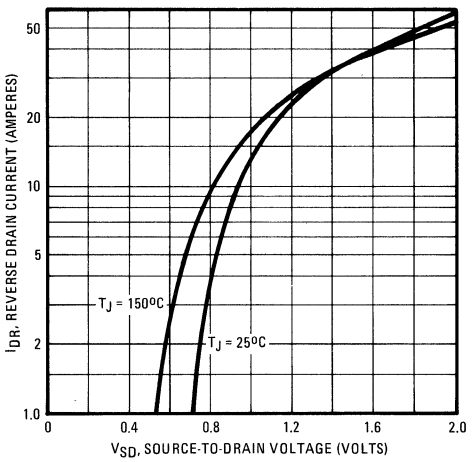


Fig. 7 — Typical Source-Drain Diode Forward Voltage

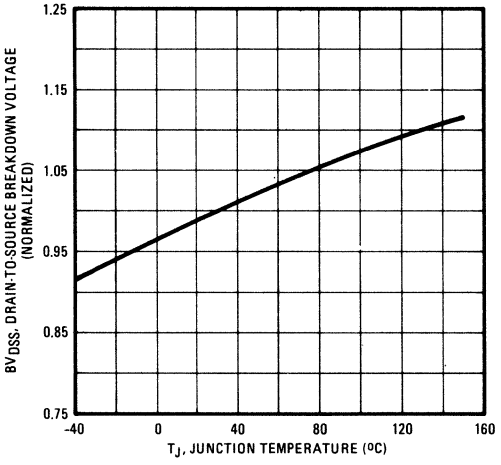


Fig. 8 — Breakdown Voltage Vs. Temperature

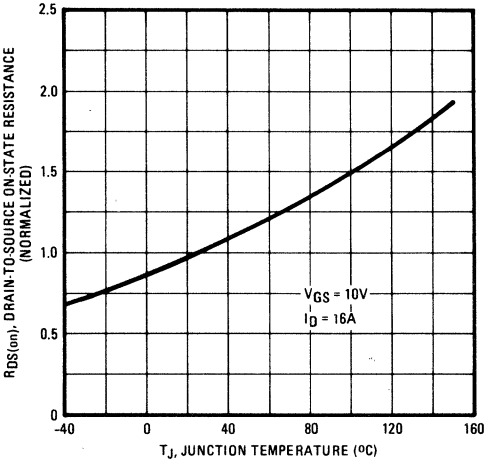


Fig. 9 — Normalized On-Resistance Vs. Temperature

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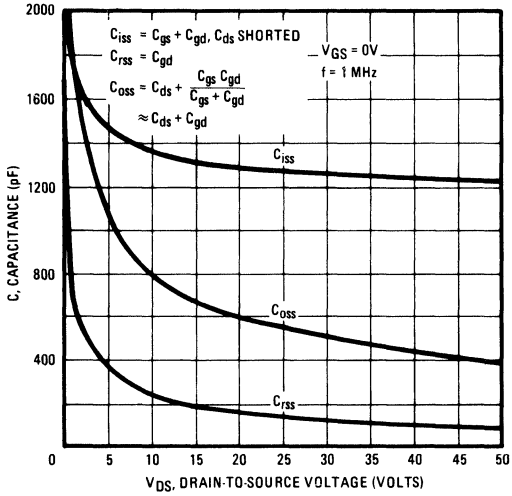


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

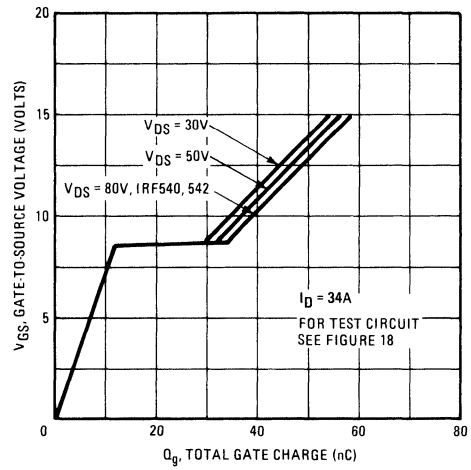


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

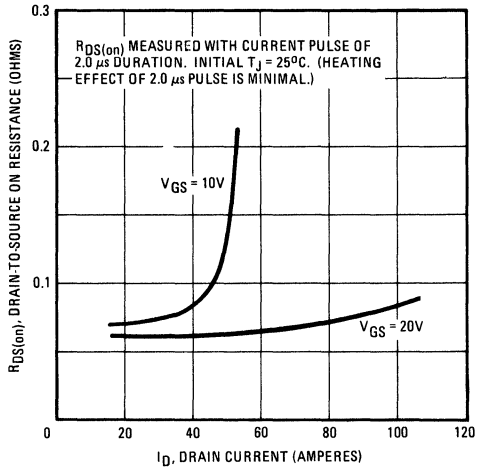


Fig. 12 — Typical On-Resistance Vs. Drain Current

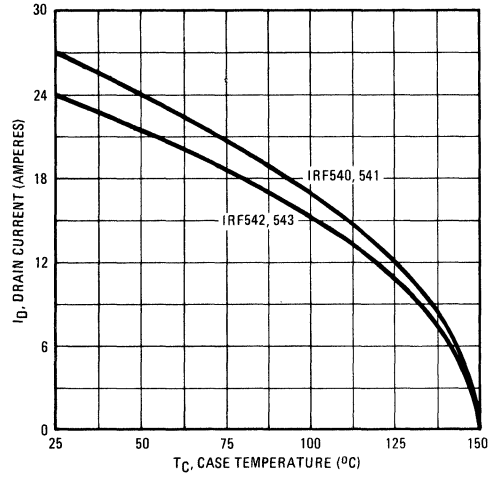


Fig. 13 — Maximum Drain Current Vs. Case Temperature

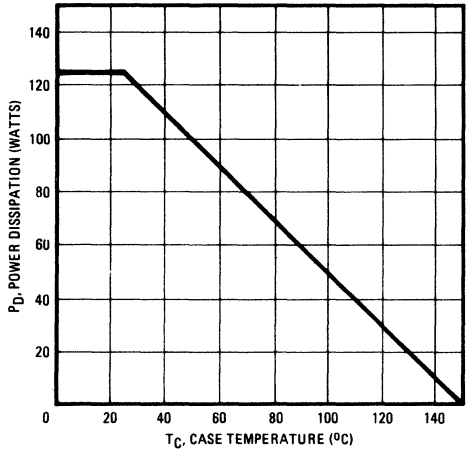


Fig. 14 — Power Vs. Temperature Derating Curve

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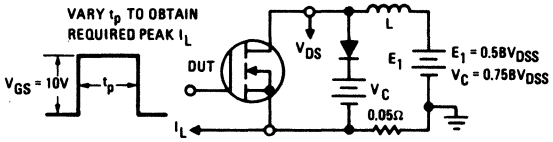


Fig. 15 — Clamped Inductive Test Circuit

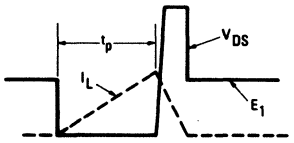


Fig. 16 — Clamped Inductive Waveforms

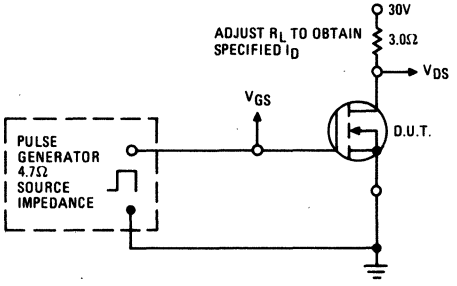


Fig. 17 — Switching Time Test Circuit

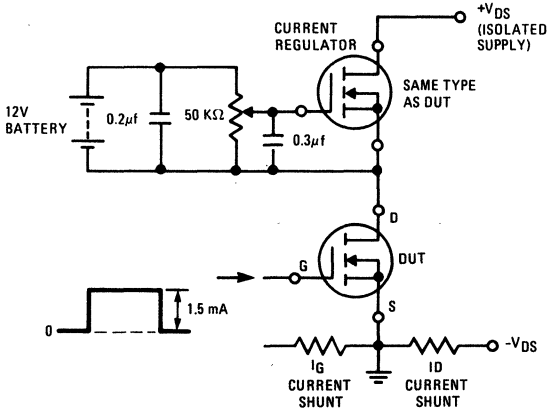


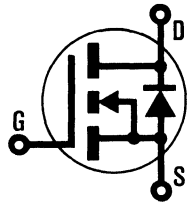
Fig. 18 — Gate Charge Test Circuit

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS

IRF610
IRF611
IRF612
IRF613



N-Channel

200 Volt, 1.5 Ohm HEXFET TO-220AB Plastic Package

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

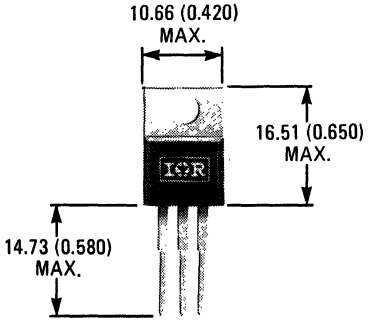
Features:

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

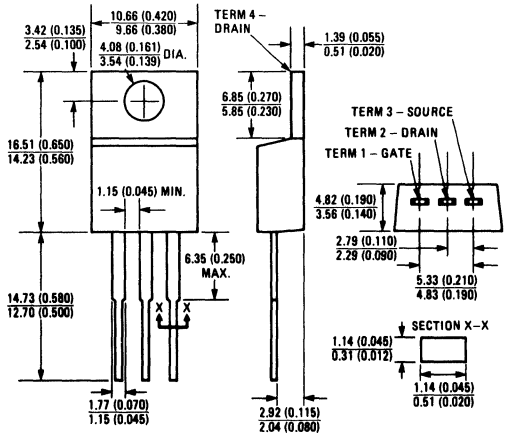
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF610	200V	1.5Ω	2.5A
IRF611	150V	1.5Ω	2.5A
IRF612	200V	2.4Ω	2.0A
IRF613	150V	2.4Ω	2.0A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Case Style TO-220AB
Dimensions in Millimeters and (Inches)

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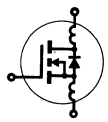
Absolute Maximum Ratings

Parameter		IRF610	IRF611	IRF612	IRF613	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	2.5	2.5	2.0	2.0	A
I_D @ T_C = 100°C	Continuous Drain Current	1.5	1.5	1.25	1.25	A
I_{DM}	Pulsed Drain Current ③	10	10	8.0	8.0	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	20 (See Fig. 14)				W
	Linear Derating Factor	0.16 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		10	10	8.0	8.0	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF610 IRF612	200	–	–	V	V_{GS} = 0V
		IRF611 IRF613	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF610 IRF611	2.5	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF612 IRF613	2.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF610 IRF611	–	1.0	1.5	Ω	V_{GS} = 10V, I_D = 1.25A
		IRF612 IRF613	–	1.5	2.4	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.8	1.3	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 1.25A
C_{iss}	Input Capacitance	ALL	–	135	150	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	60	80	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	16	25	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	8.0	15	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 1.25A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	15	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	10	15	ns	
t_f	Fall Time	ALL	–	8.0	15	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	5.0	7.5	nC	V_{GS} = 10V, I_D = 3.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	2.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	3.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	6.4	K/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF610 IRF611	–	–	2.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF612 IRF613	–	–	2.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF610 IRF611	–	–	10	A	
		IRF612 IRF613	–	–	8.0	A	
V_{SD}	Diode Forward Voltage ②	IRF610 IRF611	–	–	2.0	V	T_C = 25°C, I_S = 2.5A, V_{GS} = 0V
		IRF612 IRF613	–	–	1.8	V	T_C = 25°C, I_S = 2.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	290	–	ns	T_J = 150°C, I_F = 2.5A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	2.0	–	μC	T_J = 150°C, I_F = 2.5A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

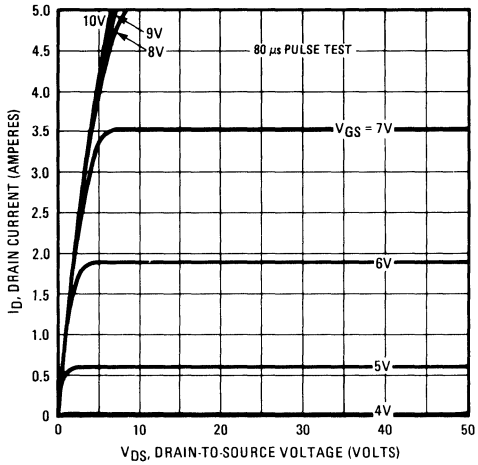


Fig. 1 — Typical Output Characteristics

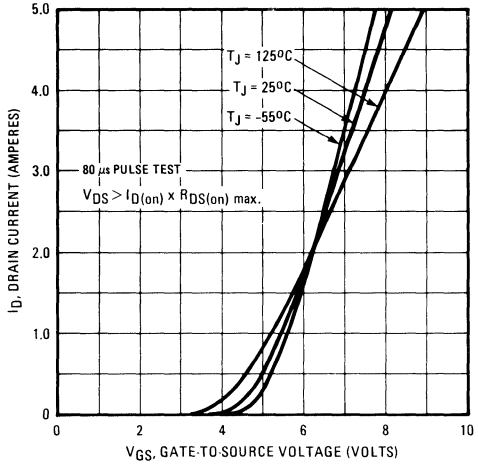


Fig. 2 — Typical Transfer Characteristics

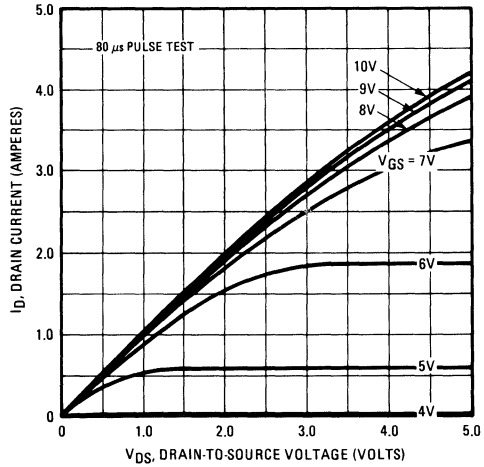


Fig. 3 — Typical Saturation Characteristics

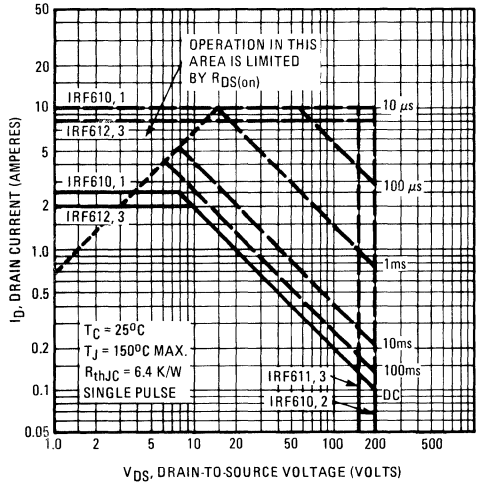


Fig. 4 — Maximum Safe Operating Area

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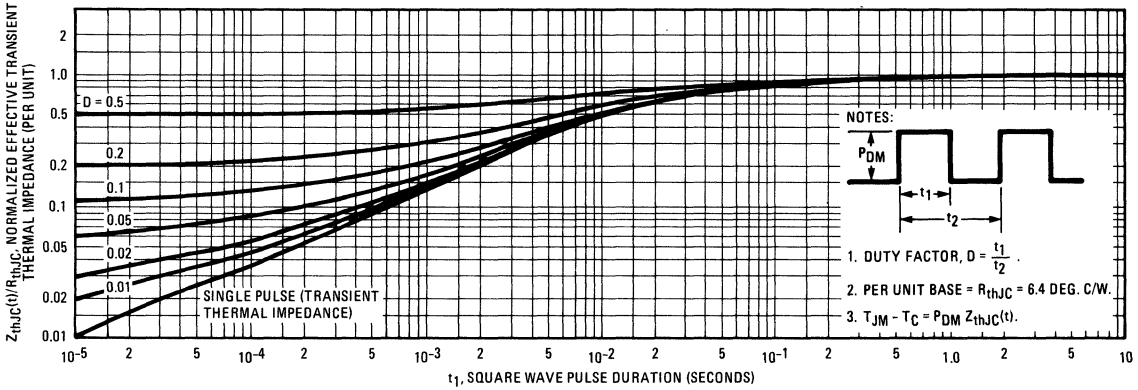


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

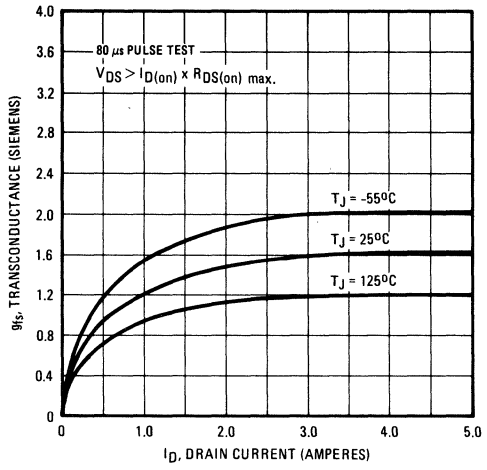


Fig. 6 — Typical Transconductance Vs. Drain Current

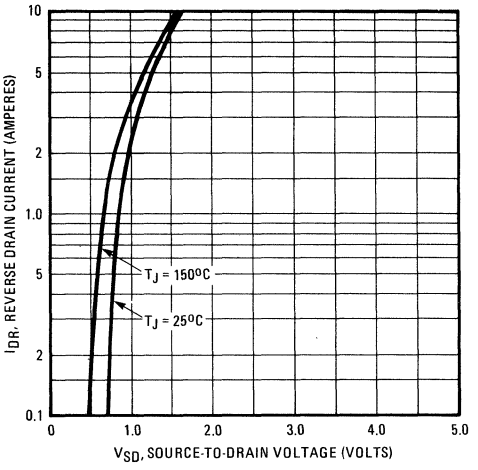


Fig. 7 — Typical Source-Drain Diode Forward Voltage

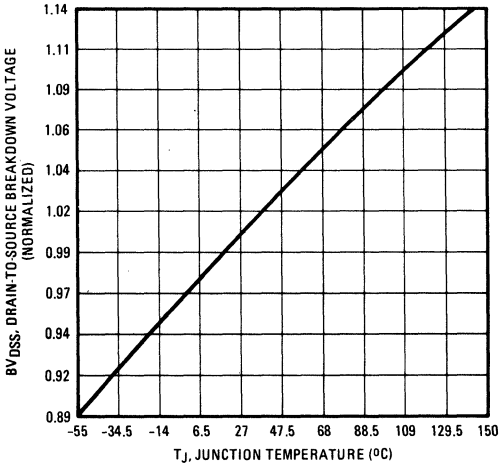


Fig. 8 — Breakdown Voltage Vs. Temperature

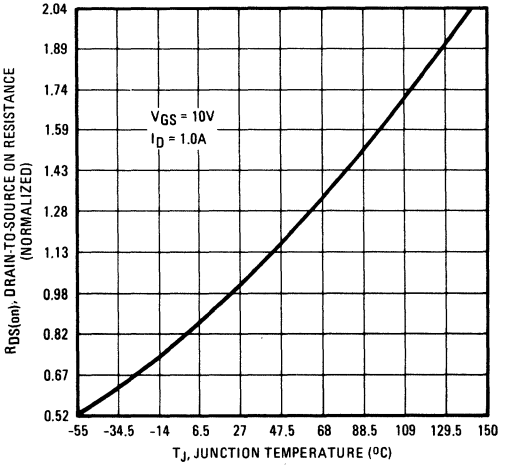


Fig. 9 — Normalized On-Resistance Vs. Temperature

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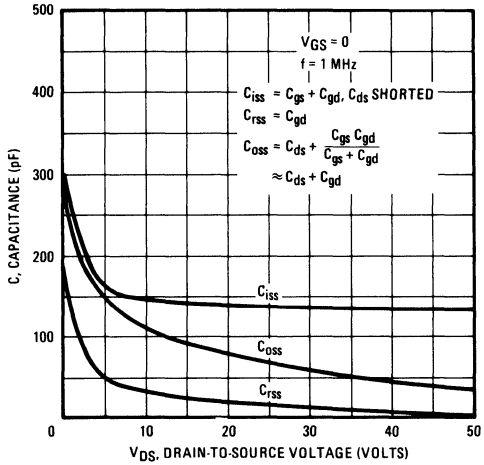


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

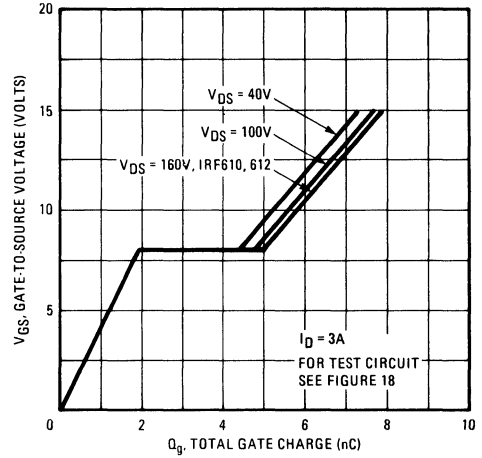


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

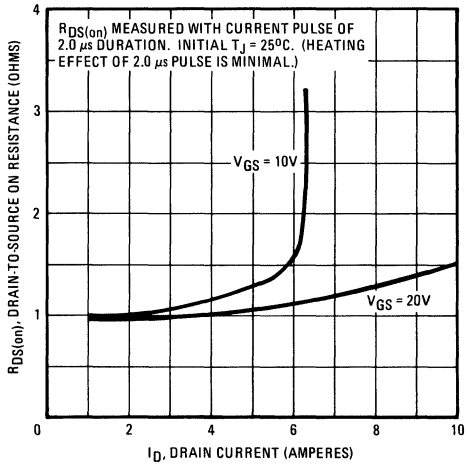


Fig. 12 — Typical On-Resistance Vs. Drain Current

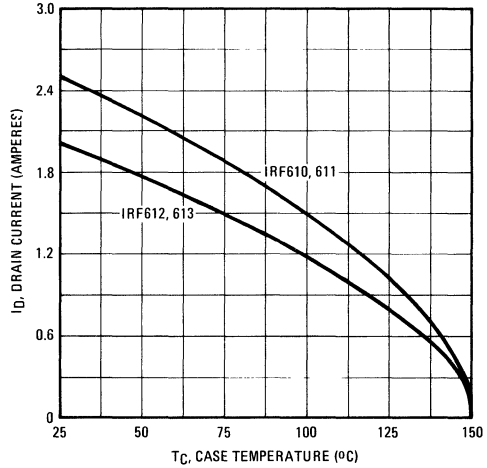


Fig. 13 — Maximum Drain Current Vs. Case Temperature

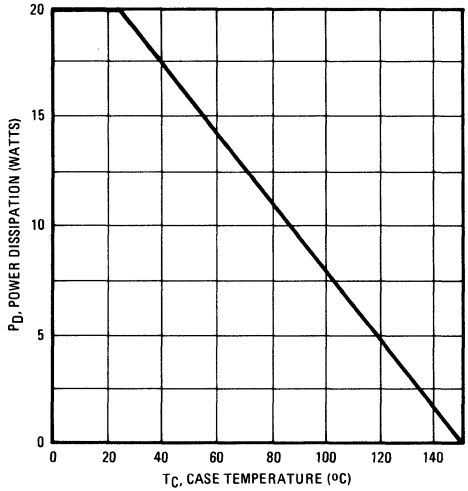


Fig. 14 — Power Vs. Temperature Derating Curve

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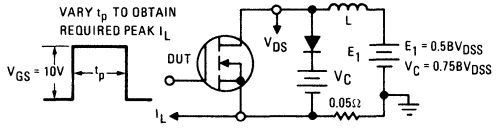


Fig. 15 – Clamped Inductive Test Circuit

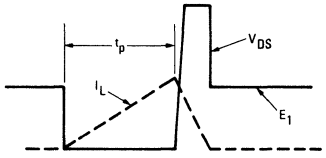


Fig. 16 – Clamped Inductive Waveforms

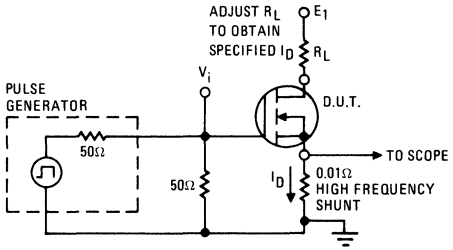


Fig. 17 – Switching Time Test Circuit

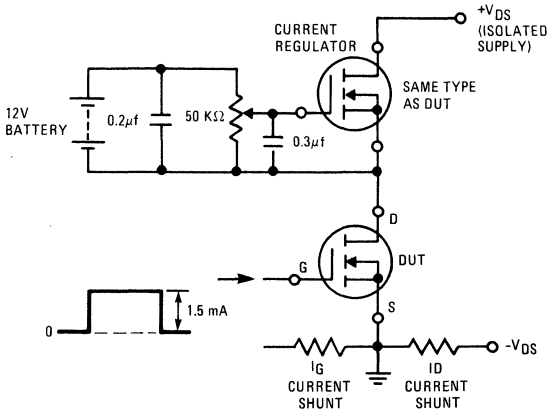


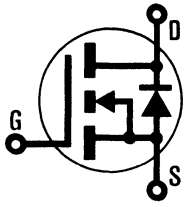
Fig. 18 – Gate Charge Test Circuit

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HEXFET® TRANSISTORS

IRF620
IRF621
IRF622
IRF623



N-Channel

200 Volt, 0.8 Ohm HEXFET TO-220AB Plastic Package

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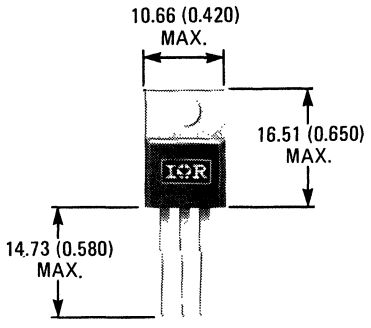
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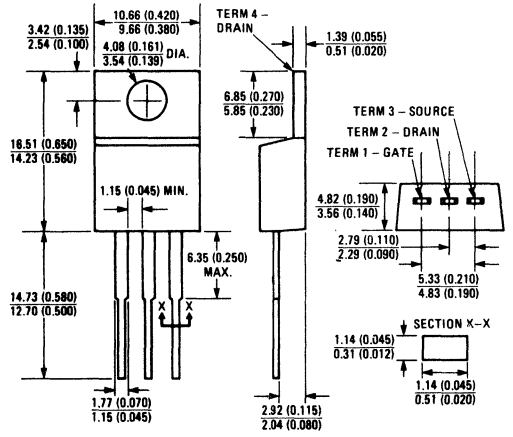
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF620	200V	0.8Ω	5.0A
IRF621	150V	0.8Ω	5.0A
IRF622	200V	1.2Ω	4.0A
IRF623	150V	1.2Ω	4.0A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Case Style TO-220AB
Dimensions in Millimeters and (Inches)

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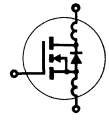
Absolute Maximum Ratings

Parameter		IRF620	IRF621	IRF622	IRF623	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	5.0	5.0	4.0	4.0	A
I_D @ T_C = 100°C	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_{DM}	Pulsed Drain Current ③	20	20	16	16	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		20	20	16	16	
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF620 IRF622	200	–	–	V	V_{GS} = 0V
		IRF621 IRF623	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF620 IRF621	5.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF622 IRF623	4.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF620 IRF621	–	0.5	0.8	Ω	V_{GS} = 10V, I_D = 2.5A
		IRF622 IRF623	–	0.8	1.2	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.3	2.5	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 2.5A
C_{iss}	Input Capacitance	ALL	–	450	600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	150	300	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	40	80	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} ≈ 2.5 BV_{DSS}, I_D = 2.5A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	30	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	30	60	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	11	15	nC	V_{GS} = 50V, I_D = 6.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	5.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	6.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	3.12	K/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF620 IRF621	–	–	5.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF622 IRF623	–	–	4.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF620 IRF621	–	–	20	A	
		IRF622 IRF623	–	–	16	A	
V_{SD}	Diode Forward Voltage ②	IRF620 IRF621	–	–	1.8	V	T_C = 25°C, I_S = 5.0A, V_{GS} = 0V
		IRF622 IRF623	–	–	1.4	V	T_C = 25°C, I_S = 4.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	350	–	ns	T_J = 150°C, I_F = 5.0A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	2.3	–	μC	T_J = 150°C, I_F = 5.0A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

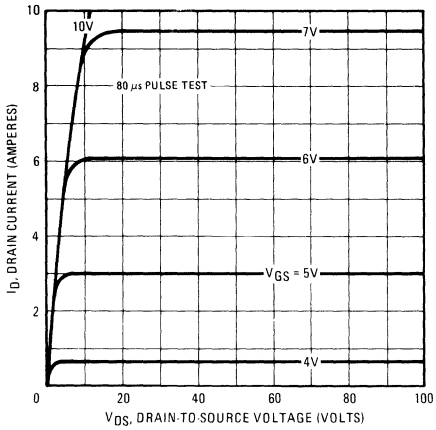


Fig. 1 – Typical Output Characteristics

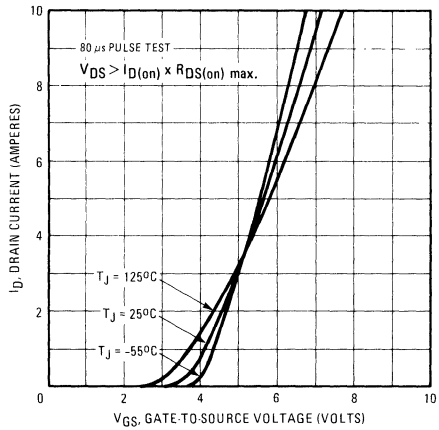


Fig. 2 – Typical Transfer Characteristics

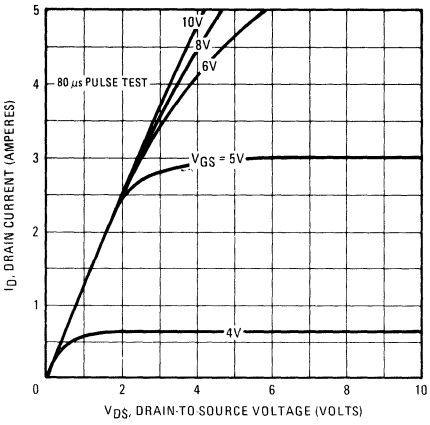


Fig. 3 – Typical Saturation Characteristics

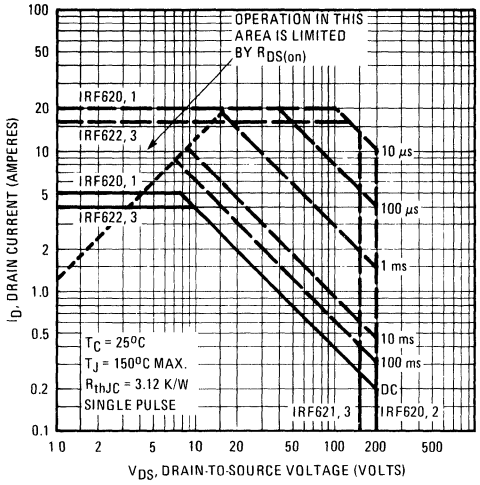


Fig. 4 – Maximum Safe Operating Area

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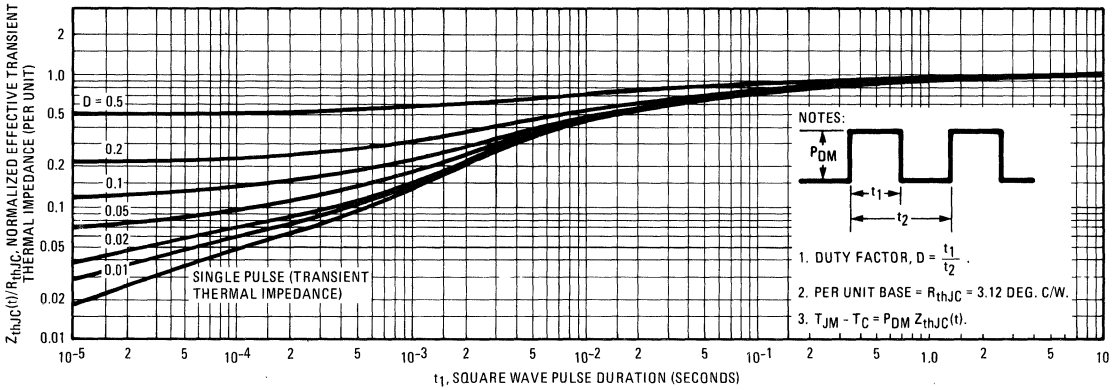


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

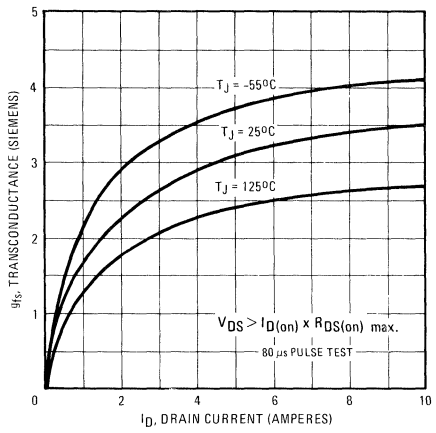


Fig. 6 – Typical Transconductance Vs. Drain Current

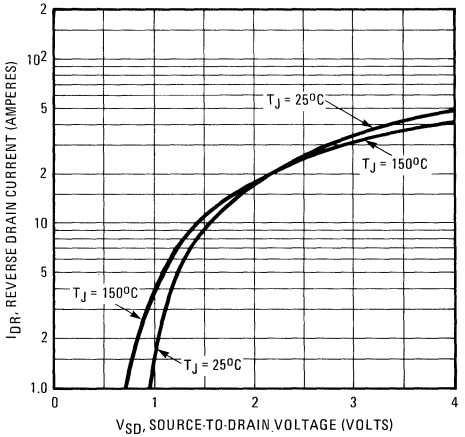


Fig. 7 – Typical Source-Drain Diode Forward Voltage

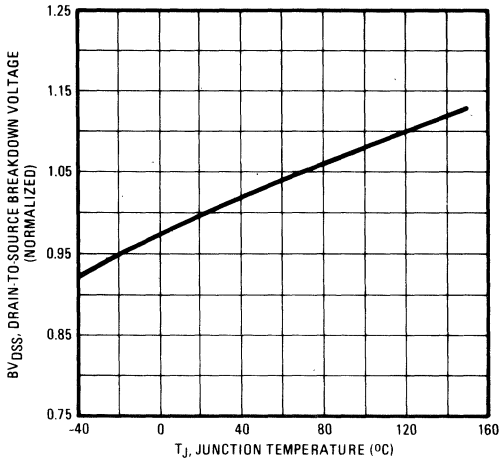


Fig. 8 – Breakdown Voltage Vs. Temperature

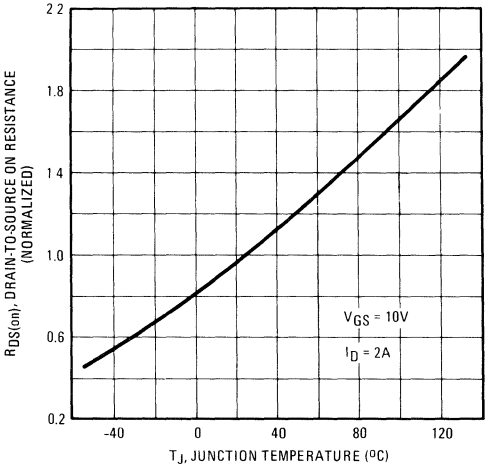


Fig. 9 – Normalized On-Resistance Vs. Temperature

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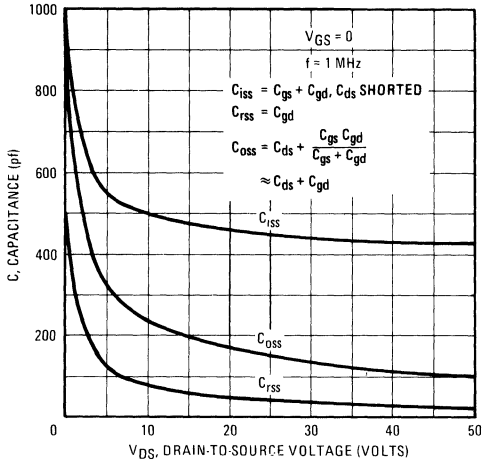


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

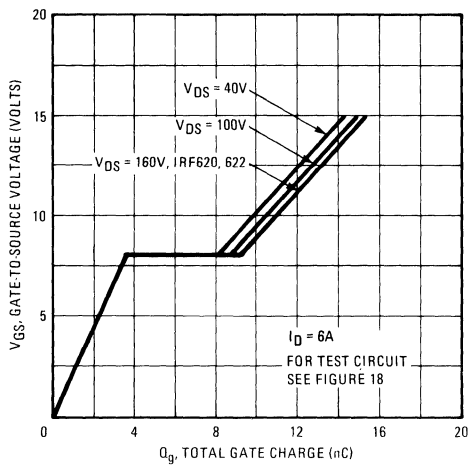


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

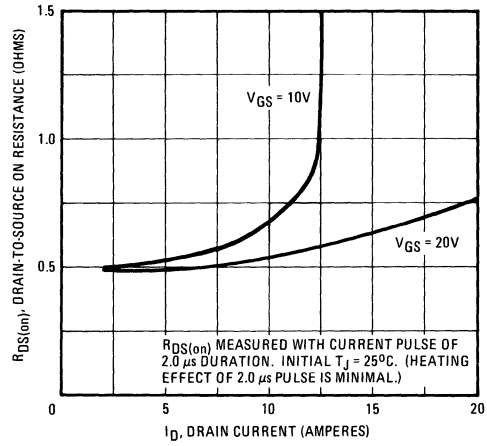


Fig. 12 — Typical On-Resistance Vs. Drain Current

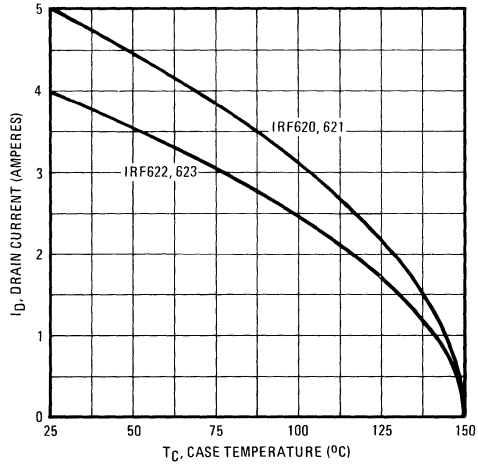


Fig. 13 — Maximum Drain Current Vs. Case Temperature

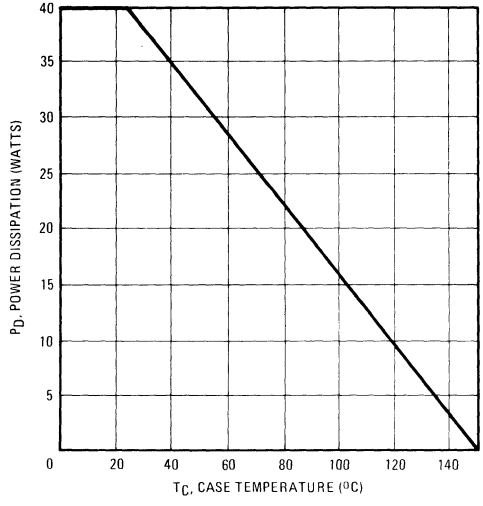


Fig. 14 — Power Vs. Temperature Derating Curve

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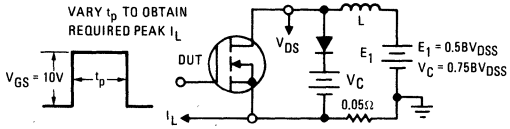


Fig. 15 — Clamped Inductive Test Circuit

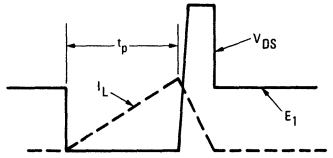


Fig. 16 — Clamped Inductive Waveforms

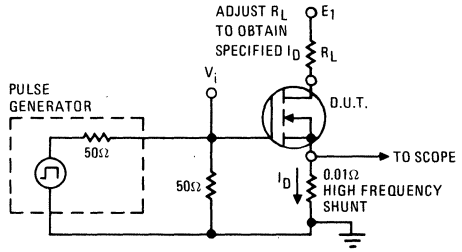


Fig. 17 — Switching Time Test Circuit

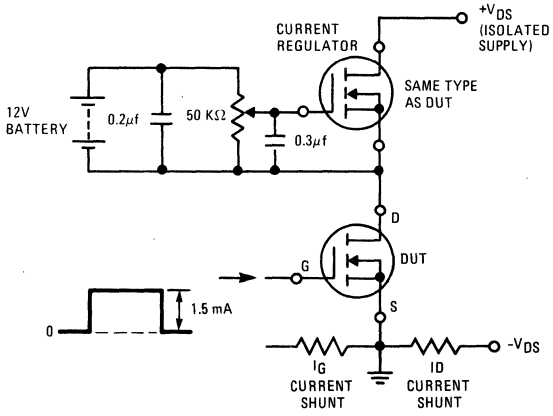


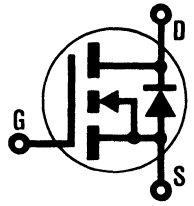
Fig. 18 — Gate Charge Test Circuit

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS

IRF630
IRF631
IRF632
IRF633



N-Channel

200 Volt, 0.4 Ohm HEXFET
TO-220AB Plastic Package

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

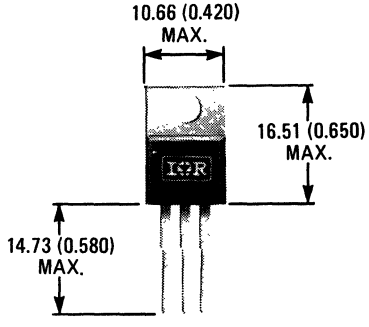
Features:

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

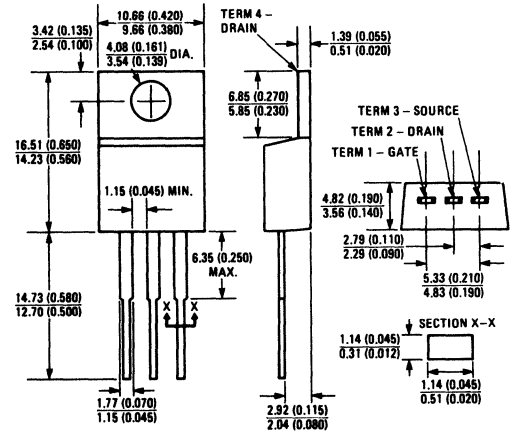
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF630	200V	0.4Ω	9.0A
IRF631	150V	0.4Ω	9.0A
IRF632	200V	0.6Ω	8.0A
IRF633	150V	0.6Ω	8.0A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Case Style TO-220AB
Dimensions in Millimeters and (Inches)

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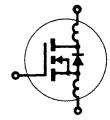
Absolute Maximum Ratings

Parameter		IRF630	IRF631	IRF632	IRF633	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	9.0	9.0	8.0	8.0	A
I_D @ T_C = 100°C	Continuous Drain Current	6.0	6.0	5.0	5.0	A
I_{DM}	Pulsed Drain Current ③	36	36	32	32	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		36	36	32	32	
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF630 IRF632	200	–	–	V	V_{GS} = 0V
		IRF631 IRF633	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF630 IRF631	9.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF632 IRF633	8.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF630 IRF631	–	0.25	0.4	Ω	V_{GS} = 10V, I_D = 5.0A
		IRF632 IRF633	–	0.4	0.6	Ω	
g_{fs}	Forward Transconductance ②	ALL	3.0	4.8	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 5.0A
C_{iss}	Input Capacitance	ALL	–	600	800	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	250	450	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	80	150	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} ≈ 90V, I_D = 5.0A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	50	ns	
t_f	Fall Time	ALL	–	–	40	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	19	30	nC	V_{GS} = 10V, I_D = 12A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	10	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	9.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67	K/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF630 IRF631	–	–	9.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF632 IRF633	–	–	8.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF630 IRF631	–	–	36	A	
		IRF632 IRF633	–	–	32	A	
V_{SD}	Diode Forward Voltage ②	IRF630 IRF631	–	–	2.0	V	T_C = 25°C, I_S = 9.0A, V_{GS} = 0V
		IRF632 IRF633	–	–	1.8	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	450	–	ns	T_J = 150°C, I_F = 9.0A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	3.0	–	μC	T_J = 150°C, I_F = 9.0A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

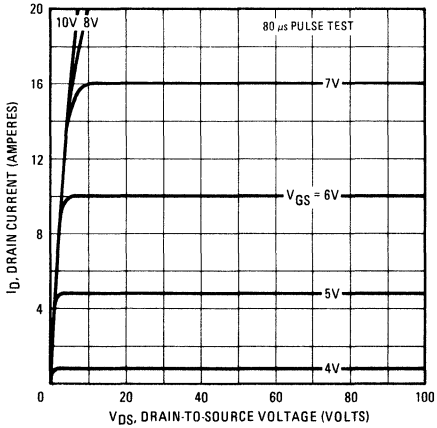


Fig. 1 – Typical Output Characteristics

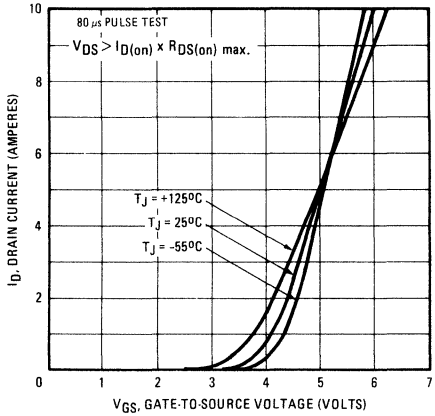


Fig. 2 – Typical Transfer Characteristics

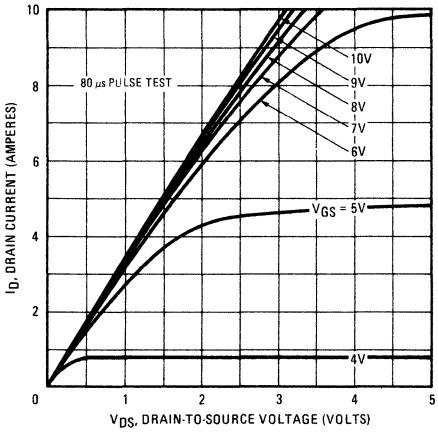


Fig. 3 – Typical Saturation Characteristics

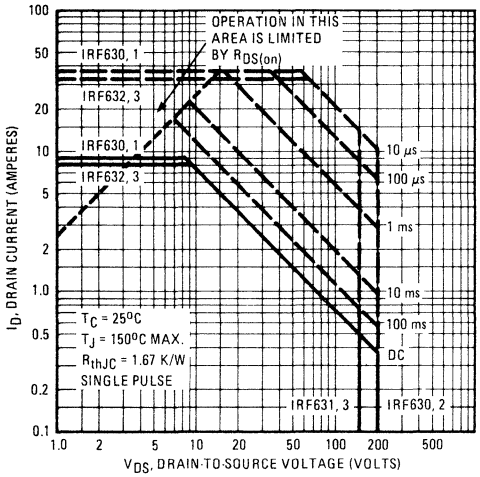


Fig. 4 – Maximum Safe Operating Area

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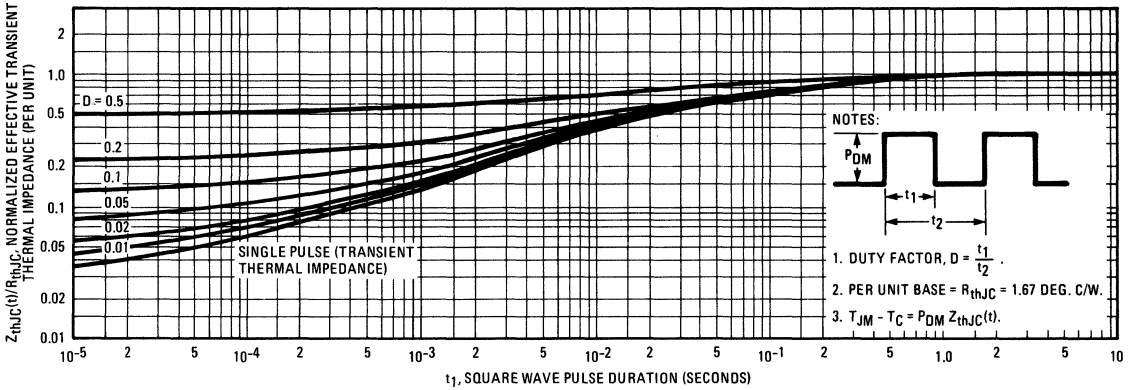


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

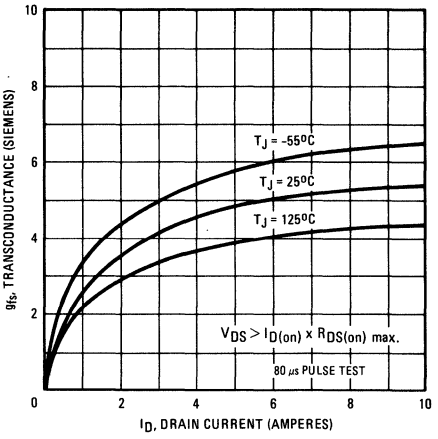


Fig. 6 — Typical Transconductance Vs. Drain Current

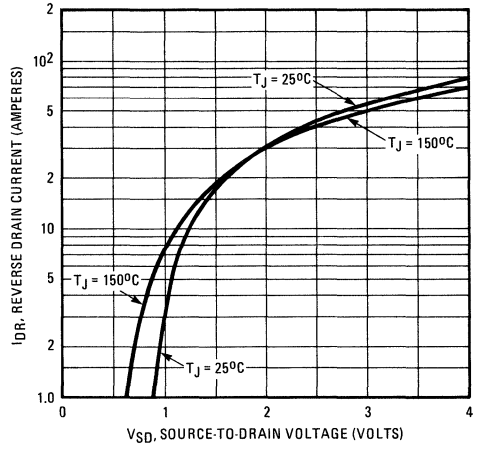


Fig. 7 — Typical Source-Drain Diode Forward Voltage

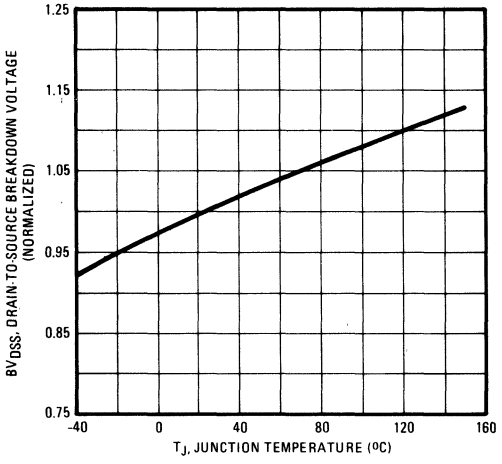


Fig. 8 — Breakdown Voltage Vs. Temperature

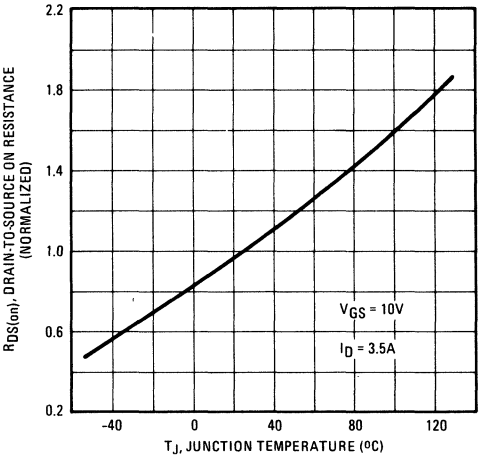


Fig. 9 — Normalized On-Resistance Vs. Temperature

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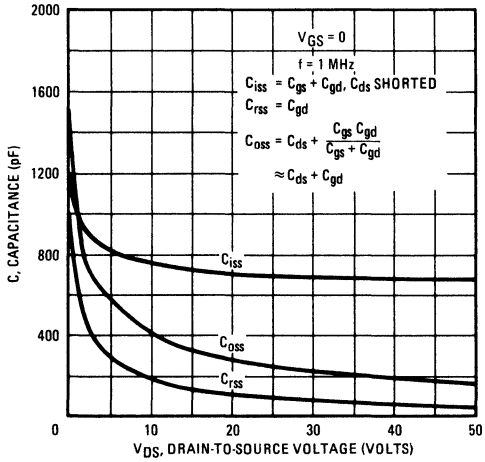


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

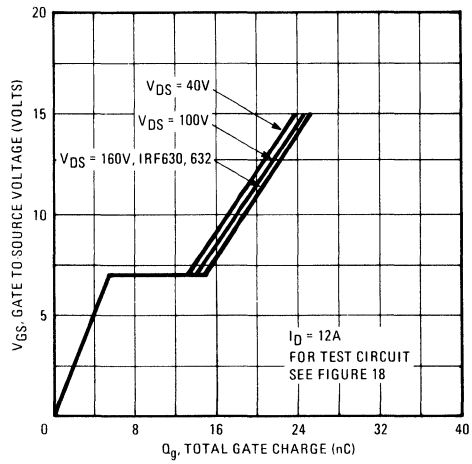


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

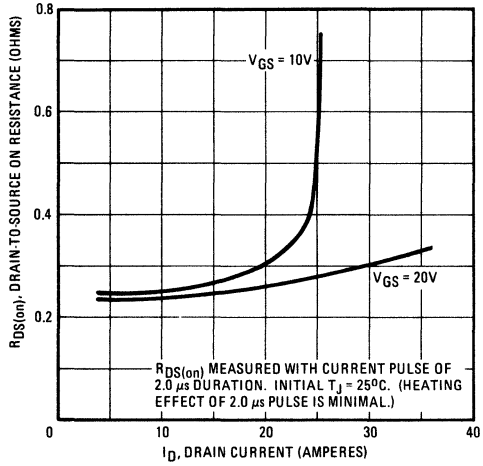


Fig. 12 — Typical On-Resistance Vs. Drain Current

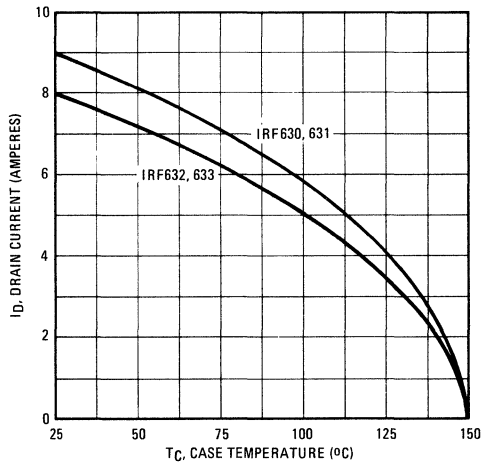


Fig. 13 — Maximum Drain Current Vs. Case Temperature

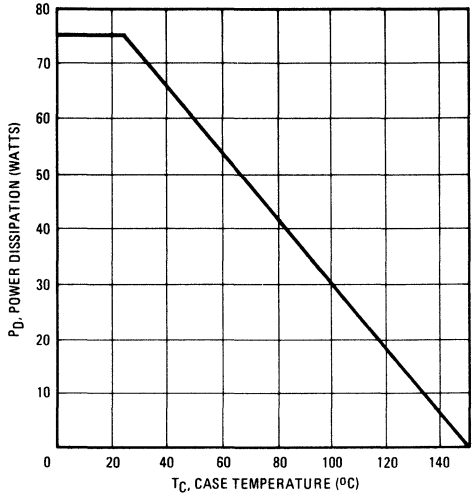


Fig. 14 — Power Vs. Temperature Derating Curve

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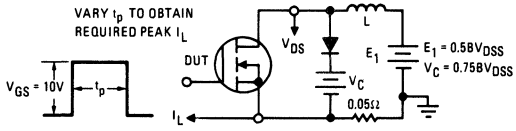


Fig. 15 — Clamped Inductive Test Circuit

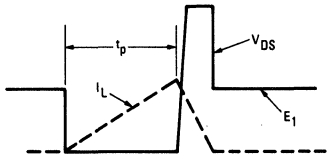


Fig. 16 — Clamped Inductive Waveforms

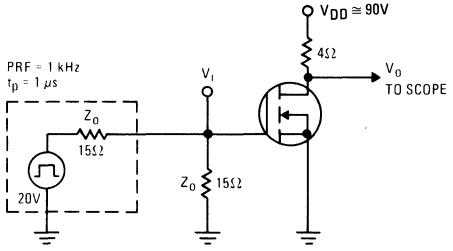


Fig. 17 — Switching Time Test Circuit

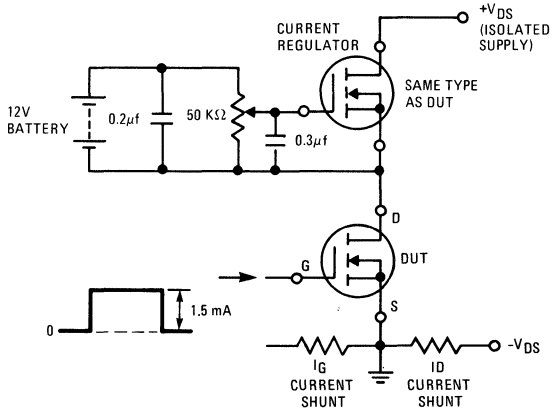


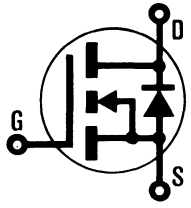
Fig. 18 — Gate Charge Test Circuit

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS IRF640

N-CHANNEL POWER MOSFETs



IRF641

IRF642

IRF643

200 Volt, 0.2 Ohm HEXFET TO-220AB Plastic Package

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

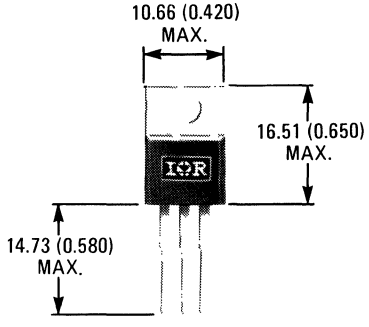
Features:

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

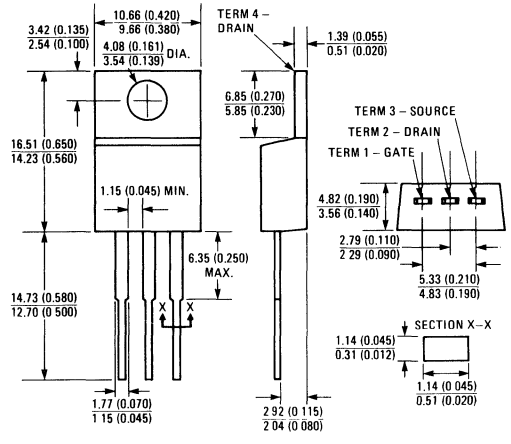
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF640	200V	0.18Ω	18A
IRF641	150V	0.18Ω	18A
IRF642	200V	0.22Ω	16A
IRF643	150V	0.22Ω	16A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Case Style TO-220AB
Dimensions in Millimeters and (Inches)

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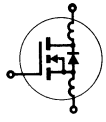
Absolute Maximum Ratings

Parameter		IRF640	IRF641	IRF642	IRF643	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	18	18	16	16	A
I_D @ T_C = 100°C	Continuous Drain Current	11	11	10	10	A
I_{DM}	Pulsed Drain Current ③	72	72	64	64	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		72	72	64	64	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 100				°C
	Lead Temperature	300 (0.064 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF640 IRF642	200	–	–	V	V_{GS} = 0V
		IRF641 IRF643	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF640 IRF641	18	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)\ max.}$, V_{GS} = 10V
		IRF642 IRF643	16	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF640 IRF641	–	0.14	0.18	Ω	V_{GS} = 10V, I_D = 10A
		IRF642 IRF643	–	0.20	0.22	Ω	
g_{fs}	Forward Transconductance ②	ALL	6.0	10	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)\ max.}$, I_D = 10A
C_{iss}	Input Capacitance	ALL	–	1275	1600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	500	750	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	160	300	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	16	30	ns	V_{DD} ≈ 75V, I_D = 10A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	27	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	40	80	ns	
t_f	Fall Time	ALL	–	31	60	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	43	60	nC	V_{GS} = 10V, I_D = 22A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	16	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	27	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.0	K/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF640 IRF641	–	–	18	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF642 IRF643	–	–	16	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF640 IRF641	–	–	72	A	
		IRF642 IRF643	–	–	64	A	
V_{SD}	Diode Forward Voltage ②	IRF640 IRF641	–	–	2.0	V	T_C = 25°C, I_S = 18A, V_{GS} = 0V
		IRF642 IRF643	–	–	1.9	V	T_C = 25°C, I_S = 16A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	650	–	ns	T_J = 150°C, I_F = 18A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.1	–	μC	T_J = 150°C, I_F = 18A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

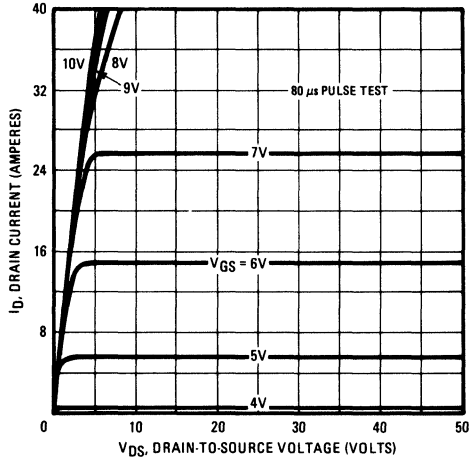


Fig. 1 — Typical Output Characteristics

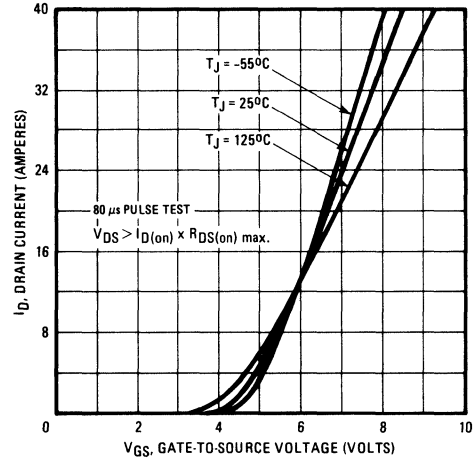


Fig. 2 — Typical Transfer Characteristics

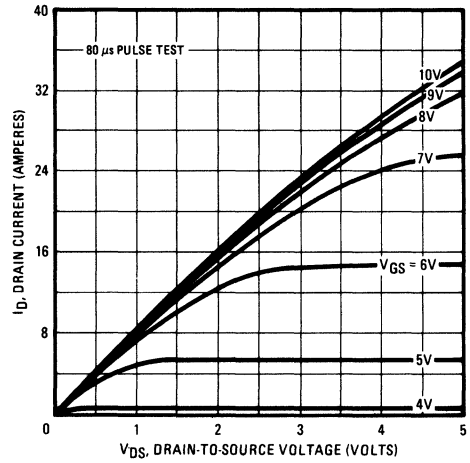


Fig. 3 — Typical Saturation Characteristics

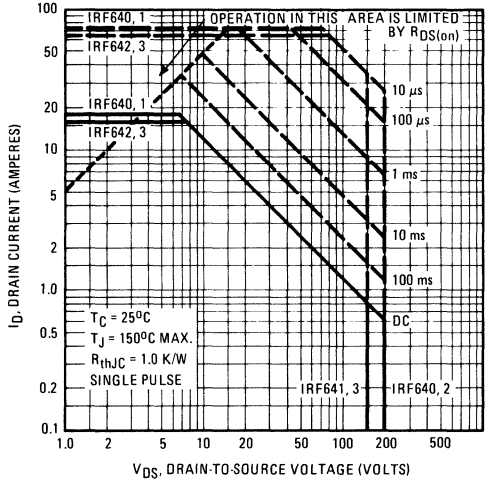


Fig. 4 — Maximum Safe Operating Area

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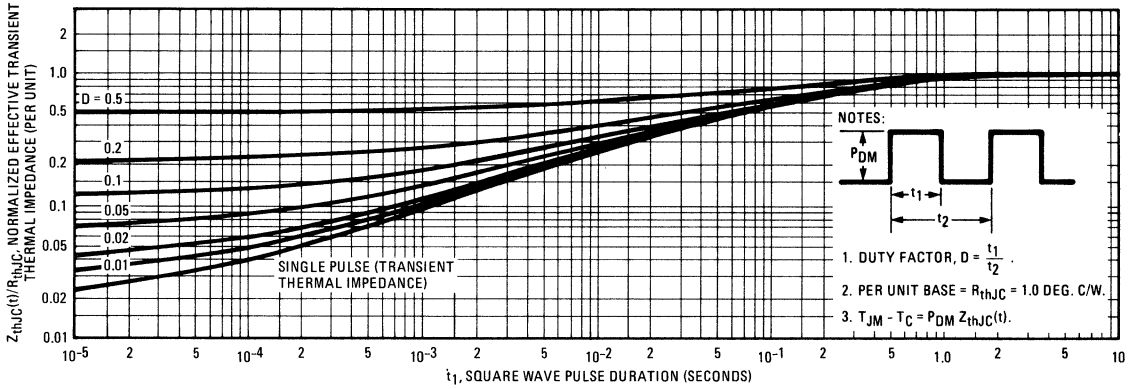


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

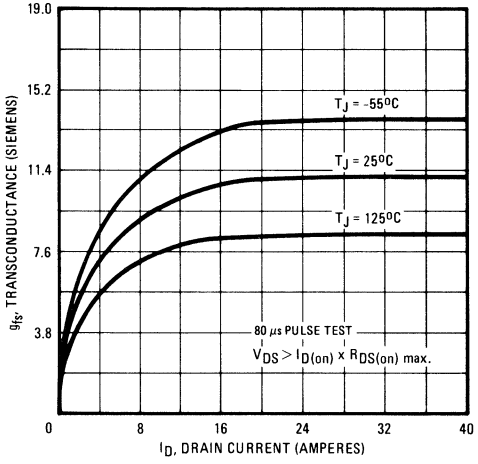


Fig. 6 — Typical Transconductance Vs. Drain Current

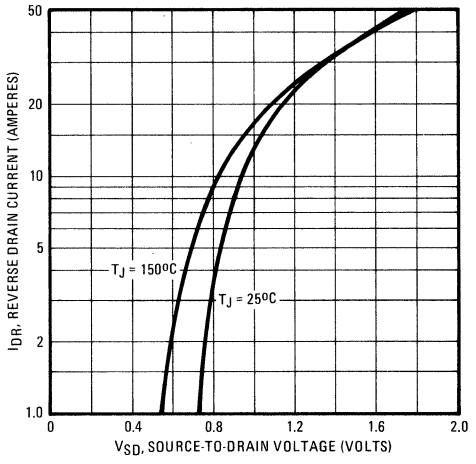


Fig. 7 — Typical Source-Drain Diode Forward Voltage

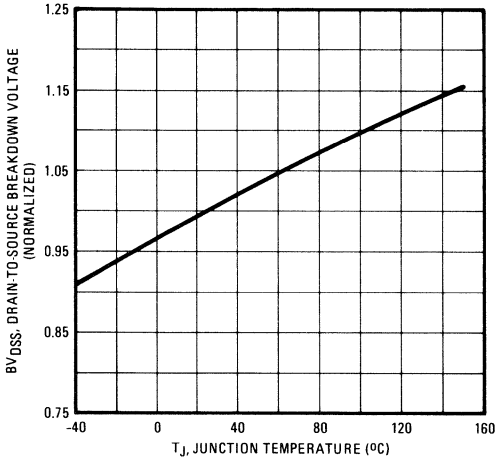


Fig. 8 — Breakdown Voltage Vs. Temperature

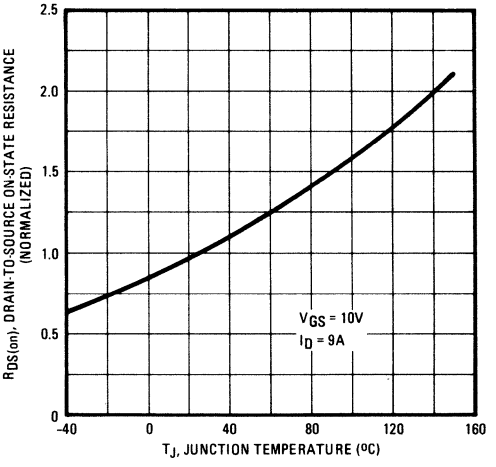


Fig. 9 — Normalized On-Resistance Vs. Temperature

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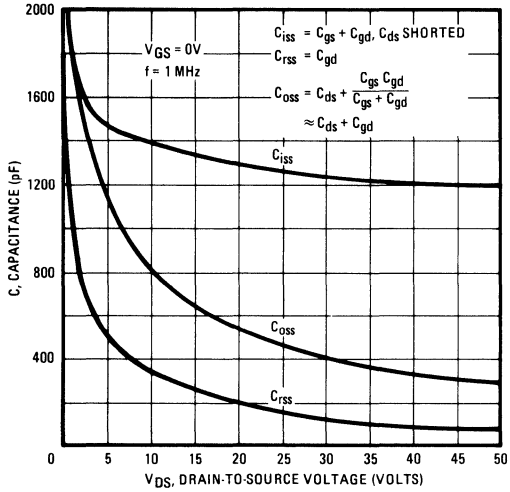


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

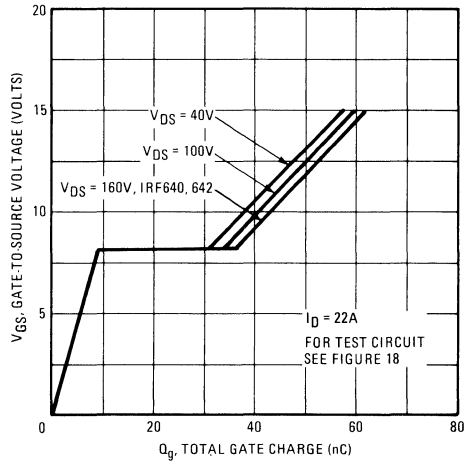


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

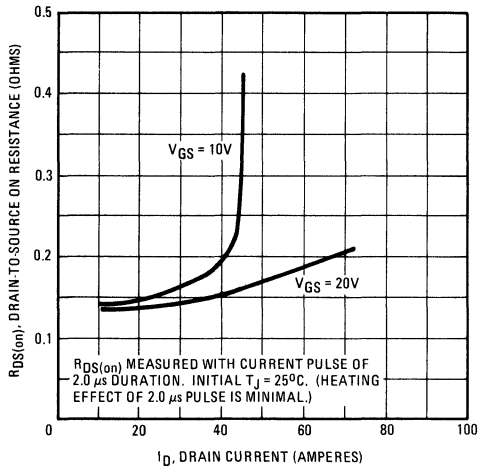


Fig. 12 — Typical On-Resistance Vs. Drain Current

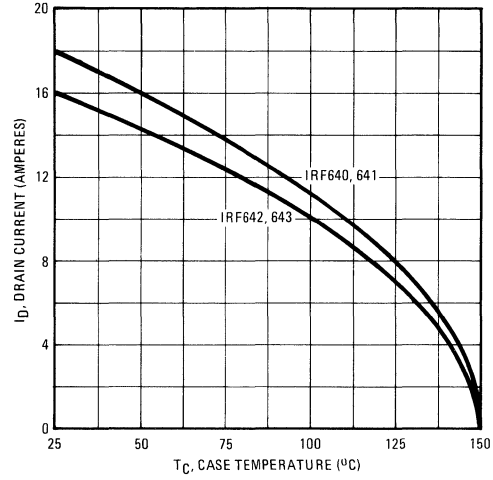


Fig. 13 — Maximum Drain Current Vs. Case Temperature

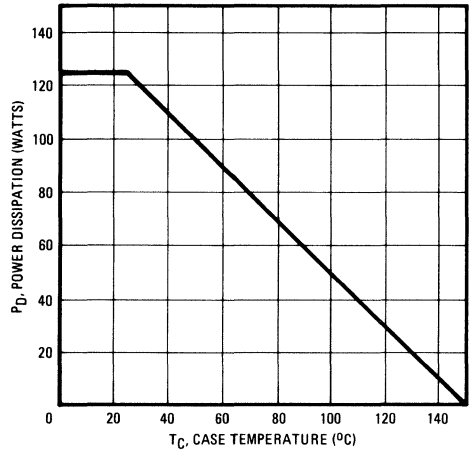


Fig. 14 — Power Vs. Temperature Derating Curve

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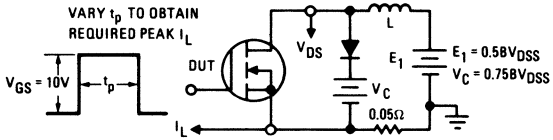


Fig. 15 — Clamped Inductive Test Circuit

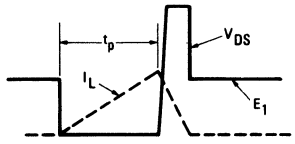


Fig. 16 — Clamped Inductive Waveforms

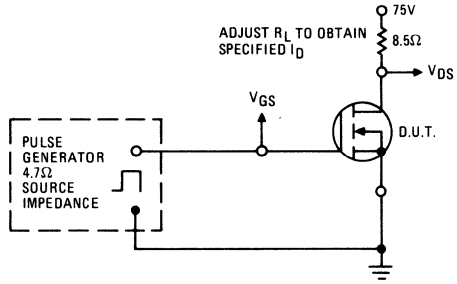


Fig. 17 — Switching Time Test Circuit

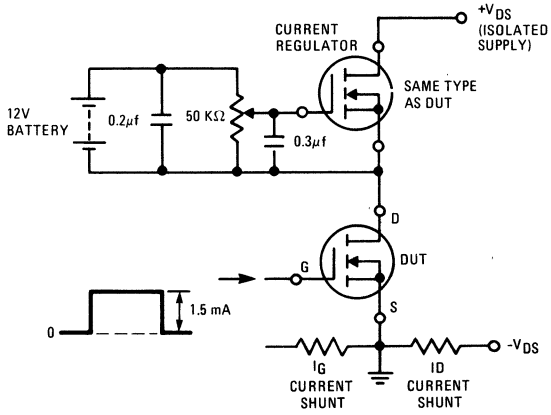


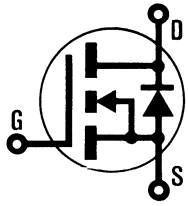
Fig. 18 — Gate Charge Test Circuit

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS

IRF710
IRF711
IRF712
IRF713



N-Channel

400 Volt, 3.6 Ohm HEXFET TO-220AB Plastic Package

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

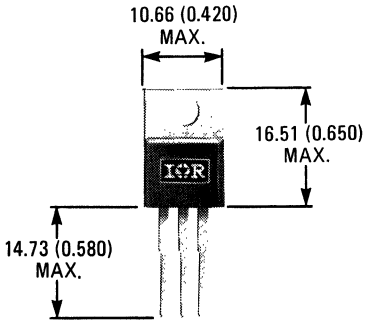
Features:

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

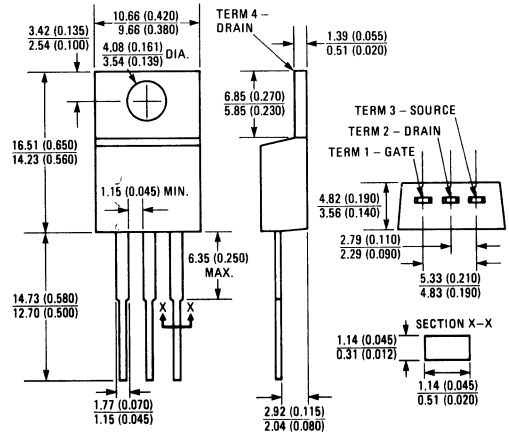
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF710	400V	3.6Ω	1.5A
IRF711	350V	3.6Ω	1.5A
IRF712	400V	5.0Ω	1.3A
IRF713	350V	5.0Ω	1.3A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Case Style TO-220AB
Dimensions in Millimeters and (Inches)

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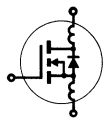
Absolute Maximum Ratings

Parameter		IRF710	IRF711	IRF712	IRF713	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	1.5	1.5	1.3	1.3	A
I_D @ T_C = 100°C	Continuous Drain Current	1.0	1.0	0.8	0.8	A
I_{DM}	Pulsed Drain Current ③	6.0	6.0	5.0	5.0	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	20 (See Fig. 14)				W
	Linear Derating Factor	0.16 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		6.0	6.0	5.0	5.0	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF710 IRF712	400	–	–	V	V_{GS} = 0V
		IRF711 IRF713	350	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF710 IRF711	1.5	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF712 IRF713	1.3	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF710 IRF711	–	3.3	3.6	Ω	V_{GS} = 10V, I_D = 0.8A
		IRF712 IRF713	–	3.6	5.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.5	1.2	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 0.8A
C_{iss}	Input Capacitance	ALL	–	135	150	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	35	50	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	8.0	15	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	3.0	10	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 0.8A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	10	20	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	5.0	10	ns	
t_f	Fall Time	ALL	–	8.0	15	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	6.0	7.5	nC	V_{GS} = 10V, I_D = 2.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	3.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	3.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	6.4	K/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF710 IRF711	–	–	1.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF712 IRF713	–	–	1.3	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF710 IRF711	–	–	6.0	A	
		IRF712 IRF713	–	–	5.0	A	
V_{SD}	Diode Forward Voltage ②	IRF710 IRF711	–	–	1.6	V	T_C = 25°C, I_S = 1.5A, V_{GS} = 0V
		IRF712 IRF713	–	–	1.5	V	T_C = 25°C, I_S = 1.3A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	380	–	ns	T_J = 150°C, I_F = 1.5A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	2.7	–	μC	T_J = 150°C, I_F = 1.5A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

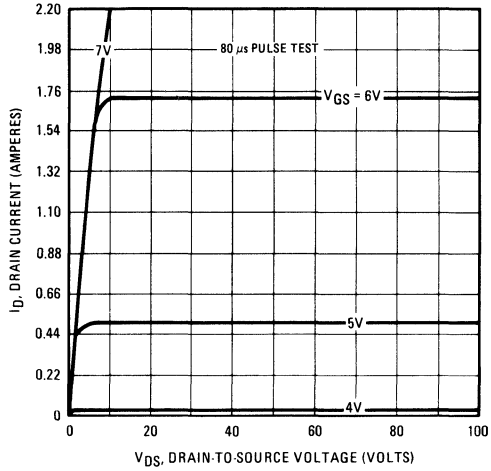


Fig. 1 — Typical Output Characteristics

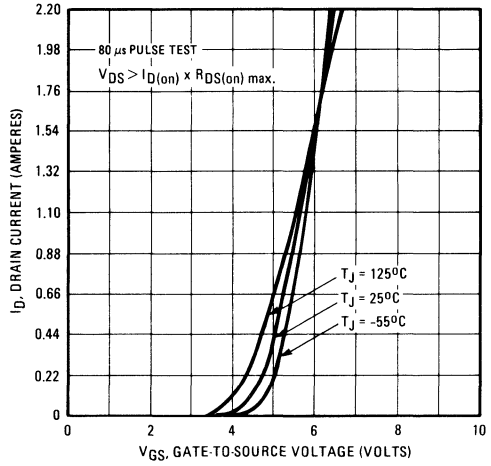


Fig. 2 — Typical Transfer Characteristics

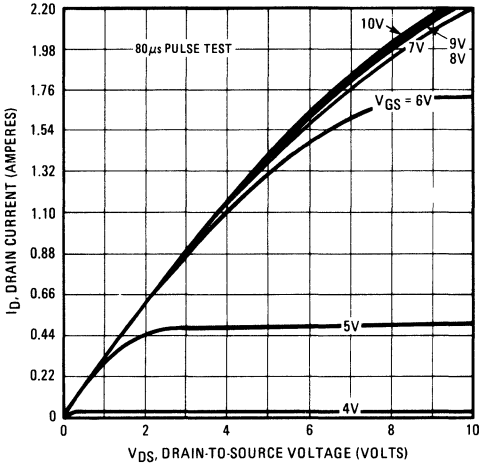


Fig. 3 — Typical Saturation Characteristics

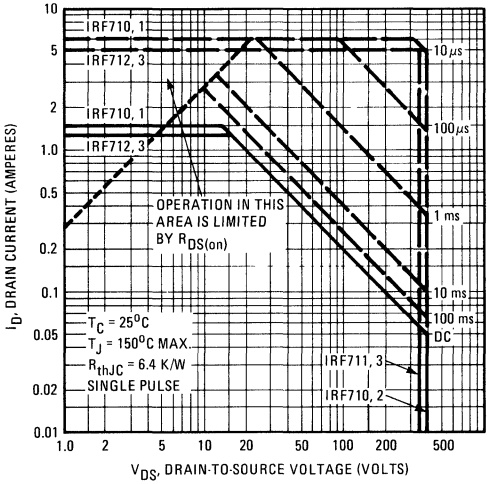


Fig. 4 — Maximum Safe Operating Area

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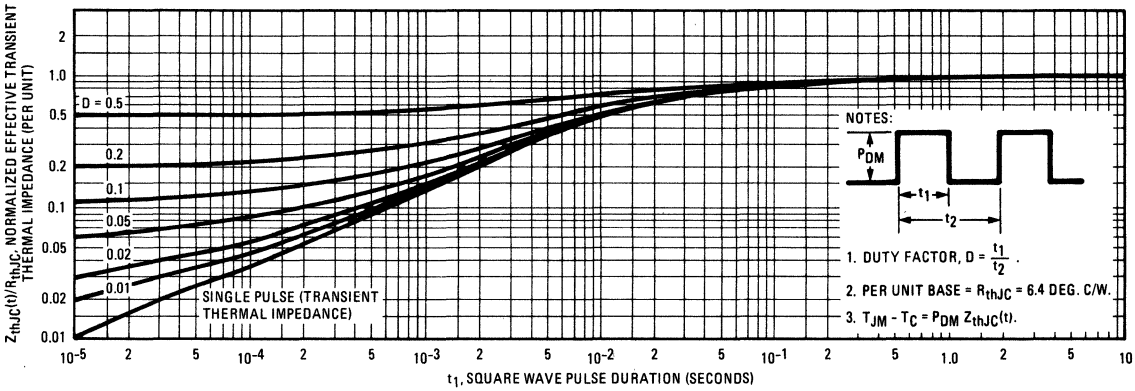


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

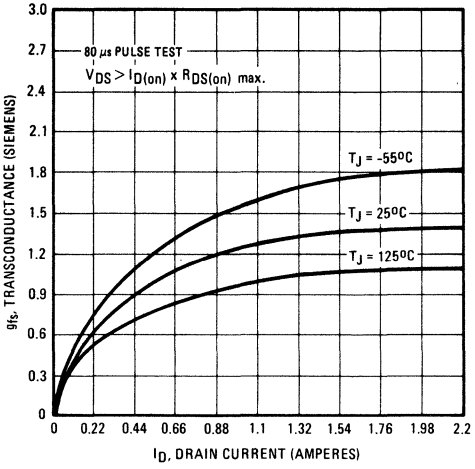


Fig. 6 — Typical Transconductance Vs. Drain Current

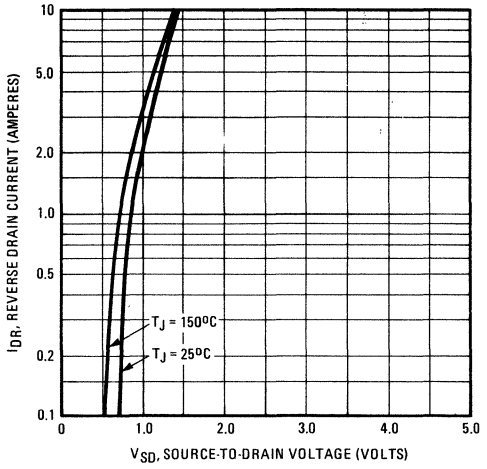


Fig. 7 — Typical Source-Drain Diode Forward Voltage

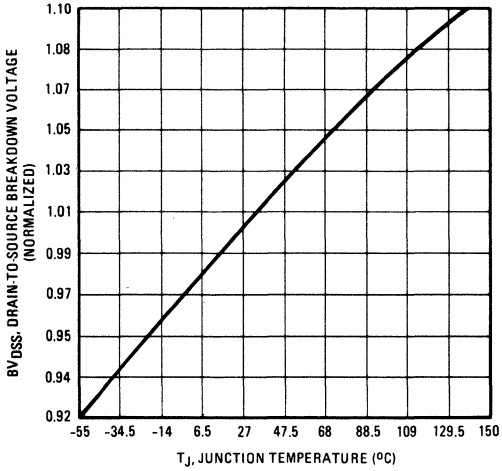


Fig. 8 — Breakdown Voltage Vs. Temperature

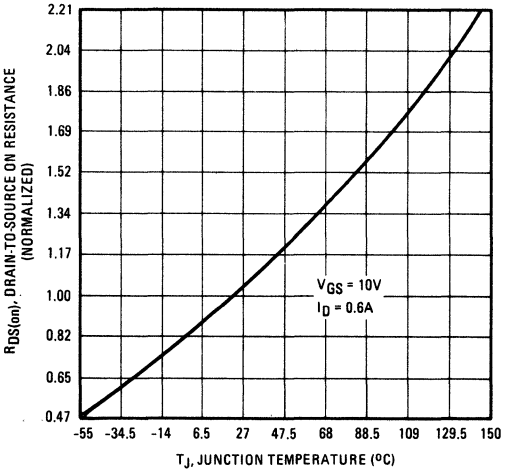


Fig. 9 — Normalized On-Resistance Vs. Temperature

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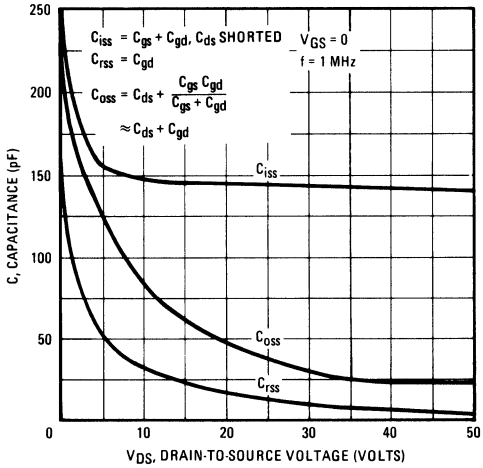


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

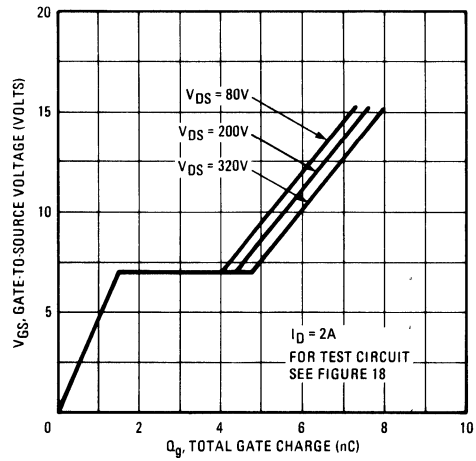


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

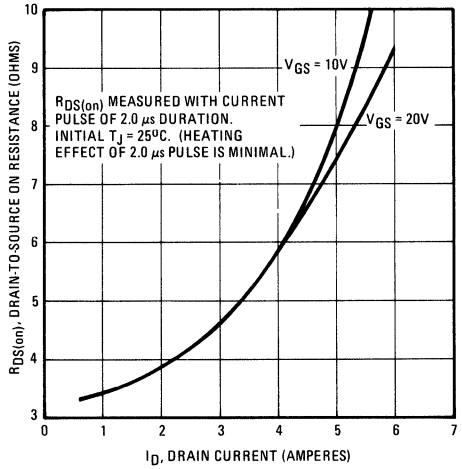


Fig. 12 — Typical On-Resistance Vs. Drain Current

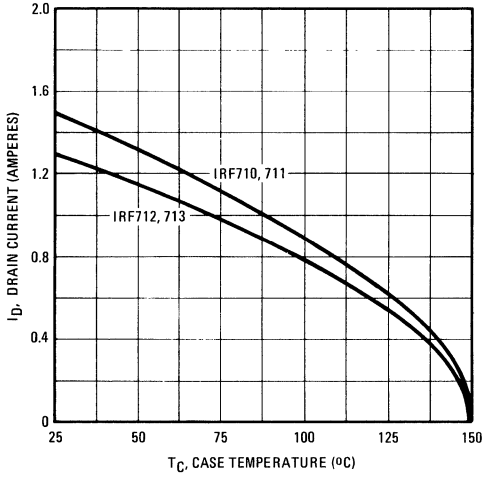


Fig. 13 — Maximum Drain Current Vs. Case Temperature

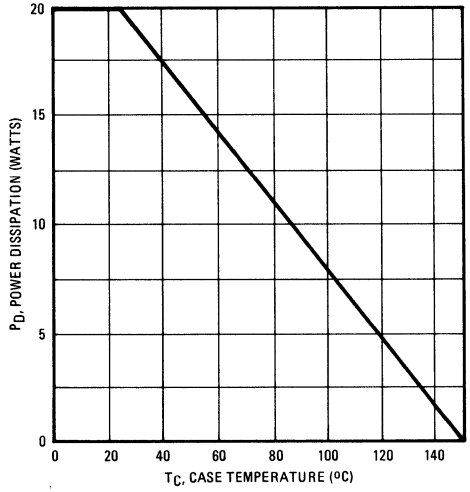


Fig. 14 — Power Vs. Temperature Derating Curve

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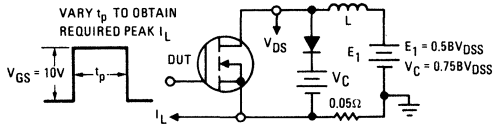


Fig. 15 — Clamped Inductive Test Circuit

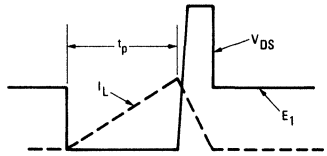


Fig. 16 — Clamped Inductive Waveforms

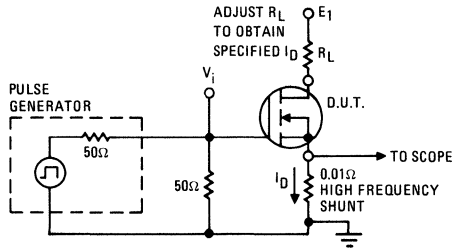


Fig. 17 — Switching Time Test Circuit

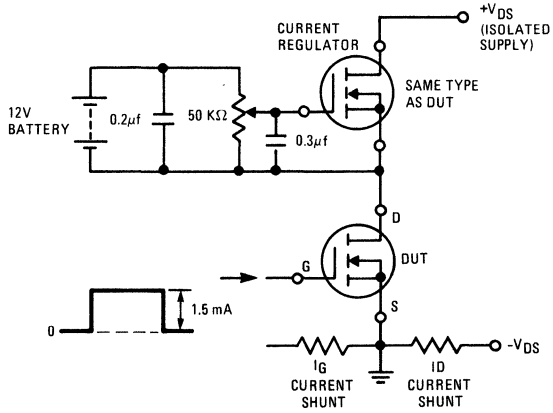


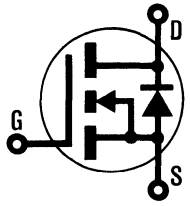
Fig. 18 — Gate Charge Test Circuit

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS

IRF720
IRF721
IRF722
IRF723



N-Channel

400 Volt, 1.8 Ohm HEXFET TO-220AB Plastic Package

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

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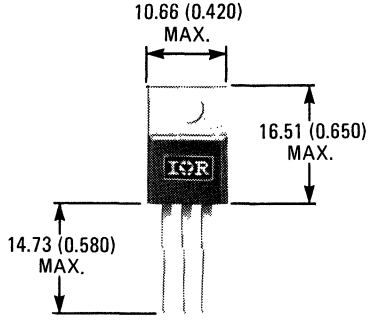
Features:

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

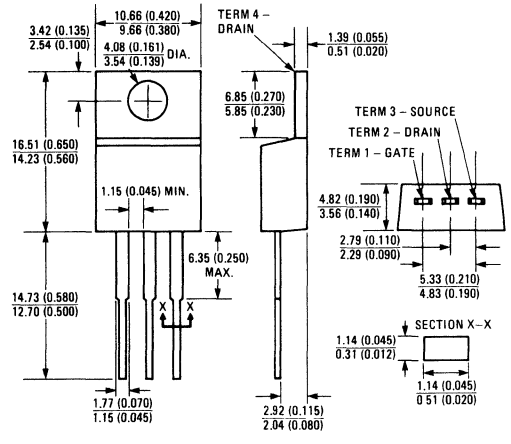
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF720	400V	1.8Ω	3.0A
IRF721	350V	1.8Ω	3.0A
IRF722	400V	2.5Ω	2.5A
IRF723	350V	2.5Ω	2.5A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Case Style TO-220AB
Dimensions in Millimeters and (Inches)

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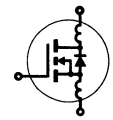
Absolute Maximum Ratings

Parameter		IRF720	IRF721	IRF722	IRF723	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_D @ T_C = 100°C	Continuous Drain Current	2.0	2.0	1.5	1.5	A
I_{DM}	Pulsed Drain Current ③	12	12	10	10	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		12	12	10	10	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF720 IRF722	400	–	–	V	V_{GS} = 0V
		IRF721 IRF723	350	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF720 IRF721	3.0	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		IRF722 IRF723	2.5	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF720 IRF721	–	1.5	1.8	Ω	V_{GS} = 10V, I_D = 1.5A
		IRF722 IRF723	–	1.8	2.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	2.0	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 1.5A
C_{iss}	Input Capacitance	ALL	–	450	600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	100	200	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	20	40	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 1.5A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	25	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	25	50	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	12	15	nC	V_{GS} = 10V, I_D = 4.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	6.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	6.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	3.12	K/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF720 IRF721	–	–	3.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF722 IRF723	–	–	2.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF720 IRF721	–	–	12	A	
		IRF722 IRF723	–	–	10	A	
V_{SD}	Diode Forward Voltage ②	IRF720 IRF721	–	–	1.6	V	T_C = 25°C, I_S = 3.0A, V_{GS} = 0V
		IRF722 IRF723	–	–	1.5	V	T_C = 25°C, I_S = 2.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	450	–	ns	T_J = 150°C, I_F = 3.0A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	3.1	–	μC	T_J = 150°C, I_F = 3.0A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

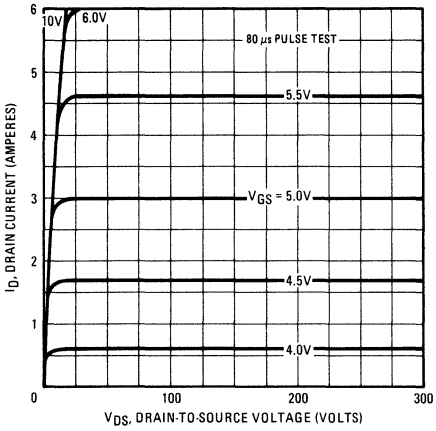


Fig. 1 – Typical Output Characteristics

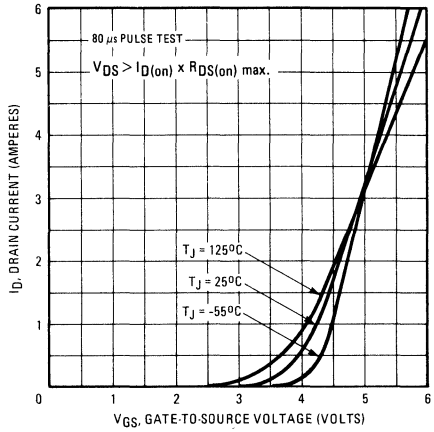


Fig. 2 – Typical Transfer Characteristics

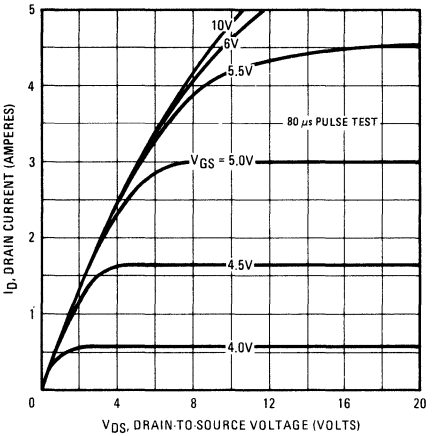


Fig. 3 – Typical Saturation Characteristics

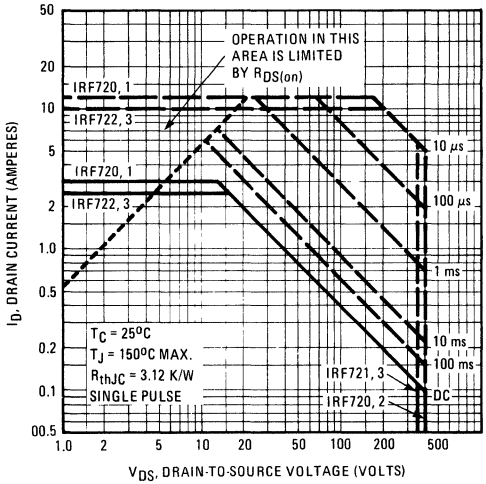


Fig. 4 – Maximum Safe Operating Area

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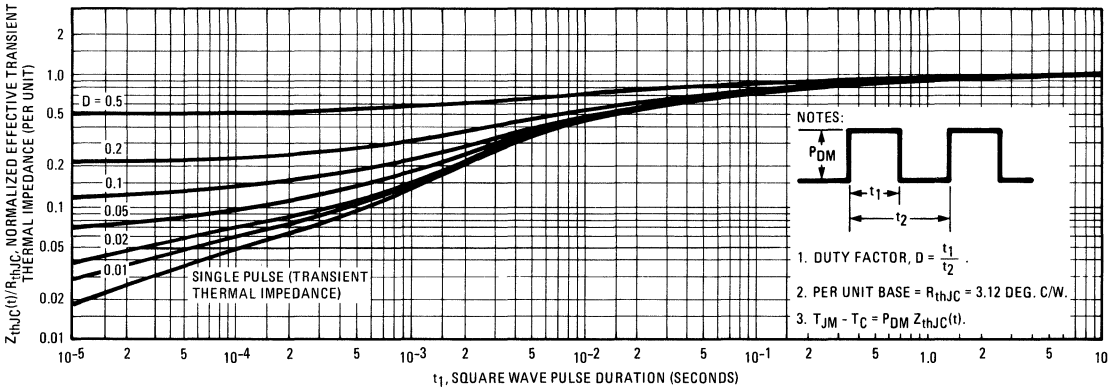


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

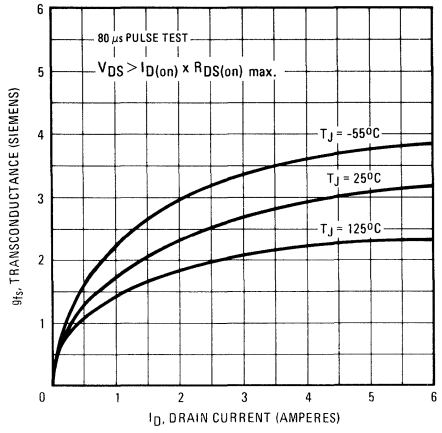


Fig. 6 — Typical Transconductance Vs. Drain Current

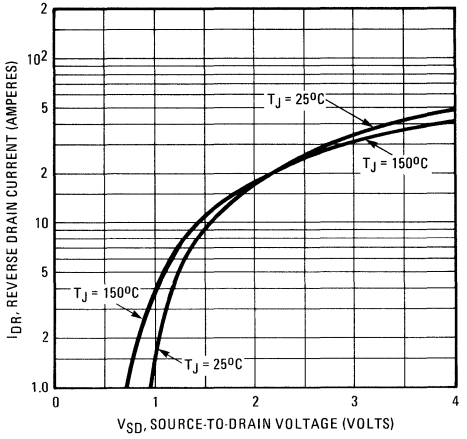


Fig. 7 — Typical Source-Drain Diode Forward Voltage

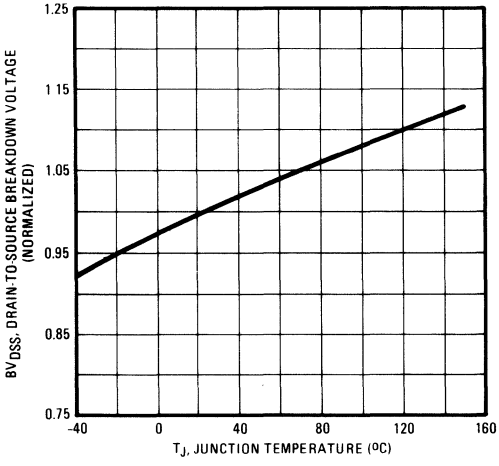


Fig. 8 — Breakdown Voltage Vs. Temperature

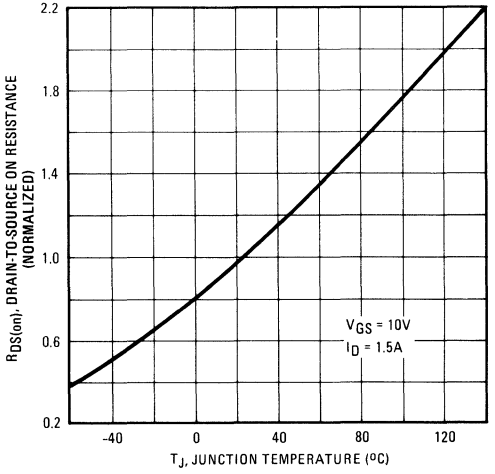


Fig. 9 — Normalized On-Resistance Vs. Temperature

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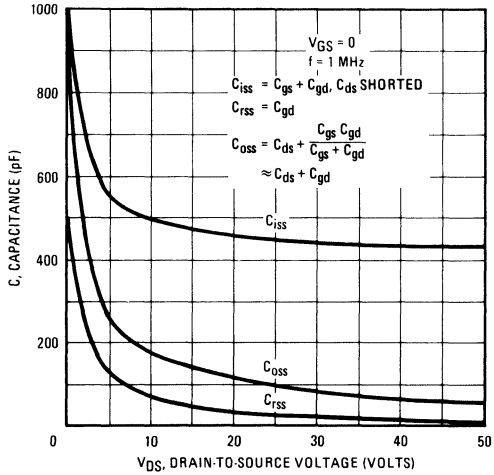


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

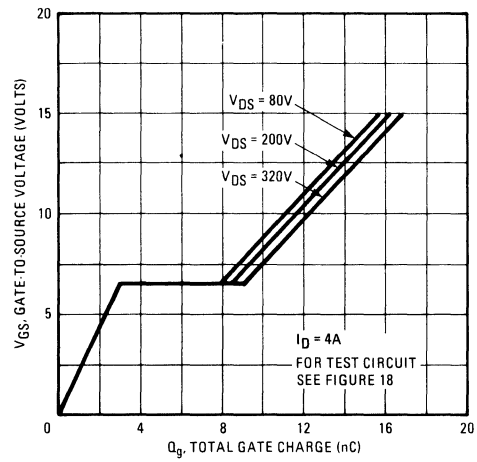


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

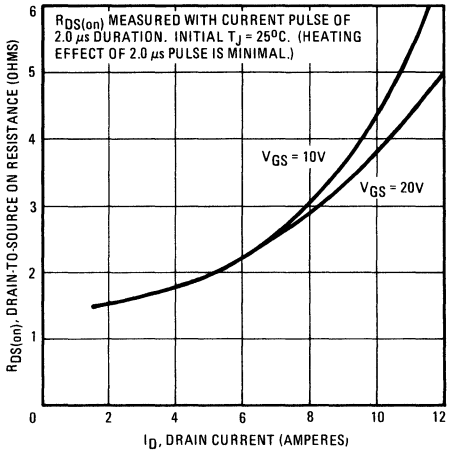


Fig. 12 — Typical On-Resistance Vs. Drain Current

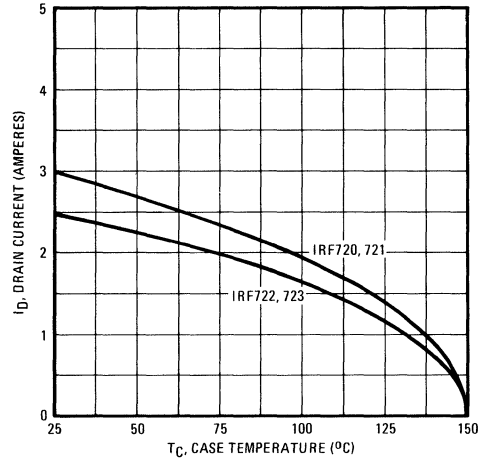


Fig. 13 — Maximum Drain Current Vs. Case Temperature

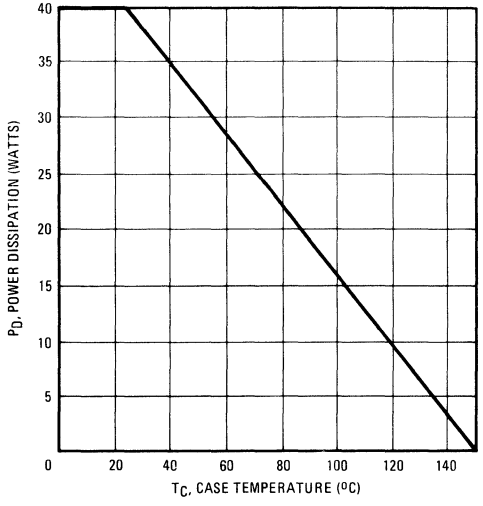


Fig. 14 — Power Vs. Temperature Derating Curve

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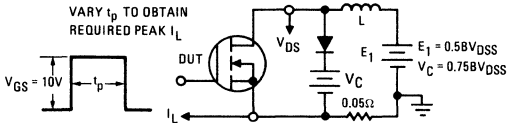


Fig. 15 — Clamped Inductive Test Circuit

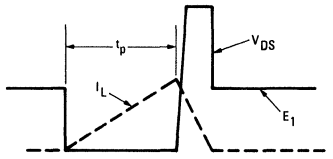


Fig. 16 — Clamped Inductive Waveforms

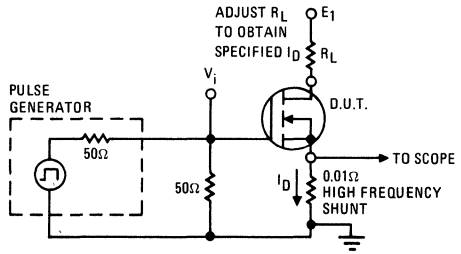


Fig. 17 — Switching Time Test Circuit

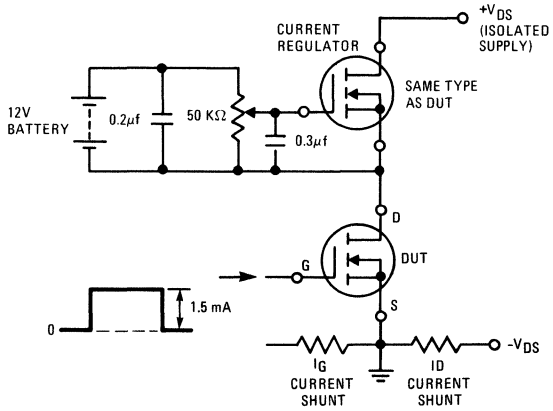


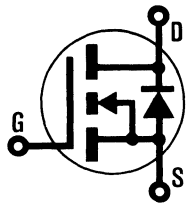
Fig. 18 — Gate Charge Test Circuit

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS

IRF730
IRF731
IRF732
IRF733



N-Channel

400 Volt, 1.0 Ohm HEXFET TO-220AB Plastic Package

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

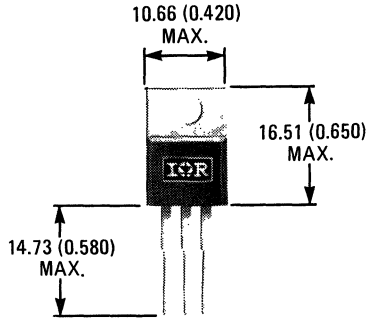
Features:

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

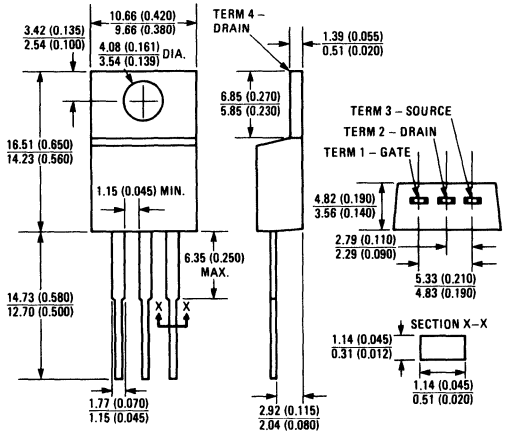
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF730	400V	1.0Ω	5.5A
IRF731	350V	1.0Ω	5.5A
IRF732	400V	1.5Ω	4.5A
IRF733	350V	1.5Ω	4.5A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Case Style TO-220AB
Dimensions in Millimeters and (Inches)

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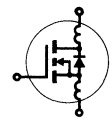
Absolute Maximum Ratings

Parameter		IRF730	IRF731	IRF732	IRF733	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	5.5	5.5	4.5	4.5	A
I_D @ T_C = 100°C	Continuous Drain Current	3.5	3.5	3.0	3.0	A
I_{DM}	Pulsed Drain Current ③	22	22	18	18	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		22	22	18	18	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF730 IRF732	400	–	–	V	V_{GS} = 0V
		IRF731 IRF733	350	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF730 IRF731	5.5	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF732 IRF733	4.5	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF730 IRF731	–	0.8	1.0	Ω	V_{GS} = 10V, I_D = 3.0A
		IRF732 IRF733	–	1.0	1.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	3.0	4.0	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 3.0A
C_{iss}	Input Capacitance	ALL	–	600	800	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	150	300	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	40	80	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} ≈ 175V, I_D = 3.0A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	35	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	55	ns	
t_f	Fall Time	ALL	–	–	35	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	18	30	nC	V_{GS} = 10V, I_D = 7.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	11	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	7.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67	K/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF730 IRF731	–	–	5.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF732 IRF733	–	–	4.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF730 IRF731	–	–	22	A	
		IRF732 IRF733	–	–	18	A	
V_{SD}	Diode Forward Voltage ②	IRF730 IRF731	–	–	1.6	V	T_C = 25°C, I_S = 5.5A, V_{GS} = 0V
		IRF732 IRF733	–	–	1.5	V	T_C = 25°C, I_S = 4.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	600	–	ns	T_J = 150°C, I_F = 5.5A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.0	–	μC	T_J = 150°C, I_F = 5.5A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

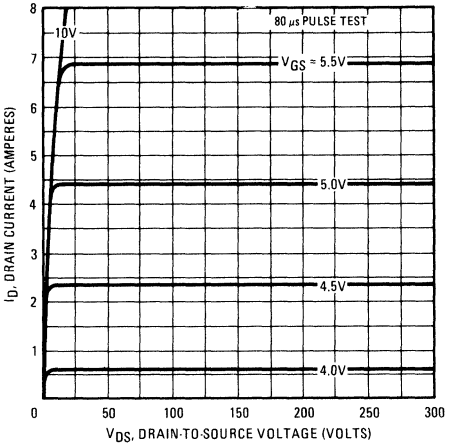


Fig. 1 — Typical Output Characteristics

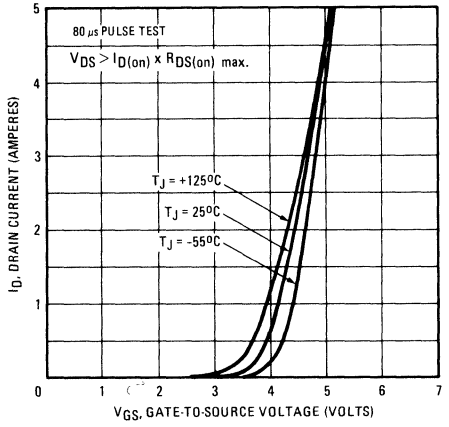


Fig. 2 — Typical Transfer Characteristics

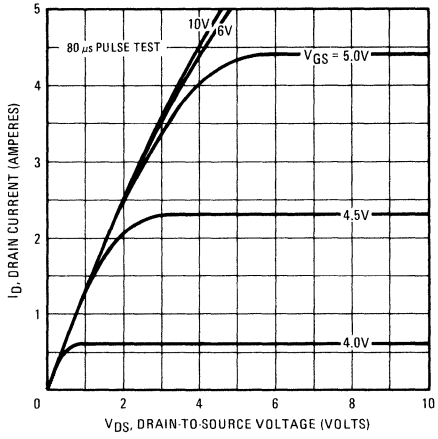


Fig. 3 — Typical Saturation Characteristics

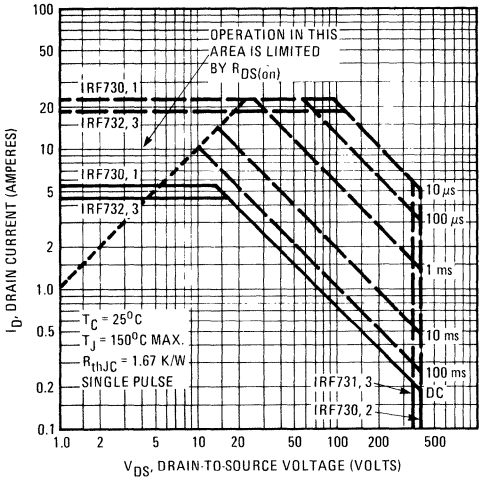


Fig. 4 — Maximum Safe Operating Area

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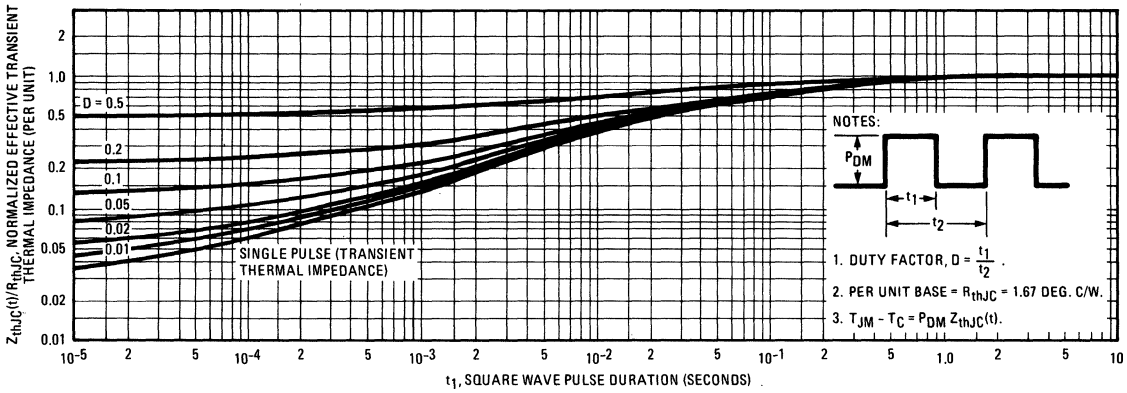


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

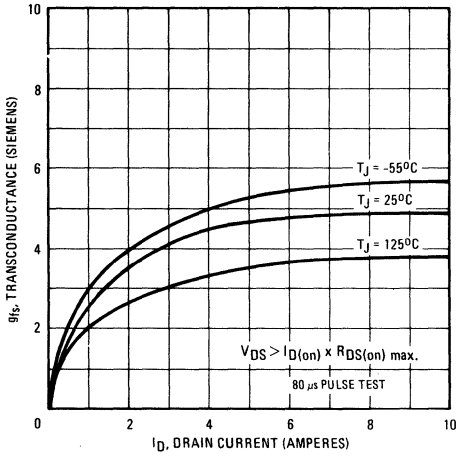


Fig. 6 — Typical Transconductance Vs. Drain Current

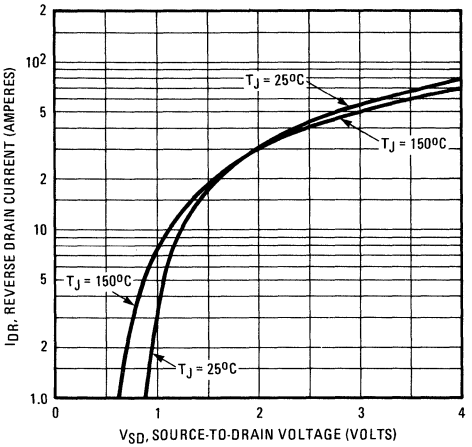


Fig. 7 — Typical Source-Drain Diode Forward Voltage

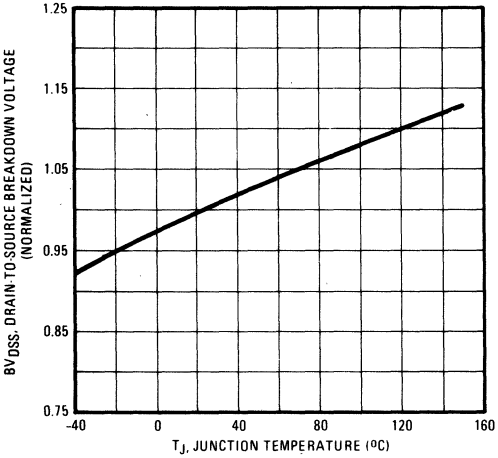


Fig. 8 — Breakdown Voltage Vs. Temperature

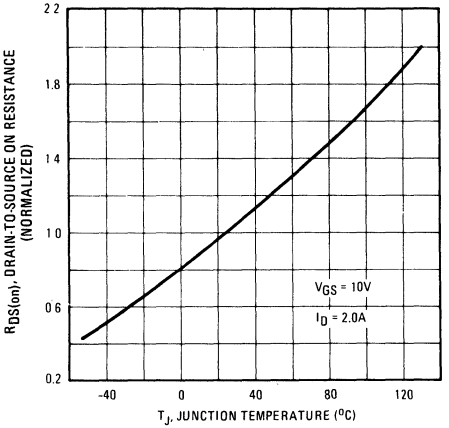


Fig. 9 — Normalized On-Resistance Vs. Temperature

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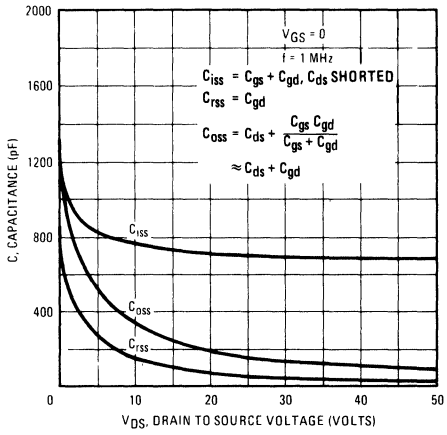


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

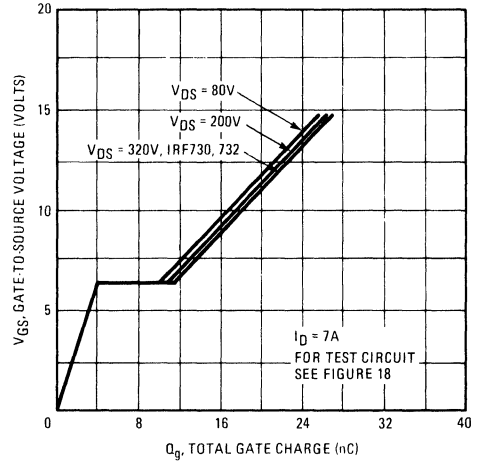


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

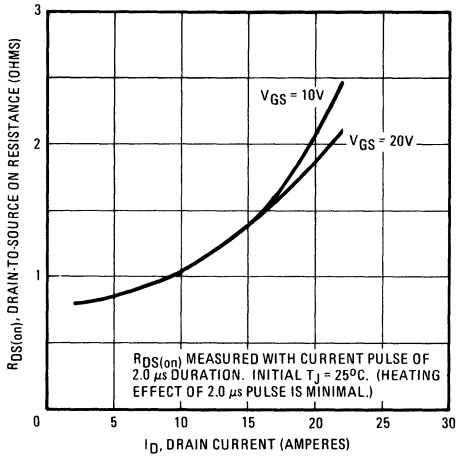


Fig. 12 — Typical On-Resistance Vs. Drain Current

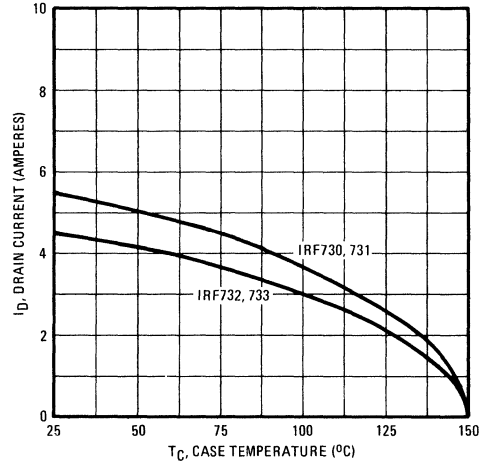


Fig. 13 — Maximum Drain Current Vs. Case Temperature

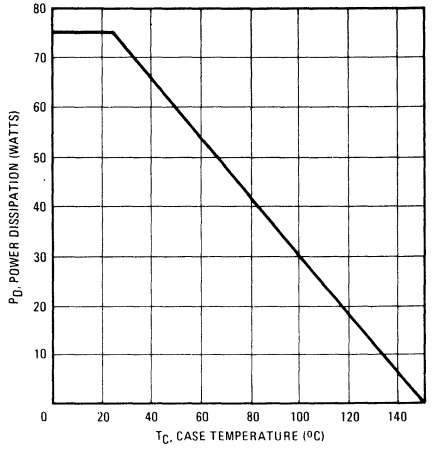


Fig. 14 — Power Vs. Temperature Derating Curve

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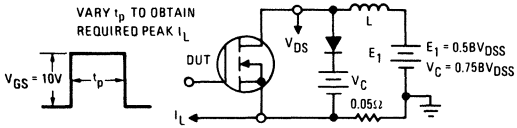


Fig. 15 — Clamped Inductive Test Circuit

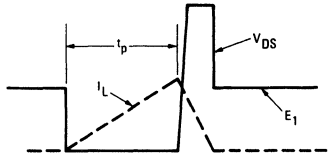


Fig. 16 — Clamped Inductive Waveforms

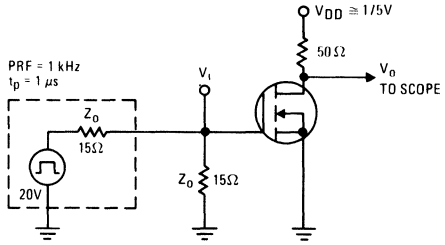


Fig. 17 — Switching Time Test Circuit

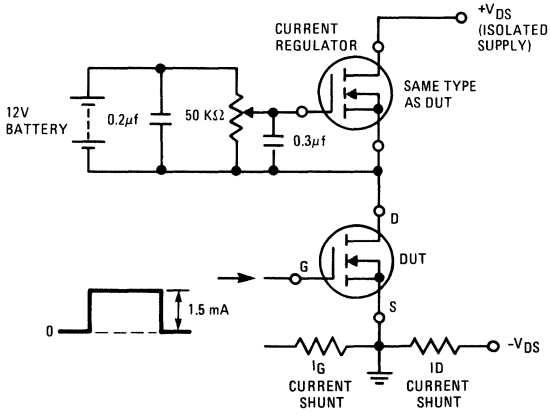


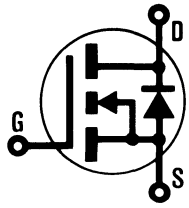
Fig. 18 — Gate Charge Test Circuit

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS IRF740

N-CHANNEL POWER MOSFETs



IRF741
IRF742
IRF743

400 Volt, 0.55 Ohm HEXFET TO-220AB Plastic Package

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

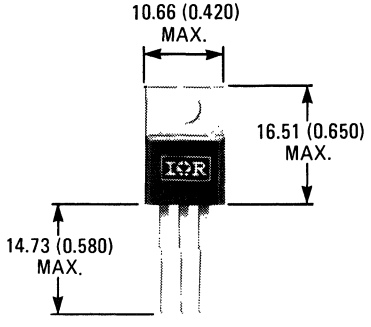
Features:

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

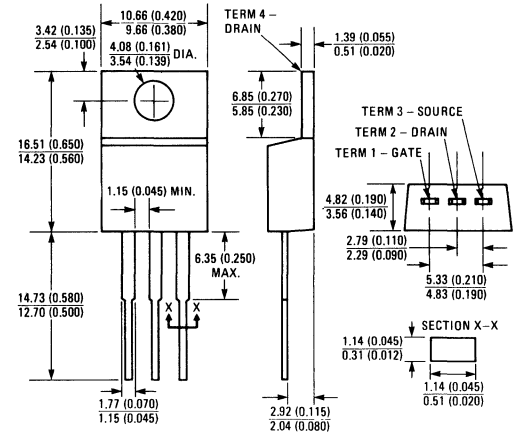
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF740	400V	0.55Ω	10A
IRF741	350V	0.55Ω	10A
IRF742	400V	0.80Ω	8.0A
IRF743	350V	0.80Ω	8.0A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Case Style TO-220AB
Dimensions in Millimeters and (Inches)

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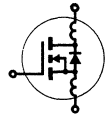
Absolute Maximum Ratings

Parameter		IRF740	IRF741	IRF742	IRF743	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	10	10	8.0	8.0	A
I_D @ T_C = 100°C	Continuous Drain Current	6.0	6.0	5.0	5.0	A
I_{DM}	Pulsed Drain Current ③	40	40	32	32	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 40	40	32	32	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF740 IRF742	400	–	–	V	V_{GS} = 0V
		IRF741 IRF743	350	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF740 IRF741	10	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF742 IRF743	8.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF740 IRF741	–	0.47	0.55	Ω	V_{GS} = 10V, I_D = 5.0A
		IRF742 IRF743	–	.68	.80	Ω	
g_{fs}	Forward Transconductance ②	ALL	4.0	7.0	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 5.0A
C_{iss}	Input Capacitance	ALL	–	1250	1600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	300	450	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	80	150	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	17	35	ns	V_{DD} ≈ 175V, I_D = 5.0A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	5.0	15	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	45	90	ns	
t_f	Fall Time	ALL	–	16	35	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	41	60	nC	V_{GS} = 10V, I_D = 12A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	18	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	23	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.0	K/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF740 IRF741	–	–	10	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF742 IRF743	–	–	8.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF740 IRF741	–	–	40	A	
		IRF742 IRF743	–	–	32	A	
V_{SD}	Diode Forward Voltage ②	IRF740 IRF741	–	–	2.0	V	T_C = 25°C, I_S = 10A, V_{GS} = 0V
		IRF742 IRF743	–	–	1.9	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	800	–	ns	T_J = 150°C, I_F = 10A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	5.7	–	μC	T_J = 150°C, I_F = 10A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

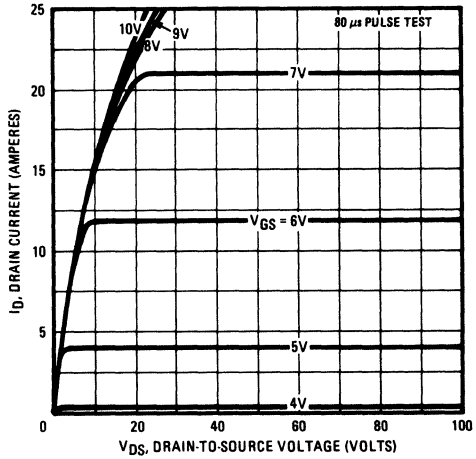


Fig. 1 — Typical Output Characteristics

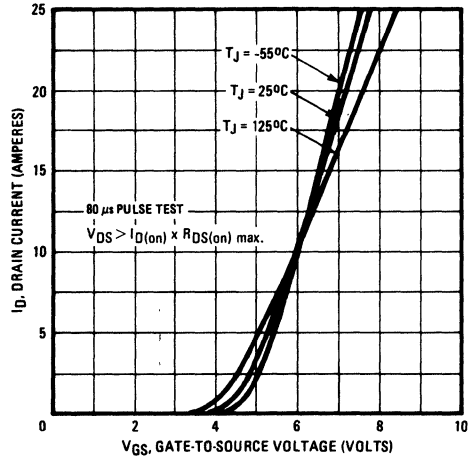


Fig. 2 — Typical Transfer Characteristics

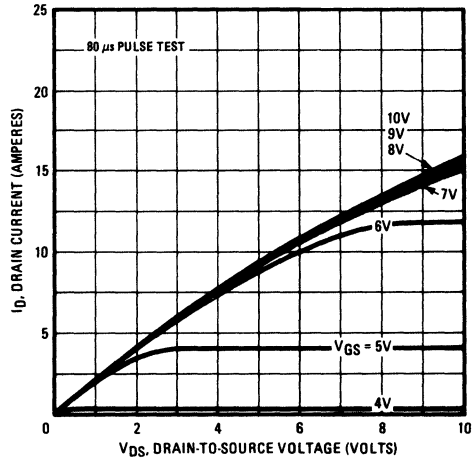


Fig. 3 — Typical Saturation Characteristics

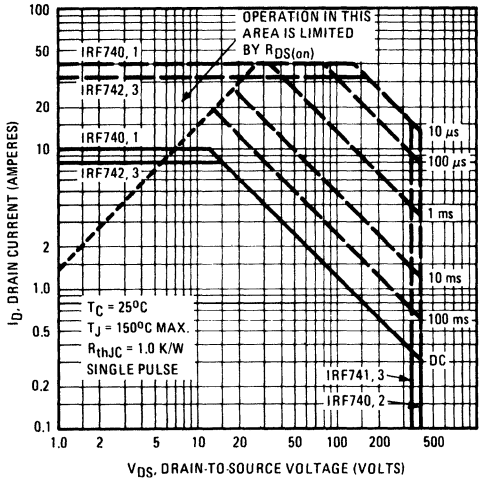


Fig. 4 — Maximum Safe Operating Area

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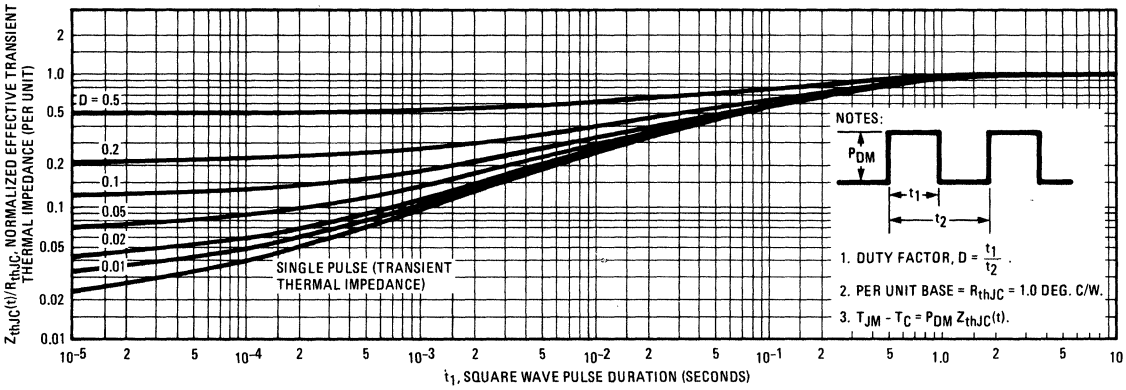


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

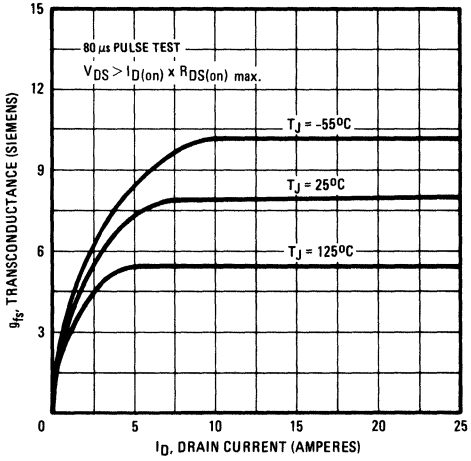


Fig. 6 — Typical Transconductance Vs. Drain Current

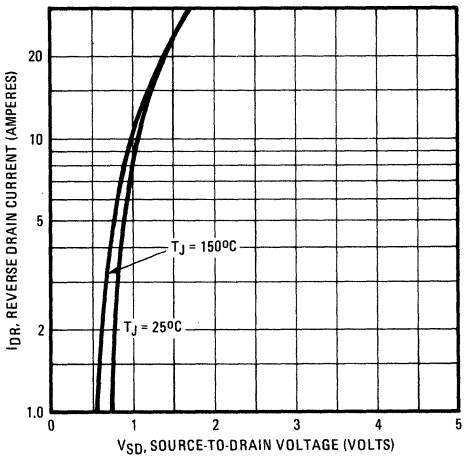


Fig. 7 — Typical Source-Drain Diode Forward Voltage

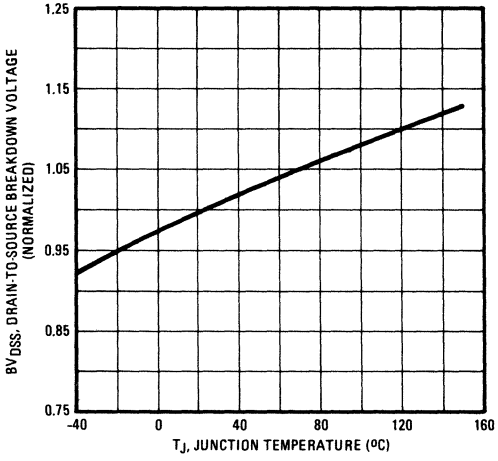


Fig. 8 — Breakdown Voltage Vs. Temperature

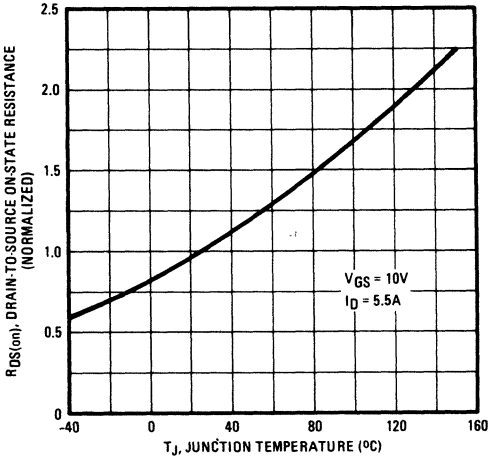


Fig. 9 — Normalized On-Resistance Vs. Temperature

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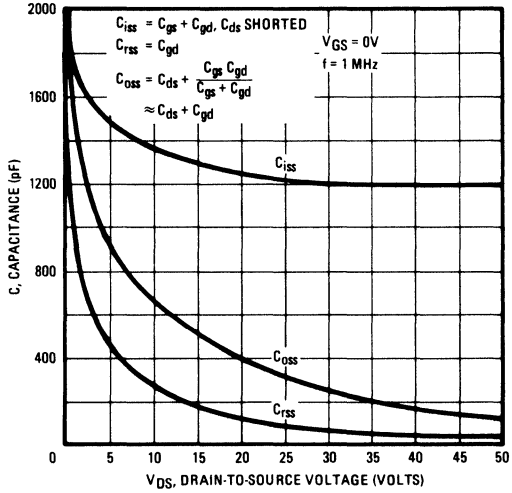


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

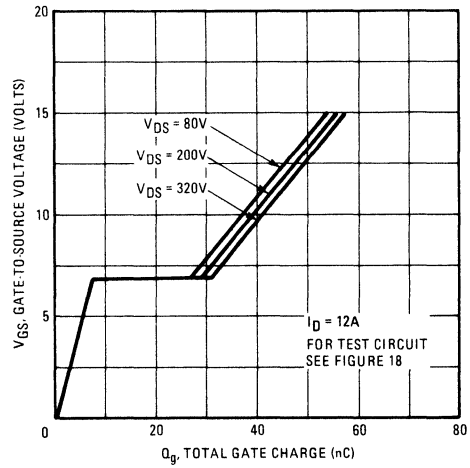


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

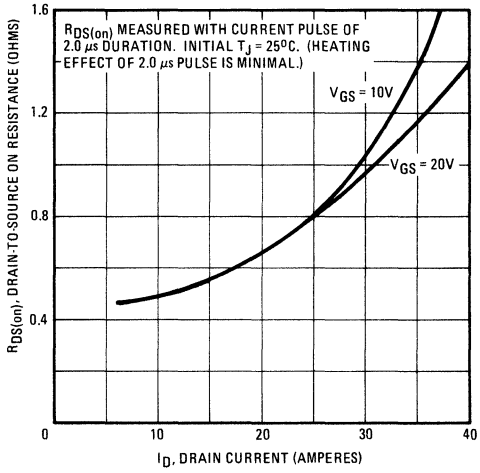


Fig. 12 — Typical On-Resistance Vs. Drain Current

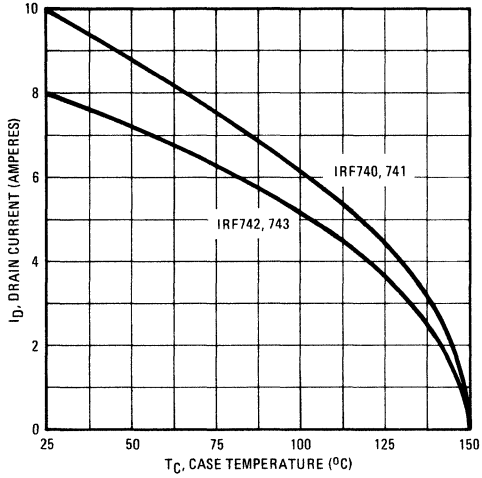


Fig. 13 — Maximum Drain Current Vs. Case Temperature

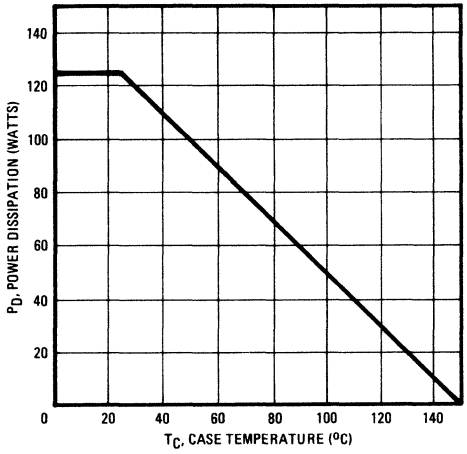


Fig. 14 — Power Vs. Temperature Derating Curve

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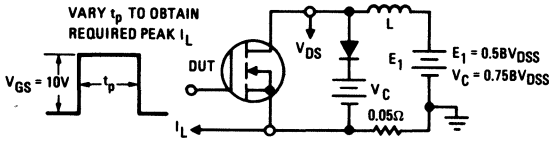


Fig. 15 — Clamped Inductive Test Circuit

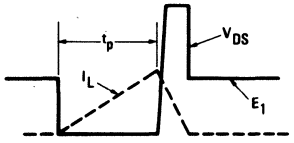


Fig. 16 — Clamped Inductive Waveforms

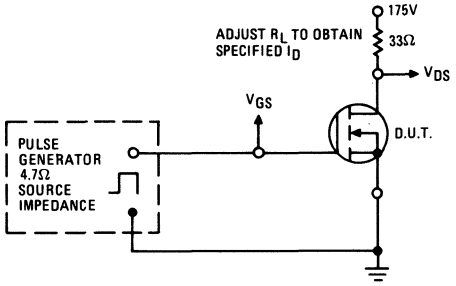


Fig. 17 — Switching Time Test Circuit

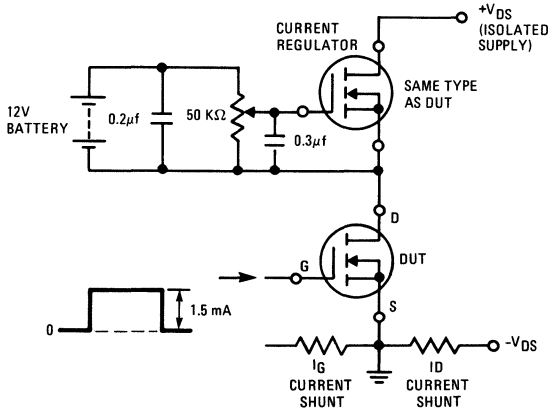


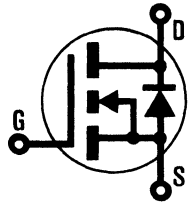
Fig. 18 — Gate Charge Test Circuit

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS

IRF820
IRF821
IRF822
IRF823



N-Channel

500 Volt, 3.0 Ohm HEXFET TO-220AB Plastic Package

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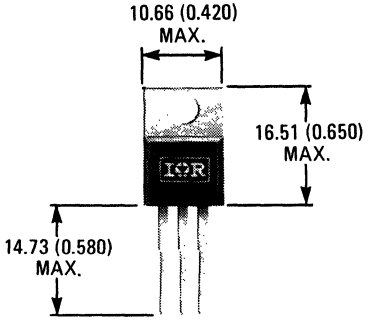
Features:

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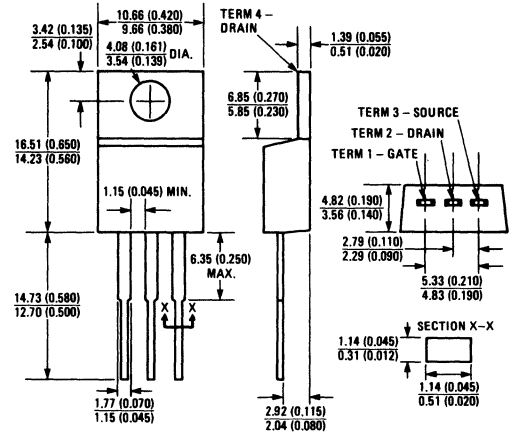
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF820	500V	3.0Ω	2.5A
IRF821	450V	3.0Ω	2.5A
IRF822	500V	4.0Ω	2.0A
IRF823	450V	4.0Ω	2.0A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Case Style TO-220AB
Dimensions in Millimeters and (Inches)

Downloaded from Arrow.com.

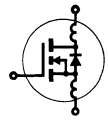
Absolute Maximum Ratings

Parameter		IRF820	IRF821	IRF822	IRF823	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	2.5	2.5	2.0	2.0	A
I_D @ T_C = 100°C	Continuous Drain Current	1.5	1.5	1.0	1.0	A
I_{DM}	Pulsed Drain Current ③	10	10	8.0	8.0	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 10	10	8.0	8.0	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF820 IRF822	500	–	–	V	V_{GS} = 0V
		IRF821 IRF823	450	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	−500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF820 IRF821	2.5	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF822 IRF823	2.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF820 IRF821	–	2.5	3.0	Ω	V_{GS} = 10V, I_D = 1.0A
		IRF822 IRF823	–	3.0	4.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	1.75	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 1.0A
C_{iss}	Input Capacitance	ALL	–	300	400	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	75	150	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	20	40	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	30	60	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 1.0A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	25	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	30	60	ns	
t_f	Fall Time	ALL	–	15	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	11	15	nC	V_{GS} = 10V, I_D = 3.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	5.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	6.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	3.12	K/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF820 IRF821	–	–	2.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF822 IRF823	–	–	2.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF820 IRF821	–	–	10	A	
		IRF822 IRF823	–	–	8.0	A	
V_{SD}	Diode Forward Voltage ②	IRF820 IRF821	–	–	1.6	V	T_C = 25°C, I_S = 2.5A, V_{GS} = 0V
		IRF822 IRF823	–	–	1.5	V	T_C = 25°C, I_S = 2.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	600	–	ns	T_J = 150°C, I_F = 2.5A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	3.5	–	μC	T_J = 150°C, I_F = 2.5A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

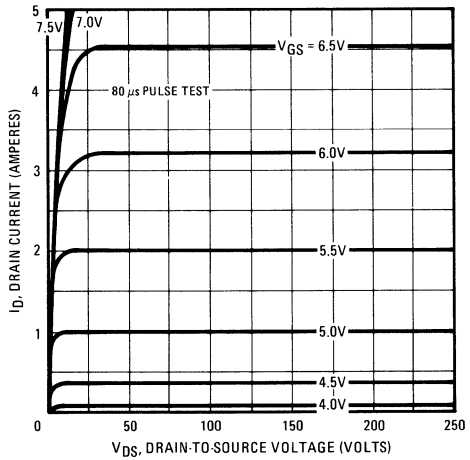


Fig. 1 — Typical Output Characteristics

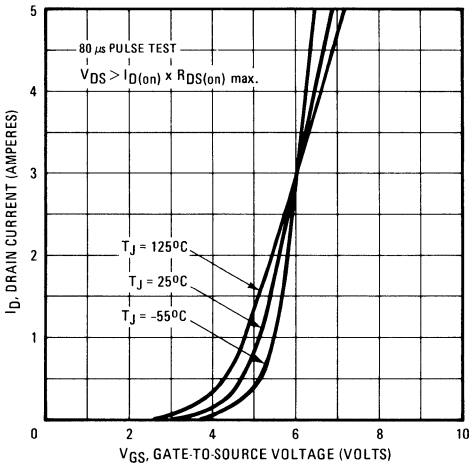


Fig. 2 — Typical Transfer Characteristics

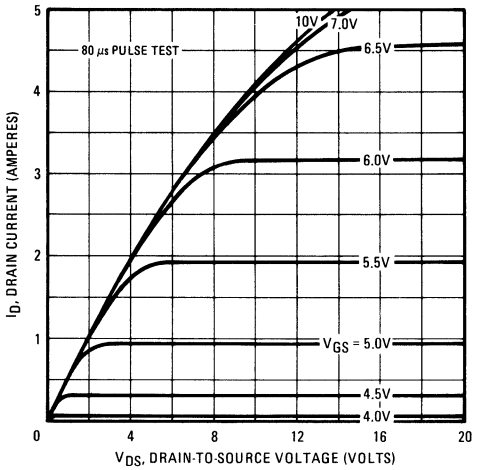


Fig. 3 — Typical Saturation Characteristics

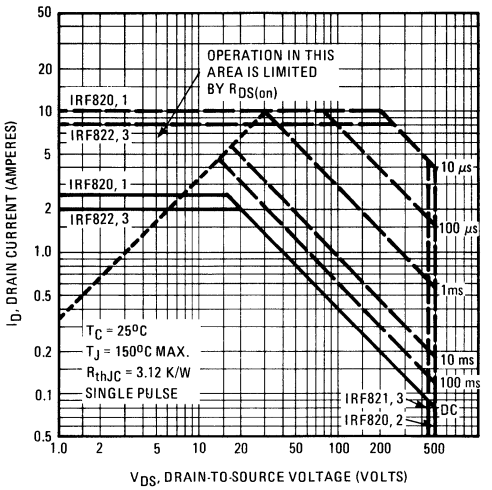


Fig. 4 — Maximum Safe Operating Area

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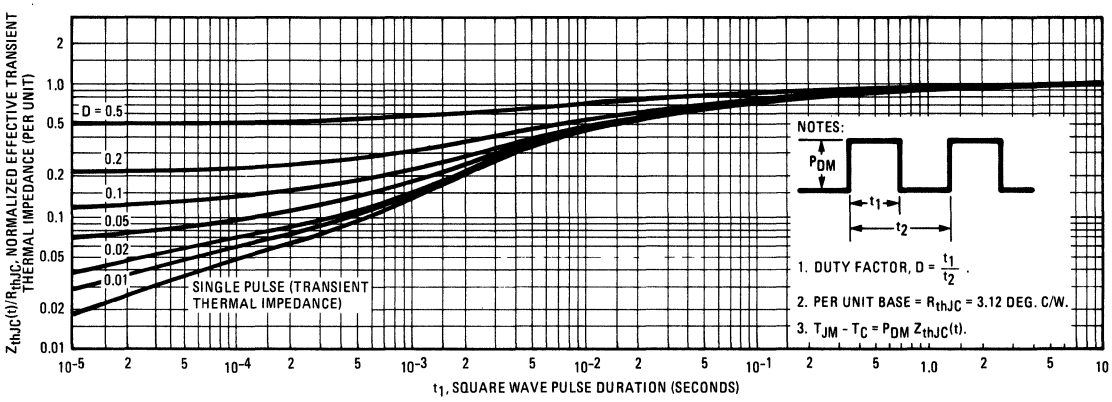


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

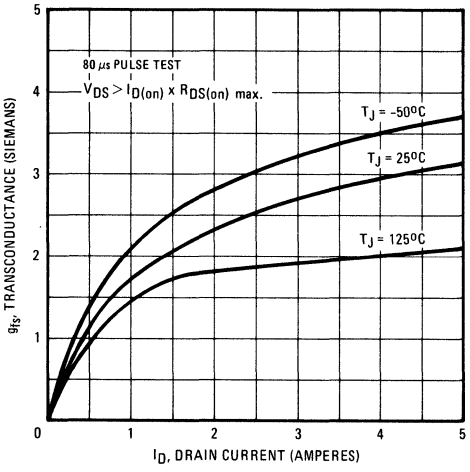


Fig. 6 — Typical Transconductance Vs. Drain Current

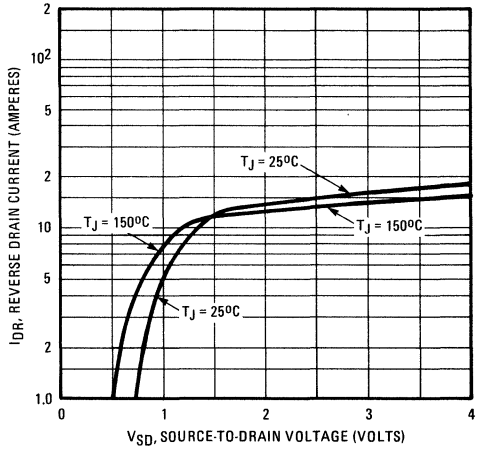


Fig. 7 — Typical Source-Drain Diode Forward Voltage

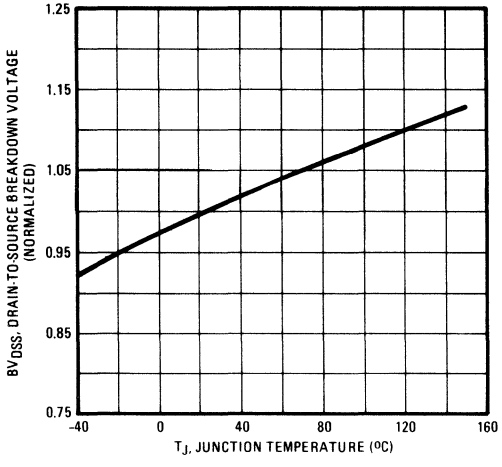


Fig. 8 — Breakdown Voltage Vs. Temperature

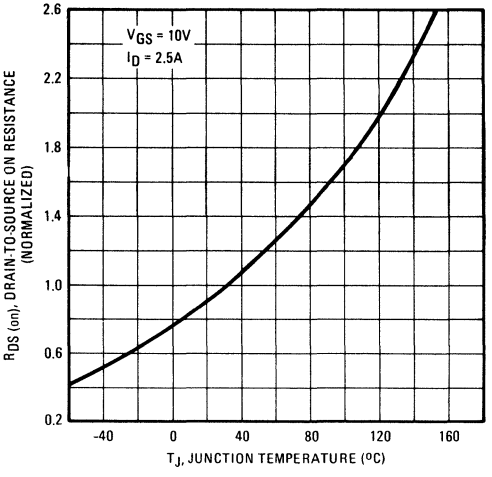


Fig. 9 — Normalized On-Resistance Vs. Temperature

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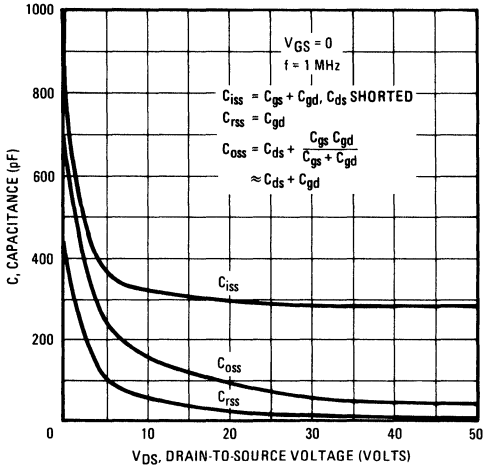


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

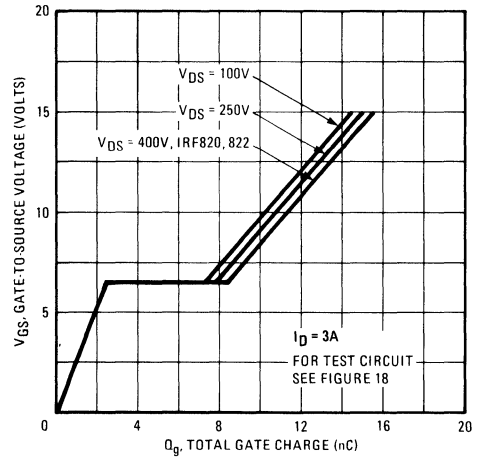


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

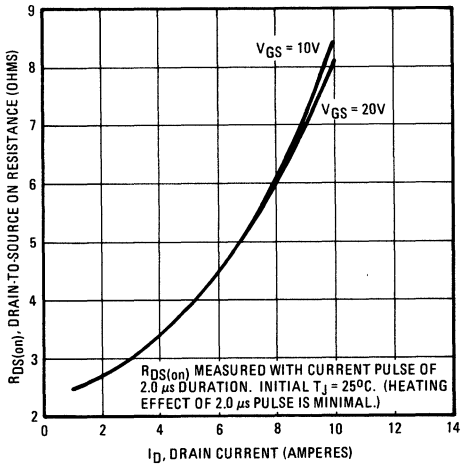


Fig. 12 — Typical On-Resistance Vs. Drain Current

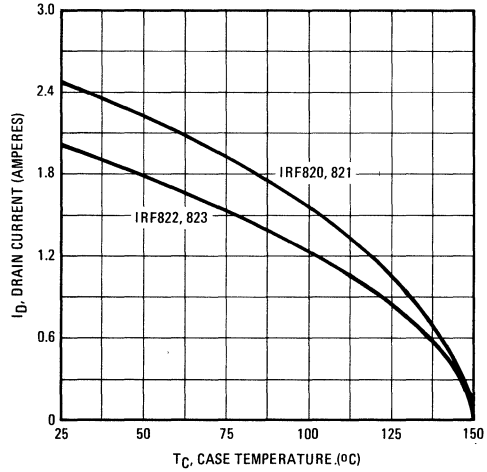


Fig. 13 — Maximum Drain Current Vs. Case Temperature

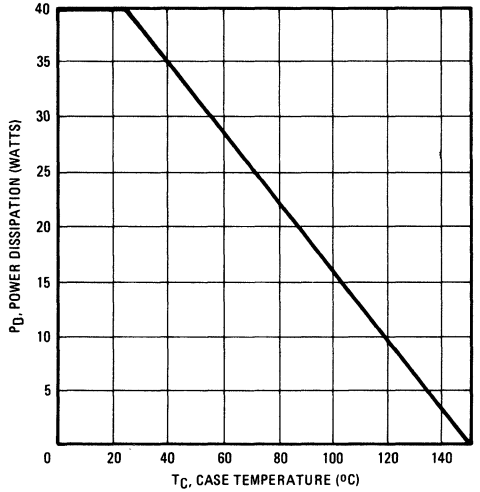


Fig. 14 — Power Vs. Temperature Derating Curve

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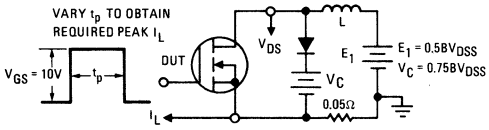


Fig. 15 — Clamped Inductive Test Circuit

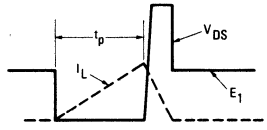


Fig. 16 — Clamped Inductive Waveforms

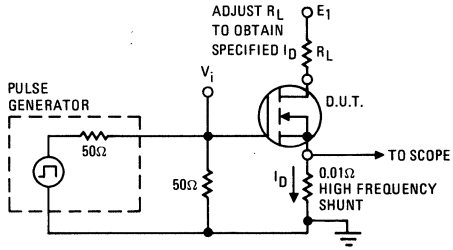


Fig. 17 — Switching Time Test Circuit

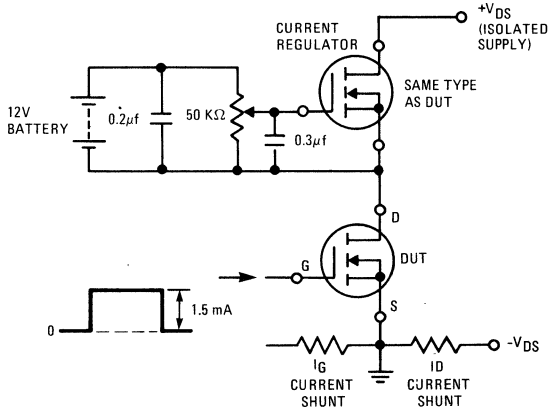


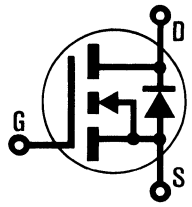
Fig. 18 — Gate Charge Test Circuit

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS

IRF830
IRF831
IRF832
IRF833



N-Channel

500 Volt, 1.5 Ohm HEXFET
TO-220AB Plastic Package

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

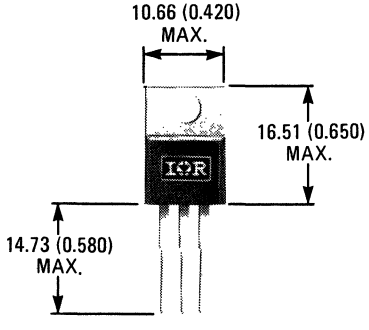
Features:

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

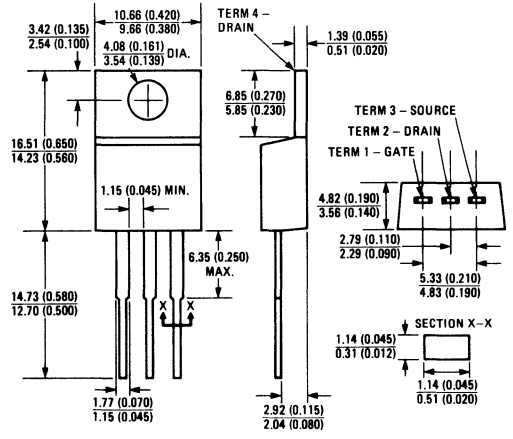
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF830	500V	1.5Ω	4.5A
IRF831	450V	1.5Ω	4.5A
IRF832	500V	2.0Ω	4.0A
IRF833	450V	2.0Ω	4.0A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Case Style TO-220AB
Dimensions in Millimeters and (Inches)

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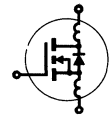
Absolute Maximum Ratings

Parameter		IRF830	IRF831	IRF832	IRF833	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	4.5	4.5	4.0	4.0	A
I_D @ T_C = 100°C	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_{DM}	Pulsed Drain Current ③	18	18	16	16	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		18	18	16	16	
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF830 IRF832	500	–	–	V	V_{GS} = 0V
		IRF831 IRF833	450	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF830 IRF831	4.5	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF832 IRF833	4.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF830 IRF831	–	1.3	1.5	Ω	V_{GS} = 10V, I_D = 2.5A
		IRF832 IRF833	–	1.5	2.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	2.5	3.25	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 2.5A
C_{iss}	Input Capacitance	ALL	–	600	800	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	100	200	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	30	60	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} ≈ 225V, I_D = 2.5A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	30	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	55	ns	
t_f	Fall Time	ALL	–	–	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	22	30	nC	V_{GS} = 10V, I_D = 6.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	11	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	11	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67	K/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF830 IRF831	–	–	4.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF832 IRF833	–	–	4.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF830 IRF831	–	–	18	A	
		IRF832 IRF833	–	–	16	A	
V_{SD}	Diode Forward Voltage ②	IRF830 IRF831	–	–	1.6	V	T_C = 25°C, I_S = 4.5A, V_{GS} = 0V
		IRF832 IRF833	–	–	1.5	V	T_C = 25°C, I_S = 4.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	800	–	ns	T_J = 150°C, I_F = 4.5A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.6	–	μC	T_J = 150°C, I_F = 4.5A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

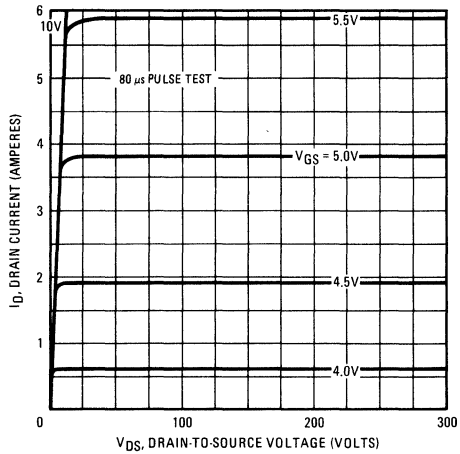


Fig. 1 — Typical Output Characteristics

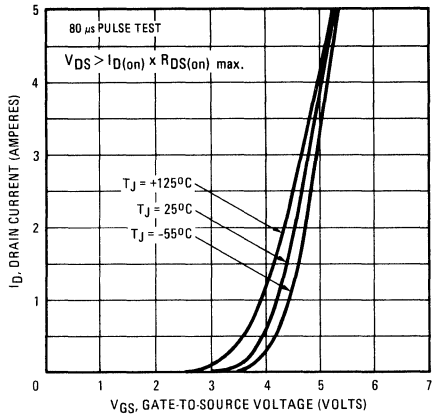


Fig. 2 — Typical Transfer Characteristics

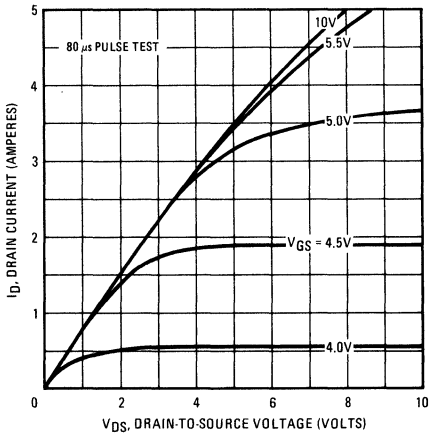


Fig. 3 — Typical Saturation Characteristics

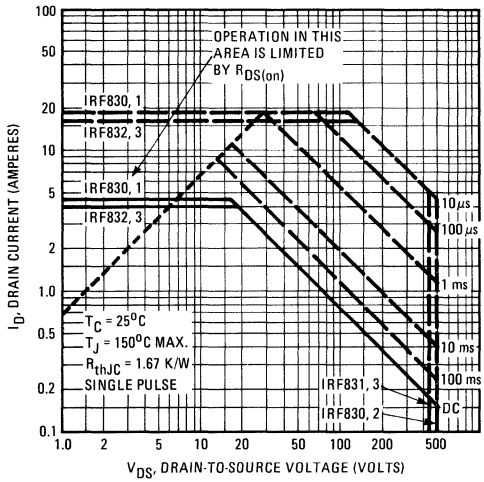


Fig. 4 — Maximum Safe Operating Area

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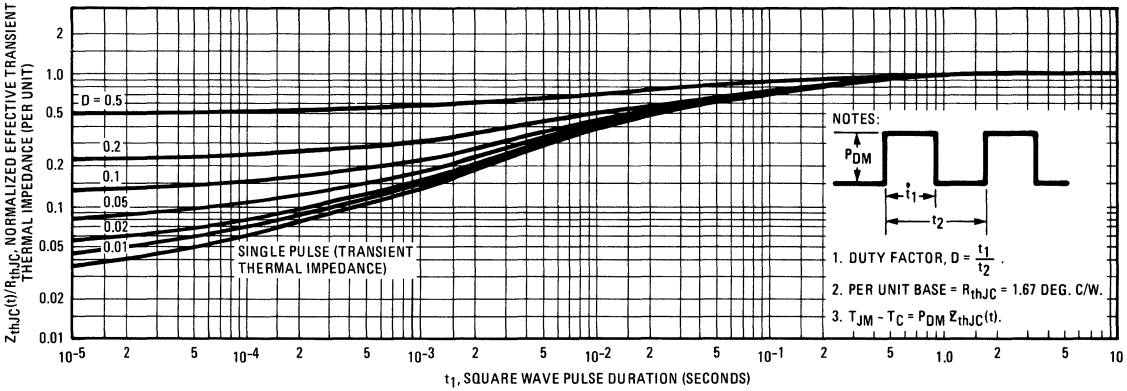


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

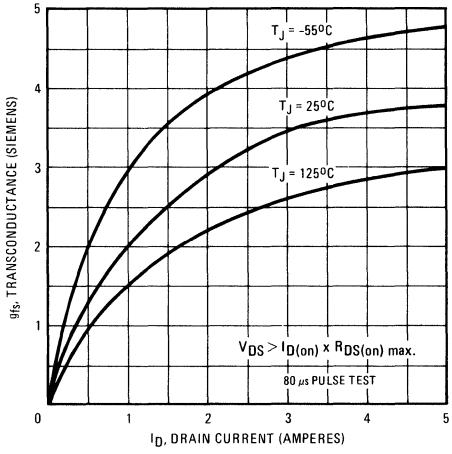


Fig. 6 — Typical Transconductance Vs. Drain Current

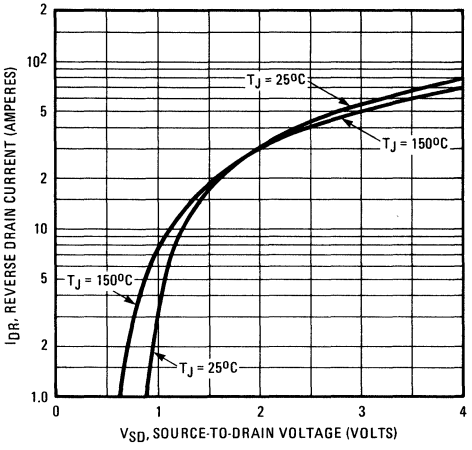


Fig. 7 — Typical Source-Drain Diode Forward Voltage

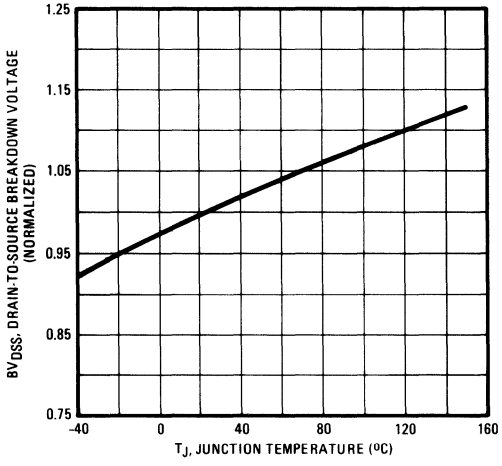


Fig. 8 — Breakdown Voltage Vs. Temperature

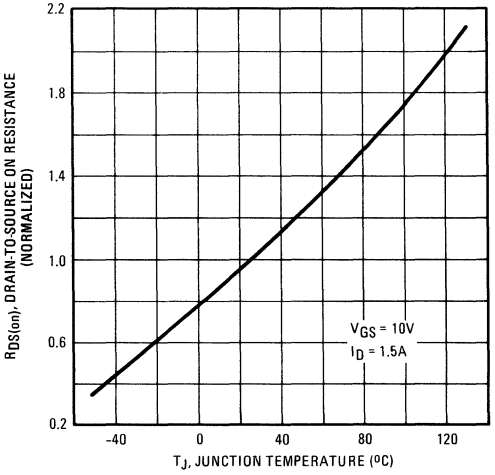


Fig. 9 — Normalized On-Resistance Vs. Temperature

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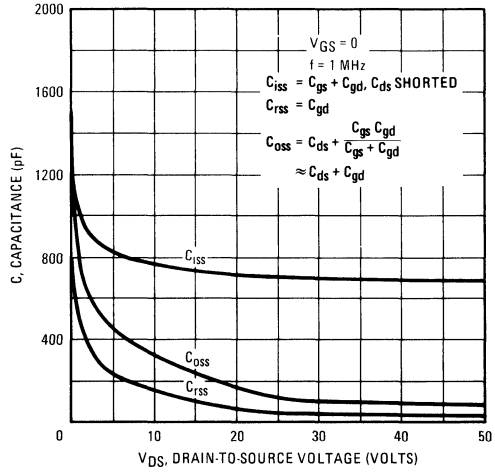


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

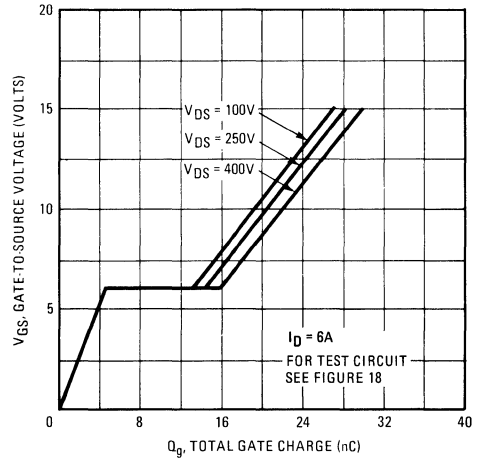


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

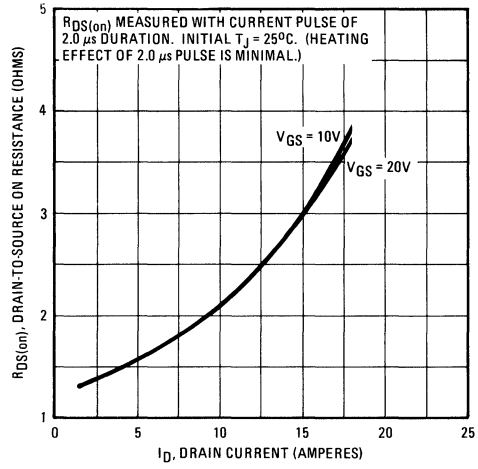


Fig. 12 — Typical On-Resistance Vs. Drain Current

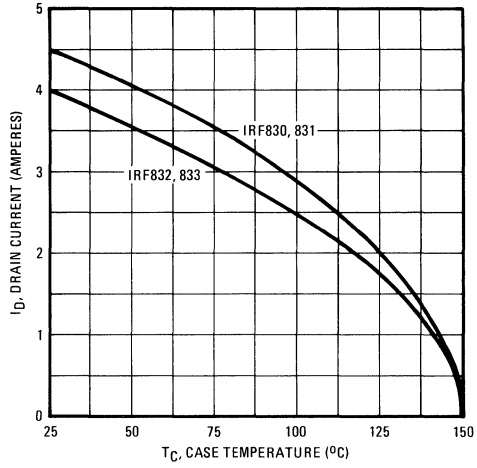


Fig. 13 — Maximum Drain Current Vs. Case Temperature

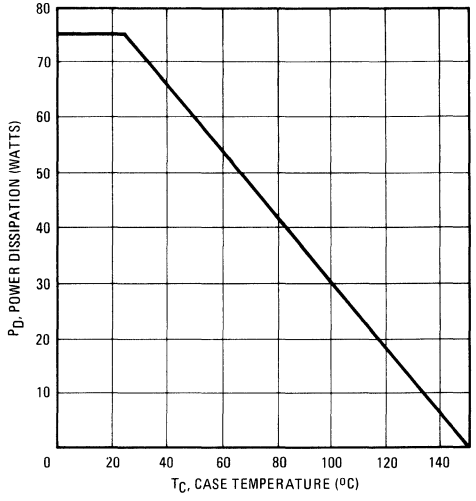


Fig. 14 — Power Vs. Temperature Derating Curve

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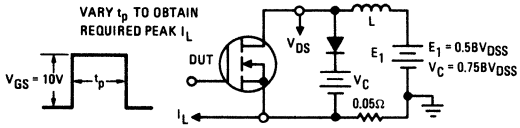


Fig. 15 — Clamped Inductive Test Circuit

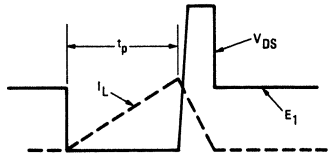


Fig. 16 — Clamped Inductive Waveforms

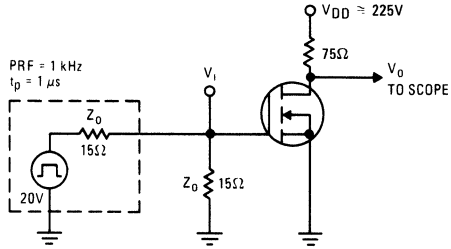


Fig. 17 — Switching Time Test Circuit

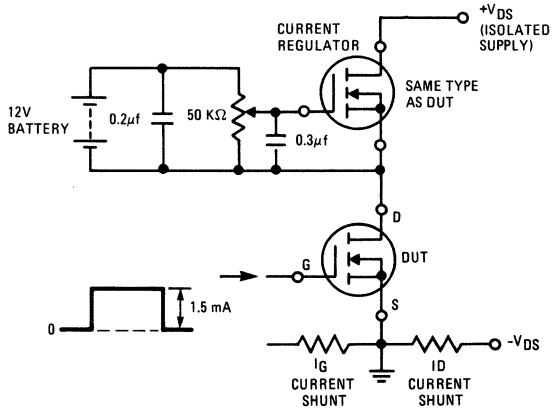


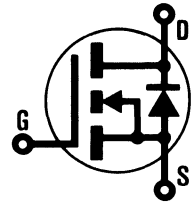
Fig. 18 — Gate Charge Test Circuit

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS IRF840 IRF841 IRF842 IRF843

N-CHANNEL POWER MOSFETs



500 Volt, 0.85 Ohm HEXFET TO-220AB Plastic Package

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

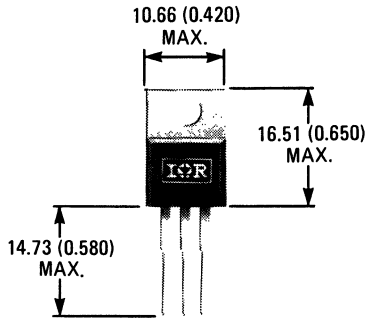
Features:

- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

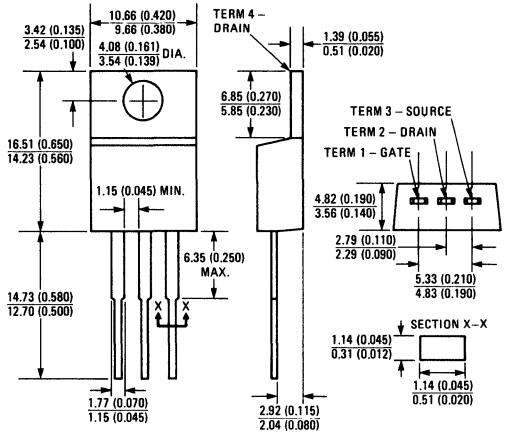
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF840	500V	0.85Ω	8.0A
IRF841	450V	0.85Ω	8.0A
IRF842	500V	1.10Ω	7.0A
IRF843	450V	1.10Ω	7.0A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Case Style TO-220AB
Dimensions in Millimeters and (Inches)

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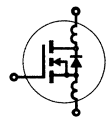
Absolute Maximum Ratings

Parameter		IRF840	IRF841	IRF842	IRF843	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_D @ T_C = 100°C	Continuous Drain Current	5.0	5.0	4.0	4.0	A
I_{DM}	Pulsed Drain Current ③	32	32	28	28	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	125 (See Fig. 14)				W
	Linear Derating Factor	1.0 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	32	(See Fig. 15 and 16) L = 100μH 32	28	28	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF840 IRF842	500	–	–	V	V_{GS} = 0V
		IRF841 IRF843	450	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF840 IRF841	8.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF842 IRF843	7.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF840 IRF841	–	0.1	1.0	Ω	V_{GS} = 10V, I_D = 4.0A
		IRF842 IRF843	–	0.2	4.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	4.0	6.5	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 4.0A
C_{iss}	Input Capacitance	ALL	–	1225	1600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	200	350	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	85	150	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	17	35	ns	V_{DD} ≈ 200V, I_D = 4.0A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	5	15	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	42	90	ns	
t_f	Fall Time	ALL	–	14	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	42	60	nC	V_{GS} = 10V, I_D = 10A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	20	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	22	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.0	K/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF840 IRF841	—	—	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF842 IRF843	—	—	7.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF840 IRF841	—	—	32	A	
		IRF842 IRF843	—	—	28	A	
V_{SD}	Diode Forward Voltage ②	IRF840 IRF841	—	—	2.0	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 100A/μs
		IRF842 IRF843	—	—	1.9	V	T_C = 25°C, I_S = 7.0A, V_{GS} = 100A/μs
t_{rr}	Reverse Recovery Time	ALL	—	1100	—	ns	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	6.4	—	μC	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

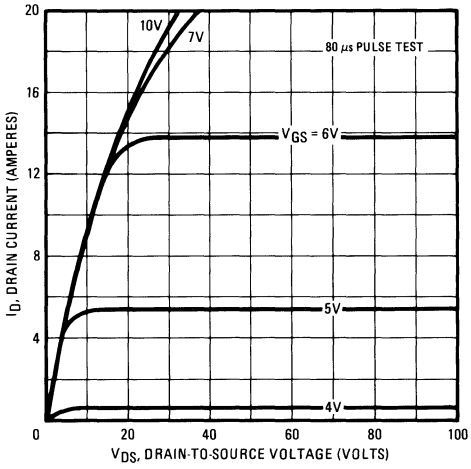


Fig. 1 — Typical Output Characteristics

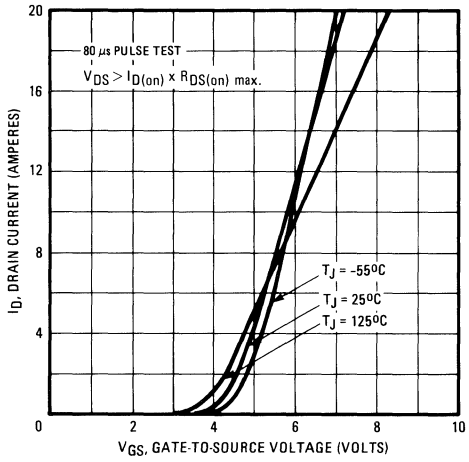


Fig. 2 — Typical Transfer Characteristics

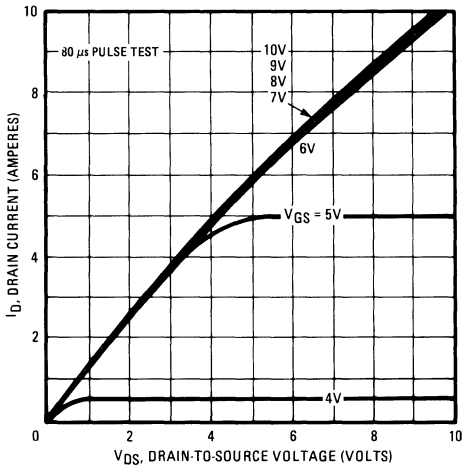


Fig. 3 — Typical Saturation Characteristics

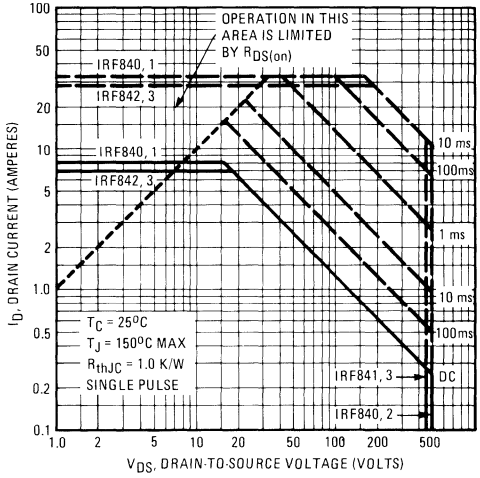


Fig. 4 — Maximum Safe Operating Area

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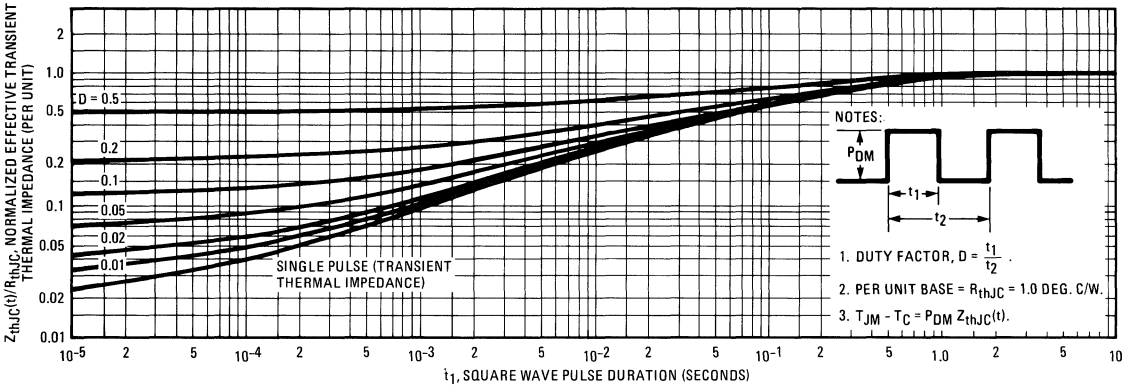


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

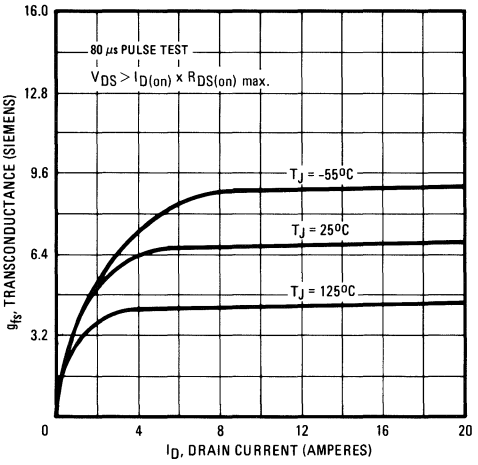


Fig. 6 — Typical Transconductance Vs. Drain Current

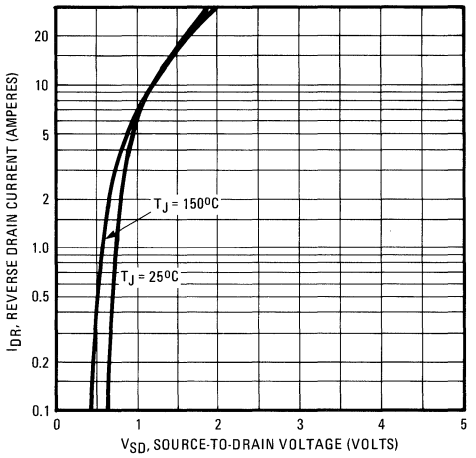


Fig. 7 — Typical Source-Drain Diode Forward Voltage

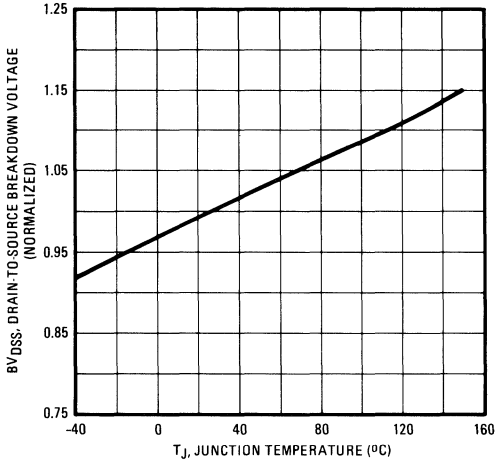


Fig. 8 — Breakdown Voltage Vs. Temperature

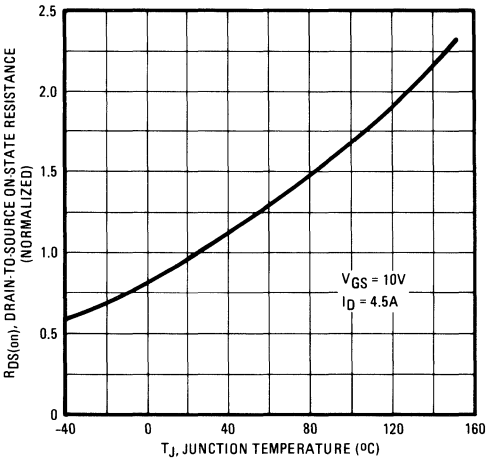


Fig. 9 — Normalized On-Resistance Vs. Temperature

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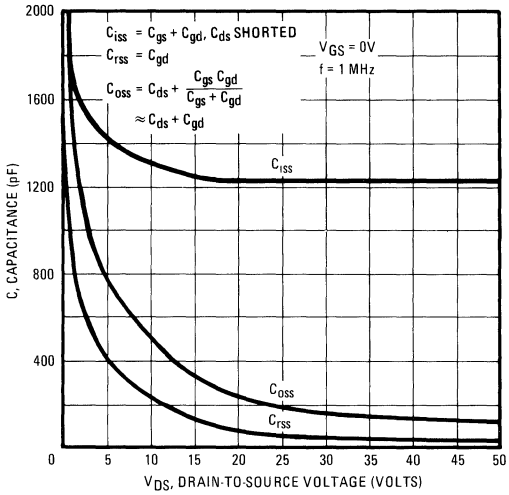


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

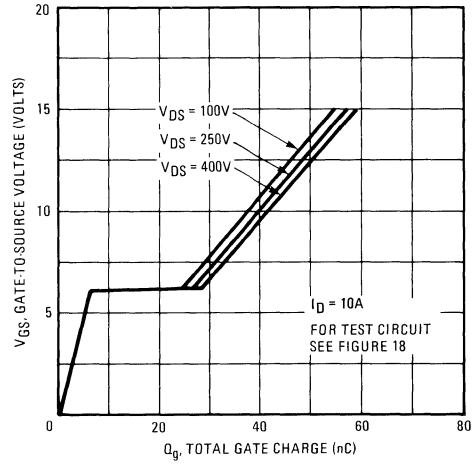


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

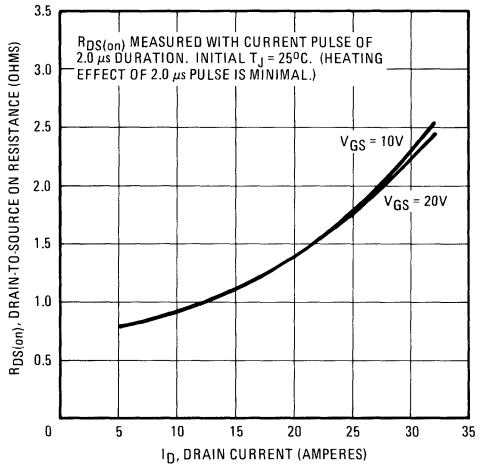


Fig. 12 — Typical On-Resistance Vs. Drain Current

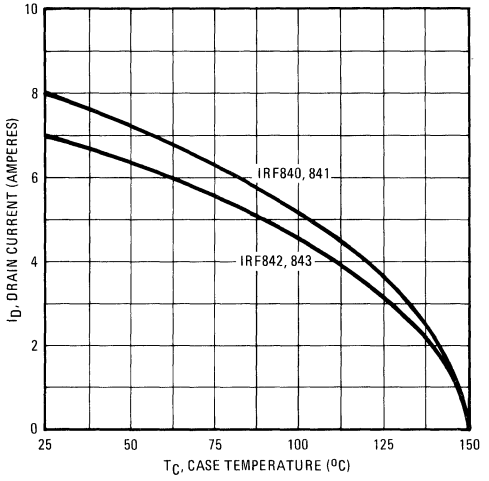


Fig. 13 — Maximum Drain Current Vs. Case Temperature

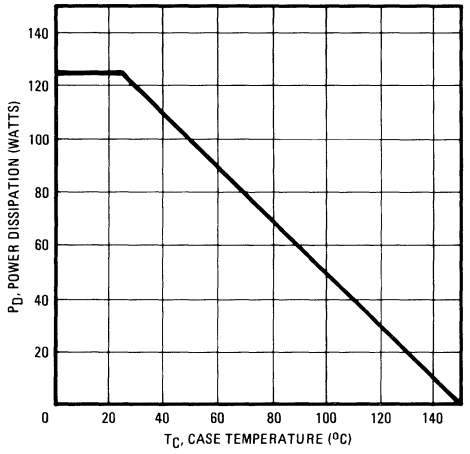


Fig. 14 — Power Vs. Temperature Derating Curve

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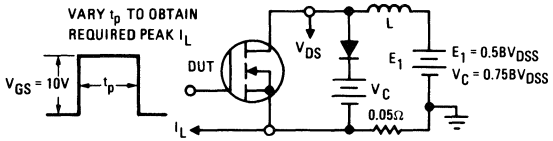


Fig. 15 — Clamped Inductive Test Circuit

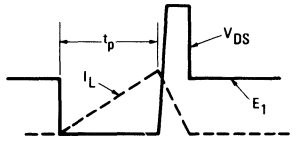


Fig. 16 — Clamped Inductive Waveforms

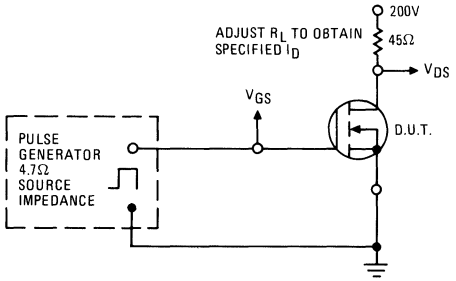


Fig. 17 — Switching Time Test Circuit

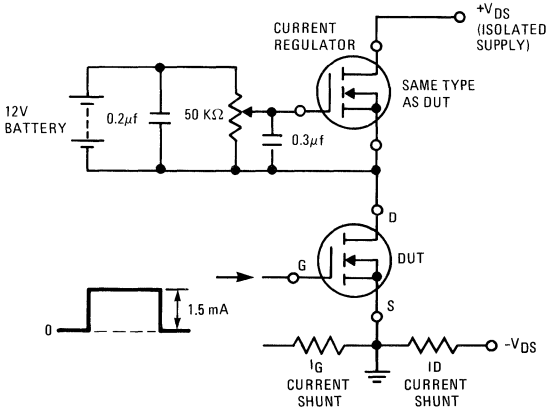


Fig. 18 — Gate Charge Test Circuit

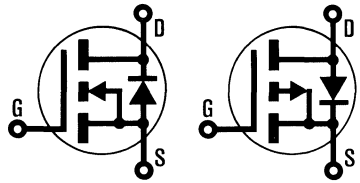
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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS IRF5522

IRF5523

MOSFET COMPLEMENTARY PAIRS



100 Volt Complementary HEXFETs TO-220AB Plastic Package

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

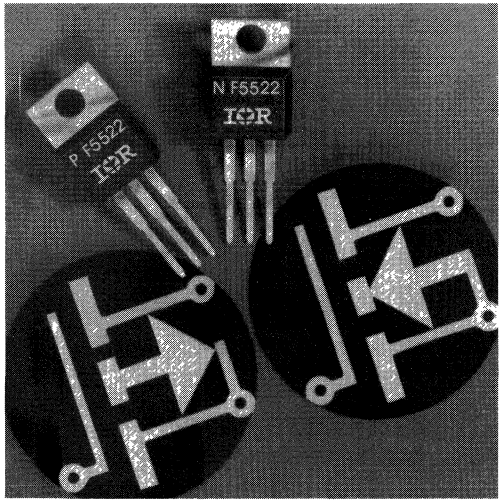
This complementary pair is particularly well suited for audio applications but can be also used in power supplies, motor controls, inverters, choppers, and high energy pulse circuits.

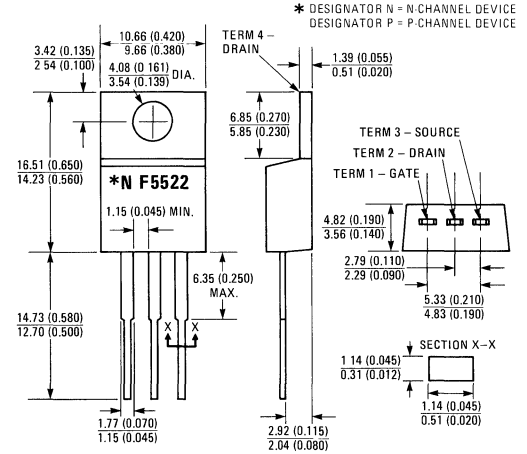
Features:

- Compact Plastic Package
- No Storage Time
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

Product Summary

Part Number	V_{DS}	I_{DM}	P_D
IRF5522	±100V	±12A	40W
IRF5523	±60V	±12A	40W





Case Style TO-220AB
Dimensions in Millimeters and (Inches)

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Absolute Maximum Ratings

Parameter		IRF5522		IRF5523		Units
		N-CHANNEL	P-CHANNEL	N-CHANNEL	P-CHANNEL	
V_{DS}	Drain – Source Voltage	100	-100	60	-60	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 1 MΩ)	100	-100	60	-60	V
I_D @ T_C = 100°C	Continuous Drain Current	4.0	-3.5	4.0	-3.5	A
I_D @ T_C = 25°C	Continuous Drain Current	7.0	-5.0	7.0	-5.0	A
I_{DM}	Pulsed Drain Current	12	-12	12	-12	A
V_{GS}	Gate – Source Voltage	±20				V
P_D	Max. Power Dissipation	40				W
	Linear Derating Factor	0.32				W/K
T_J T_{stg}	Operating and Storage Temperature Range	-55 to 150				°C

Electrical Characteristics @ T_C = 25°C(Unless Otherwise Specified)

Parameter		Device Type		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	IRF5522	N-CHANNEL	100	–	–	V	V_{GS} = 0V I_D = 250 μA (N-CHANNEL) I_D = -250 μA (P-CHANNEL)
			P-CHANNEL	-100	–	–		
		IRF5523	N-CHANNEL	-60	–	–		
			P-CHANNEL	-60	–	–		
$V_{GS(th)}$	Gate Threshold Voltage	ALL	N-CHANNEL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = ±250 μA
			P-CHANNEL	-2.0	–	-4.0		
I_{GSS}	Gate – Source Leakage	ALL	N-CHANNEL	–	–	500	nA	V_{GS} = 20V
			P-CHANNEL	–	–	-500		V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	N-CHANNEL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
				–	–	1000		V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_J = 125°C
			P-CHANNEL	–	–	-250		V_{DS} = Max. Rating, V_{GS} = 0V
				–	–	-1000		V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_J = 125°C
$R_{DS(on)}$	Static Drain-Source On-State Resistance	ALL	N-CHANNEL	–	0.3	0.4	Ω	V_{GS} = 10V, I_D = 3A
			P-CHANNEL	–	0.6	0.8		V_{GS} = -10V, I_D = -2A
g_{fs}	Forward Transconductance	ALL	N-CHANNEL	1.5	2.5	–	S (℧)	V_{DS} = 25V, I_D = 3A
			P-CHANNEL	0.9	1.8	–		V_{DS} = -25V, I_D = -2A
C_{iss}	Input Capacitance	ALL	N-CHANNEL	–	450	600	pF	V_{GS} = 0V, f = 1 MHz V_{DS} = 25V (N-CHANNEL) V_{DS} = -25V (P-CHANNEL) See Figs. 11 and 12
			P-CHANNEL	–	300	450		
C_{oss}	Output Capacitance	ALL	ALL	–	200	400		
C_{rss}	Reverse Transfer Capacitance	ALL	ALL	–	50	100		

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	ALL	–	–	3.12	K/W	
R_{thCS}	Case-to-Sink	ALL	ALL	–	1.0	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	ALL	–	–	80	K/W	Free Air Operation

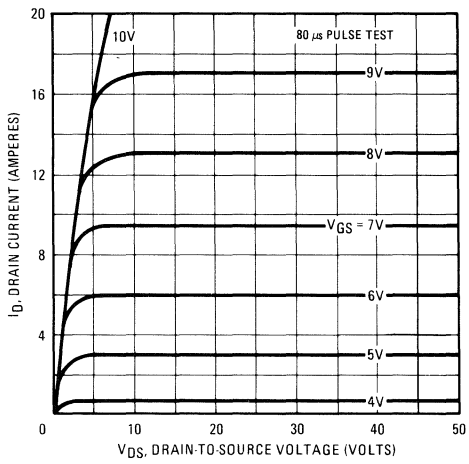


Fig. 1 – Typical Output Characteristics (N-Channel Device)

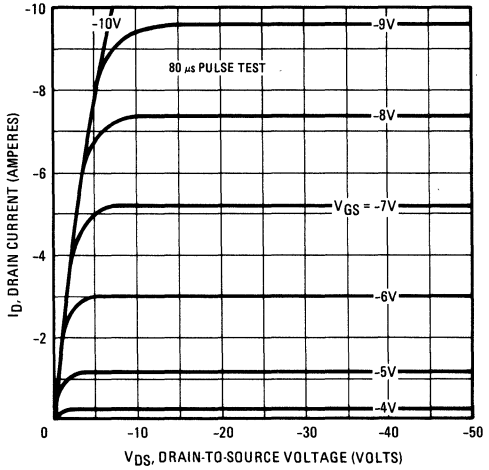


Fig. 2 – Typical Output Characteristics (P-Channel Device)

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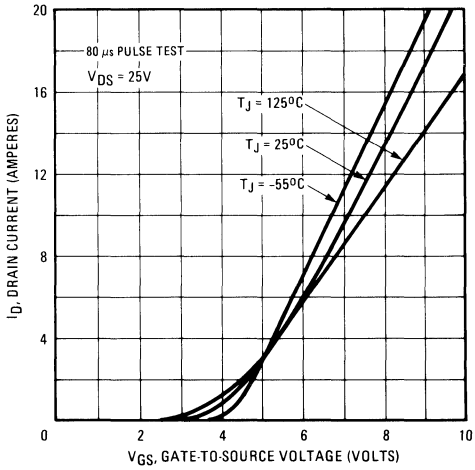


Fig. 3 — Typical Transfer Characteristics (N-Channel Device)

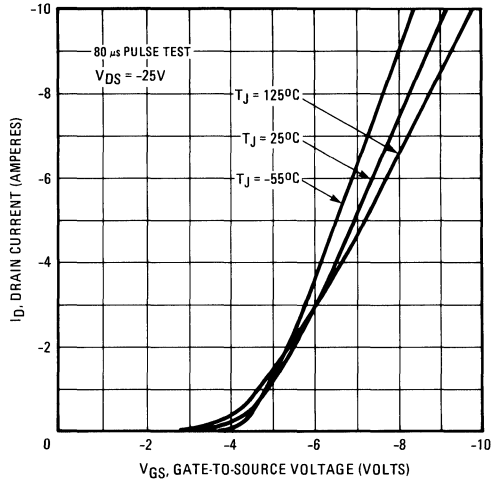


Fig. 4 — Typical Transfer Characteristics (P-Channel Device)

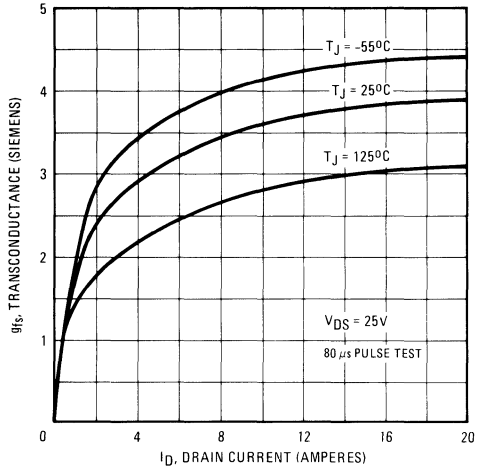


Fig. 5 — Typical Transconductance Vs. Drain Current (N-Channel Device)

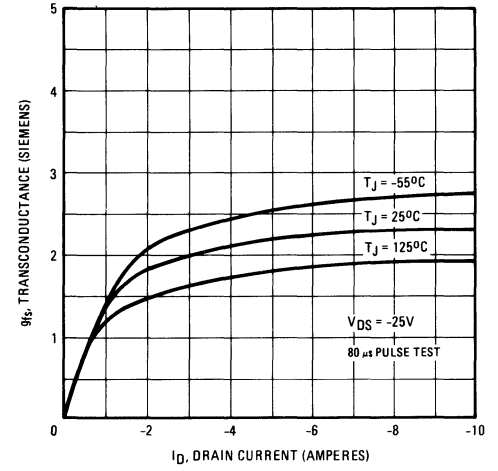


Fig. 6 — Typical Transconductance Vs. Drain Current (P-Channel Device)

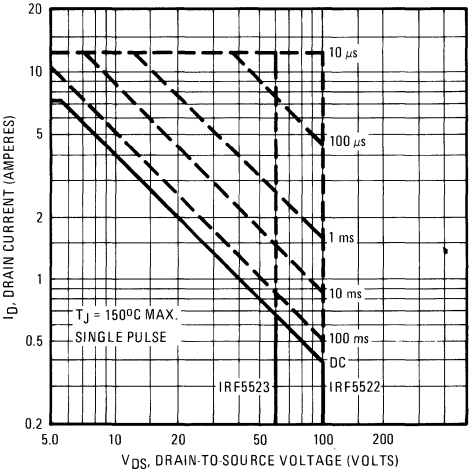


Fig. 7 — Maximum Safe Operating Area (N-Channel Device)

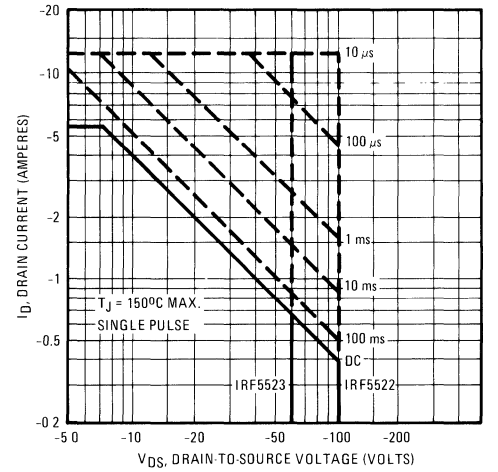


Fig. 8 — Maximum Safe Operating Area (P-Channel Device)

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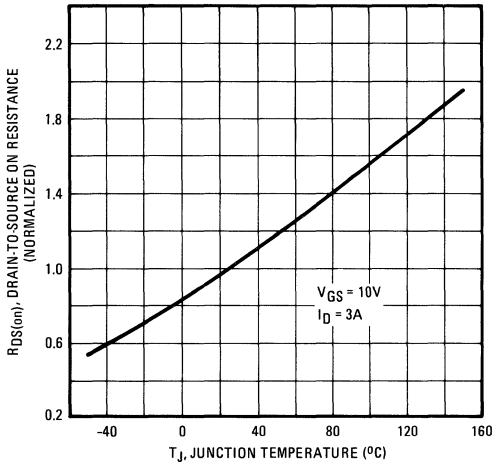


Fig. 9 — Normalized On-Resistance Vs. Temperature (N-Channel Device)

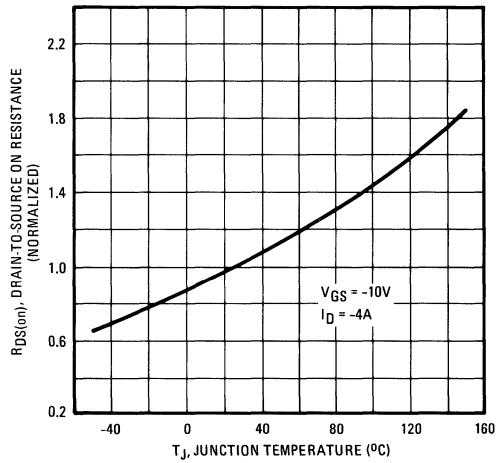


Fig. 10 — Normalized On-Resistance Vs. Temperature (P-Channel Device)

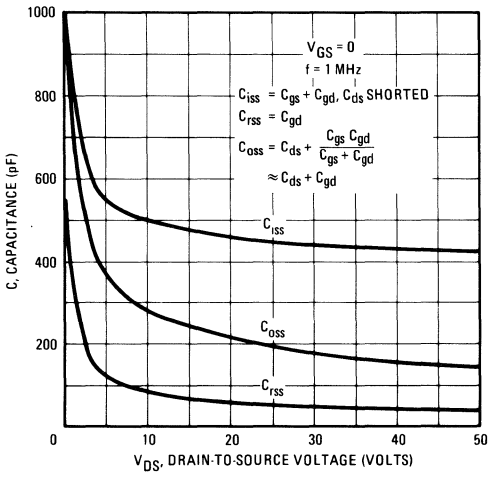


Fig. 11 — Typical Capacitance Vs. Drain-to-Source Voltage (N-Channel Device)

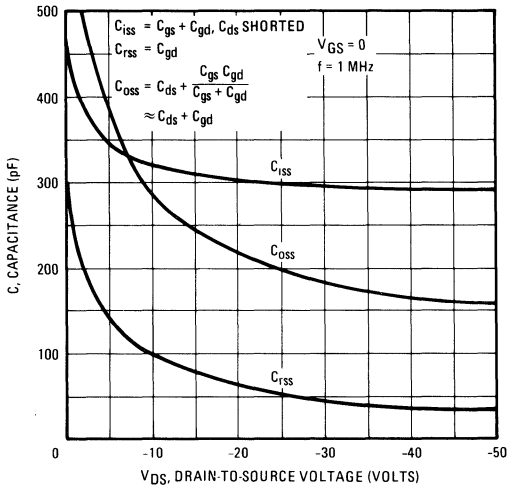


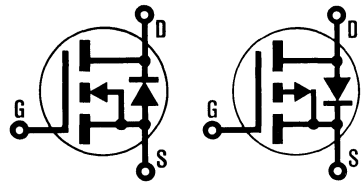
Fig. 12 — Typical Capacitance Vs. Drain-to-Source Voltage (P-Channel Device)

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HEXFET® TRANSISTORS IRF5532 IRF5533

MOSFET COMPLEMENTARY PAIRS



N-Channel P-Channel

100 Volt Complementary HEXFETs TO-220AB Plastic Package

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

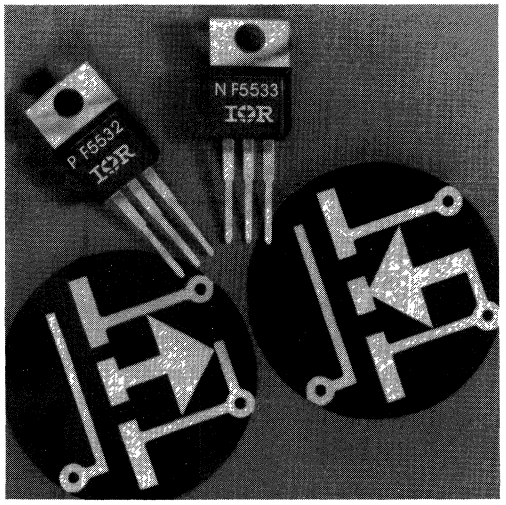
This complementary pair is particularly well suited for audio applications but can be also used in power supplies, motor controls, inverters, choppers, and high energy pulse circuits.

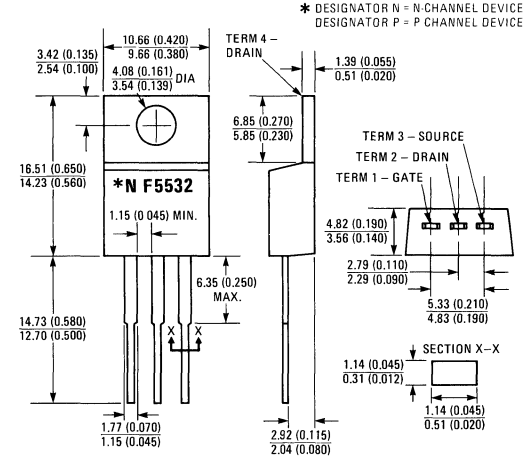
Features:

- Compact Plastic Package
- No Storage Time
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

Product Summary

Part Number	V_{DS}	I_{DM}	P_D
IRF5532	±100V	±25A	75W
IRF5533	±60V	±25A	75W





Case Style TO-220AB
Dimensions in Millimeters and (Inches)

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Absolute Maximum Ratings

Parameter		IRF5532		IRF5533		Units
		N-CHANNEL	P-CHANNEL	N-CHANNEL	P-CHANNEL	
V_{DS}	Drain – Source Voltage	100	-100	60	-60	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 1 MΩ)	100	-100	60	-60	V
I_D @ T_C = 100°C	Continuous Drain Current	8.0	-6.5	8.0	-6.5	A
I_D @ T_C = 25°C	Continuous Drain Current	12	-10	12	-10	A
I_{DM}	Pulsed Drain Current	25	-25	25	-25	A
V_{GS}	Gate – Source Voltage	±20				V
P_D	Max. Power Dissipation	75				W
	Linear Derating Factor	0.6				W/K
T_J T_{stg}	Operating and Storage Temperature Range	-55 to 150				°C

Electrical Characteristics @ T_C = 25°C(Unless Otherwise Specified)

Parameter		Device Type		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	IRF5532	N-CHANNEL	100	–	–	V	V_{GS} = 0V I_D = 250 μA (N-CHANNEL) I_D = -250 μA (P-CHANNEL)
			P-CHANNEL	-100	–	–		
		IRF5533	N-CHANNEL	60	–	–		
			P-CHANNEL	-60	–	–		
$V_{GS(th)}$	Gate Threshold Voltage	ALL	N-CHANNEL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250 μA
			P-CHANNEL	-2.0	–	-4.0		V_{DS} = V_{GS}, I_D = -250 μA
I_{GSS}	Gate – Source Leakage	ALL	N-CHANNEL	–	–	500	nA	V_{GS} = 20V
			P-CHANNEL	–	–	-500		V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	N-CHANNEL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
				–	–	1000		V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_J = 125°C
			P-CHANNEL	–	–	-250		V_{DS} = Max. Rating, V_{GS} = 0V
				–	–	-1000		V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_J = 125°C
$R_{DS(on)}$	Static Drain-Source On-State Resistance	ALL	N-CHANNEL	–	0.20	0.25	Ω	V_{GS} = 10V, I_D = 6A
			P-CHANNEL	–	0.30	0.40		V_{GS} = -10V, I_D = -4A
g_{fs}	Forward Transconductance	ALL	N-CHANNEL	4.0	5.5	12	S (℧)	V_{DS} = 15V, I_D = 9A
			P-CHANNEL	3.0	4.5	9		V_{DS} = -15V, I_D = -6A
C_{iss}	Input Capacitance	ALL	N-CHANNEL	350	600	800	pF	V_{GS} = 0V, f = 1.0 MHz V_{DS} = 25V (N-CHANNEL) V_{DS} = -25V (P-CHANNEL) See Figs. 11 and 12
			P-CHANNEL	–	500	700		
C_{oss}	Output Capacitance	ALL	ALL	150	300	500		
C_{rss}	Reverse Transfer Capacitance	ALL	ALL	50	100	200		

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	ALL	–	–	1.67	K/W	
R_{thCS}	Case-to-Sink	ALL	ALL	–	1.0	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	ALL	–	–	80	K/W	Free Air Operation

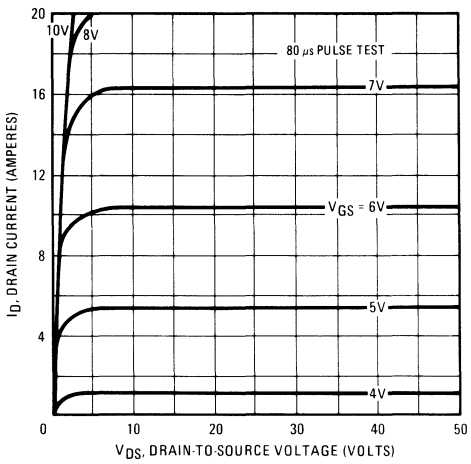


Fig. 1 – Typical Output Characteristics (N-Channel Device)

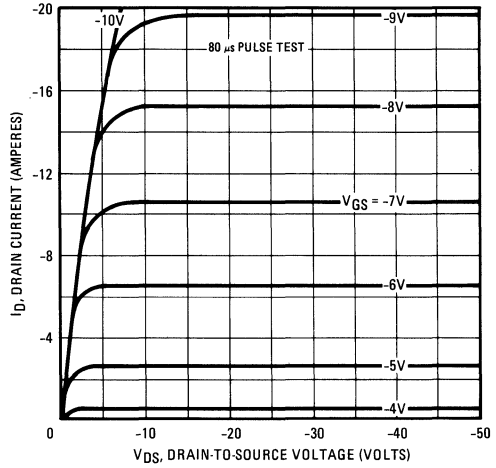


Fig. 2 – Typical Output Characteristics (P-Channel Device)

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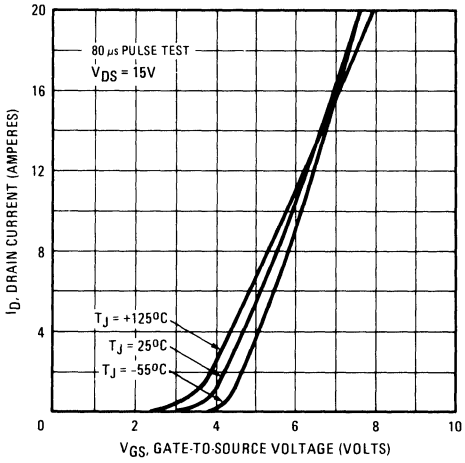


Fig. 3 — Typical Transfer Characteristics (N-Channel Device)

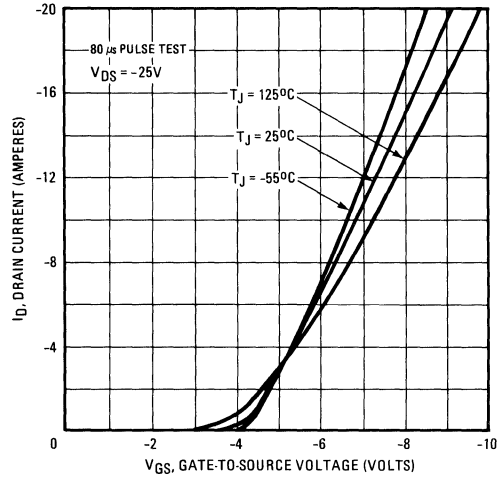


Fig. 4 — Typical Transfer Characteristics (P-Channel Device)

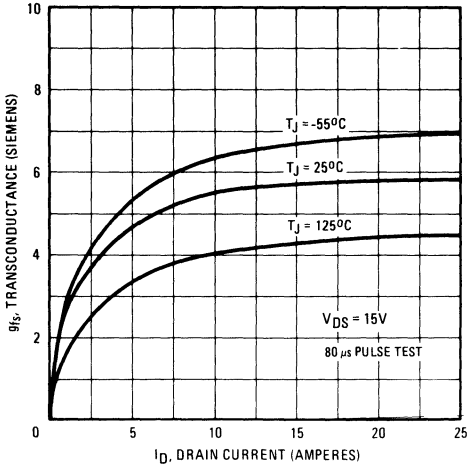


Fig. 5 — Typical Transconductance Vs. Drain Current (N-Channel Device)

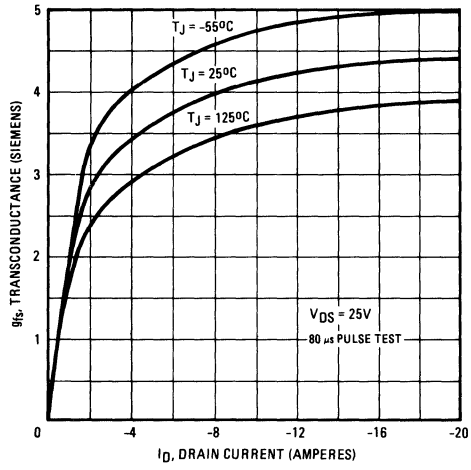


Fig. 6 — Typical Transconductance Vs. Drain Current (P-Channel Device)

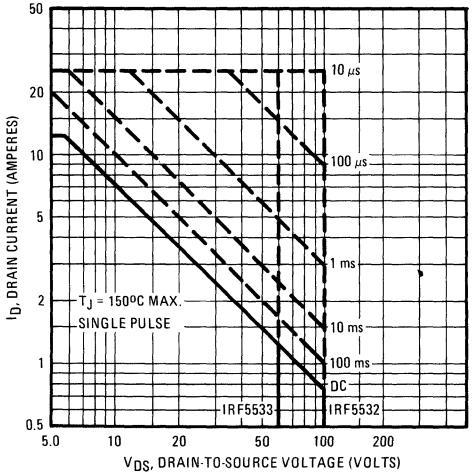


Fig. 7 — Maximum Safe Operating Area (N-Channel Device)

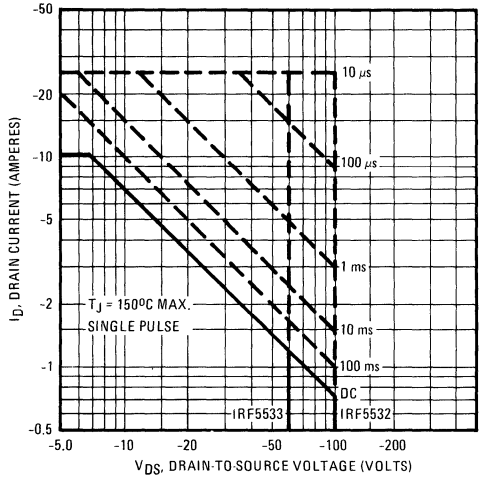


Fig. 8 — Maximum Safe Operating Area (P-Channel Device)

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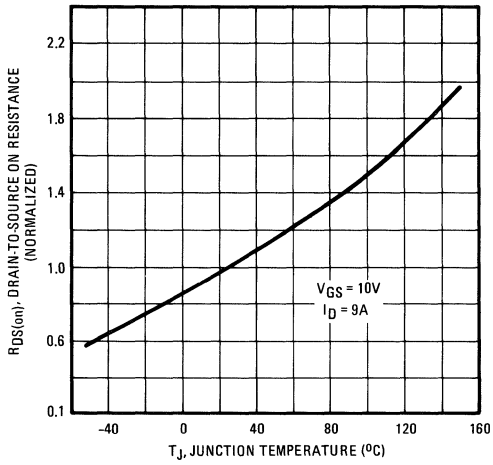


Fig. 9 — Normalized On-Resistance Vs. Temperature (N-Channel Device)

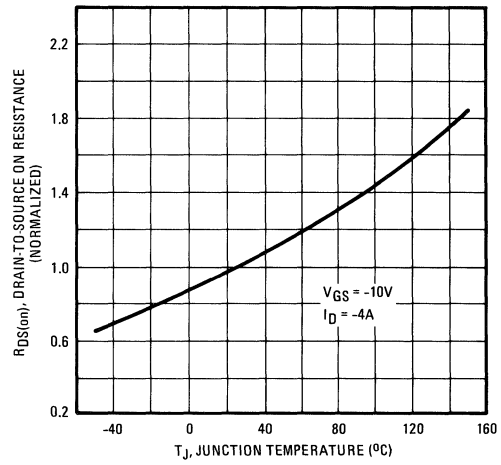


Fig. 10 — Normalized On-Resistance Vs. Temperature (P-Channel Device)

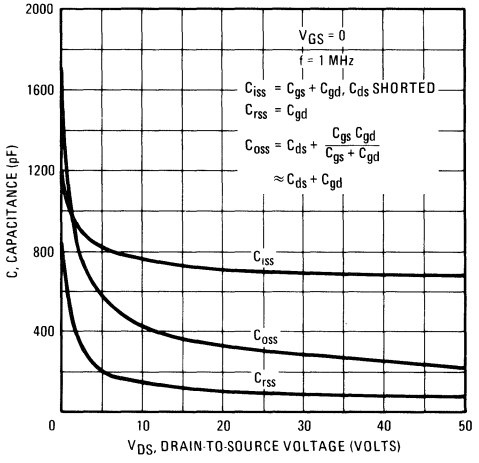


Fig. 11 — Typical Capacitance Vs. Drain-to-Source Voltage (N-Channel Device)

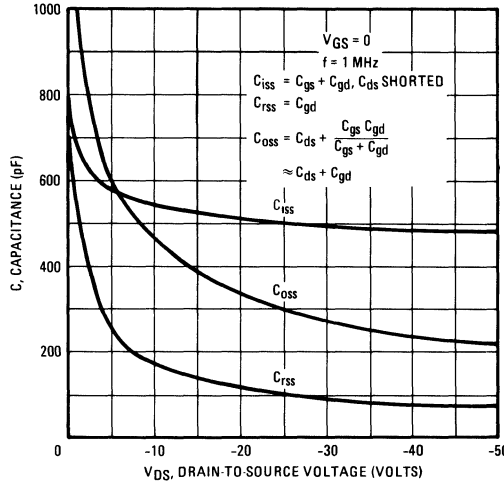
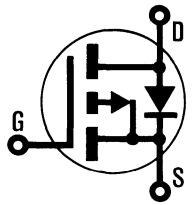


Fig. 12 — Typical Capacitance Vs. Drain-to-Source Voltage (P-Channel Device)

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HEXFET® TRANSISTORS IRF9130 IRF9131 IRF9132 IRF9133



P-Channel

-100 Volt, 0.3 Ohm HEXFET

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The P-Channel HEXFETs are designed for applications which require the convenience of reverse polarity operation. They retain all of the features of the more common N-Channel HEXFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and excellent temperature stability. The P-Channel IRF9130 device is an approximate electrical complement to the N-Channel IRF120 HEXFET.

P-Channel HEXFETs are intended for use in power stages where complementary symmetry with N-Channel devices offers circuit simplification. They are also very useful in drive stages because of the circuit versatility offered by the reverse polarity connection. Applications include motor control, audio amplifiers, switched mode converters, control circuits and pulse amplifiers.

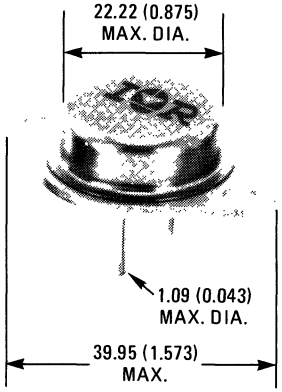
Features:

- P-Channel Versatility
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

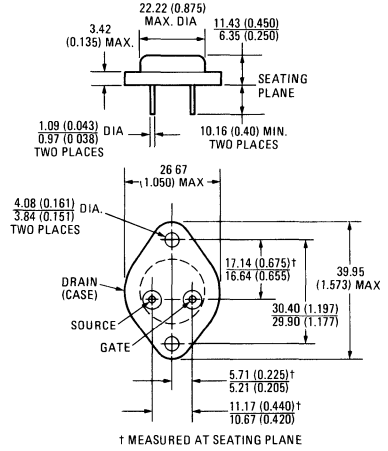
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF9130	-100V	0.30Ω	-12A
IRF9131	-60V	0.30Ω	-12A
IRF9132	-100V	0.40Ω	-10A
IRF9133	-60V	0.40Ω	-10A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Conforms to JEDEC Outline TO-204AA (TO-3)
Dimensions in Millimeters and (Inches)

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IRF9130, IRF9131, IRF9132, IRF9133 Devices

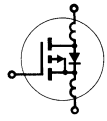
Absolute Maximum Ratings

Parameter		IRF9130	IRF9131	IRF9132	IRF9133	Units
V_{DS}	Drain - Source Voltage ①	-100	-60	-100	-60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	-100	-60	-100	-60	V
I_D @ T_C = 25°C	Continuous Drain Current	-12	-12	-10	-10	A
I_D @ T_C = 100°C	Continuous Drain Current	-7.5	-7.5	-6.5	-6.5	A
I_{DM}	Pulsed Drain Current ③	-48	-48	-40	-40	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH -48	-48	-40	-40	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF9130 IRF9132	-100	–	–	V	V_{GS} = 0V
		IRF9131 IRF9133	-60	–	–	V	I_D = -250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	-2.0	–	-4.0	V	V_{DS} = V_{GS}, I_D = -250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	-100	nA	V_{GS} = -20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	100	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	-250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	-1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF9130 IRF9131	-12	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = -10V
		IRF9132 IRF9133	-10	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF9130 IRF9131	–	0.25	0.30	Ω	V_{GS} = -10V, I_D = -6.5A
		IRF9132 IRF9133	–	0.30	0.40	Ω	
g_{fs}	Forward Transconductance ②	ALL	2.0	3.7	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = -6.5A
C_{iss}	Input Capacitance	ALL	–	500	700	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	300	450	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	100	200	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	30	60	ns	$V_{DD} \approx 0.5\ BV_{DSS}$, I_D = -6.5A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	70	140	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	70	140	ns	
t_f	Fall Time	ALL	–	70	140	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	25	45	nC	V_{GS} = -15V, I_D = -15A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	13	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	12	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF9130 IRF9131	—	—	-12	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF9132 IRF9133	—	—	-10	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF9130 IRF9131	—	—	-48	A	
		IRF9132 IRF9133	—	—	-40	A	
V_{SD}	Diode Forward Voltage ②	IRF9130 IRF9131	—	—	-6.3	V	T_C = 25°C, I_S = -12A, V_{GS} = 0V
		IRF9132 IRF9133	—	—	-6.0	V	T_C = 25°C, I_S = -10A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	300	—	ns	T_J = 150°C, I_F = -12A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	1.8	—	μC	T_J = 150°C, I_F = -12A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

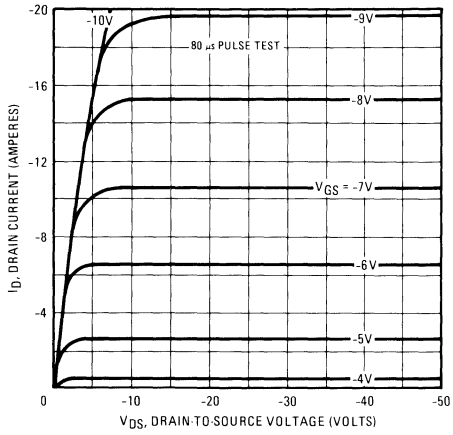


Fig. 1 — Typical Output Characteristics

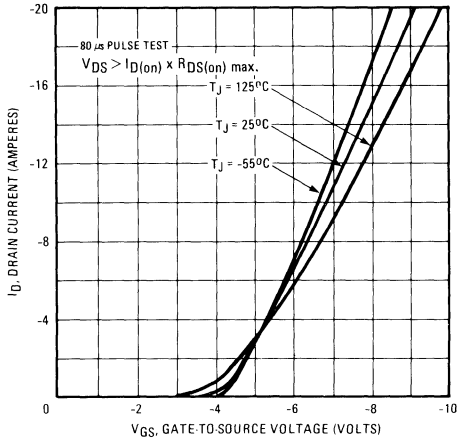


Fig. 2 — Typical Transfer Characteristics

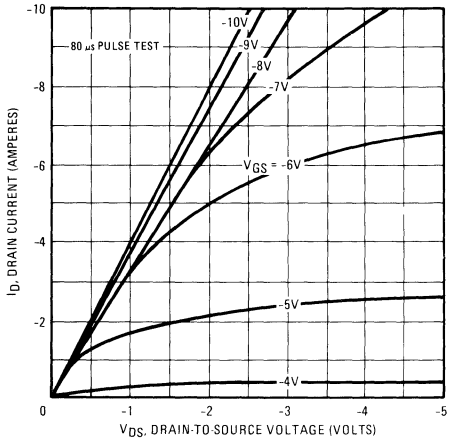


Fig. 3 — Typical Saturation Characteristics

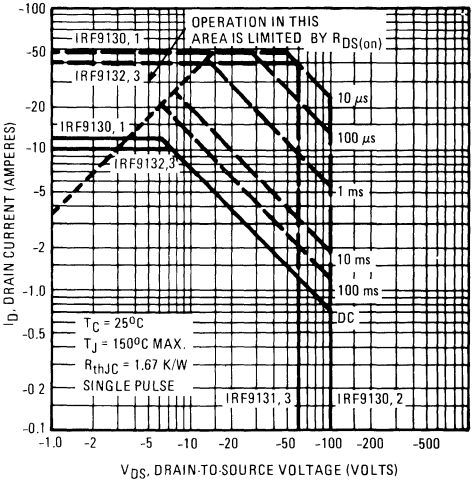


Fig. 4 — Maximum Safe Operating Area

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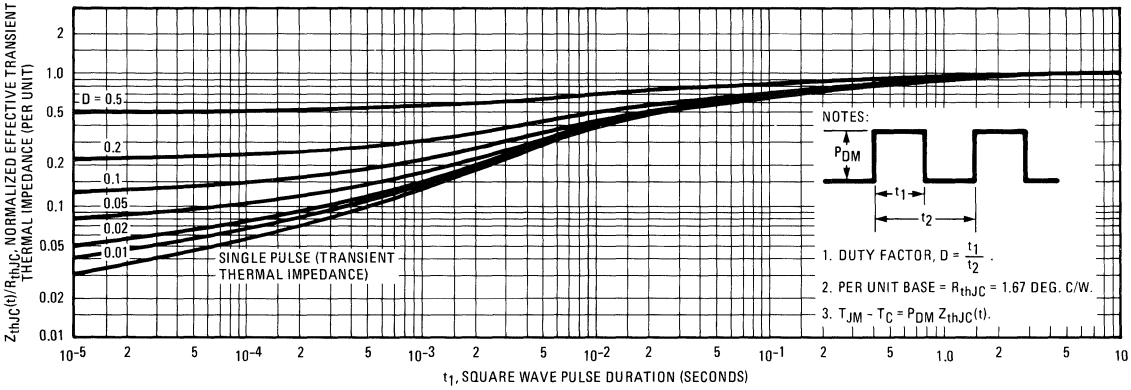


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

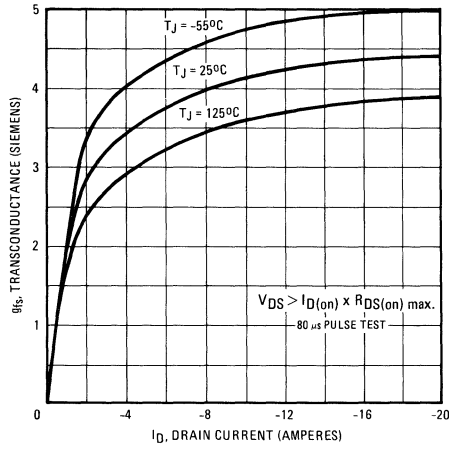


Fig. 6 — Typical Transconductance Vs. Drain Current

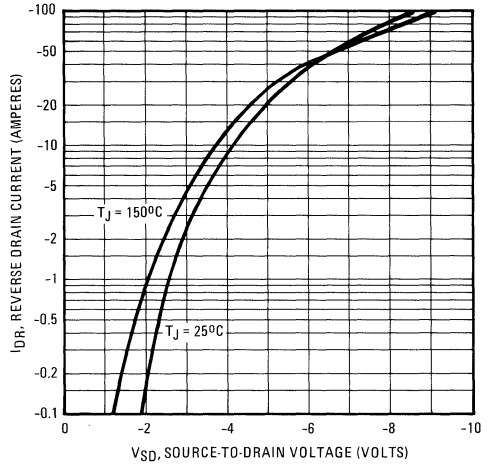


Fig. 7 — Typical Source-Drain Diode Forward Voltage

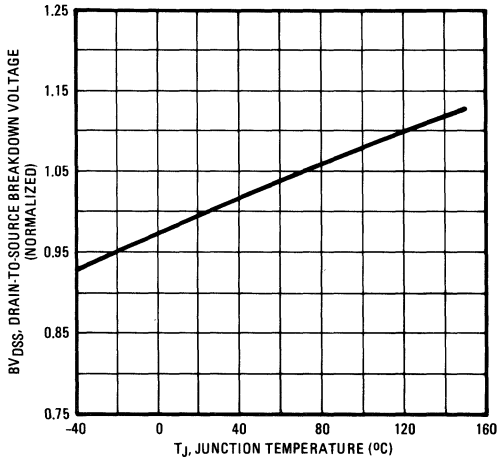


Fig. 8 — Breakdown Voltage Vs. Temperature

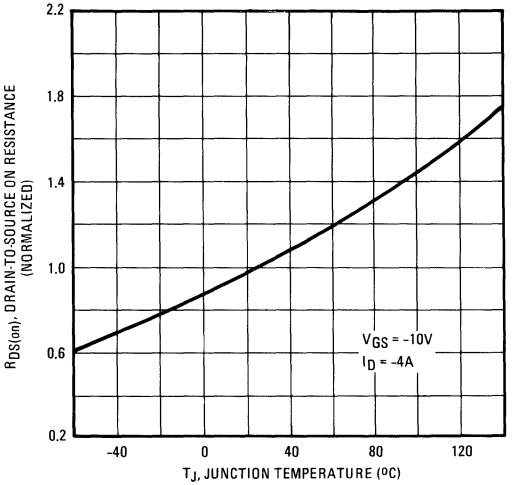


Fig. 9 — Normalized On-Resistance Vs. Temperature

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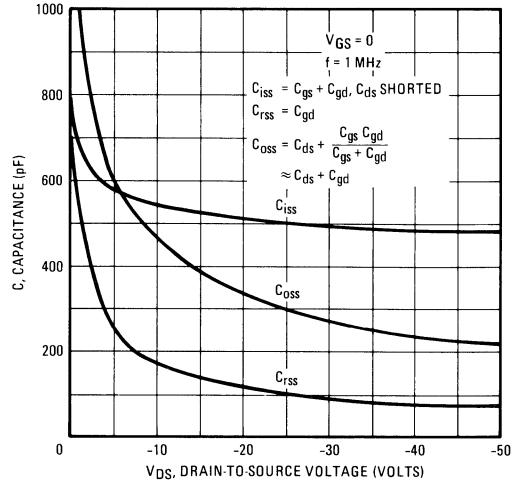


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

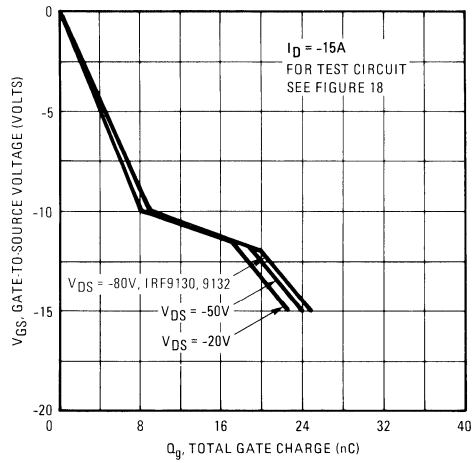


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

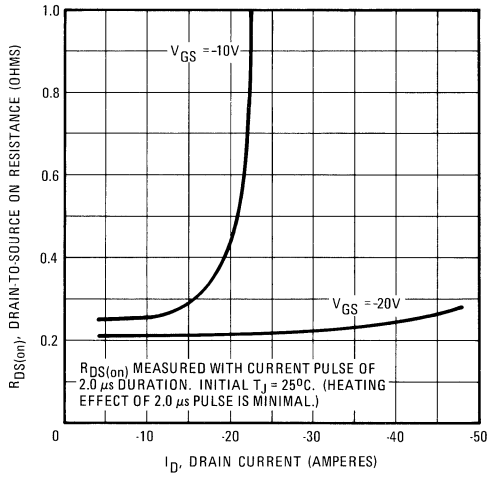


Fig. 12 — Typical On-Resistance Vs. Drain Current

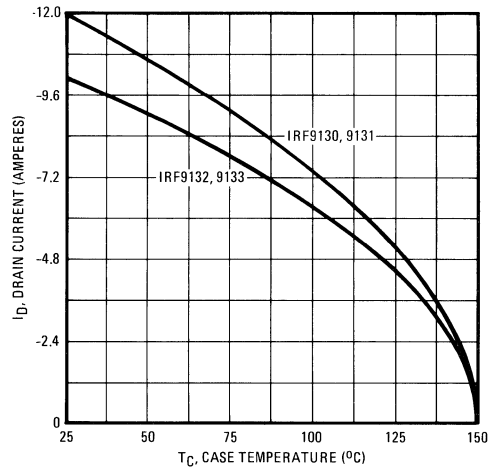


Fig. 13 — Maximum Drain Current Vs. Case Temperature

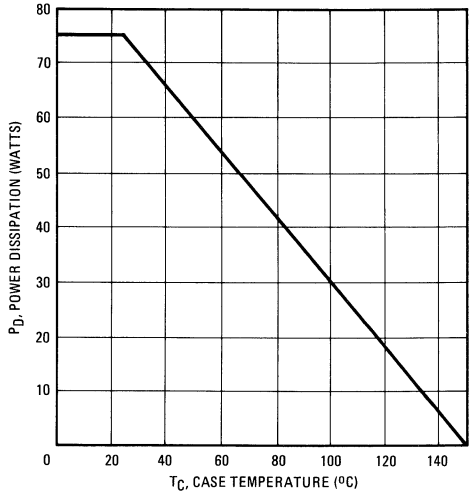


Fig. 14 — Power Vs. Temperature Derating Curve

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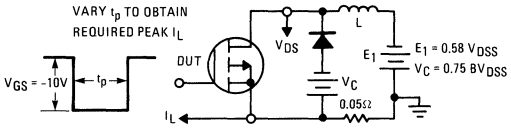


Fig. 15 — Clamped Inductive Test Circuit

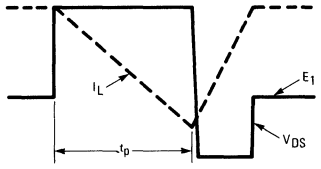
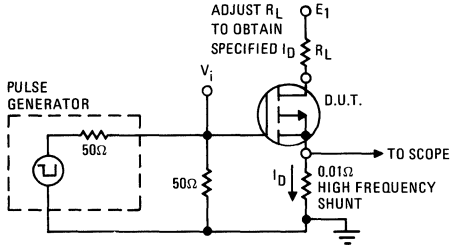


Fig. 16 — Clamped Inductive Waveforms



— Switching Time Test Circuit

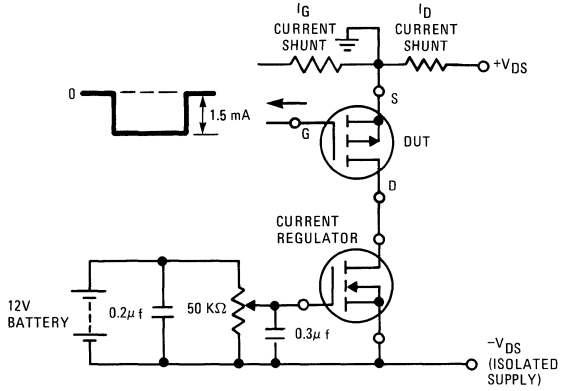


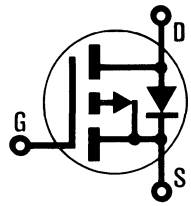
Fig. 18 — Gate Charge Test Circuit

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS IRF9230

P-CHANNEL 200 VOLT POWER MOSFETs



IRF9231
IRF9232
IRF9233

-200 Volt, 0.8 Ohm HEXFET

The HEXFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The P-Channel HEXFETs are designed for applications which require the convenience of reverse polarity operation. They retain all of the features of the more common N-Channel HEXFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and excellent temperature stability. The P-Channel IRF9230 device is an approximate electrical complement to the N-Channel IRF220 HEXFET.

P-Channel HEXFETs are intended for use in power stages where complementary symmetry with N-Channel devices offers circuit simplification. They are also very useful in drive stages because of the circuit versatility offered by the reverse polarity connection. Applications include motor control, audio amplifiers, switched mode converters, control circuits and pulse amplifiers.

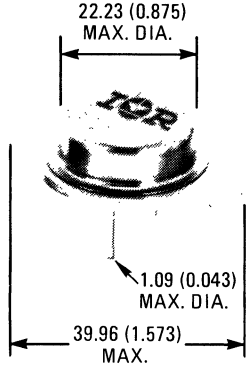
Features:

- P-Channel Versatility
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

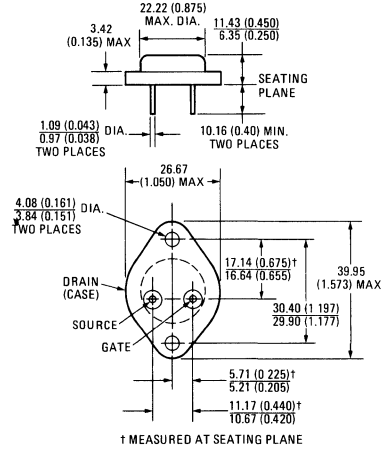
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF9230	-200V	0.8Ω	-6.5A
IRF9231	-150V	0.8Ω	-6.5A
IRF9232	-200V	1.2Ω	-5.5A
IRF9233	-150V	1.2Ω	-5.5A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



† MEASURED AT SEATING PLANE

Conforms to JEDEC Outline TO-204AA (TO-3)
All Dimensions in Millimeters and (Inches)

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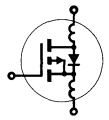
Absolute Maximum Ratings

Parameter		IRF9230	IRF9231	IRF9232	IRF9233	Units
V_{DS}	Drain - Source Voltage ①	-200	-150	-200	-150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	-200	-150	-200	-150	V
I_D @ T_C = 25°C	Continuous Drain Current	-6.5	-6.5	-5.5	-5.5	A
I_D @ T_C = 100°C	Continuous Drain Current	-4.0	-4.0	-3.5	-3.5	A
I_{DM}	Pulsed Drain Current ③	-26	-26	-22	-22	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		-26	-26	-22	-22	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF9230 IRF9232	-200	—	—	V	V_{GS} = 0V
		IRF9231 IRF9233	-150	—	—	V	I_D = -250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	-100	nA	V_{GS} = -20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	100	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	-250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	-1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF9230 IRF9231	-6.5	—	—	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = -10V
		IRF9232 IRF9233	-5.5	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF9230 IRF9231	—	0.5	0.8	Ω	V_{GS} = -10V, I_D = -3.5A
		IRF9232 IRF9233	—	0.8	1.2	Ω	
g_{fs}	Forward Transconductance ②	ALL	2.2	3.5	—	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = -3.5A
C_{iss}	Input Capacitance	ALL	—	550	650	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	170	300	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	50	90	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	30	50	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = -3.5A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	50	100	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	50	100	ns	
t_f	Fall Time	ALL	—	40	80	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	31	45	nC	V_{GS} = -15V, I_D = -8.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	18	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	13	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	1.67	K/W	
R_{thCS}	Case-to-Sink	ALL	—	0.1	—	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF9230 IRF9231	–	–	-6.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF9232 IRF9233	–	–	-5.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF9230 IRF9231	–	–	-26	A	
		IRF9232 IRF9233	–	–	-22	A	
V_{SD}	Diode Forward Voltage ②	IRF9230 IRF9231	–	–	-6.5	V	T_C = 25°C, I_S = -6.5A, V_{GS} = 0V
		IRF9232 IRF9233	–	–	-6.3	V	T_C = 25°C, I_S = -5.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	400	–	ns	T_J = 150°C, I_F = -6.5A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	2.6	–	μC	T_J = 150°C, I_F = -6.5A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

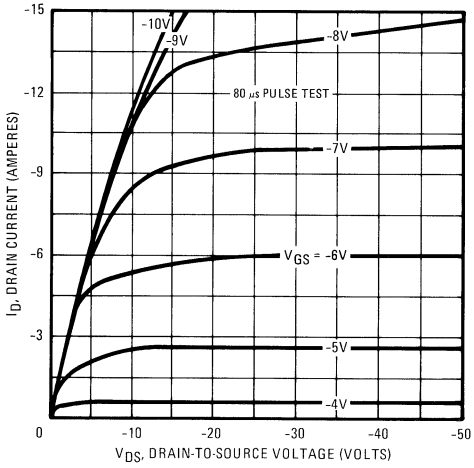


Fig. 1 — Typical Output Characteristics

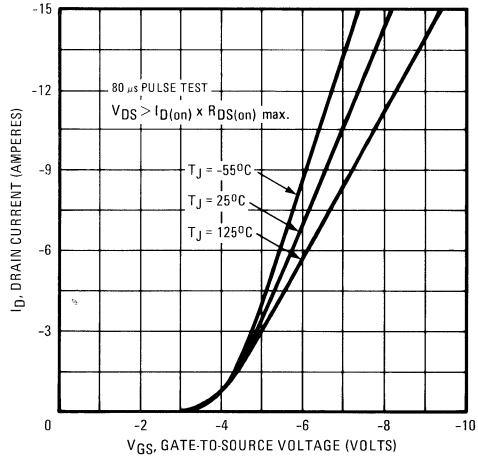


Fig. 2 — Typical Transfer Characteristics

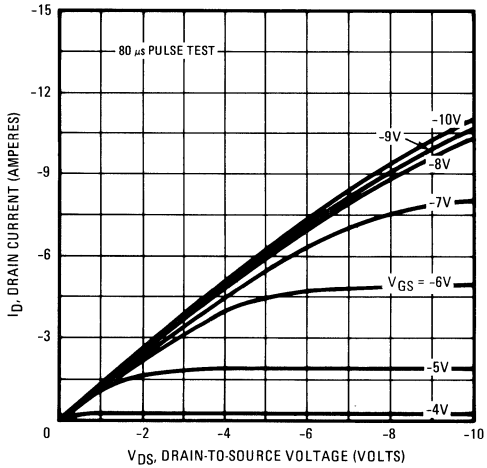


Fig. 3 — Typical Saturation Characteristics

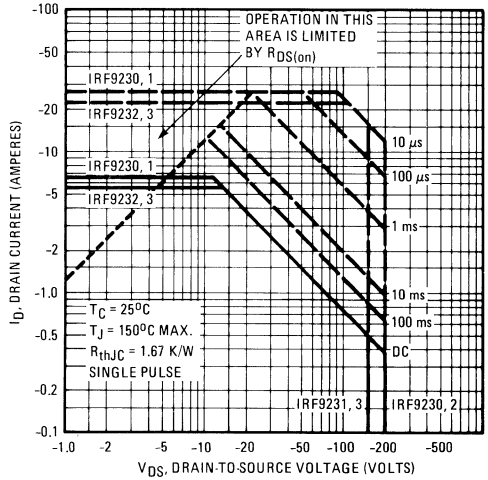


Fig. 4 — Maximum Safe Operating Area

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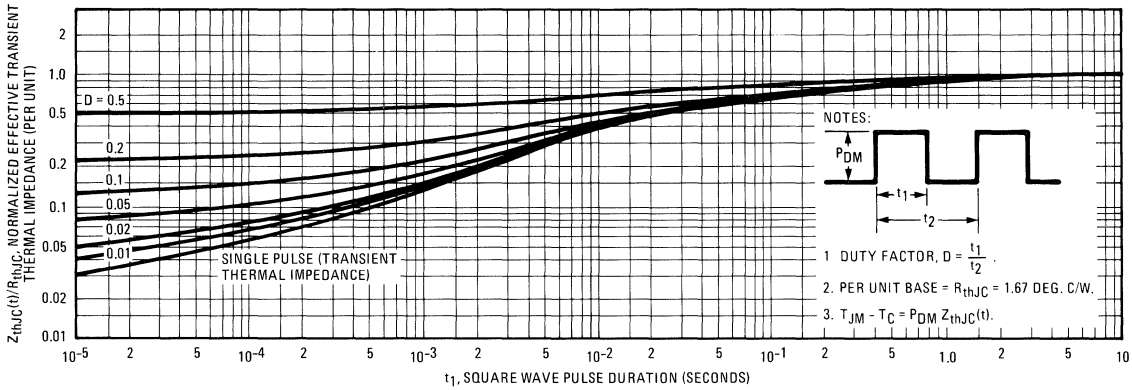


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

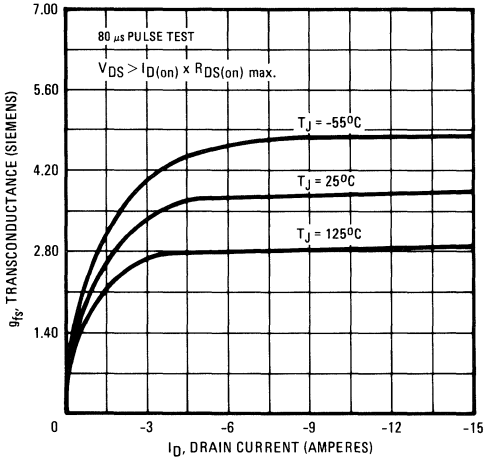


Fig. 6 — Typical Transconductance Vs. Drain Current

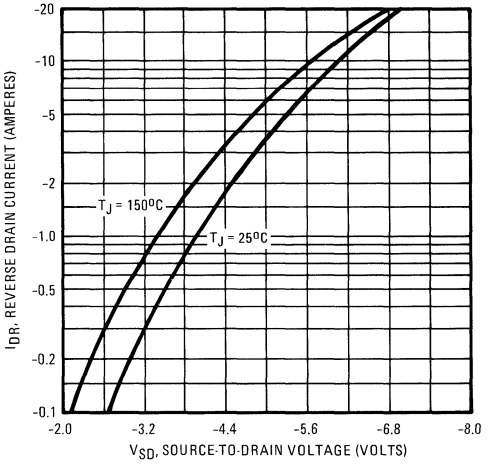


Fig. 7 — Typical Source-Drain Diode Forward Voltage

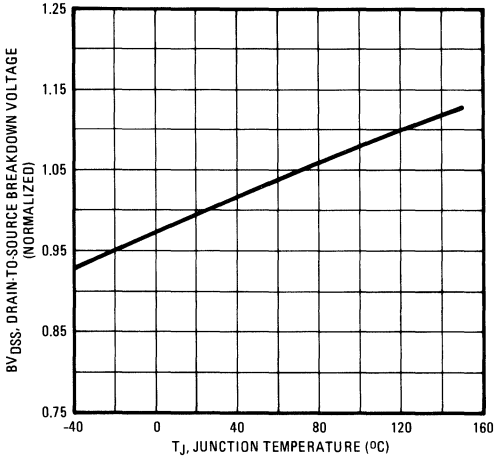


Fig. 8 — Breakdown Voltage Vs. Temperature

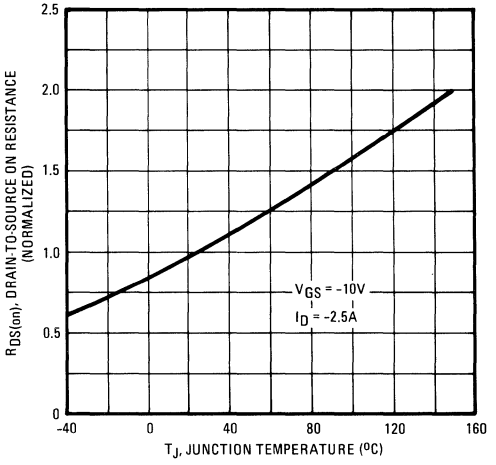


Fig. 9 — Normalized On-Resistance Vs. Temperature

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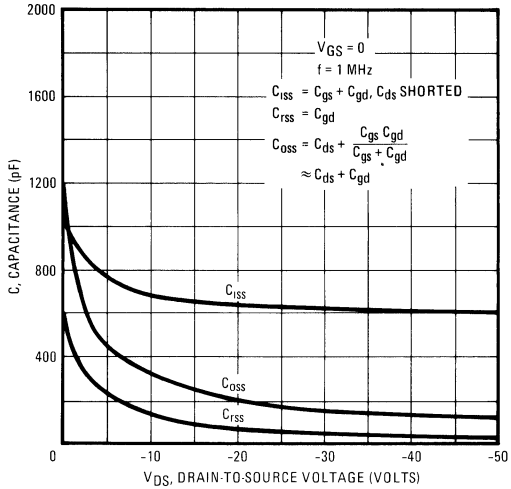


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

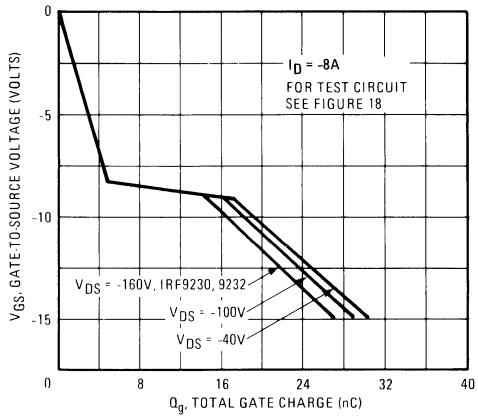


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

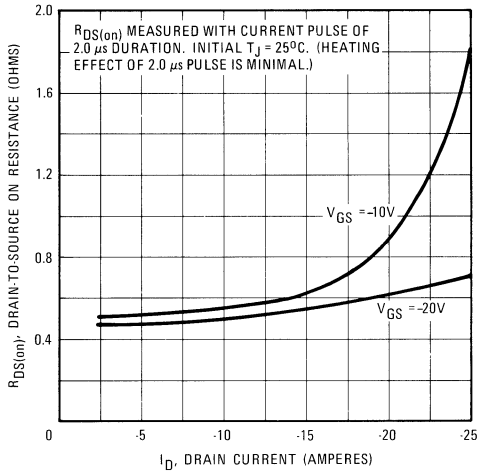


Fig. 12 — Typical On-Resistance Vs. Drain Current

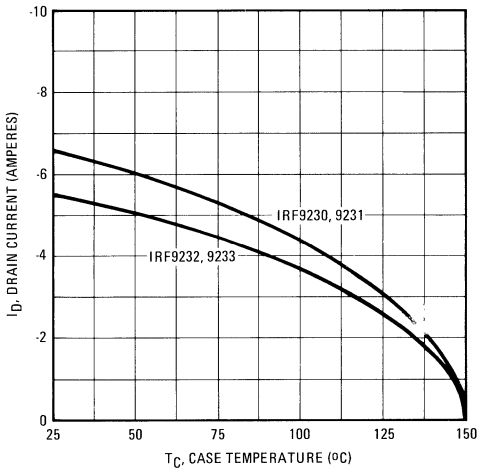


Fig. 13 — Maximum Drain Current Vs. Case Temperature

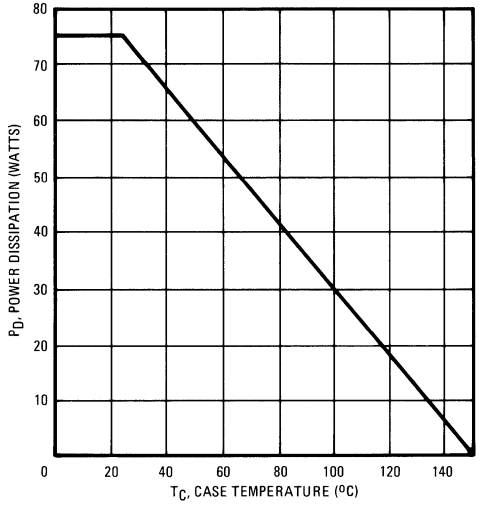


Fig. 14 — Power Vs. Temperature Derating Curve

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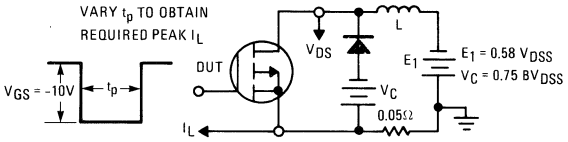


Fig. 15 — Clamped Inductive Test Circuit

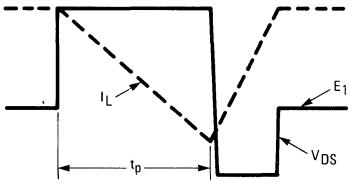


Fig. 16 — Clamped Inductive Waveforms

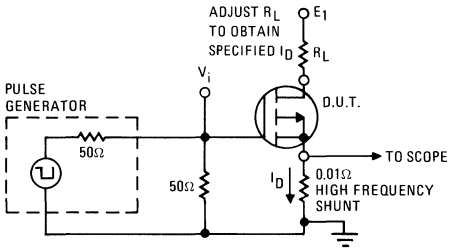


Fig. 17 — Switching Time Test Circuit

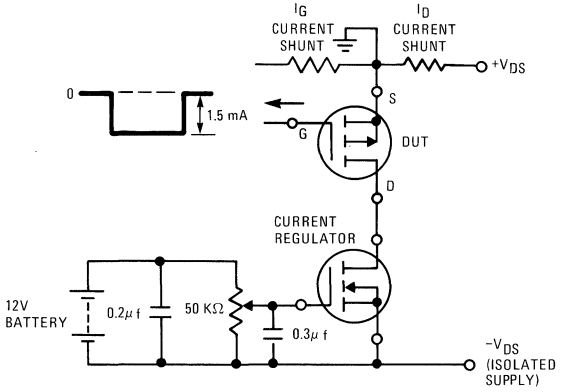
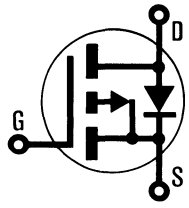


Fig. 18 — Gate Charge Test Circuit

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS IRF9520



P-Channel

IRF9521

IRF9522

IRF9523

-100 Volt, 0.6 Ohm HEXFET TO-220AB Plastic Package

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The P-Channel HEXFETs are designed for applications which require the convenience of reverse polarity operation. They retain all of the features of the more common N-Channel HEXFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and excellent temperature stability.

P-Channel HEXFETs are intended for use in power stages where complementary symmetry with N-Channel devices offers circuit simplification. They are also very useful in drive stages because of the circuit versatility offered by the reverse polarity connection. Applications include motor control, audio amplifiers, switched mode converters, control circuits and pulse amplifiers.

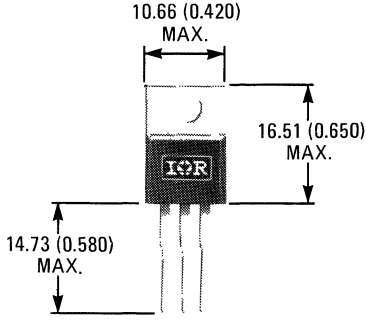
Features:

- P-Channel Versatility
- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

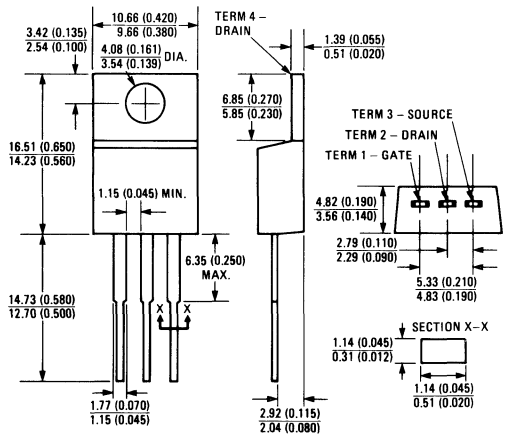
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF9520	-100V	0.60Ω	-6.0A
IRF9521	-60V	0.60Ω	-6.0A
IRF9522	-100V	0.80Ω	-5.0A
IRF9523	-60V	0.80Ω	-5.0A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Case Style TO-220AB
Dimensions in Millimeters and (Inches)

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IRF9520, IRF9521, IRF9522, IRF9523 Devices

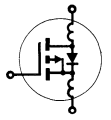
Absolute Maximum Ratings

Parameter		IRF9520	IRF9521	IRF9522	IRF9523	Units
V_{DS}	Drain - Source Voltage ①	-100	-60	-100	-60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	-100	-60	-100	-60	V
I_D @ T_C = 25°C	Continuous Drain Current	-6.0	-6.0	-5.0	-5.0	A
I_D @ T_C = 100°C	Continuous Drain Current	-4.0	-4.0	-3.5	-3.5	A
I_{DM}	Pulsed Drain Current ③	-24	-24	-20	-20	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		-24	-24	-20	-20	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF9520 IRF9522	-100	–	–	V	V_{GS} = 0V
		IRF9521 IRF9523	-60	–	–	V	I_D = -250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	-2.0	–	-4.0	V	V_{DS} = V_{GS}, I_D = -250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	-500	nA	V_{GS} = -20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	500	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	-250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	-1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF9520 IRF9521	-6.0	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = -10V
		IRF9522 IRF9523	-5.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF9520 IRF9521	–	0.5	0.6	Ω	V_{GS} = -10V, I_D = -3.5A
		IRF9522 IRF9523	–	0.6	0.8	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.9	2.0	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = -3.5A
C_{iss}	Input Capacitance	ALL	–	300	450	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	200	350	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	50	100	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	25	50	ns	$V_{DD} \approx 0.5\ BV_{DSS}$, I_D = -3.5A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	50	100	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	50	100	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	16	22	nC	V_{GS} = -15V, I_D = -8.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	9.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	7.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	3.12	K/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	K/W	Free Air Operation

Downloaded from Arrow.com.

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF9520 IRF9521	–	–	-6.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF9522 IRF9523	–	–	-5.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF9520 IRF9521	–	–	-24	A	
		IRF9522 IRF9523	–	–	-20	A	
V_{SD}	Diode Forward Voltage ②	IRF9520 IRF9521	–	–	-6.3	V	T_C = 25°C, I_S = -6.0A, V_{GS} = 0V
		IRF9522 IRF9523	–	–	-6.0	V	T_C = 25°C, I_S = -5.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	230	–	ns	T_J = 150°C, I_F = -6.0A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	1.3	–	μC	T_J = 150°C, I_F = -6.0A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

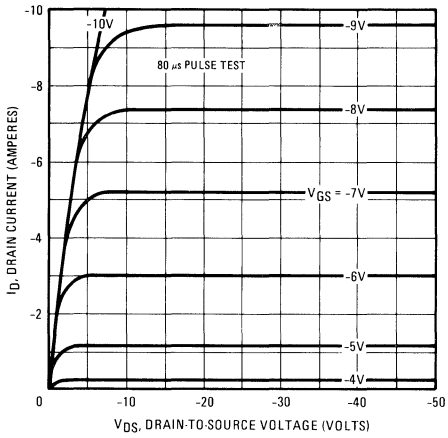


Fig. 1 — Typical Output Characteristics

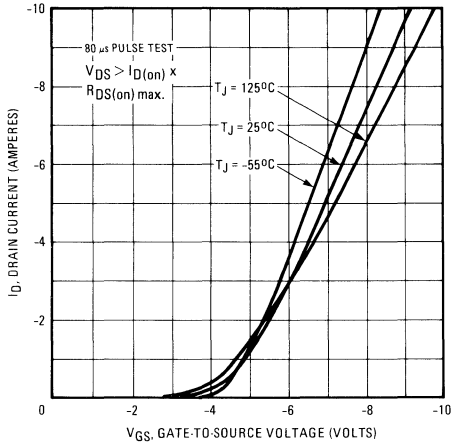


Fig. 2 — Typical Transfer Characteristics

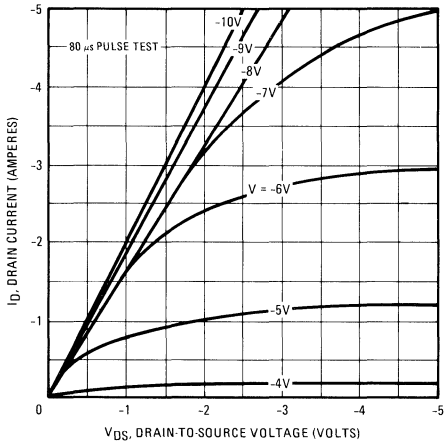


Fig. 3 — Typical Saturation Characteristics

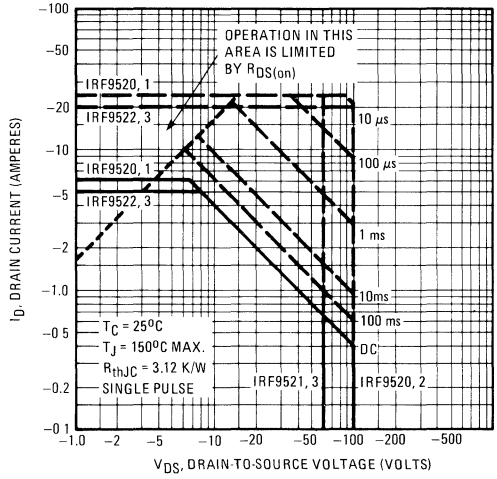


Fig. 4 — Maximum Safe Operating Area

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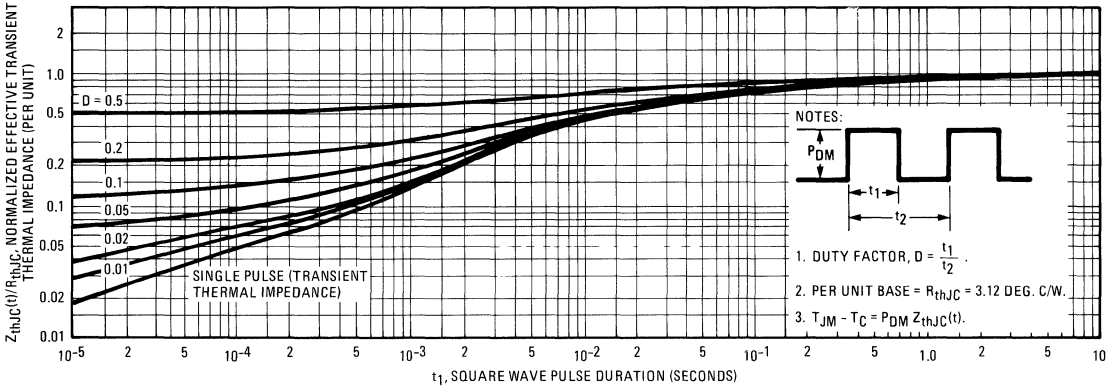


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

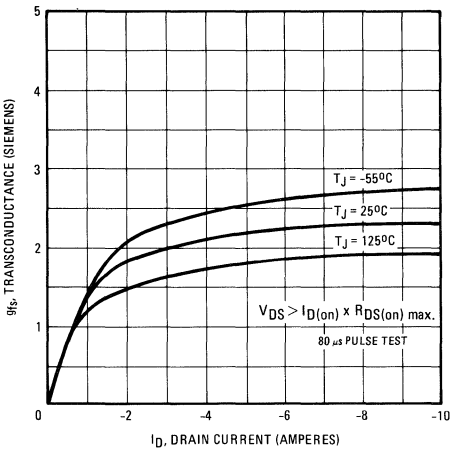


Fig. 6 — Typical Transconductance Vs. Drain Current

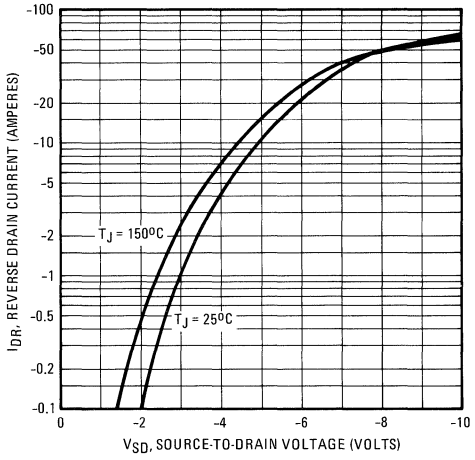


Fig. 7 — Typical Source-Drain Diode Forward Voltage

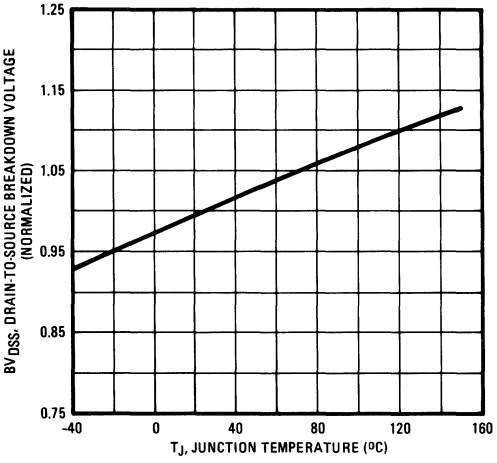


Fig. 8 — Breakdown Voltage Vs. Temperature

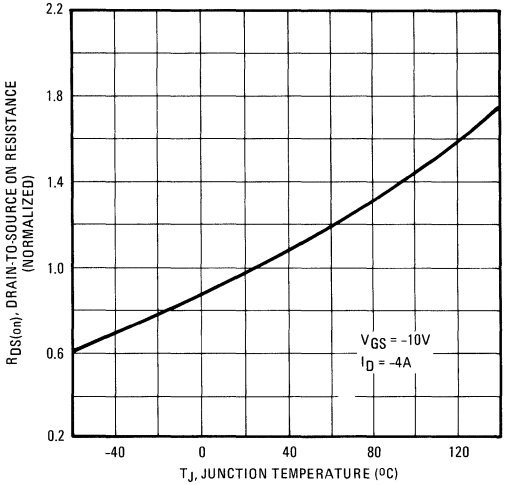


Fig. 9 — Normalized On-Resistance Vs. Temperature

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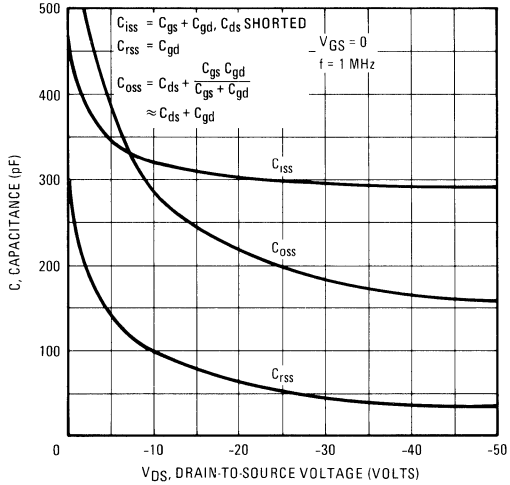


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

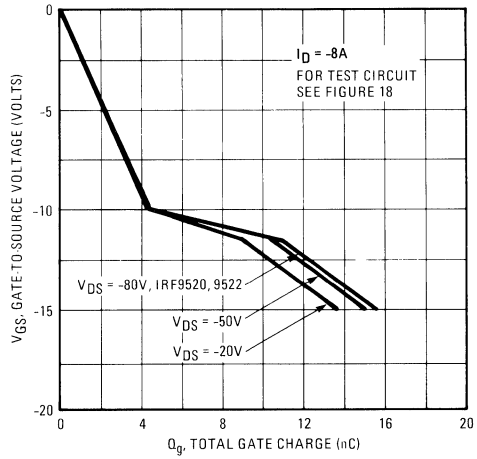


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

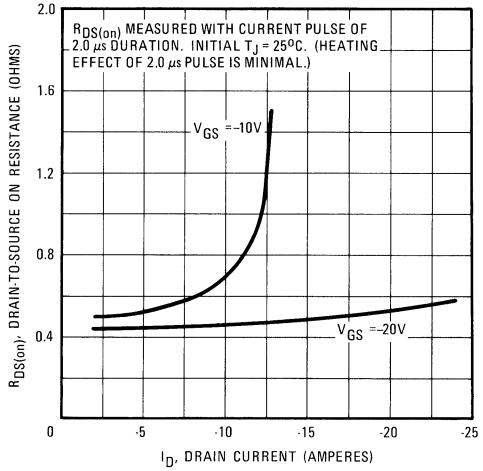


Fig. 12 — Typical On-Resistance Vs. Drain Current

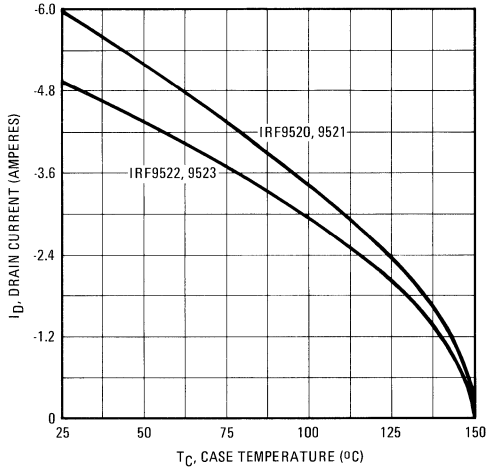


Fig. 13 — Maximum Drain Current Vs. Case Temperature

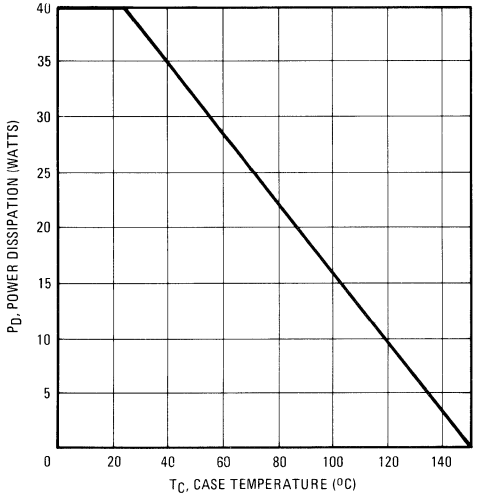


Fig. 14 — Power Vs. Temperature Derating Curve

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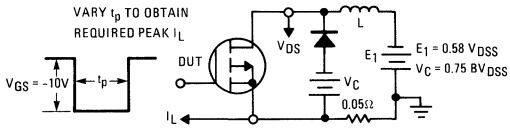


Fig. 15 — Clamped Inductive Test Circuit

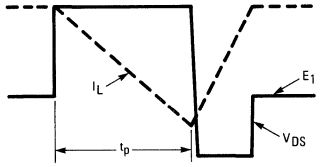


Fig. 16 — Clamped Inductive Waveforms

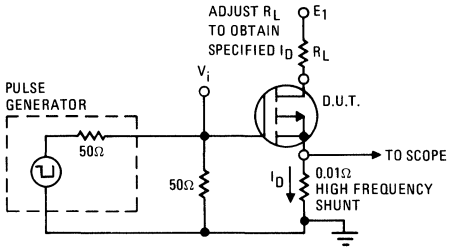


Fig. 17 — Switching Time Test Circuit

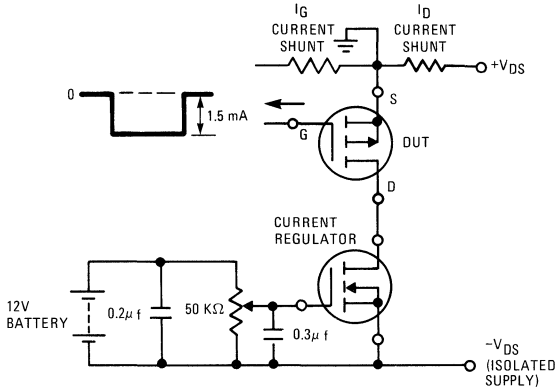


Fig. 18 — Gate Charge Test Circuit

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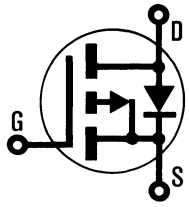
INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS IRF9530

IRF9531

IRF9532

IRF9533



P-Channel

-100 Volt, 0.3 Ohm HEXFET
TO-220AB Plastic Package

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The P-Channel HEXFETs are designed for applications which require the convenience of reverse polarity operation. They retain all of the features of the more common N-Channel HEXFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and excellent temperature stability. The P-Channel IRF9530 device is an approximate electrical complement to the N-Channel IRF520 HEXFET.

P-Channel HEXFETs are intended for use in power stages where complementary symmetry with N-Channel devices offers circuit simplification. They are also very useful in drive stages because of the circuit versatility offered by the reverse polarity connection. Applications include motor control, audio amplifiers, switched mode converters, control circuits and pulse amplifiers.

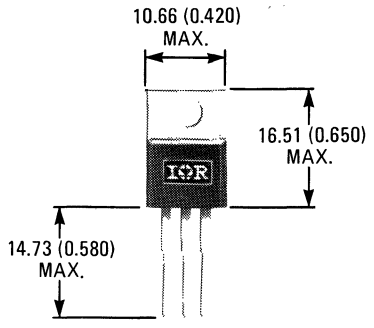
Features:

- P-Channel Versatility
- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

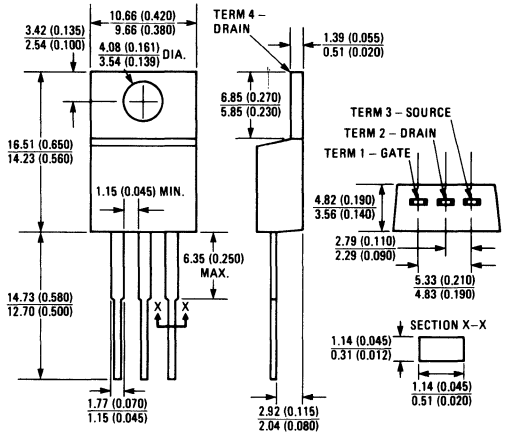
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF9530	-100V	0.30Ω	-12A
IRF9531	-60V	0.30Ω	-12A
IRF9532	-100V	0.40Ω	-10A
IRF9533	-60V	0.40Ω	-10A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Case Style TO-220AB
Dimensions in Millimeters and (Inches)

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IRF9530, IRF9531, IRF9532, IRF9533 Devices

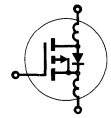
Absolute Maximum Ratings

Parameter		IRF9530	IRF9531	IRF9532	IRF9533	Units
V_{DS}	Drain - Source Voltage ①	-100	-60	-100	-60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	-100	-60	-100	-60	V
I_D @ T_C = 25°C	Continuous Drain Current	-12	-12	-10	-10	A
I_D @ T_C = 100°C	Continuous Drain Current	-7.5	-7.5	-6.5	-6.5	A
I_{DM}	Pulsed Drain Current ③	-48	-48	-40	-40	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH -48	-48	-40	-40	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF9530 IRF9532	-100	—	—	V	V_{GS} = 0V
		IRF9531 IRF9533	-60	—	—	V	I_D = -250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	-500	nA	V_{GS} = -20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	500	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	-250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	-1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF9530 IRF9531	-12	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = -10V
		IRF9532 IRF9533	-10	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF9530 IRF9531	—	0.25	0.30	Ω	V_{GS} = -10V, I_D = -6.5A
		IRF9532 IRF9533	—	0.30	0.40	Ω	
g_{fs}	Forward Transconductance ②	ALL	2.0	3.8	—	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = -6.5A
C_{iss}	Input Capacitance	ALL	—	500	700	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	300	450	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	100	200	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	30	60	ns	$V_{DD} \approx 0.5\ BV_{DSS}$, I_D = -6.5A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	70	140	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	70	140	ns	
t_f	Fall Time	ALL	—	70	140	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	25	45	nC	V_{GS} = -15V, I_D = -15A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	13	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	12	—	nC	
L_D	Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.
			—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	1.67	K/W	
R_{thCS}	Case-to-Sink	ALL	—	1.0	—	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF9530 IRF9531	–	–	-12	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF9532 IRF9533	–	–	-10	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF9530 IRF9531	–	–	-48	A	
		IRF9532 IRF9533	–	–	-40	A	
V_{SD}	Diode Forward Voltage ②	IRF9530 IRF9531	–	–	-6.3	V	T_C = 25°C, I_S = −12A, V_{GS} = 0V
		IRF9532 IRF9533	–	–	-6.0	V	T_C = 25°C, I_S = −10A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	300	–	ns	T_J = 150°C, I_F = −12A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	1.8	–	μC	T_J = 150°C, I_F = −12A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

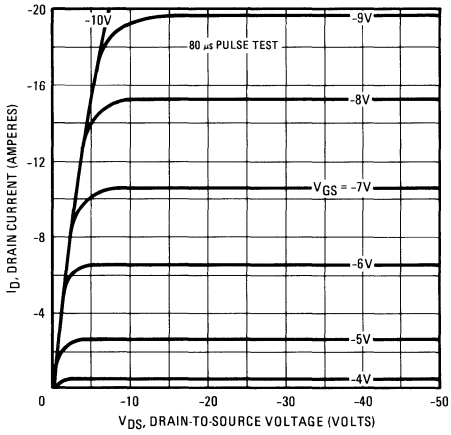


Fig. 1 — Typical Output Characteristics

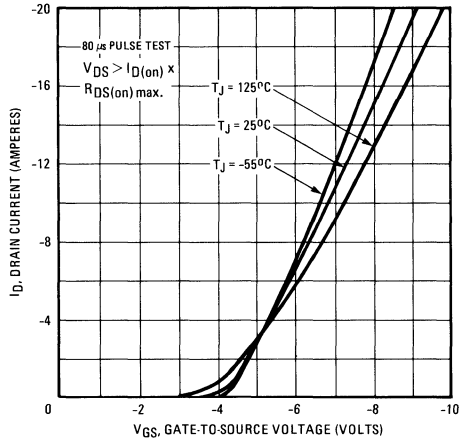


Fig. 2 — Typical Transfer Characteristics

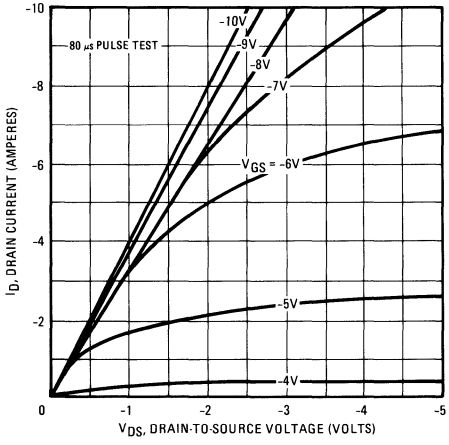


Fig. 3 — Typical Saturation Characteristics

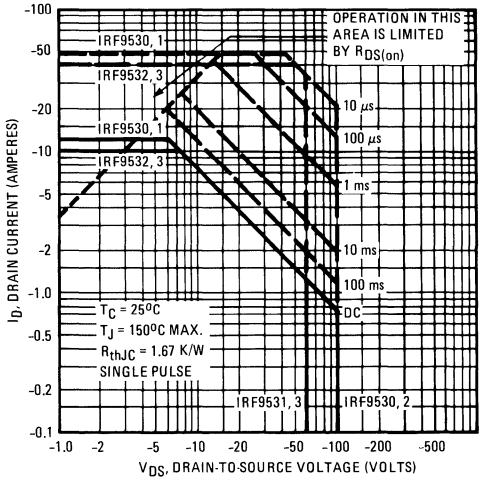


Fig. 4 — Maximum Safe Operating Area

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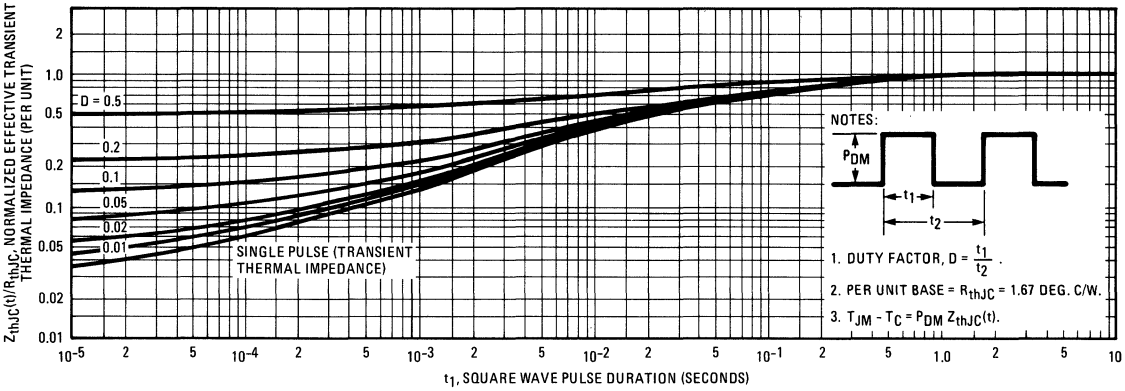


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

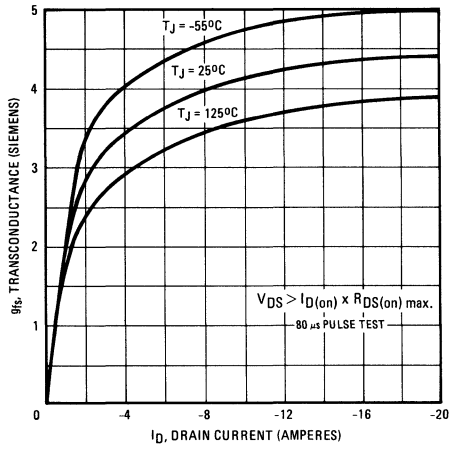


Fig. 6 — Typical Transconductance Vs. Drain Current

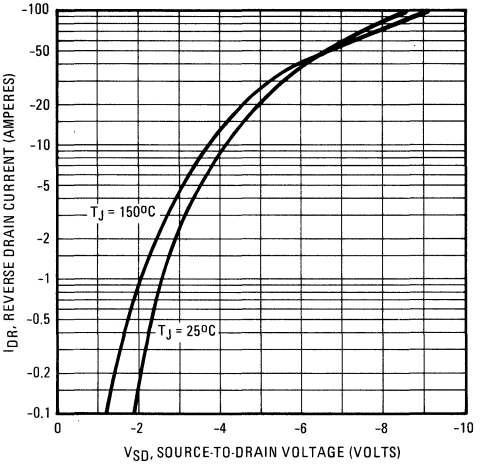


Fig. 7 — Typical Source-Drain Diode Forward Voltage

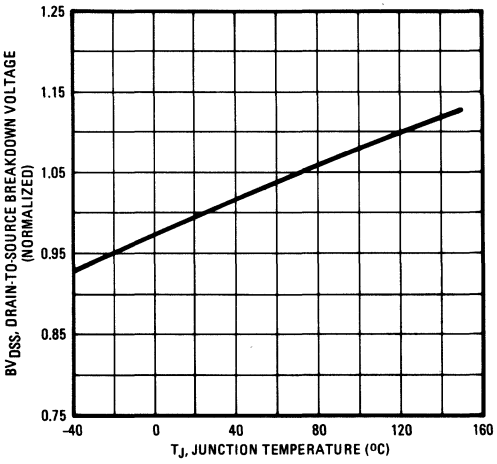


Fig. 8 — Breakdown Voltage Vs. Temperature

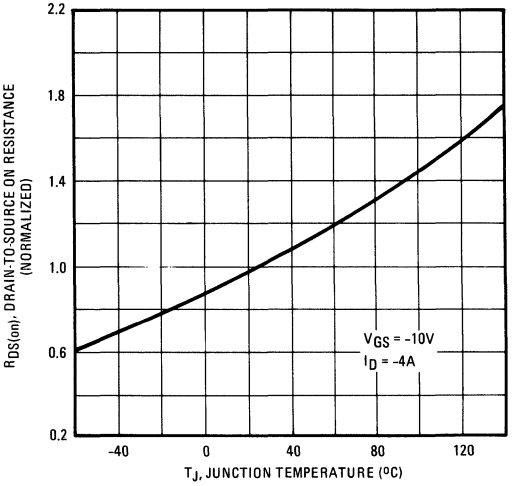


Fig. 9 — Normalized On-Resistance Vs. Temperature

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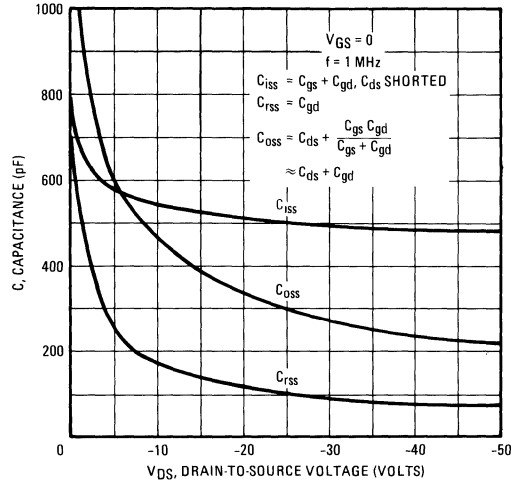


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

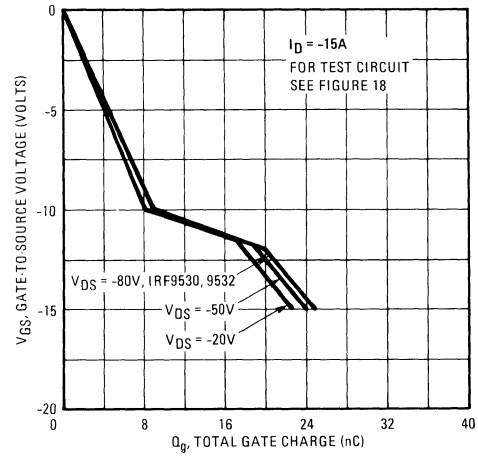


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

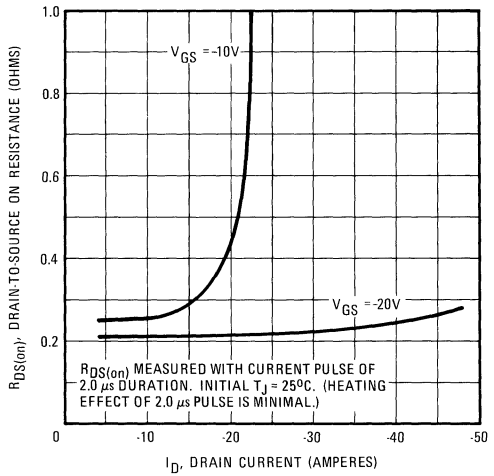


Fig. 12 — Typical On-Resistance Vs. Drain Current

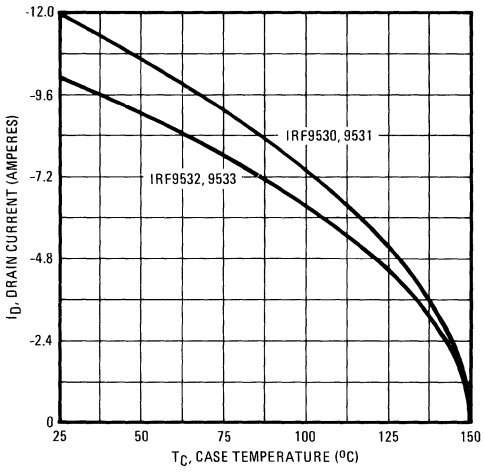


Fig. 13 — Maximum Drain Current Vs. Case Temperature

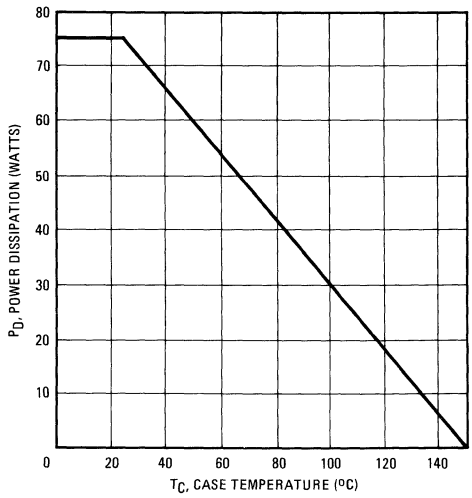


Fig. 14 — Power Vs. Temperature Derating Curve

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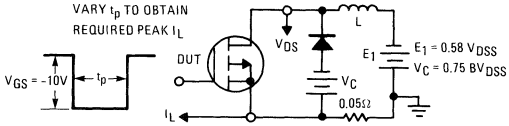


Fig. 15 — Clamped Inductive Test Circuit

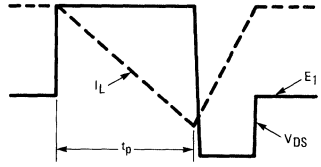


Fig. 16 — Clamped Inductive Waveforms

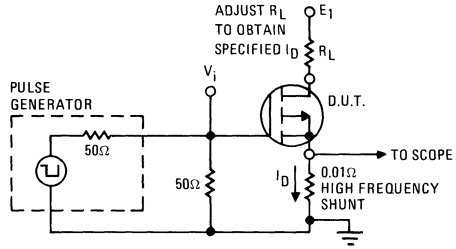


Fig. 17 — Switching Time Test Circuit

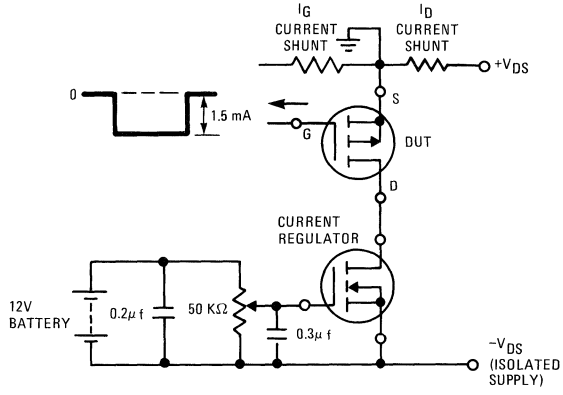


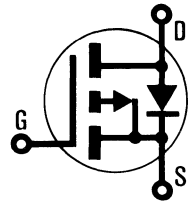
Fig. 18 — Gate Charge Test Circuit

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS IRF9610

P-CHANNEL 200 VOLT DEVICES



IRF9611
IRF9612
IRF9613

-200 Volt, 3.0 Ohm HEXFET TO-220AB Plastic Package

The HEXFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The P-Channel HEXFETs are designed for applications which require the convenience of reverse polarity operation. They retain all of the features of the more common N-Channel HEXFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and excellent temperature stability. The P-Channel IRF9610 device is an approximate electrical complement to the N-Channel IRF610 HEXFET for linear applications.

P-Channel HEXFETs are intended for use in power stages where complementary symmetry with N-Channel devices offers circuit simplification. They are also very useful in drive stages because of the circuit versatility offered by the reverse polarity connection. Applications include motor control, audio amplifiers, switched mode converters, control circuits and pulse amplifiers.

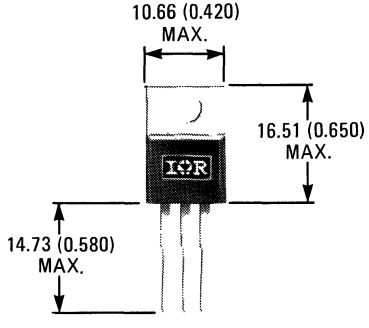
Features:

- P-Channel Versatility
- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

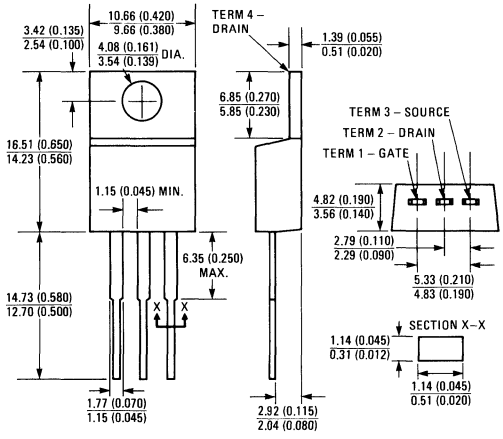
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF9610	-200V	3.0Ω	-1.75A
IRF9611	-150V	3.0Ω	-1.75A
IRF9612	-200V	4.5Ω	-1.5A
IRF9613	-150V	4.5Ω	-1.5A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Case Style TO-220AB
All Dimensions in Millimeters and (Inches)

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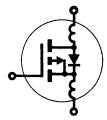
Absolute Maximum Ratings

Parameter		IRF9610	IRF9611	IRF9612	IRF9613	Units
V_{DS}	Drain - Source Voltage ①	-200	-150	-200	-150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	-200	-150	-200	-150	V
I_D @ T_C = 25°C	Continuous Drain Current	-1.75	-1.75	-1.5	-1.5	A
I_D @ T_C = 100°C	Continuous Drain Current	-1.0	-1.0	-0.9	-0.9	A
I_{DM}	Pulsed Drain Current ③	-7.0	-7.0	-6.0	-6.0	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	20 (See Fig. 14)				W
	Linear Derating Factor	0.16 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		-7.0	-7.0	-6.0	-6.0	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF9610 IRF9612	-200	—	—	V	V_{GS} = 0V
		IRF9611 IRF9613	-150	—	—	V	I_D = -250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	-500	nA	V_{GS} = -20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	500	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	-250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	-1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF9610 IRF9611	-1.75	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = -10V
		IRF9612 IRF9613	-1.5	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF9610 IRF9611	—	2.3	3.0	Ω	V_{GS} = -10V, I_D = -0.9A
		IRF9612 IRF9613	—	3.5	4.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.9	1.3	—	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = -0.9A
C_{iss}	Input Capacitance	ALL	—	170	300	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	50	100	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	15	35	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	8.0	15	ns	$V_{DD} \approx 0.5\ BV_{DSS}$, I_D = -0.9A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	15	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	10	15	ns	
t_f	Fall Time	ALL	—	8.0	15	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	8.0	11	nC	V_{GS} = -15V, I_D = -3.5A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	5.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	3.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.
			—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	6.4	K/W	
R_{thCS}	Case-to-Sink	ALL	—	1.0	—	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF9610 IRF9611	—	—	-1.75	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF9612 IRF9613	—	—	-1.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF9610 IRF9611	—	—	-7.0	A	
		IRF9612 IRF9613	—	—	-6.0	A	
V_{SD}	Diode Forward Voltage ②	IRF9610 IRF9611	—	—	-5.8	V	T_C = 25°C, I_S = -1.75A, V_{GS} = 0V
		IRF9612 IRF9613	—	—	-5.5	V	T_C = 25°C, I_S = -1.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	240	—	ns	T_J = 150°C, I_F = -1.75A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	1.7	—	μC	T_J = 150°C, I_F = -1.75A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

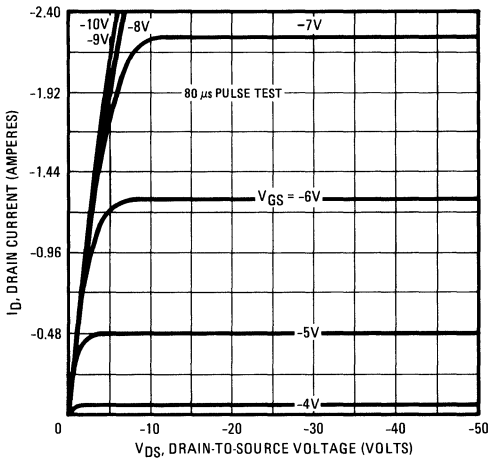


Fig. 1 — Typical Output Characteristics

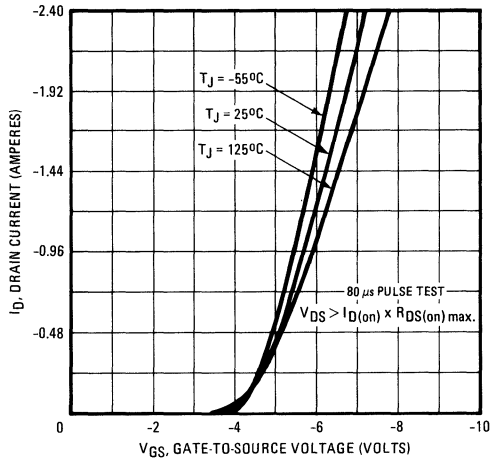


Fig. 2 — Typical Transfer Characteristics

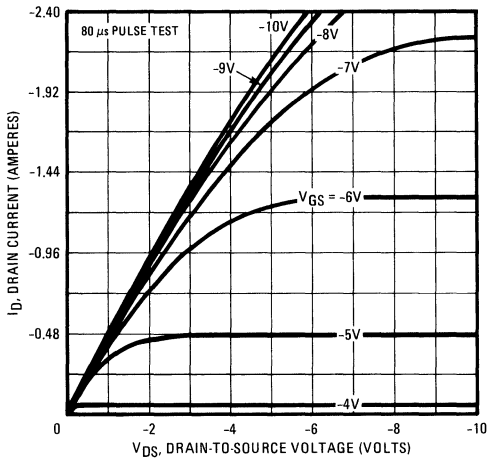


Fig. 3 — Typical Saturation Characteristics

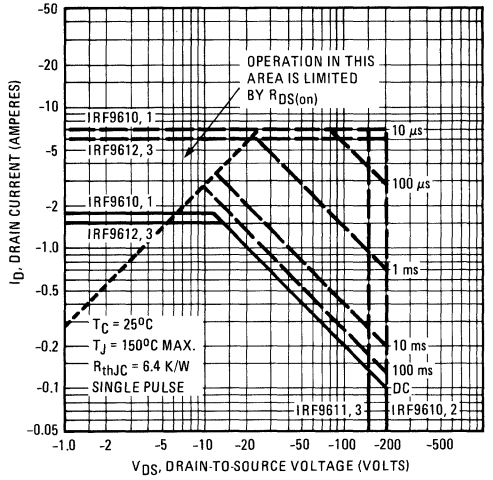


Fig. 4 — Maximum Safe Operating Area

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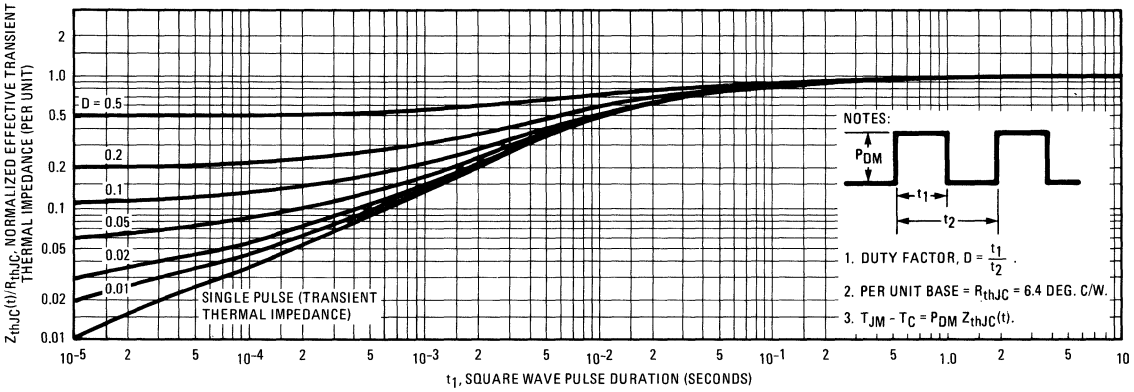


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

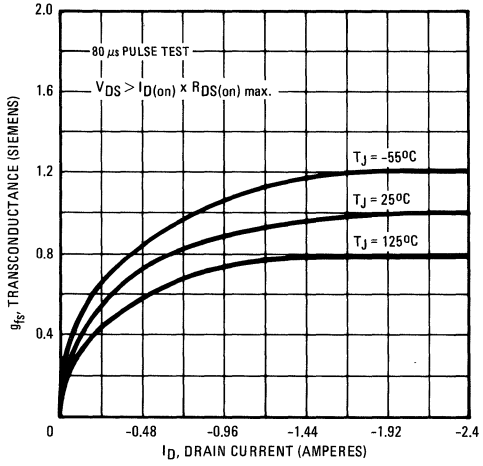


Fig. 6 — Typical Transconductance Vs. Drain Current

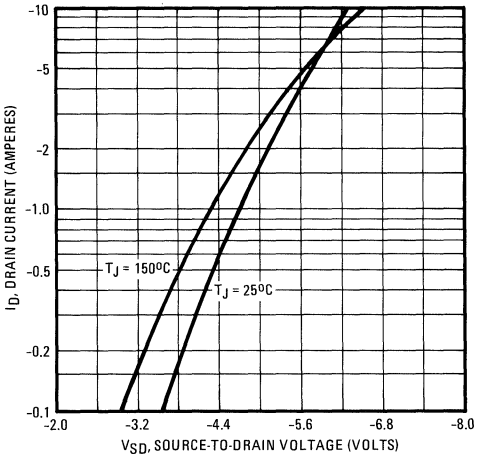


Fig. 7 — Typical Source-Drain Diode Forward Voltage

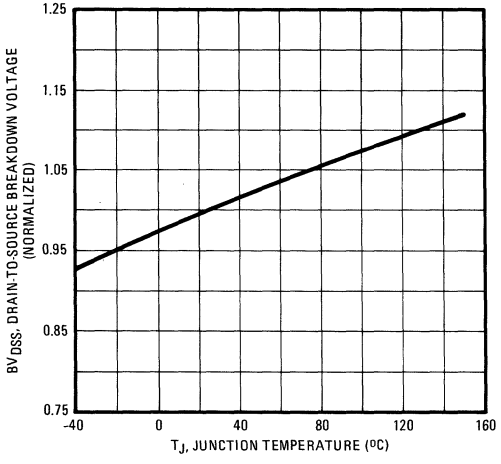


Fig. 8 — Breakdown Voltage Vs. Temperature

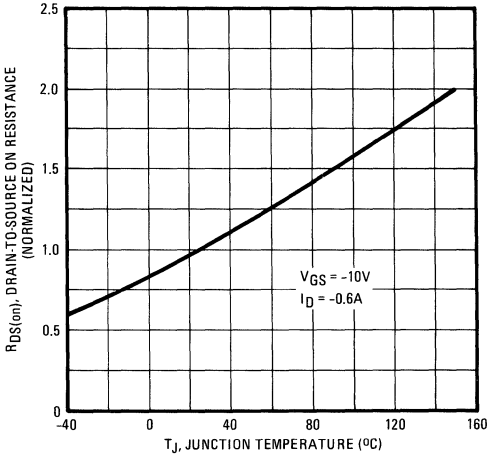


Fig. 9 — Normalized On-Resistance Vs. Temperature

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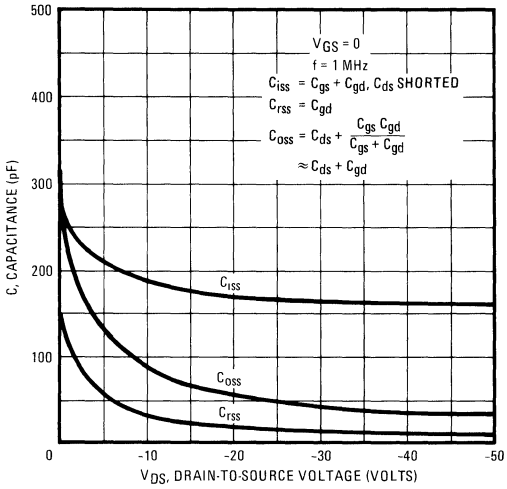


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

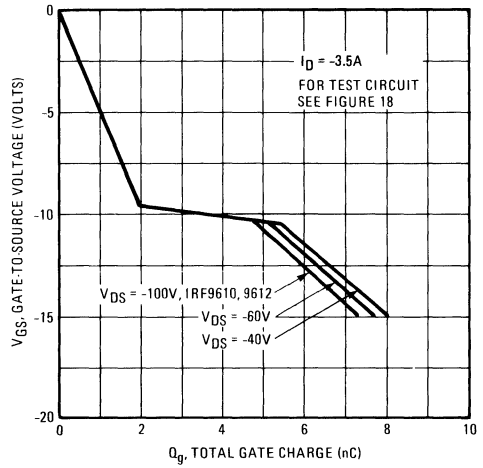


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

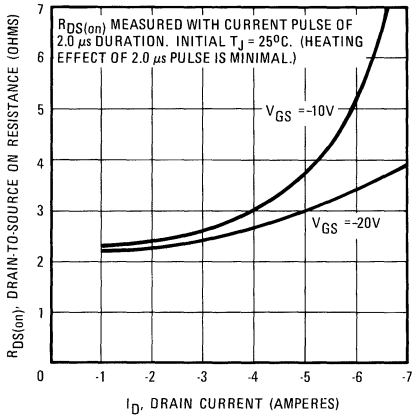


Fig. 12 — Typical On-Resistance Vs. Drain Current

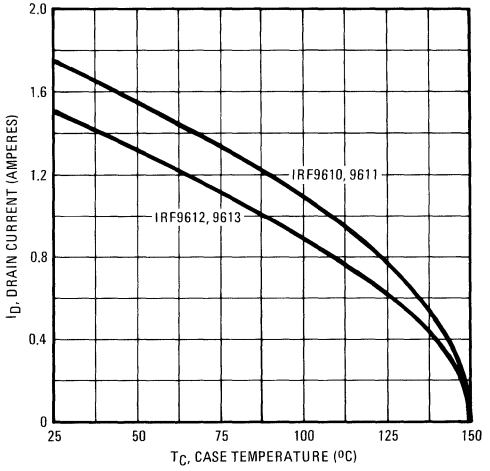


Fig. 13 — Maximum Drain Current Vs. Case Temperature

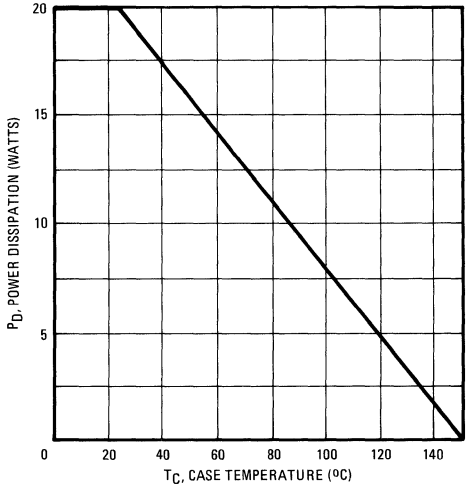


Fig. 14 — Power Vs. Temperature Derating Curve

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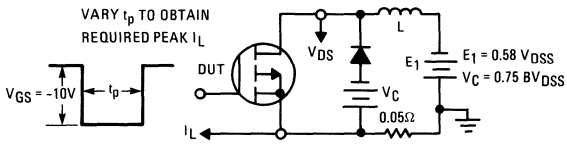


Fig. 15 — Clamped Inductive Test Circuit

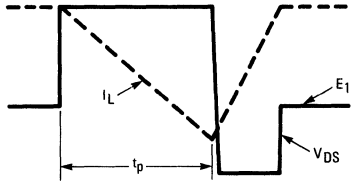


Fig. 16 — Clamped Inductive Waveforms

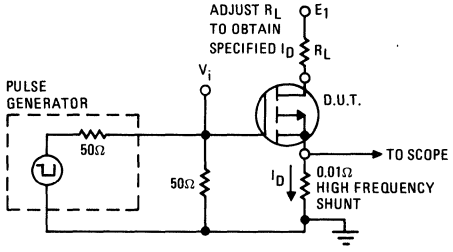


Fig. 17 — Switching Time Test Circuit

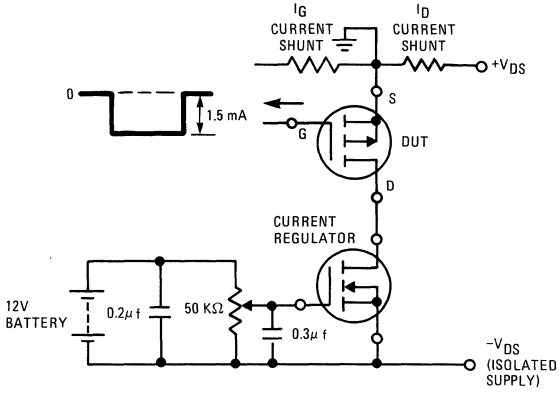


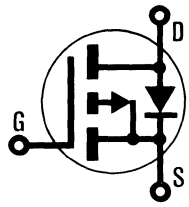
Fig. 18 — Gate Charge Test Circuit

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS IRF9620

P-CHANNEL 200 VOLT POWER MOSFETs



IRF9621
IRF9622
IRF9623

-200 Volt, 1.5 Ohm HEXFET TO-220AB Plastic Package

The HEXFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The P-Channel HEXFETs are designed for applications which require the convenience of reverse polarity operation. They retain all of the features of the more common N-Channel HEXFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and excellent temperature stability. The P-Channel IRF9620 device is an approximate electrical complement to the N-Channel IRF610 HEXFET.

P-Channel HEXFETs are intended for use in power stages where complementary symmetry with N-Channel devices offers circuit simplification. They are also very useful in drive stages because of the circuit versatility offered by the reverse polarity connection. Applications include motor control, audio amplifiers, switched mode converters, control circuits and pulse amplifiers.

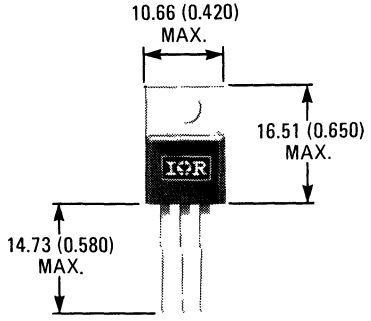
Features:

- P-Channel Versatility
- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

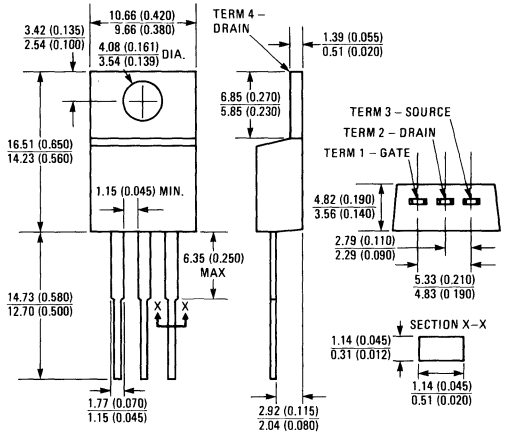
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF9620	-200V	1.5Ω	-3.5A
IRF9621	-150V	1.5Ω	-3.5A
IRF9622	-200V	2.4Ω	-3.0A
IRF9623	-150V	2.4Ω	-3.0A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Case Style TO-220AB
All Dimensions in Millimeters and (Inches)

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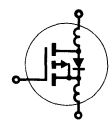
Absolute Maximum Ratings

Parameter		IRF9620	IRF9621	IRF9622	IRF9623	Units
V_{DS}	Drain - Source Voltage ①	-200	-150	-200	-150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	-200	-150	-200	-150	V
I_D @ T_C = 25°C	Continuous Drain Current	-3.5	-3.5	-3.0	-3.0	A
I_D @ T_C = 100°C	Continuous Drain Current	-2.0	-2.0	-1.5	-1.5	A
I_{DM}	Pulsed Drain Current ③	-14	-14	-12	-12	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		-14	-14	-12	-12	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF9620 IRF9622	-200	—	—	V	V_{GS} = 0V
		IRF9621 IRF9623	-150	—	—	V	I_D = -250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	-500	nA	V_{GS} = -20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	500	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	-250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	-1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF9620 IRF9621	-3.5	—	—	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = -10V
		IRF9622 IRF9623	-3.0	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF9620 IRF9621	—	1.0	1.5	Ω	V_{GS} = -10V, I_D = -1.5A
		IRF9622 IRF9623	—	1.5	2.4	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	1.8	—	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = -1.5A
C_{iss}	Input Capacitance	ALL	—	350	400	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	100	125	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	30	45	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	15	40	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 1.5A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	25	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	20	50	ns	
t_f	Fall Time	ALL	—	15	40	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	16	22	nC	V_{GS} = 15V, I_D = -4.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	9.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	7.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.
			—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	3.12	K/W	
R_{thCS}	Case-to-Sink	ALL	—	1.0	—	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF9620 IRF9621	—	—	-3.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF9622 IRF9623	—	—	-3.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF9620 IRF9621	—	—	-14	A	
		IRF9622 IRF9623	—	—	-12	A	
V_{SD}	Diode Forward Voltage ②	IRF9620 IRF9621	—	—	-7.0	V	T_C = 25°C, I_S = -3.5A, V_{GS} = 0V
		IRF9622 IRF9623	—	—	-6.8	V	T_C = 25°C, I_S = -3.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	300	—	ns	T_J = 150°C, I_F = -3.5A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	1.9	—	μC	T_J = 150°C, I_F = -3.5A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

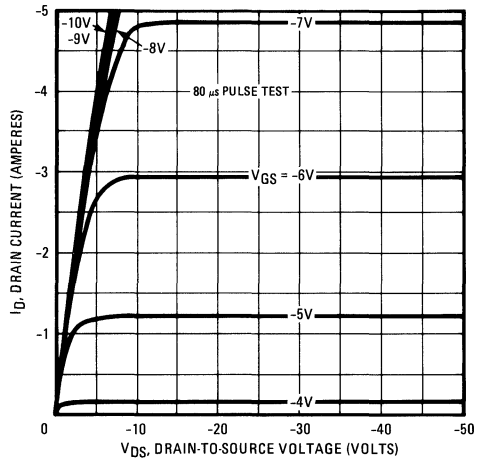


Fig. 1 — Typical Output Characteristics

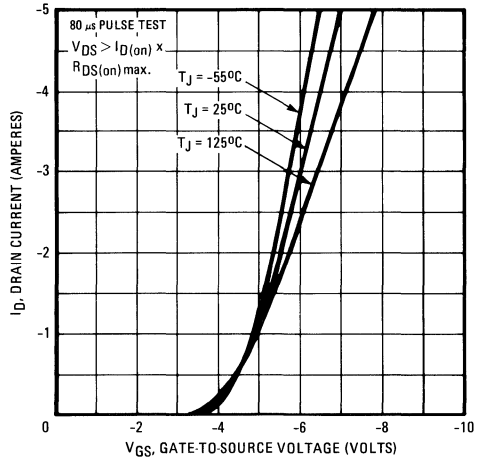


Fig. 2 — Typical Transfer Characteristics

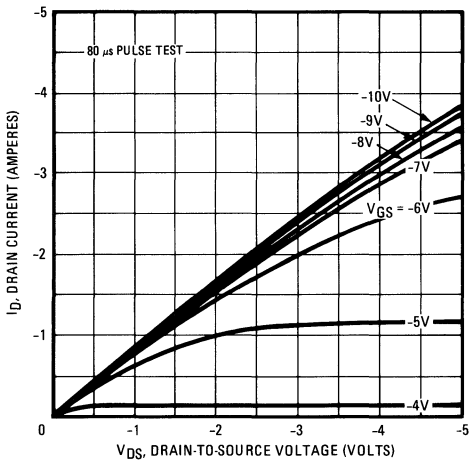


Fig. 3 — Typical Saturation Characteristics

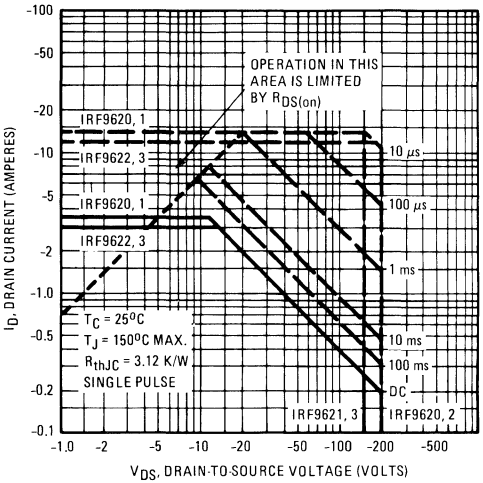


Fig. 4 — Maximum Safe Operating Area

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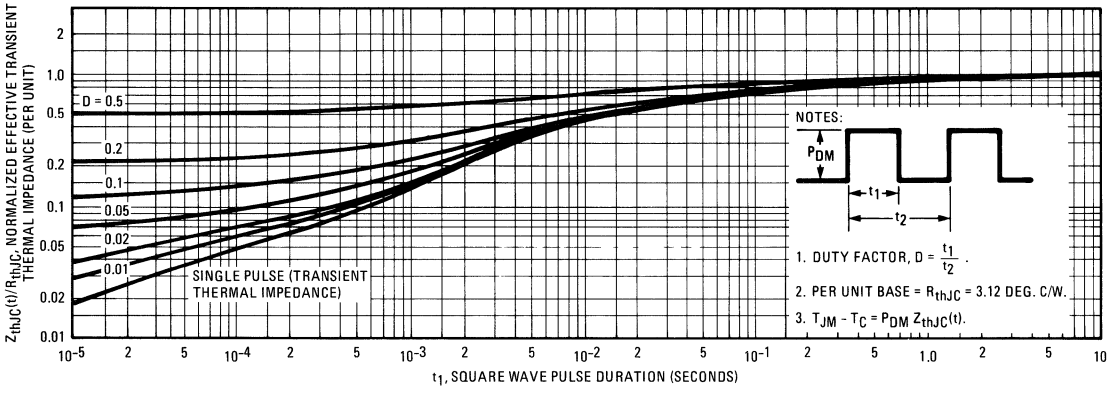


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

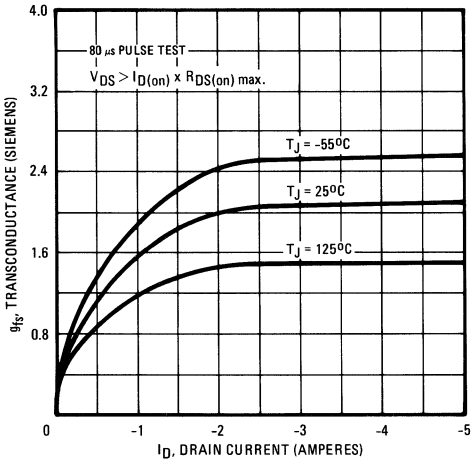


Fig. 6 — Typical Transconductance Vs. Drain Current

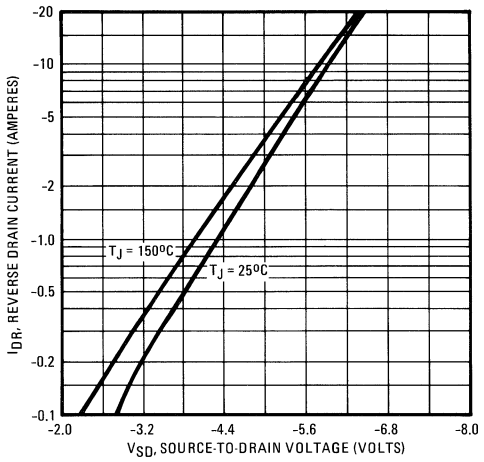


Fig. 7 — Typical Source-Drain Diode Forward Voltage

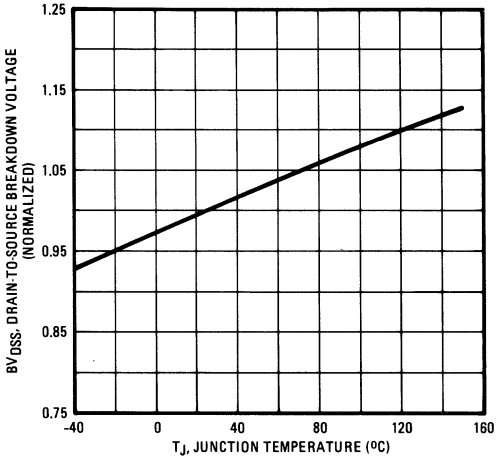


Fig. 8 — Breakdown Voltage Vs. Temperature

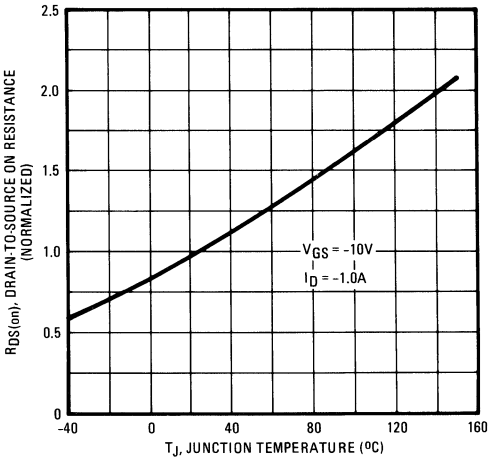


Fig. 9 — Normalized On-Resistance Vs. Temperature

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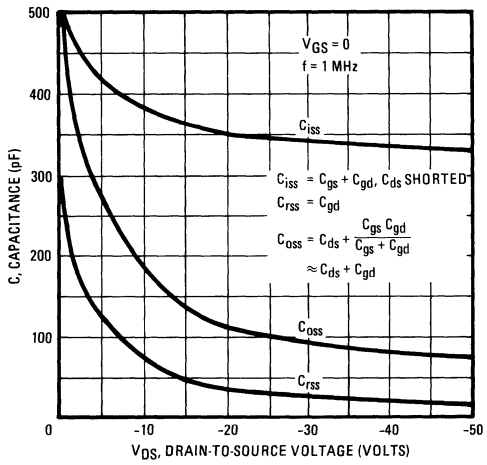


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

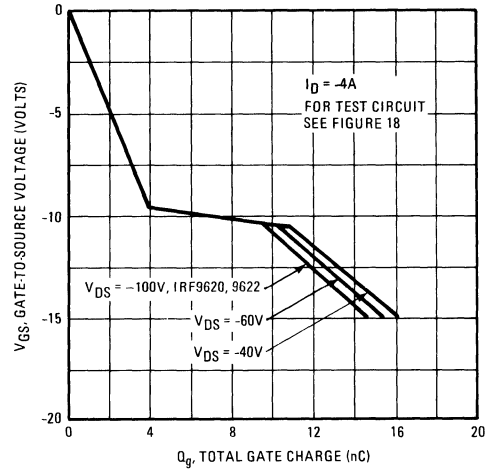


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

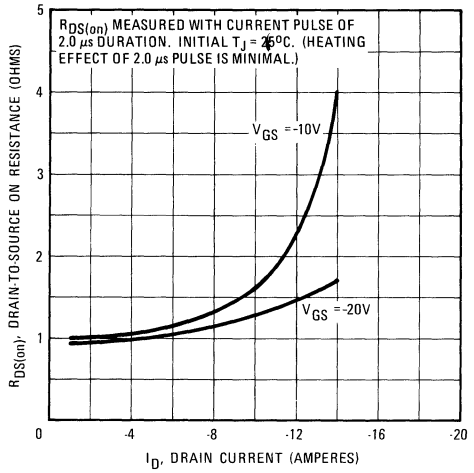


Fig. 12 — Typical On-Resistance Vs. Drain Current

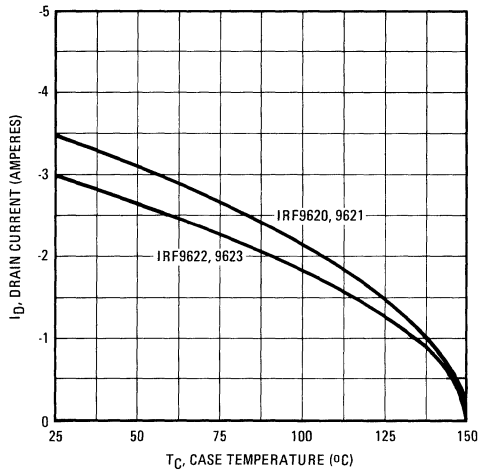


Fig. 13 — Maximum Drain Current Vs. Case Temperature

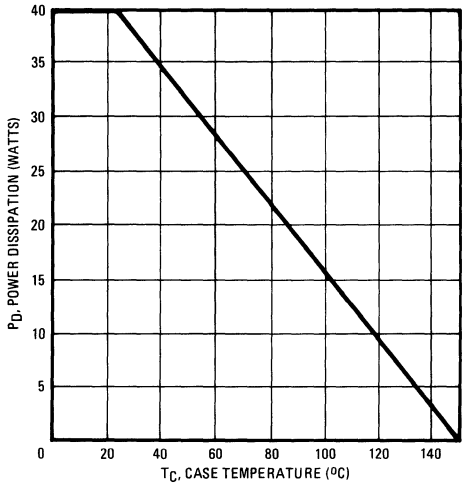


Fig. 14 — Power Vs. Temperature Derating Curve

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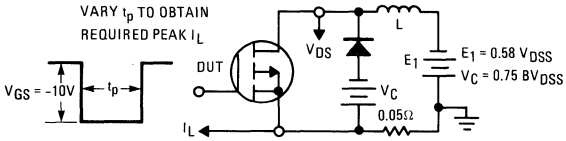


Fig. 15 — Clamped Inductive Test Circuit

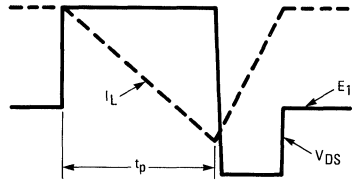


Fig. 16 — Clamped Inductive Waveforms

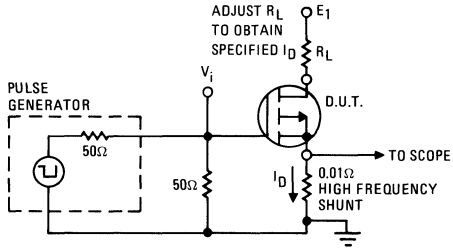


Fig. 17 — Switching Time Test Circuit

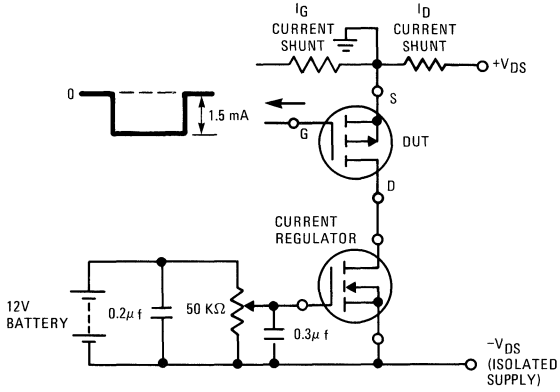


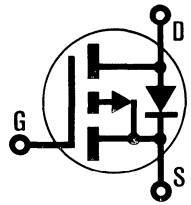
Fig. 18 — Gate Charge Test Circuit

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INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS IRF9630

P-CHANNEL 200 VOLT POWER MOSFETs



IRF9631
IRF9632
IRF9633

-200 Volt, 0.8 Ohm HEXFET
TO-220AB Plastic Package

The HEXFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The P-Channel HEXFETs are designed for applications which require the convenience of reverse polarity operation. They retain all of the features of the more common N-Channel HEXFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and excellent temperature stability. The P-Channel IRF9630 device is an approximate electrical complement to the N-Channel IRF620 HEXFET.

P-Channel HEXFETs are intended for use in power stages where complementary symmetry with N-Channel devices offers circuit simplification. They are also very useful in drive stages because of the circuit versatility offered by the reverse polarity connection. Applications include motor control, audio amplifiers, switched mode converters, control circuits and pulse amplifiers.

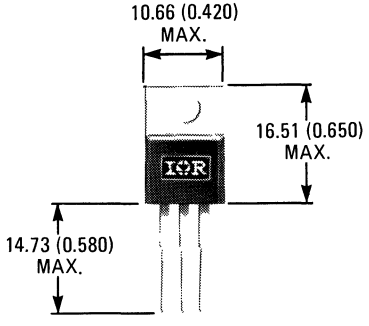
Features:

- P-Channel Versatility
- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- No Second Breakdown
- Excellent Temperature Stability

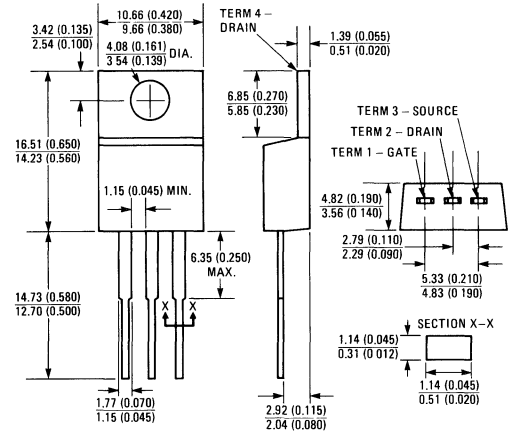
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF9630	-200V	0.8Ω	-6.5A
IRF9631	-150V	0.8Ω	-6.5A
IRF9632	-200V	1.2Ω	-5.5A
IRF9633	-150V	1.2Ω	-5.5A

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Case Style TO-220AB
All Dimensions in Millimeters and (Inches)

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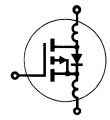
Absolute Maximum Ratings

Parameter		IRF9630	IRF9631	IRF9632	IRF9633	Units
V_{DS}	Drain - Source Voltage ①	-200	-150	-200	-150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 1 MΩ) ①	-200	-150	-200	-150	V
I_D @ T_C = 25°C	Continuous Drain Current	-6.5	-6.5	-5.5	-5.5	A
I_D @ T_C = 100°C	Continuous Drain Current	-4.0	-4.0	-3.5	-3.5	A
I_{DM}	Pulsed Drain Current ③	-26	-26	-22	-22	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		-26	-26	-22	-22	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF9630 IRF9632	-200	–	–	V	V_{GS} = 0V
		IRF9631 IRF9633	-150	–	–	V	I_D = -250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	-2.0	–	-4.0	V	V_{DS} = V_{GS}, I_D = -250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	-500	nA	V_{GS} = -20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	500	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	-250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	-1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF9630 IRF9631	-6.5	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = -10V
		IRF9632 IRF9633	-5.5	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF9630 IRF9631	–	0.5	0.8	Ω	V_{GS} = -10V, I_D = -3.5A
		IRF9632 IRF9633	–	0.8	1.2	Ω	
g_{fs}	Forward Transconductance ②	ALL	2.2	3.5	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = -3.5A
C_{iss}	Input Capacitance	ALL	–	550	650	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	170	300	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	50	90	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	30	50	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = -3.5A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	50	100	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	40	80	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	31	45	nC	V_{GS} = -15V, I_D = -8.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	18	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	13	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67	K/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	K/W	Free Air Operation

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Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF9630 IRF9631	—	—	-6.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF9632 IRF9633	—	—	-5.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF9630 IRF9631	—	—	-26	A	
		IRF9632 IRF9633	—	—	-22	A	
V_{SD}	Diode Forward Voltage ②	IRF9630 IRF9631	—	—	-6.5	V	T_C = 25°C, I_S = -6.5A, V_{GS} = 0V
		IRF9632 IRF9633	—	—	-6.3	V	T_C = 25°C, I_S = -5.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	400	—	ns	T_J = 150°C, I_F = -6.5A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	2.6	—	μC	T_J = 150°C, I_F = -6.5A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

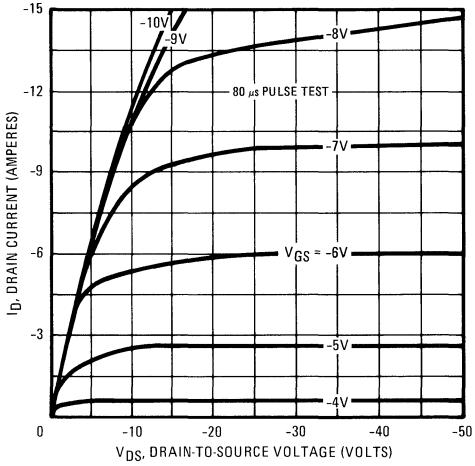


Fig. 1 — Typical Output Characteristics

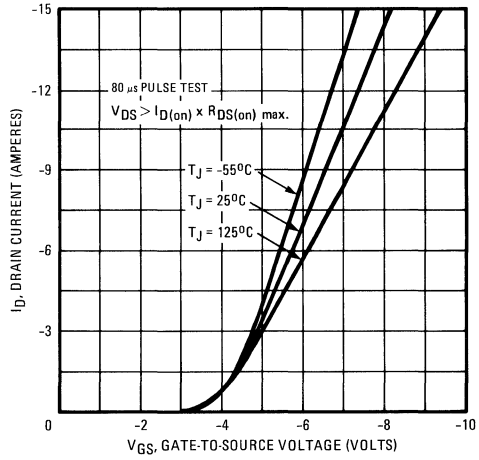


Fig. 2 — Typical Transfer Characteristics

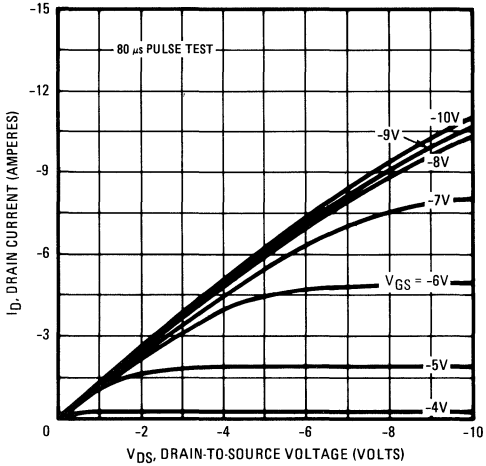


Fig. 3 — Typical Saturation Characteristics

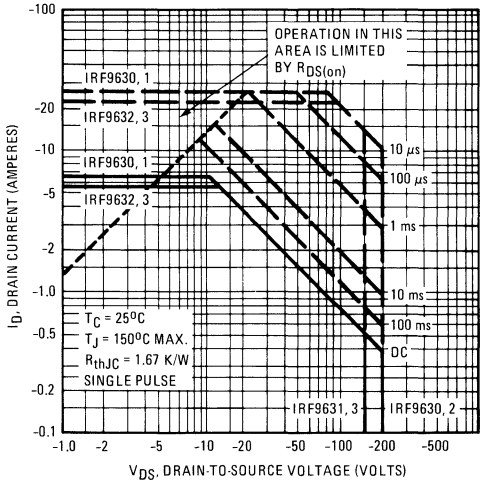


Fig. 4 — Maximum Safe Operating Area

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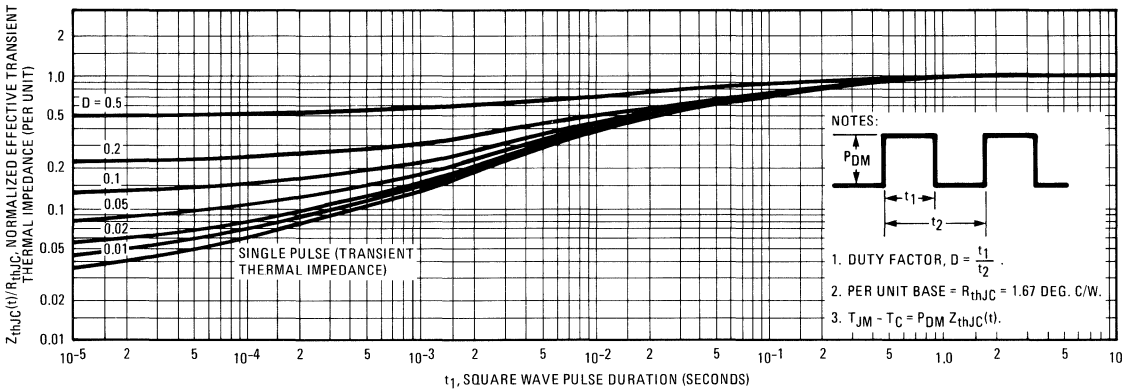


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

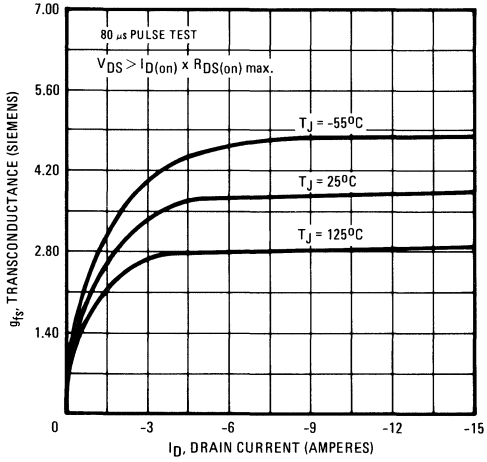


Fig. 6 — Typical Transconductance Vs. Drain Current

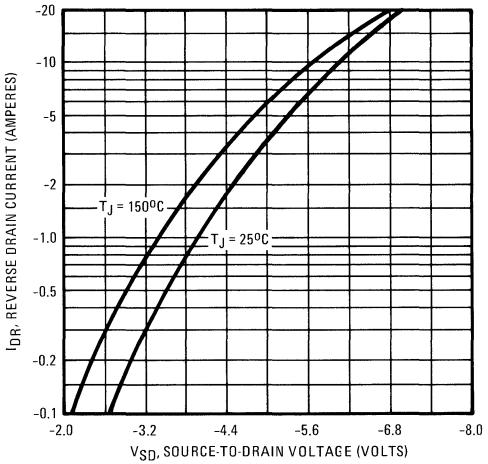


Fig. 7 — Typical Source-Drain Diode Forward Voltage

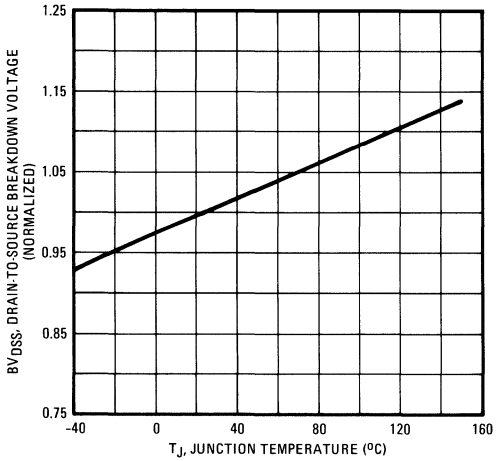


Fig. 8 — Breakdown Voltage Vs. Temperature

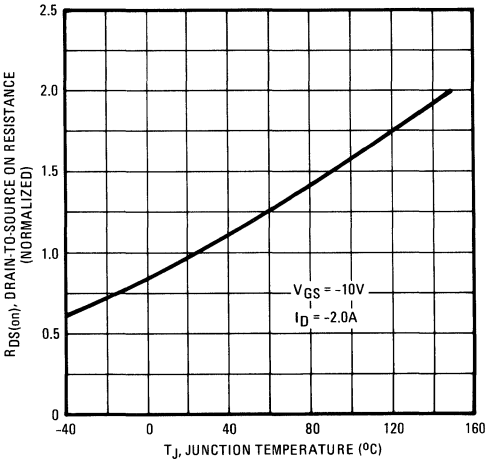


Fig. 9 — Normalized On-Resistance Vs. Temperature

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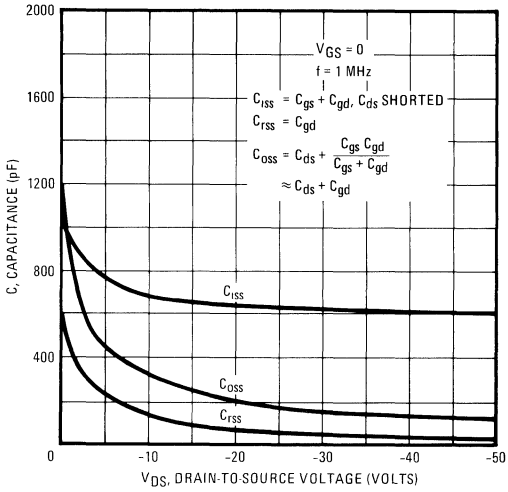


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

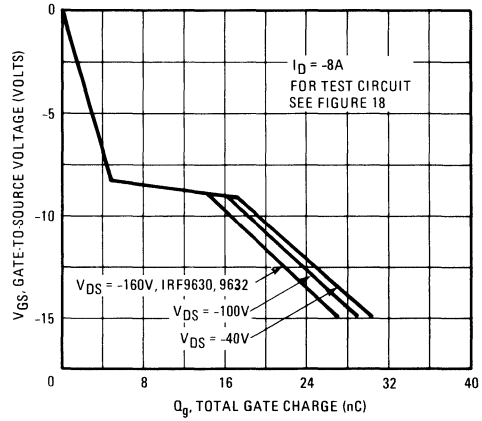


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

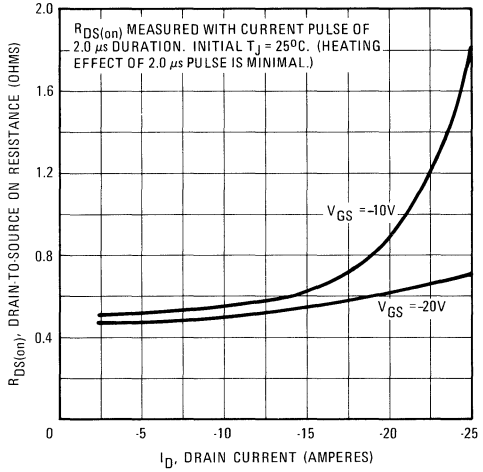


Fig. 12 — Typical On-Resistance Vs. Drain Current

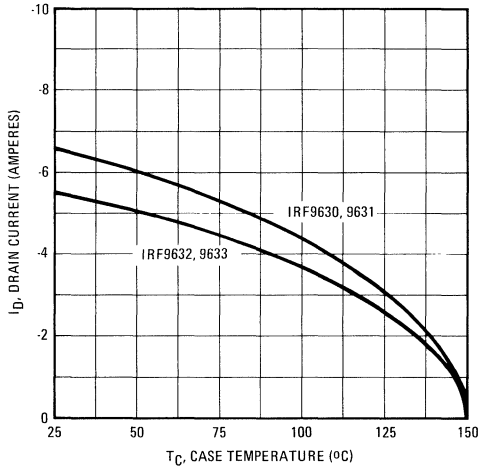


Fig. 13 — Maximum Drain Current Vs. Case Temperature

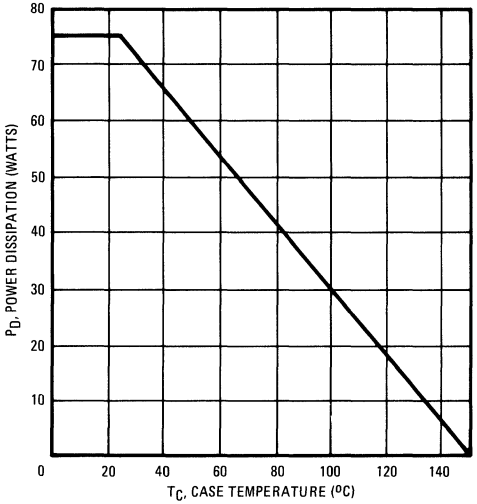


Fig. 14 — Power Vs. Temperature Derating Curve

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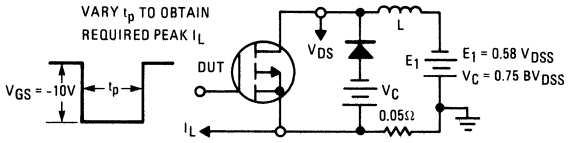


Fig. 15 — Clamped Inductive Test Circuit

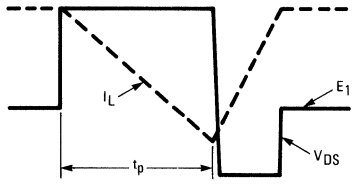


Fig. 16 — Clamped Inductive Waveforms

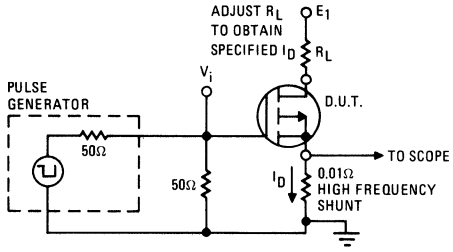


Fig. 17 — Switching Time Test Circuit

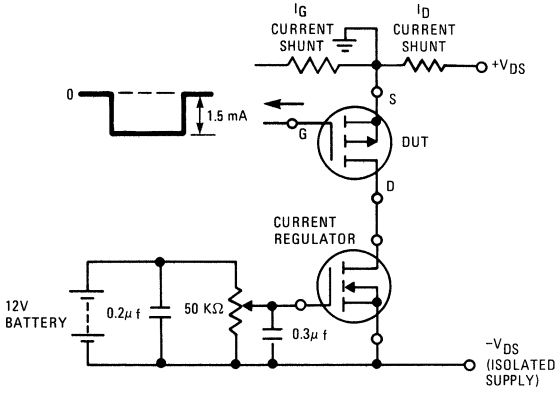
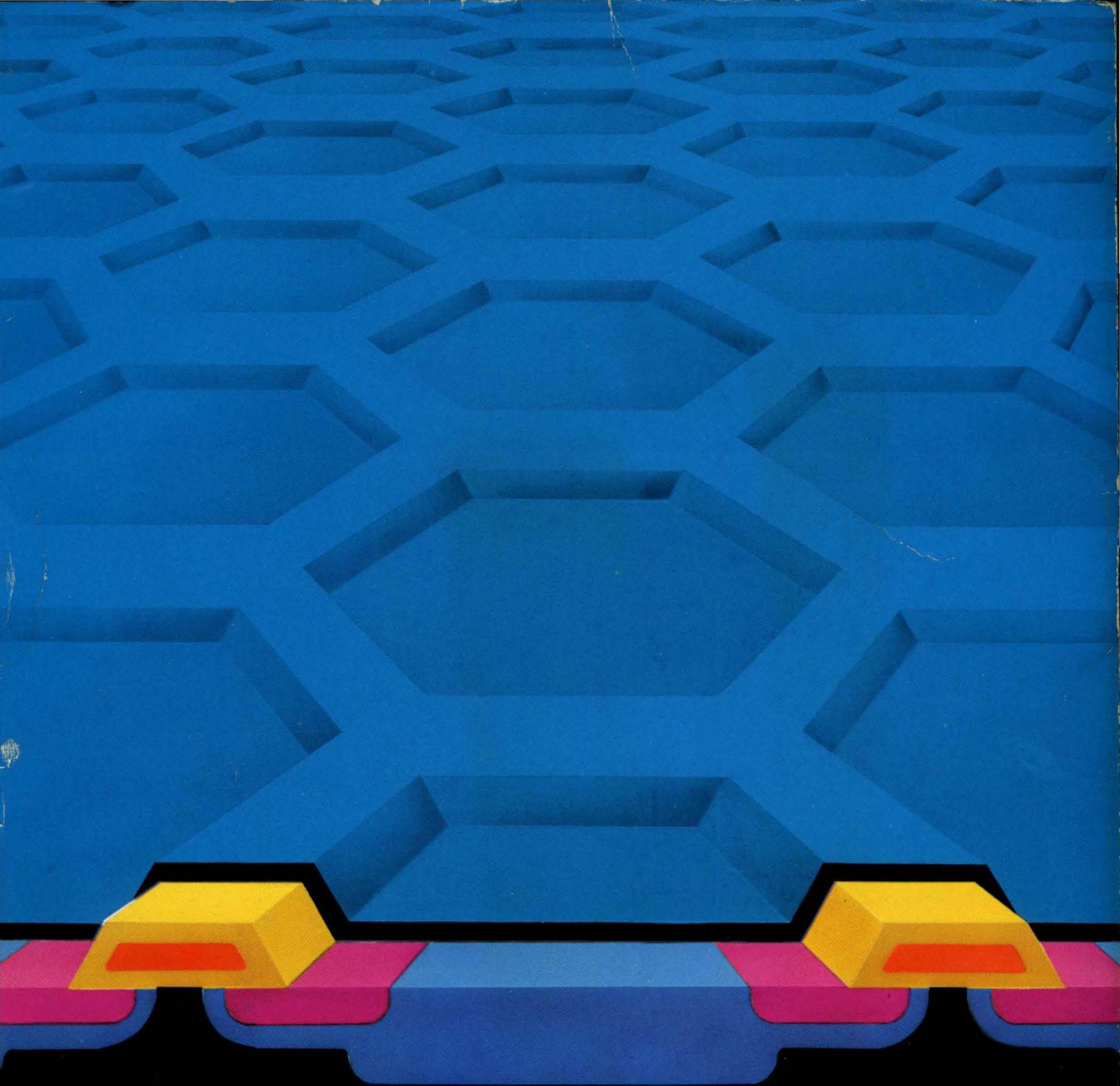


Fig. 18 — Gate Charge Test Circuit

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