SY89113U

2.5V Low Jitter, Low Skew 1:12 LVDS Fanout Buffer with 2:1 Input MUX and Internal Termination

Features

- Selects between 1 of 2 Inputs, and Provides 12 Precision, Low Skew LVDS Output Copies
- Guaranteed AC Performance Overtemperature and Voltage:
  - DC to >1 GHz Throughput
  - <975 ps Propagation Delay CLK0-to-Q
  - <250 ps Rise/Fall Time
  - <25 ps Output-to-Output Skew
- Ultra-low Jitter Design:
  - 130 fs RMS Phase Jitter (Typ)
  - 0.7 ps_{RMS} Crosstalk Induced Jitter
- Unique, Patent-pending 2:1 Input MUX Provides Superior Isolation to Minimize Channel-to-Channel Crosstalk
- CLK0 Input Features a Unique, Patent-pending Input Termination and VT Pin that Accepts AC- and DC-coupled Inputs (CML, LVPECL, LVDS)
- CLK1 Accepts Virtually Any Logic Standard:
  - Single-ended: TTL/CMOS (Including 3.3V Logic), LVPECL
  - Differential: LVPECL, LVDS, CML, HSTL
- 325 mV LVDS-compatible Output Swing
- Power Supply: 2.5V ±5%
- Industrial Temperature Range –40°C to +85°C
- Available in 44-lead (7 mm × 7 mm) VQFN Package

Applications

- Multi-processor Server
- SONET/SDH Clock/Data Distribution
- Fibre Channel Distribution
- Gigabit Ethernet Clock Distribution

General Description

The SY89113U is a 2.5V low jitter, low skew, 1:12 LVDS fanout buffer optimized for precision telecom and enterprise server distribution applications. The input includes a 2:1 MUX for clock switchover applications. Unlike other multiplexers, this input includes a unique isolation design that minimizes channel-to-channel crosstalk. The SY89113U distributes clock frequencies from DC to >1 GHz guaranteed over temperature and voltage.

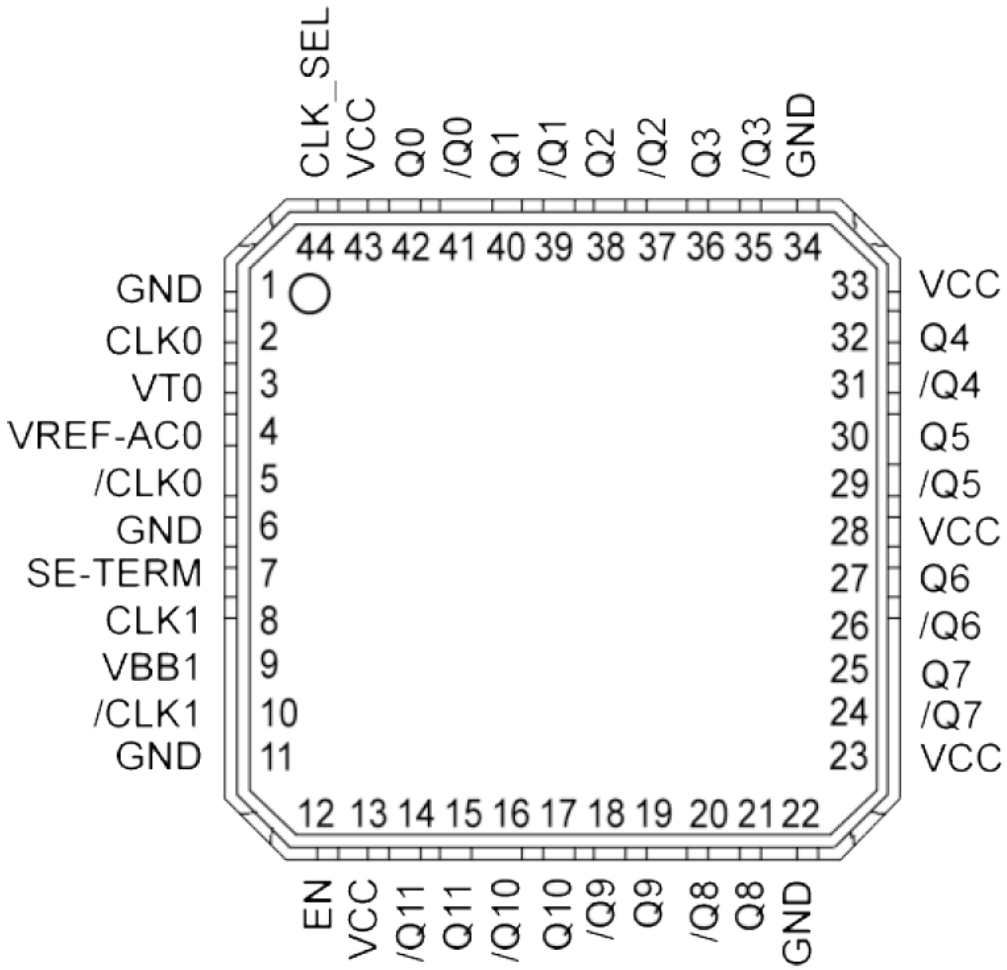
The SY89113U incorporates a synchronous output enable (EN) so that the outputs will only be enabled/disabled when they are already in the LOW state. CLK0 differential input includes Microchip's unique, 3-pin input termination architecture that directly interfaces to any differential signal (AC- or DC-coupled) as small as 100 mV (200 mV_{PP}) without any level shifting or termination resistor networks in the signal path.

CLK1 differential input includes a new version of Microchip's unique, Any-Input architecture that directly interfaces with single-ended TTL/CMOS logic (including 3.3V logic), single-ended LVPECL, differential (AC- or DC-coupled) LVDS, HSTL, CML, and LVPECL logic levels as small as 200 mV (400 mV_{PP}). CLK1 input requires external termination. LVDS output swing 325 mV into 100Ω with extremely fast rise/fall time guaranteed to be less than 250 ps.

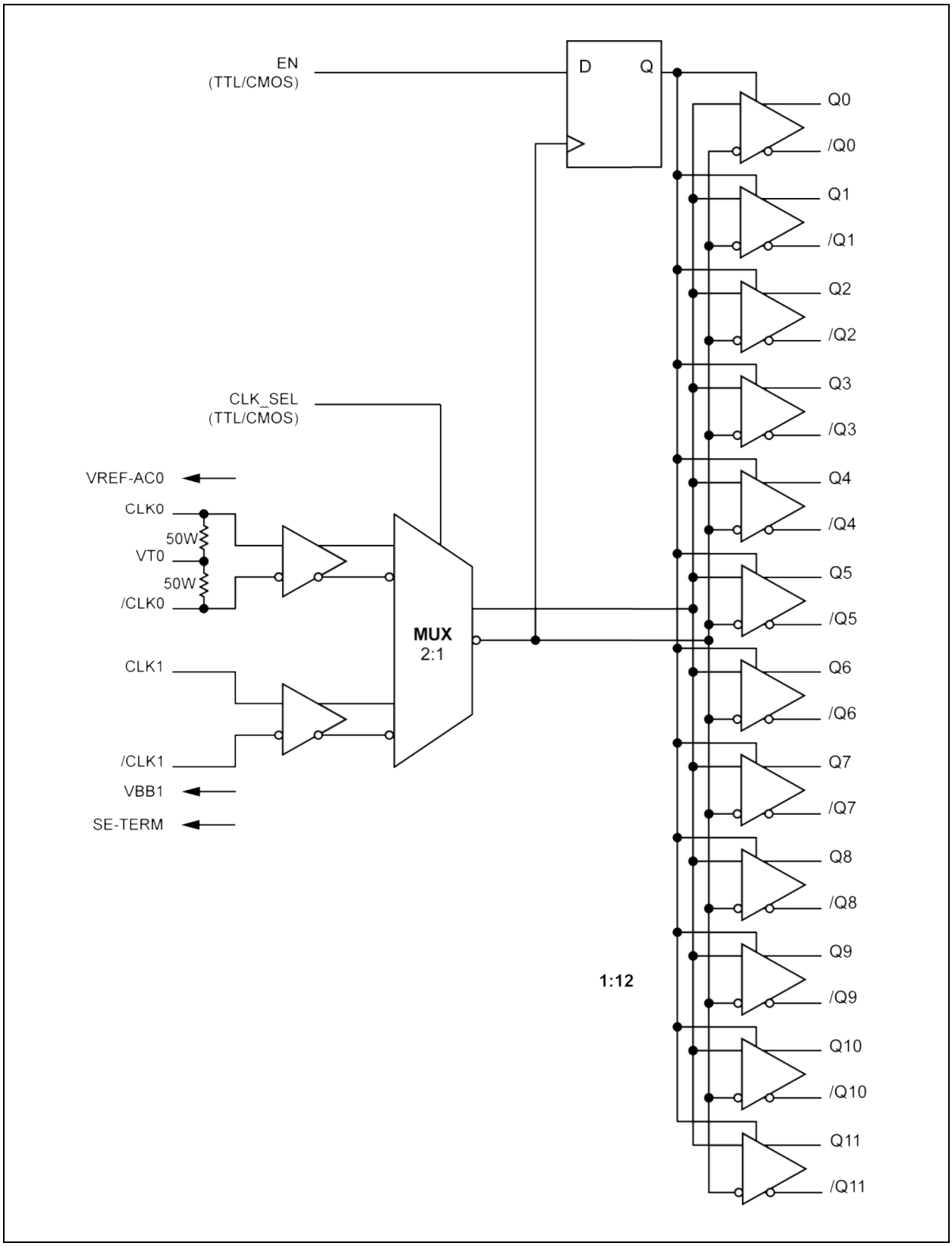
The SY89113U operates from a 2.5V±5% supply and is guaranteed over the full industrial temperature range of -40°C to +85°C. The SY89113U is part of Microchip's high-speed, Precision Edge® product line.

Package Type

SY89113U
44-Lead VQFN



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (Differential Input CLK0, CLK1)..... –0.5V to V_{CC}
Current on Reference Voltage Outputs, source or sink current on VREF-AC0/VBB1.....±2 mA
Termination Current, source or sink current on VT0.....±100 mA
Input Current, source or sink current on CLK0, /CLK0.....±50 mA

Operating Ratings††

Supply Voltage (V_{CC}) ..... +2.375V to +2.625V

† **Notice:** Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

†† **Notice:** The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

TABLE 1-1: DC ELECTRICAL CHARACTERISTICS

T_A = –40°C to +85°C unless otherwise stated. (Note 1)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Power Supply	V_{CC}	2.375	—	2.625	V	—
Power Supply Current	I_{CC}	—	240	330	mA	No load, max. V_{CC}
Input Resistance (CLK0-to-VT)	R_{IN}	45	50	55	Ω	—
Differential Input Resistance (CLK0-to-/CLK0)	R_{DIFF_IN}	90	100	110	Ω	—
Input High Voltage (CLK0, /CLK0)	V_{IH}	1.2	—	V_{CC}	V	—
Input High Voltage (CLK1, /CLK1)		0.2	—	V_{CC}	V	Note 2
		1.2	—	3.6	V	Note 3
Input Low Voltage (CLK0, /CLK0)	V_{IL}	0.1	—	V_{CC}	V	—
Input Low Voltage (CLK1, /CLK1)		0.2	—	—	V	Note 2
		0	—	—	V	Note 3
Input Voltage Swing (CLK0, /CLK0)	V_{IN}	0.1	—	V_{CC}	V	See Figure 8-1
Input Voltage Swing (CLK1, /CLK1)		0.2	—	—	V	See Figure 8-1
Differential Input Voltage Swing |CLK0-to-/CLK0|	V_{DIFF_IN}	0.2	—	—	V	See Figure 8-2
Differential Input Voltage Swing |CLK1-to-/CLK1|		0.4	—	—	V	See Figure 8-2
CLK0-to-VT0 (CLK0, /CLK0)	V_{T0}	—	—	1.28	V	—
Output Reference Voltage	$V_{REF-AC0}$	V_{CC} – 1.3	V_{CC} – 1.2	V_{CC} – 1.1	V	—
	V_{BB1}	V_{CC} – 1.525	V_{CC} – 1.425	V_{CC} – 1.325	V	—

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

2: SE-TERM not connected.

3: Using single-ended TTL/CMOS input signals, SE-TERM connects to GND. See Figure 11-6.

TABLE 1-2: LVDS OUTPUTS DC ELECTRICAL CHARACTERISTICS

V_{CC} = +2.5V ±5%; R_L = 100Ω across the outputs pair; and T_A = –40°C to +85°C, unless otherwise stated. (Note 1)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Output Voltage Swing (Q, /Q)	V_{OUT}	250	325	—	mV	See Figure 8-1
Differential Output Voltage Swing (Q, /Q)	$V_{DIFF-OUT}$	500	650	—	mV	See Figure 8-2
Output Common Mode Voltage	V_{OCM}	1.125	—	1.275	V	—
Change in V_{OS} between complementary output states	ΔV_{OS}	—	—	25	mV	—

Note 1: The circuit is designed to meet the DC specifications, shown in the above table, after thermal equilibrium has been established.

TABLE 1-3: LVTTL/CMOS DC ELECTRICAL CHARACTERISTICS

V_{CC} = +2.5V ±5%; T_A = –40°C to +85°C, unless otherwise stated. (Note 1)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Input HIGH Voltage	V_{IH}	2.0	—	—	V	—
Input LOW Voltage	V_{IL}	—	—	0.8	V	—
Input HIGH Current	I_{IH}	–125	—	30	µA	—
Input LOW Current	I_{IL}	–300	—	—	µA	—

Note 1: The circuit is designed to meet the DC specifications, shown in the above table, after thermal equilibrium has been established.

TABLE 1-4: AC ELECTRICAL CHARACTERISTICS

V_{CC} = +2.5V ±5%; R_L = 100Ω across the outputs; and T_A = –40°C to +85°C, unless otherwise stated. (Note 1)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Maximum Operating Frequency	f_{MAX}	1	—	—	GHz	V_{OUT} ≥ 200 mV
Propagation Delay, CLK0-to-Q	t_{PD}	625	750	975	ps	V_{IN} ≥ 100 mV
Propagation Delay, CLK1-to-Q		700	900	1200	ps	V_{IN} ≥ 200 mV
Propagation Delay, CLK_SEL-to-Q		500	700	900	ps	—
Differential Propagation Delay Temperature	t_{PD} Tempco	—	90	—	fs/°C	—
Set-up Time, EN-to-CLK0	t_S	100	—	—	ps	Note 2
Set-up Time, EN-to-CLK1		0	—	—	ps	Note 2
Hold Time, CLK0-to-EN	t_H	500	—	—	ps	Note 2
Hold Time, CLK1-to-EN		600	—	—	ps	Note 2
Output-to-output Skew	t_{SKEW}	—	—	25	ps	Note 3
Part-to-part Skew CLK0		—	—	200	ps	Note 4
Part-to-part Skew CLK1		—	—	250	ps	Note 4
RMS Phase Jitter		—	130	—	fs	Output = 622 MHz, Integration Range 12 kHz – 20 MHz (Note 5)
Adjacent Channel Crosstalk-induced Jitter		—	—	0.7	ps_{RMS}	
Output Rise/Fall Time (20% to 80%)	t_r, t_f	80	150	250	ps	At full output swing

Note 1: High-frequency AC-parameters are guaranteed by design and characterization.

2: Set-up and hold times apply to synchronous applications that intend to enable/disable before the next clock cycle. For asynchronous applications, set-up and hold do not apply.

3: Output-to-output skew is measured between two different outputs under identical input transitions.

4: Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.

5: Crosstalk-induced jitter is defined as: the added jitter that results from signals applied to two adjacent channels. It is measured at the output while applying two similar, differential clock frequencies that are asynchronous with respect to each other at the inputs.

TABLE 1-5: TEMPERATURE SPECIFICATIONS

Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Range						
Operating Ambient Temperature	T_A	–40	—	+85	°C	—
Lead Temperature	T_{LEAD}	—	+260	—	°C	Soldering, 20 sec.
Storage Temperature	T_S	–65	—	+150	°C	—
Package Thermal Resistance (Note 1)						
VQFN, Still Air	θ_{JA}	—	+24	—	°C/W	—
VQFN, Junction-to-Board	ψ_{JB}	—	+8	—	°C/W	—

Note 1: Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. ψ_{JB} and θ_{JA} values are determined for a 4-layer board in still-air, unless otherwise stated.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1, 6, 11, 22, 34	GND, Exposed Pad	**Ground:** GND pins and exposed pad must both be connected to the most negative potential of chip the ground.
2, 5	CLK0, /CLK0	**Differential Inputs:** This input pair is a differential signal input to the device. Input accepts AC- or DC-coupled signals as small as 100 mV (200 mV_{PP}). Each pin of the pair internally terminates to a VT pin through 50Ω. Note that this input defaults to an indeterminate state if left open. Please refer to Section 10.0, CLK0 Input Interface Applications for more details.
3	VT0	**Input Termination Center-Tap:** Each side of the differential input pair CLK0, /CLK0 terminates to the VT pin. The VT pin provides a center-tap to a termination network for maximum interface flexibility. See Section 10.0, CLK0 Input Interface Applications for more details. For DC-coupled CML or LVDS inputs, the VT pin is left floating.
4	VREF-AC0	**Reference Voltage:** This output biases to VCC–1.2V. It is used when AC-coupling the input CLK0. For AC-coupled applications, connect VREF-AC0 to the VT0 pin and bypass with 0.01 µF low ESR capacitor to VCC. See Section 10.0, CLK0 Input Interface Applications for more details. Maximum sink/source current is ±1.5mA. Due to the limited drive capability, the VREF-AC0 pin is only intended to drive its respective input pin.
7	SE-TERM	**Input Termination Pin:** When CLK1 is driven by a single-ended TTL/CMOS signal, tie this pin to GND. In all other modes, let this pin float. See Section 11.0, CLK1 Input Interface Applications for more details.
8, 10	CLK1, /CLK1	**Differential Inputs:** This input pair is a differential signal input to the device. This input accepts Any-Logic standard as small as 200 mV (400 mV_{PP}). Note that this input defaults to an indeterminate state if left open. Tie either the true or the complement input to ground while the other input is floating. This input can be used for single-ended signals (including TTL/CMOS signals from a 3.3V driver). See Section 11.0, CLK1 Input Interface Applications for more details.
9	VBB1	**Reference Voltage:** This output biases to VCC–1.425V. VBB1 is designed to act as a switching reference for the CLK1 and /CLK1 inputs when configured in single-ended PECL input mode. VBB1 can be used for AC-coupling of CLK1, see Figure 11-4 for details. Maximum sink/source current is ±1.5mA. Due to the limited drive capability, the VBB1 pin is only intended to drive its respective input pin.
12	EN	**Synchronous Output Enable:** This single-ended, TTL/CMOS-compatible input functions as a synchronous output enable. The synchronous enable ensures that enable/disable will only occur when the outputs are in a logic LOW state. Note that this input is internally connected to a 25 kΩ pull-up resistor and will default to logic HIGH state (enable) if left open.
13, 23, 28, 33, 43	VCC	**Positive Power Supply:** Bypass with 0.1 µF || 0.01 µF low ESR capacitors and place as close to the VCC pins as possible.
44	CLK_SEL	**Multiplexer Inputs Selector:** This single-ended, TTL/CMOS-compatible input selects the inputs to the multiplexer. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to logic HIGH state if open.

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
42, 41 40, 39 38, 37 36, 35 32, 31 30, 29 27, 26 25, 24 21, 20 19, 18 17, 16 15, 14	Q0, /Q0 Q1, /Q1 Q2, /Q2 Q3, /Q3 Q4, /Q4 Q5, /Q5 Q6, /Q6 Q7, /Q7 Q8, /Q8 Q9, /Q9 Q10, /Q10 Q11, /Q11	**Differential LVDS Outputs:** These LVDS output pairs are the precision, low skew copies of the selected input. Please refer to Table 2-2 below for details. Unused output pairs should be terminated with 100Ω across the pair. Each output is designed to drive 325 mV into 100Ω. See Section 6.0, LVDS Output Interface Applications for more details.

TABLE 2-2: TRUTH TABLE

EN	CLK_SEL	Q	/Q
H	L	CLK0	/CLK0
H	H	CLK1	/CLK1
L	X	L (Note 1)	H (Note 1)

Note 1: Transition occurs on next negative transition of the non-inverted input.

3.0 TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 2.5V; GND = 0V; V_{IN} = 400 mV; R_L = 100Ω across the outputs; and T_A = 25°C, unless otherwise stated.

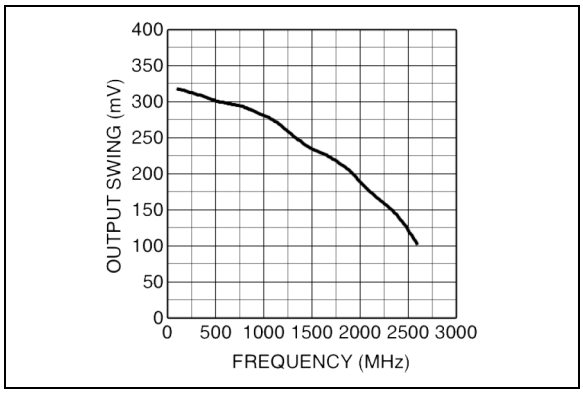


FIGURE 3-1: OUTPUT SWING VS. FREQUENCY.

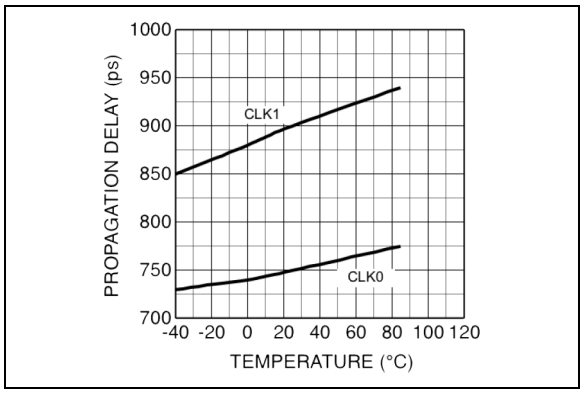


FIGURE 3-3: PROPAGATION DELAY VS. TEMPERATURE.

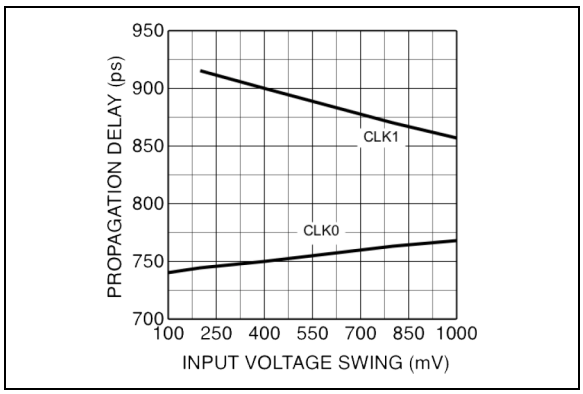


FIGURE 3-2: PROPAGATION DELAY VS. INPUT VOLTAGE SWING.

4.0 TYPICAL FUNCTIONAL CHARACTERISTICS

V_{CC} = 2.5V; GND = 0V; V_{IN} = 400 mV; R_L = 100Ω across the outputs; and T_A = 25°C, unless otherwise stated.

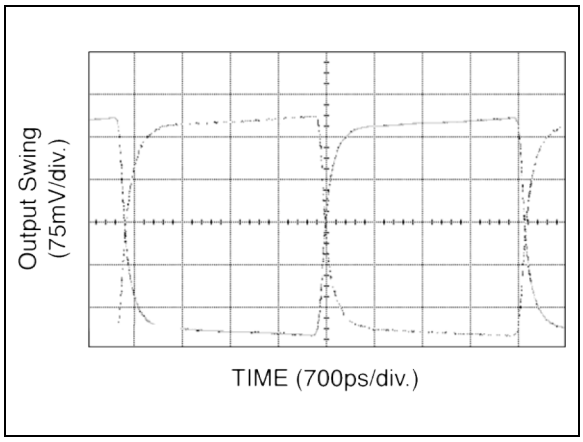


FIGURE 4-1: 200 MHZ OUTPUT.

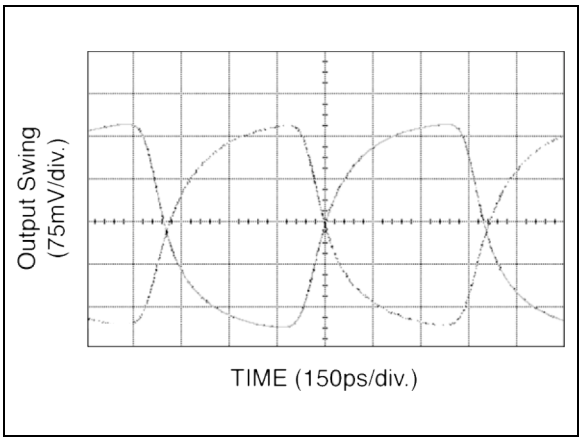


FIGURE 4-2: 1 GHZ OUTPUT.

5.0 SINGLE-ENDED TTL/CMOS RECOMMENDED RESISTOR VALUE

The SY89113U can be driven by a TTL/CMOS input signal. See Figure 11-6. The resistor R, in Table 5-1 below, is calculated according to the following equation:

EQUATION 5-1:

$$R = 1.594 \times \left(\frac{1}{\left[\frac{5.057 \times V_{CC}}{2 \times V_{CC} + V_{IH} + V_{IL}} \right] - 1} - 1 \right) \Omega$$

Equation 5-1 is used to determine the optimum value of R for best duty cycle.

TABLE 5-1: SINGLE-ENDED TTL/CMOS RECOMMENDED RESISTORS

input Signal	Recommended R (Ω)
1.8V CMOS	261
2.5V CMOS	732
3.3V CMOS	1470

6.0 LVDS OUTPUT INTERFACE APPLICATIONS

LVDS specifies a small swing of 325 mV typical on a nominal 1.2V common mode above ground. The common mode voltage has tight limits to permit large variations in ground between an LVDS driver and receiver. Also, change in common mode voltage, as a function of data input, is kept to a minimum to keep EMI low.

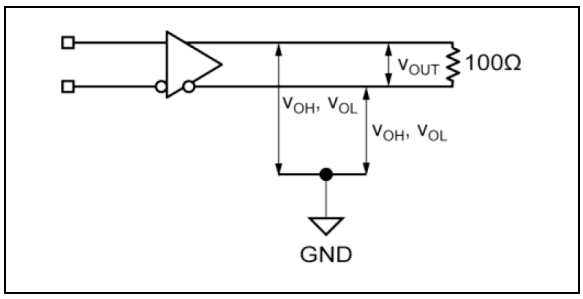


FIGURE 6-1: LVDS DIFFERENTIAL MEASUREMENT.

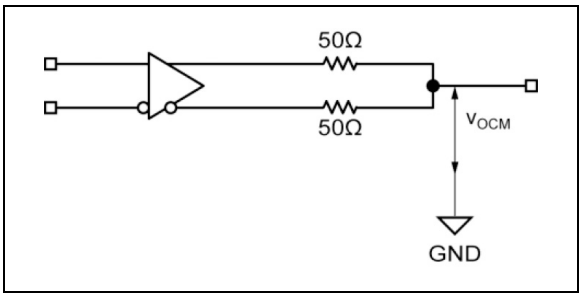


FIGURE 6-2: LVDS COMMON MODE MEASUREMENT.

7.0 TIMING DIAGRAMS

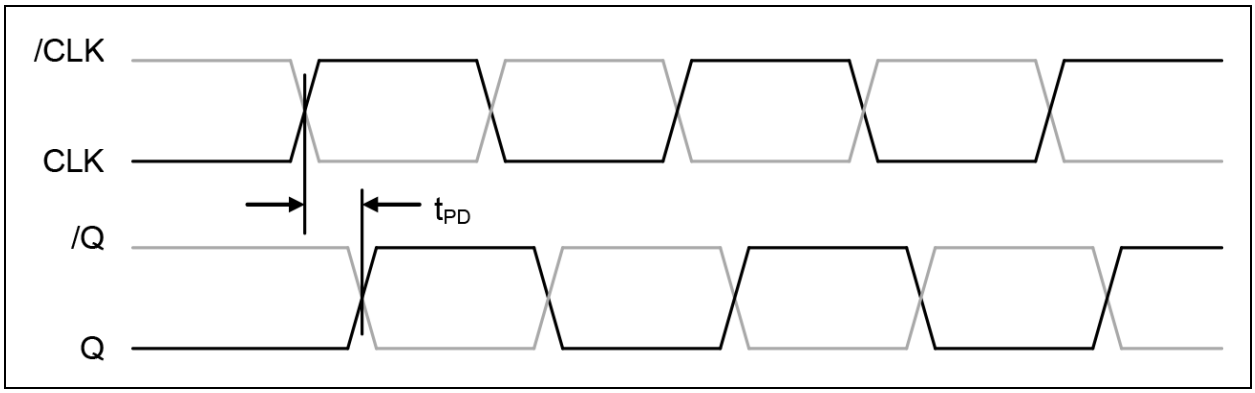


FIGURE 7-1: TIMING DIAGRAM: DIFFERENTIAL IN-TO-DIFFERENTIAL OUT.

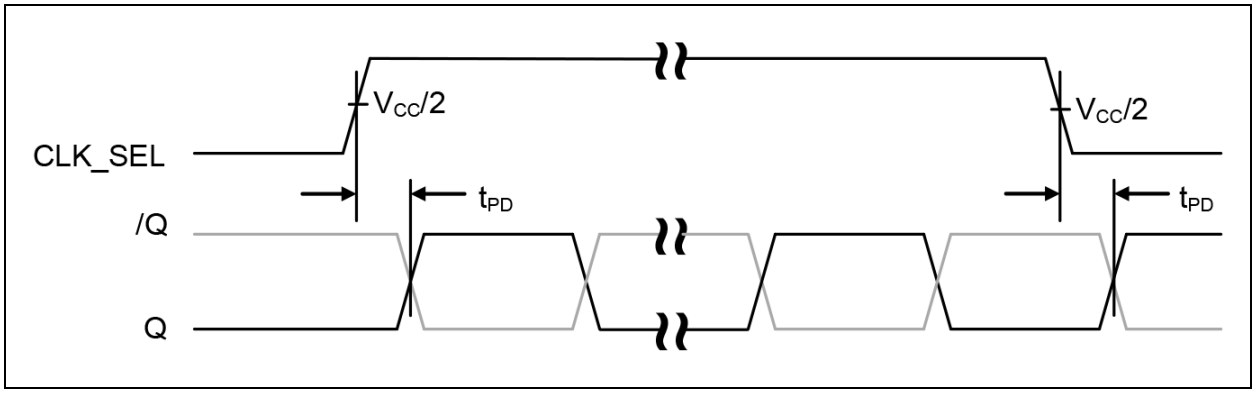


FIGURE 7-2: TIMING DIAGRAM: CLK_SEL-TO-DIFFERENTIAL OUT.

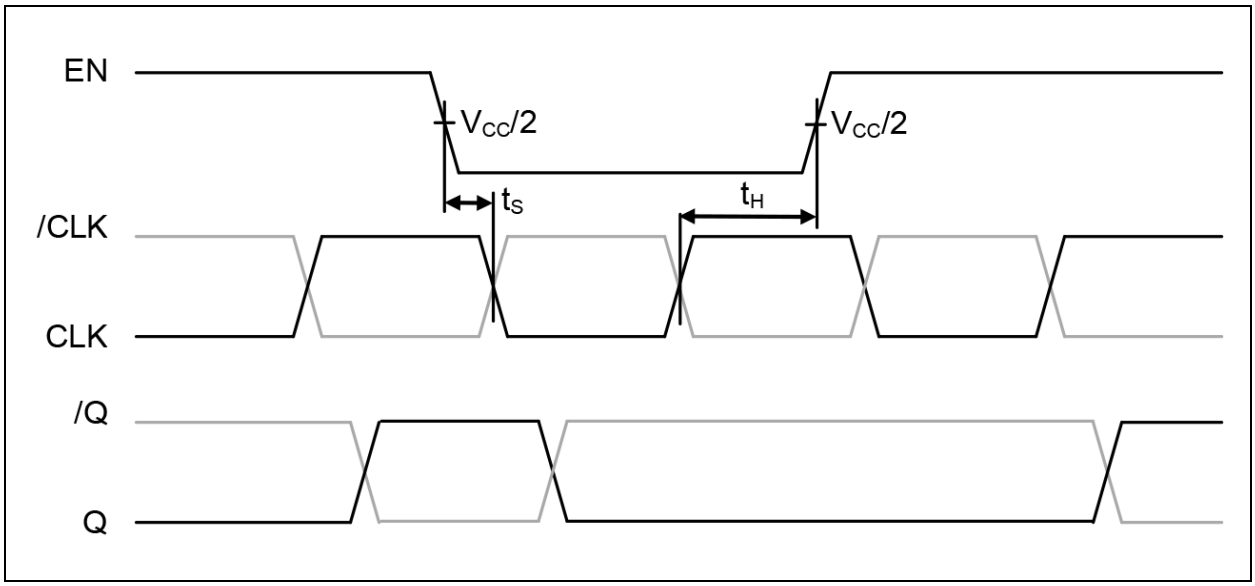


FIGURE 7-3: TIMING DIAGRAM: SETUP AND HOLD TIME EN-TO-DIFFERENTIAL IN.

8.0 SINGLE-ENDED AND DIFFERENTIAL SWINGS

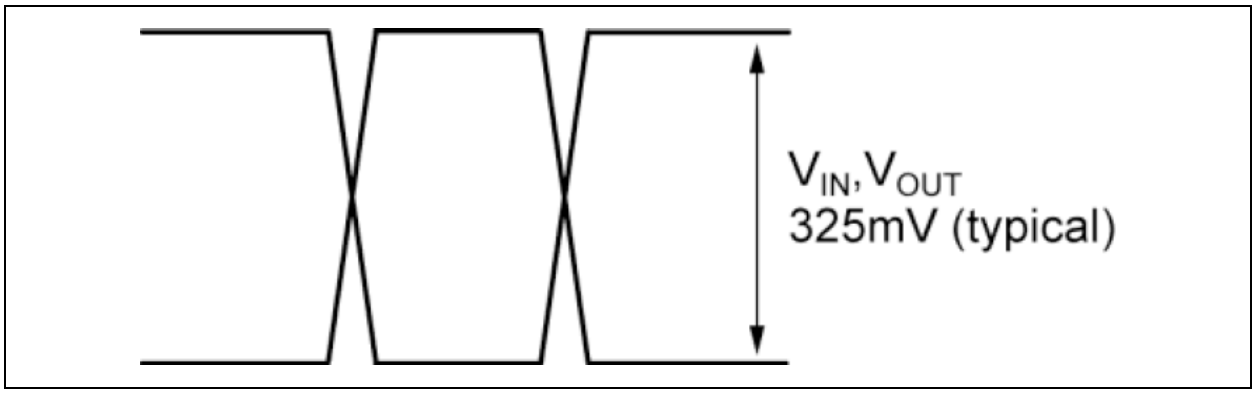


FIGURE 8-1: SINGLE-ENDED VOLTAGE SWING CLK0.

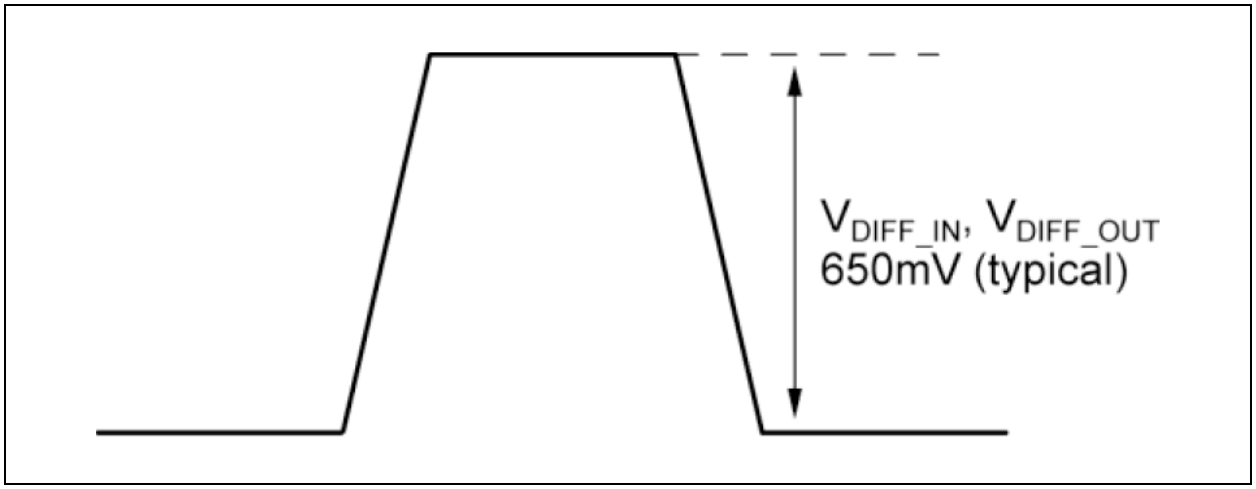


FIGURE 8-2: DIFFERENTIAL VOLTAGE SWING CLK0.

9.0 INPUT AND OUTPUT STAGES

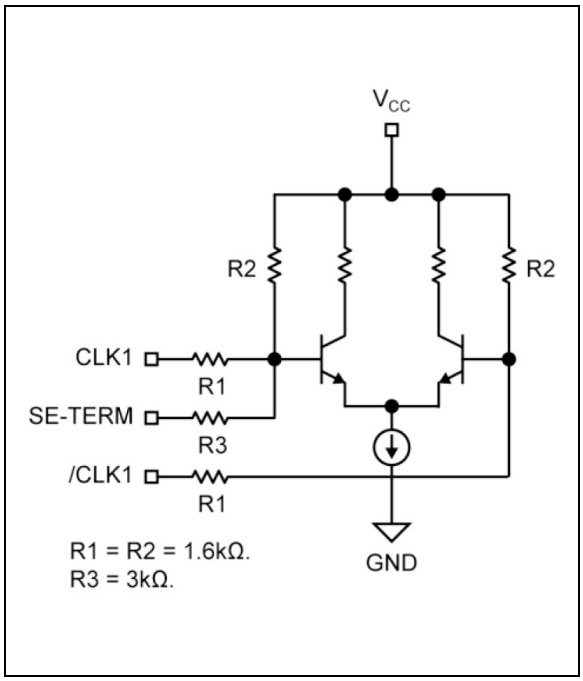


FIGURE 9-1: CLK1 DIFFERENTIAL INPUT BUFFER.

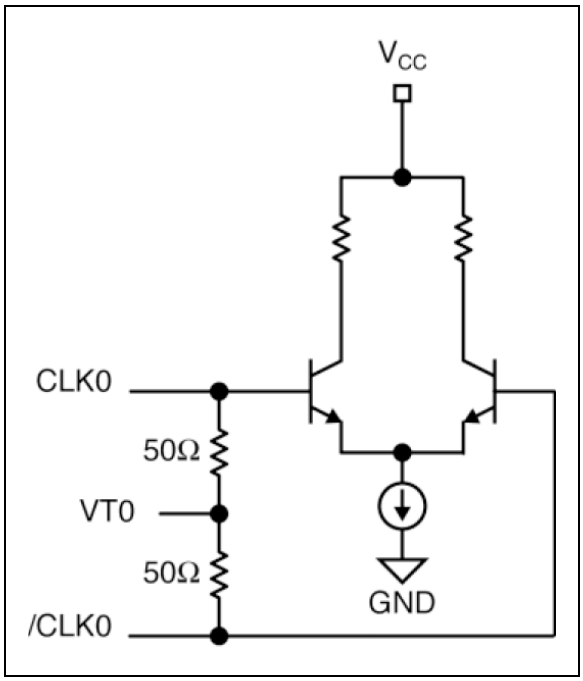


FIGURE 9-2: CLK0 DIFFERENTIAL INPUT STRUCTURE.

10.0 CLK0 INPUT INTERFACE APPLICATIONS

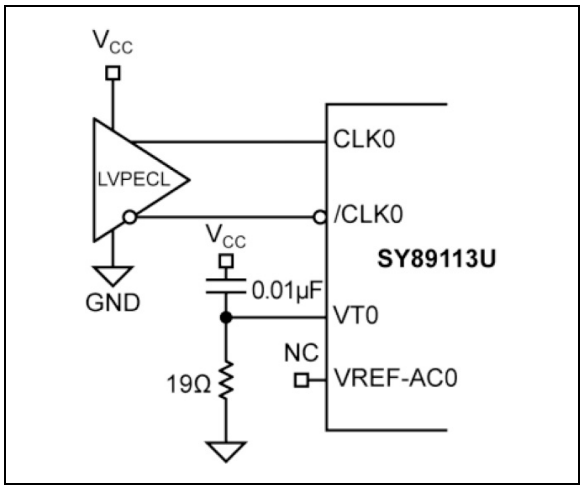


FIGURE 10-1: DC-COUPLED LVPECL INPUT INTERFACE.

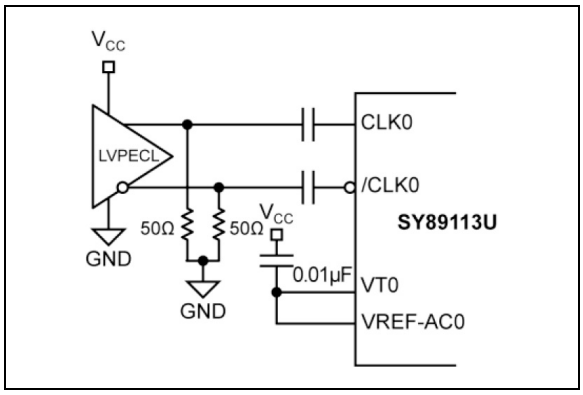


FIGURE 10-2: AC-COUPLED LVPECL INPUT INTERFACE.

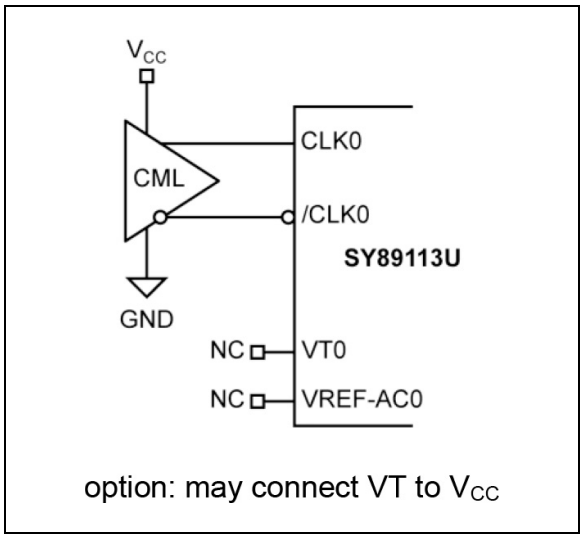


FIGURE 10-3: DC-COUPLED CML INPUT INTERFACE.

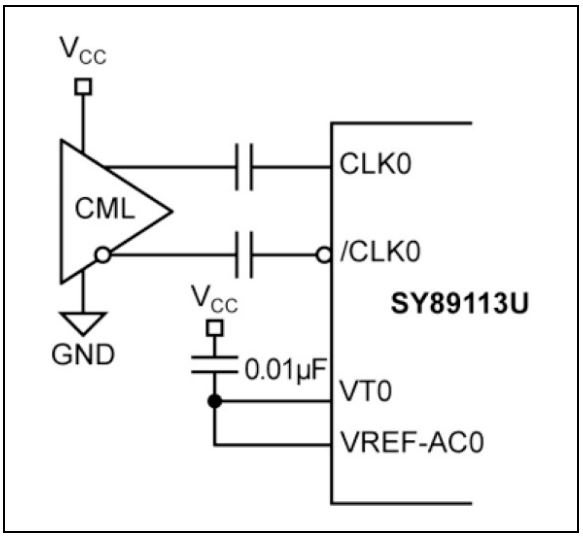


FIGURE 10-4: AC-COUPLED CML INPUT INTERFACE.

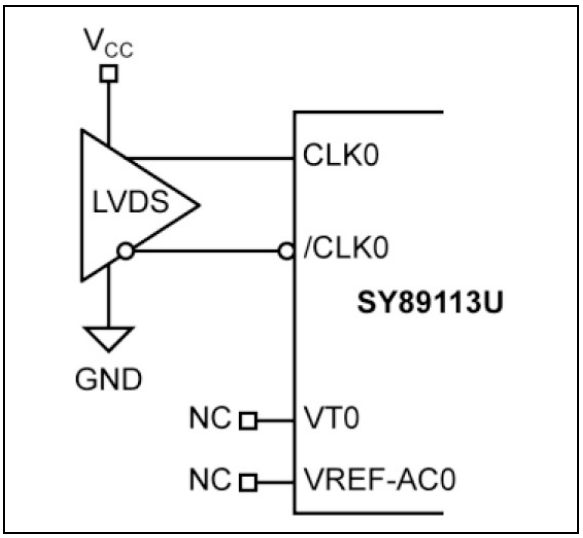


FIGURE 10-5: DC-COUPLED LVDS INPUT INTERFACE.

11.0 CLK1 INPUT INTERFACE APPLICATIONS

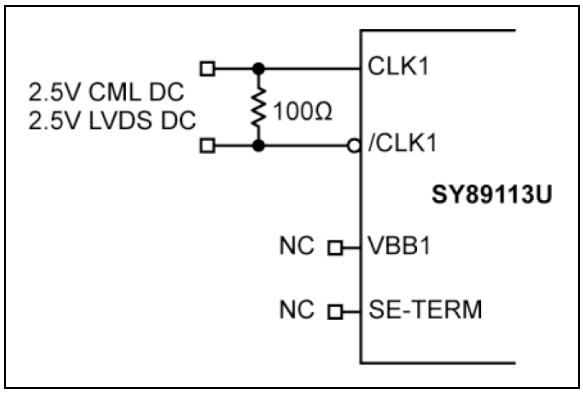


FIGURE 11-1: DC-COUPLED CML, LVDS INPUT INTERFACE.

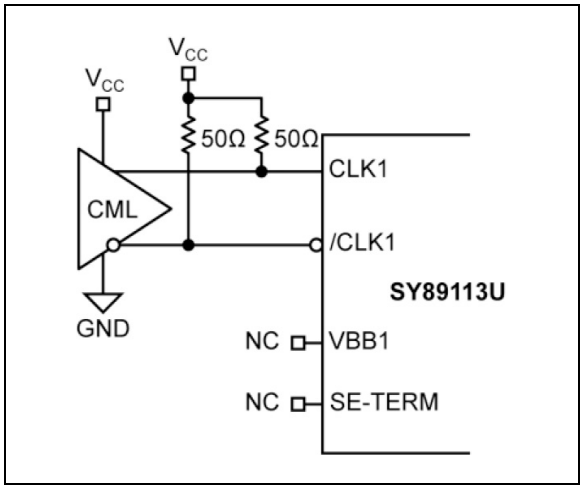


FIGURE 11-2: DC-COUPLED CML INPUT INTERFACE.

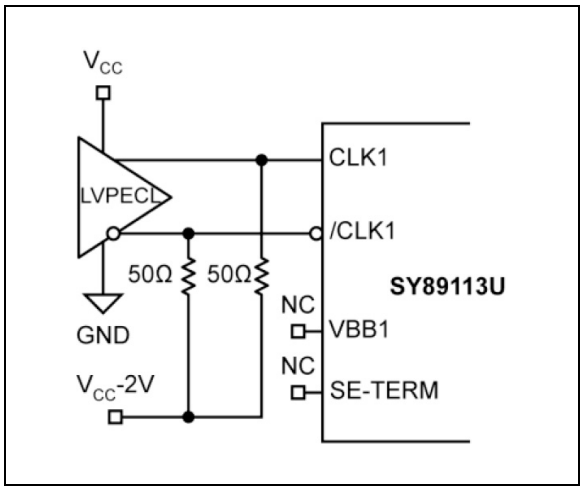


FIGURE 11-3: DC-COUPLED PECL INPUT INTERFACE.

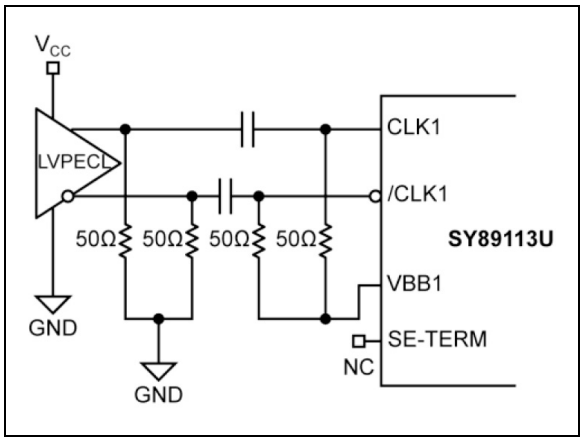


FIGURE 11-4: AC-COUPLED PECL INPUT INTERFACE.

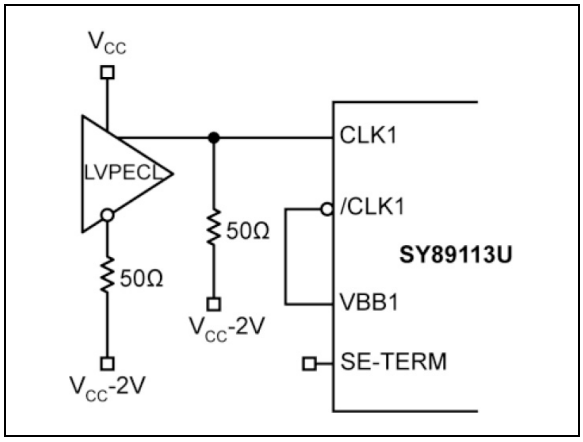


FIGURE 11-5: SINGLE-ENDED PECL INPUT INTERFACE.

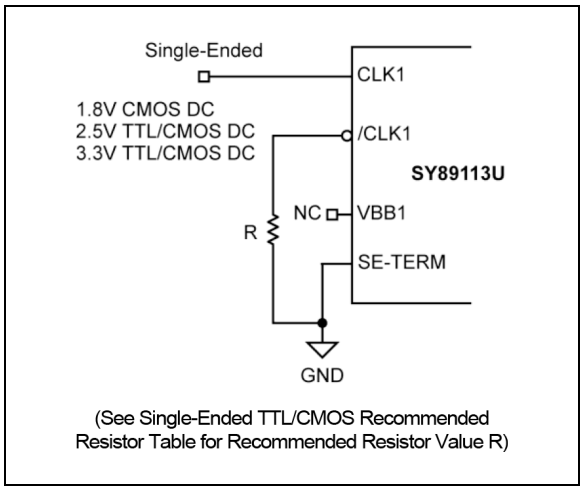
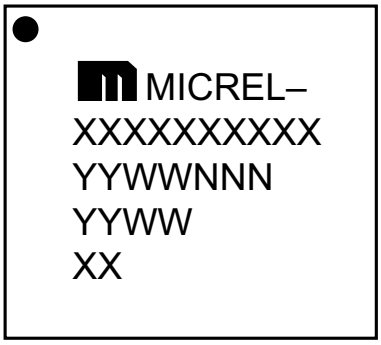


FIGURE 11-6: SINGLE-ENDED TTL/CMOS INPUT INTERFACE.

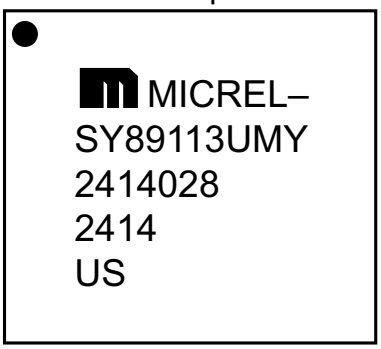
12.0 PACKAGING INFORMATION

12.1 Package Marking Information

44-Lead VQFN*



Example*



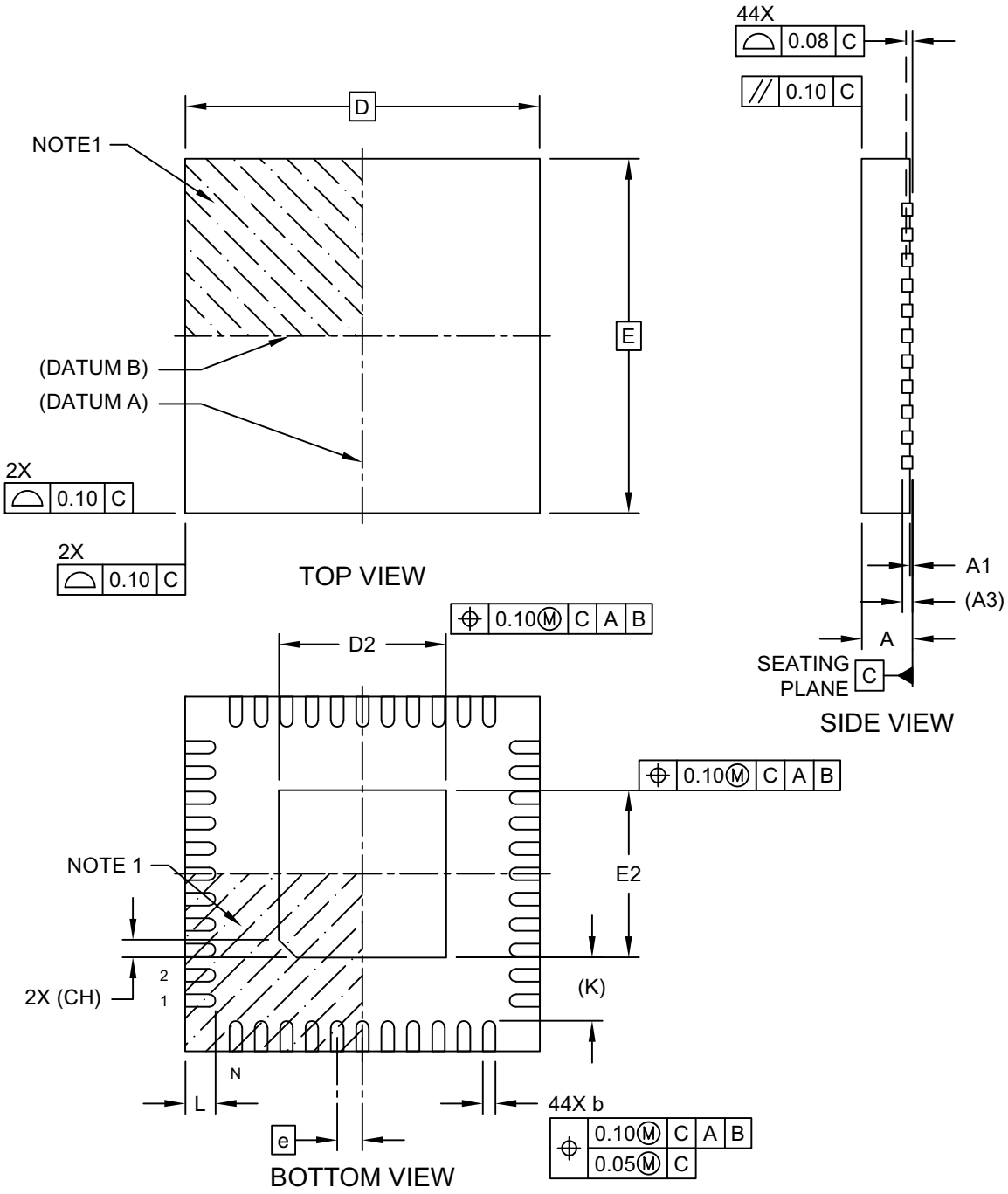
Legend:	XX...X	Product code or customer-specific information
	W	Week code
	NNN	Alphanumeric traceability code (week)
	*	This package is Pb-free. The Pb-free JEDEC designator can be found on the outer packaging for this package.
	●	Pin one index is identified by a dot

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

44-Lead 7 mm × 7 mm VQFN [QPA] Package Outline and Recommended Land Pattern

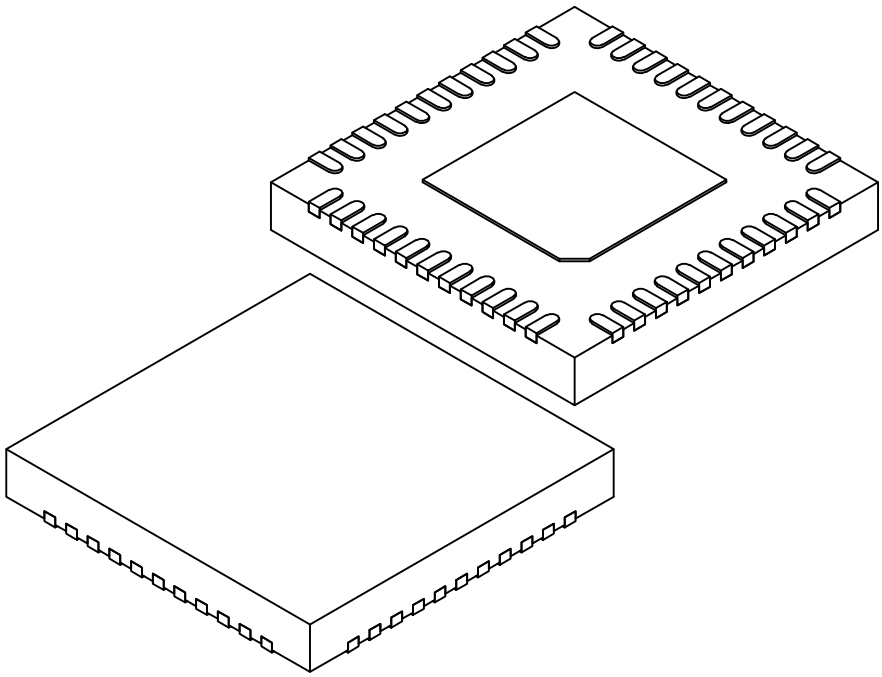
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1291 Rev A Sheet 1 of 2

44-Lead 7 mm × 7 mm VQFN [QPA] Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		44	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		7.00 BSC	
Exposed Pad Length	D2	3.20	3.30	3.40
Overall Width	E		7.00 BSC	
Exposed Pad Width	E2	3.20	3.30	3.40
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.50	0.60	0.70
Terminal-to-Exposed-Pad	K		0.20 REF	
Exposed Pad Corner Chamfer	CH		0.35 REF	

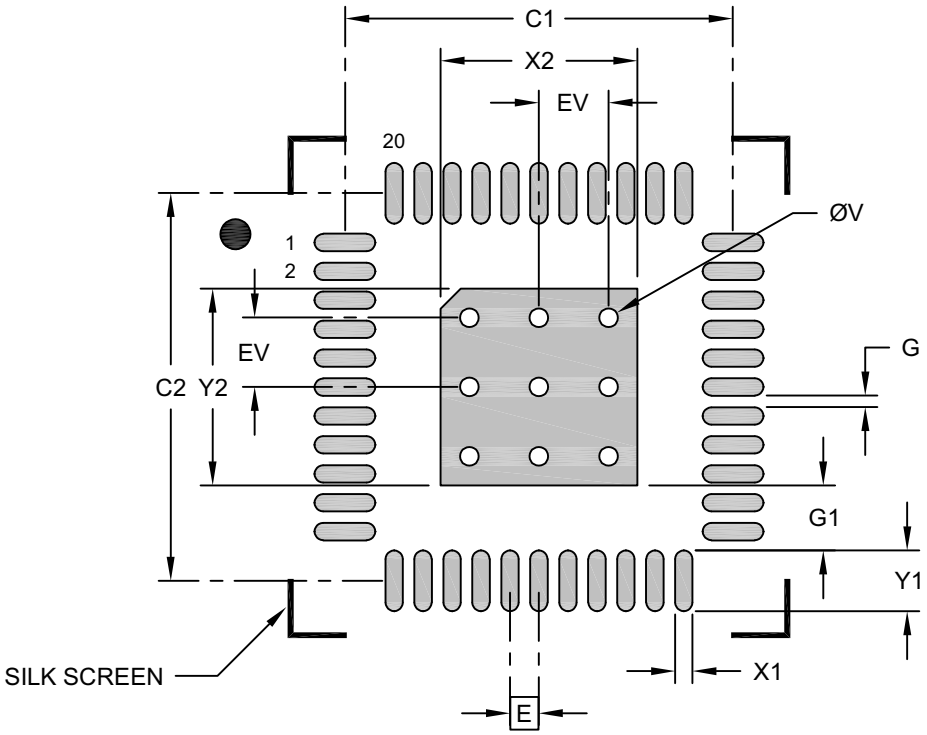
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1291 Rev A Sheet 2 of 2

44-Lead 7 mm × 7 mm VQFN [QPA] Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Center Pad Width	X2			3.40
Center Pad Length	Y2			3.40
Contact Pad Spacing	C1		6.70	
Contact Pad Spacing	C2		6.70	
Contact Pad Width (Xnn)	X1			0.30
Contact Pad Length (Xnn)	Y1			1.05
Contact Pad to Center Pad (Xnn)	G1	1.13		
Contact Pad to Contact Pad (Xnn)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3291 Rev A

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (February 2024)

- Converted Micrel data sheet for SY89113U to Microchip format as DS20006881A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	X	-XX
Device	Supply Voltage Range	Package	Temperature Range	Special Processing

Device:	SY89113	=	2.5V Low Jitter, Low Skew 1:12 LVDS Fanout Buffer with 2:1 Input MUX and Internal Termination
Voltage Option:	U	=	2.5V
Package:	M	=	44-Lead VQFN
Temperature Range:	Y	=	–40°C to 85°C
Special Processing:	<blank>	=	260/Tray
	TR	=	1,000/Reel

Examples:

a) **SY89113UMY**

2.5V, 44-Lead VQFN, –40°C to 85°C, 260/Tray

b) **SY89113UMY-TR**

2.5V, 44-Lead VQFN, –40°C to 85°C, 1,000/Reel

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