

MOSFET

OptiMOS™ Power-Transistor, -100 V

Features

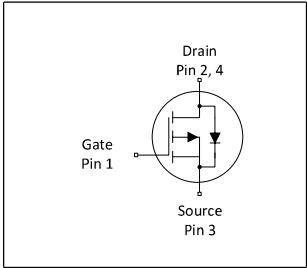
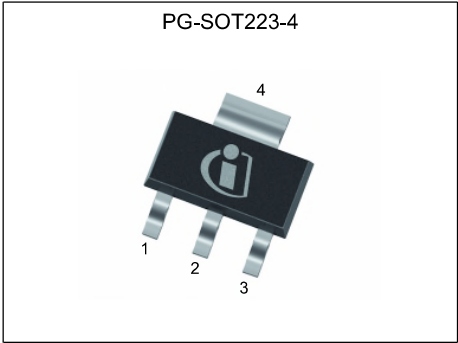
- P-channel
- Very low on-resistance $R_{DS(on)}$ @ $V_{GS}= 4.5\text{ V}$
- Logic level
- 100% avalanche tested
- Enhancement mode
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	-100	V
$R_{DS(on),max}$	980	mΩ
I_D	-1.55	A
Q_{oss}	-2.3	nC
Q_G	-3.6	nC



RoHS

Type / Ordering Code	Package	Marking	Related Links
ISP98DP10LM	PG-SOT223-4	98DP10LM	-

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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	-1.55 -0.98 -0.95 -0.93	A	$V_{GS}=-10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=-10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=-4.5\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=-10\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=70\text{ °C/W}^{2)}$
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	-6.2	A	$T_A=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	45	mJ	$I_D=-0.9\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	5.0 1.8	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{thJA}=70\text{ °C/W}^{2)}$
Operating and storage temperature	T_j , T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	25	°C/W	-
Thermal resistance, junction - ambient, 6 cm ² cooling area	R_{thJA}	-	-	70	°C/W	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	-100	-	-	V	$V_{GS}=0\text{ V}$, $I_D=-1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	-1.0	-1.5	-2.0	V	$V_{DS}=V_{GS}$, $I_D=-165\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	-0.1 -10	-1.0 -100	μA	$V_{DS}=-100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=-100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	-10	-100	nA	$V_{GS}=-20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	802.1 845.8	980 1050	m Ω	$V_{GS}=-10\text{ V}$, $I_D=-0.9\text{ A}$ $V_{GS}=-4.5\text{ V}$, $I_D=-0.7\text{ A}$
Gate resistance	R_G	-	4.4	-	Ω	-
Transconductance	g_{fs}	-	2.5	-	S	$ V_{DS} \geq 2 I_D /R_{DS(on)max}$, $I_D=-0.9\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance ¹⁾	C_{iss}	-	270	350	pF	$V_{GS}=0\text{ V}$, $V_{DS}=-50\text{ V}$, $f=1\text{ MHz}$
Output capacitance ¹⁾	C_{oss}	-	20	26	pF	$V_{GS}=0\text{ V}$, $V_{DS}=-50\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance ¹⁾	C_{rss}	-	6	10	pF	$V_{GS}=0\text{ V}$, $V_{DS}=-50\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	9.98	-	ns	$V_{DD}=-50\text{ V}$, $V_{GS}=-10\text{ V}$, $I_D=-0.9\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	6.24	-	ns	$V_{DD}=-50\text{ V}$, $V_{GS}=-10\text{ V}$, $I_D=-0.9\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	14.01	-	ns	$V_{DD}=-50\text{ V}$, $V_{GS}=-10\text{ V}$, $I_D=-0.9\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Fall time	t_f	-	8.18	-	ns	$V_{DD}=-50\text{ V}$, $V_{GS}=-10\text{ V}$, $I_D=-0.9\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$

¹⁾ Defined by design. Not subject to production test.

Table 6 Gate charge characteristics¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	-0.8	-	nC	$V_{DD}=-50\text{ V}$, $I_D=-0.9\text{ A}$, $V_{GS}=0\text{ to }-4.5\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	-0.4	-	nC	$V_{DD}=-50\text{ V}$, $I_D=-0.9\text{ A}$, $V_{GS}=0\text{ to }-4.5\text{ V}$
Gate to drain charge ²⁾	Q_{gd}	-	-1.8	-2.7	nC	$V_{DD}=-50\text{ V}$, $I_D=-0.9\text{ A}$, $V_{GS}=0\text{ to }-4.5\text{ V}$
Switching charge	Q_{sw}	-	-2.1	-	nC	$V_{DD}=-50\text{ V}$, $I_D=-0.9\text{ A}$, $V_{GS}=0\text{ to }-4.5\text{ V}$
Gate charge total ²⁾	Q_g	-	-3.6	-4.5	nC	$V_{DD}=-50\text{ V}$, $I_D=-0.9\text{ A}$, $V_{GS}=0\text{ to }-4.5\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	-2.8	-	V	$V_{DD}=-50\text{ V}$, $I_D=-0.9\text{ A}$, $V_{GS}=0\text{ to }-4.5\text{ V}$
Gate charge total	Q_g	-	-7.2	-	nC	$V_{DD}=-50\text{ V}$, $I_D=-0.9\text{ A}$, $V_{GS}=0\text{ to }-10\text{ V}$
Output charge ²⁾	Q_{oss}	-	-2.3	-3.1	nC	$V_{DS}=-50\text{ V}$, $V_{GS}=0\text{ V}$

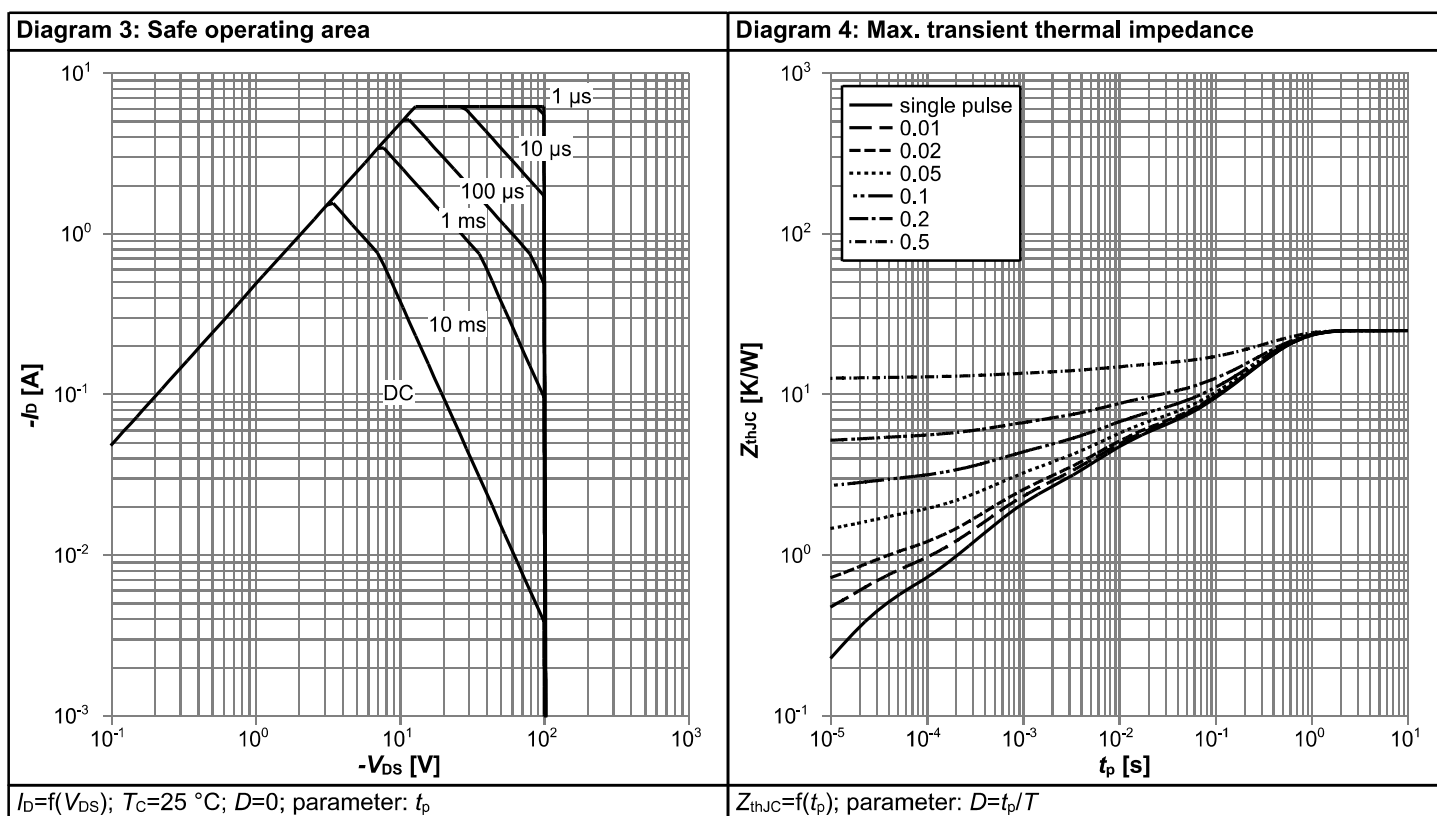
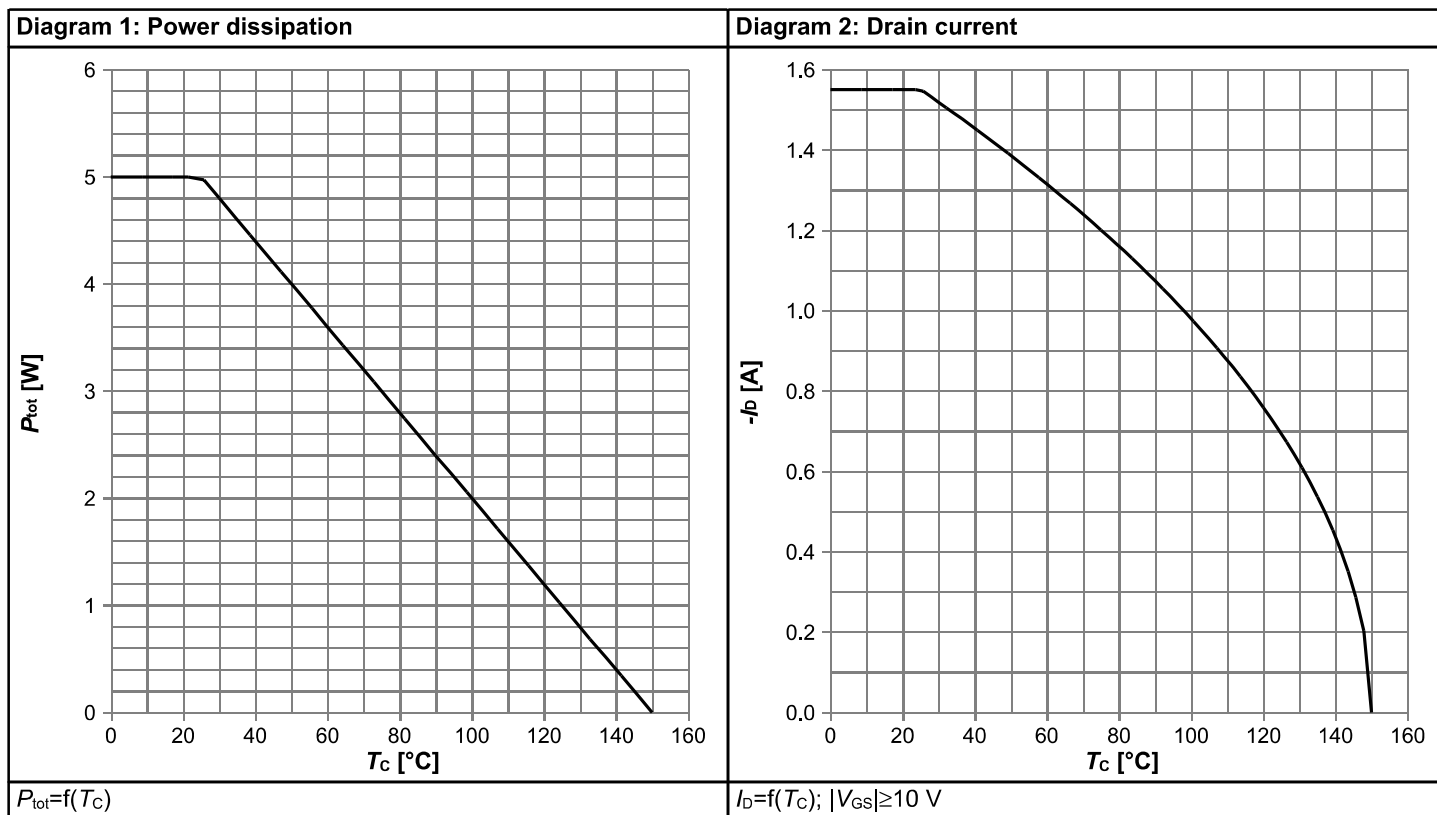
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	-1.55	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	-6.2	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	-0.81	-1.2	V	$V_{GS}=0\text{ V}$, $I_F=-0.9\text{ A}$, $T_j=25\text{ °C}$
Reverse recovery time ²⁾	t_{rr}	-	19.41	38.82	ns	$V_R=-50\text{ V}$, $I_F=-0.9\text{ A}$, $di_F/dt=-100\text{ A}/\mu\text{s}$
Reverse recovery charge ²⁾	Q_{rr}	-	21.71	43.42	nC	$V_R=-50\text{ V}$, $I_F=-0.9\text{ A}$, $di_F/dt=-100\text{ A}/\mu\text{s}$

¹⁾ See "Gate charge waveforms" for parameter definition

²⁾ Defined by design. Not subject to production test.

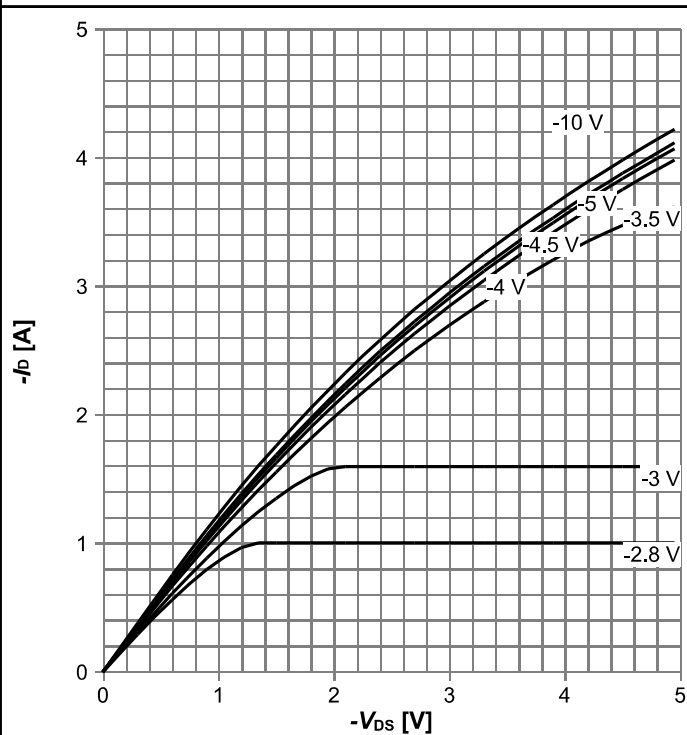
4 Electrical characteristics diagrams



OptiMOS™ Power-Transistor, -100 V

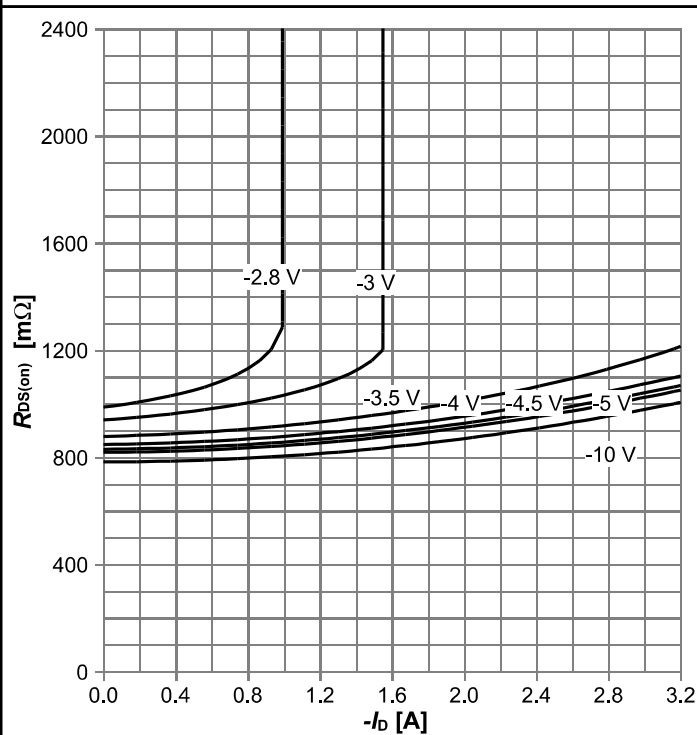
ISP98DP10LM

Diagram 5: Typ. output characteristics



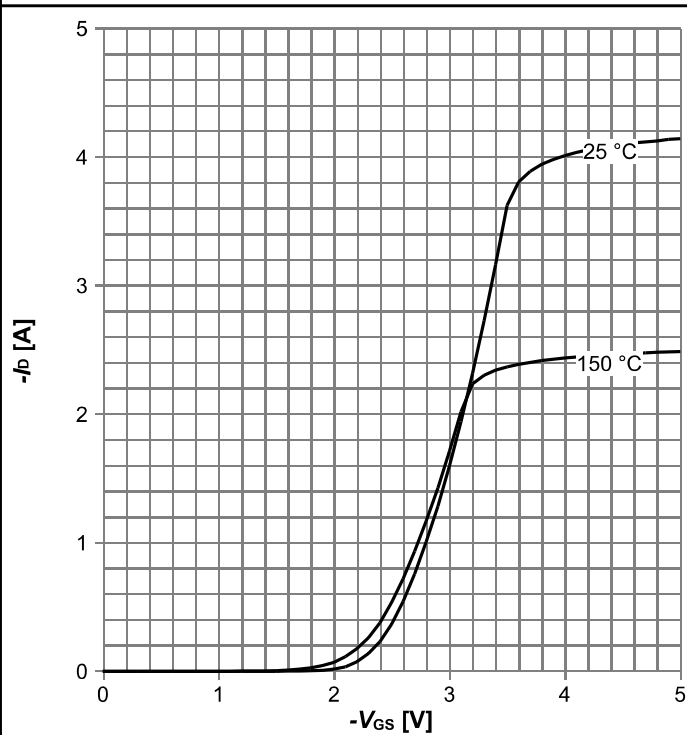
$I_D = f(V_{DS})$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



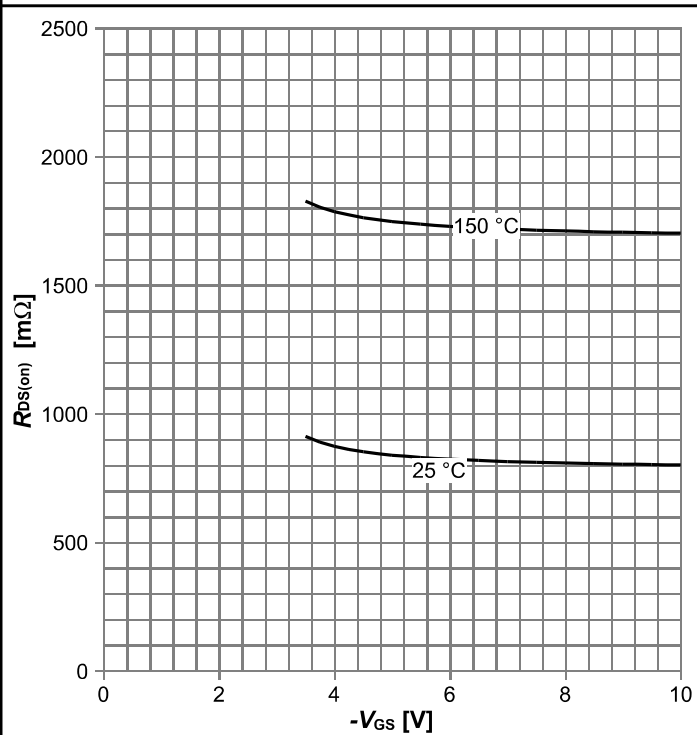
$R_{DS(on)} = f(I_D)$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



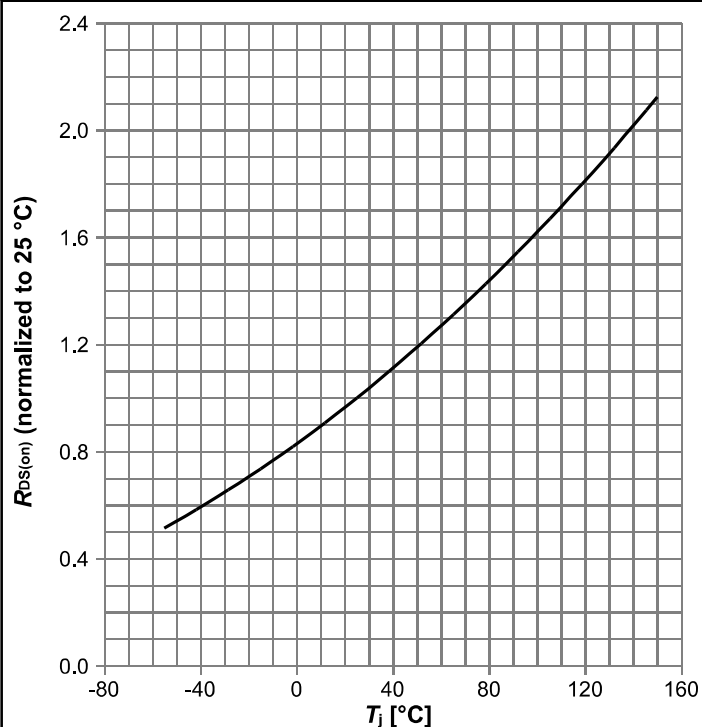
$I_D = f(V_{GS})$, $|V_{DS}| > 2|I_D|R_{DS(on)\max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



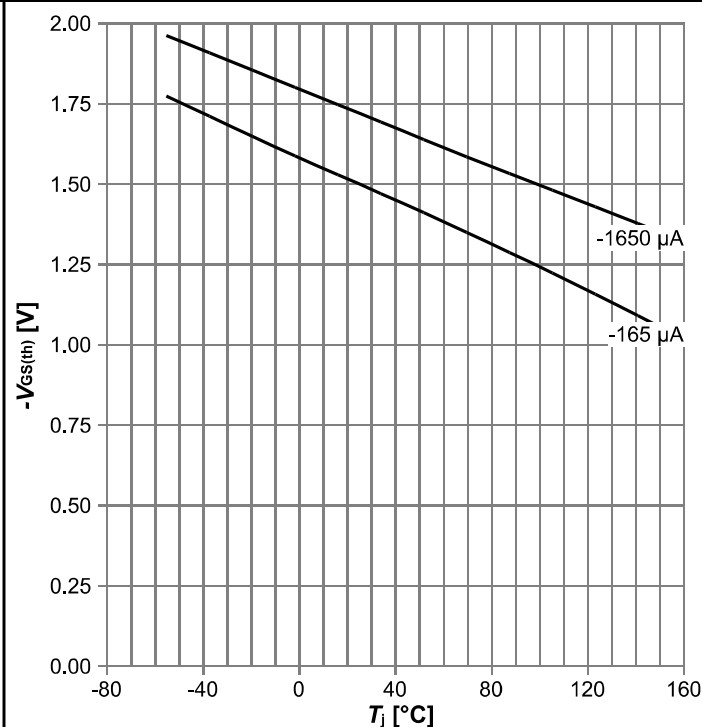
$R_{DS(on)} = f(V_{GS})$, $I_D = -0.9\text{ A}$; parameter: T_j

Diagram 9: Normalized drain-source on resistance



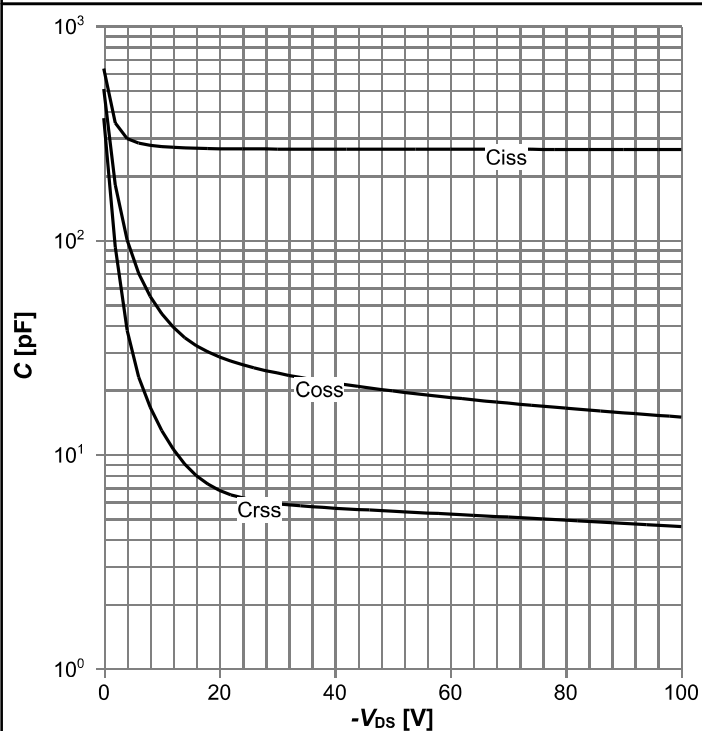
$R_{DS(on)}=f(T_j)$, $I_D=-0.9$ A, $V_{GS}=-10$ V

Diagram 10: Typ. gate threshold voltage



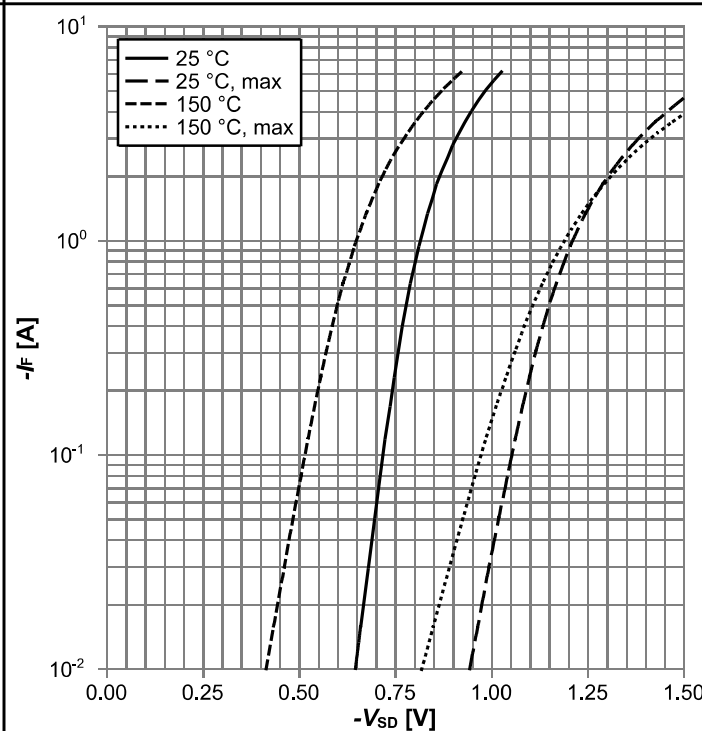
$V_{GS(th)}=f(T_j)$, $V_{GS}=V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



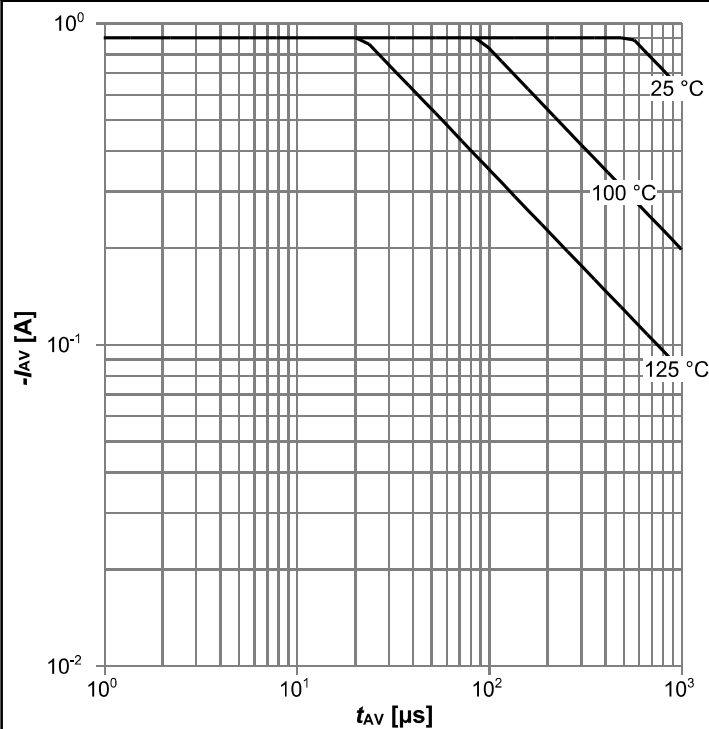
$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz

Diagram 12: Forward characteristics of reverse diode



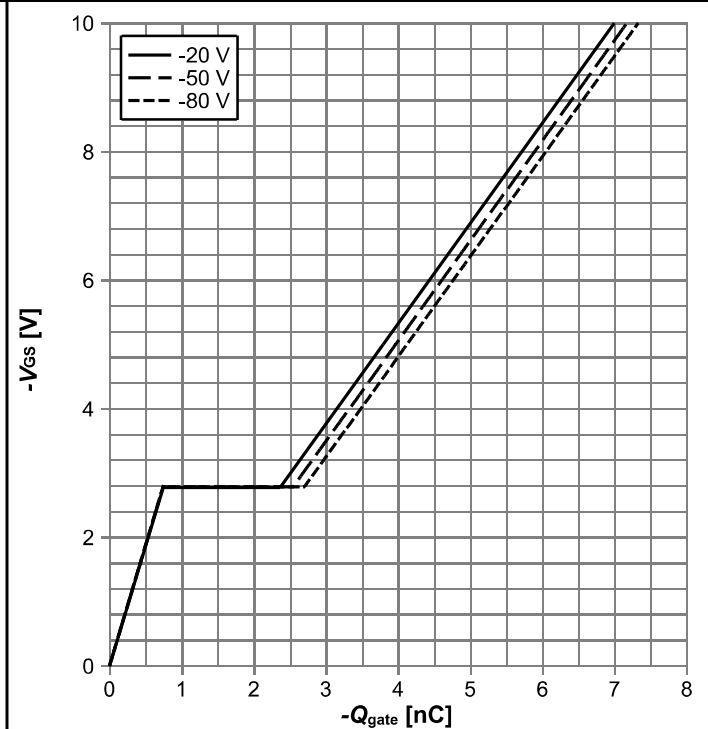
$I_F=f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



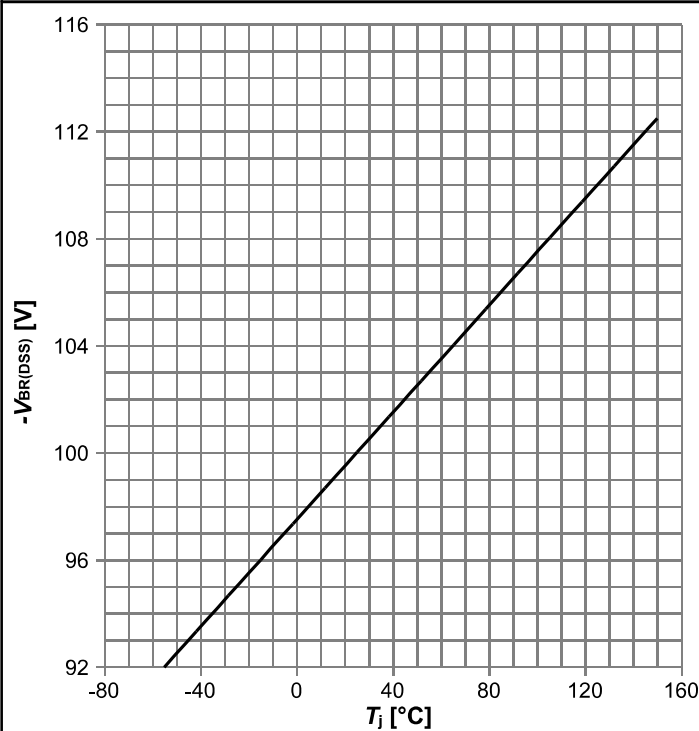
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



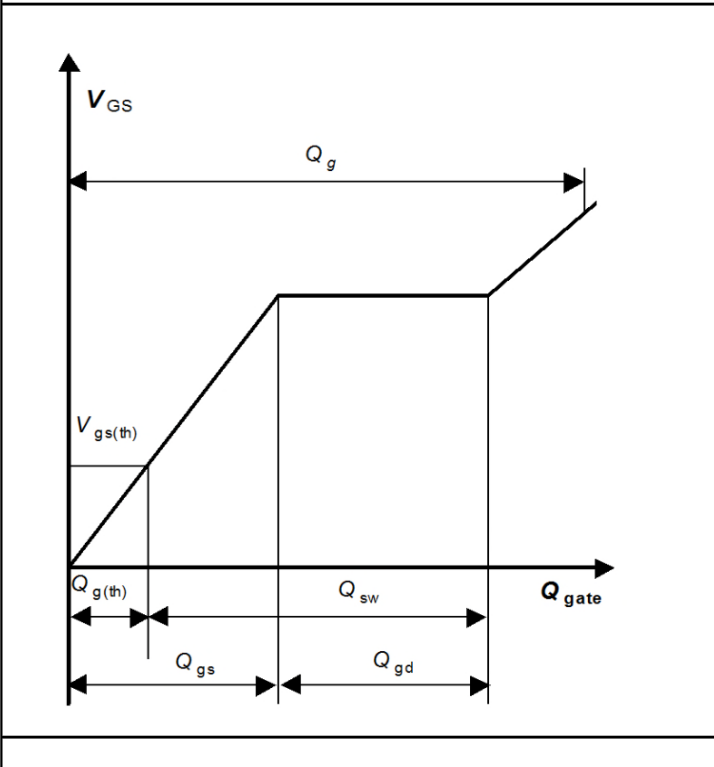
$V_{GS}=f(Q_{gate})$, $I_D=-0.9\text{ A}$ pulsed, $T_j=25\text{ °C}$; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

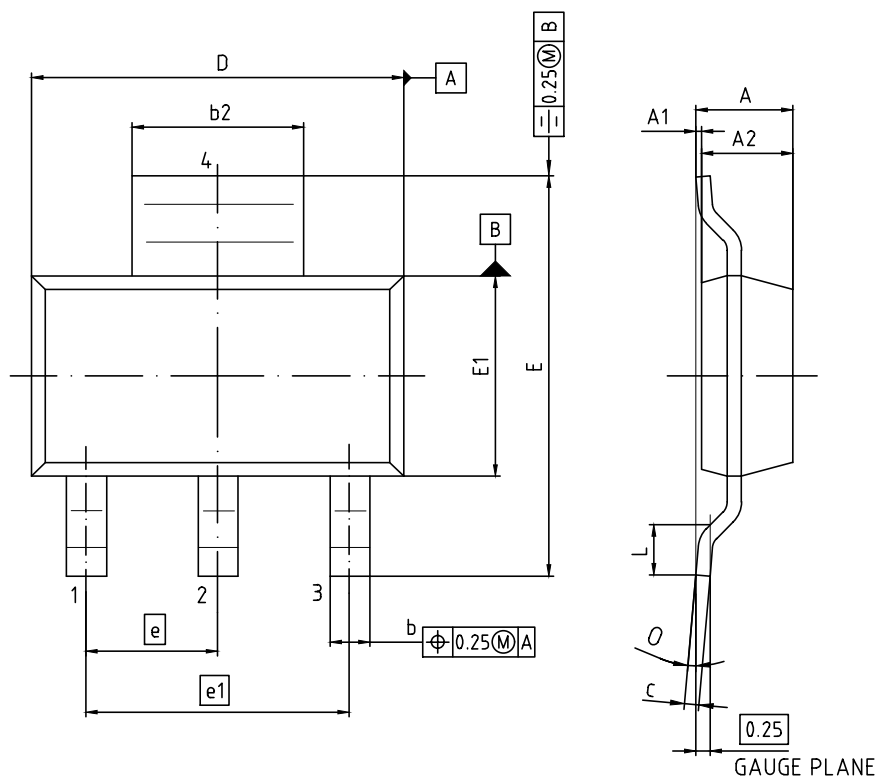


$V_{BR(DSS)}=f(T_j)$; $I_D=-1\text{ mA}$

Diagram Gate charge waveforms



5 Package Outlines



DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	1.60	1.80
A1	-	0.10
A2	1.50	1.70
b	0.60	0.80
b2	2.90	3.10
c	0.24	0.32
D	6.30	6.70
E	6.70	7.30
E1	3.30	3.70
e	2.30	
e1	4.60	
L	0.75	-
O	0°	10°

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Figure 1 Outline PG-SOT223-4, dimensions in mm

Revision History

ISP98DP10LM

Revision: 2021-05-10, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2021-05-10	Release of final version

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