# SY58606U

## 4.25 Gbps Precision, 1:2 CML Fanout Buffer with Internal Termination and Fail Safe Input

### Features

- Precision 1:2, 400 mV CML Fanout Buffer
- Guaranteed AC Performance over Temperature and Voltage:
  - DC-to >4.25 Gbps Throughput
  - <320 ps Propagation Delay (IN-to-Q)
  - <15 ps Within-Device Skew
  - <85 ps Rise/Fall Times
- Fail Safe Input
  - Prevents Outputs From Oscillating When Input is Invalid
- Ultra-Low Jitter Design
  - 100 $fs_{RMS}$ Typical Additive Jitter
- High-Speed CML Outputs
- 2.5V ±5% or 3.3V ±10% Power Supply Operation
- Industrial Temperature Range: –40°C to +85°C
- Available In 16-lead (3 mm x 3 mm) QFN Package

### Applications

- Data Distribution: OC-48, OC-48+FEC, XAUI
- SONET Clock and Data Distribution
- Fibre Channel Clock and Data Distribution
- Gigabit Ethernet Clock And Data Distribution

### Markets

- Storage
- ATE
- Test and Measurement
- Enterprise Networking Equipment
- High-End Servers
- Access
- Metro Area Network Equipment

United States Patent No. RE44,134

### General Description

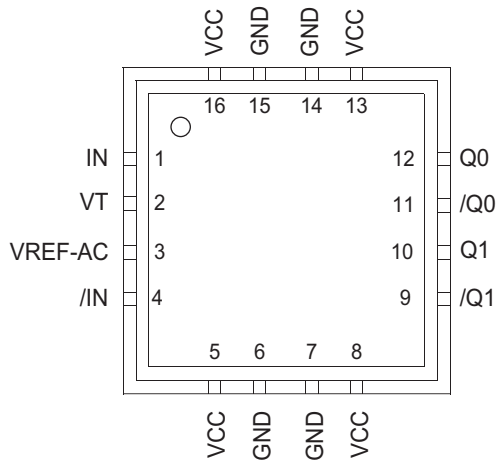
The SY58606U is a 2.5/3.3V, high-speed, fully differential 1:2 CML fanout buffer optimized to provide two identical output copies with less than 15 ps of skew and 100 $fs_{RMS}$ of typical additive phase jitter. The SY58606U can process clock signals as fast as 3 GHz or data patterns up to 4.25 Gbps.

The differential input includes Microchip's unique, 3-lead input termination architecture that interfaces to LVPECL, LVDS, or CML differential signals, (AC- or DC-coupled) as small as 100 mV (200 $mV_{PP}$) without any level-shifting or termination resistor networks in the signal path. For AC-coupled input interface applications, an integrated voltage reference ($V_{REF-AC}$) is provided to bias the $V_T$ pin. The outputs are 400 mV CML, with extremely fast rise/fall times guaranteed to be less than 85 ps.

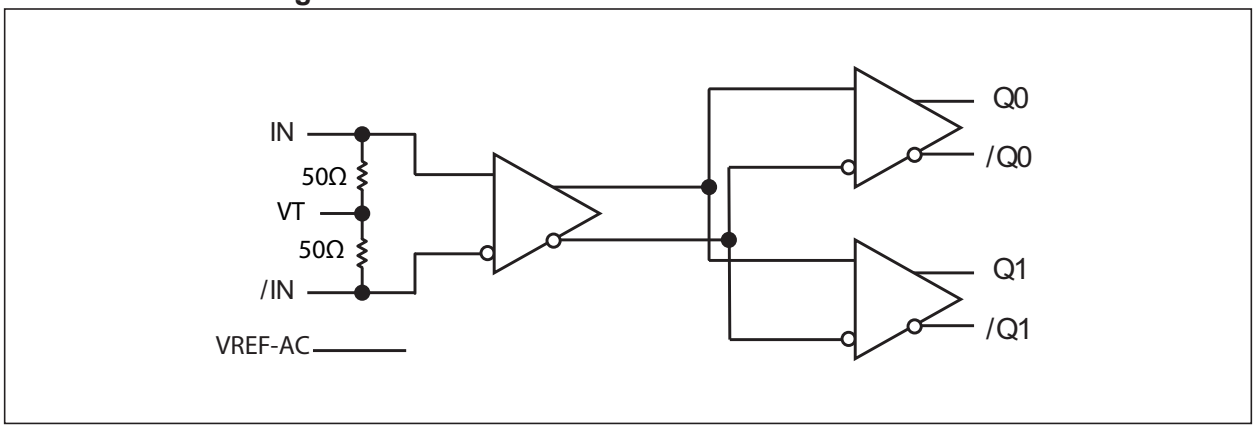
The SY58606U operates from a 2.5V ±5% supply or 3.3V ±10% supply and is guaranteed over the full industrial temperature range (–40°C to +85°C). For applications that require LVPECL or LVDS outputs, consider Microchip's SY58607U and SY58608U, 1:2 fanout buffers with 800 mV and 325 mV output swings respectively. The SY58606U is part of Microchip's high-speed, Precision Edge® product line.

### Package Type

**SY58606U**
3 mm x 3 mm QFN-16 (M)
(Top View)



## Functional Block Diagram



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

Supply Voltage ($V_{CC}$) ..... –0.5V to +4.0V
Input Voltage ($V_{IN}$) ..... –0.5V to $V_{CC}$
CML Output Voltage ($V_{OUT}$) ..... $V_{CC}$ – 1.0V to $V_{CC}$ + 0.5V
Current ($I_T$)
    Source or Sink on VT Pin ..... ±100 mA
Input Current
    Source or Sink Current on, IN, /IN ..... ±50 mA
Current ($I_{REF}$)
    Source or Sink Current on VREF-AC (Note 1) ..... ±1.5 mA
Maximum Operating Junction Temperature ..... +125°C
Lead Temperature (Soldering, 20 sec.) ..... +260°C
Storage Temperature ($T_S$) ..... –65°C to +150°C

### Operating Ratings ††

Supply Voltage ($V_{CC}$) ..... +2.375V to +3.60V
Ambient Temperature ($T_A$) ..... –40°C to +85°C
Package Thermal Resistance (Note 2)
QFN-16, Still-Air ($\theta_{JA}$) ..... 60°C/W
QFN-16, Junction-to-Board ($\Psi_{JB}$) ..... 33°C/W

**† Notice:** Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

**†† Notice:** The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

**Note 1:** Due to the limited drive capability, use for input of the same package only.

**2:** Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. $\Psi_{JB}$ and $\theta_{JA}$ values are determined for a 4-layer board in still-air number, unless otherwise stated.

## DC ELECTRICAL CHARACTERISTICS (Note 1)

**Electrical Characteristics:** $T_A$ = –40°C to +85°C, unless otherwise stated.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Power Supply Voltage Range | $V_{CC}$ | 2.375 | 2.5 | 2.625 | V | — |
| | | 3.0 | 3.3 | 3.6 | | |
| Power Supply Current | $I_{CC}$ | — | 60 | 77 | mA | No load, max. $V_{CC}$ |
| Differential Input Resistance (IN-to-/IN) | $R_{DIFF\_IN}$ | 90 | 100 | 110 | Ω | — |
| Input HIGH Voltage (IN, /IN) | $V_{IH}$ | $V_{CC}$ – 1.6 | — | $V_{CC}$ | V | IN, /IN, Note 2 |
| Input LOW Voltage (IN, /IN) | $V_{IL}$ | 0 | — | $V_{IH}$ – 0.1 | V | IN, /IN |
| Input Voltage Swing (IN, /IN) | $V_{IN}$ | 0.1 | — | 1.7 | V | See Figure 5-5, (Note 3) |
| Differential Input Voltage Swing (\|IN - /IN\|) | $V_{DIFF\_IN}$ | 0.2 | — | — | V | See Figure 5-6 |
| Input Voltage Threshold that Triggers FSI | $V_{IN\_FSI}$ | — | 30 | 100 | mV | — |
| Output Reference Voltage | $V_{REF-AC}$ | $V_{CC}$ – 1.3 | $V_{CC}$ – 1.2 | $V_{CC}$ – 1.1 | V | — |
| Voltage from Input to VT | $V_{T-IN}$ | — | — | 1.28 | V | — |

**Note 1:** The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

**2:** $V_{IN(MIN)}$ not lower than 1.2V.

**3:** $V_{IN(MAX)}$ is specified when VT is floating.

## CML OUTPUTS DC ELECTRICAL CHARACTERISTICS (Note 1)

**Electrical Characteristics:** $V_{CC}$ = +2.5V ±5% or +3.3V ±10%, $R_L$ = 100Ω across the outputs; $T_A$ = –40°C to +85°C, unless otherwise stated.

| Parameter | Symbol | Min. | Typ. | Max. | Units | Condition |
|---|---|---|---|---|---|---|
| Output High Voltage | $V_{OH}$ | $V_{CC}$ – 0.02 | $V_{CC}$ – 0.01 | $V_{CC}$ | V | $R_L$ = 50Ω to $V_{CC}$ |
| Output Voltage Swing | $V_{OUT}$ | 325 | 400 | — | mV | See Figure 5-5 |
| Differential Output Voltage Swing | $V_{DIFF\_OUT}$ | 650 | 800 | — | mV | See Figure 5-6 |
| Output Source Impedance | $R_{OUT}$ | 45 | 50 | 55 | Ω | — |

**Note 1:** The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

## AC ELECTRICAL CHARACTERISTICS

**Electrical Characteristics:** $V_{CC}$ = +2.5V ±5% or +3.3V ±10%, $R_L$ = 100Ω across the outputs; Input $t_r/t_f$: ≤300 ps; $T_A$ = –40°C to +85°C, unless otherwise stated.

| Parameter | Symbol | Min. | Typ. | Max. | Units | Condition |
|---|---|---|---|---|---|---|
| Maximum Frequency | $f_{MAX}$ | 4.25 | — | — | Gbps | NRZ (Data) |
| | | 2.5 | 3.0 | — | GHz | $V_{OUT}$ ≥ 200 mV (Clock), $V_{IN}$ ≥ 400 mV |
| Propagation Delay IN-to-Q | $t_{PD}$ | 150 | 270 | 400 | ps | $V_{IN}$: 100 mV - 200 mV |
| | | 120 | 220 | 320 | ps | $V_{IN}$: 200 mV - 800 mV |
| Within Device Skew | $t_{SKEW}$ | — | 3 | 15 | ps | Note 1 |
| Part-to-Part Skew | | — | — | 100 | ps | Note 2 |
| Additive Jitter | $t_{JITTER}$ | — | 100 | — | $fs_{RMS}$ | Carrier = 622 MHz<br>Integration Range: 12 kHz – 20 MHz |
| Output Rise/Fall Time (20% to 80%) | $t_r$, $t_f$ | 30 | 50 | 85 | ps | At full output swing |
| Duty Cycle | — | 47 | — | 53 | % | Differential I/O |

**Note 1:** Within-device skew is measured between two different outputs under identical input transitions.

**2:** Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.

## TEMPERATURE SPECIFICATIONS

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **Temperature Ranges** | | | | | | |
| Operating Ambient Temperature Range | $T_A$ | –40 | — | +85 | °C | — |
| Maximum Operating Junction Temperature | $T_J$ | — | — | +125 | °C | — |
| Lead Temperature | — | — | — | +260 | °C | Soldering, 20 sec. |
| Storage Temperature Range | $T_S$ | –65 | — | +150 | °C | — |
| **Package Thermal Resistances (Note 1)** | | | | | | |
| Thermal Resistance, 3x3 QFN-16Ld | $\theta_{JA}$ | — | 60 | — | °C/W | Still-air |
| | $\psi_{JB}$ | — | 33 | — | °C/W | Junction-to-board |

**Note 1:** Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. $\psi_{JB}$ and $\theta_{JA}$ values are determined for a 4-layer board in still-air number, unless otherwise stated.

## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

$V_{CC}$ = 3.3V, GND = 0V, $R_L$ = 100Ω across the outputs, $T_A$ = +25°C, unless otherwise stated.

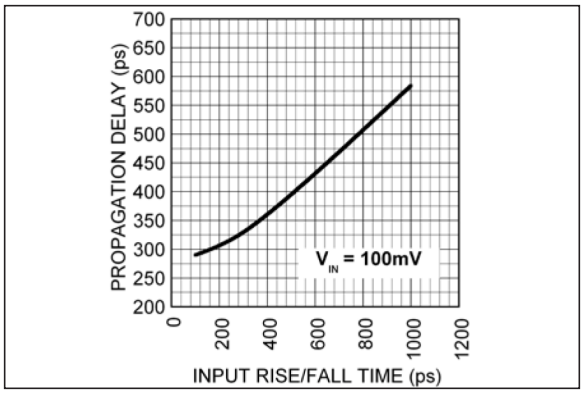



***FIGURE 2-1:*** *Propagation Delay vs. Input Rise/Fall Time.*

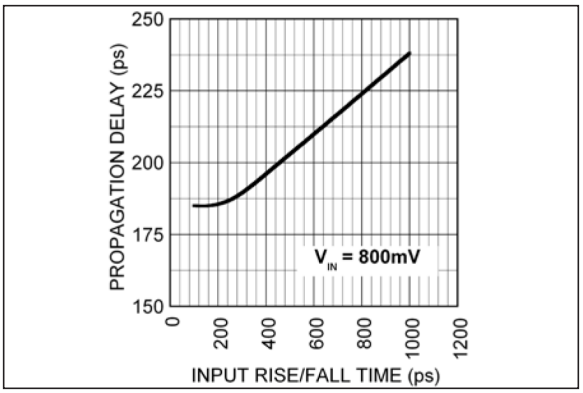



***FIGURE 2-4:*** *Propagation Delay vs. Input Rise/Fall Time.*

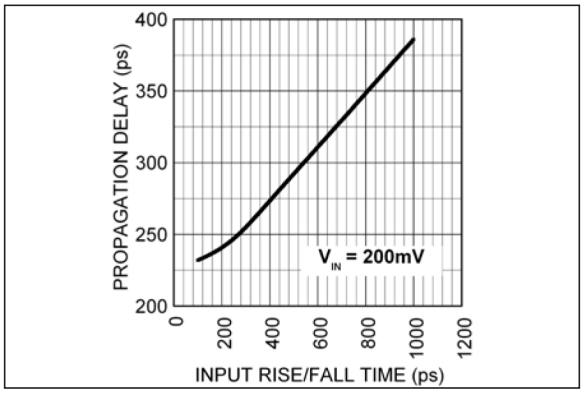



***FIGURE 2-2:*** *Propagation Delay vs. Input Rise/Fall Time.*

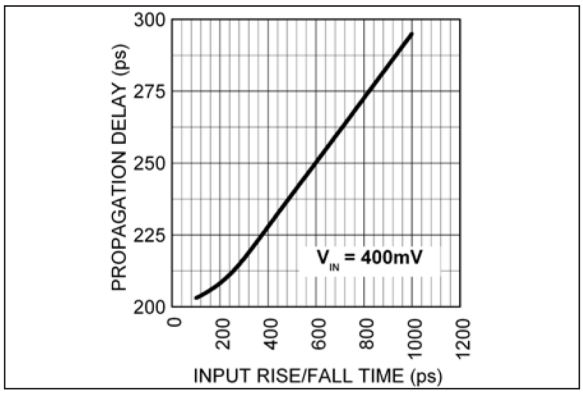



***FIGURE 2-3:*** *Propagation Delay vs. Input Rise/Fall Time.*

$V_{CC}$ = 2.5V, GND = 0V, $V_{IN}$ = 325 mV, Data Pattern: $2^{23}$-1, $R_L$ = 100Ω across the outputs, $T_A$ = +25°C, unless otherwise stated.

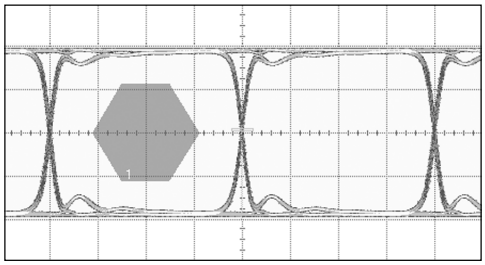



***FIGURE 2-5:*** *1.25 Gbps Data.*

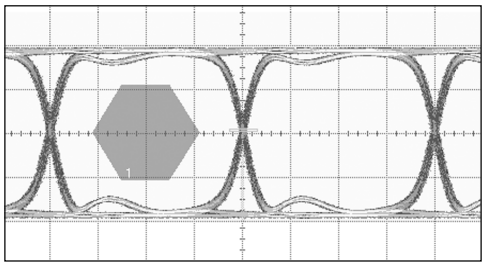



***FIGURE 2-6:*** *2.5 Gbps Data.*

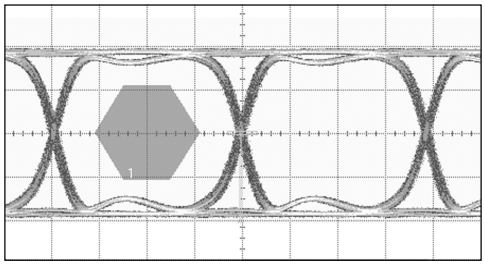



***FIGURE 2-7:*** *3.2 Gbps Data.*

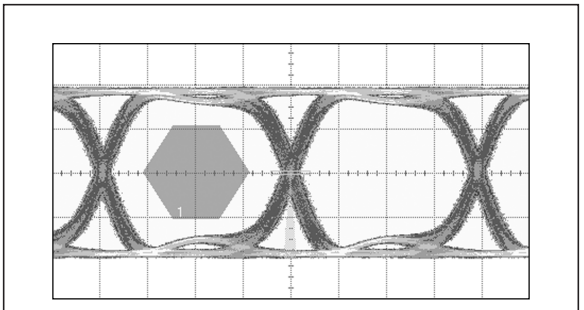



***FIGURE 2-8:*** *4.25 Gbps Data.*

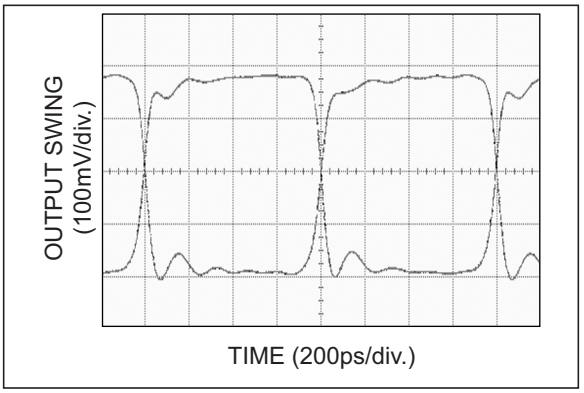



***FIGURE 2-9:*** *625 MHz Clock.*

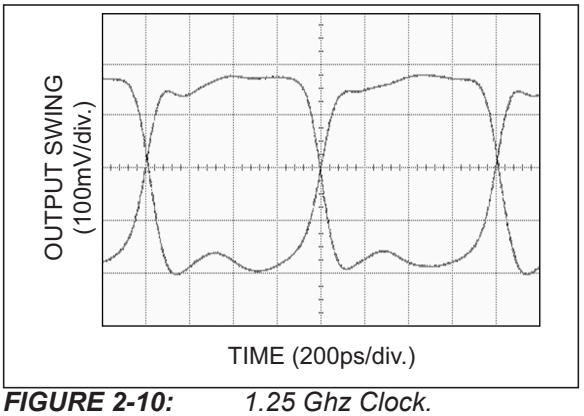



***FIGURE 2-10:*** *1.25 Ghz Clock.*

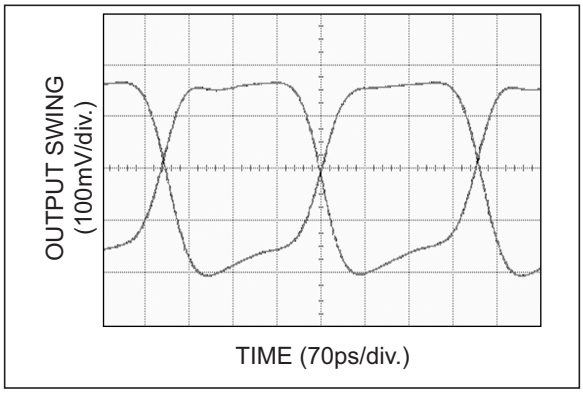



***FIGURE 2-11:*** *2 GHz Clock.*

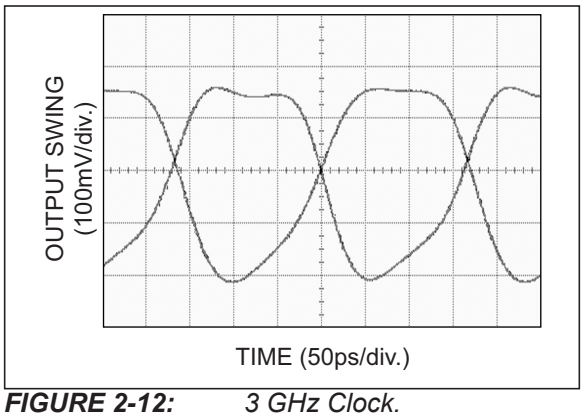



***FIGURE 2-12:*** *3 GHz Clock.*

## 3.0 ADDITIVE PHASE NOISE PLOT

$V_{CC}$ = +3.3V, $T_A$ = +25°C.

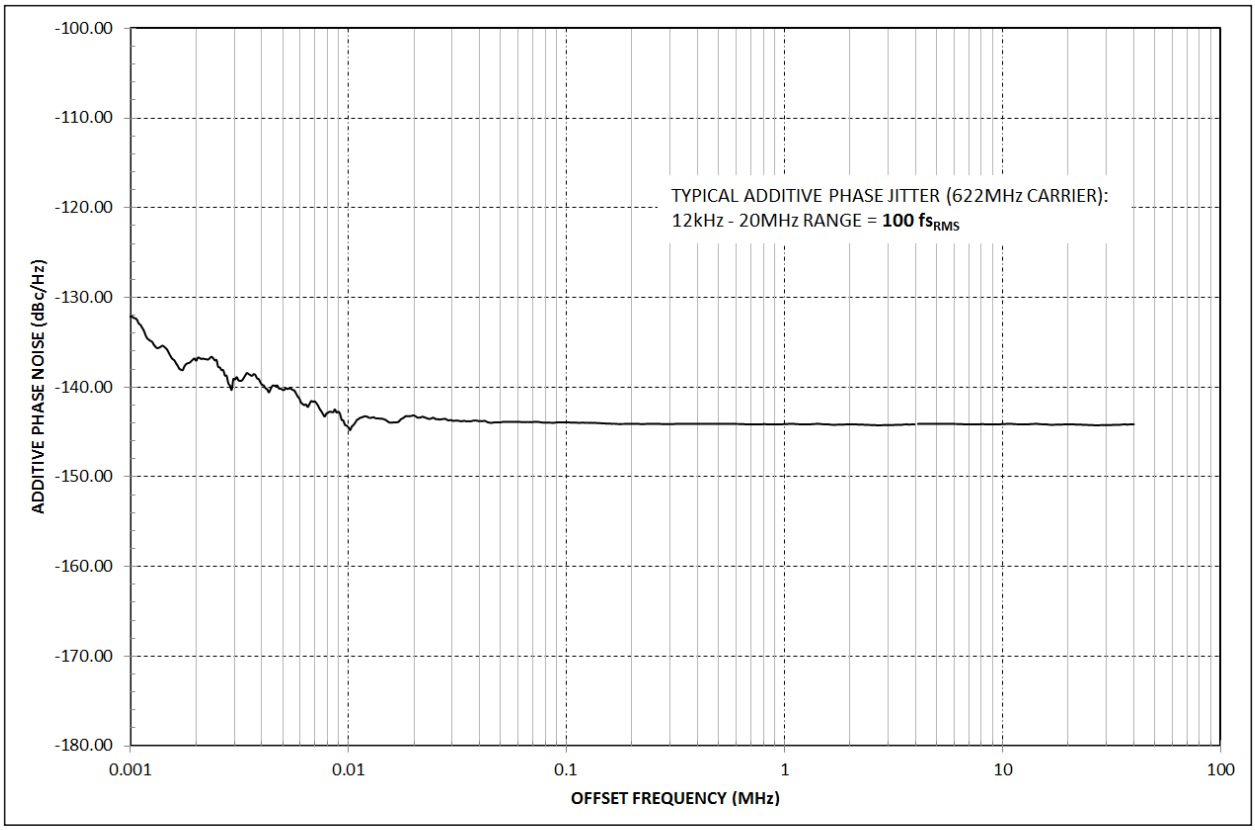



***FIGURE 3-1:*** *Additive Noise Plot.*

## 4.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 4-1.

**TABLE 4-1: PIN FUNCTION TABLE**

| Pin Number | Symbol | Description |
|---|---|---|
| 1, 4 | IN, /IN | Differential Input: This input pair is the differential signal input to the device. Input accepts DC-coupled differential signals as small as 100 mV (200 $mV_{PP}$). Each pin of this pair internally terminates with 50Ω to the VT pin. If the input swing falls below a certain threshold (typical 30 mV), the Fail Safe Input (FSI) feature will guarantee a stable output by latching the output to its last valid state. See the Input Interface Applications section. |
| 2 | VT | Input Termination Center Tap: Each side of the differential input pair terminates to the VT pin. This pin provides a center-tap to a termination network for maximum interface flexibility. See the Input Interface Applications section. |
| 3 | VREF-AC | Reference Voltage: This output biases to $V_{CC}$ – 1.2V. It is used for AC-coupling inputs IN and /IN. Connect VREF-AC directly to the VT pin. Bypass with 0.01 µF low-ESR capacitor to VCC. Maximum sink/source current is ±1.5 mA. See the Input Interface Applications section. |
| 5, 8,13, 16 | VCC | Positive Power Supply: Bypass with 0.1 µF//0.01 µF low-ESR capacitors as close to the VCC pins as possible. |
| 6, 7, 14, 15 | GND, Exposed pad | Ground: Exposed pad must be connected to a ground plane that is the same potential as the ground pins. |
| 9, 10<br>11, 12 | /Q1, Q1<br>/Q0, Q0 | CML Differential Output Pairs: Differential buffered copies of the input signal. The output swing is typically 400 mV. Unused output pair may be left floating with no impact on jitter. See the CML Output Termination section. |

## 5.0 FUNCTIONAL DESCRIPTION

### 5.1 Fail-Safe Input (FSI)

The input includes a special fail-safe circuit to sense the amplitude of the input signal and to latch the outputs when there is no input signal present, or when the amplitude of the input signal drops sufficiently below 100 $mV_{PK}$ (200 $mV_{PP}$), typically 30 $mV_{PK}$. Maximum frequency of SY58606U is limited by the FSI function.

### 5.2 Input Clock Failure Case

If the input clock fails to a floating, static, or extremely low signal swing, then the FSI function will eliminate a metastable condition and guarantee a stable output. No ringing and no undetermined state will occur at the output under these conditions.

Note that the FSI function will not prevent duty cycle distortion in case of a slowly deteriorating (but still toggling) input signal. Due to the FSI function, the propagation delay will depend on rise and fall time of the input signal and on its amplitude. Refer to the Typical Performance Curves section for detailed information.

### Timing Diagrams

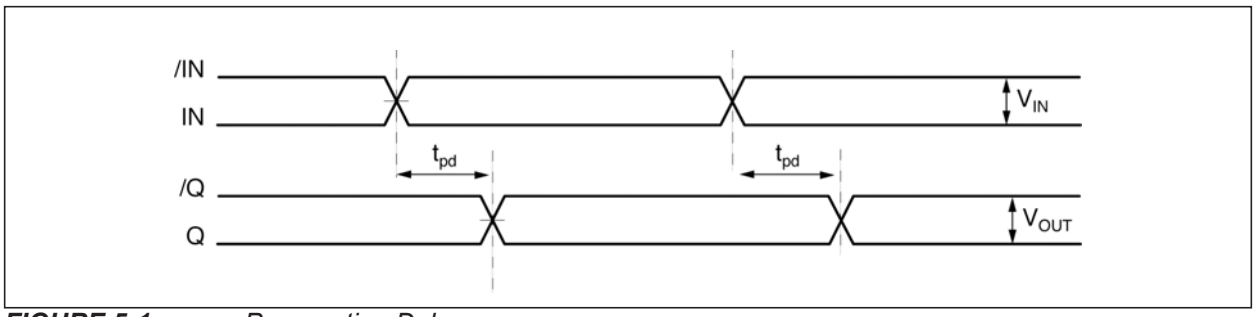



***FIGURE 5-1:*** *Propagation Delay.*

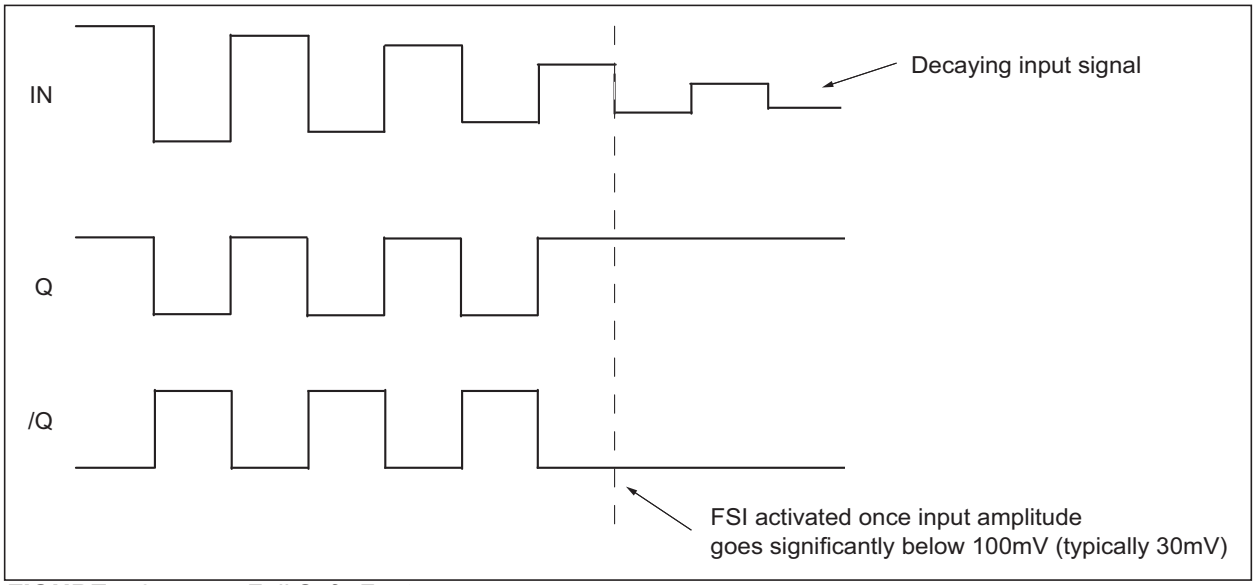



***FIGURE 5-2:*** *Fail Safe Feature.*

## Input and Output Stage

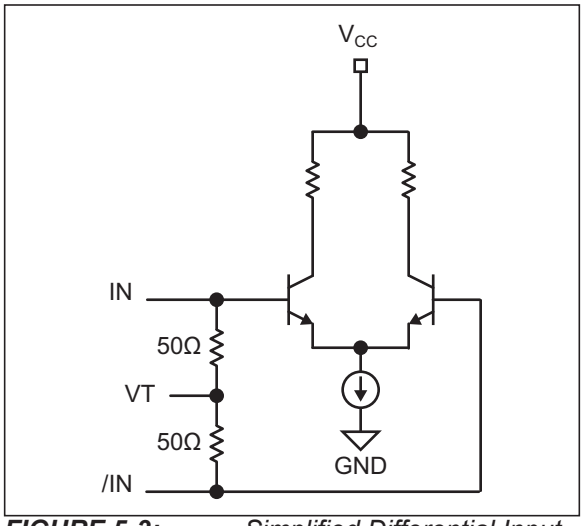



***FIGURE 5-3:*** *Simplified Differential Input Buffer.*

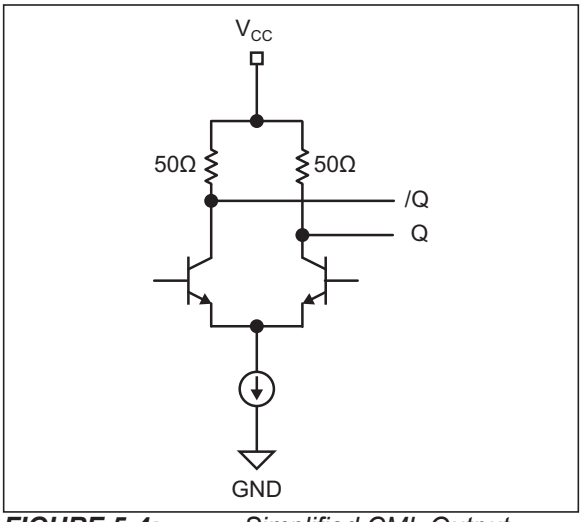



***FIGURE 5-4:*** *Simplified CML Output Buffer.*

## Single-Ended and Differential Swings

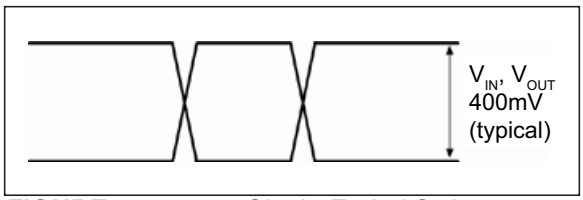



***FIGURE 5-5:*** *Single-Ended Swing.*

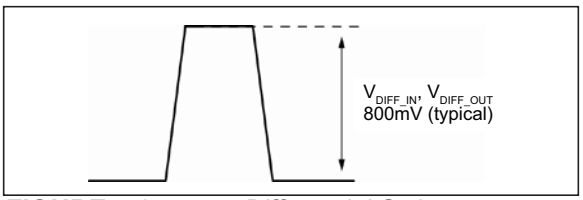



***FIGURE 5-6:*** *Differential Swing.*

## 6.0 INPUT INTERFACE APPLICATIONS

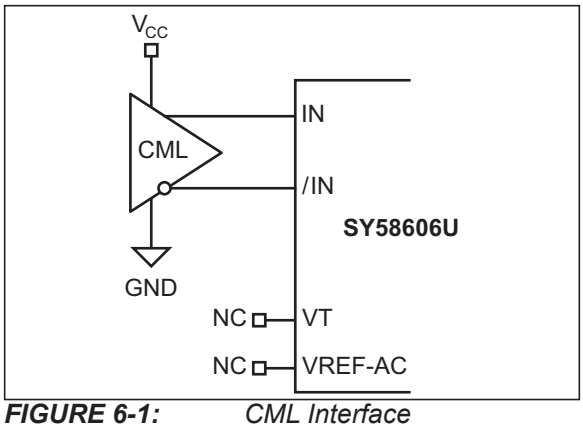



***FIGURE 6-1:*** *CML Interface (DC-Coupled) May connect VT to $V_{CC}$.*

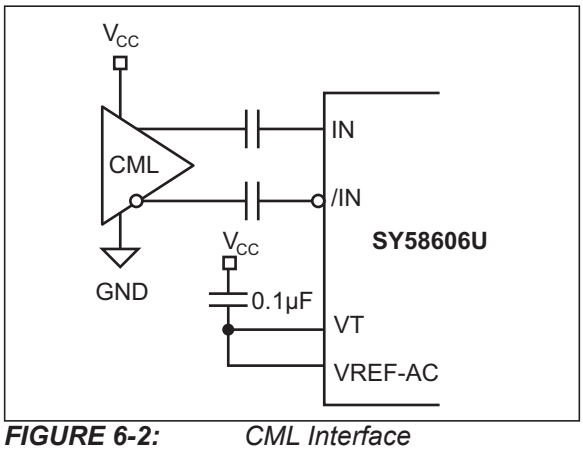



***FIGURE 6-2:*** *CML Interface (AC-Coupled).*

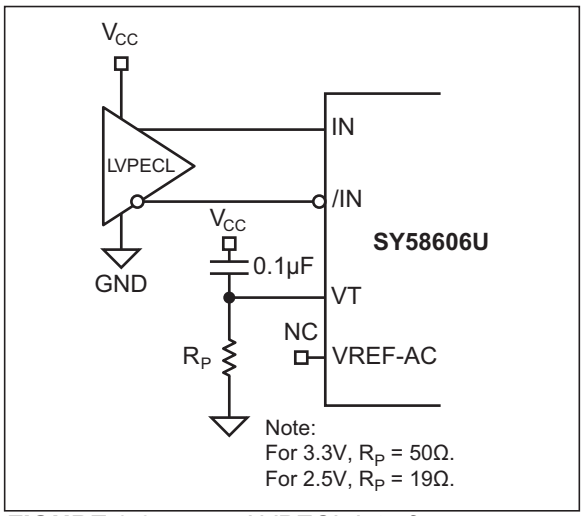



***FIGURE 6-3:*** *LVPECL Interface (DC-Coupled).*

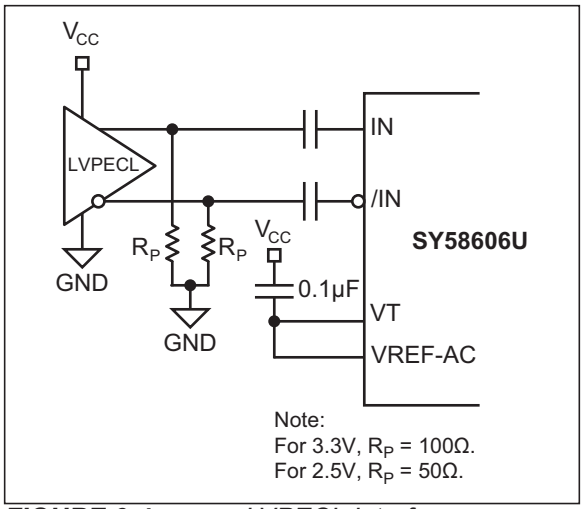



***FIGURE 6-4:*** *LVPECL Interface (AC-Coupled).*

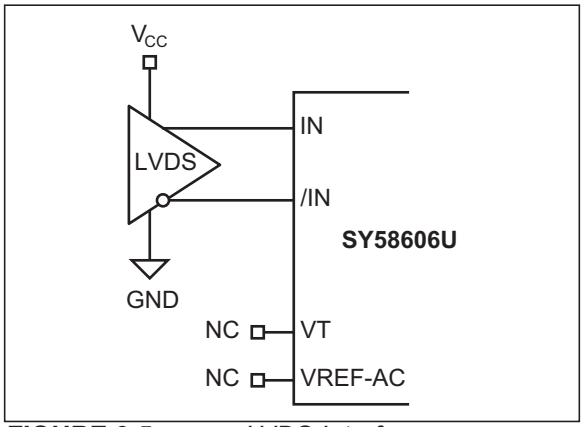



***FIGURE 6-5:*** *LVDS Interface (DC-Coupled).*

## 7.0 CML OUTPUT TERMINATION

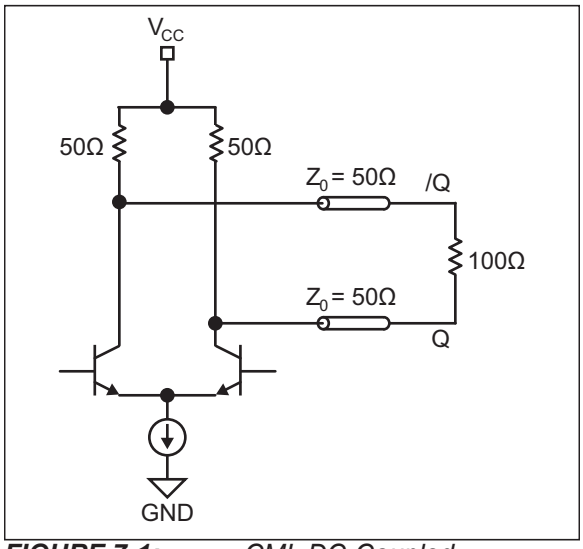



***FIGURE 7-1:*** *CML DC-Coupled Termination.*

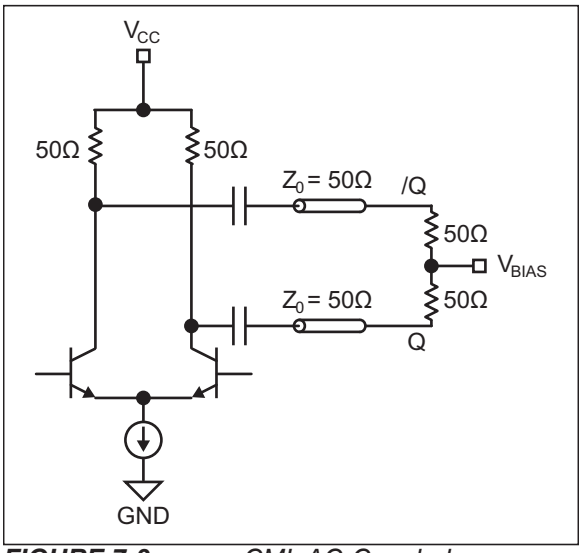



***FIGURE 7-3:*** *CML AC-Coupled Termination.*

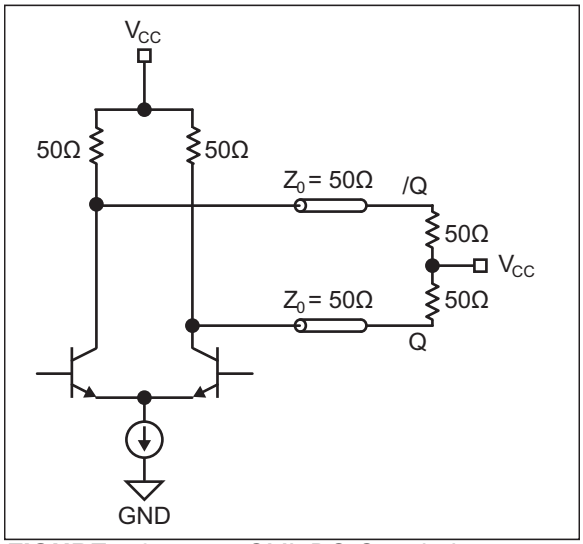



***FIGURE 7-2:*** *CML DC-Coupled Termination.*

## 8.0 PACKAGING INFORMATION

### 8.1 Package Marking Information

16-Lead QFN*

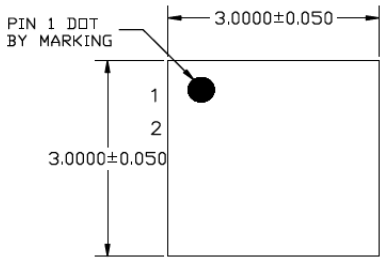

Example


| | | |
|---|---|---|
| **Legend:** | XX...X | Product code or customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC® designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |
| | ●, ▲, ▼ | Pin one index is identified by a dot, delta up, or delta down (triangle mark). |
| **Note**: | | In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo. |
| | | Underbar (_) and/or Overbar (¯) symbol may not be to scale. |

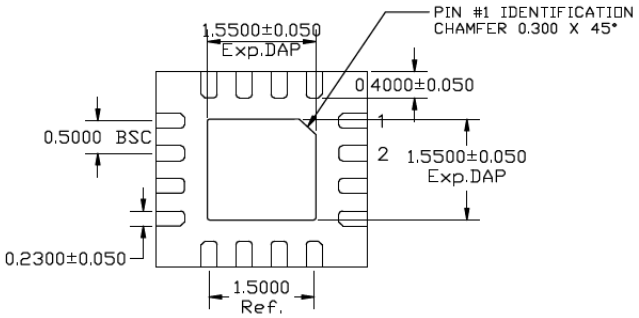
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

**TITLE**
16 LEAD QFN 3x3mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

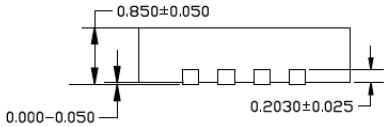
| DRAWING # | QFN33-16LD-PL-1 | UNIT | MM |
|---|---|---|---|




TOP VIEW
NOTE: 1, 2, 3




BOTTOM VIEW
NOTE: 1, 2, 3

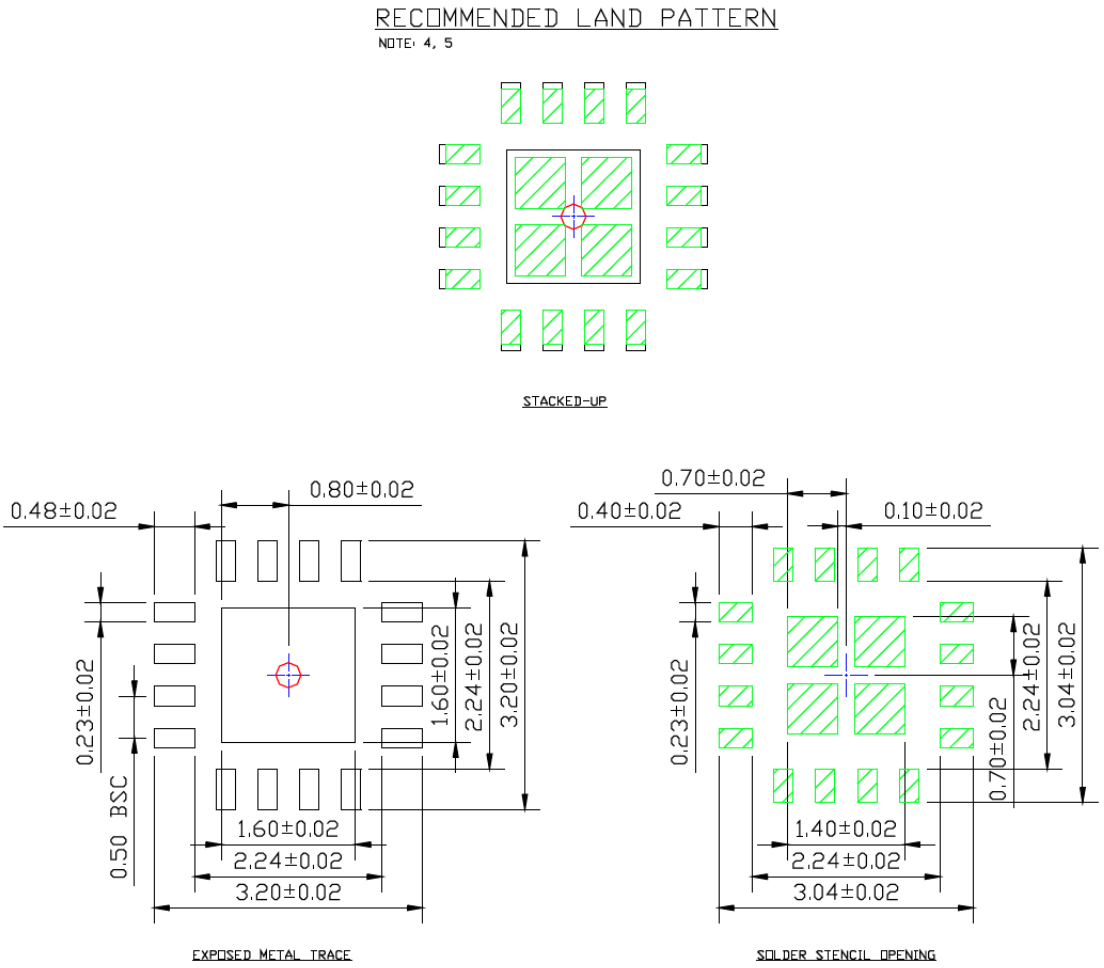



SIDE VIEW
NOTE: 1, 2, 3

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076 MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.35 MM IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.60x0.60 MM IN SIZE, 0.20 MM SPACING.

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

POD-Land Pattern drawing # QFN33-16LD-PL-1



**NOTES:**

# APPENDIX A: REVISION HISTORY

## Revision A (May 2019)

- Converted Micrel document SY58606U to Microchip data sheet template DS20006199A.
- Minor text changes throughout.

**NOTES:**

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

| PART NO. | X | X | X | XX |
|---|---|---|---|---|
| Device | Supply Voltage | Package | Temperature Range | Tape and Reel |

| | | | |
|---|---|---|---|
| **Device:** | SY58606: | | 4.25 Gbps Precision, 1:2 CML Fanout Buffer with Internal Termination and Fail Safe Input |
| **Supply Voltage:** | U | = | 2.5V/3.3V |
| **Package:** | M | = | 3 mm x 3 mm QFN-16 |
| **Temperature Range:** | G | = | –40°C to 85°C (NiPdAu Lead-Free) |
| **Special Processing:** | <blank> | = | 100/Tube |
| | TR | = | 1,000/Reel |

**Examples:**

a) SY58606UMG: SY58606, 2.5V/3.3V Supply Voltage, 3 mm x 3 mm 16-Lead QFN, –40°C to +85°C Temperature Range, 100/Tube

b) SY58606UMG-TR: SY58606, 2.5V/3.3V Supply Voltage, 3 mm x 3 mm 16-Lead QFN, –40°C to +85°C Temperature Range, 1,000/Reel

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

**NOTES:**

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.



*Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.*

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