MAX16193

0.3% Accuracy Dual-Channel Supervisory Circuit

General Description

The MAX16193 is an ultra-high accuracy, dual-channel window-detector supervisor circuit that monitors a system's supply rails for undervoltage and overvoltage faults. Input channel 1 (IN1) monitors low core voltage rails from a 0.6V to 0.9V threshold range with ±0.3% accuracy while input-channel 2 (IN2) monitors higher system rails in i a 0.9V to 3.3V threshold range with ±0.3% accuracy. A variety of factory trimmed undervoltage/overvoltage thresholds from ±2% to ±5% are available to accommodate different supply voltages and tolerances.

The MAX16193 features two independent, active-low reset outputs. Both reset output are available in either an open-drain or push-pull version. Each reset output asserts low when the corresponding monitored rail falls outside of the undervoltage/overvoltage threshold window. The reset outputs deassert after a factory-set reset timeout period when the corresponding rail voltage returns to its nominal voltage level.

The MAX16193 is available in a small, 2mm x 3mm, 8-pin standard TDFN chip-on-lead package for industrial and a side-wettable package for automotive. It can operate over the temperature range of -40°C to +125°C.

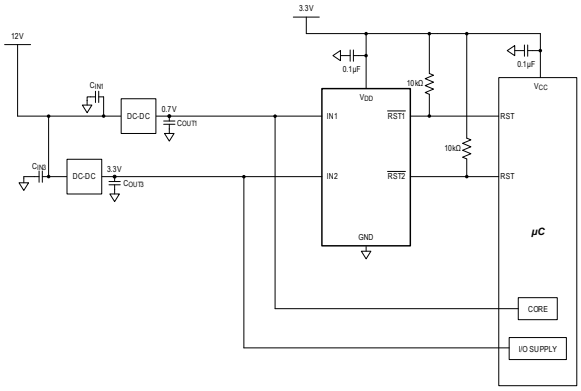
Applications

- Advanced Driver-Assistance Systems (ADAS)
- Programmable Logic Controllers (PLC)
- FPGA-Based Systems
- Medical Equipment
- Multivoltage ASICs
- Servers
- Storage Equipment

Benefits and Features

- ±0.3% IN1 Threshold Accuracy
- ±0.3% IN2 Threshold Accuracy
- 0.6V to 0.9V IN1 Threshold Range
- 0.9V to 3.3V IN2 Threshold Range
- ±2% to ±5% UV/OV Monitoring Range
- Open-Drain/Push-Pull Reset Output Options
- Enables Functional Safety at System Level
- Automotive:
  - 8-Pin TDFN, 2mm x 3mm Side-Wettable Flanks with exposed pad
  - AEC-Q100 Qualified
- Industrial:
  - 8-Pin TDFN, 2mm x 3mm Package with exposed pad
- -40°C to +125°C Temperature Range

Typical Application Circuit



Ordering Information appears at end of data sheet.

19-101424; Rev 2; 7/26

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Absolute Maximum Ratings

V_{DD} to GND .....-0.3V to +6V

IN1, IN2 to GND .....-0.3V to +6V

$\overline{RST1}$ $\overline{RST2}$ (Open Drain Outputs) to GND .....-0.3V to +6V

$\overline{RST1}$ $\overline{RST2}$ (Push-Pull Outputs) to GND -0.3V to VDD + 0.3V

Input/Output Continuous Current..... ±20mA

Continuous Power Dissipation (TDFN) ((T823Y+3C, T823+3C) T_A = +70°C, derate 16.7mW/°C above +70°C)..... 1333.3mW

Operating Temperature Range ..... -40°C to +125°C

Junction Temperature ..... +150°C

Soldering Temperature (Reflow) ..... +260°C

Storage Temperature Range ..... -65°C to +150°C

Lead Temperature (Soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

Package Code	T823Y+3C	T823+3C
Outline Number	*21-100417*	*21-0174*
Land Pattern Number	*90-0091*	*90-0091*
Thermal Resistance, Four Layer Board:		
Junction-to-Ambient (θ_{JA})	60°C/W	60°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	11°C/W	11°C/W

For the latest package outline information and land patterns (footprints), go to *Package Index*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *Thermal Characterization of IC Packages*.

Electrical Characteristics

(V_{DD} = 1.7V to 5.5V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = 3.3V, V_{IN1} = V_{IN1_NOM}, V_{IN2} = V_{IN2_NOM}, and T_A = +25°C under normal conditions, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Operating Voltage Range	V_{DD}	Output guaranteed to be at known state	1.7		5.5	V
Minimum Supply Voltage	V_{DD}	$\overline{RST1}$ and $\overline{RST2}$ are guaranteed to be at a known logic	1.1			V
Supply Current	I_{DD}	$\overline{RST1}$ and $\overline{RST2}$ not asserted		50	100	µA
Undervoltage Lockout Threshold	V_{UVLO}	V_{DD} rising	1.30	1.50	1.68	V
Undervoltage Lockout Hysteresis	V_{UVLO_HYS}	V_{DD} falling		47		mV
INPUT VOLTAGE (IN1 AND IN2)						
IN1 Input Voltage Range (Note 1)	V_{IN1_NOM}		0.6		0.9	V
IN2 Input Voltage Range (Note 1)	V_{IN2_NOM}		0.9		3.3	V

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(V_{DD} = 1.7V to 5.5V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = 3.3V, V_{IN1} = V_{IN1_NOM}, V_{IN2} = V_{IN2_NOM}, and T_A = +25°C under normal conditions, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage/Overvoltage Threshold Programming Range	TOL	Reset occurs when V_{IN} falls outside of V_{IN_NOM} x (1±TOL)	±2		±5	% of V_{IN_NOM}
INPUT THRESHOLD ACCURACY						
IN1/IN2 Overvoltage Threshold Accuracy	V_{OVTH_A}	V_{IN1} /V_{IN2} rising, V_{OVTH} = V_{IN_NOM} x (1+TOL%)	-0.3		+0.3	%
IN1/IN2 Undervoltage Threshold Accuracy	V_{UVTH_A}	V_{IN1} / V_{IN2} falling, V_{UVTH} = V_{IN_NOM} x (1 - TOL%)	-0.3		+0.3	%
Undervoltage/Overvoltage Hysteresis	V_{HYS}			0.15		$\%V_{TH}$
Input Current	I_{IN1}	V_{IN1} = V_{IN1_NOM}		3	6	µA
	I_{IN2}	V_{IN2} = V_{IN2_NOM}		6	12	µA
RESET OUTPUT ($\overline{RST1}$ AND $\overline{RST2}$)						
Reset Timeout Period Accuracy (Note 3)	t_{RP}	From time $V_{IN_}$ enters overvoltage/undervoltage threshold-window to time $\overline{RST_}$ goes high	-20		+20	%
IN1-to-$\overline{RST1}$ Propagation Delay	t_D	(V_{UVTH} + 1%) to (V_{UVTH} - 1%) or (V_{OVTH} - 1%) to (V_{OVTH} + 1%)		5		µs
IN2-to-$\overline{RST2}$ Propagation Delay	t_D	(V_{UVTH} + 1%) to (V_{UVTH} - 1%) or (V_{OVTH} - 1%) to (V_{OVTH} + 1%)		5		µs
OUTPUT VOLTAGE						
Output Voltage Low	V_{OL}	V_{DD} ≥ 4.25V, I_{SINK} = 1mA			0.1	V
		V_{DD} = 2.5V, I_{SINK} = 250µA			0.1	
		V_{DD} = 1.2V, I_{SINK} = 25µA			0.1	
Output Voltage High (Push-Pull)	V_{OH}	V_{DD} = 1.70V, I_{SOURCE} = 200µA	0.8 x V_{DD}			V
		V_{DD} ≥ 4.5V, I_{SOURCE} = 800µA	0.8 x V_{DD}			

Note 1: Input voltage for IN1 and IN2 is factory programmable to a midpoint between the undervoltage threshold and overvoltage threshold levels.

Note 2: Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

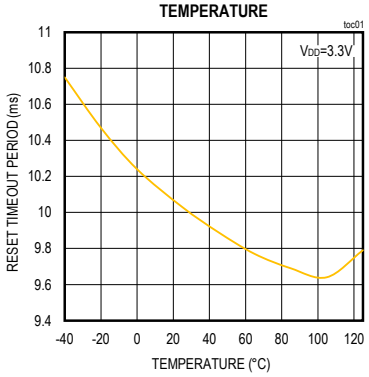
Note 3: For Reset Timeout Period t_{RP} = 50µs, only typical specification is given.

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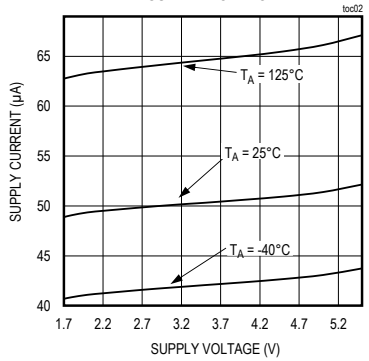
Typical Operating Characteristics

(V_{DD} = 1.70V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

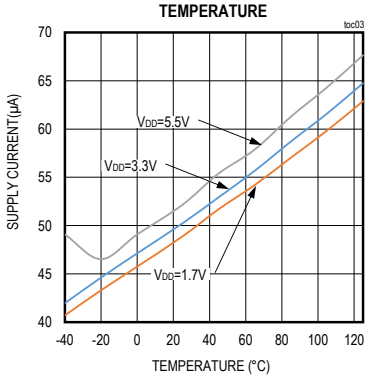
RESET TIMEOUT PERIOD VS TEMPERATURE



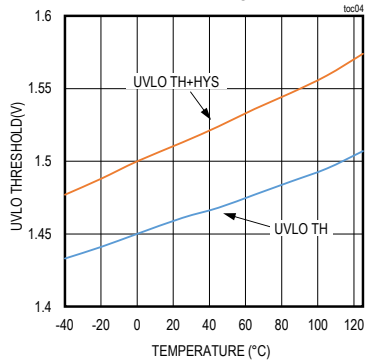
SUPPLY CURRENT VS SUPPLY VOLTAGE



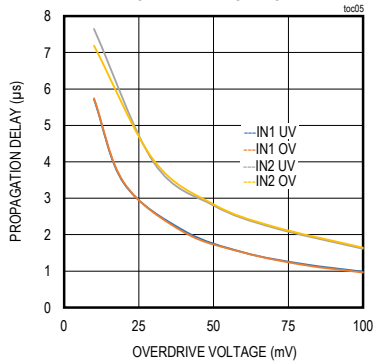
SUPPLY CURRENT VS TEMPERATURE



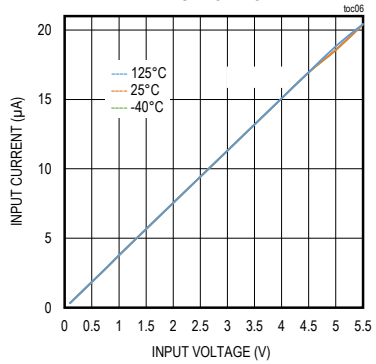
UVLO THRESHOLD VS TEMPERATURE



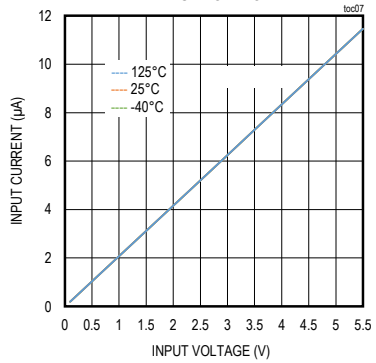
PROPAGATION DELAY VS OVERDRIVE VOLTAGE



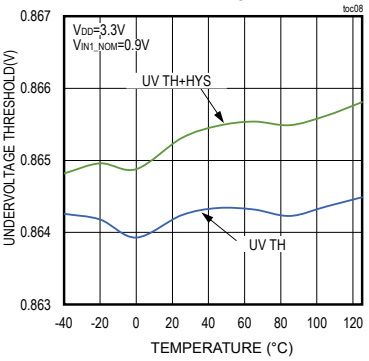
IN1 INPUT CURRENT VS INPUT VOLTAGE



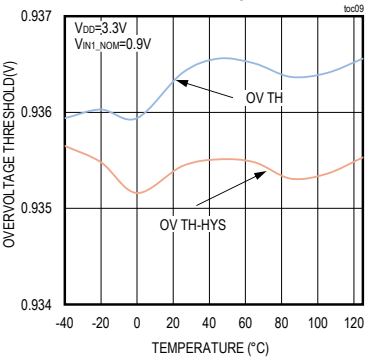
IN2 INPUT CURRENT VS INPUT VOLTAGE



UNDERVOLTAGE THRESHOLD VS TEMPERATURE

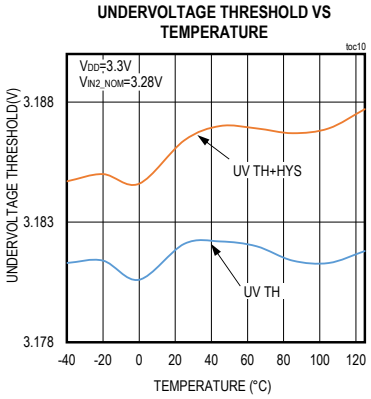


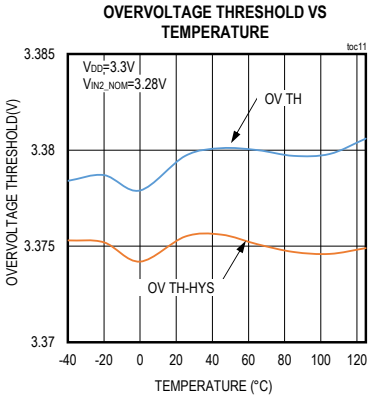
OVERVOLTAGE THRESHOLD VS TEMPERATURE

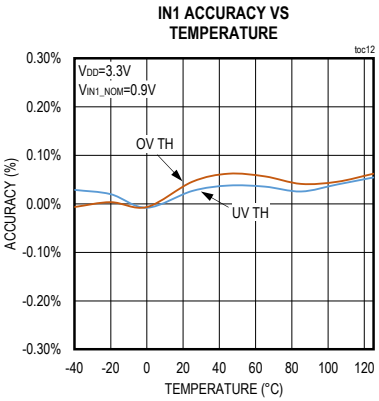


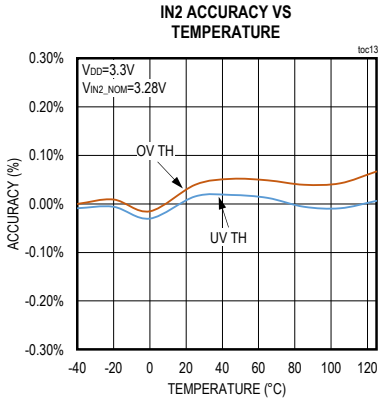
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(V_{DD} = 1.70V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

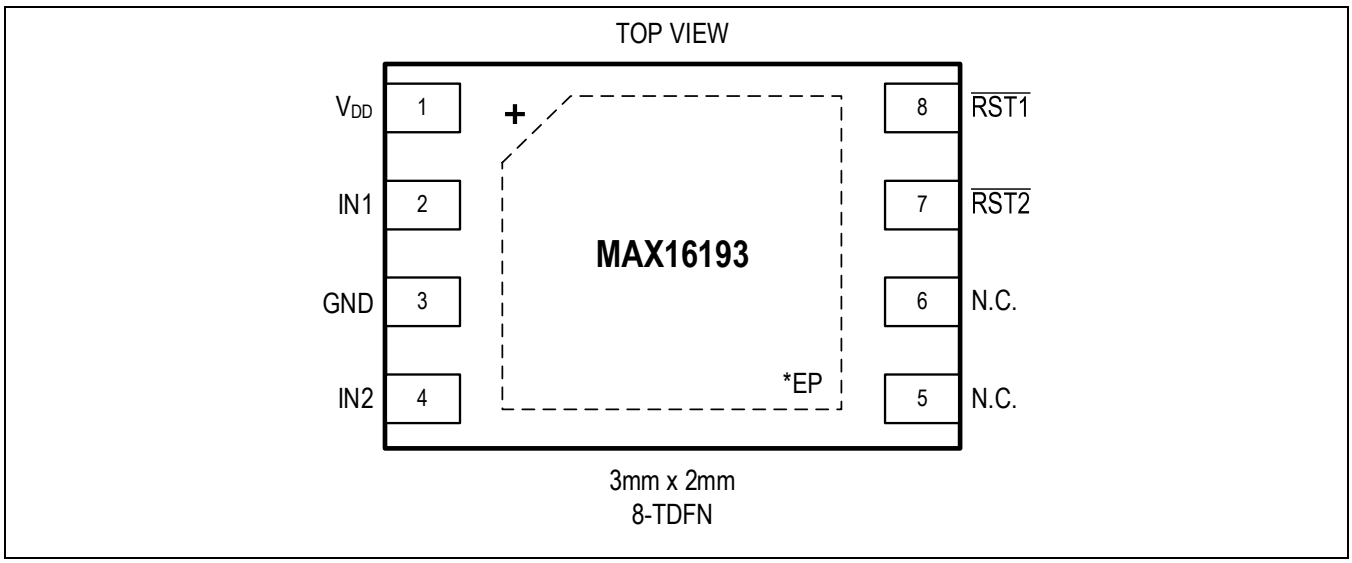








Pin Configurations



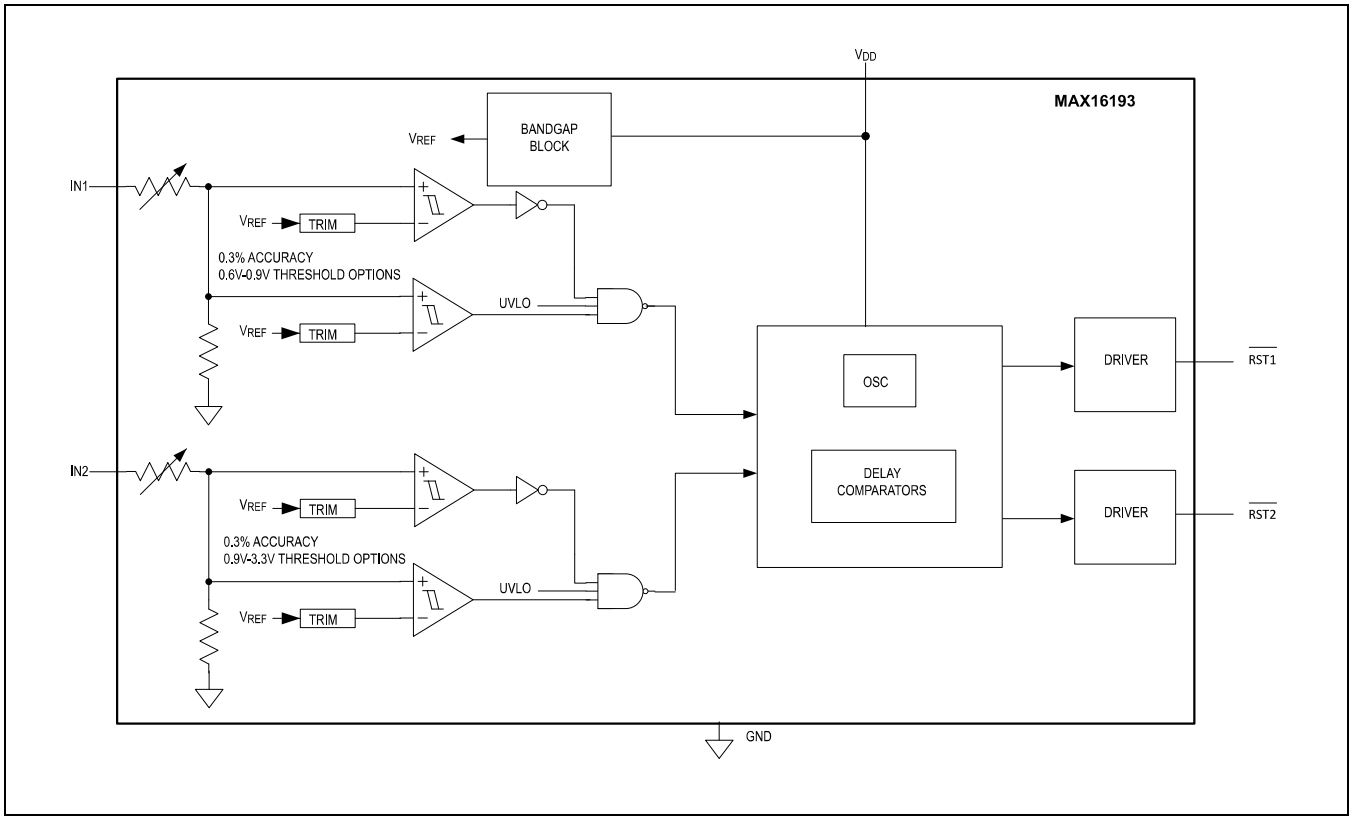
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Pin Descriptions

PIN	NAME	FUNCTION
1	V_{DD}	Supply Input. Bypass V_{DD} to ground with a 0.1µF capacitor.
2	IN1	Monitoring Input 1. IN1 monitors supply rails for undervoltage/overvoltage faults with respect to a nominal input threshold. IN1 monitors supply range from 0.6V to 0.9V. When V_{IN1} falls outside the undervoltage/overvoltage thresholds window, $\overline{RST1}$ asserts and stays asserted for the reset timeout period after V_{IN1} falls within undervoltage/overvoltage thresholds window.
3	GND	Ground.
4	IN2	Monitoring Input 2. IN2 monitors supply rails for undervoltage/overvoltage faults with respect to nominal input threshold. IN2 monitors supply range from 0.9V to 3.3V. When V_{IN2} falls outside the window between the undervoltage and overvoltage thresholds, $\overline{RST2}$ asserts and stays asserted for the reset timeout period after V_{IN2} falls within this window.
5, 6	N.C.	No Connect
7	$\overline{RST2}$	Active-Low, Open-Drain or Push-Pull Reset Output 2. For the open-drain version, connect $\overline{RST2}$ with a 10kΩ pull-up resistor.
8	$\overline{RST1}$	Active-Low, Open-Drain or Push-Pull Reset Output 1. For the open-drain version, connect $\overline{RST1}$ with a 10kΩ pull-up resistor.
-	EP	Exposed Pad. EP is internally connected to GND. Connect EP to the GND plane for improved heat dissipation. Do not use EP as the only ground connection.

Functional Diagrams

Functional Block Diagram



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Detailed Description

The MAX16193 is a dual-channel, 0.3% accurate window-detector supervisor circuit that monitors two supply voltages in a system. The MAX16193 offers factory-trimmed nominal input voltage levels and a factory-trimmed window between the undervoltage and overvoltage thresholds, from ±2% to ±5%. Contact Analog Devices for a threshold not listed in the *Ordering Information* table.

Reset Timeout Period

The active-low, open-drain reset outputs $\overline{RST1}$ and $\overline{RST2}$ assert low when the respective input voltage falls outside the factory-trimmed undervoltage and overvoltage threshold window. The corresponding reset output deasserts after the reset timeout period when the input voltage falls within the set window threshold. At power-up, resets stay asserted for the reset timeout period once V_{DD} is above the UVLO. The reset output is available in a factory-programmable open-drain or push-pull option. The reset output with open-drain configuration requires a pullup resistor. See *Figure 1* for more details.

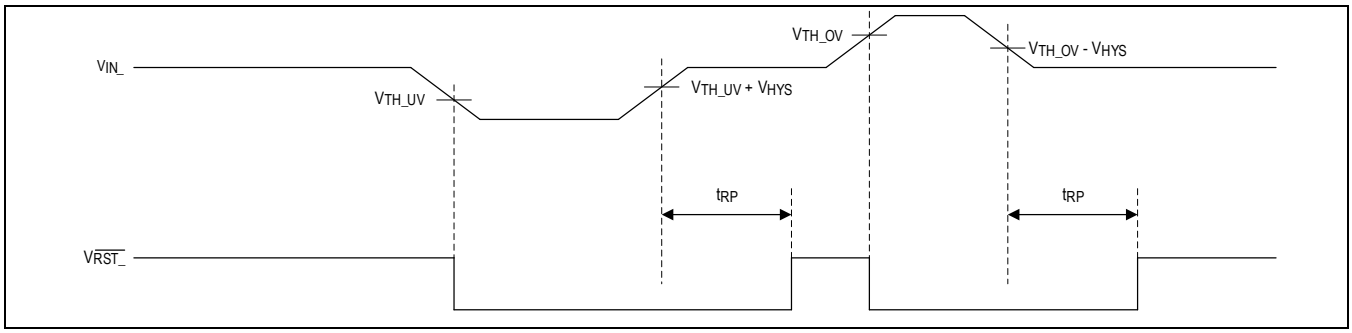


Figure 1. Reset Output Timing Diagram

Applications Information

Setting Input Thresholds and Hysteresis

The MAX16193 monitors a system supply voltage for undervoltage/overvoltage window threshold. Depending on the system supply tolerance requirement, the undervoltage/overvoltage thresholds can be factory-trimmed from ±2% to ±5% with respect to the selected nominal input threshold voltage. The following is a detailed calculation of how to determine the undervoltage/overvoltage threshold levels with ±0.3% threshold accuracy.

$V_{IN_NOM} = 0.9V$

$TOL = ±3\%$

$V_{UVTH} = V_{IN_NOM} (1 - 3\%) = 0.9V \times (1 - 0.03) = 0.873V$

$V_{OVTH} = V_{IN_NOM} (1 + 3\%) = 0.9V \times (1 + 0.03) = 0.927V$

Where V_{IN_NOM} is the selected nominal input threshold voltage, TOL is the input tolerance, V_{UVTH} is undervoltage threshold voltage, and V_{OVTH} is the overvoltage threshold voltage.

The MAX16193 monitors the supply voltage with ±0.3% accuracy over the operating temperature and supply range. The accuracy range is shown as follows:

$V_{UVTH_A} = V_{IN_NOM} (1 - 3\% \pm 0.3\%)$

$V_{OVTH_A} = V_{IN_NOM} (1 + 3\% \pm 0.3\%)$

Where V_{UVTH_A} is the undervoltage threshold accuracy range and V_{OVTH_A} is the overvoltage threshold accuracy range. See *Figure 2* for details.

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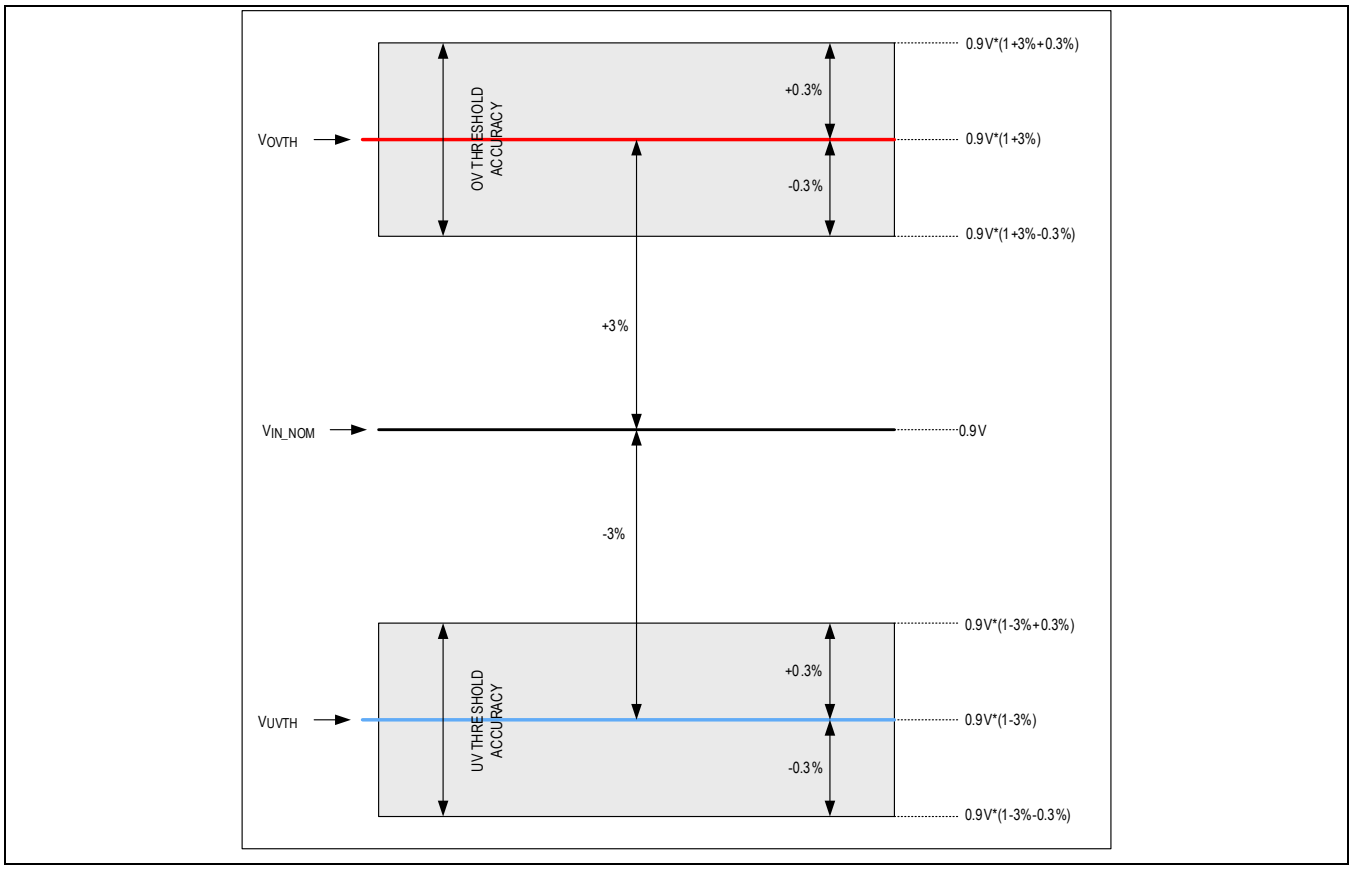


Figure 2. Undervoltage/Overvoltage Threshold Accuracy

Hysteresis adds noise immunity to the voltage monitors and prevents oscillation due to repeated triggering when the monitored voltage is near the threshold trip voltage.

Use the following equation to calculate the threshold hysteresis:

V_{IN_NOM} = 0.9V

Hysteresis = 0.15%

V_{HYST} = 0.9V x 0.15% = 0.00135V

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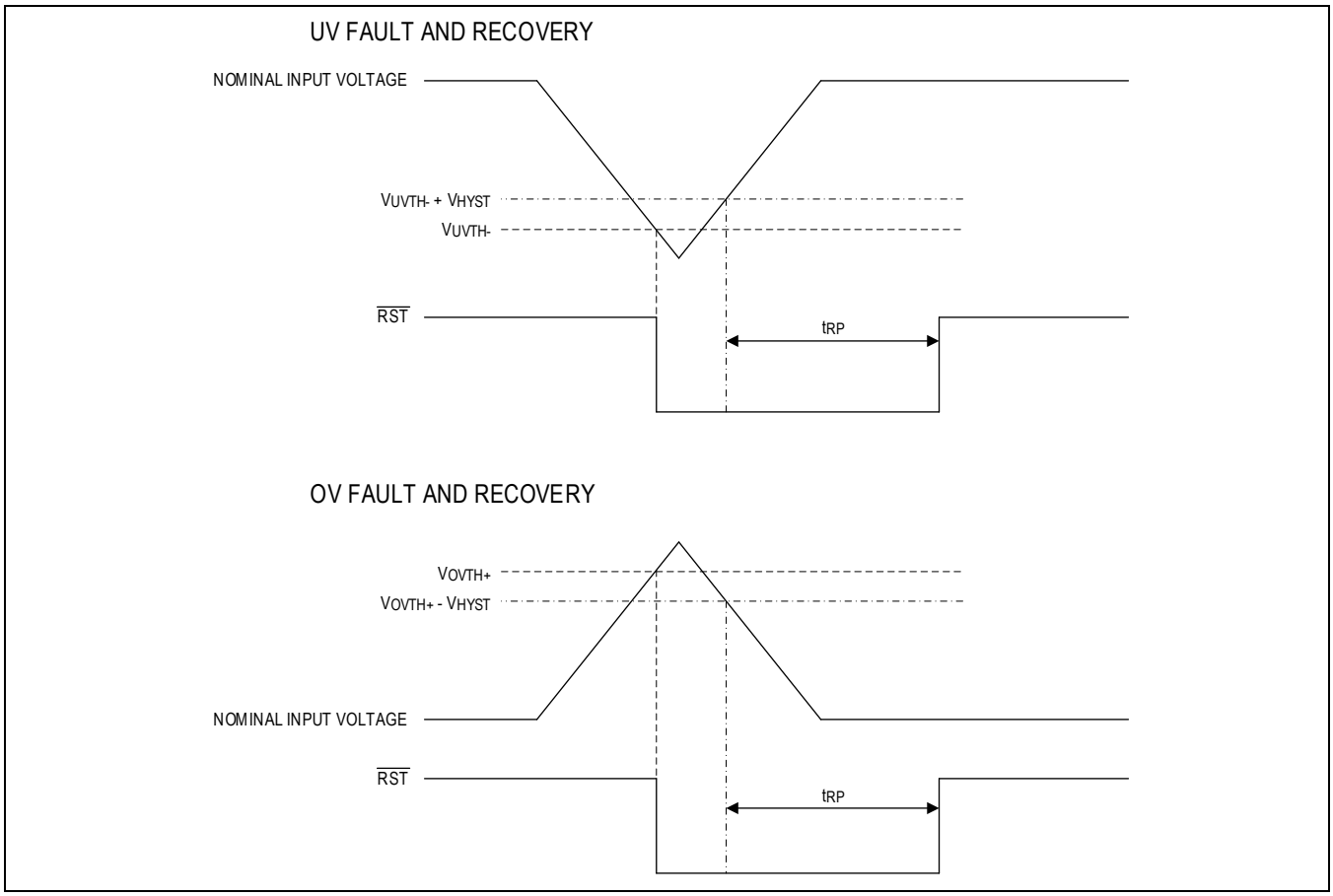


Figure 3. Undervoltage/Overvoltage Threshold Hysteresis

Power-Supply Bypassing/Noise Immunity

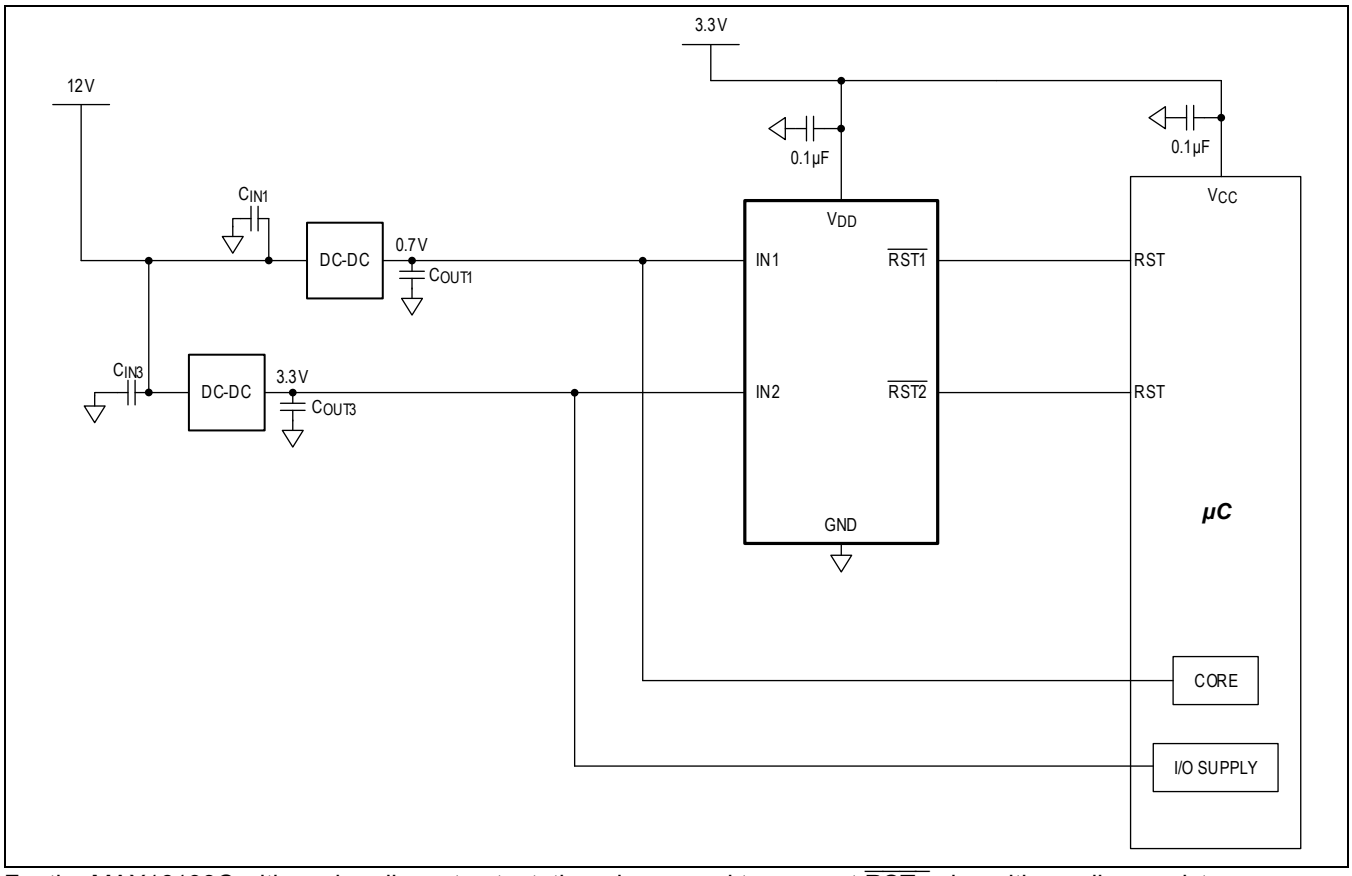
The MAX16193 operates from a 1.7V to 5.5V supply. Bypass V_{DD} to ground with a 0.1µF capacitor as close to the device as possible. An additional capacitor improves transient immunity.

Selector Guide Table

PART NUMBER	IN1/IN2 THRESHOLD VOLTAGE (V/V)	IN1/IN2 TOLERANCE (%/%)	IN1/IN2 ACCURACY (%/%)	IN1/IN2 HYSTERESIS (%/%)	RESET OUTPUT	RESET TIMEOUT
MAX16193ATA00/VY+T	0.9/3.280	4/3	0.3/0.3	0.15/0.15	Open Drain	10ms
MAX16193BATA00+T	0.9/3.280	4/3	0.3/0.3	0.15/0.15	Open Drain	10ms
MAX16193BATA01+T	0.9/1.1	2.40/2.40	0.3/0.3	0.15/0.15	Open Drain	< 50µs
MAX16193CATA00+T	0.9/3.280	4/3	0.3/0.3	0.15/0.15	Push-Pull	10ms

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Typical Application Circuit



For the MAX16193C with push-pull reset output, there is no need to connect $\overline{RST_}$ pins with a pull-up resistor.

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX16193ATA00/VY+T	-40°C to +125°C	8 TDFN (T823Y+3C)
MAX16193BATA00+T	-40°C to +125°C	8 TDFN (T823+3C)
MAX16193BATA01+T	-40°C to +125°C	8 TDFN (T823+3C)
MAX16193CATA00+T	-40°C to +125°C	8 TDFN (T823+3C)

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

/V Denotes an automotive qualified part.

Y = Side-wettable package.

Chip Information

PROCESS: BiCMOS

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	03/22	Release for Market Intro	—
1	09/23	Updated General Description, Applications, Benefits and Features, Absolute Maximum Ratings, Package Information Table, Electrical Characteristics, Typical Operating Characteristics, Selector Guide Table, Typical Application Circuit, and Ordering Information	1-10
2	7/26	Added exposed pad details in the Benefits and Features and Pin Descriptions sections; updated Global Conditions, Electrical Characteristics, Pin Configurations, Selector Guide Table, and Ordering Information	1, 2, 3, 5, 6, 9, 10

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