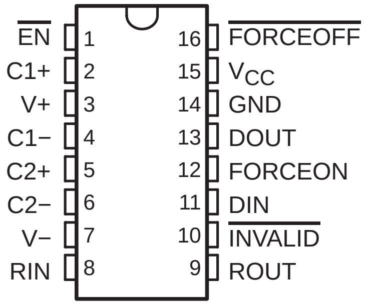
SN65C3221-Q1
3-V TO 5.5-V SINGLE-CHANNEL RS-232 COMPATIBLE LINE DRIVER/RECEIVER

- **Qualified for Automotive Applications**
- **Operates With 3-V to 5.5-V V_{CC} Supply**
- **Operates Up To 1 Mbit/s**
- **Low Standby Current . . . 1 μA Typical**
- **External Capacitors . . . 4 × 0.1 μF**
- **Accepts 5-V Logic Input With 3.3-V Supply**
- **RS-232 Bus-Pin ESD Protection Exceeds ±15 kV Using Human-Body Model (HBM)**
- **Auto-Powerdown Feature Automatically Disables Drivers for Power Savings**
- **Applications**
  - **Battery-Powered, Hand-Held, and Portable Equipment**
  - **PDAs and Palmtop PCs**
  - **Notebooks, Sub-Notebooks, and Laptops**
  - **Digital Cameras**
  - **Mobile Phones and Wireless Devices**

DB or PW PACKAGE
(TOP VIEW)



description/ordering information

The SN65C3221 consists of one line driver, one line receiver, and a dual charge-pump circuit with ±15-kV ESD protection pin to pin (serial-port connection pins, including GND). This device provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. This device operates at data signaling rates up to 1 Mbit/s and a driver output slew rate of 24 V/μs to 150 V/μs.

Flexible control options for power management are available when the serial port is inactive. The auto-powerdown feature functions when FORCEON is low and $\overline{\text{FORCEOFF}}$ is high. During this mode of operation, if the device does not sense a valid RS-232 signal on the receiver input, the driver output is disabled. If $\overline{\text{FORCEOFF}}$ is set low and $\overline{\text{EN}}$ is high, both the driver and receiver are shut off, and the supply current is reduced to 1 μA. Disconnecting the serial port or turning off the peripheral drivers causes the auto-powerdown condition to occur. Auto-powerdown can be disabled when FORCEON and $\overline{\text{FORCEOFF}}$ are high. With auto-powerdown enabled, the device is activated automatically when a valid signal is applied to the receiver input. The $\overline{\text{INVALID}}$ output notifies the user if an RS-232 signal is present at the receiver input. $\overline{\text{INVALID}}$ is high (valid data) if the receiver input voltage is greater than 2.7 V or less than −2.7 V, or has been between −0.3 V and 0.3 V for less than 30 μs. $\overline{\text{INVALID}}$ is low (invalid data) if the receiver input voltage is between −0.3 V and 0.3 V for more than 30 μs. See Figure 5 for receiver input levels.

ORDERING INFORMATION[†]

T_A	PACKAGE[‡]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	TSSOP (PW)	Reel of 2000	SN65C3221IPWRQ1	3221Q1
	SSOP (DB)	Reel of 2000	SN65C3221IDBRQ	3221Q1

[†] For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.

[‡] Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.

Function Tables

EACH DRIVER

INPUTS				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	$\overline{\text{FORCEOFF}}$	VALID RIN RS-232 LEVEL		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	
L	L	H	No	Z	Powered off by auto-powerdown feature
H	L	H	No	Z	

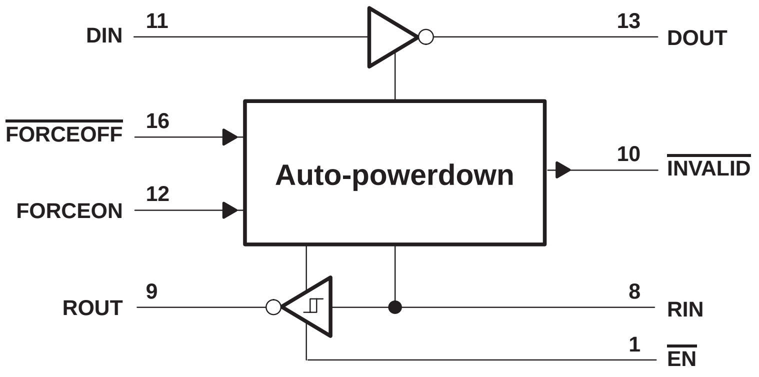
H = high level, L = low level, X = irrelevant, Z = high impedance

EACH RECEIVER

INPUTS			OUTPUT ROUT
RIN	$\overline{\text{EN}}$	VALID RIN RS-232 LEVEL	
L	L	X	H
H	L	X	L
X	H	X	Z
Open	L	No	H

H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = disconnected input or connected driver off

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)		−0.3 V to 6 V
Positive output supply voltage range, V+ (see Note 1)		−0.3 V to 7 V
Negative output supply voltage range, V− (see Note 1)		0.3 V to −7 V
Supply voltage difference, V+ − V− (see Note 1)		13 V
Input voltage range, V_I:	Driver ($\overline{\text{FORCEOFF}}$, FORCEON, $\overline{\text{EN}}$)	−0.3 V to 6 V
	Receiver	−25 V to 25 V
Output voltage range, V_O:	Driver	−10 V to 13.2 V
	Receiver ($\overline{\text{INVALID}}$)	−0.3 V to V_{CC} + 0.3 V
Package thermal impedance, θ_{JA} (see Note 2 and Note 3)		108°C/W
Operating virtual junction temperature, T_J		150°C
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to network GND.
2. Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4 and Figure 6)

				MIN	NOM	MAX	UNIT
	Supply voltage		V_{CC} = 3.3 V	3	3.3	3.6	V
			V_{CC} = 5 V	4.5	5	5.5	
V_{IH}	Driver and control high-level input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON, $\overline{\text{EN}}$	V_{CC} = 3.3 V	2			V
			V_{CC} = 5 V	2.4			
V_{IL}	Driver and control low-level input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON, $\overline{\text{EN}}$				0.8	V
V_I	Driver and control input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON		0		5.5	V
V_I	Receiver input voltage			−25		25	V
T_A	Operating free-air temperature			−40		85	°C

NOTE 4: Test conditions are C1−C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2−C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

PARAMETER			TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_I	Input leakage current	$\overline{\text{FORCEOFF}}$, FORCEON, $\overline{\text{EN}}$			±0.01	±1	μA
I_{CC}	Supply current (T_A = 25°C)	Auto-powerdown disabled	No load, $\overline{\text{FORCEOFF}}$ and FORCEON at V_{CC}		0.3	1	mA
		Powered off	No load, $\overline{\text{FORCEOFF}}$ at GND		1	10	μA
		Auto-powerdown enabled	No load, $\overline{\text{FORCEOFF}}$ at V_{CC}, FORCEON at GND, All RIN are open or grounded		1	10	

‡ All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

NOTE 4: Test conditions are C1−C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2−C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	DOUT at R_L = 3 kΩ to GND,	DIN = GND	5	5.4		V
V_{OL}	Low-level output voltage	DOUT at R_L = 3 kΩ to GND,	DIN = V_{CC}	−5	−5.4		V
I_{IH}	High-level input current	V_I = V_{CC}			±0.01	±1	μA
I_{IL}	Low-level input current	V_I at GND			±0.01	±1	μA
I_{OS}	Short-circuit output current‡	V_{CC} = 3.6 V,	V_O = 0 V		±35	±60	mA
		V_{CC} = 5.5 V,	V_O = 0 V		±35	±75	
r_o	Output resistance	V_{CC}, V+, and V− = 0 V,	V_O = ±2 V	300	10M		Ω
I_{off}	Output leakage current	$\overline{\text{FORCEOFF}}$ = GND	V_O = −10 V to +12 V, V_{CC} = 3 V to 3.6 V			±25	μA
			V_O = ±10 V, V_{CC} = 4.5 V to 5.5 V			±25	

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

‡ Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.

NOTE 4: Test conditions are C1−C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2−C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
	Maximum data rate (see Figure 1)	R_L = 3 kΩ	C_L = 1000 pF		250			kbit/s
			C_L = 250 pF,	V_{CC} = 3 V to 4.5 V	1000			
			C_L = 1000 pF,	V_{CC} = 4.5 V to 5.5 V	1000			
$t_{sk(p)}$	Pulse skew§	C_L = 150 pF to 2500 pF	R_L = 3 kΩ to 7 kΩ,	See Figure 2		100		ns
SR(tr)	Slew rate, transition region (see Figure 1)	V_{CC} = 3.3 V, R_L = 3 kΩ to 7 kΩ	C_L = 150 pF to 1000 pF		24		150	V/μs

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

§ Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

NOTE 4: Test conditions are C1−C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2−C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

ESD protection

TERMINAL		TEST CONDITIONS	TYP	UNIT
NAME	NO.			
DOUT	13	HBM	±15	kV

RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

PARAMETER		TEST CONDITIONS	MIN	TYP[†]	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −1 mA	V_{CC}−0.6 V	V_{CC}−0.1 V		V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 3.3 V		1.6	2.4	V
		V_{CC} = 5 V		1.9	2.4	
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 3.3 V	0.6	1.1		V
		V_{CC} = 5 V	0.8	1.4		
V_{hys}	Input hysteresis (V_{IT+} − V_{IT-})			0.5		V
I_{off}	Output leakage current	$\overline{\text{FORCEOFF}}$ = 0 V		±0.05	±10	μA
r_i	Input resistance	V_I = ±3 V to ±25 V	3	5	7	kΩ

[†] All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

NOTE 4: Test conditions are C1−C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2−C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4)

PARAMETER		TEST CONDITIONS	MIN	TYP[†]	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 150 pF, See Figure 3		150		ns
t_{PHL}	Propagation delay time, high- to low-level output	C_L = 150 pF, See Figure 3		150		ns
t_{en}	Output enable time	C_L = 150 pF, R_L = 3 kΩ, See Figure 4		200		ns
t_{dis}	Output disable time	C_L = 150 pF, R_L = 3 kΩ, See Figure 4		200		ns
$t_{sk(p)}$	Pulse skew[‡]	See Figure 3		50		ns

[†] All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

[‡] Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

NOTE 4: Test conditions are C1−C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2−C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

ESD protection

TERMINAL		TEST CONDITIONS	TYP	UNIT
NAME	NO.			
RIN	8	HBM	±15	kV

AUTO-POWERDOWN SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

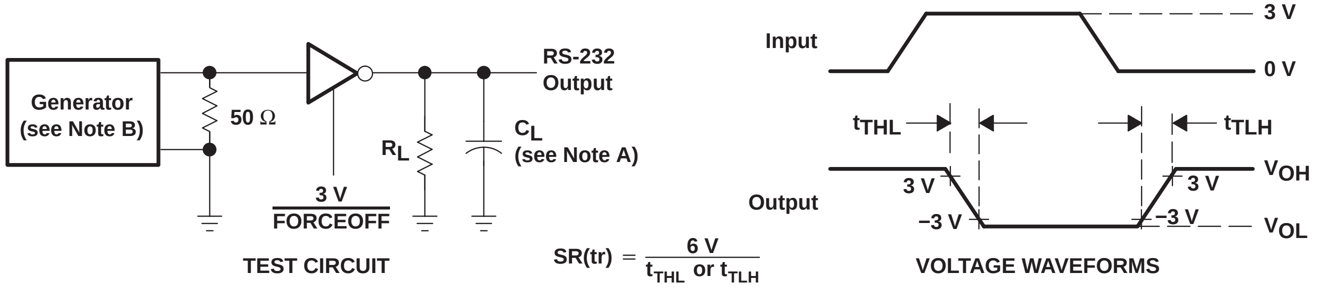
PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{T+(valid)}$	Receiver input threshold for $\overline{\text{INVALID}}$ high-level output voltage	FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V_{CC}		2.7	V
$V_{T-(valid)}$	Receiver input threshold for $\overline{\text{INVALID}}$ high-level output voltage	FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V_{CC}	−2.7		V
$V_{T(invalid)}$	Receiver input threshold for $\overline{\text{INVALID}}$ low-level output voltage	FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V_{CC}	−0.3	0.3	V
V_{OH}	$\overline{\text{INVALID}}$ high-level output voltage	I_{OH} = −1 mA, FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V_{CC}	V_{CC}−0.6		V
V_{OL}	$\overline{\text{INVALID}}$ low-level output voltage	I_{OL} = 1.6 mA, FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V_{CC}		0.4	V

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

PARAMETER		MIN	TYP†	MAX	UNIT
t_{valid}	Propagation delay time, low- to high-level output		1		µs
$t_{invalid}$	Propagation delay time, high- to low-level output		30		µs
t_{en}	Supply enable time		100		µs

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



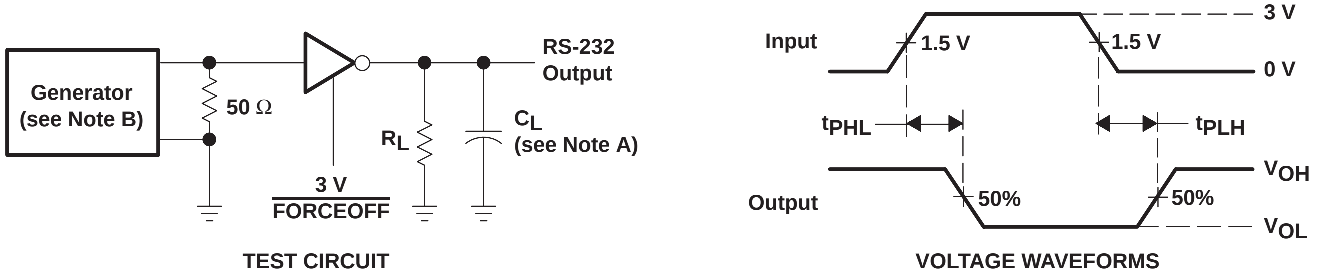
$$SR(tr) = \frac{6\ V}{t_{THL}\ or\ t_{TLH}}$$

TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Figure 1. Driver Slew Rate

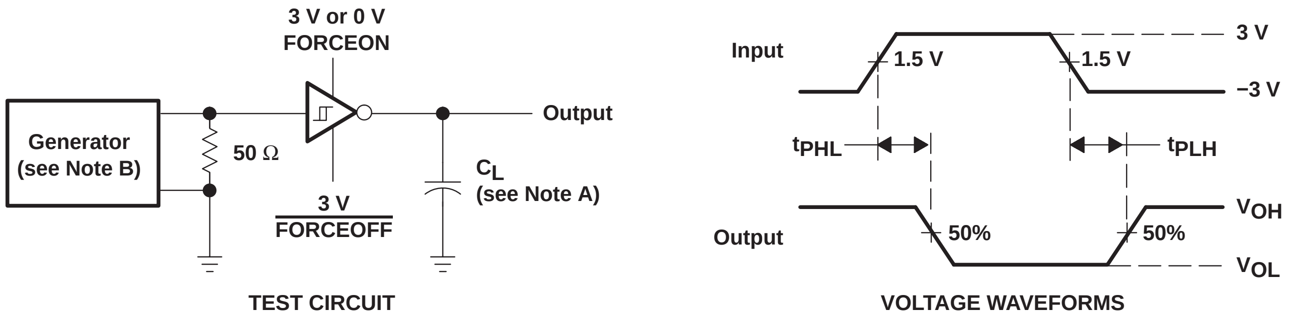


TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Figure 2. Driver Pulse Skew



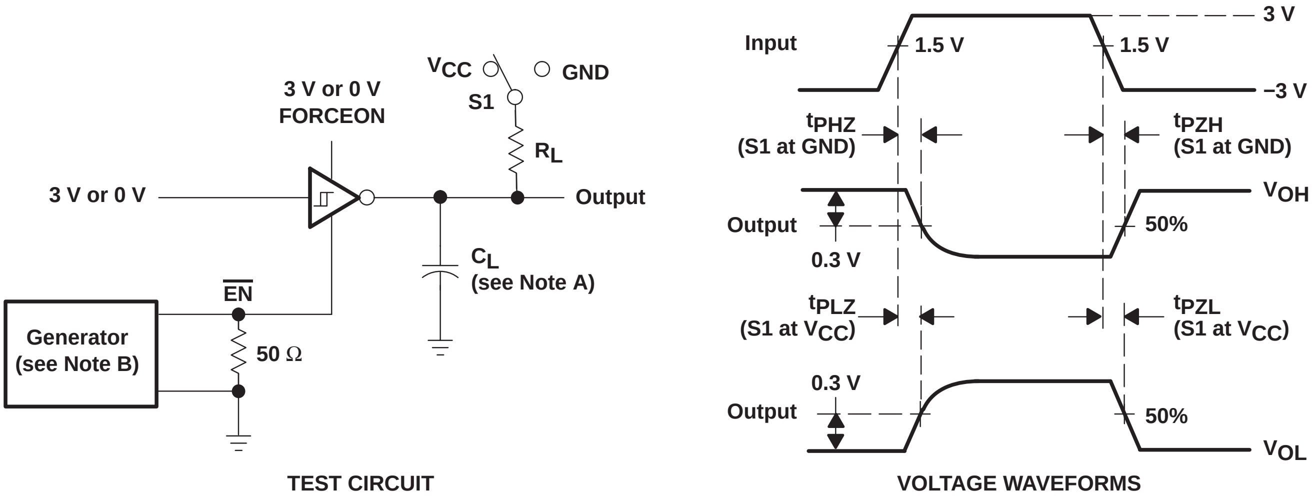
TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Figure 3. Receiver Propagation Delay Times

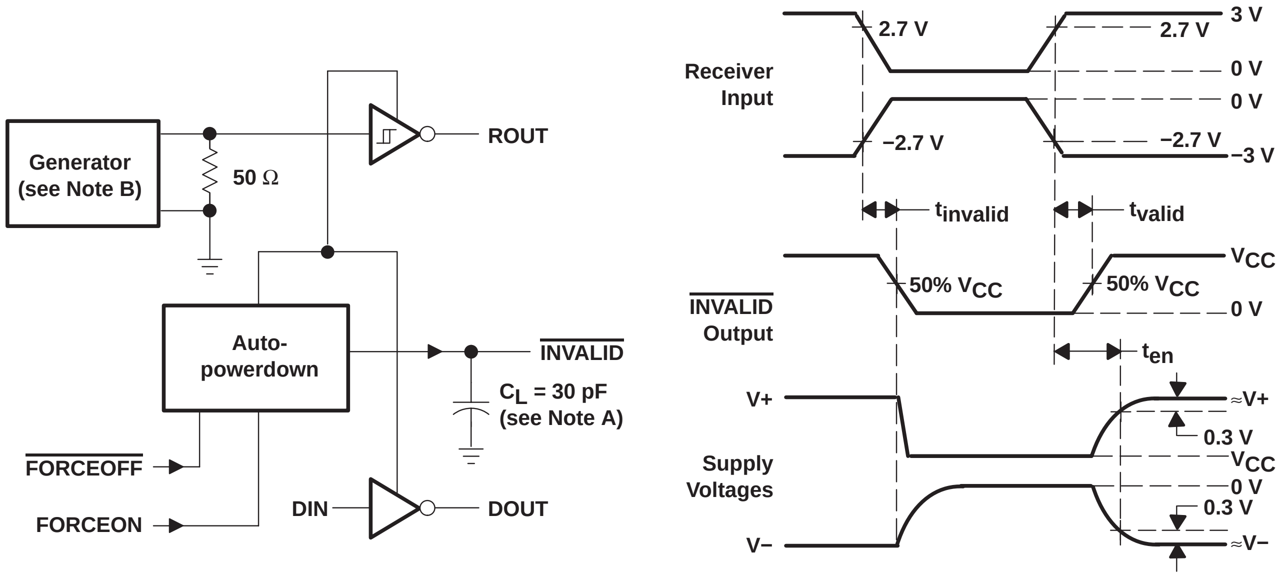
PARAMETER MEASUREMENT INFORMATION



NOTES:
- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.
- C. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- D. t_{PZL} and t_{PZH} are the same as t_{en}.

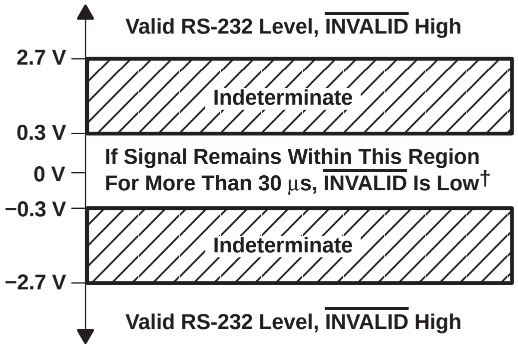
Figure 4. Receiver Enable and Disable Times

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

VOLTAGE WAVEFORMS

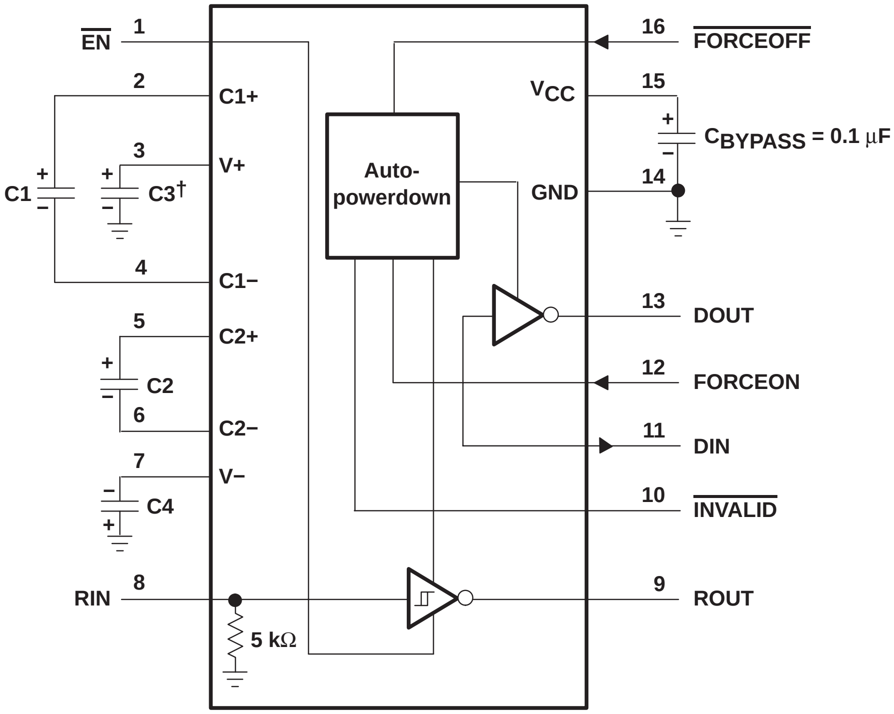


† Auto-powerdown disables drivers and reduces supply current to 1 µA.

NOTES:
A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 5 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Figure 5. INVALID Propagation Delay Times and Driver Enabling Time

APPLICATION INFORMATION



† C3 can be connected to V_{CC} or GND.

NOTE A: Resistor values shown are nominal.

V_{CC} vs CAPACITOR VALUES

V_{CC}	C1	C2, C3, and C4
3.3 V ± 0.3 V	0.1 μF	0.1 μF
5 V ± 0.5 V	0.047 μF	0.33 μF
3 V to 5.5 V	0.1 μF	0.47 μF

Figure 6. Typical Operating Circuit and Capacitor Values

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65C3221IPWRG4Q1	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-40 to 85	CB3221I
SN65C3221IPWRQ1	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CB3221I

[1] **Status:** For more details on status, see our product life cycle.

[2] **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[3] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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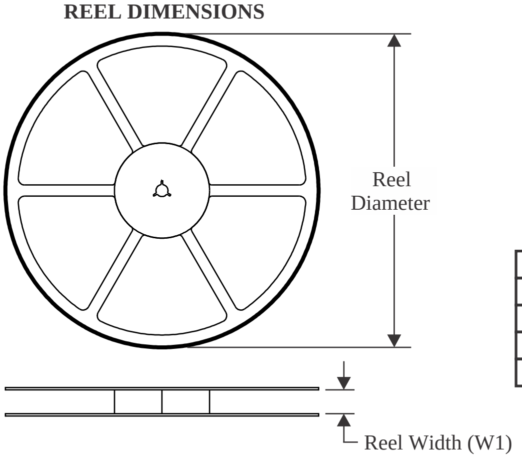
OTHER QUALIFIED VERSIONS OF SN65C3221-Q1 :

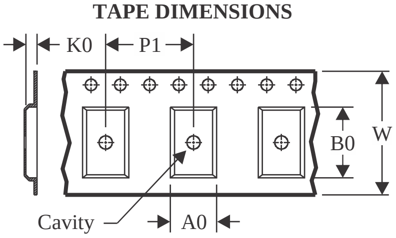
- Catalog : SN65C3221

NOTE: Qualified Version Definitions:

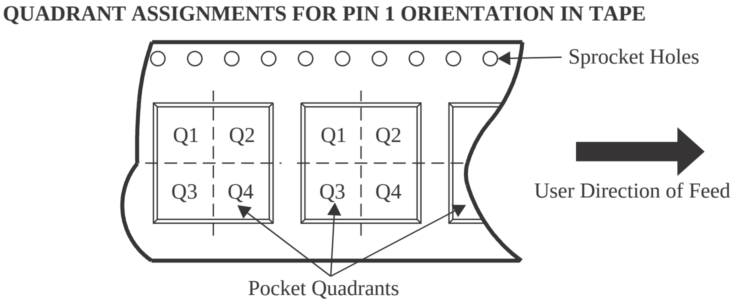
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION





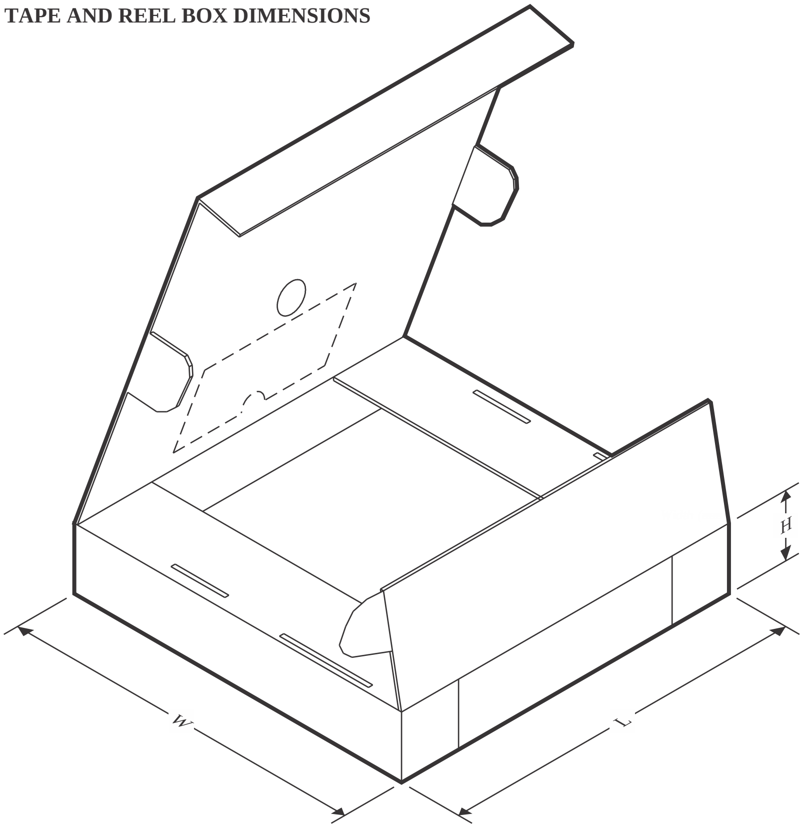
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

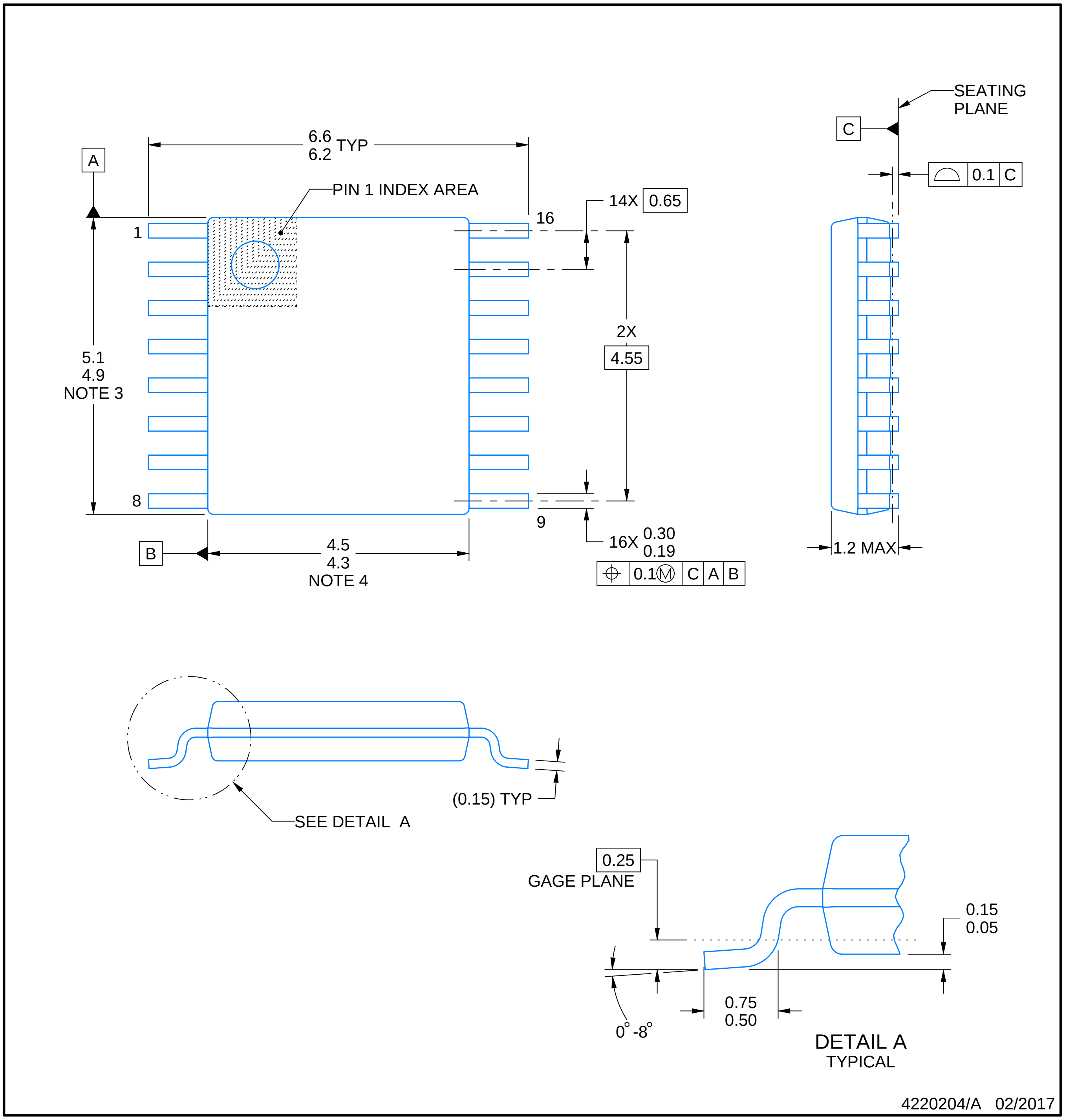
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65C3221IPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

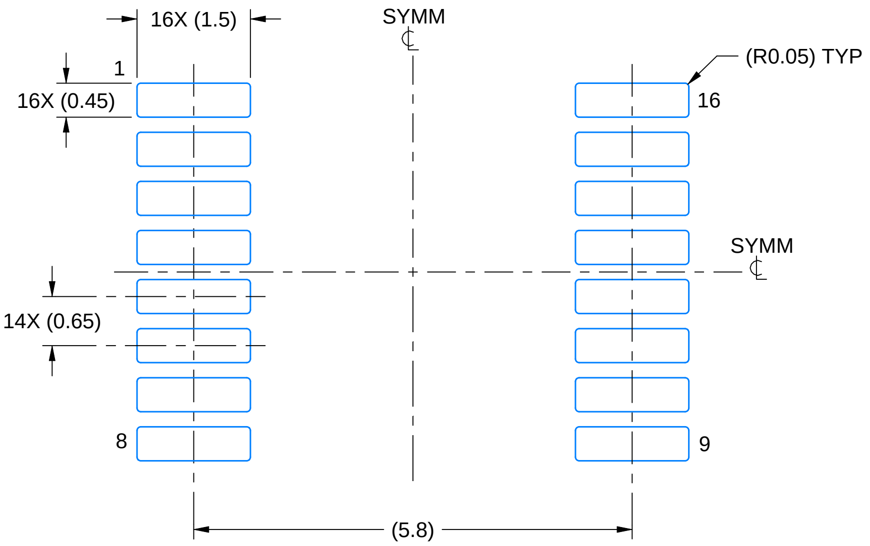
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65C3221IPWRQ1	TSSOP	PW	16	2000	356.0	356.0	35.0



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK DEFINED (PREFERRED)

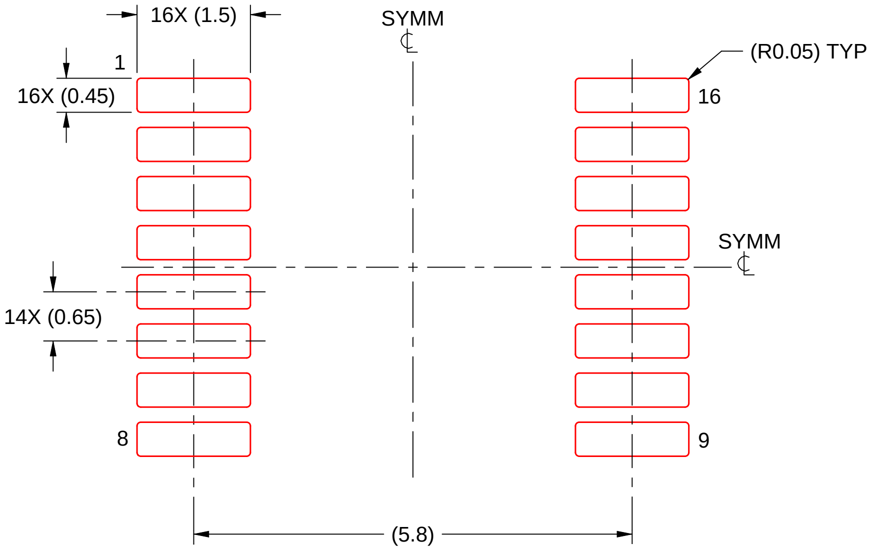
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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