# MOSFET – N-Channel, POWERTRENCH®
## 60 V

# FDD5612

### General Description

This N−Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers.

These MOSFETs feature faster switching and lower gate charge than other MOSFETs with comparable $R_{DS(ON)}$ specifications. The result is a MOSFET that is easy and safer to drive (even at very high frequencies), and DC/DC power supply designs with higher overall efficiency.

### Features

- 18 A, 60 V
  - $R_{DS(ON)}$ = 55 mΩ @ $V_{GS}$ = 10 V
  - $R_{DS(ON)}$ = 64 mΩ @ $V_{GS}$ = 6 V
- Optimized for Use in High Frequency DC/DC Converters
- Low Gade Charge
- Very Fast Switching
- This Device is Pb−Free and are RoHS Compliant

**ON Semiconductor®**

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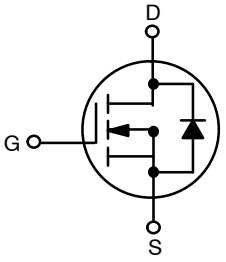
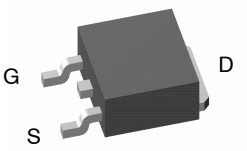
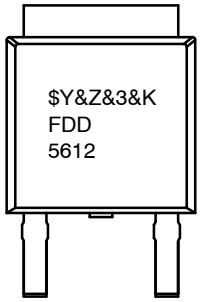



**DPAK3 (TO−252 3 LD)**
**CASE 369AS**

### MARKING DIAGRAM




| | |
|---|---|
| $Y | = ON Semiconductor Logo |
| &Z | = Assembly Plant Code |
| &3 | = Numeric Date Code |
| &K | = Lot Code |
| FDD5612 | = Specific Device Code |

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

## ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C, Unless otherwise noted)

| Symbol | Parameter | | Ratings | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain−Source Voltage | | 60 | V |
| $V_{GSS}$ | Gate−Source Voltage | | ±20 | V |
| $I_D$ | Drain Current − Continuous | $T_C$ = 25°C | 18 | A |
| | | $T_C$ = 100°C | 13 | |
| | | $T_A$ = 25°C (Note 1a) | 5.4 | |
| | | $T_A$ = 25°C (Note 1b) | 3.5 | |
| | Drain Current − Pulsed | | 100 | |
| $P_D$ | Maximum Power Dissipation | $T_C$ = 25°C | 42 | W |
| | | $T_C$ = 100°C | 21 | |
| | | $T_A$ = 25°C (Note 1a) | 3.8 | |
| | | $T_A$ = 25°C (Note 1b) | 1.6 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | −55 to +175 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## THERMAL CHARACTERISTICS

| Symbol | Parameter | Ratings | Unit |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction−to−Case | 3.5 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction−to−Ambient (Note 1a) | 40 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction−to−Ambient (Note 1b) | 96 | °C/W |

## PACKAGE MARKING AND ORDERING INFORMATION

| Part Number | Device | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|
| FDD5612 | FDD5612 | 13” | 16 mm | 2500 Units |

## ELECTRICAL CHARACTERISTICS ($T_A$ = 25°C unless otherwise noted)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **DRAIN−SOURCE AVALANCHE RATINGS** (Note 1) | | | | | | |
| $W_{DSS}$ | Single Pulse Drain−Source Avalanche Energy | $V_{DD}$ = 30 V, $I_D$ = 5.4 A | | | 90 | mJ |
| $I_{AR}$ | Maximum Drain−Source Avalanche Current | | | | 5.4 | A |
| **OFF CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain−Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 μA | 60 | | | V |
| $\Delta BV_{DSS}$ / $\Delta T_J$ | Breakdown Voltage Temperature Coefficient | $I_D$ = −250 μA, Referenced to 25°C | | 62 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 48 V, $V_{GS}$ = 0 V | | | 1 | μA |
| $I_{GSSF}$ | Gate−Body Leakage, Forward | $V_{GS}$ = 20 V, $V_{DS}$ = 0 V | | | 100 | nA |
| $I_{GSSR}$ | Gate−Body Leakage, Reverse | $V_{GS}$ = −20V, $V_{DS}$ = 0 V | | | −100 | nA |
| **ON CHARACTERISTICS** (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | 1 | 2.4 | 3 | V |
| $\Delta V_{GS(th)}$ / $\Delta T_J$ | Gate Threshold Voltage Temperature Coefficient | $I_D$ = 250 μA, Referenced to 25°C | | −6 | | mV/°C |

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted) (continued)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **ON CHARACTERISTICS** (Note 2) | | | | | | |
| $R_{DS(on)}$ | Static Drain–Source On–Resistance | $V_{GS}$ = 10 V, $I_D$ = 5.4 A<br>$V_{GS}$ = 6 V, $I_D$ = 5 A<br>$V_{GS}$ = 10 V, $I_D$ = 5.4 A, $T_J$ = 125°C | | 36<br>42<br>64 | 55<br>64<br>103 | mΩ |
| $I_{D(on)}$ | On–State Drain Current | $V_{GS}$ = 10 V, $V_{DS}$ = 5 V | 20 | | | A |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 5 V, $I_D$ = 5.4 A | | 15 | | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 30 V, $V_{GS}$ = 0 V, f = 1.0 MHz | | 660 | | pF |
| $C_{oss}$ | Output Capacitance | | | 79 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 36 | | pF |
| **SWITCHING CHARACTERISTICS** (Note 2) | | | | | | |
| $t_{d(on)}$ | Turn–On Delay Time | $V_{DD}$ = 30 V, $I_D$ = 1 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | | 8 | 16 | ns |
| $t_r$ | Turn–On Rise Time | | | 4 | 8 | ns |
| $t_{d(off)}$ | Turn–Off Delay Time | | | 24 | 38 | ns |
| $t_f$ | Turn–Off Fall Time | | | 4 | 8 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 30 V, $I_D$ = 5.4 A, $V_{GS}$ = 10 V | | 7.5 | 11 | nC |
| $Q_{gs}$ | Gate–Source Charge | | | 2.5 | | nC |
| $Q_{gd}$ | Gate–Drain Charge | | | 3 | | nC |
| **DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS** | | | | | | |
| $I_S$ | Source Current (Body Diode) | $T_C$ = 25°C | | | 18 | A |
| $V_{SD}$ | Drain–Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 2.7 A (Note 2) | | 0.8 | 1.2 | V |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is the sum of the junction–to–case and case–to–ambient thermal resistance where the case thermal reference is defined as the drain tab. $R_{\theta JA}$ is the guaranteed design while $R_{\theta JA}$ is determined by the user's design. $R_{\theta JA}$ has been used to determine some of the maximum ratings.

a) $R_{\theta JA}$ = 40°C/W when mounted on a 1in$^2$ pad of 2 oz copper

b) $R_{\theta JA}$ = 96°C/W when mounted on a 0.076 in$^2$ pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

## TYPICAL CHARACTERISTICS

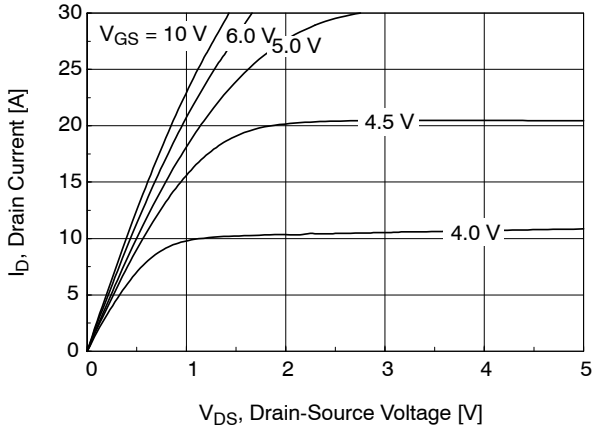



**Figure 1. On-Region Characteristics**

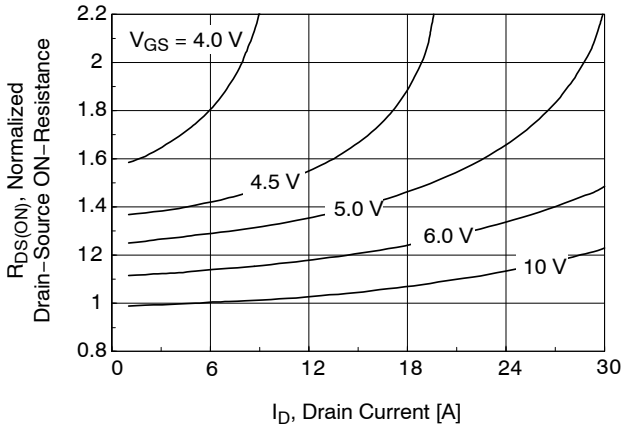



**Figure 2. On−Resistance Variation with Drain Current and Gate Voltage**

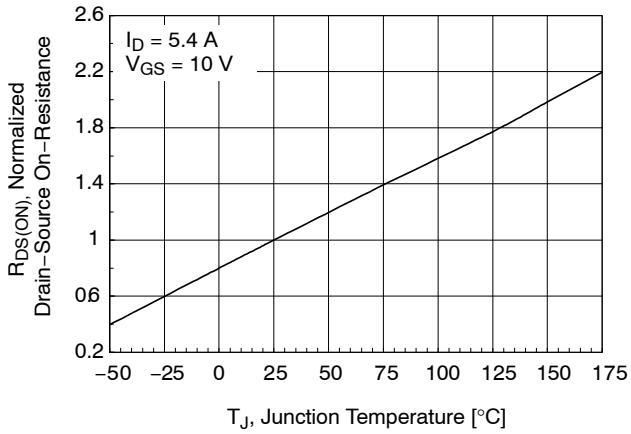



**Figure 3. On-Resistance Variation with Temperature**

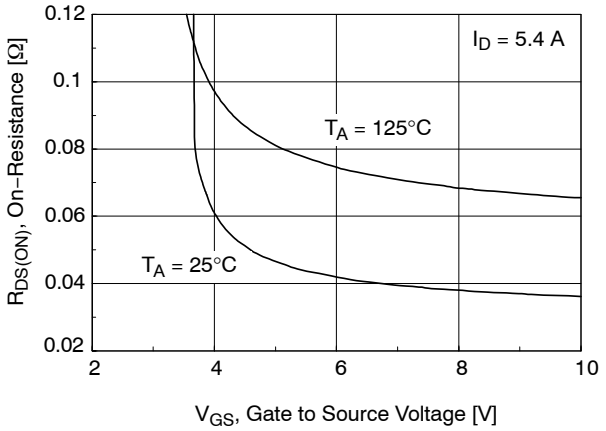



**Figure 4. On−Resistance Variation with Gate−to−Source Voltage**

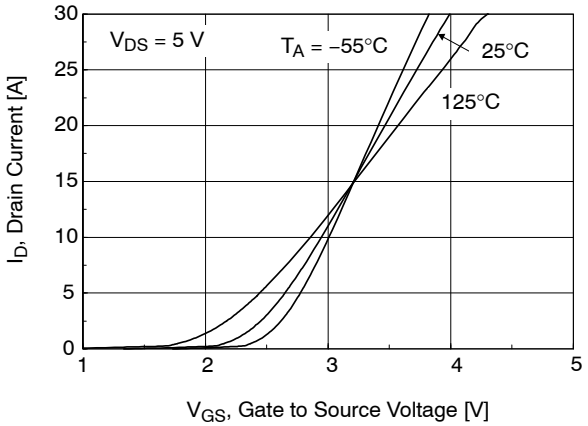



**Figure 5. Transfer Characteristics**

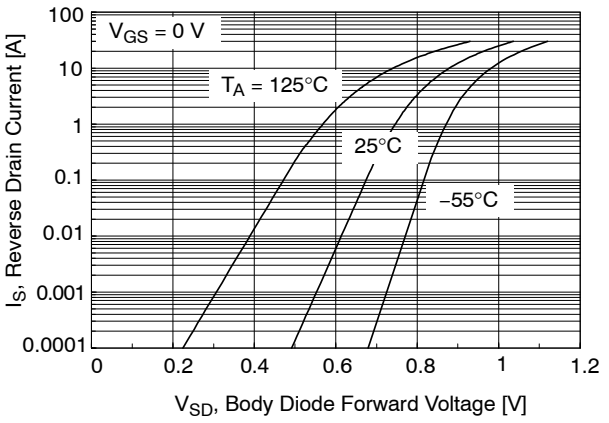



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature**

## TYPICAL CHARACTERISTICS (continued)

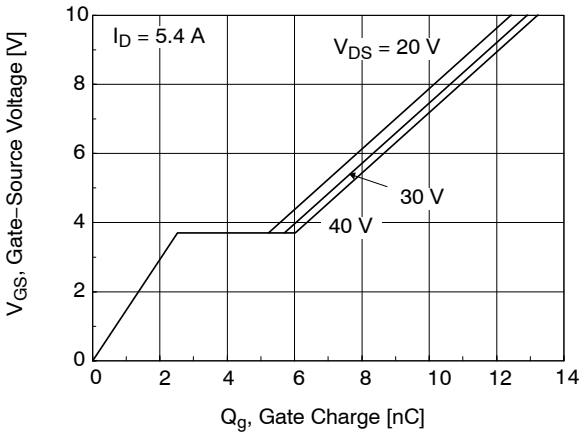



**Figure 7. Gate Charge Characteristics**

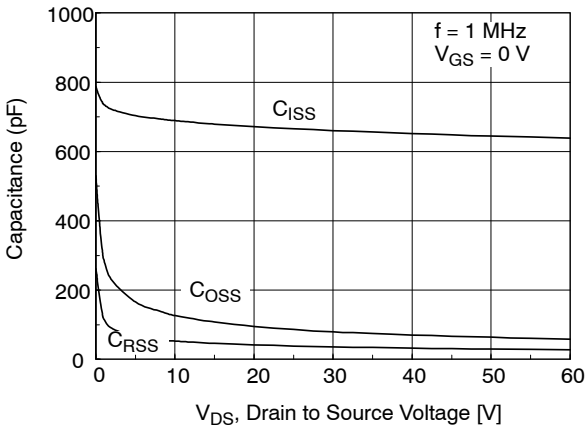



**Figure 8. Capacitance Characteristics**

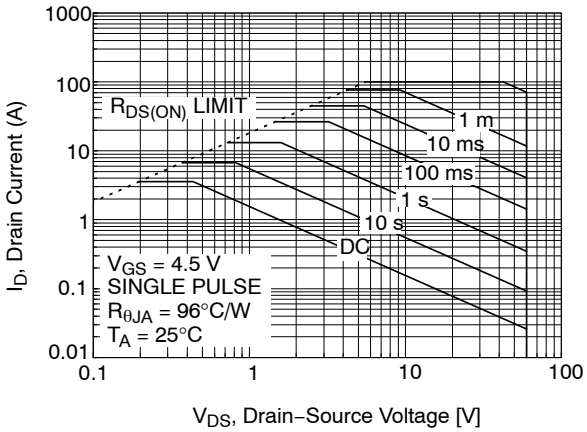



**Figure 9. Maximum Safe Operating Area**

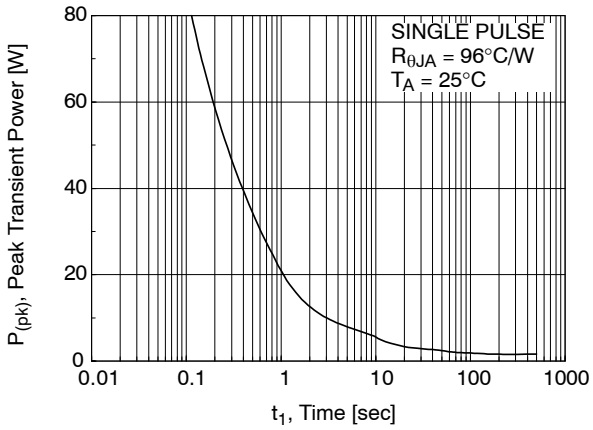



**Figure 10. Single Pulse Maximum Power Dissipation**

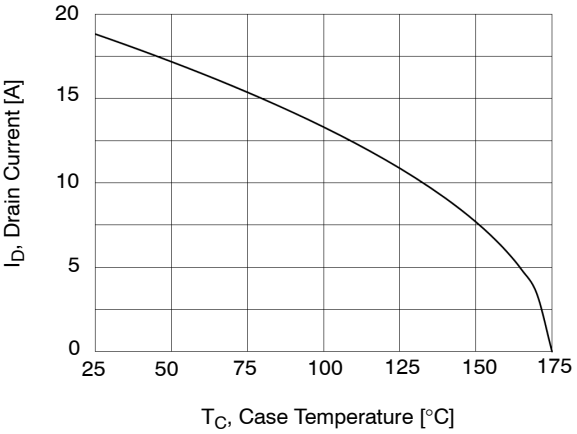



**Figure 11. Maximum Drain Current vs. Case Temperature**

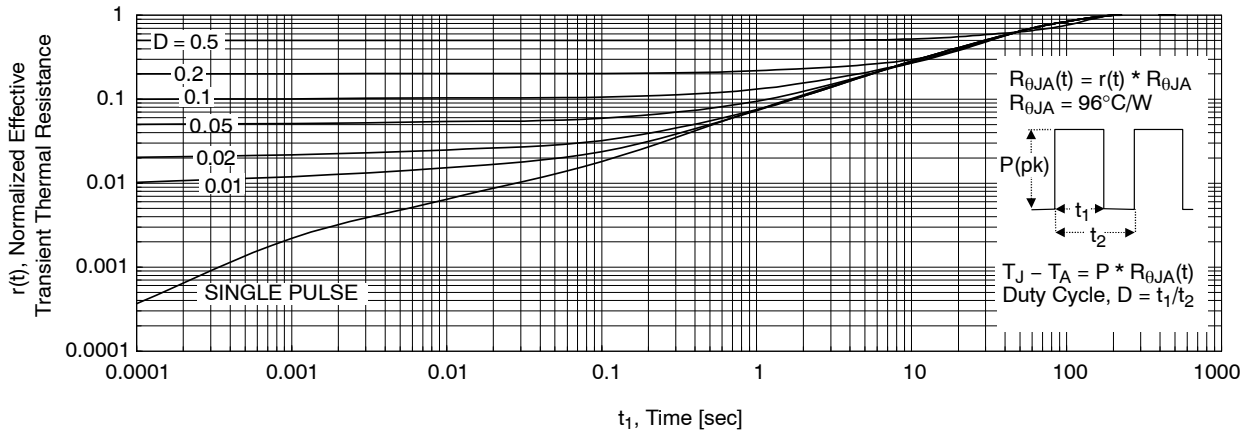
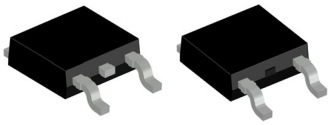



**Figure 12. Transient Thermal Response Curve**

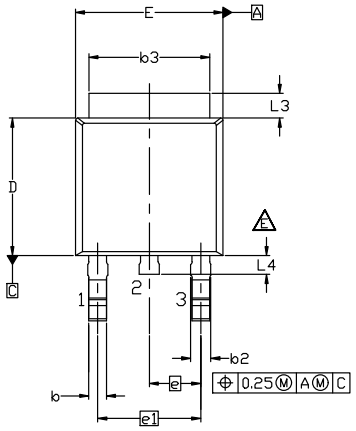
NOTES:

3. Thermal characterization performed using the conditions described in Note 1b.
4. Transient thermal response will change depending on the circuit board design.

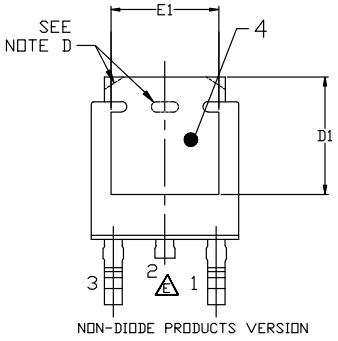


## DPAK3 6.10x6.54x2.29, 4.57P
CASE 369AS
ISSUE B

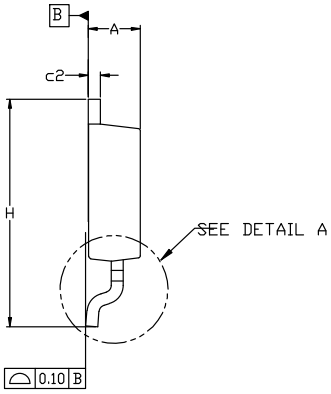
DATE 20 DEC 2023



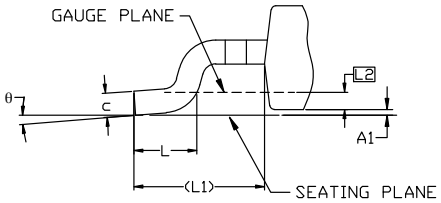

NON-DIODE PRODUCTS VERSION




NON-DIODE PRODUCTS VERSION

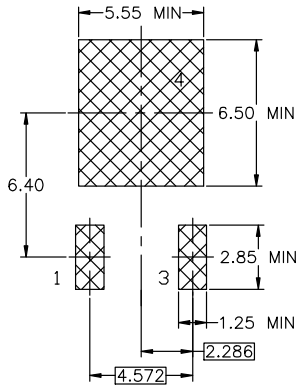



NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE F, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2018.
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
E) FOR DIODE PRODUCTS, L4 IS 0.25 MM MAX PLASTIC BODY STUB WITHOUT CENTER LEAD.
F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.




DETAIL A
(ROTATED -90°)
SCALE: 12X

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 2.18 | 2.29 | 2.39 |
| A1 | 0.00 | – | 0.127 |
| b | 0.64 | 0.77 | 0.89 |
| b2 | 0.76 | 0.95 | 1.14 |
| b3 | 5.21 | 5.34 | 5.46 |
| c | 0.45 | 0.53 | 0.61 |
| c2 | 0.45 | 0.52 | 0.58 |
| D | 5.97 | 6.10 | 6.22 |
| D1 | 5.21 | --- | --- |
| E | 6.35 | 6.54 | 6.73 |
| E1 | 4.32 | --- | --- |
| e | 2.286 BSC | | |
| e1 | 4.572 BSC | | |
| H | 9.40 | 9.91 | 10.41 |
| L | 1.40 | 1.59 | 1.78 |
| L1 | 2.90 REF | | |
| L2 | 0.51 BSC | | |
| L3 | 0.89 | 1.08 | 1.27 |
| L4 | --- | --- | 1.02 |
| θ | 0° | --- | 10° |




LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

### GENERIC MARKING DIAGRAM*


*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

| | | |
|---|---|---|
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| **DESCRIPTION:** | **DPAK3 6.10x6.54x2.29, 4.57P** | **PAGE 1 OF 1** |

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