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TEXAS INSTRUMENTS

TLIN2024-Q1 Fault Protected Quad Local Interconnect Network (LIN) Transceiver with Dominant State Timeout

1 Features

- AEC Q100 Qualified for automotive applications
  - Temperature: –40 to 125°C ambient
  - HBM Classification level: ±8 kV
  - CDM Classification level: ±1.5 kV
- Compliant to LIN2.0, LIN2.1, LIN2.2, LIN2.2A and ISO/DIS 17987–4.2
- Conforms to SAE J2602 recommended practice for LIN
- Supports 12 V and 24 V battery applications
- LIN transmit data rate up to 20 kbps
- Wide operating ranges
  - 4 V to 48 V supply voltage
  - ±60 V LIN bus fault protection
  - Sleep mode: ultra-low current consumption allows wake up event from:
    - LIN bus
    - Local wake up through EN
  - Power up and down glitch free operation
- Protection features:
  - Under voltage protection on V_{SUP}
  - TXD Dominant time out protection (DTO)
  - Thermal shutdown protection
  - Unpowered node or ground disconnection failsafe at system level.
- 3.5 mm × 5.5 mm QFN package with improved automated optical inspection (AOI) capability

2 Applications

- Body Electronics and Lighting
- Infotainment and Cluster
- Hybrid Electric Vehicles and Power Train Systems
- Passive Safety

3 Description

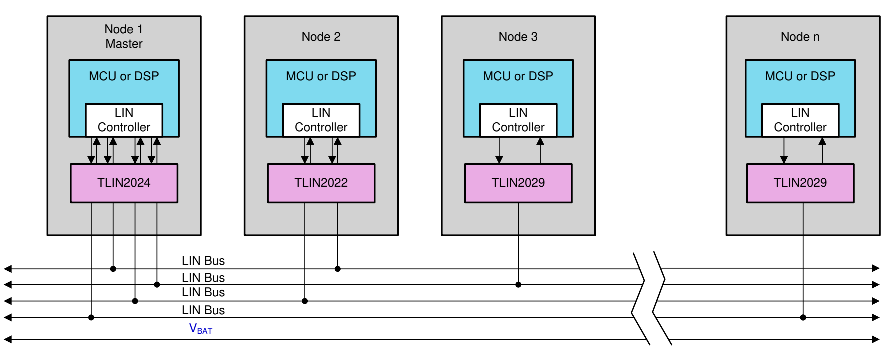
The TLIN2024-Q1 device is a quad Local Interconnect Network (LIN) physical layer transceiver, which integrates wake up and protection features, compliant to LIN2.0, LIN2.1, LIN2.2, LIN2.2A and ISO/DIS 17987–4.2 standards. LIN is a single wire bidirectional bus typically used for low speed in-vehicle networks using data rates up to 20 kbps. The LIN receiver supports data rates up to 100 kbps for in-line programming. The TLIN2024-Q1 has two separate dual LIN transceiver blocks. The $V_{SUP1/2}$ control separate dual transceiver blocks. The TLIN2024-Q1 converts the LIN protocol data stream on the TXD input into a LIN bus signal using a current-limited wave-shaping driver which reduces electromagnetic emissions (EME). The receiver converts the data stream to logic level signals that are sent to the microprocessor through the open-drain RXD pin. Ultra-low current consumption is possible using the sleep mode which allows wake up via LIN bus or EN pin. The integrated resistor, electrostatic discharge (ESD) protection, and fault protection allow designers to save board space in their applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLIN2024-Q1	VQFN (24)	3.50 mm × 5.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2018) to Revision B **Page**

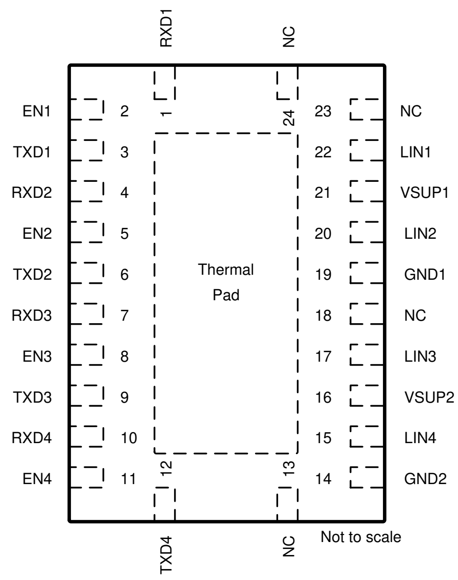
- Changed *Feature* From: HBM Classification level: ±6 kV To: HBM Classification level: ±8 kV ... 1
- Changed *Feature* From: ±58 V LIN bus fault protection To: ±60 V LIN bus fault protection ... 1
- Changed the $V_{SUP1/2}$ MAX value From: 58 V To: 60 V in the Absolute Maximum Ratings. ... 4
- Changed the V_{LIN} values From: -58 V to 58 V To: -60 V to 60 V in the Absolute Maximum Ratings. ... 4
- Changed the V_{LOGIC} MAX value From: 5.5 V To: 6 V in the Absolute Maximum Ratings. ... 4
- Deleted J2962-1 ESD and ISO Pulses from ESD Ratings ... 4
- Changed the HBM value from ±6000 to ±8000 in the ESD Ratings ... 4
- Changed IEC 61000-4-2 to IEC 62228-2 and made three rows, two for contact and added indirect ESD ... 4
- Changed I_{CC} to I_{SUP} ... 5
- Changed the Supply Current 4 V Sleep Mode TYP values From: 20 µA To: 7 µA and the MAX value From: 40 µA To: 20 µA ... 5
- Changed the Supply Current 14 V Sleep Mode MAX value From: 60 µA To: 30 µA ... 5
- Changed the C_{LINPIN} MAX value From: 45 pF To: 25 pF ... 6
- Added TEST CONDITION: VSUP = 14 V to C_{LINPIN} ... 6
- Changed From ±58 V To: ±60 V in Overview Section ... 20
- Cleaned up wording in Overview section second paragraph ... 20

Changes from Original (April 2018) to Revision A **Page**

- Changed R_{SLAVE} Typical value from 30 kΩ to 45 kΩ in the Electrical Characteristics ... 6

5 Pin Configuration and Functions

RGY Package
24-Pin RGY (VQFN)
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
RXD1	1	O	Channel 1 RXD Output (open-drain) interface reporting state of LIN bus voltage
EN1	2	I	Channel 1 Enable Input
TXD1	3	I	Channel 1 TXD input interface to control state of LIN output
RXD2	4	O	Channel 2 RXD Output (open-drain) interface reporting state of LIN bus voltage
EN2	5	I	Channel 2 Enable Input
TXD2	6	I	Channel 2 TXD input interface to control state of LIN output
RXD3	7	O	Channel 3 RXD Output (open-drain) interface reporting state of LIN bus voltage
EN3	8	I	Channel 3 Enable Input
TXD3	9	I	Channel 3 TXD input interface to control state of LIN output
RXD4	10	O	Channel 4 RXD Output (open-drain) interface reporting state of LIN bus voltage
EN4	11	I	Channel 4 Enable Input
TXD4	12	I	Channel 4 TXD input interface to control state of LIN output
GND2	14	GND	Ground pin for Channels 3 and 4
LIN4	15	I/O	Channel 4 LIN Bus single-wire transmitter and receiver
V_{SUP2}	16	Supply	Channels 3 and 4 Supply Voltage (connected to battery in series with external reverse blocking diode
LIN3	17	I/O	Channel 3 LIN Bus single-wire transmitter and receiver
GND1	19	GND	Ground pin for Channels 1 and 2
LIN2	20	I/O	Channel 2 LIN Bus single-wire transmitter and receiver
V_{SUP1}	21	Supply	Channels 1 and 2 Supply Voltage (connected to battery in series with external reverse blocking diode
LIN1	22	I/O	Channel 1 LIN Bus single-wire transmitter and receiver
NC	13, 18, 23, 24	–	Not Connected

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

Symbol	Parameter	MIN	MAX	UNIT
$V_{SUP1/2}$	Supply voltage range (ISO/DIS 17987 Param 10)	–0.3	60	V
V_{LIN}	LIN Bus input voltage (ISO/DIS 17987 Param 82)	–60	60	V
V_{LOGIC}	Logic Pin Voltage (RXDx, TXDx, ENx)	–0.3	6	V
T_A	Ambient temperature range	–40	125	°C
T_J	Junction temperature range	–55	150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

ESD Ratings				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM) RXD, EN Pins, per AEC Q100-002[1]		±4000	V
		Human body model (HBM) LIN and V_{SUP}, per AEC Q100-002[2]		±8000	
		Charged device model (CDM), per AEC Q100-011	All terminals	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) LIN bus a stressed with respect to GND.

6.3 ESD Ratings - IEC

ESD and Surge Protection Ratings			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge, LIN and V_{SUP} to GND, per IEC 62228-2	Contact discharge, without LIN bus filter capacitor[1]	±5000	V
		Contact discharge, with LIN bus filter capacitor[1]	±9000	V
		Indirect ESD[1]	±15000	V

(1) IEC 62228-2 ESD test performed by a third party. Different system level configurations may lead to different results

6.4 Thermal Information

THERMAL METRIC[1]		TLIN2024 RGY (QFN) 24-PINS	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	34.3	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	30.8	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	13.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	13.3	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

6.5 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER - DEFINITION		MIN	NOM	MAX	UNIT
$V_{SUP1/2}$	Supply voltage	4		48	V
V_{LINx}	LINx Bus input voltage	0		45	V
V_{LOGIC}	Logic Pin Voltage (RXDx, TXDx, ENx)	0		5.5	V

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER - DEFINITION		MIN	NOM	MAX	UNIT
TSD	Thermal shutdown edge	165			°C
$TSD_{(HYS)}$	Thermal shutdown hysteresis		15		°C

6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply						
V_{SUP}	Operational supply voltage (ISO/DIS 17987 Param 10, 53)	Device is operational beyond the LIN defined nominal supply voltage range See Figure 8 and Figure 9	4		45	V
	Nominal supply voltage (ISO/DIS 17987 Param 10, 53): Normal Mode: Ramp VSUP while LIN signal is a 10 kHZ Square Wave with 50 % duty cycle and 36V swing. Watch RXD	Normal and Standby Modes Normal Mode: Ramp V_{SUP} while LIN signal is a 10 kHZ Square Wave with 50 % duty cycle and 36V swing. See Figure 8 and Figure 9	4		45	V
		Sleep Mode	4		45	V
UV_{SUP}	Under voltage VSUP threshold		2.9		3.85	V
UV_{HYS}	Delta hysteresis voltage for VSUP under voltage threshold			0.2		V
I_{SUP}	Supply Current (1)	Normal Mode: EN = High, bus dominant: total bus load where R_{LIN} > 500 Ω and C_{LIN} < 10 nF (See Figure 14)		3	15	mA
		Standby Mode: EN = Low, bus dominant: total bus load where R_{LIN} > 500 Ω and C_{LIN} < 10 nF (See Figure 14)		2.2	8	mA
I_{SUP}	Supply Current (1)	Normal Mode: EN = High, Bus Recessive: LIN = V_{SUP},		1	2	mA
		Standby Mode: EN = Low, Bus Recessive: LIN = V_{SUP},		40	80	µA
		Sleep Mode: 4.0 V < V_{SUP} < 14 V, LIN = V_{SUP}, EN = 0 V, TXD and RXD Floating		7	20	µA
		Sleep Mode: 14 V < V_{SUP} < 36 V, LIN = V_{SUP}, EN = 0 V, TXD and RXD Floating			30	µA
RXD OUTPUT PIN (OPEN DRAIN)						
V_{OL}	Output Low voltage	Based upon External pull up to V_{CC}			0.6	V
I_{OL}	Low level output current, open drain	LIN = 0 V, RXD = 0.4 V	1.5			mA
I_{ILG}	Leakage current, high-level	LIN = V_{SUP}, RXD = 5 V	–5	0	5	µA
TXD INPUT PIN						
V_{IL}	Low level input voltage		–0.3		0.8	V
V_{IH}	High level input voltage		2		5.5	V
V_{IT}	Input threshold voltage, normal modes& selective wake modes		30		500	mV
I_{ILG}	Low level input leakage current	TXD = Low	–5	0	5	µA
R_{TXD}	Interal pulldown resitor value		125	350	800	kΩ
EN INPUT PIN						
V_{IL}	Low level input voltage		–0.3		0.8	V
V_{IH}	High level input voltage		2		5.5	V

(1) Values are for each V_{SUP} pin

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT}	Hysteresis voltage	By design and characterization	30		500	V
I_{ILG}	Low level input current	EN = Low	-5	0	5	µA
R_{EN}	Internal Pulldown resistor		125	350	800	kΩ
LIN PIN						
V_{OH}	High level output voltage	LIN recessive, TXD = high, I_O = 0 mA, V_{SUP} = 7 V to 45 V	0.85			V_{SUP}
		LIN recessive, TXD = high, I_O = 0 mA, 4 V ≤ V_{SUP} < 7 V	3.0			V
V_{OL}	Low level output voltage	LIN dominant, TXD = low, V_{SUP} = 7 V to 45 V			0.2	V_{SUP}
		LIN dominant, TXD = low, 4 V ≤ V_{SUP} < 7 V			1.2	V
$V_{SUP\_NON\_OP}$	VSUP where Impact of recessive LIN Bus < 5% (ISO/DIS 17987 Param 56)	TXD& RXD open LIN = 4 V to 58 V	-0.3		58	V
I_{BUS_LIM}	Limiting current (ISO/DIS 17987 Param 57)	TXD = 0 V, V_{LIN} = 36 V, R_{MEAS} = 440 Ω, V_{SUP} = 36 V, V_{BUSdom} < 4.518 V See Figure 13	75	120	200	mA
$I_{BUS\_PAS\_dom}$	Receiver leakage current, dominant (ISO/DIS 17987 Param 58)	LIN = 0 V, V_{SUP} = 24 V Driver off/recessive See Figure 14	-1			mA
$I_{BUS\_PAS\_rec}$	Receiver leakage current, recessive (ISO/DIS 17987 Param 59)	LIN > V_{SUP}, 4 V < V_{SUP} < 45 V Driver off; See Figure 15			20	µA
$I_{BUS\_NO\_GND}$	Leakage current, loss of ground (ISO/DIS 17987 Param 60)	GND = V_{SUP}, 0 V ≤ V_{LIN} ≤ 36 V, V_{SUP} = 24 V; See Figure 16	-1.5		1.5	mA
$I_{BUS\_NO\_BAT}$	Leakage current, loss of supply (ISO/DIS 17987 Param 16, 61)	LIN = 36 V, V_{SUP} = GND; See Figure 17			5	µA
V_{BUSdom}	Low level input voltage (ISO/DIS 17987 Param 17, 62)	LIN dominant (including LIN dominant for wake up) See Figure 11 and Figure 10			0.4	V_{SUP}
V_{BUSrec}	High level input voltage (ISO/DIS 17987 Param 18, 63)	Lin recessive See Figure 11 and Figure 10	0.6			V_{SUP}
V_{BUS_CNT}	Receiver center threshold (ISO/DIS 17987 Param 19, 64)	$V_{BUS\_CNT} = (V_{IL} + V_{IH})/2$ See Figure 11 and Figure 10	0.475	0.5	0.525	V_{SUP}
V_{HYS}	Hysteresis voltage (ISO/DIS 17987 Param 20, 65)	$V_{HYS} = (V_{IL} - V_{IH})$ See Figure 11 and Figure 10	0.05		0.175	V_{SUP}
V_{SERIAL_DIODE}	Serial diode LIN term pullup path (ISO/DIS 17987 Param 21, 66)	By design and characterization	0.4	0.7	1	V
R_{SLAVE}	Pullup resistor to VSUP (ISO/DIS 17987 Param 26, 71)	Normal and Standby modes	20	45	60	kΩ
I_{RSLEEP}	Pullup current source to V_{SUP}	Sleep mode, V_{SUP} = 27 V, LIN = GND	-20		-2	µA
C_{LINPIN}	Capacitance of LIN pin	V_{SUP} = 14 V			25	pF

6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$D1_{12V}$	Duty Cycle 1 (ISO/DIS 17987 Param 27)(1)	$TH_{REC(MAX)}$ = 0.744 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP}, V_{SUP} = 7 V to 18 V, t_{BIT} = 50 µs (20 kbps), D1 = $t_{BUS\_rec(min)}$/(2 x t_{BIT}) (See Figure 18 and Figure 19)	0.396			

(1) Duty cycles: LIN driver bus load conditions (CLINBUS, RLINBUS): Load1 = 1 nF, 1 kΩ; Load2 = 10 nF, 500 Ω. Duty cycles 3 and 4 are defined for 10.4-kbps operation. The TLIN1029 also meets these lower data rate requirements, while it is capable of the higher speed 20-kbps operation as specified by duty cycles 1 and 2. SAEJ2602 derives propagation delay equations from the LIN 2.0 duty cycle definitions, for details see the SAEJ2602 specification

Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$D1_{12V}$	Duty Cycle 1	$TH_{REC(MAX)}$ = 0.625 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP}, V_{SUP} = 4 V to 7 V, t_{BIT} = 50 µs (20 kbps), D1 = $t_{BUS\_rec(min)}/(2 \times t_{BIT})$ (See Figure 18 and Figure 19)	0.396			
$D2_{12V}$	Duty Cycle 2 (ISO/DIS 17987 Param 28)	$TH_{REC(MAX)}$ = 0.422 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.284 x V_{SUP}, V_{SUP} = 4.6 V to 18 V, t_{BIT} = 50 µs (20 kbps), D2 = $t_{BUS\_rec(MAX)}/(2 \times t_{BIT})$ (See Figure 18 and Figure 19)			0.581	
$D3_{12V}$	Duty Cycle 3 (ISO/DIS 17987 Param 29)	$TH_{REC(MAX)}$ = 0.778 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.616 x V_{SUP}, V_{SUP} = 7 V to 18 V, t_{BIT} = 96 µs (10.4 kbps), D3 = $t_{BUS\_rec(min)}/(2 \times t_{BIT})$ (See Figure 18 and Figure 19)	0.417			
$D3_{12V}$	Duty Cycle	$TH_{REC(MAX)}$ = 0.645 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.616 x V_{SUP}, V_{SUP} = 4 V to 7 V, t_{BIT} = 96 µs (10.4 kbps), D3 = $t_{BUS\_rec(min)}/(2 \times t_{BIT})$ (See Figure 18 and Figure 19)	0.417			
$D4_{12V}$	Duty Cycle 4 (ISO/DIS 17987 Param 30)	$TH_{REC(MIN)}$ = 0.389 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.251 x V_{SUP}, V_{SUP} = 4.6 V to 18 V, t_{BIT} = 96 µs (10.4 kbps), D4 = $t_{BUS\_rec(MAX)}/(2 \times t_{BIT})$ (See Figure 18 and Figure 19)			0.59	
$D1_{24V}$	Duty Cycle 1 (ISO/DIS 17987 Param 27)[1]	$TH_{REC(MAX)}$ = 0.710 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.544 x V_{SUP}, V_{SUP} = 15 V to 36 V, t_{BIT} = 50 µs (20 kbps), D1 = $t_{BUS\_rec(min)}/(2 \times t_{BIT})$ (See Figure 18 and Figure 19)	0.33			
$D2_{24V}$	Duty Cycle 2 (ISO/DIS 17987 Param 28)	$TH_{REC(MAX)}$ = 0.446 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.302 x V_{SUP}, V_{SUP} = 15.6 V to 36 V, t_{BIT} = 50 µs (20 kbps), D2 = $t_{BUS\_rec(MAX)}/(2 \times t_{BIT})$ (See Figure 18 and Figure 19)			0.642	
$D3_{24V}$	Duty Cycle 3 (ISO/DIS 17987 Param 29)	$TH_{REC(MAX)}$ = 0.744 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP}, V_{SUP} = 7 V to 36 V, t_{BIT} = 96 µs (10.4 kbps), D3 = $t_{BUS\_rec(min)}/(2 \times t_{BIT})$ (See Figure 18 and Figure 19)	0.386			
$D3_{24V}$	Duty Cycle	$TH_{REC(MAX)}$ = 0.645 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP}, V_{SUP} = 4 V to 7 V, t_{BIT} = 96 µs (10.4 kbps), D3 = $t_{BUS\_rec(min)}/(2 \times t_{BIT})$ (See Figure 18 and Figure 19)	0.386			
$D4_{24V}$	Duty Cycle 4 (ISO/DIS 17987 Param 30)	$TH_{REC(MIN)}$ = 0.442 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.284 x V_{SUP}, V_{SUP} = 4.6 V to 36 V, t_{BIT} = 96 µs (10.4 kbps), D4 = $t_{BUS\_rec(MAX)}/(2 \times t_{BIT})$ (See Figure 18 and Figure 19)			0.591	

6.8 Timing Requirements

SYMBOL	DESCRIPTION	TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{rx_pdr}	Receiver rising propagation delay time (ISO/DIS 17987 Param 31)	R_{RXD} = 2.4 kΩ, C_{RXD} = 20 pF (See Figure 20 and Figure 21)			6	µs
t_{rx_pdf}	Receiver falling propagation delay time (ISO/DIS 17987 Param 31)				6	µs

Timing Requirements (continued)

SYMBOL	DESCRIPTION	TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{rs_sym}	Symmetry of receiver propagation delay time Receiver rising propagation delay time (ISO/DIS 17987 Param 32)	Rising edge with respect to falling edge, (trx_sym = trx_pdf – trx_pdr), R_{RXD} = 2.4 kΩ, C_{RXD} = 20 pF (See Figure 20 and Figure 21)	–2		2	µs
t_{LINBUS}	LIN wakeup time (Minimum dominant time on LIN bus for wakeup)	See Figure 24, Figure 27, and Figure 28	25	100	150	µs
t_{CLEAR}	Time to clear false wakeup prevention logic if LIN bus had a bus stuck dominant fault (recessive time on LIN bus to clear bust stuck dominant fault)	See Figure 28	8	17	50	µs
t_{DST}	Dominant state time out		20	34	80	ms
t_{MODE_CHANGE}	Mode change delay time	Time to change from standby mode to normal mode or normal mode to sleep mode through EN pin: See Figure 22 and Figure 29	2		15	µs
t_{NOMINT}	Normal mode initialization time	Time for normal mode to initialize and data on RXD pin to be valid See Figure 22			35	µs
t_{PWR}	Power up time	Upon power up time it takes for valid data on RXD			1.5	ms

6.9 Typical Characteristics

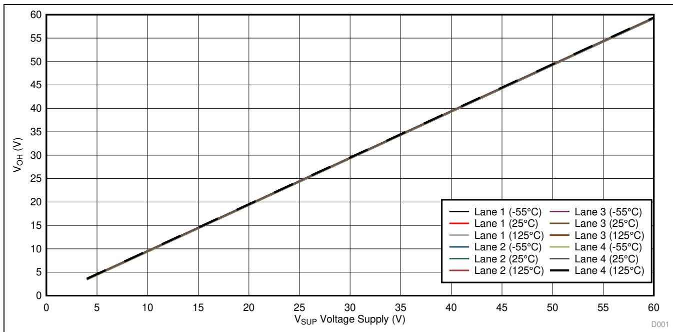


Figure 1. V_{OH} vs V_{SUP} and Temperature

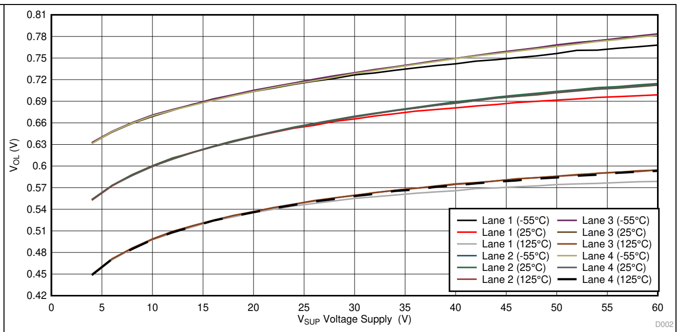


Figure 2. V_{OL} vs V_{SUP} and Temperature

Typical Characteristics (continued)

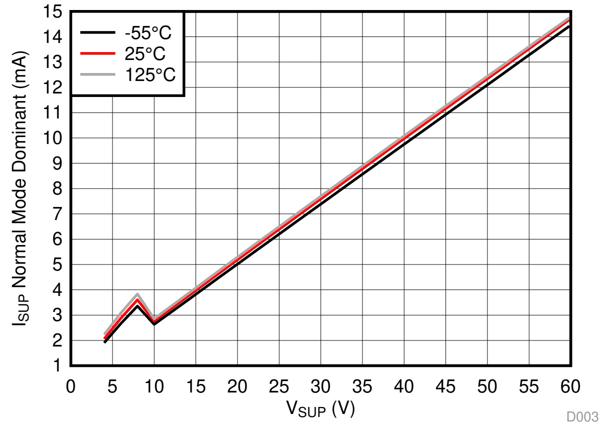


Figure 3. Normal Mode Dominant vs V_{SUP}

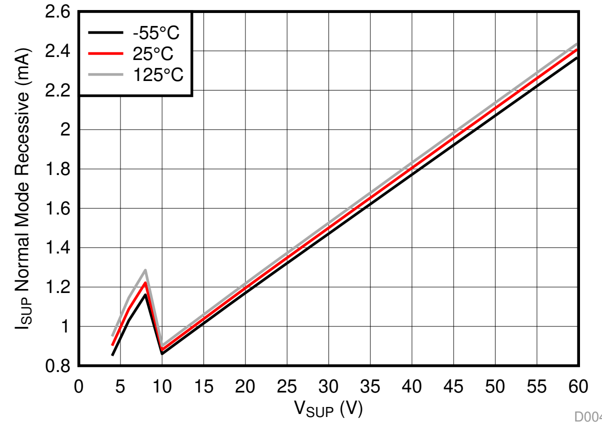


Figure 4. Normal Mode Recessive vs V_{SUP}

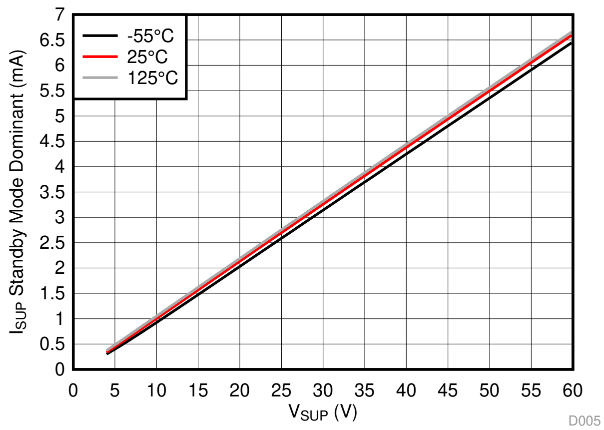


Figure 5. Standby Mode Dominant vs V_{SUP}

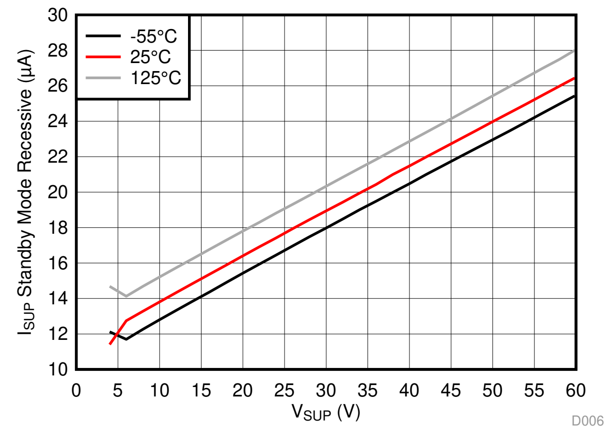


Figure 6. Standby Mode Recessive vs V_{SUP}

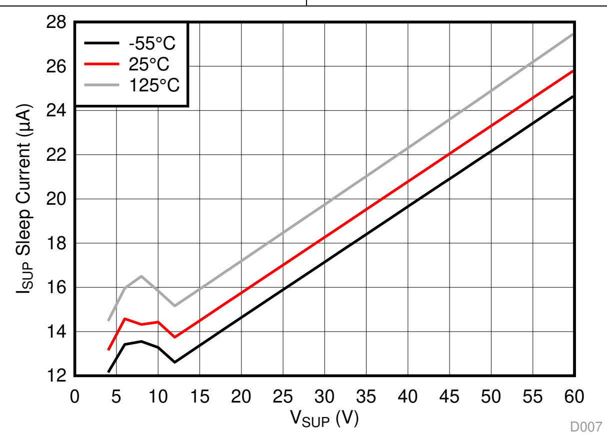


Figure 7. Sleep Mode vs V_{SUP}

7 Parameter Measurement Information

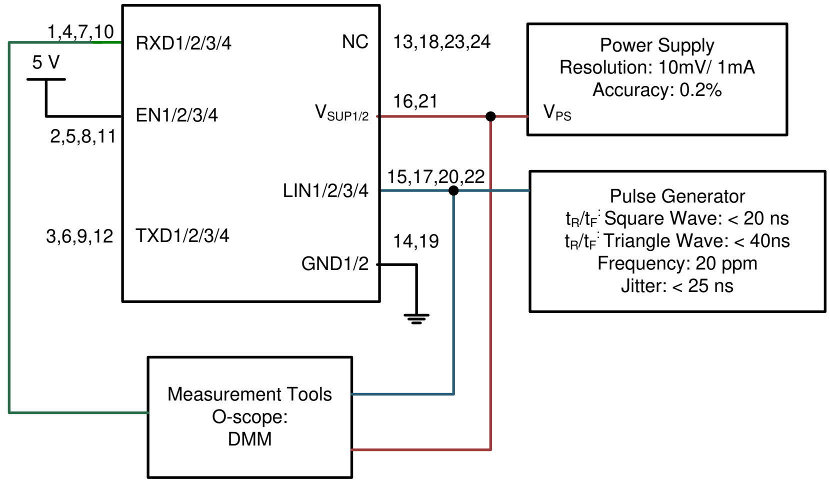


Figure 8. Test System: Operating Voltage Range with RX and TX Access

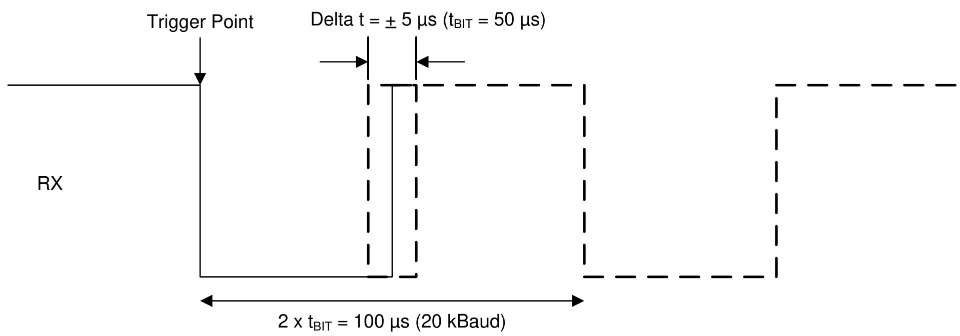


Figure 9. RX Response: Operating Voltage Range

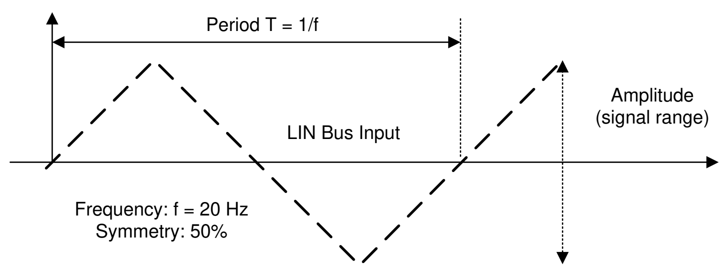


Figure 10. LIN Bus Input Signal

Parameter Measurement Information (continued)

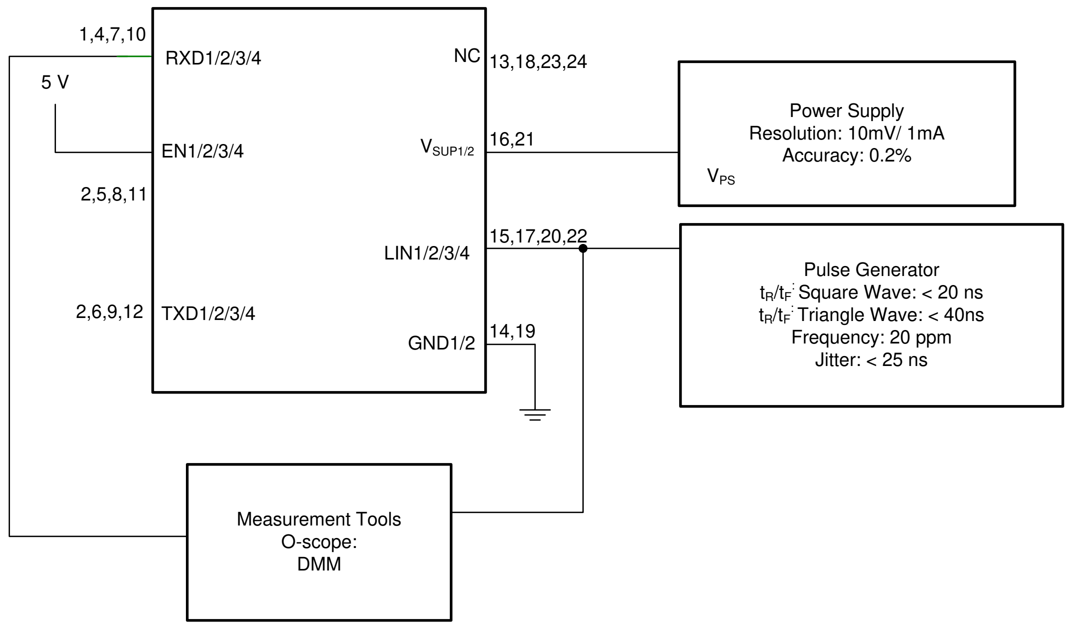


Figure 11. LIN Receiver Test with RX Access

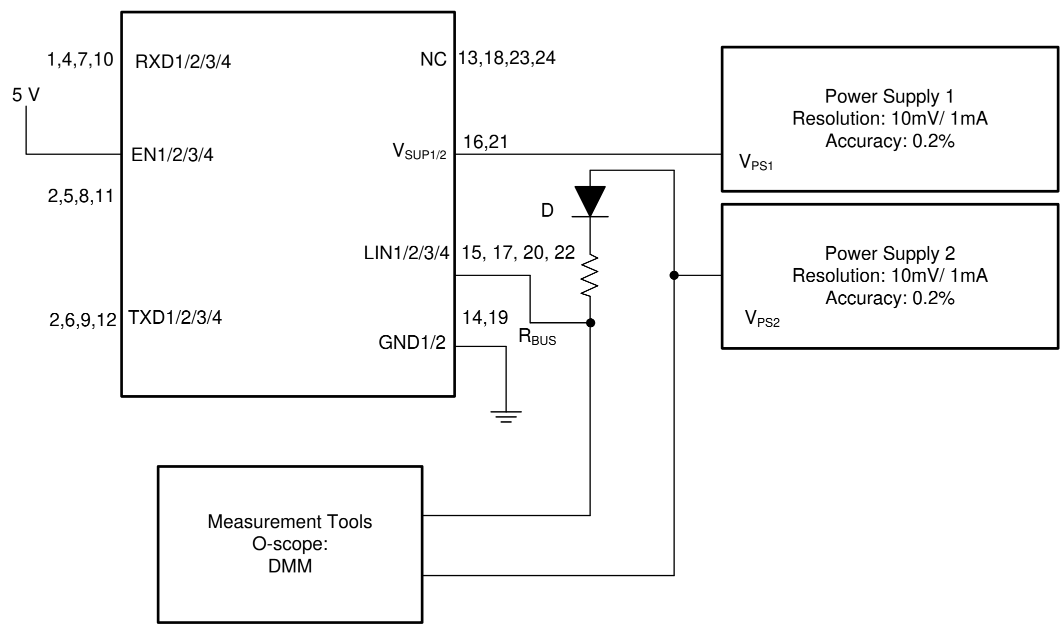


Figure 12. $V_{SUP\_NON\_OP}$

Parameter Measurement Information (continued)

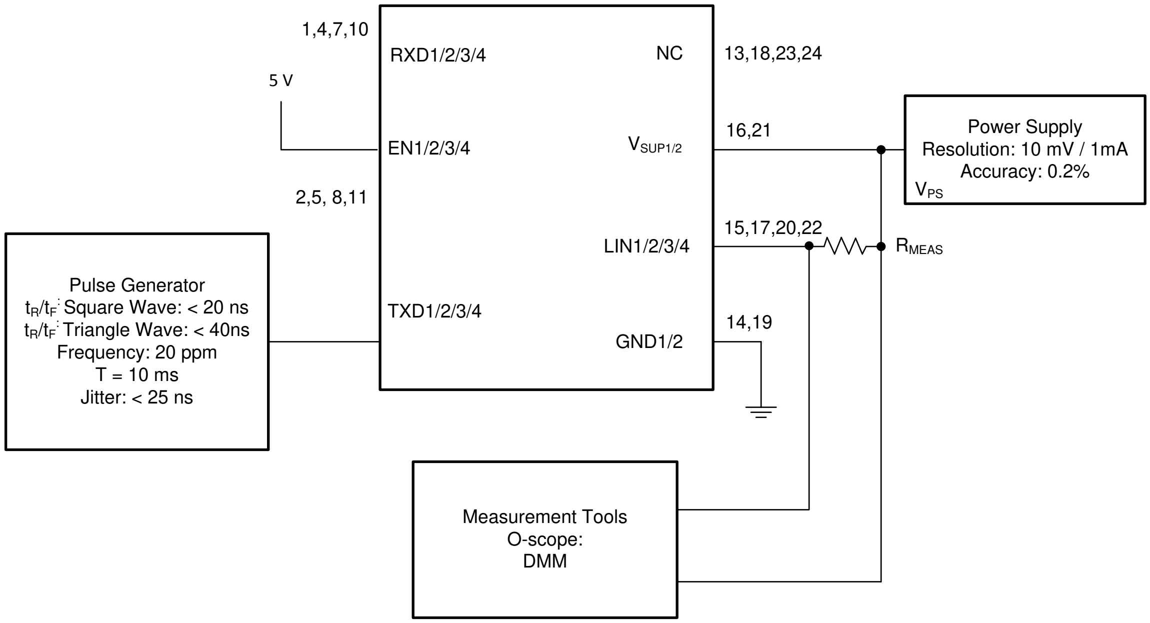


Figure 13. Test Circuit for I_{BUS_LIM} at Dominant State (Driver on)

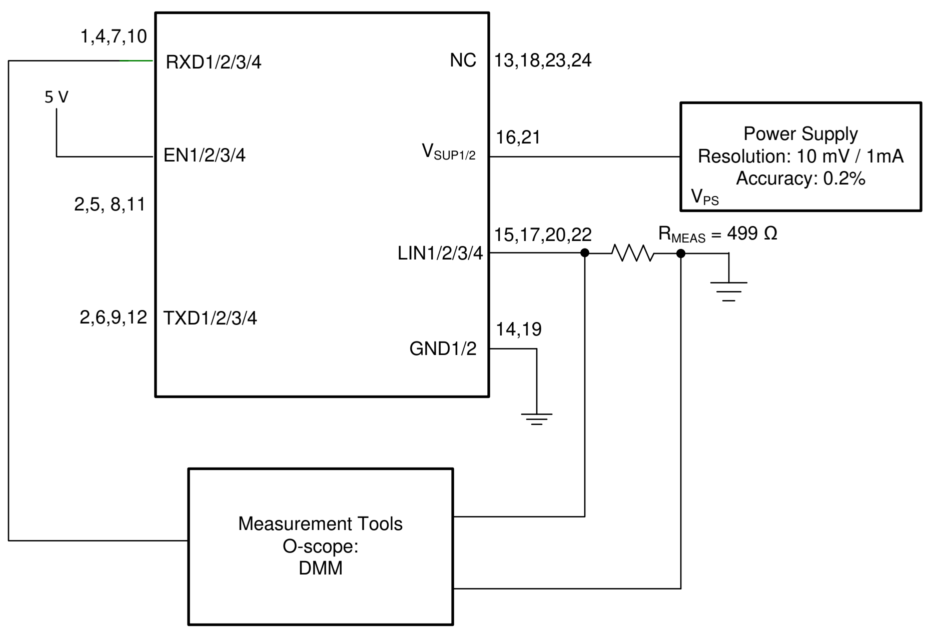


Figure 14. Test Circuit for $I_{BUS\_PAS\_dom}$; TXD = Recessive State V_{BUS} = 0 V

Parameter Measurement Information (continued)

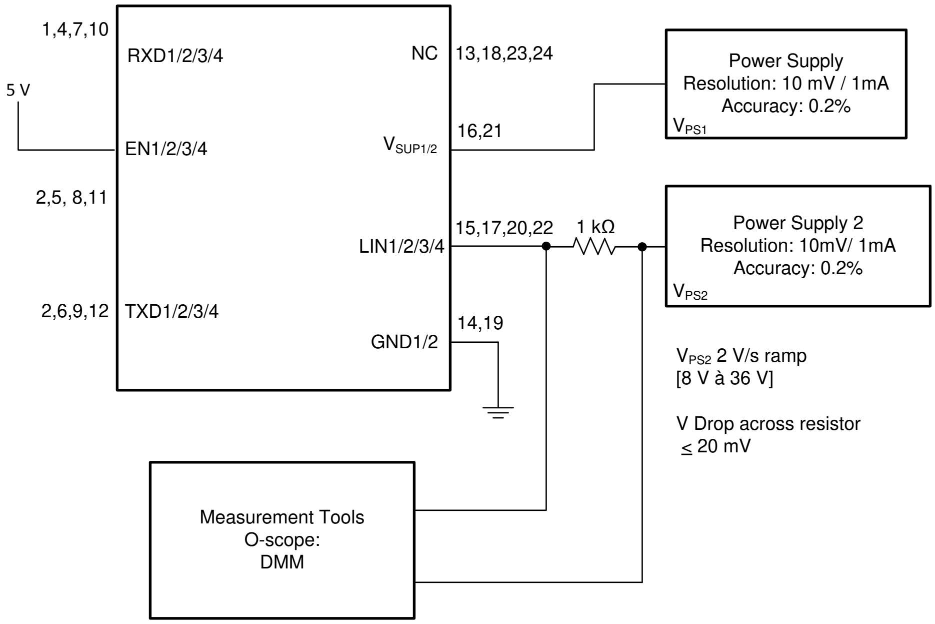


Figure 15. Test Circuit for $I_{BUS\_PAS\_rec}$

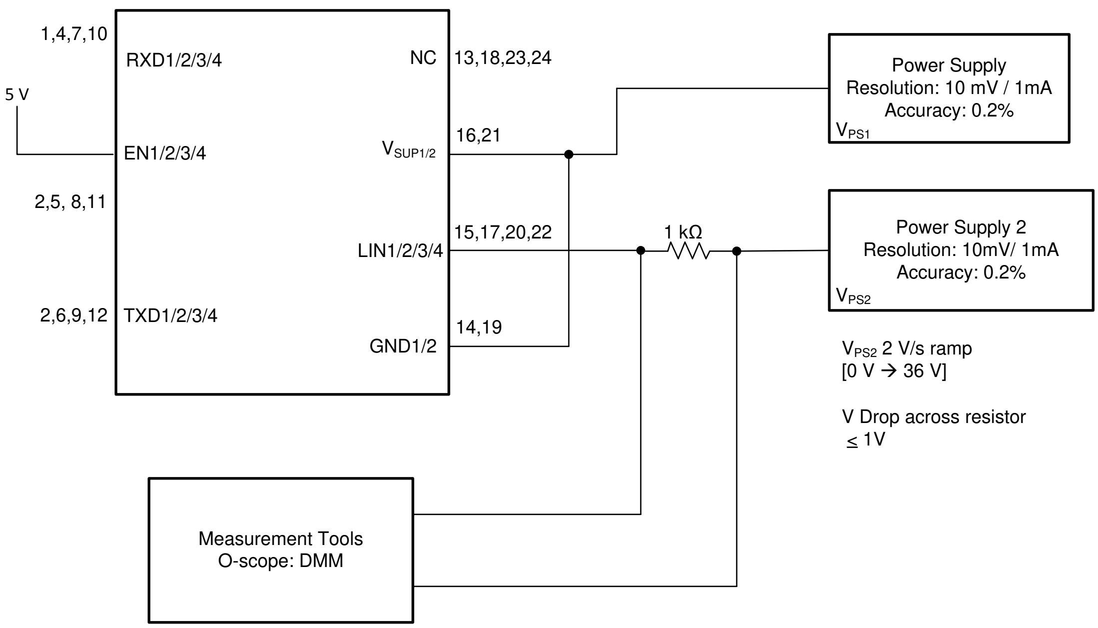


Figure 16. Test Circuit for $I_{BUS\_NO\_GND}$ Loss of GND

Parameter Measurement Information (continued)

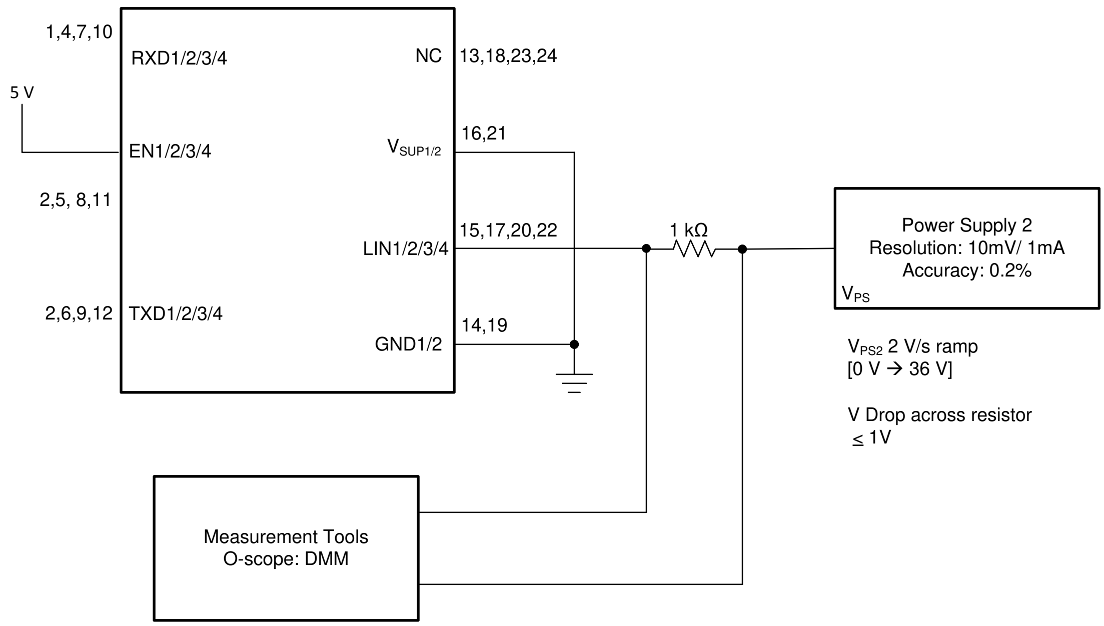


Figure 17. Test Circuit for $I_{BUS\_NO\_BAT}$ Loss of Battery

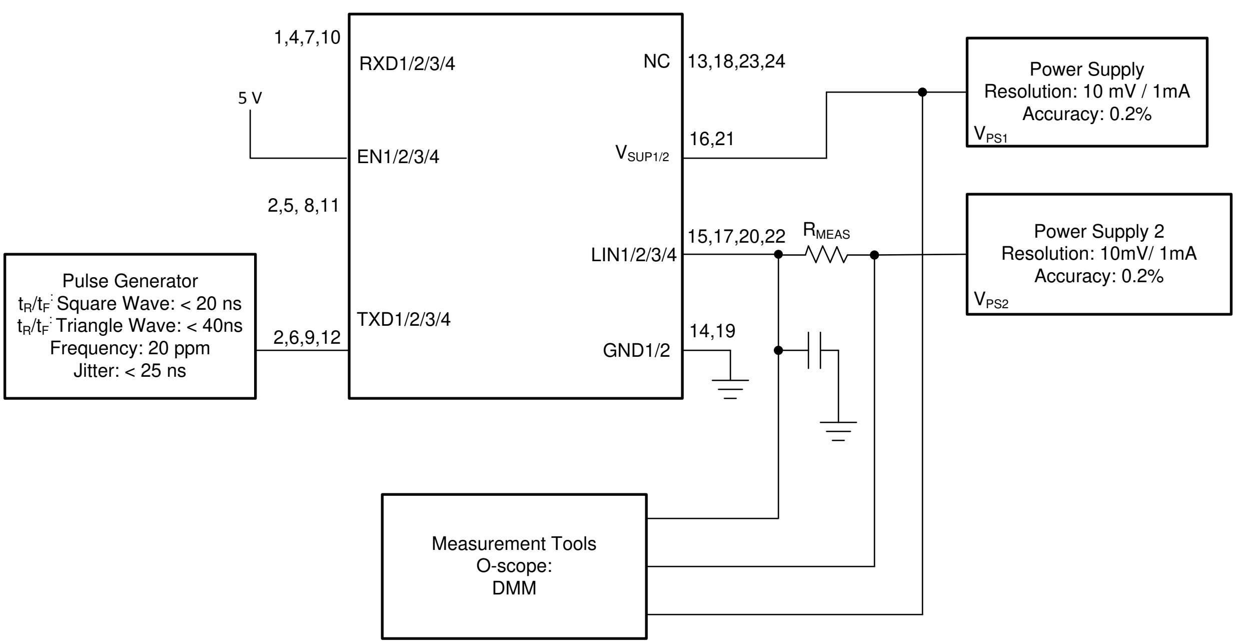


Figure 18. Test Circuit Slope Control and Duty Cycle

Parameter Measurement Information (continued)

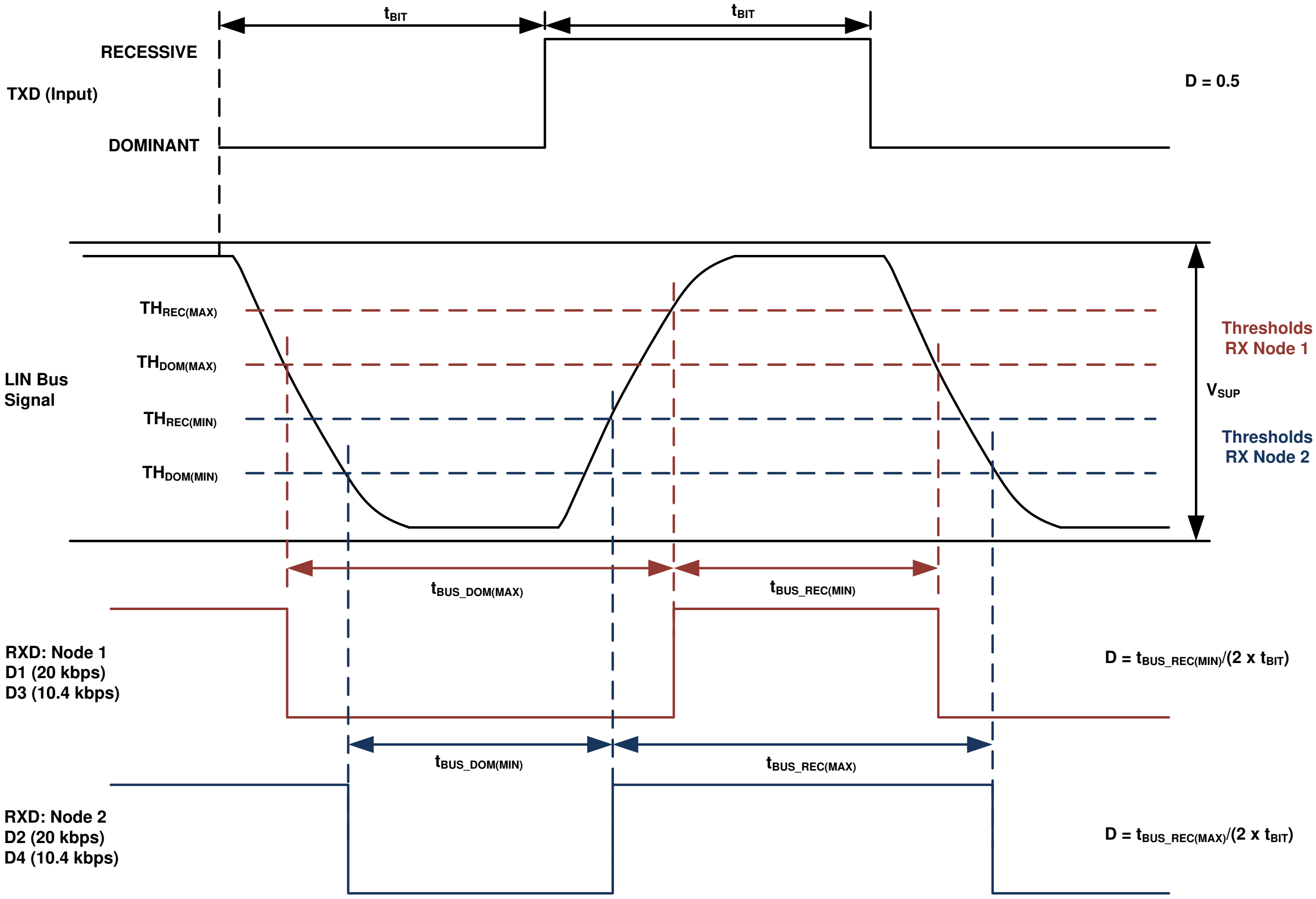


Figure 19. Definition of Bus Timing Parameters

Parameter Measurement Information (continued)

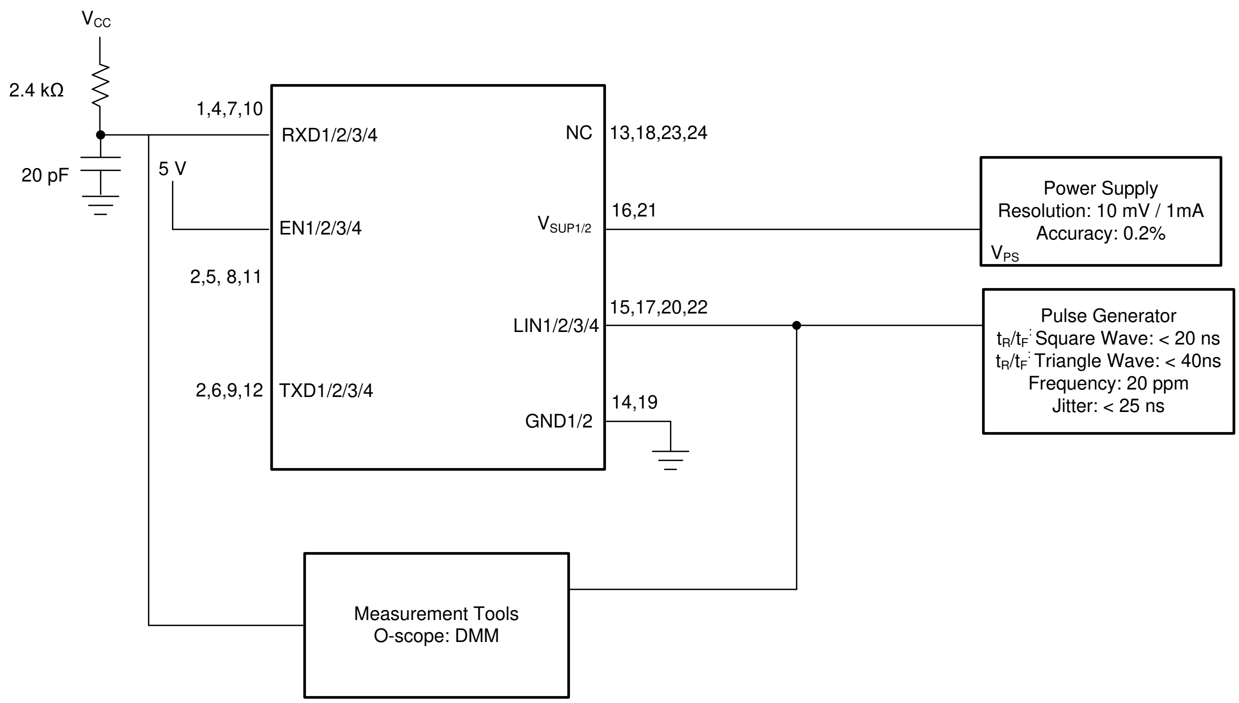


Figure 20. Propagation Delay Test Circuit

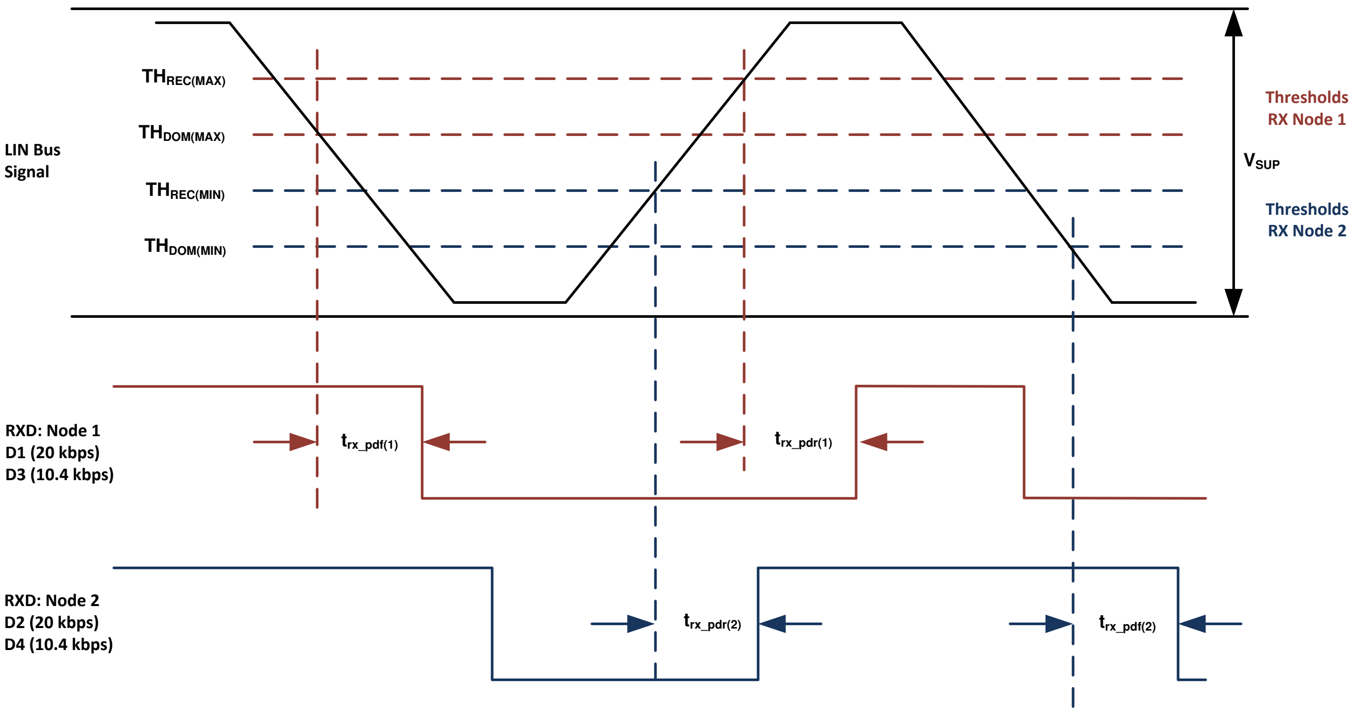


Figure 21. Propagation Delay

Parameter Measurement Information (continued)

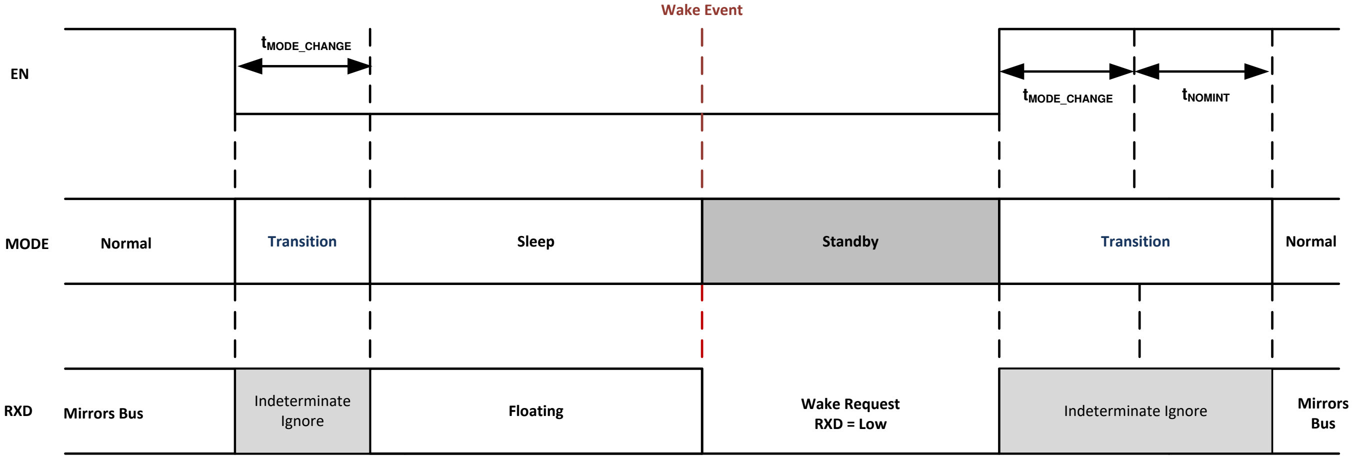


Figure 22. Mode Transitions

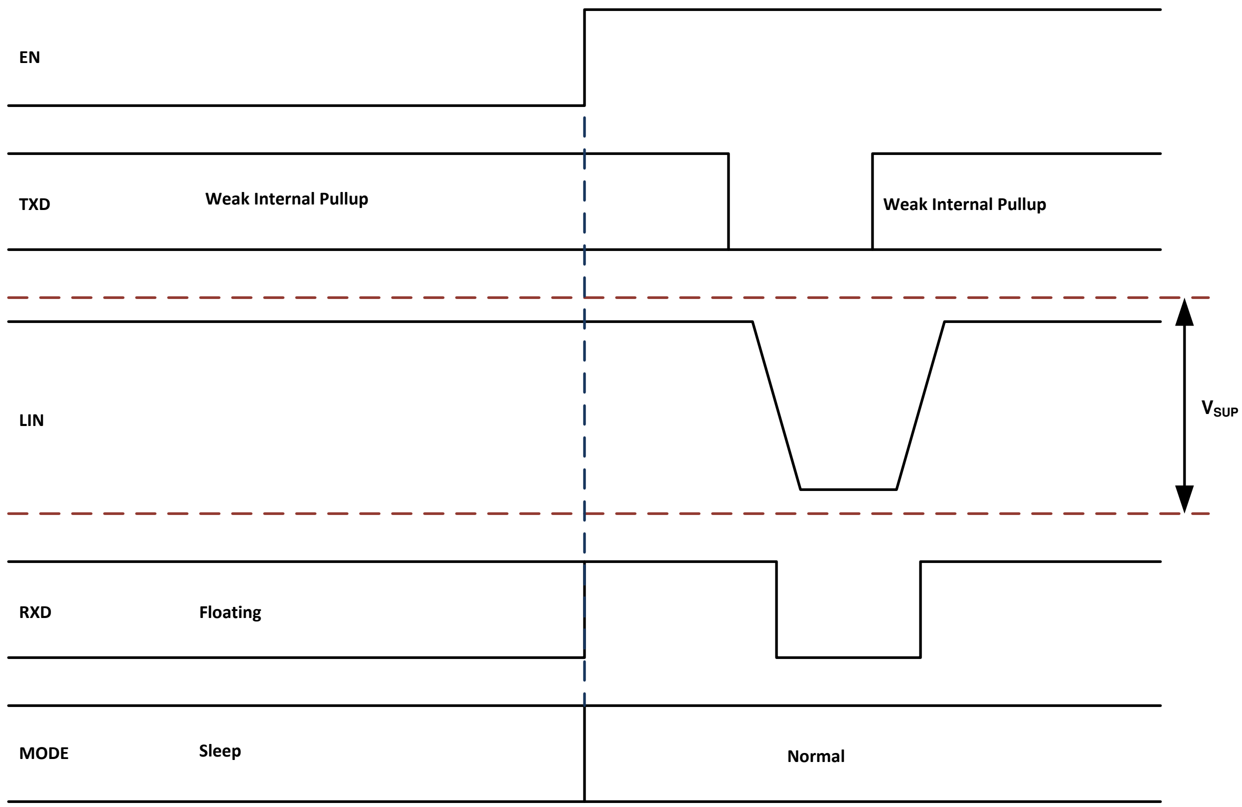


Figure 23. Wake Up Through EN

Parameter Measurement Information (continued)

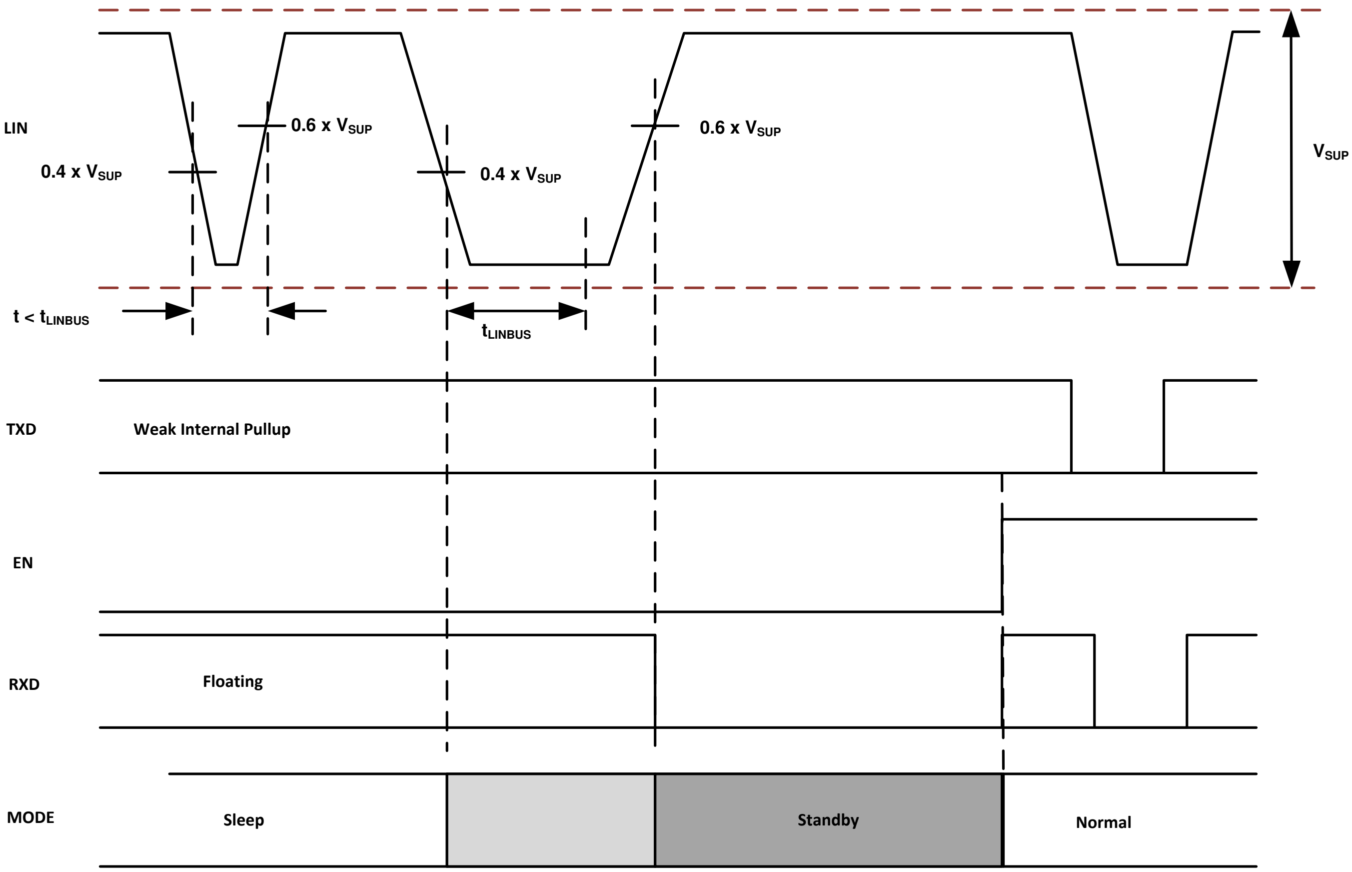


Figure 24. Wake Up Through LIN

Parameter Measurement Information (continued)

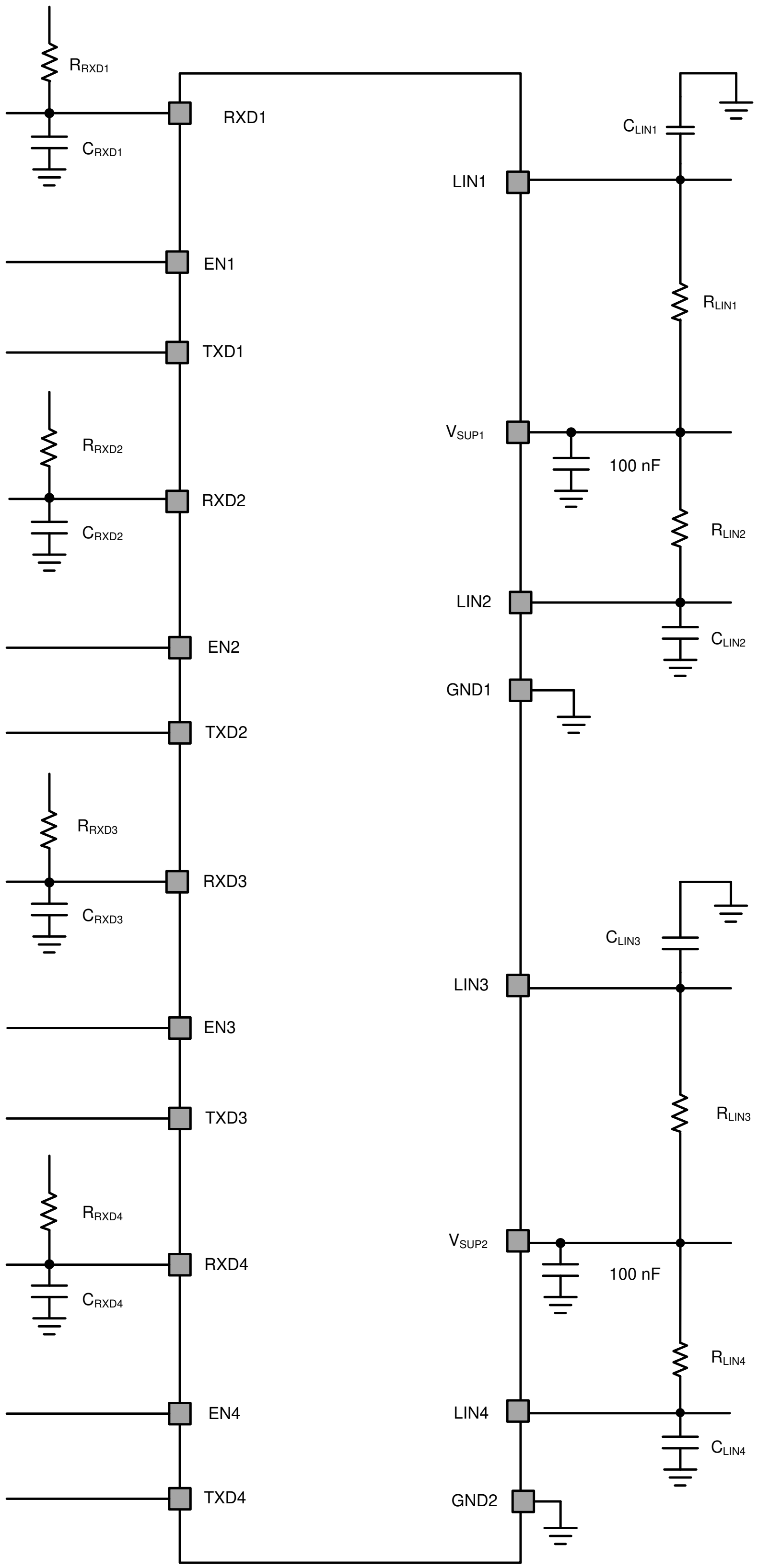


Figure 25. Test Circuit for AC Characteristics

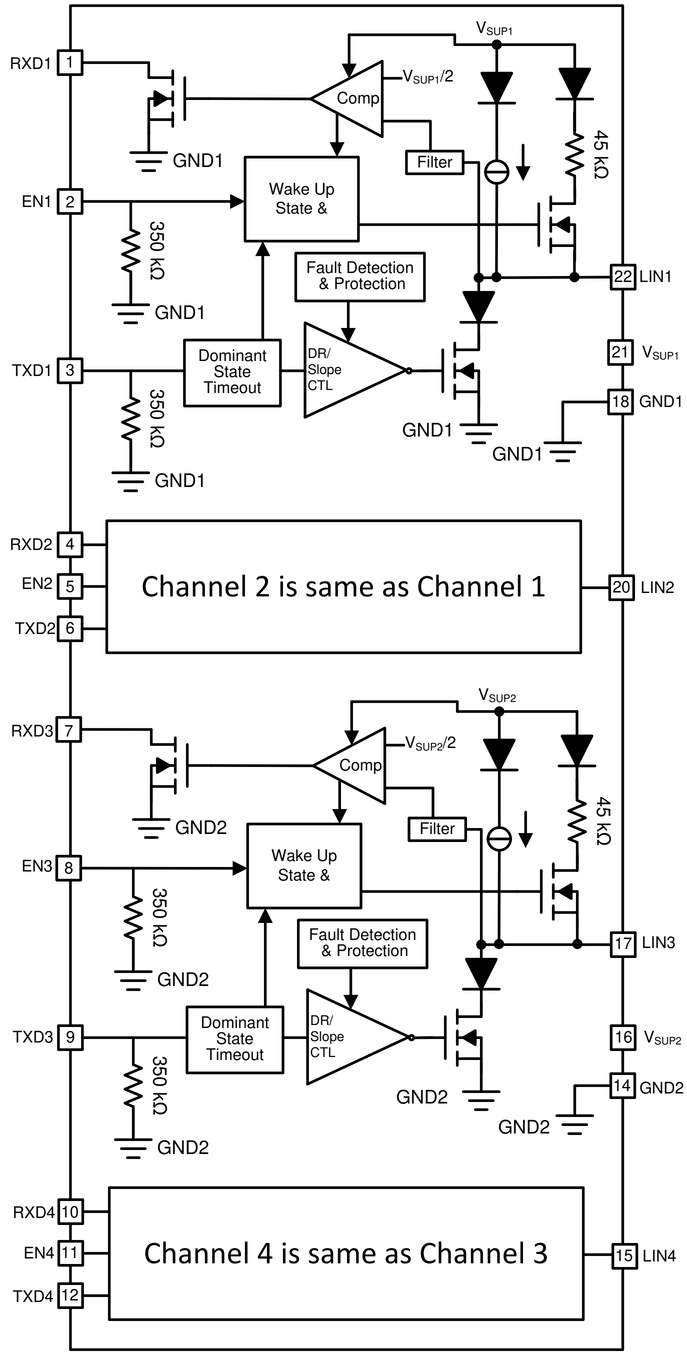
8 Detailed Description

8.1 Overview

The TLIN2024-Q1 device is a Quad Local Interconnect Network (LIN) physical layer transceiver, compliant to LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A and ISO/DIS 17987–4.2, with integrated wake-up and protection features. The TLIN2024-Q1 has two separate dual LIN transceiver blocks. $V_{SUP1/2}$ provides power to the separate dual transceiver blocks. The LIN bus is a single wire bidirectional bus typically used for low speed in vehicle networks using data rates up to 20 kbps. The TLIN2024-Q1 LIN receivers work up to 100 kbps supporting in-line programming. The LIN protocol output data stream on the TXD in converted by the TLIN2024-Q1 into LIN bus signal using a current-limited wave shaping driver as outlined by the LIN physical layer specification. The receiver converts the data stream to logic level signals that are sent to the microprocessor through the open drain RXD pin. The LIN bus has two states: dominant state (voltage near ground) and recessive state (voltage near battery). In the recessive state, the LIN bus is pulled high by the internal pull-up resistor (45 kΩ) and a series diode. No external pull-up components are required for slave applications. Master applications require an external pull-up resistor (1 kΩ) plus a series diode per the LIN specification. The TLIN2024-Q1 provides many protection features such as ESD, EMC and high bus standoff voltage.

The TLIN2024-Q1 support wide operating ranges with $V_{SUP1/2}$ of 4 V to 48 V, ±60 V LIN bus fault protection, -40 to +125 C T_A. Sleep mode is supported which is Ultra-Low current consumption. There are two methods to wake up the TLIN2024-Q1 from sleep mode; by the LIN bus and local wake-up using the EN pin. The TLIN2024-Q1 provides protection features that include ±8 kV HBM and IEC ESD protection on LIN pins, under voltage protection on $V_{SUP1/2}$, TXD dominant time out protection (DTO), thermal shutdown protection and unpowered node or ground disconnection failsafe at system level. V_{SUP1} and GND1 supplies transceivers 1 and 2 while V_{SUP2} and GND2 supplies transceiver 3 and 4. The TLIN2024-Q1 is part of the LIN family that includes the TLIN2022 and TLIN2029 LIN transceivers.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 LIN (Local Interconnect Network) Bus

These high voltage input/output pins are single wire LIN bus transmitters and receivers. The LIN pins can survive excessive DC and transient voltages up to 58 V. Reverse currents from the LIN pins to supply ($V_{SUP1/2}$) are minimized with blocking diodes, even in the event of a ground shift or loss of supply ($V_{SUP1/2}$).

Feature Description (continued)

8.3.1.1 LIN Transmitter Characteristics

The transmitter has thresholds and AC parameters according to the LIN specification. The transmitter is a low side transistor with and internal current limitation and thermal shutdown. During a thermal shutdown condition, the transmitter is disabled to protect the device. There is an internal pull-up resistor with a serial diode structure to $V_{SUP1/2}$, so no external pull-up components are required for the LIN slave mode applications. An external pull-up resistor and series diode to $V_{SUP1/2}$ must be added when the device is used for a master node application.

8.3.1.2 LIN Receiver Characteristics

The receiver characteristic thresholds are ratio-metric with the device supply pin according to the LIN specification.

The receiver is capable of receiving higher data rates (> 100 kbps) than supported by LIN or SAE J2602 specifications. This allows the TLIN2024-Q1 to be used for high speed downloads at the end-of-line production or other applications. The actual data rate achievable depends on system time constants (bus capacitance and pull-up resistance) and driver characteristics used in the system.

8.3.1.2.1 Termination

There is an internal pull-up resistor with a serial diode structure to $V_{SUP1/2}$, so no external pull-up components are required for the LIN slave mode applications. An external pull-up resistor (1 kΩ) and a series diode to $V_{SUP1/2}$ must be added when the device is used for master node applications as per the LIN specification.

Figure 26 shows a Master Node configuration and how the voltage levels are defined

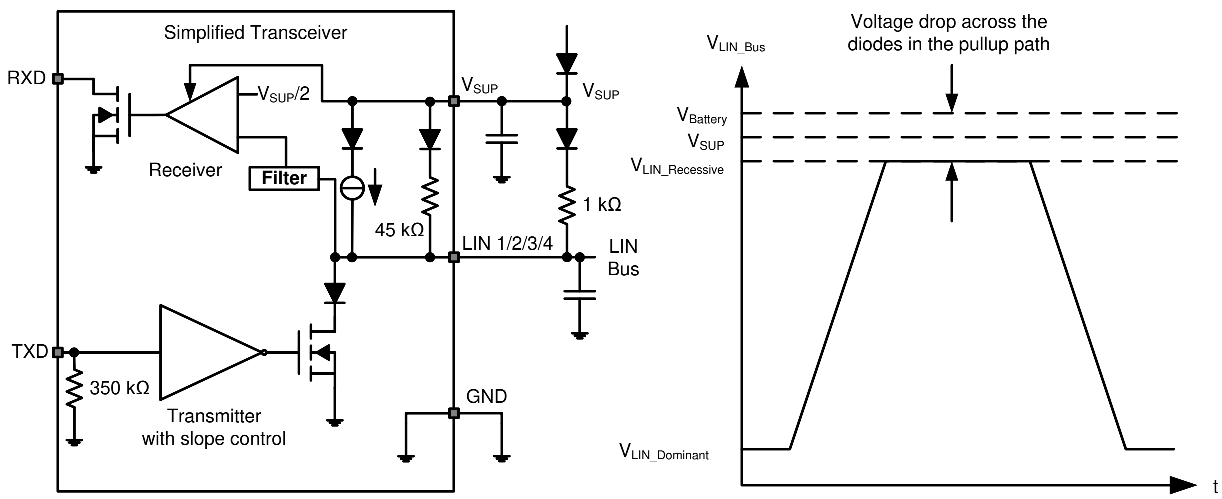


Figure 26. Master Node Configuration with Voltage Levels

8.3.2 TXD (Transmit Input/Output)

TXD is the interface to the processors LIN protocol controller or SCI/UART that is used to control the state of the LIN output. When TXD is low the LIN output is dominant (near ground). When TXD is high the LIN output is recessive (near $V_{Battery}$). See Figure 26. The TXD input structure is compatible with microprocessors with 3.3 V and 5 V I/O. TXD has an internal pull-down resistor. The LIN bus is protected from being stuck dominant through a system failure driving TXD low through the dominant state timer-out timer.

8.3.3 RXD (Receive Output)

RXD is the interface to the processors LIN protocol controller or SCI/UART, which reports the state of the LIN bus voltage. LIN recessive (near $V_{Battery}$) is represented by a high level on the RXD and LIN dominant (near ground) is represented by a low level on the RXD pin. The RXD output structure is an open-drain output stage. This allows the device to be used with 3.3 V and 5 V I/O microprocessors. If the microprocessor's RXD pin does not have an integrated pull-up, an external pull-up resistor to the microprocessor I/O supply voltage is required. In standby mode the RXD pin is driven low to indicate a wake up request from the LIN bus.

Feature Description (continued)

8.3.4 $V_{SUP1/2}$ (Supply Voltage)

$V_{SUP1/2}$ are the power supply pins. $V_{SUP1/2}$ is connected to the battery through and external reverse battery blocking diode (See Figure 26). If there is a loss of power at the ECU level, the device has extremely low leakage from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

8.3.5 GND (Ground)

GND1/2 are the device ground connections. The device can operate with a ground shift as long as the ground shift does not reduce $V_{SUP1/2}$ below the minimum operating voltage. If there is a loss of ground at the ECU level, the device has a low leakage from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

8.3.6 EN (Enable Input)

EN controls the operational modes of the device. When EN is high the device is in normal operating mode allowing a transmission path from TXD to LIN and from LIN to RXD. When EN is low the device is put into sleep mode and there are no transmission paths available. The device can enter normal mode only after wake up. EN has an internal pull-down resistor to endure the device remains in low power mode even if EN floats.

8.3.7 Protection Features

The TLIN2024-Q1 has several protection features that will now be described.

8.3.8 TXD Dominant Time Out (DTO)

During normal mode, if TXD is inadvertently driven permanently low by a hardware or software application failure, the LIN bus is protected by the dominant state timeout timer. This timer is triggered by a falling edge on the TXD pin. If the low signal remains on TXD for longer than t_{DST}, the transmitter is disabled, thus allowing the LIN bus to return to recessive state and communication to resume on the bus. The protection is cleared and the t_{DST} timer is reset by a rising edge on TXD. The TXD pin has an internal pull-down to ensure the device fails to a known state if TXD is disconnected. During this fault, the transceiver remains in normal mode (assuming no change of stated request on EN), the transmitter is disabled, the RXD pin reflects the LIN bus and the LIN bus pull-up termination remains on.

8.3.9 Bus Stuck Dominant System Fault: False Wake Up Lockout

The TLIN2024-Q1 contains logic to detect bus stuck dominant system faults and prevents the device from waking up falsely during the system fault. Upon entering sleep mode, the device detects the state of the LIN bus. If the bus is dominant, the wake up logic is locked out until a valid recessive on the bus “clears” the bus stuck dominant, preventing excessive current use Figure 27 and Figure 28 show the behavior of this protection.

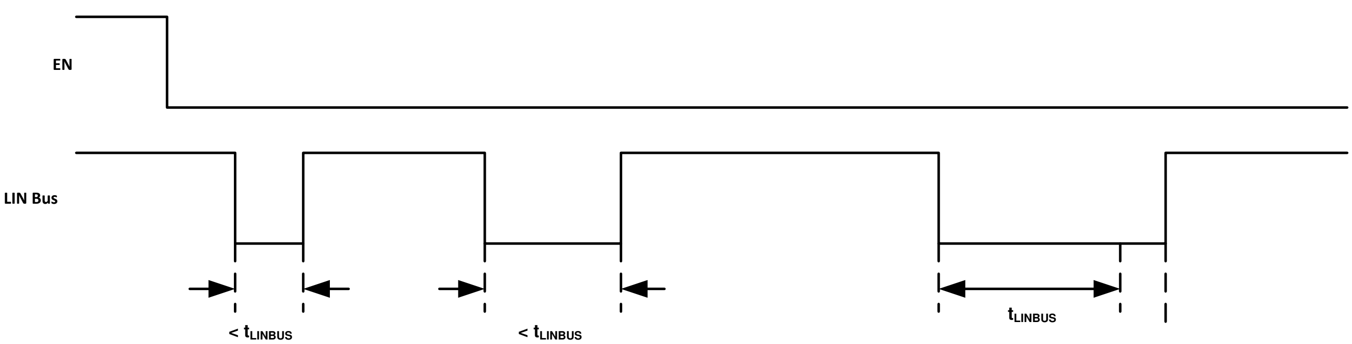


Figure 27. No Bus Fault: Entering Sleep Mode with Bus Recessive Condition and Wakeup

Feature Description (continued)

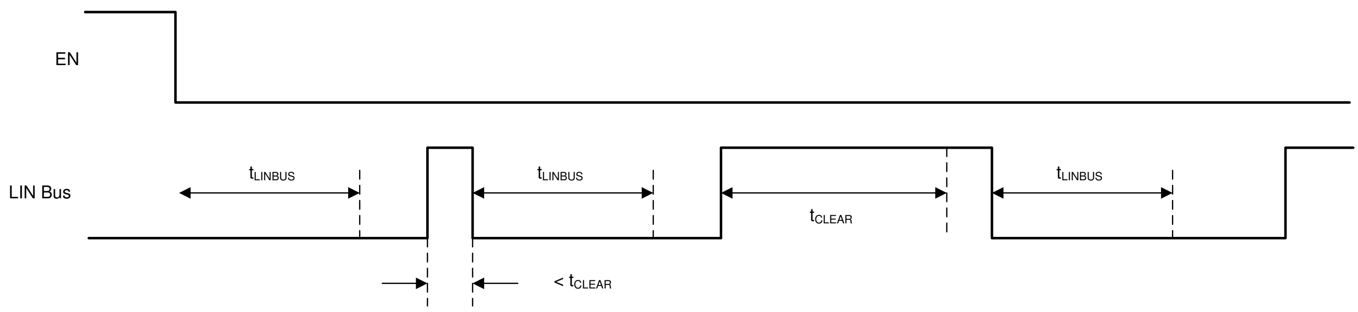


Figure 28. Bus Fault: Entering Sleep Mode with Bus Stuck Dominant Fault, Clearing, and Wakeup

8.3.10 Thermal Shutdown

The LIN transmitter is protected limiting the current; however if the junction temperature of the device exceeds the thermal shutdown threshold, the device puts the LIN transmitter into the recessive state. Once the over temperature fault condition has been removed and the junction temperature has cooled beyond the hysteresis temperature, the transmitter is re-enabled, assuming the device remained in the normal operation mode. During this fault, the transceiver remains in normal mode (assuming no change of state request on EN), the transmitter is in recessive state, the RXD pin reflects the LIN bus and LIN bus pull-up termination remains on.

8.3.11 Under Voltage on V_{SUP}

The TLIN2024-Q1 contains a power on reset circuit to avoid false bus messages during under voltage conditions when $V_{SUP1/2}$ is less than $UV_{SUP1/2}$.

8.3.12 Unpowered Device and LIN Bus

In automotive applications some LIN nodes in a system can be unpowered (ignition supplied) while others in the network remains powered by the battery. The TLIN2024-Q1 has a low unpowered leakage current from the bus so an unpowered node does not affect the network or load it down.

8.4 Device Functional Modes

The TLIN2024-Q1 has three functional modes of operation, normal, sleep, and standby. The next sections describe these modes as well as how the device moves between the different modes. Figure 29 graphically shows the relationship while Table 1 shows the state of pins.

Table 1. Operating Modes

MODE	ENx	RXDx	LIN BUS TERMINATION	TRANSMITTER	COMMENT
Sleep	Low	Floating	Weak Current Pull-up	Off	
Standby	Low	Low	45 kΩ (typical)	Off	Wake up event detected, waiting on MCU to set EN
Normal	High	LINx Bus Data	45 kΩ (typical)	On	LINx transmission up to 20 kbps

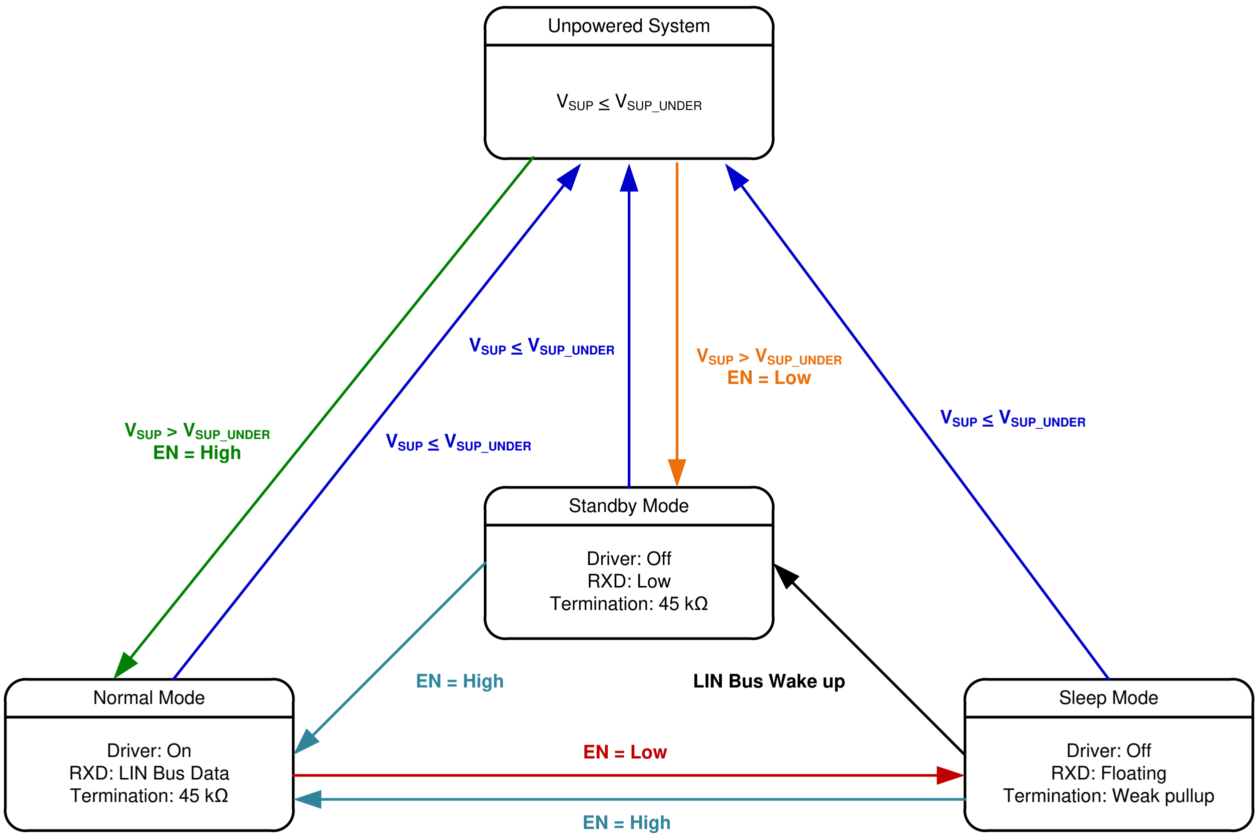


Figure 29. Operating State Diagram

8.4.1 Normal Mode

If the EN pin is high at power up, the device powers up in normal mode. The EN pin controls the mode of the device. In normal operational mode, the receiver and transmitter are active and the LIN transmission up to the LIN specified maximum of 20 kbps is supported. The receiver detects the data stream on the LIN bus and outputs it on RXD for the LIN controller. A recessive signal on the LIN bus is a digital high and a dominate signal on the LIN bus is a digital low. The driver transmits input data from TXD to the LIN bus. Normal mode is entered as EN transitions high while the TLIN2024-Q1 is in sleep or standby mode for > t_{MODE_CHANGE}.

8.4.2 Sleep Mode

Sleep Mode is the power saving mode for the TLIN2024-Q1. Even with extremely low current consumption in this mode, the TLIN2024-Q1 can still wake up from LIN bus through a wake up signal or if EN is set high for > t_{MODE_CHANGE}. The Lin bus is filtered to prevent false wake up events. The wake up events must be active for the respective time periods (t_{LINBUS}).

The sleep mode is entered by setting EN low for longer than t_{MODE_CHANGE}.

While the device is in sleep mode, the following conditions exist.

- The LIN bus driver is disabled and the internal LIN bus termination is switched off (to minimize power loss if LIN is short circuited to ground). However, the weak current pull-up is active to prevent false wake up events in case an external connection to the LIN bus is lost.
- The normal receiver is disabled.
- EN input and LIN wake up receiver are active.

8.4.3 Standby Mode

During power up if EN is low the device enters standby mode. Standby mode is entered whenever a wake up event occurs through LIN bus while the device is in sleep mode. The LIN bus slave termination circuit is turned on when standby mode is entered. Standby mode is signaled through a low level on RXD. See Standby Mode Application Note for more application information.

When EN is set high for longer than t_{MODE_CHANGE} while the device is in standby mode the device returns to normal mode and the normal transmission paths from TXD to LIN bus and LIN bus to RXD are enabled.

8.4.4 Wake Up Events

There are two ways to wake up from sleep mode:

- Remote wake up initiated by the falling edge of a recessive (high) to dominant (low) state transition on LIN bus where the dominant state is be held for t_{LINBUS} filter time. After this t_{LINBUS} filter time has been met and a rising edge on the LIN bus going from dominate state to recessive state initiates a remote wake up event, eliminating false wake ups from disturbances on the LIN bus or if the bus is shorted to ground.
- Local wake up through EN being set high for longer than t_{MODE_CHANGE}.

8.4.4.1 Wake Up Request (RXD)

When the TLIN2024-Q1 encounters a wake up event from the LIN bus, RXD goes low and the device transitions to standby mode until EN is reasserted high and the device enters normal mode. Once the device enters normal mode the RXD pin is releasing the wake up request signal and the RXD pin then reflects the receiver output from the LIN bus.

8.4.4.2 Mode Transitions

When the TLIN2024-Q1 is transitioning between modes the device needs the time, t_{MODE_CHANGE}, to allow the change to fully propagate from the EN pin through the device into the new state. When transitioning from sleep or standby mode to normal mode the transition time is the sum of t_{MODE_CHANGE} and t_{NOMINT}.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLIN2024-Q1 can be used as both a slave device and a master device in a LIN network. The device comes with the ability to support both remote wake up request and local wake up request.

9.2 Typical Application

The device comes with an integrated 45 kΩ pull-up resistor and series diode for slave applications. For master applications, an external 1 kΩ pull-up resistor with series blocking diode can be used. Figure 30 shows the device being used in both master and slave applications.

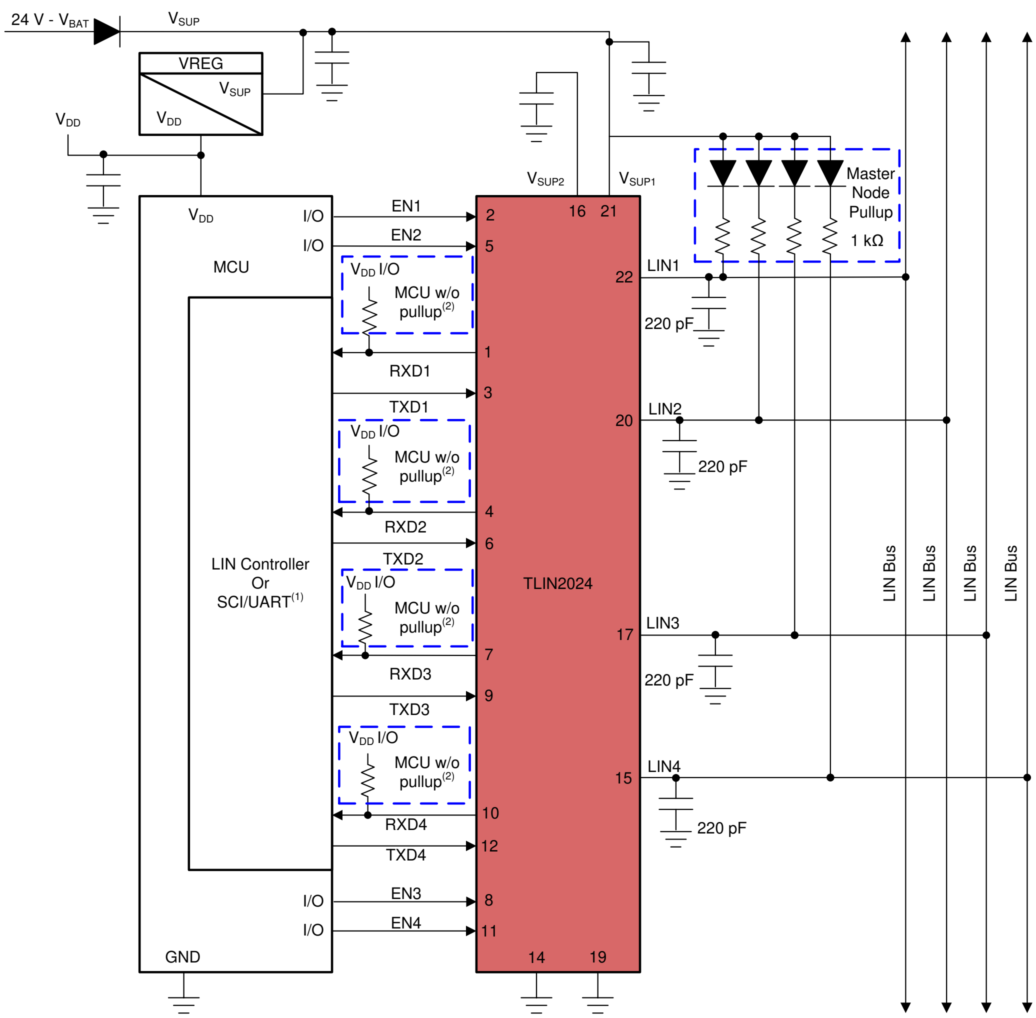


Figure 30. Typical LIN Bus

Typical Application (continued)

9.2.1 Design Requirements

1. RXD on MCU or LIN slave has internal pull-up; no external pull-up resistor is needed.
2. RXD on MCU or LIN slave without internal pull-up requires external pull-up resistor.
3. Master node applications require and external 1 kΩ pull-up resistor and serial diode.
4. Decoupling capacitor values are system dependant but usually have a 100 nF, 1 µF and ≥ 10 µF.

9.2.2 Detailed Design Procedure

The RXD output structure is an open drain output stage. This allows the TLIN2024-Q1 to be used with 3.3 V and 5 V I/O microprocessors. If the RXD pin of the microprocessor does not have an integrated pull-up, an external pull-up resistor to the microprocessor I/O supply voltage is required.

The $V_{SUP1/2}$ pins of the device should be decoupled with a 100 nF capacitor as close to the supply pin on the device as possible.

9.2.2.1 Normal Mode Application Note

When using the TLIN2024-Q1 in systems which are monitoring the RXD pin for a wake up request, special care should be taken during the mode transitions. The output of the RXD pin is indeterminate for the transition period between states as the receivers are switched. The application software should not look for an edge on the RXD pin indicating a wake up request until t_{MODE_CHANGE} plus t_{NOMINT} when going from sleep or standby to normal mode. This is shown in Figure 22

9.2.2.2 Standby Mode Application Note

If the TLIN2024-Q1 detects an under voltage on $V_{SUP1/2}$, the RXD pin transitions low and would signal to the software that the TLIN2024-Q1 is in standby mode and should be returned to sleep mode for the lowest power state.

9.2.2.3 TXD Dominant State Timeout Application Note

The maximum dominant TXD time allowed by the TXD dominant state time out limits the minimum possible data rate of the device. The LIN protocol has different constraints for master and slave applications thus there are different maximum consecutive dominant bits for each application case and thus different minimum data rates.

Typical Application (continued)

9.2.3 Application Curves

and show the propagation delay from the TXD pin to the LIN pin for both dominant to recessive and recessive to dominant stated under lightly loaded conditions.

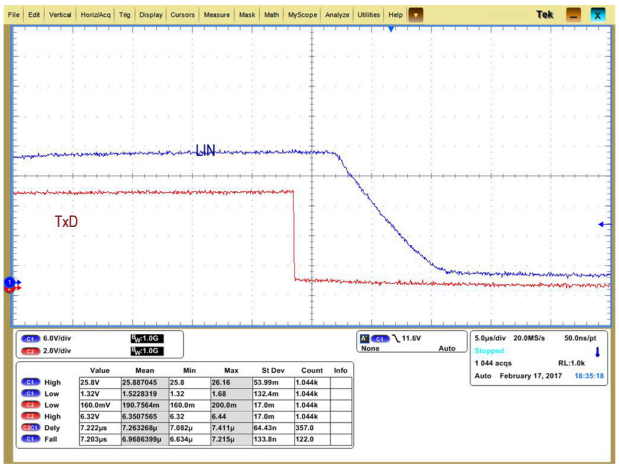


Figure 31. Dominant to Recessive Propagation

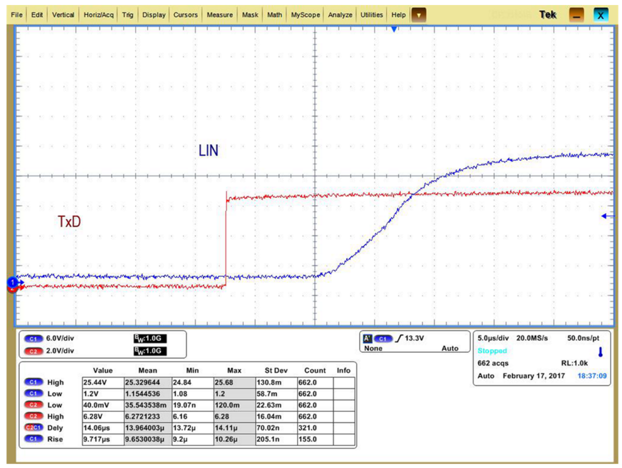


Figure 32. Recessive to Dominant Propagation

10 Power Supply Recommendations

The TLIN2024-Q1 was designed to operate directly off a car battery, or any other DC supply ranging from 4 V to 45 V. A 100 nF decoupling capacitor should be placed as close to the $V_{SUP1/2}$ pin of the device as possible. Most applications will include a 1 µF and ≥ 10 µF decoupling capacitors.

11 Layout

In order for the PCB design to be successful, start with design of the protection and filtering circuitry. Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high frequency layout techniques must be applied during PCB design. Placement at the connector also prevents these noisy events from propagating further into the PCB and system.

11.1 Layout Guidelines

- **Pins 1, 4, 7 and 10 (RXD1/2/3/4):** The pins are open drain outputs and require an external pull-up resistor in the range of 1 kΩ and 10 kΩ to function properly. If the microprocessor paired with the transceiver does not have an integrated pull-up, an external resistor should be placed between RXD and the regulated voltage supply for the microprocessor.
- **Pins 2, 5, 8 and 11 (EN1/2/3/4):** EN is an input pin that is used to place the device in a low power sleep mode. If this feature is not used the pin should be pulled high to the regulated voltage supply of the microprocessor through a series resistor, values between 1 kΩ and 10 kΩ. Additionally, a series resistor may be placed on the pinto limit current on the digital lines in the case of an over voltage fault.
- **Pin 13, 18, 23 and 24 (NC):** Not Connected
- **Pins 3, 6, 9 and 12 (TXD1/2/3/4):** The TXD pins are the transmitter input signals to the device from the microprocessor. A series resistor can be placed to limit the input current to the device in the case of an overvoltage on this pin. A capacitor to ground can be placed close to the input pin of the device to filter noise.
- **Pin 14, 19 (GND2/1):** This is the ground connection for the device. This pin should be tied to the ground plane through a short trace with the use of two vias to limit total return inductance.
- **Pins 22, 20, 17 and 15 (LIN1/2/3/4):** This pin connects to the LIN bus. For slave applications a 220 pF capacitor to ground is implemented. For maser applications and additional series resistor and blocking diode should be placed between the LIN pin and the $V_{SUP1/2}$ pin. See Figure 30.
- **Pin 21, 160 ($V_{SUP1/2}$):** This is the supply pin for the device. A 100 nF decoupling capacitor should be placed as close to the device as possible.

NOTE

All ground and power connections should be made as short as possible and use at least two vias to minimize the total loop inductance.

11.2 Layout Example

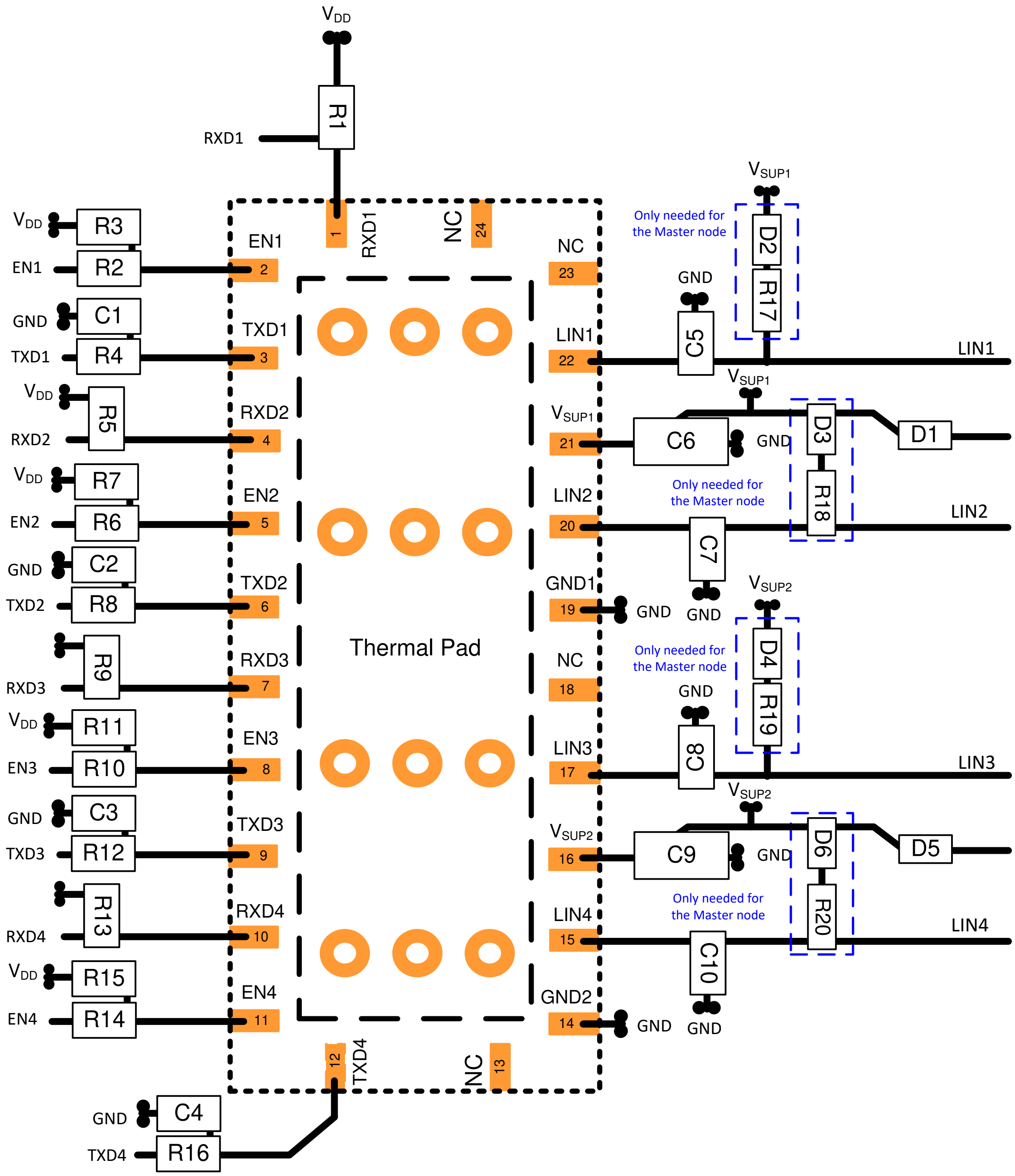


Figure 33. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

This device will conform to the following LIN standards. The core of what is needed is covered within this system spec, however reference should be made to these standards and any discrepancies pointed out and discussed. This document should provide all the basics of what is needed.

12.1.1 Related Documentation

For related documentation see the following:

LIN Standards:

- ISO/DIS 17987-1.2: Road vehicles -- Local Interconnect Network (LIN) -- Part 1: General information and use case definition
- ISO/DIS 17987-4.2: Road vehicles -- Local Interconnect Network (LIN) -- Part 4: Electrical Physical Layer (EPL) specification 12V/24V
- SAE J2602-1: LIN Network for Vehicle Applications

EMC requirements:

- SAE J2962-2: TBD
- ISO 10605: Road vehicles - Test methods for electrical disturbances from electrostatic discharge
- ISO 11452-4:2011: Road vehicles - Component test methods for electrical disturbances from narrowband radiated electromagnetic energy - Part 4: Harness excitation methods
- ISO 7637-1:2015: Road vehicles - Electrical disturbances from conduction and coupling - Part 1: Definitions and general considerations
- ISO 7637-3: Road vehicles - Electrical disturbances from conduction and coupling - Part 3: Electrical transient transmission by capacitive and inductive coupling via lines other than supply lines
- IEC 62132-4:2006: Integrated circuits - Measurement of electromagnetic immunity 150 kHz to 1 GHz - Part 4: Direct RF power injection method
- IEC 6100-4-2
- IEC 61967-4
- CISPR25

Conformance Test requirements:

- ISO/DIS 17987-7.2: Road vehicles -- Local Interconnect Network (LIN) -- Part 7: Electrical Physical Layer (EPL) conformance test specification
- SAE J2602-2: LIN Network for Vehicle Applications Conformance Test

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLIN2024RGYRQ1	PREVIEW	VQFN	RGY	24	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	TL024	
TLIN2024RGYTQ1	PREVIEW	VQFN	RGY	24	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	TL024	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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