

MC74HCT273A

Octal D Flip-Flop with Common Clock and Reset with LSTTL-Compatible Inputs

High-Performance Silicon-Gate CMOS

The MC74HCT273A may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

The HCT273A is identical in pinout to the LS273.

This device consists of eight D flip-flops with common Clock and Reset inputs. Each flip-flop is loaded with a low-to-high transition of the Clock input. Reset is asynchronous and active low.

Features

- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 V to 5.5 V
- Low Input Current: 1.0 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7 A
- Chip Complexity: 284 FETs or 71 Equivalent Gates
- These Devices are Pb-Free and are RoHS Compliant

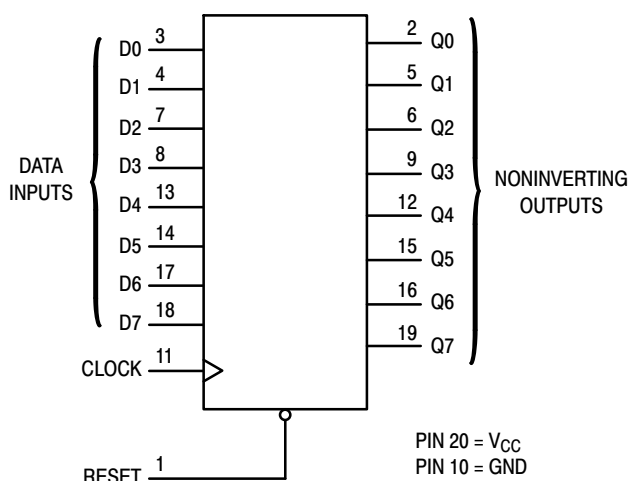
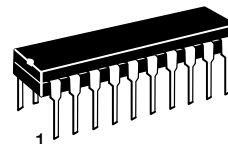


Figure 1. Logic Diagram

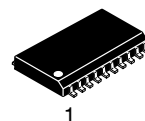


ON Semiconductor®

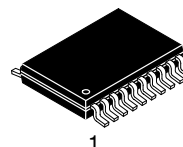
<http://onsemi.com>



PDIP-20
N SUFFIX
CASE 738



SOIC-20W
DW SUFFIX
CASE 751D



TSSOP-20
DT SUFFIX
CASE 948E

PIN ASSIGNMENT

RESET	1	20	V _{CC}
Q0	2	19	Q7
D0	3	18	D7
D1	4	17	D6
Q1	5	16	Q6
Q2	6	15	Q5
D2	7	14	D5
D3	8	13	D4
Q3	9	12	Q4
GND	10	11	CLOCK

FUNCTION TABLE

Inputs			Output
Reset	Clock	D	Q
L	X	X	L
H	↗	H	H
H	↘	L	L
H	L	X	No Change
H	↖	X	No Change

X = Don't Care

Z = High Impedance

ORDERING INFORMATION

See detailed ordering, shipping information, and marking information in the package dimensions section on page 5 of this data sheet.

MC74HCT273A

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air PDIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (SOIC or PDIP)	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} – 0.1 V I _{out} ≤ 20 μA	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} – 0.1 V I _{out} ≤ 20 μA	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA	4.5	3.98	3.84	3.7	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA	4.5	0.26	0.33	0.4	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	5.5	± 0.1	± 1.0	± 1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	5.5	4.0	40	160	μA
ΔI _{CC}	Additional Quiescent Supply Current	V _{in} = 2.4 V, Any One Input V _{in} = V _{CC} or GND, Other Inputs I _{out} = 0 μA	5.5	≥ –55°C	25°C to 125°C		mA
				2.9	2.4		

MC74HCT273A

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0 \text{ V} \pm 10\%$, $C_L = 50 \text{ pF}$, Input $t_r = t_f = 6.0 \text{ ns}$)

Symbol	Parameter	Fig.	Guaranteed Limit			Unit
			- 55 to 25°C	≤ 85°C	≤ 125°C	
$f_{\max}$	Maximum Clock Frequency (50% Duty Cycle)	2, 5	30	24	20	MHz
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Clock to Q	2, 5	25	28	35	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q		25	28	35	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output	2, 5	18	20	22	ns

C _{PD}	Power Dissipation Capacitance (Per Gate)*	Typical @ 25°C, V _{CC} = 5.0 V	pF
		30	

* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

TIMING REQUIREMENTS ($V_{CC} = 5.0 \text{ V} \pm 10\%$, $C_L = 50 \text{ pF}$, Input $t_r = t_f = 6.0 \text{ ns}$)

Symbol	Parameter	Fig.	Guaranteed Limit						Unit
			– 55 to 25°C		≤ 85°C		≤ 125°C		
			Min	Max	Min	Max	Min	Max	
t _{su}	Minimum Setup Time, Data to Clock		10		12		15		ns
t _h	Minimum Hold Time, Clock to Data		3.0		3.0		3.0		ns
t _{rec}	Minimum Recovery Time, Set or Reset Inactive to Clock		5.0		5.0		5.0		ns
t _w	Minimum Pulse Width, Clock	2	12		15		18		ns
t _w	Minimum Pulse Width, Set or Reset		12		15		18		ns
t _r , t _f	Maximum Input Rise and Fall Times	2		500		500		500	ns

SWITCHING WAVEFORMS

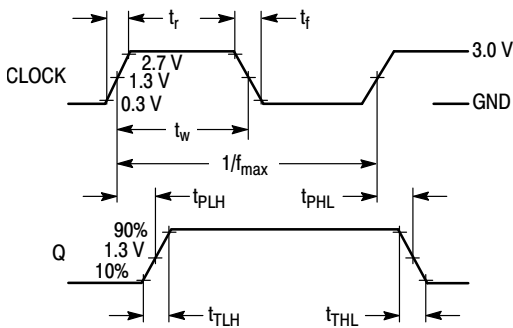


Figure 2.

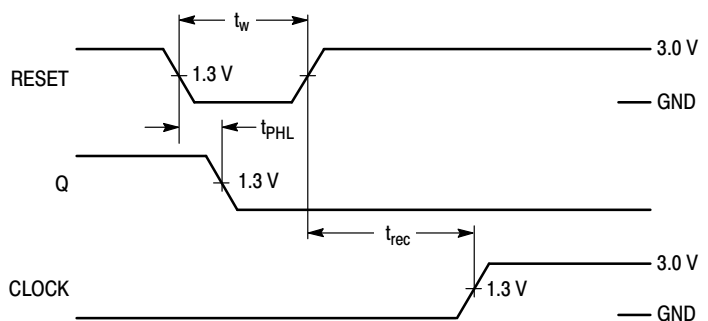


Figure 3.

MC74HCT273A

SWITCHING WAVEFORMS

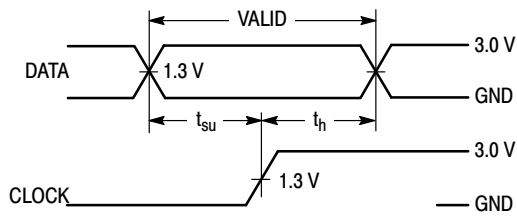
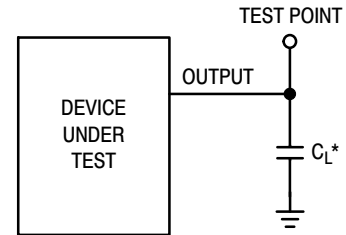


Figure 4.



*Includes all probe and jig capacitance

Figure 5. Test Circuit

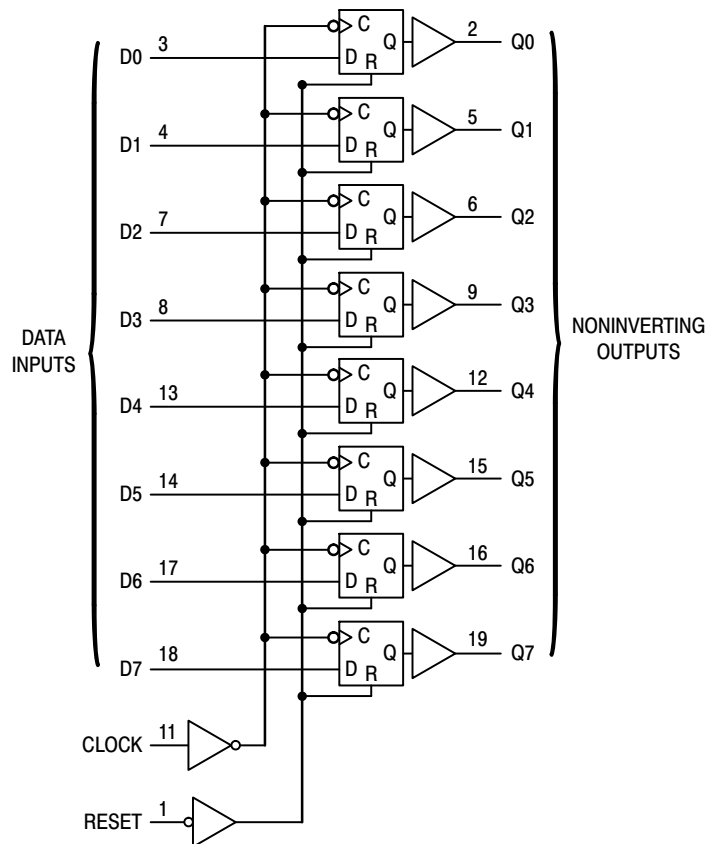


Figure 6. Expanded Logic Diagram

MC74HCT273A

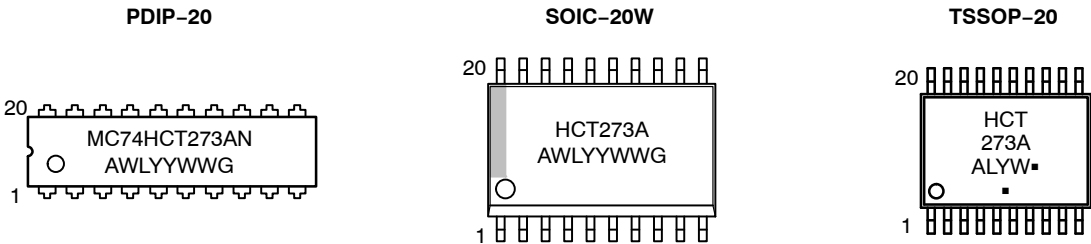
ORDERING INFORMATION

Device	Package	Shipping†
MC74HCT273ANG	PDIP–20 (Pb–Free)	18 Units / Rail
MC74HCT273ADWG	SOIC–20 (Pb–Free)	38 Units / Rail
MC74HCT273ADWR2G	SOIC–20 (Pb–Free)	1000 / Tape & Reel
MC74HCT273ADTR2G	TSSOP–20*	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*These packages are inherently Pb–Free.

MARKING DIAGRAMS



A

= Assembly Location

WL, L

= Wafer Lot

YY, Y

= Year

WW, W

= Work Week

G or ■

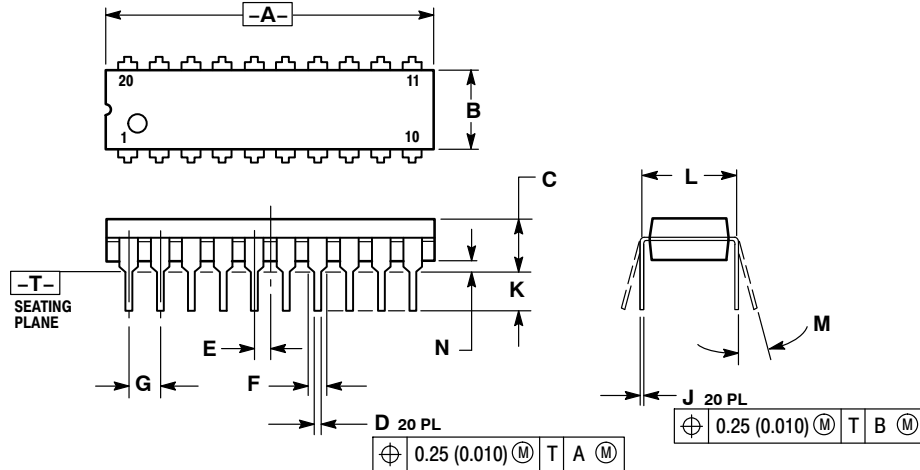
= Pb–Free Package

(Note: Microdot may be in either location)

MC74HCT273A

PACKAGE DIMENSIONS

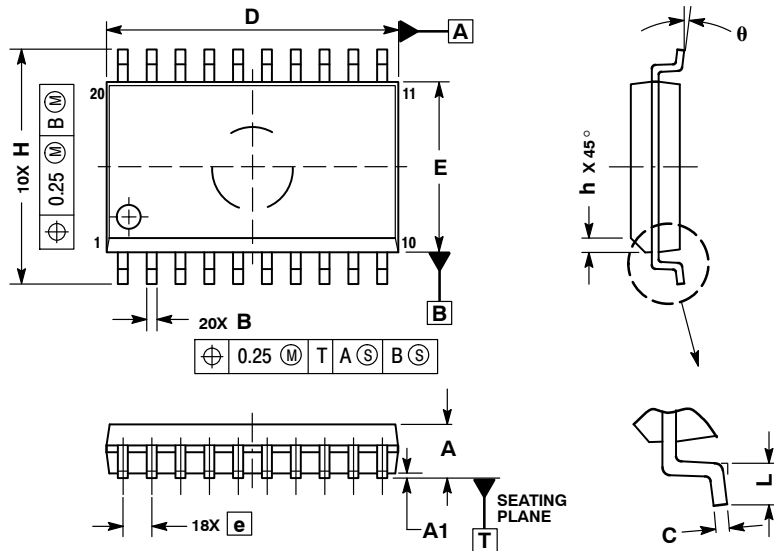
PDIP-20
N SUFFIX
PLASTIC DIP PACKAGE
CASE 738-03
ISSUE E



- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 - CONTROLLING DIMENSION: INCH.
 - DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 - DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

SOIC-20W
DW SUFFIX
CASE 751D-05
ISSUE G



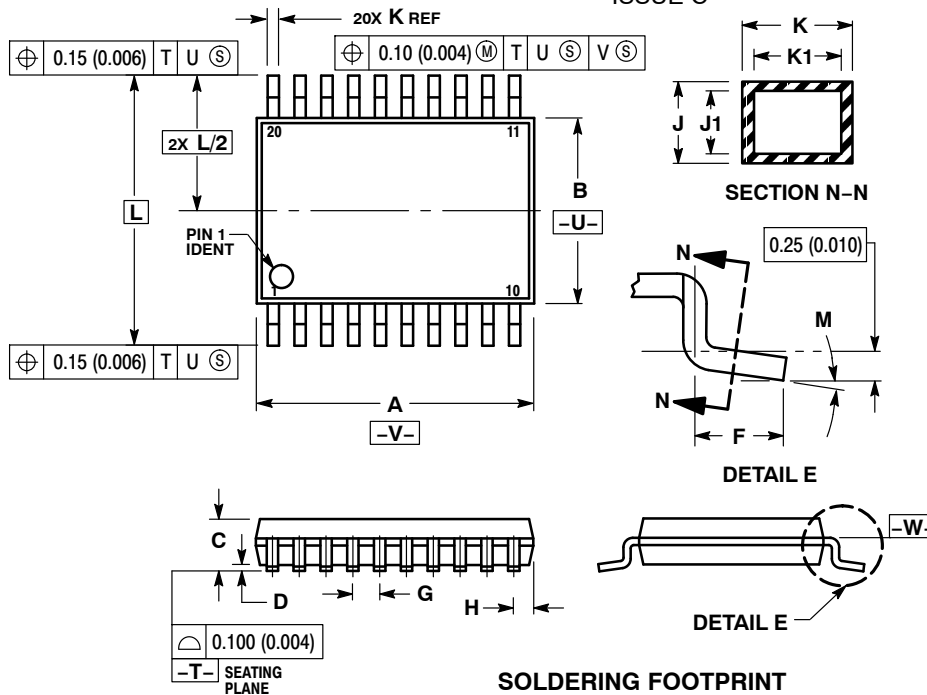
- NOTES:
- DIMENSIONS ARE IN MILLIMETERS.
 - INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 - DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
 - MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
 - DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

MC74HCT273A

PACKAGE DIMENSIONS

TSSOP-20
DT SUFFIX
CASE 948E-02
ISSUE C

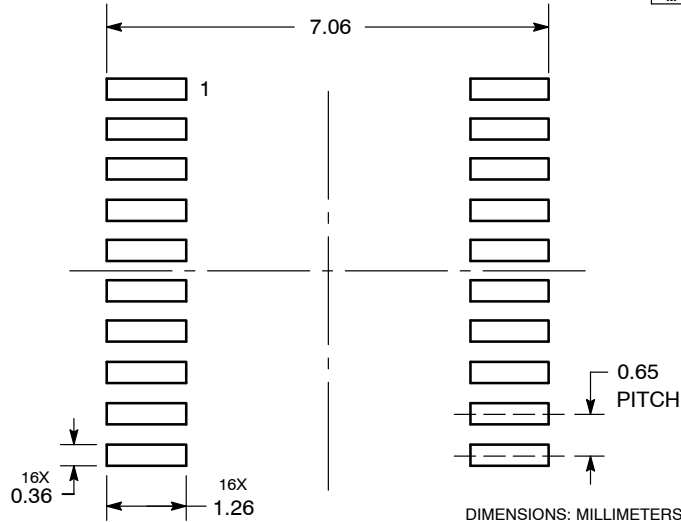


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT



ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative

MC74HCT273A/D