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April 1st, 2010
Renesas Electronics Corporation

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7545 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

REJ03B0140-0107
Rev.1.07
Mar 19, 2009

DESCRIPTION

The 7545 Group is the 8-bit microcomputer based on the 740 family core technology.
The 7545 Group has an 8-bit timer, power-on reset circuit and the voltage drop detection circuit. Also, Function set ROM is equipped.

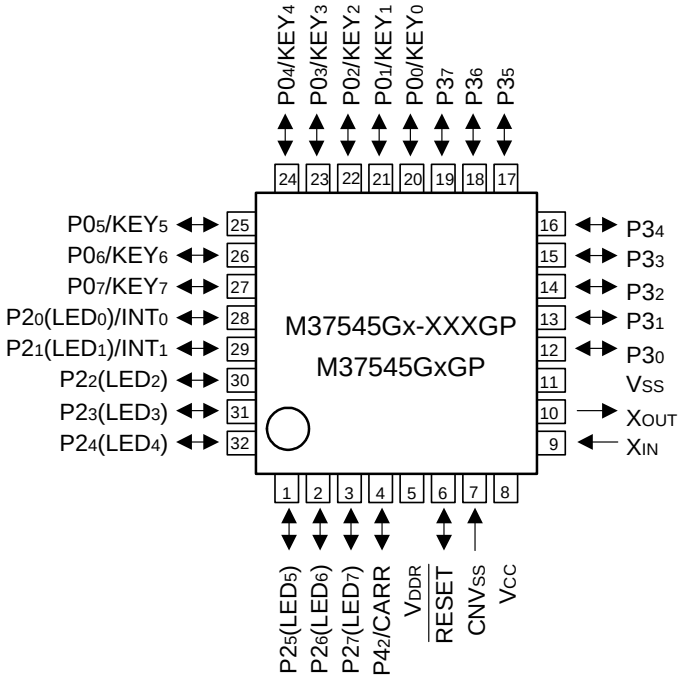
FEATURES

- Basic machine-language instructions 71
- The minimum instruction execution time ..... 2.00 µs
  (at 4 MHz oscillation frequency for the shortest instruction)
- Memory size ROM ..... 4K to 60K bytes
  RAM ..... 256, 512 bytes
- Programmable I/O ports 25
- Key-on wakeup input ..... 8 inputs
- LED output port 8
- Interrupts ..... 7 sources, 7 vectors
- Timers ..... 8-bit × 3
- Carrier wave generating circuit .....1 channel (8-bit timer × 2)
- Clock generating circuit ..... Built-in type
  (connect to external ceramic resonator or quartz-crystal oscillator)
- Watchdog timer ..... 16-bit × 1
- Power-on reset circuit ..... Built-in type
- Voltage drop detection circuit ..... Built-in type
- Power source voltage
  XIN oscillation frequency at ceramic/quartz-crystal oscillation
  At 4 MHz ..... 1.8 to 3.6 V
- Power dissipation 1.8mW
- Operating temperature range ..... −20 to 85 °C

APPLICATION

Remote control transmit.

PIN CONFIGURATION (TOP VIEW)

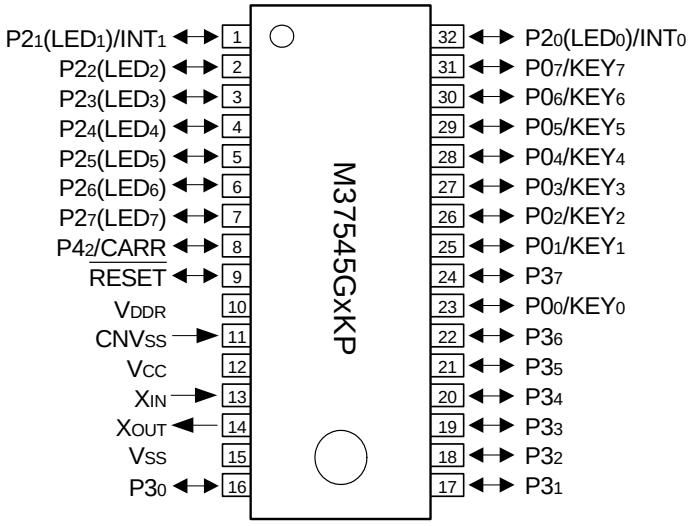


Package type: PLQP0032GB-A (32P6U-A)

Fig. 1 Pin configuration (PLQP0032GB-A type)

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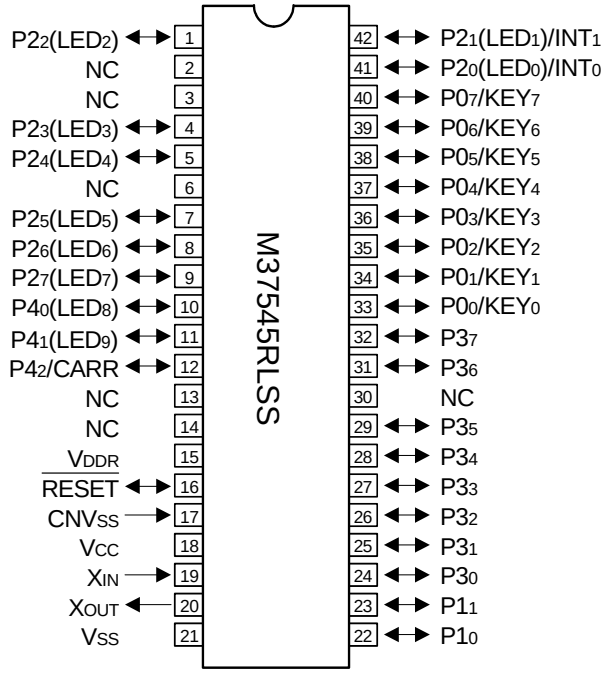
PIN CONFIGURATION (TOP VIEW)



Package type: PLSP0032JB-A

Fig. 2 Pin configuration (PLSP0032JB-A type)

PIN CONFIGURATION (TOP VIEW)



Package type: 42S1M

Fig. 3 Pin configuration (42S1M type)

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Table 1 Performance overview (1)

Parameter			Function
Number of basic instructions			71
Instruction execution time			2.00 μs (Minimum instruction)
Memory sizes	ROM	M37545G1	4096 bytes × 8 bits
		M37545G2	8192 bytes × 8 bits
		M37545G4	16384 bytes × 8 bits
		M37545G6	24576 bytes × 8 bits
		M37545G8	32768 bytes × 8 bits
		M37545GC	49152 bytes × 8 bits
		M37545GF	61440 bytes × 8 bits
	RAM	M37545G1/G2	RAM1: 240 bytes × 8 bits, RAM2: 16 bytes × 8 bits
		M37545G4/G6/G8/GC/GF	RAM1: 384 bytes × 8 bits, RAM2: 128 bytes × 8 bits
I/O port	$P0_0$–$P0_7$	I/O	• 1-bit × 8 • CMOS compatible input level • CMOS 3-state output structure • Whether the pull-up function/key-on wakeup function is to be used or not can be determined by program.
	$P1_0$, $P1_1$	I/O (RLSS-only pin)	• 1-bit × 2 • CMOS compatible input level • The output structure can be switched to N-channel open-drain or CMOS by software.
	$P2_0$–$P2_7$	I/O	• 1-bit × 8 • CMOS compatible input level • The output structure can be switched to N-channel open-drain or CMOS by software. • P2 can output a large current for driving LED. • $P2_0$ and $P2_1$ are also used as INT_0 and INT_1, respectively.
	$P3_0$–$P3_7$	I/O	• 1-bit × 8 • CMOS compatible input level • The output structure can be switched to N-channel open-drain or CMOS by software.
	$P4_0$, $P4_1$	I/O (RLSS-only pin)	• 1-bit × 2 • CMOS compatible input level • CMOS 3-state output structure
	$P4_2$	I/O	• 1-bit × 1 • CMOS compatible input level • CMOS 3-state output structure • Carrier wave output pin for remote-control transmitter
Timer	Timer 1		8-bit timer with timer 1 latch Count source is Prescaler output.
	Timer 2		8-bit timer with timer 2 primary latch and timer 2 secondary latch Count source can be selected from $f(X_{IN})/16$, $f(X_{IN})/8$, $f(X_{IN})/2$ or $f(X_{IN})/1$.
	Timer 3		8-bit timer with timer 3 latch Count source can be selected from $f(X_{IN})/16$, $f(X_{IN})/8$ or $f(X_{IN})/2$ or carrier wave output.
Carrier wave generating circuit			Remote-control waveform is generated by using timer 2 and timer 3. 455 kHz carrier wave generating mode is available.
Watchdog timer			16-bit × 1
Power-on reset circuit			Built-in
Voltage drop detection circuit (Not available for RLSS)			Typ. 1.75 V (Ta=25 °C)
Interrupt	Source		7 sources (External × 3, Timer × 3, Software)
Function set ROM area	Function set ROM		Function set ROM is assigned to address $FFDA_{16}$. Enable/disable of watchdog timer and STP instruction can be selected. Valid/invalid of voltage drop detection circuit can be selected.
	ROM code protect		ROM code protect is assigned to address $FFDB_{16}$. Read/write the built-in QzROM by serial programmer is disabled by setting "00" to ROM code protect.
Device structure			CMOS silicon gate
Package			32-pin plastic molded LQFP (PLQP0032GB-A) 32-pin plastic molded SSOP (PLSP0032JB-A)
Operating temperature range			−20 to 85 °C
Power source voltage	$f(X_{IN})$ = 4 MHz		1.8 to 3.6 V

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Table 2 Performance overview (2)

Parameter		Function
Power dissipation	At CPU active	Typ. 0.6 mA ($f(X_{IN})$=4 MHz, Vcc=3.0 V, output transistors “off”)
	At WIT instruction executed	Typ. 0.3 mA ($f(X_{IN})$=4 MHz, Vcc=3.0 V, output transistors “off” , in WIT state, function except timer 1 disabled)
	At STP instruction executed	Typ. 0.1 μA (Ta = 25 °C, $V_{CC} \geq V_{DDR} \geq V_{CC}$–0.6 V, output transistors “off”, in STP state, all oscillation stopped)
	During reset by voltage drop detection circuit	Typ. 0.1 μA (Ta = 25 °C, V_{DDR} = 1.1 V, 1.8 V ≥ V_{CC} ≥ 0V)

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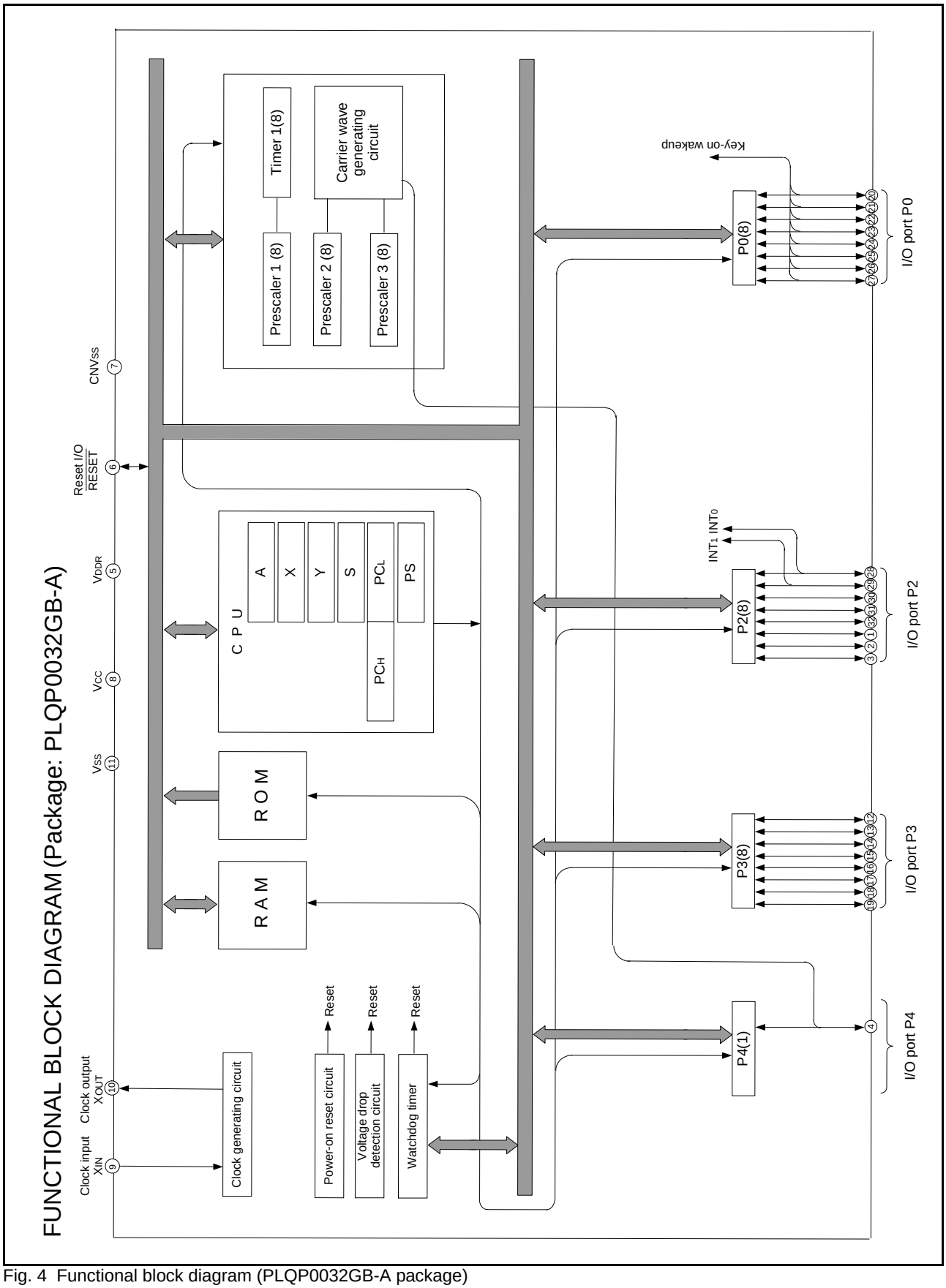


Fig. 4 Functional block diagram (PLQP0032GB-A package)

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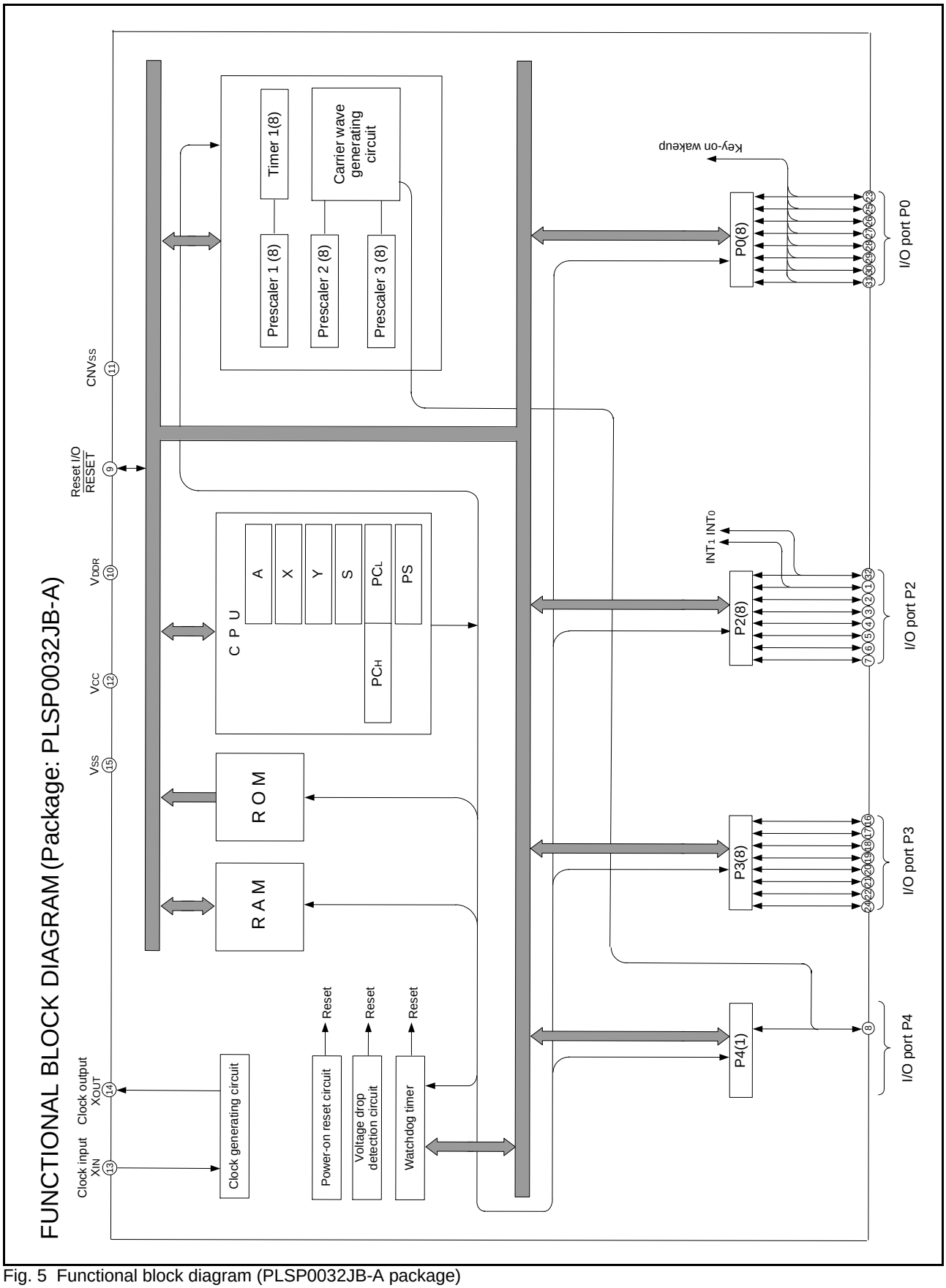


Fig. 5 Functional block diagram (PLSP0032JB-A package)

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PIN DESCRIPTION

Table 3 Pin description

Pin	Name	Function	Function expect a port function
V_{CC}, V_{SS}	Power source	• Apply voltage of 1.8 to 3.6V to V_{CC}, and 0 V to V_{SS}.	
V_{DDR}	Power source	• Power source pin only for RAM2. When this pin is used, connect an approximately 0.1 μF bypass capacitor across the V_{SS} line and the V_{DDR} line. When not used, connect it to V_{SS}.	
CNVss	CNVss	• Chip operating mode control pin, which is always connected to Vss.	
$\overline{\text{RESET}}$	Reset I/O	• An N-channel open-drain I/O pin for a system reset. This pin has a pull-up transistor. When the watchdog timer, the built-in power-on reset or the voltage drop detection circuit causes the system to be reset, the $\overline{\text{RESET}}$ pin outputs "L" level.	
X_{IN}	Clock input	• Input and output pins for main clock generating circuit • Connect a ceramic resonator or quartz-crystal oscillator between the X_{IN} and X_{OUT} pins.	
X_{OUT}	Clock output		
$P0_0$/KEY_0– $P0_7$/KEY_7	I/O port P0	• 8-bit I/O port. • I/O direction register allows each pin to be individually programmed as either input or output. • CMOS compatible input level • CMOS 3-state output structure • Whether the pull-up function/key-on wakeup function is to be used or not can be determined by program.	• Key-input (key-on wake up interrupt input) pins
$P1_0$, $P1_1$	I/O port P1	• 2-bit I/O port having almost the same function as P0. • CMOS compatible input level • The output structure can be switched to N-channel open-drain or CMOS by software.	Note: RLSS-only pins
$P2_0$(LED_0)/INT_0 $P2_1$(LED_1)/INT_1 $P2_2$(LED_2)– $P2_7$(LED_7)	I/O port P2	• 8-bit I/O port having almost the same function as P0. • CMOS compatible input level • The output structure can be switched to N-channel open-drain or CMOS by software. • P2 can output a large current for driving LED.	• Interrupt input pins
$P3_0$–$P3_7$	I/O port P3	• 8-bit I/O port • I/O direction register allows each pin to be individually programmed as either input or output. • CMOS compatible input level • The output structure can be switched to N-channel open-drain or CMOS by software.	
$P4_0$(LED_8), $P4_1$(LED_9)	I/O port P4	• 2-bit I/O port having almost the same function as P0. • CMOS compatible input level • CMOS 3-state output structure	Note: RLSS-only pins
$P4_2$/CARR		• 1-bit I/O port • CMOS compatible input level • CMOS 3-state output structure	• Carrier wave output pin for remote-control transmit

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GROUP EXPANSION

We are planning to expand the 7545 group as follow:

Memory Type

Support for QzROM version and emulator MCU.

Memory Size

- ROM size ..... 4 K to 60 K bytes
- RAM size ..... 256, 512 bytes

Packages

- PLQP0032GB-A ... 0.8 mm-pitch 32-pin plastic molded LQFP
- PLSP0032JB-A ... 0.65 mm-pitch 32-pin plastic molded SSOP
- 42S1M .....42-pin shrink ceramic PIGGY BACK

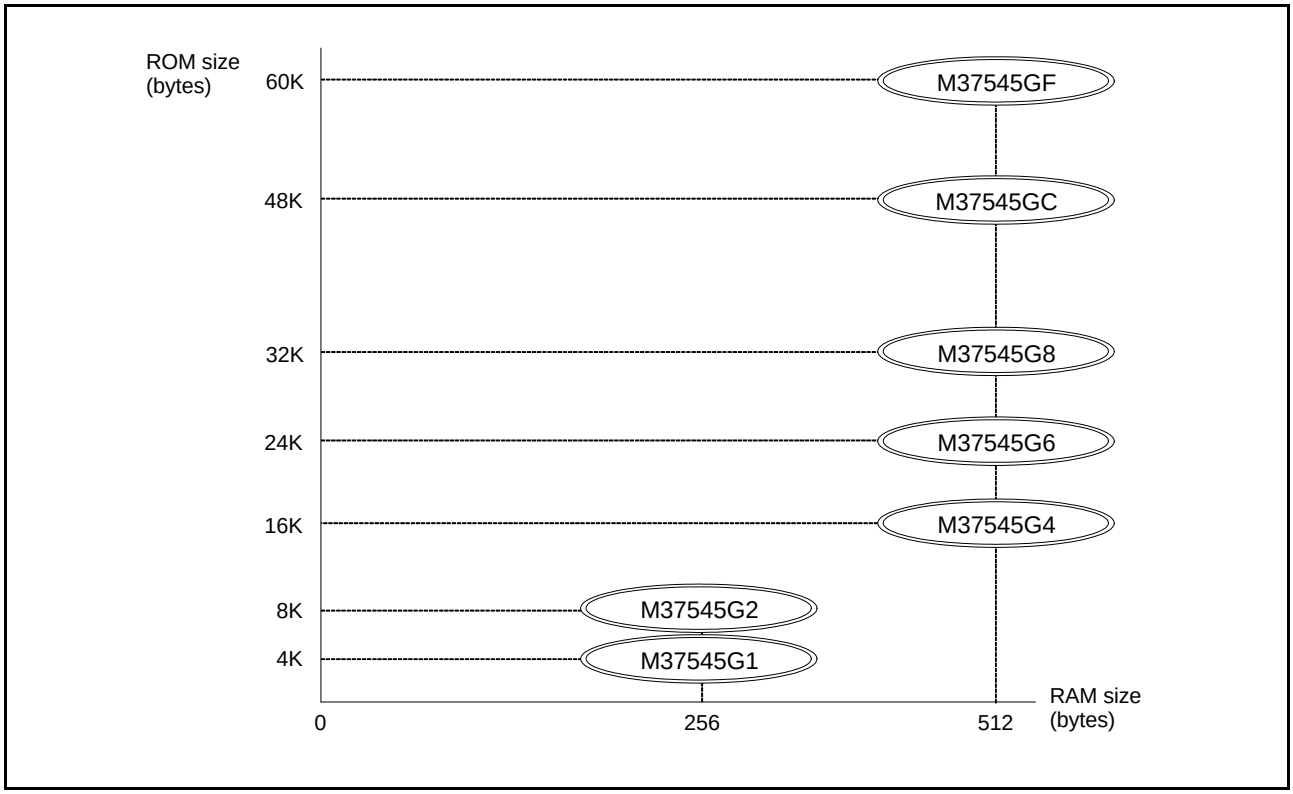


Fig. 6 Memory expansion plan

Currently supported products are listed below.

Table 4 List of supported products

Part number	ROM size (bytes) ROM size for User ( )	RAM size (bytes)	Package	Remarks
M37545G1KP	4096 (3966)	256	PLSP0032JB-A	QzROM version (blank)
M37545G2KP	8192 (8062)		PLSP0032JB-A	QzROM version (blank)
M37545G4-XXXGP	16384 (16254)	512	PLQP0032GB-A	QzROM version
M37545G4GP				QzROM version (blank)
M37545G4KP			PLSP0032JB-A	QzROM version (blank)
M37545G6-XXXGP	24576 (24446)		PLQP0032GB-A	QzROM version
M37545G6GP				QzROM version (blank)
M37545G6KP			PLSP0032JB-A	QzROM version (blank)
M37545G8-XXXGP	32768 (32638)		PLQP0032GB-A	QzROM version
M37545G8GP				QzROM version (blank)
M37545G8KP			PLSP0032JB-A	QzROM version (blank)
M37545GC-XXXGP	49152 (49022)		PLQP0032GB-A	QzROM version
M37545GCGP				QzROM version (blank)
M37545GF-XXXGP	61440 (61310)		PLQP0032GB-A	QzROM version
M37545GFGP				QzROM version (blank)
M37545RLSS	———		42S1M	Emulator MCU

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FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The MCU uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine-language instructions or the SERIES 740 <SOFTWARE> USER'S MANUAL for details on each instruction set.
Machine-resident 740 family instructions are as follows:

1. The FST and SLW instructions cannot be used.
2. The MUL and DIV instructions can be used.
3. The WIT instruction can be used.
4. The STP instruction can be used.

This instruction cannot be used while CPU operates by an on-chip oscillator.

[Accumulator (A)]

The accumulator is an 8-bit register. Data operations such as data transfer, etc., are executed mainly through the accumulator.

[Index register X (X), Index register Y (Y)]

Both index register X and index register Y are 8-bit registers. In the index addressing modes, the value of the OPERAND is added to the contents of register X or register Y and specifies the real address.
When the T flag in the processor status register is set to "1", the value contained in index register X becomes the address for the second OPERAND.

[Stack pointer (S)]

The stack pointer is an 8-bit register used during subroutine calls and interrupts. The stack is used to store the current address data and processor status when branching to subroutines or interrupt routines.
The lower eight bits of the stack address are determined by the contents of the stack pointer. The upper eight bits of the stack address are determined by the Stack Page Selection Bit. If the Stack Page Selection Bit is "0", then the RAM in the zero page is used as the stack area. If the Stack Page Selection Bit is "1", then RAM in page 1 is used as the stack area.
The Stack Page Selection Bit is located in the SFR area in the zero page. Note that the initial value of the Stack Page Selection Bit varies with each microcomputer type. Also some microcomputer types have no Stack Page Selection Bit and the upper eight bits of the stack address are fixed. The operations of pushing register contents onto the stack and popping them from the stack are shown in Figure 8.

[Program counter (PC)]

The program counter is a 16-bit counter consisting of two 8-bit registers PC_H and PC_L. It is used to indicate the address of the next instruction to be executed.

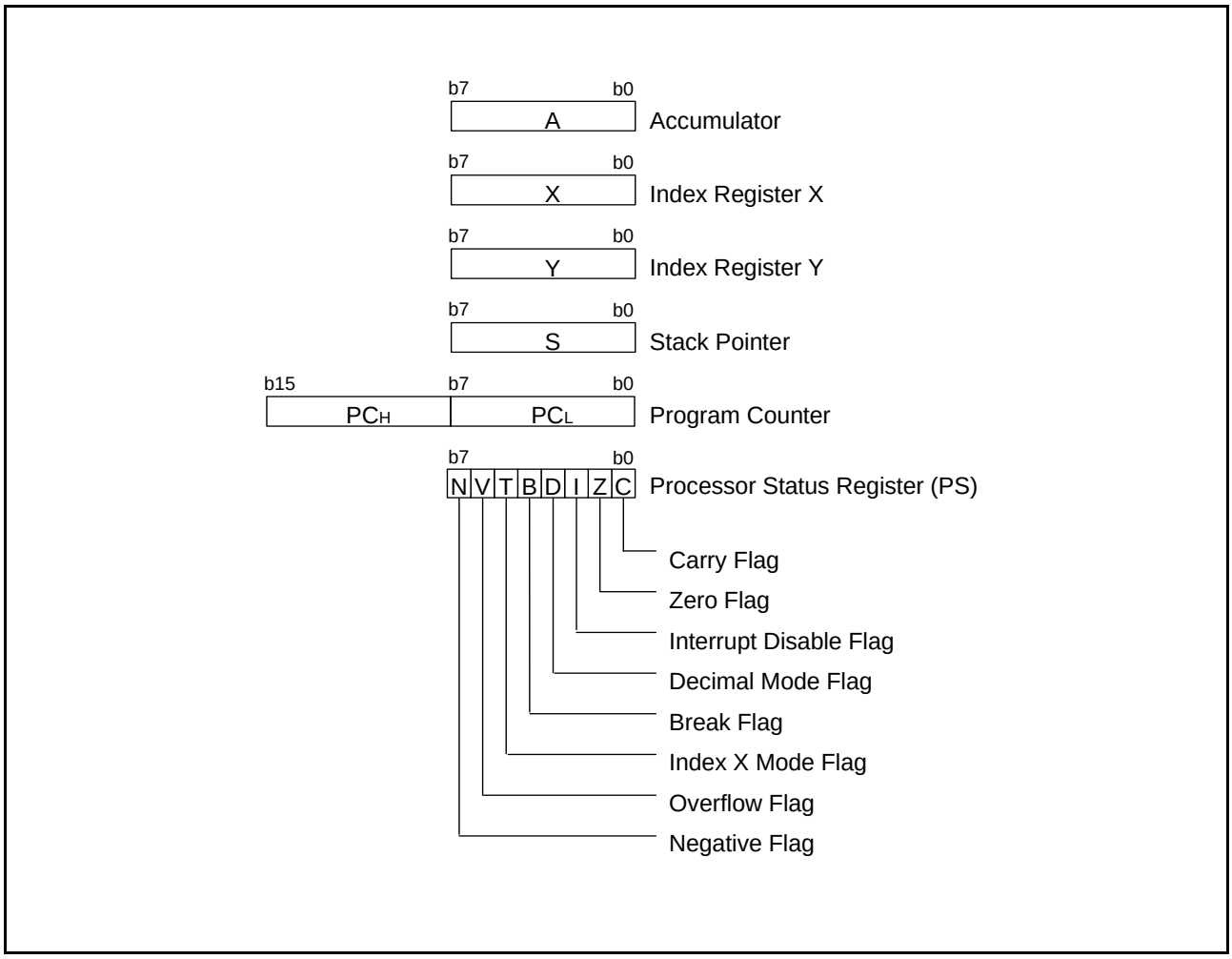


Fig. 7 740 Family CPU register structure

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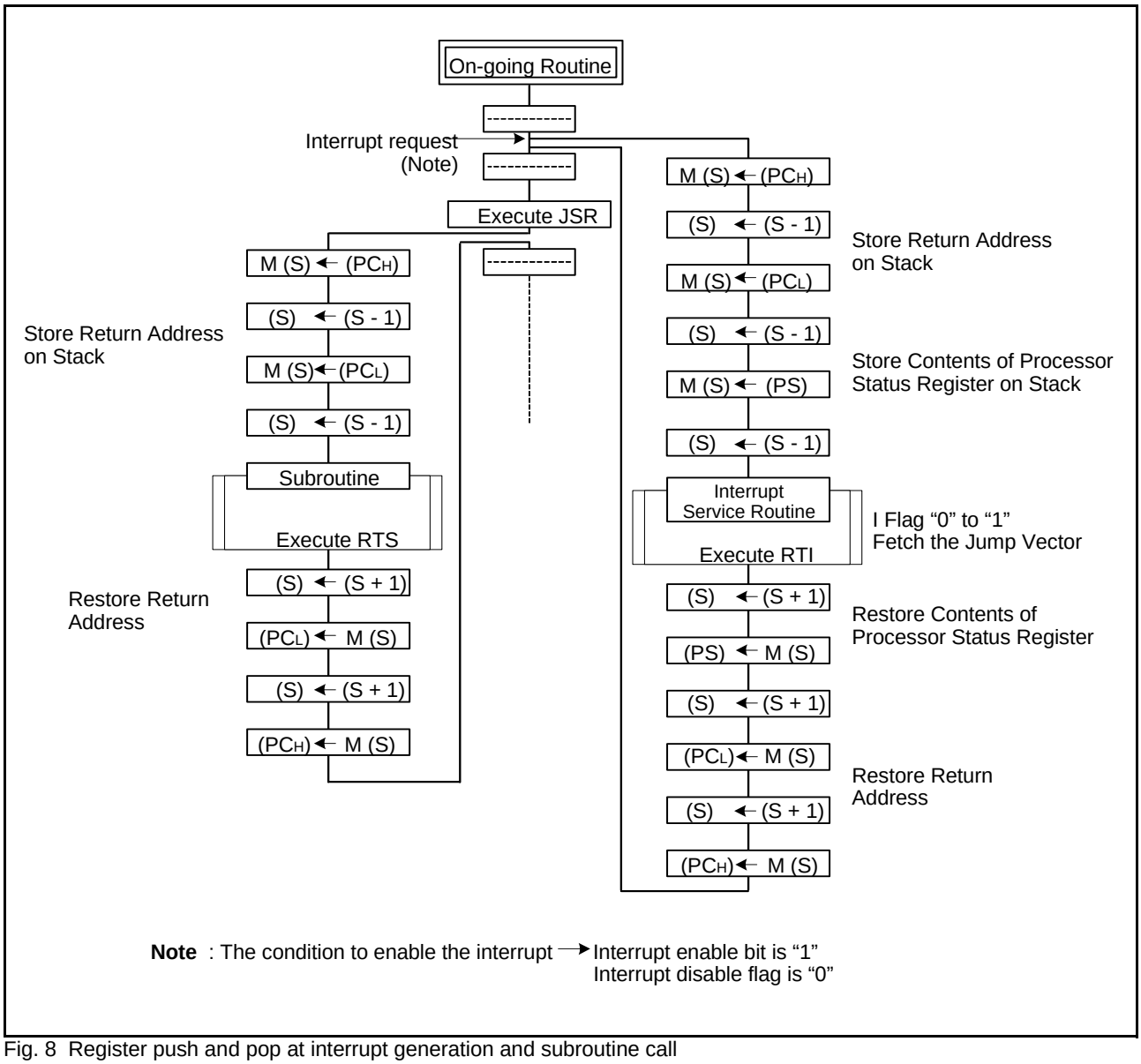


Fig. 8 Register push and pop at interrupt generation and subroutine call

Table 5 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

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[Processor status register (PS)]

The processor status register is an 8-bit register consisting of flags which indicate the status of the processor after an arithmetic operation. Branch operations can be performed by testing the Carry (C) flag, Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

After reset, the Interrupt disable (I) flag is set to "1", but all other flags are undefined. Since the Index X mode (T) and Decimal mode (D) flags directly affect arithmetic operations, they should be initialized in the beginning of a program.

Bit 0: Carry flag (C)

The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.

Bit 1: Zero flag (Z)

The Z flag is set if the result of an immediate arithmetic operation or a data transfer is "0", and cleared if the result is anything other than "0".

Bit 2: Interrupt disable flag (I)

The I flag disables all interrupts except for the interrupt generated by the BRK instruction. Interrupts are disabled when the I flag is "1".

When an interrupt occurs, this flag is automatically set to "1" to prevent other interrupts from interfering until the current interrupt is serviced.

Bit 3: Decimal mode flag (D)

The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is "0"; decimal arithmetic is executed when it is "1".

Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can be used for decimal arithmetic.

Bit 4: Break flag (B)

The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always "0". When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to "1". The saved processor status is the only place where the break flag is ever set.

Bit 5: Index X mode flag (T)

When the T flag is "0", arithmetic operations are performed between accumulator and memory. When the T flag is "1", direct arithmetic operations and direct data transfers are enabled between memory locations.

Bit 6: Overflow flag (V)

The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.

Bit 7: Negative flag (N)

The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 6 Set and clear instructions of each bit of processor status register

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	–	SEI	SED	–	SET	–	–
Clear instruction	CLC	–	CLI	CLD	–	CLT	CLV	–

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[CPU mode register (CPUM)]

The CPU mode register contains the stack page selection bit.
This register is allocated at address 003B16.
For this product, the clock speed of CPU is always f(XIN)/4.

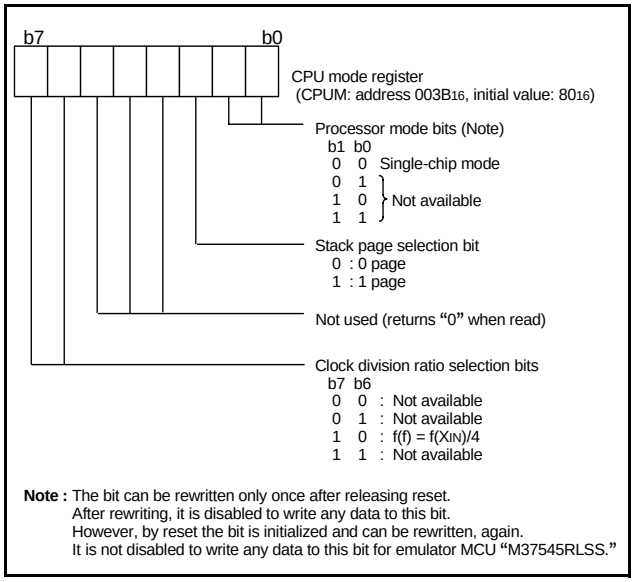


Fig. 9 Structure of CPU mode register

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MEMORY

Special Function Register (SFR) Area

The SFR area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for a stack area of subroutine calls and interrupts. RAM consists of RAM1 and RAM2. The power source for RAM1 is supplied from V_{CC} pin. The power source for RAM2 is supplied from V_{DDR} pin.

Note: When the V_{DDR} pin is used, connect an approximately 0.1 μF bypass capacitor across the V_{SS} line and the V_{DDR} line. When not used, connect it to V_{SS}.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is a user area for storing programs.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.
The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

Function Set ROM Area

[Renesas shipment test area]

Figure 10 shows the Assignment of Function set ROM area.
The random data are set to the Renesas shipment test areas (addresses $FFD4_{16}$ to address $FFD9_{16}$).
Do not rewrite the data of these areas.
When the checksum is included in the user program, avoid assigning it to these areas.

[Function set ROM data] FSROM

Function set ROM data (address $FFDA_{16}$) is used to set modes of peripheral functions. By setting this area, the operation mode of each peripheral function are set after system is released from reset.
Refer to the descriptions of peripheral functions for the details of operation of peripheral functions.

- Watchdog timer
- Low voltage detection circuit

This mode setting of peripheral functions cannot be changed by program after system is released from reset.

ROM Code Protect Address (address $FFDB_{16}$)

Address $FFDB_{16}$, which is the reserved ROM area of QzROM, is the ROM code protect address. "00_{16}" is written into this address when selecting the protect bit write by using a serial programmer or selecting protect enabled for writing shipment by Renesas Technology corp.. When "00_{16}" is set to the ROM code protect address, the protect function is enabled, so that reading or writing from/to QzROM is disabled by a serial programmer.
As for the QzROM product in blank, the ROM code is protected by selecting the protect bit write at ROM writing with a serial programmer.
As for the QzROM product shipped after writing, "00_{16}" (protect enabled) or "FF_{16}" (protect disabled) is written into the ROM code protect address when Renesas Technology corp. performs writing.
The writing of "00_{16}" or "FF_{16}" can be selected as the ROM option setup (referred to as "Mask option setup" in MM) when ordering.

<Notes>

1. Because the contents of RAM are indefinite at reset, set initial values before using.
2. Do not access to the reserved area.
3. Random data is written into the Renesas shipment test area and the reserved ROM area. Do not rewrite the data in these areas. Data of these area may be changed without notice. Accordingly, do not include these areas into programs such as checksum of all ROM areas.
4. The QzROM values in function set ROM data set the operating modes of the various peripheral functions after an MCU reset is released. Do not fail to set the value for the selected function. Bits designated with a fixed value of 1 or 0 must be set to the designated value.
5. Emulator MCU: As for M37545RLSS, set "$010000XX_2$" to Function set ROM data (address $FFDA_{16}$). Also, set "FF_{16}" to ROM code protect (address $FFDB_{16}$).

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RAM 1 area

RAM capacity (bytes)	address WWWW16
240	012F16
384	01BF16

RAM 2 area

RAM capacity (bytes)	address XXXX16
16	01CF16
128	023F16

ROM area

ROM capacity (bytes)	address YYYY16	address ZZZZ16
4096	F00016	F08016
8192	E00016	E08016
16384	C00016	C08016
24576	A00016	A08016
32768	800016	808016
49152	400016	408016
61440	100016	108016

Function set ROM area

Address	
FFD416	Renesas shipment test area
FFD516	Reserved ROM area
FFD616	Reserved ROM area
FFD716	Reserved ROM area
FFD816	Reserved ROM area
FFD916	Reserved ROM area
FFDA16	Function set ROM data
FFDB16	ROM code protect

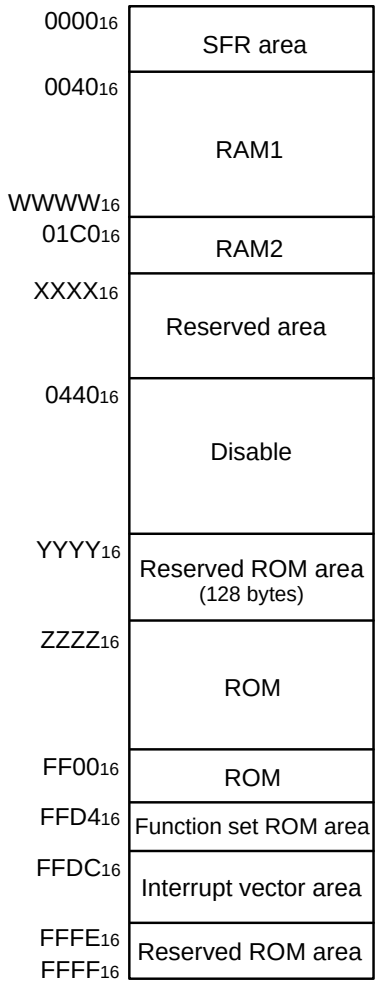


Fig. 10 Memory map diagram

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0000_{16}	Port P0 (P0)	0020_{16}	Reserved
0001_{16}	Port P0 direction register (P0D)	0021_{16}	Reserved
0002_{16}	Port P1 (P1)	0022_{16}	Reserved
0003_{16}	Port P1 direction register (P1D)	0023_{16}	Reserved
0004_{16}	Port P2 (P2)	0024_{16}	Reserved
0005_{16}	Port P2 direction register (P2D)	0025_{16}	Reserved
0006_{16}	Port P3 (P3)	0026_{16}	Reserved
0007_{16}	Port P3 direction register (P3D)	0027_{16}	Carrier wave control register (CARCNT)
0008_{16}	Port P4 (P4)	0028_{16}	Prescaler 1 (PRE1)
0009_{16}	Port P4 direction register (P4D)	0029_{16}	Timer 1 (T1)
$000A_{16}$	Reserved	$002A_{16}$	Timer count source set register (TCSS)
$000B_{16}$	Reserved	$002B_{16}$	Timer 1,2,3 control register (TC123)
$000C_{16}$	Reserved	$002C_{16}$	Timer 2 primary (T2P)
$000D_{16}$	Reserved	$002D_{16}$	Timer 2 secondary (T2S)
$000E_{16}$	Reserved	$002E_{16}$	Timer 3 (T3)
$000F_{16}$	Reserved	$002F_{16}$	Reserved
0010_{16}	Reserved	0030_{16}	Reserved
0011_{16}	Reserved	0031_{16}	Reserved
0012_{16}	Reserved	0032_{16}	Reserved
0013_{16}	Reserved	0033_{16}	Reserved
0014_{16}	Reserved	0034_{16}	Reserved
0015_{16}	Reserved	0035_{16}	Reserved
0016_{16}	Pull-up control register (PULL)	0036_{16}	Reserved
0017_{16}	Port output mode selection register (PMOD)	0037_{16}	Reserved
0018_{16}	Key-on wakeup pin selection register (KEYSEL)	0038_{16}	MISRG
0019_{16}	Key-on wakeup edge selection register (KEYEDGE)	0039_{16}	Watchdog timer control register (WDTCON)
$001A_{16}$	Reserved	$003A_{16}$	Interrupt edge selection register (INTEDGE)
$001B_{16}$	Reserved	$003B_{16}$	CPU mode register (CPUM)
$001C_{16}$	Reserved	$003C_{16}$	Interrupt request register 1 (IREQ1)
$001D_{16}$	Reserved	$003D_{16}$	Reserved
$001E_{16}$	Reserved	$003E_{16}$	Interrupt control register 1 (ICON1)
$001F_{16}$	Reserved	$003F_{16}$	Reserved

Note : Do not access to the SFR area including nothing.

Fig. 11 Memory map of special function register (SFR)

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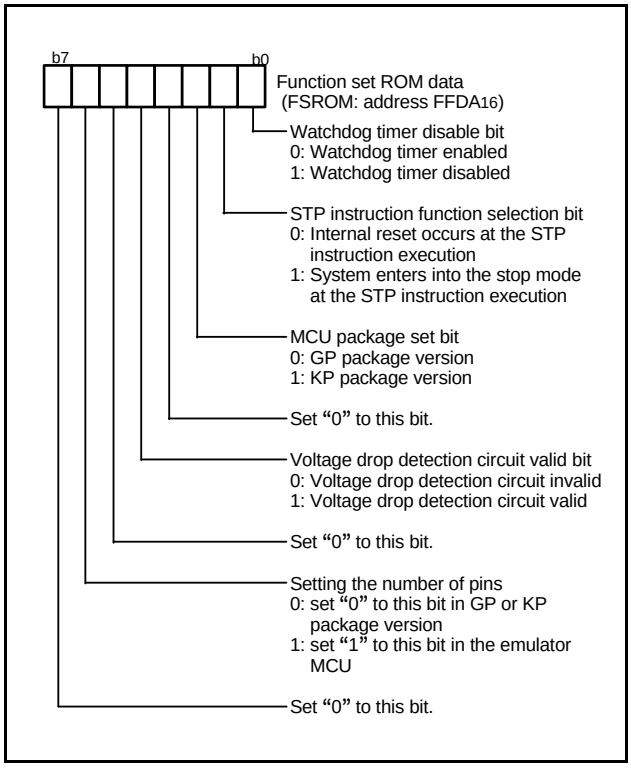


Fig. 12 Structure of Function set ROM area

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I/O PORTS

[Direction registers] PiD

The I/O ports have direction registers which determine the input/output direction of each pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input or output.

When "1" is set to the bit corresponding to a pin, this pin becomes an output port. When "0" is set to the bit, the pin becomes an input port.

When data is read from a pin set to output, not the value of the pin itself but the value of port latch is read. Pins set to input are floating, and permit reading pin values.

If a pin set to input is written to, only the port latch is written to and the pin remains floating.

[Pull-up control register] Pull

By setting the pull-up control register (address 0016_{16}), port P0 can exert pull-up control by program. However, pins set to output are disconnected from this control and cannot exert pull-up control.

[Port output mode selection register] PMOD

By setting the port output mode selection register (address 0017_{16}), CMOS output or N-channel open-drain can be selected for ports P1, P2, P3 by program.

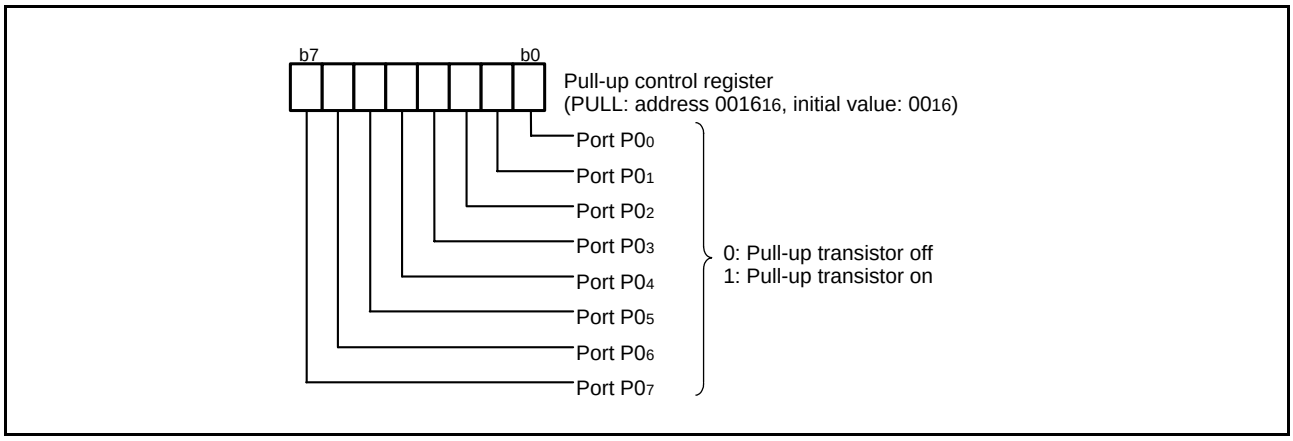


Fig. 13 Structure of pull-up control register

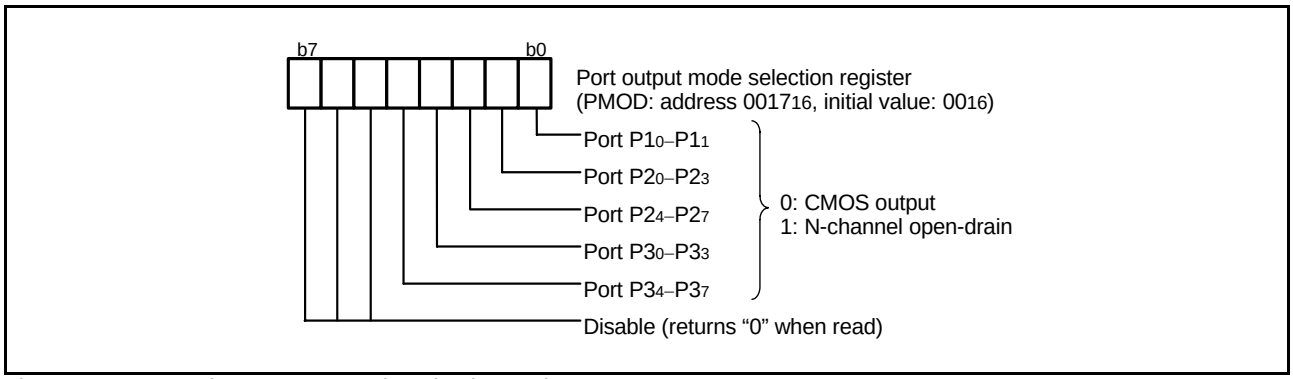


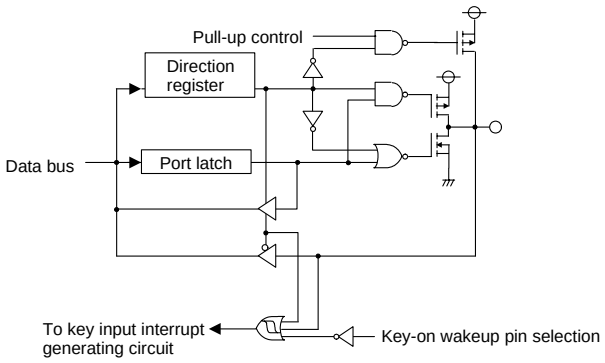
Fig. 14 Structure of port output mode selection register

Table 7 I/O port function table

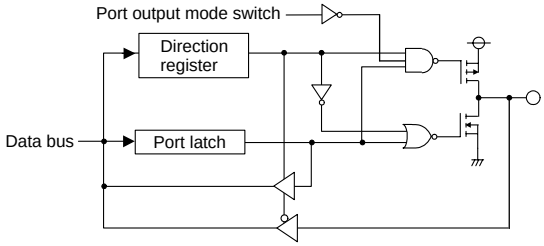
Pin	Name	Input/Output	I/O format	Non-port function	Related SFRs	Diagram No.
P00–P07	Port P0	I/O individual bits	• CMOS compatible input level • CMOS 3-state output	Key input interrupt	Pull-up control register Key-on wakeup pin selection register Key-on wakeup edge selection register	(1)
P10–P11	Port P1		• CMOS compatible input level • CMOS 3-state output or N-channel open drain	RLSS-only pin	Port output mode selection register	(2)
P20/INT0 P21/INT1	Port P2			External interrupt input	Interrupt edge selection register Port output mode selection register	(3)
P22–P27					Port output mode selection register	(2)
P30–P37	Port P3				Port output mode selection register	(2)
P40, P41	Port P4		• CMOS compatible input level • CMOS 3-state output	RLSS-only pin		(4)
P42/CARR				Carrier wave output for remote-control transmitter	Carrier wave control register	(5)

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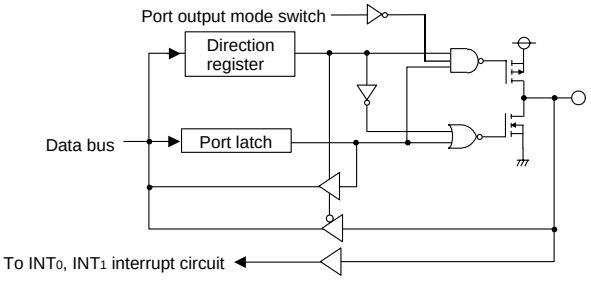
(1) Ports $P0_0$-$P0_7$



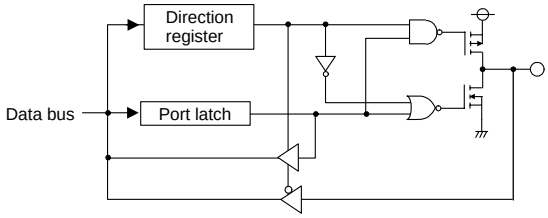
(2) Ports $P1_0$-$P1_1$, $P2_2$-$P2_7$, $P3_0$-$P3_7$



(3) Ports $P2_0$, $P2_1$



(4) Ports $P4_0$, $P4_1$



(5) Port $P4_2$

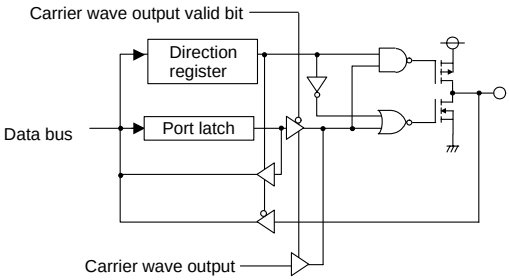


Fig. 15 Block diagram of ports (1)

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Termination of Unused Pins

1. Termination of common pins

I/O ports: Select an input port or an output port and follow each processing method.

Output ports: Open.

Input ports: If the input level become unstable, through current flow to an input circuit, and the power supply current may increase.
Especially, when expecting low consumption current (at STP or WIT instruction execution etc.), pull-up or pull-down input ports to prevent through current (built-in resistor can be used).
We recommend processing unused pins through a resistor which can secure I_{OH}(avg) or I_{OL}(avg).

Table 8 Termination of unused pins

Pin	Termination 1 (recommend)	Termination 2 (recommend)
$P0_0$/KEY_0–$P0_7$/KEY_7	I/O port	When selecting key-on wakeup function, perform termination of input port.
$P1_0$–$P1_1$(RLSS-only pin)		When selecting N-channel open-drain for output structure, open.
$P2_0$ (LED_0)/INT_0		When selecting N-channel open-drain for output structure, connect to V_{SS} through a resistor. Or set its port latch to “0” and open.
$P2_1$ (LED_1)/INT_1		When selecting N-channel open-drain for output structure, connect to V_{SS} through a resistor. Or set its port latch to “0” and open.
$P2_2$ (LED_2)–$P2_7$ (LED_7)		When selecting N-channel open-drain for output structure, open.
$P3_0$–$P3_7$		When selecting N-channel open-drain for output structure, open.
$P4_0$ (LED_8) (RLSS-only pin)		–
$P4_1$ (LED_9) (RLSS-only pin)		–
$P4_2$/CARR		When selecting CARR output function, perform termination of output port.
V_{DDR}	Connect to V_{SS}.	–

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Interrupts

The 7545 group interrupts are vector interrupts with a fixed priority scheme, and generated by 7 sources 3 external, 3 internal, and 1 software.
The interrupt sources, vector addresses(1), and interrupt priority are shown in Table 9.

Each interrupt except the BRK instruction interrupt has the interrupt request bit and the interrupt enable bit. These bits and the interrupt disable flag (I flag) control the acceptance of interrupt requests. Figure 16 shows an interrupt control diagram.

An interrupt requests is accepted when all of the following conditions are satisfied:

- Interrupt disable flag ..... "0"
- Interrupt request bit ..... "1"
- Interrupt enable bit ..... "1"

Though the interrupt priority is determined by hardware, priority processing can be performed by software using the above bits and flag.

Table 9 Interrupt vector address and priority

Interrupt source	Priority	Vector addresses(1)		Interrupt request generating conditions	Remarks
		High-order	Low-order		
Reset (2)	1	$FFFD_{16}$	$FFFC_{16}$	At reset input	Non-maskable
Key-on wakeup	2	$FFFB_{16}$	$FFFA_{16}$	AND operation of input logic level of port P0 (input)	External interrupt
INT_0	3	$FFF9_{16}$	$FFF8_{16}$	At detection of either rising or falling edge of INT_0 input	External interrupt (active edge selectable)
INT_1	4	$FFF7_{16}$	$FFF6_{16}$	At detection of either rising or falling edge of INT_1 input	External interrupt (active edge selectable)
Timer 2	5	$FFF5_{16}$	$FFF4_{16}$	At timer 2 underflow	
Timer 3	6	$FFF3_{16}$	$FFF2_{16}$	At timer 3 underflow	
Timer 1	7	$FFF1_{16}$	$FFF0_{16}$	At timer 1 underflow	STP release timer underflow
BRK instruction	8	$FFDD_{16}$	$FFDC_{16}$	At BRK instruction execution	Non-maskable software interrupt

NOTES:
1. Vector addressed contain interrupt jump destination addresses.
2. Reset function in the same way as an interrupt with the highest priority.

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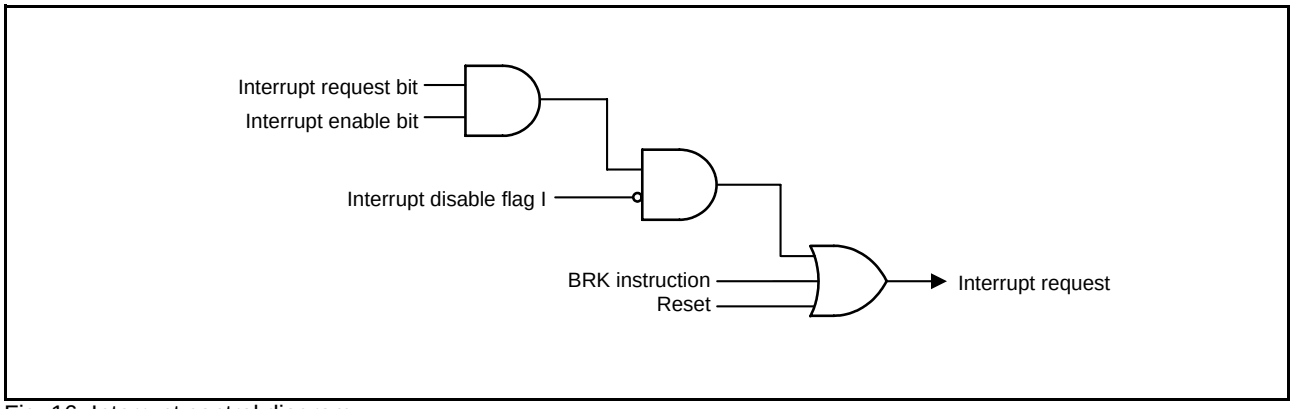


Fig. 16 Interrupt control diagram

• Interrupt Disable Flag

The interrupt disable flag is assigned to bit 2 of the processor status register. This flag controls the acceptance of all interrupt requests except for the BRK instruction. When this flag is set to "1", the acceptance of interrupt requests is disabled. When it is set to "0", acceptance of interrupt requests is enabled. This flag is set to "1" with the SET instruction and set to "0" with the CLI instruction.

When an interrupt request is accepted, the contents of the processor status register are pushed onto the stack while the interrupt disable flag remains set to "0". Subsequently, this flag is automatically set to "1" and multiple interrupts are disabled. To use multiple interrupts, set this flag to "0" with the CLI instruction within the interrupt processing routine.

The contents of the processor status register are popped off the stack with the RTI instruction.

• Interrupt Request Bits

Once an interrupt request is generated, the corresponding interrupt request bit is set to "1" and remains "1" until the request is accepted. When the request is accepted, this bit is automatically set to "0".

Each interrupt request bit can be set to "0", but cannot be set to "1", by software.

• Interrupt Enable Bits

The interrupt enable bits control the acceptance of the corresponding interrupt requests. When an interrupt enable bit is set to "0", the acceptance of the corresponding interrupt request is disabled. If an interrupt request occurs in this condition, the corresponding interrupt request bit is set to "1", but the interrupt request is not accepted. When an interrupt enable bit is set to "1", acceptance of the corresponding interrupt request is enabled. Each interrupt enable bit can be set to "0" or "1" by software.

The interrupt enable bit for an unused interrupt should be set to "0".

• Interrupt Edge Selection

The valid edge of external interrupt INT_0 and INT_1 can be selected by the interrupt edge selection register(address $003A_{16}$), respectively.

• Key-on Wakeup Pin Selection

By setting the key-on wakeup pin selection register (address 0018_{16}), the valid or invalid of key-on wakeup for each pin can be selected.

• Key-on Wakeup Edge Selection

By setting the key-on wakeup edge selection register (address 0019_{16}), the trigger edge of key-on wakeup for each pin can be selected.

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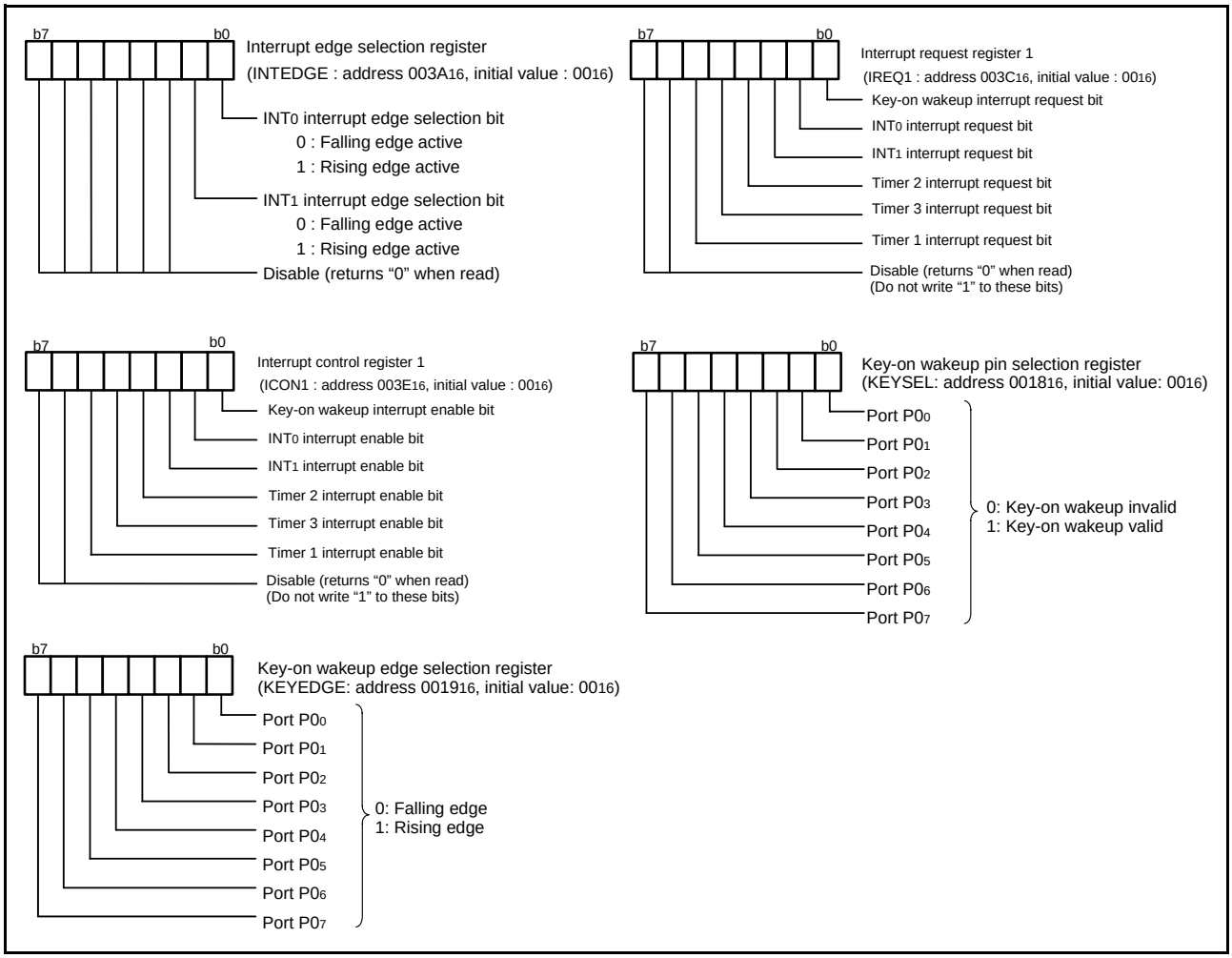


Fig. 17 Structure of interrupt-related registers

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• Interrupt Request Generation, Acceptance, and Handling

Interrupts have the following three phases.

(i) Interrupt Request Generation
An interrupt request is generated by an interrupt source (external interrupt signal input, timer underflow, etc.) and the corresponding request bit is set to "1".

(ii) Interrupt Request Acceptance
Based on the interrupt acceptance timing in each instruction cycle, the interrupt control circuit determines acceptance conditions (interrupt request bit, interrupt enable bit, and interrupt disable flag) and interrupt priority levels for accepting interrupt requests. When two or more interrupt requests are generated simultaneously, the highest priority interrupt is accepted. The value of interrupt request bit for an unaccepted interrupt remains the same and acceptance is determined at the next interrupt acceptance timing point.

(iii) Handling of Accepted Interrupt Request
The accepted interrupt request is processed.

Figure 18 shows the time up to execution in the interrupt processing routine, and Figure 19 shows the interrupt sequence. Figure 20 shows the timing of interrupt request generation, interrupt request bit, and interrupt request acceptance.

• Interrupt Handling Execution

When interrupt handling is executed, the following operations are performed automatically.

(1) Once the currently executing instruction is completed, an interrupt request is accepted.

(2) The contents of the program counters and the processor status register at this point are pushed onto the stack area in order from 1 to 3.
1. High-order bits of program counter (PC_H)
2. Low-order bits of program counter (PC_L)
3. Processor status register (PS)

(3) Concurrently with the push operation, the jump address of the corresponding interrupt (the start address of the interrupt processing routine) is transferred from the interrupt vector to the program counter.

(4) The interrupt request bit for the corresponding interrupt is set to "0". Also, the interrupt disable flag is set to "1" and multiple interrupts are disabled.

(5) The interrupt routine is executed.

(6) When the RTI instruction is executed, the contents of the registers pushed onto the stack area are popped off in the order from 3 to 1. Then, the routine that was before running interrupt processing resumes.

As described above, it is necessary to set the stack pointer and the jump address in the vector area corresponding to each interrupt to execute the interrupt processing routine.

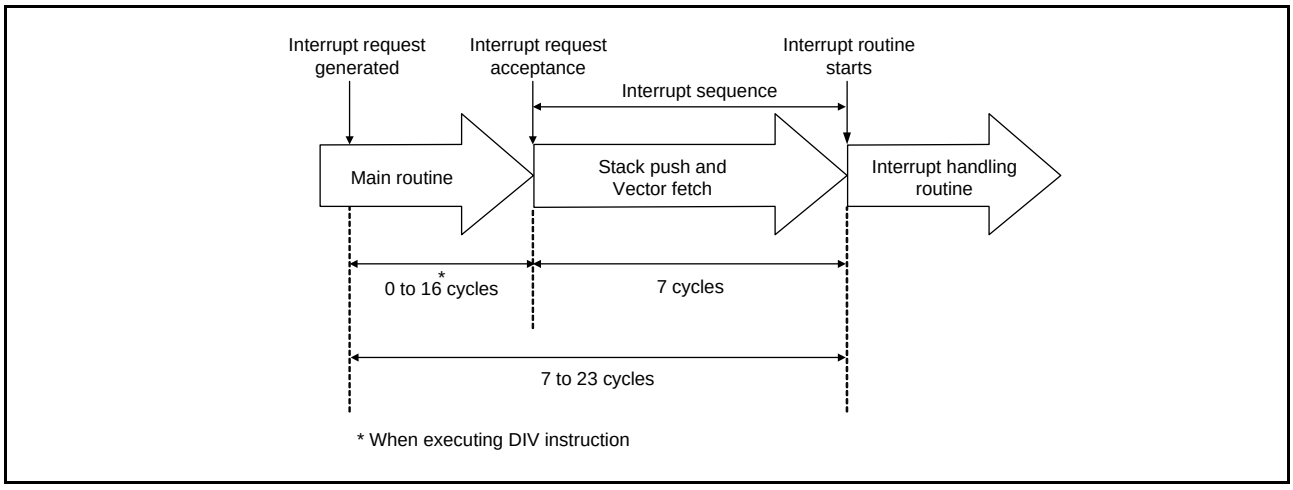
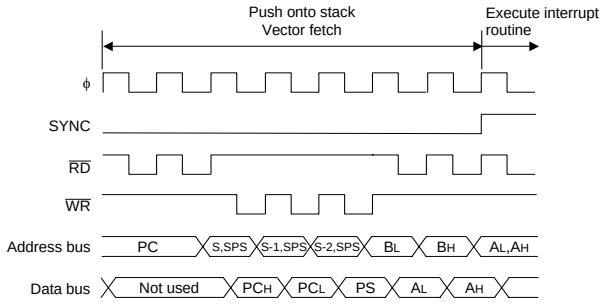


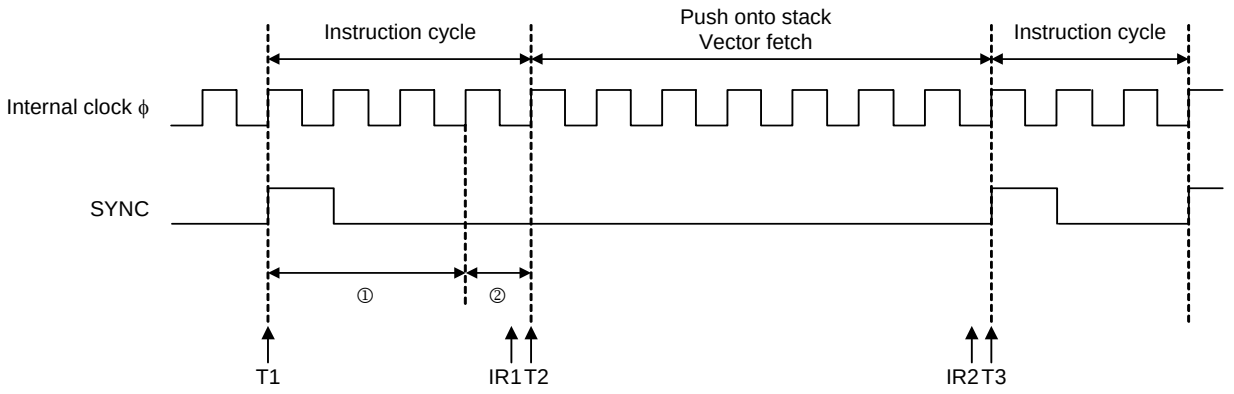
Fig. 18 Time up to execution in interrupt routine

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SYNC : CPU operation code fetch cycle
(This is an internal signal that cannot be observed from the external unit.)
BL, BH: Vector address of each interrupt
AL, AH: Jump destination address of each interrupt
SPS : "00_{16}" or "01_{16}"
([SPS] is a page selected by the stack page selection bit of CPU mode register.)

Fig. 19 Interrupt sequence



T1 T2 T3 : Interrupt acceptance timing points
IR1 IR2 : Timings points at which the interrupt request bit is set to "1".

Note : Period 2 indicates the last ϕ cycle during one instruction cycle.

(1) The interrupt request bit for an interrupt request generated during period 1 is set to "1" at timing point IR1.
(2) The interrupt request bit for an interrupt request generated during period 2 is set to "1" at timing point IR1 or IR2. The timing point at which the bit is set to "1" varies depending on conditions. When two or more interrupt requests are generated during the period 2, each request bit may be set to "1" at timing point IR1 or IR2 separately.

Fig. 20 Timing of interrupt request generation, interrupt request bit, and interrupt acceptance

<Notes>

When setting the followings, the interrupt request bit may be set to "1" .

<When setting the external interrupt active edge>

- INT_0 interrupt edge selection bit (bit 0 of Interrupt edge selection register (address $3A_{16}$))
- INT_1 interrupt edge selection bit (bit 1 of Interrupt edge selection register)
- Key-on wakeup edge selection register (address 19_{16})

If it is not necessary to generate an interrupt synchronized with these settings, take the following sequence.

(1) Set the corresponding enable bit to "0" (disabled).
(2) Set the interrupt edge selection bit (the active edge switch bit) or the interrupt source bit.
(3) Set the corresponding interrupt request bit to "0" after one or more instructions have been executed.
(4) Set the corresponding interrupt enable bit to "1" (enabled).

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Key Input Interrupt (Key-on Wake-Up)

A key-on wake-up interrupt request is generated by applying the level set by KEYEDGE to any pin of port P0 that has been set to input mode and KEYSEL has been valid. In other words, it is generated when the AND of input level goes from “1” to “0” or from “0” to “1”.

An example of using a key input interrupt is shown in Figure 21, where an interrupt request is generated by pressing one of the keys provided as an active-low key matrix which uses ports P0$_0$ to P0$_3$ as input ports.

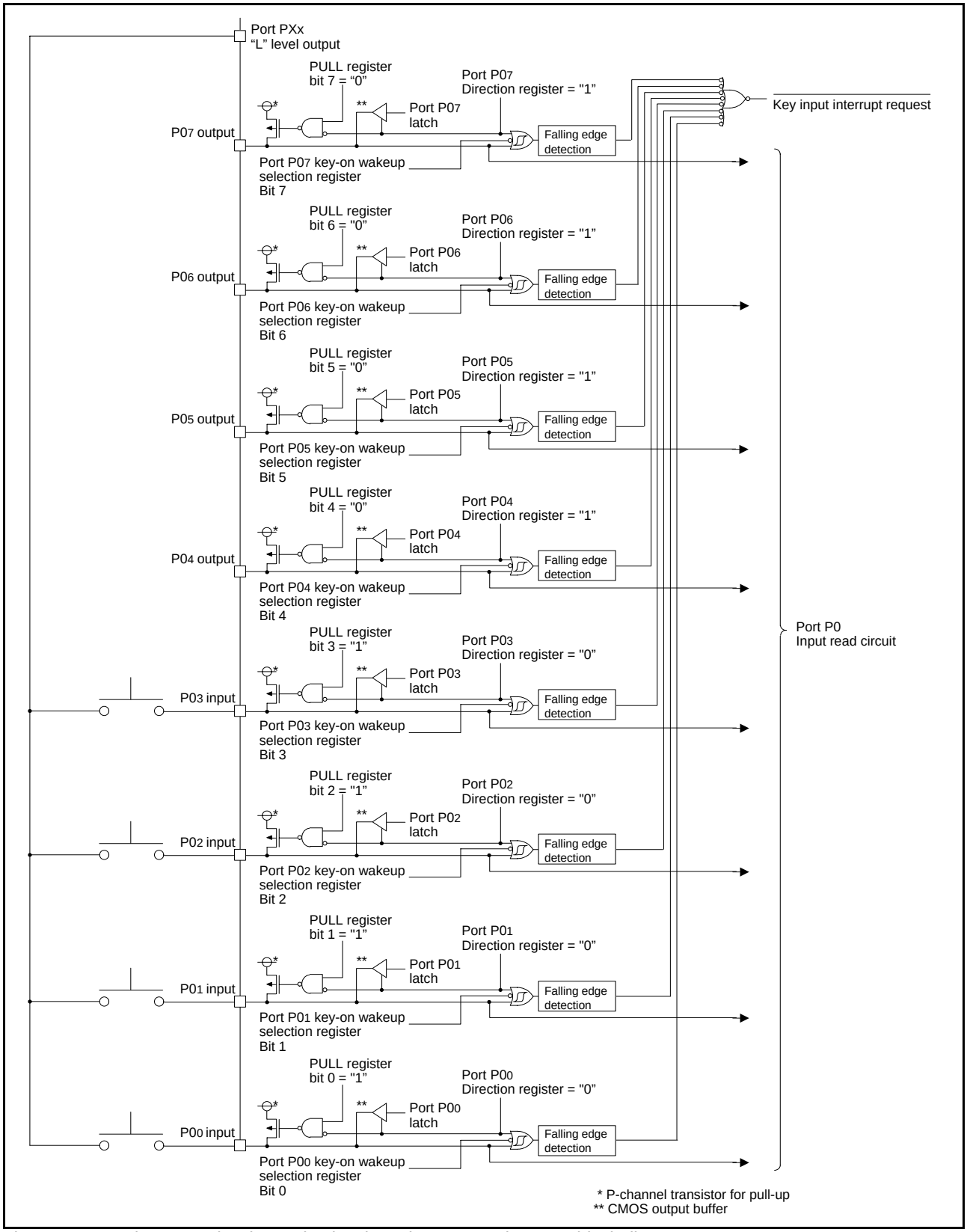


Fig. 21 Connection example when using key input interrupt and port P0 block diagram

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Timers

The 7545 Group has 3 timers: timer 1, timer 2 and timer 3.
The division ratio of every timer and prescaler is 1/(n+1) provided that the value of the timer latch or prescaler is n.
All the timers are down count timers. When a timer reaches "0", an underflow occurs at the next count pulse, and the corresponding timer latch is reloaded into the timer. When a timer underflows, the interrupt request bit corresponding to each timer is set to "1".

1. Timer 1

Timer 1 is an 8-bit timer and counts the prescaler 1 output.
When Timer 1 underflows, the timer 1 interrupt request bit is set to "1".
Prescaler 1 is an 8-bit prescaler and counts the clock which is f(XIN) divided by 16.
Prescaler 1 and Timer 1 have the prescaler 1 latch and the timer 1 latch to retain the reload value, respectively. The value of prescaler 1 latch is set to Prescaler 1 when Prescaler 1 underflows. The value of timer 1 latch is set to Timer 1 when Timer 1 underflows.
When writing to Prescaler 1 (PRE1) is executed, the value is written to both the prescaler 1 latch and Prescaler 1.
When writing to Timer 1 (T1) is executed, the value is written to both the timer 1 latch and Timer 1.
When reading from Prescaler 1 (PRE1) and Timer 1 (T1) is executed, each count value is read out.

Timer 1 always operates in the timer mode.
Prescaler 1 counts the clock which is f(XIN) divided by 16. Each time the count clock is input, the contents of Prescaler 1 is decremented by 1. When the contents of Prescaler 1 reach "00_{16}", an underflow occurs at the next count clock, and the prescaler 1 latch is reloaded into Prescaler 1 and count continues. The division ratio of Prescaler 1 is 1/(n+1) provided that the value of Prescaler 1 is n.
Timer 1 counts the underflow signal of Prescaler 1. The contents of Timer 1 is decremented by 1 each time the count clock is input.
When the contents of Timer 1 reach "00_{16}", an underflow occurs at the next count clock, and the timer 1 latch is reloaded into Timer 1 and count continues. The division ratio of Timer 1 is 1/(m+1) provided that the value of Timer 1 is m.
Timer 1 is stopped by setting "1" to the timer 1 count stop bit.

2. Timer 2

Timer 2 is an 8-bit timer and counts the clock selected by the timer 2 count source selection bit. When Timer 2 underflows, the timer 2 interrupt request bit is set to "1".
Timer 2 has two timer latches (primary latch and secondary latch) to retain the reload value.

The value written to timer 2 primary (T2P) while timer 2 is stopped is transferred to the timer 2 primary latch and the counter.
The value written to timer 2 secondary (T2S) while timer 2 is stopped is transferred only to timer 2 secondary latch.
After the count of timer 2 starts, the values written to timer 2 primary (T2P) and timer 2 secondary (T2S) are transferred only to each latch. The values are not transferred to the counter at write.
When each timer underflows, the values of timer 2 primary latch and the timer 2 secondary latch are alternately transferred to the counter. (Since a count value of a timer is retained, the written value becomes the count value of the timer after the next underflow.)
When timer 2 primary (T2P) is read, the count value of the timer is read. When timer 2 secondary (T2S) is read, a set value of timer 2 secondary is read. (Read the timer 2 primary to read the count value even during the count period of timer 2 secondary.)
When the timer 2 primary is read, the count value of timer 2 is read since the count value of the timer 2 is retained until writing to timer 2 primary (T2P) is performed after timer 2 is stopped.

Timer 2 always operates in the timer mode.
Timer 2 counts the clock selected by the timer 2 count source selection bit. The contents of Timer 2 is decremented by 1 each time the count clock is input. When the contents of Timer 2 reach "00_{16}", an underflow occurs at the next count clock, and the timer 2 primary latch or timer 2 secondary latch is alternately reloaded into Timer 2 and count continues.

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3. Timer 3

Timer 3 is an 8-bit timer and counts the clock selected by the timer 3 count source selection bit. When Timer 3 underflows, the timer 3 interrupt request bit is set to "1".
Timer 3 has a timer latch to retain the reload value.

The value written to timer 3 (T3) while timer 3 is stopped is transferred to the timer latch and the counter.
After the count of timer 3 (T3) starts, the value written to timer 3 is transferred only to the timer 3 latch. The value is not transferred to the counter at write.
When timer underflows, the value of timer 3 latch is transferred to the counter. (Since a count value of a timer is retained, the written value becomes the count value of the timer after the next underflow.)
When timer 3 (T3) is read, the count value of the timer is read.
When the timer 3 is read, the count value of timer 3 is read since the count value of the timer 3 is retained until writing to timer 3 (T3) is performed after timer 3 is stopped.

Timer 3 always operates in the timer mode.
Timer 3 counts the clock selected by the timer 3 count source selection bit. The contents of Timer 3 is decremented by 1 each time the count clock is input.
The division ratio of Timer 3 is 1/(n+1) provided that the value of Timer 3 is n.
Timer 3 is stopped by setting "1" to the timer 3 count stop bit.
Timer 2 and timer 3 are also used for the control timer of the carrier wave control circuit.

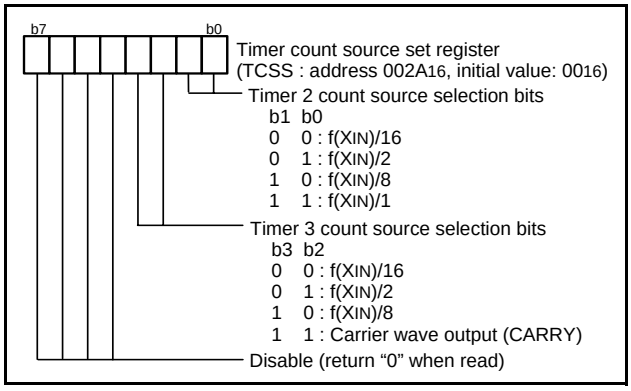


Fig. 22 Structure of timer count source set register

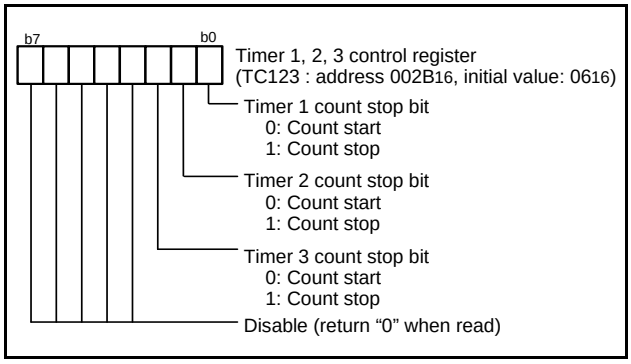


Fig. 23 Timer 1, 2, 3 control register

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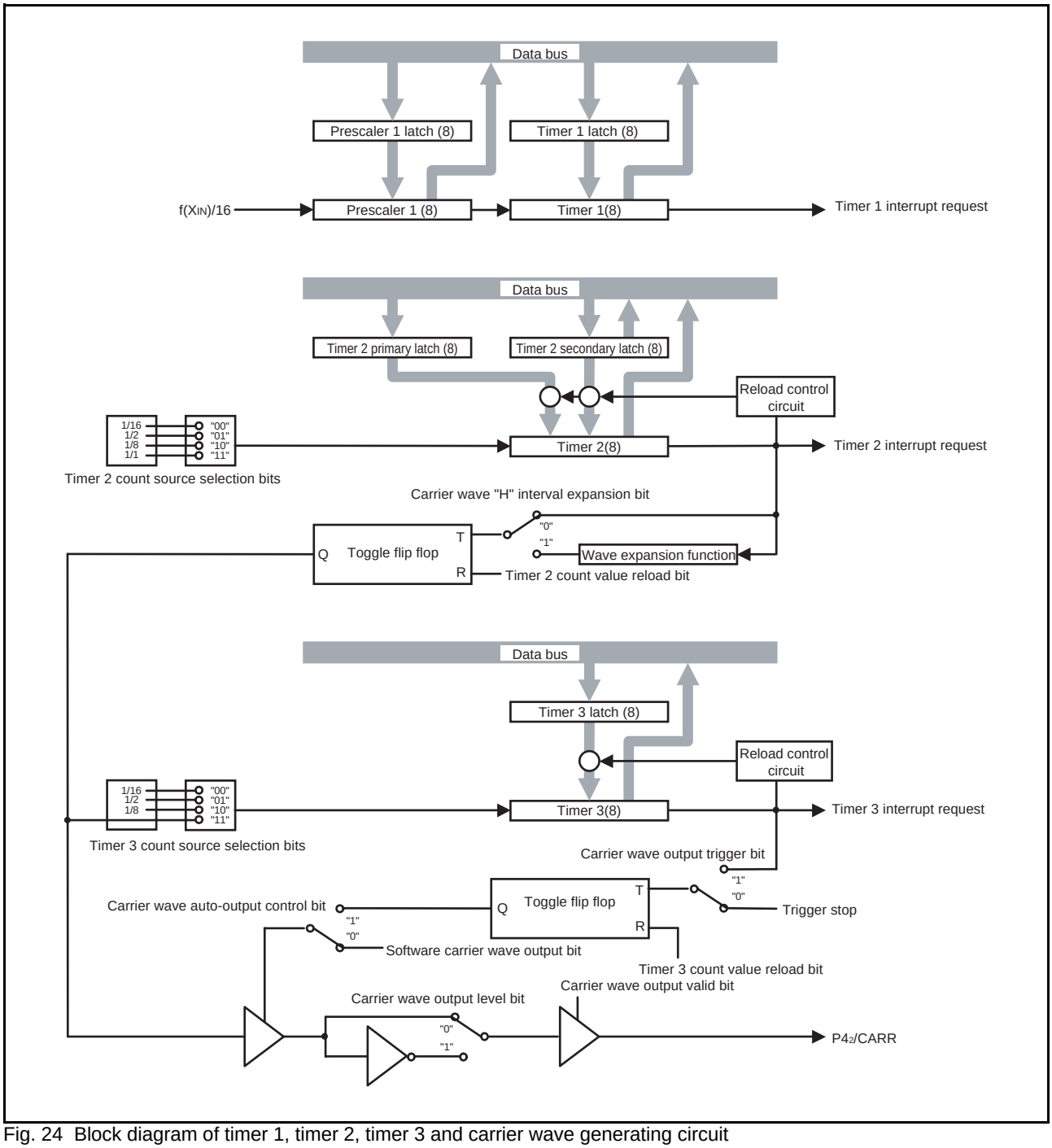


Fig. 24 Block diagram of timer 1, timer 2, timer 3 and carrier wave generating circuit

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4. Carrier wave generating circuit

The carrier wave generating circuit is used to generate the control wave of the remote control by using timer 2 and timer 3 (Figure 26).

In order to use the carrier wave generating function by timer 2, set "1" to the carrier wave output valid bit (bit 1 of the carrier wave control register (address 27_{16})).
Carrier wave "H" duration is set to the timer 2 primary, and carrier wave "L" duration is set to the timer 2 secondary. Timer 2 counts a primary latch and a secondary latch alternately, and controls carrier wave "H" duration and the "L" duration (Figure 27).
The "H" duration of the carrier waveform can be expanded for a half clock of timer 2 count source by setting "1" to the carrier wave "H" duration bit (bit 0) (Figure 28).
Therefore, the frequency of the carrier wave can be set by the resolution of 1/2 of the timer 2 count source.
For example, the carrier wave of the resolution of 125 ns (max.) can be generated at $f(X_{IN})$ = 4 MHz when $f(X_{IN})/1$ is selected for the timer 2 count source.
In order to initialize the carrier waveform, write in the timer 2 primary after stopping the count of timer 2, and then, start the count of timer 2. The output of the carrier waveform is started from a primary period.
Output/stop of the carrier waveform can be controlled by software or timer 3 (Figure 31 and Figure 32). The output of the carrier wave is started from the $P4_2$/CARR pin when "1" is set to the software carrier wave output bit (bit 2), and the output of the carrier wave is stopped when "0" is written.

The auto-output of the carrier wave using timer 3 can be performed by setting "1" to the carrier wave auto-output control bit (bit 3) (Figure 29). Each time timer 3 underflow occurs, the trigger signal which is used to turn the output of the carrier wave on/off is generated.
The trigger from timer 3 becomes valid by setting "1" to the carrier wave output trigger bit (bit 4), and the output/stop of the carrier wave from the $P4_2$/CARR pin is repeated each time timer 3 underflows. Timer 3 count continues without stopping though the output/stop state of the carrier wave at that time is maintained when "0" is written to the carrier wave auto-output control bit (bit 3) while the output of the carrier wave by timer 3 is controlled.
In order to initialize output/stop control of the carrier waveform, write in the timer 3 after stopping the count of timer 3, and then, start the count of timer 3. The output of the carrier waveform is started from "waveform output valid period".

5. 455 kHz carrier wave generating mode

The 455 kHz carrier wave generating mode is used to generate artificially the 455 kHz carrier wave by auto-control of the setting value of the timer, or the waveform expansion mode.
If "1" (valid) is set to the 455 kHz carrier wave generating mode bit (bit 5), the values of the timer latch and the carrier wave "H" duration expansion bit (bit 0) are automatically set.
Then, the nine waveforms of 2.250 µs wavelength and the seven waveforms of 2.125 µs wavelength are generated periodically as shown in Figure 30.
The carrier wave of 455.516 kHz can be pseudo generated since the average wavelength for one period becomes 2.195 µs.
In order to use 455 kHz carrier wave generating mode, use the 4 MHz oscillator and select $f(X_{IN})/1$ for the timer 2 count source.

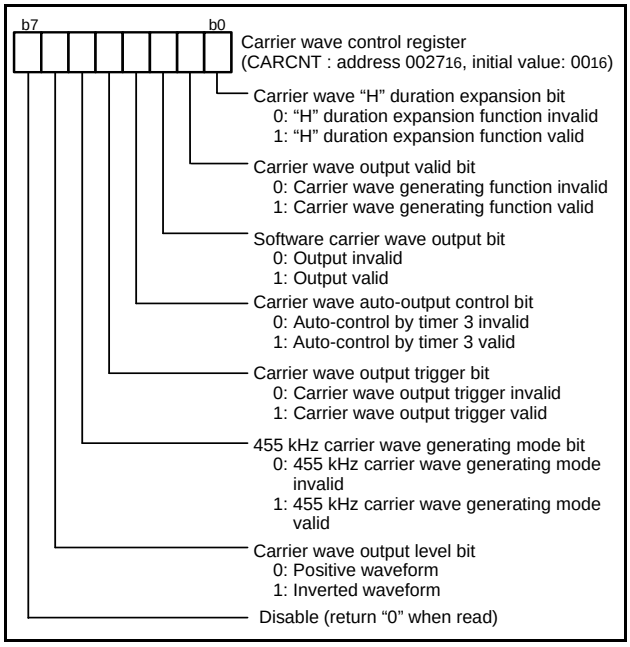


Fig. 25 Carrier wave control register

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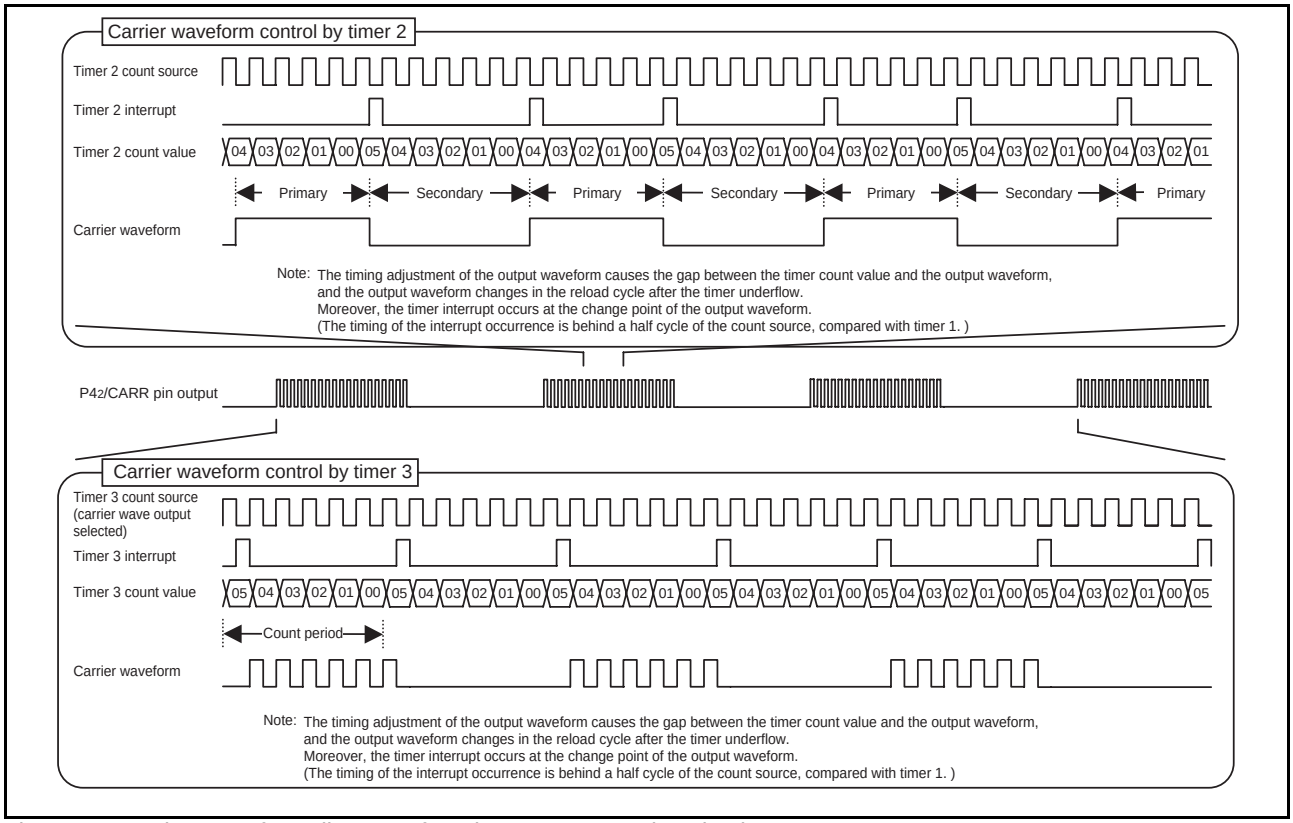


Fig. 26 Operating waveform diagram of carrier wave generating circuit

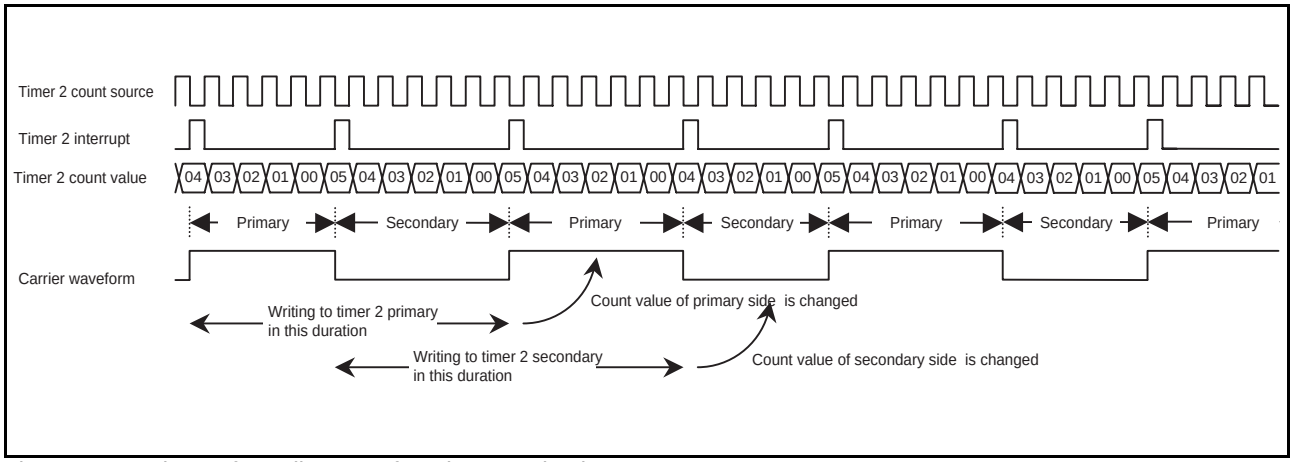


Fig. 27 Control waveform diagram of carrier wave by timer 2

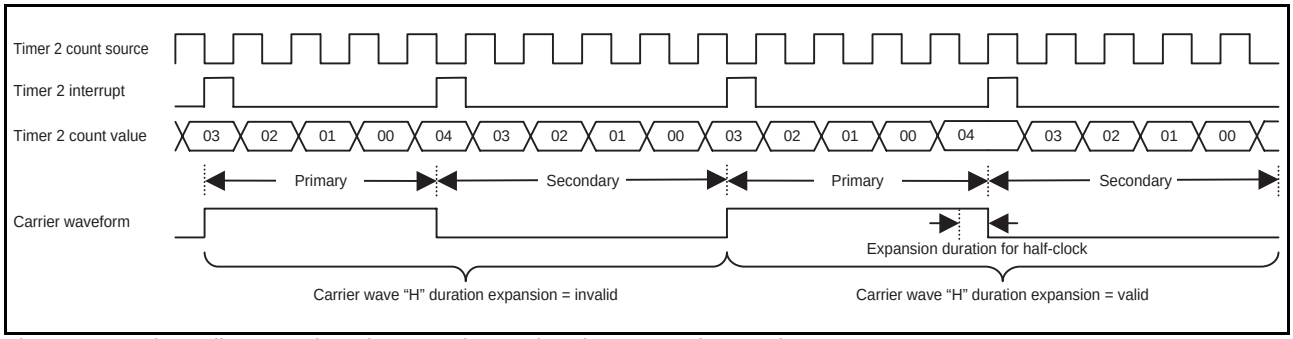


Fig. 28 Waveform diagram of carrier wave in “H” duration expansion mode

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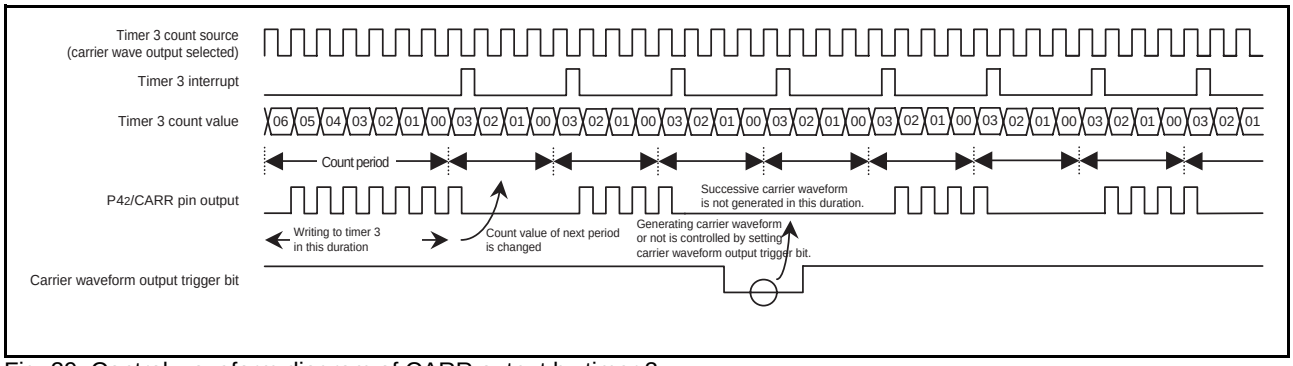


Fig. 29 Control waveform diagram of CARR output by timer 3

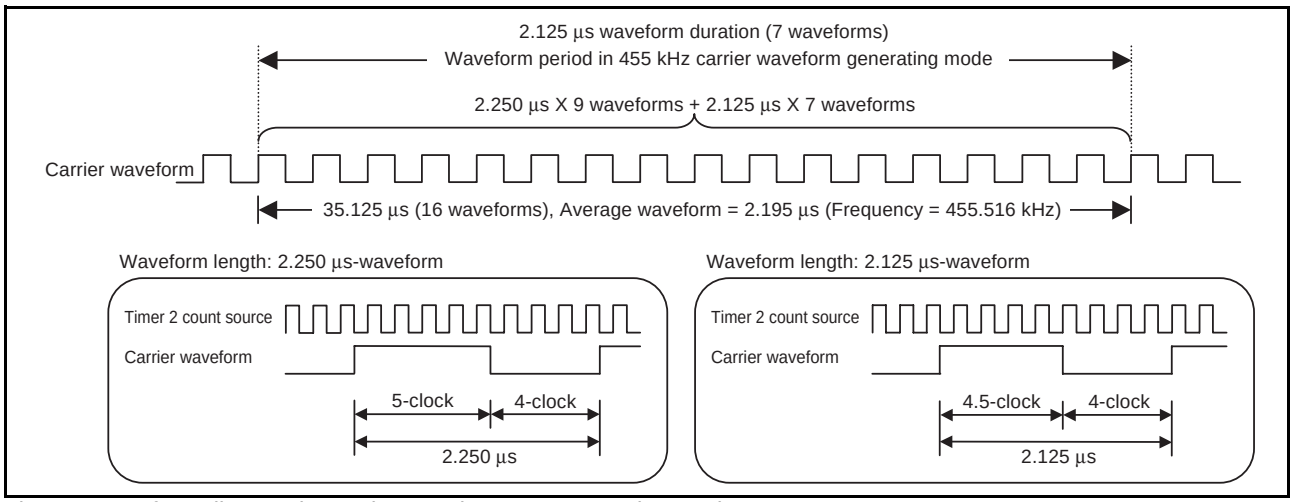


Fig. 30 Waveform diagram in 455 kHz carrier wave generating mode

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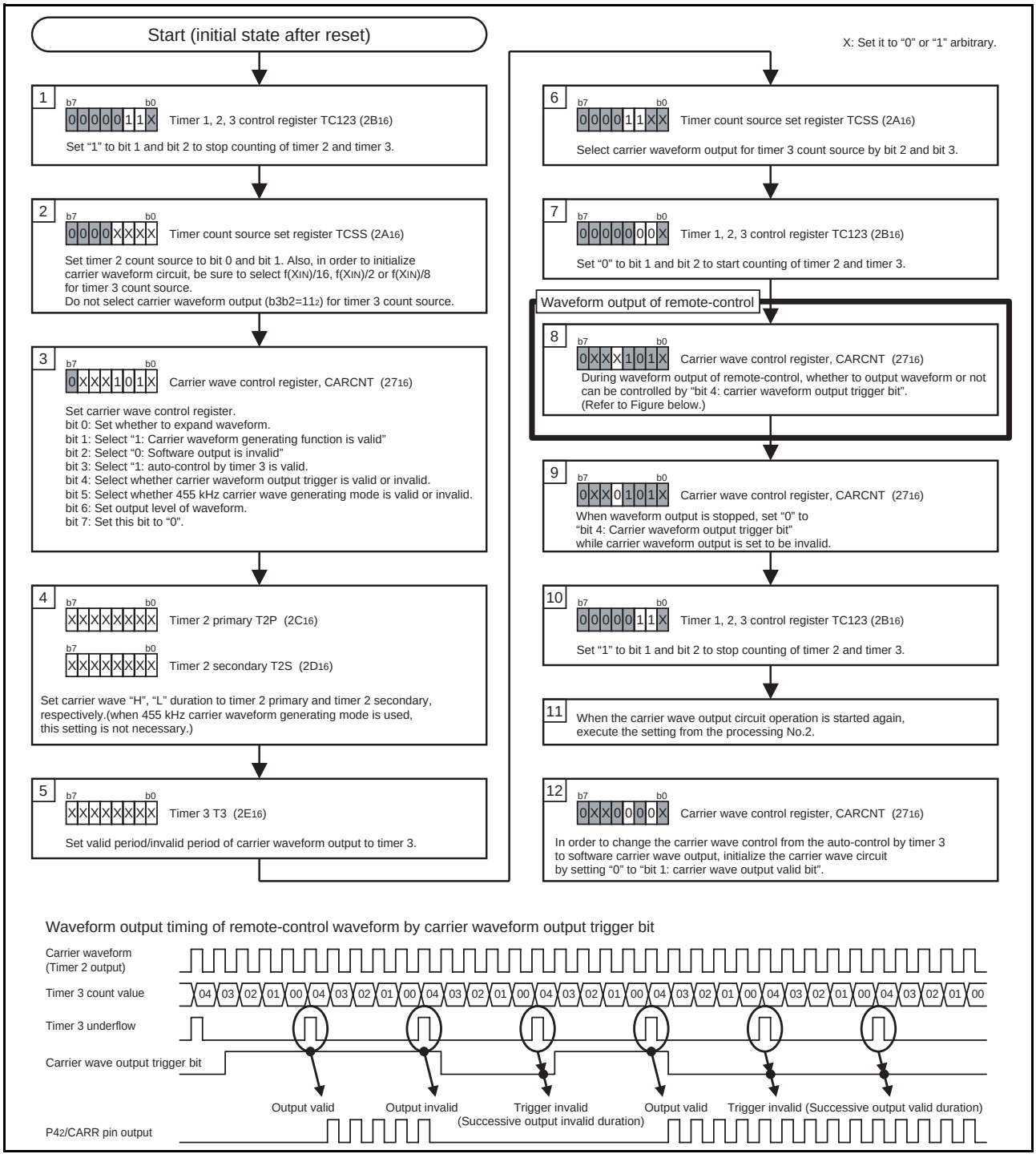


Fig. 31 Setting of carrier wave auto-control by timer 3

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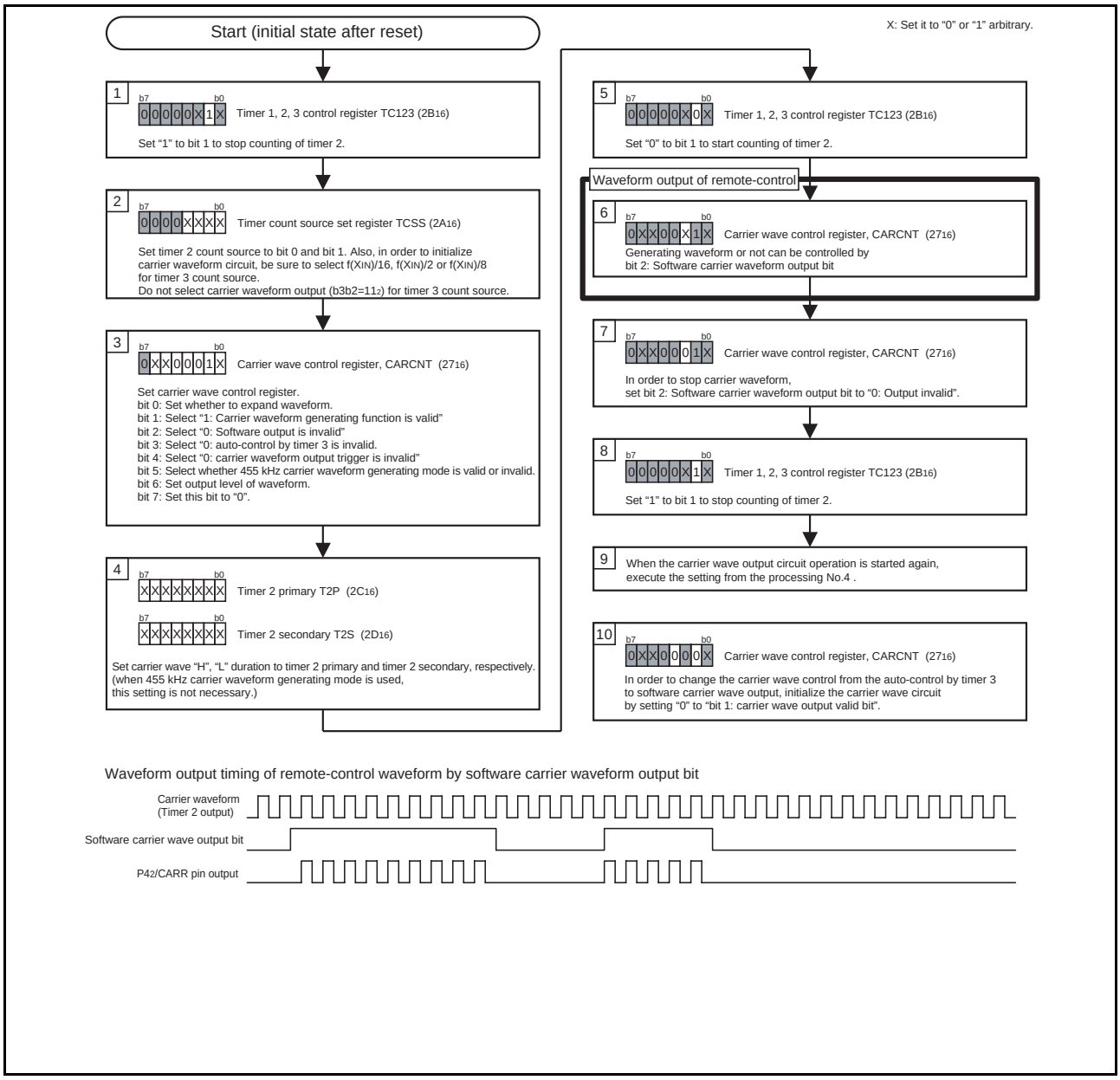


Fig. 32 Setting of carrier wave control by software

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Watchdog Timer

The watchdog timer gives a means for returning to a reset status when the program fails to run on its normal loop due to a runaway.
The watchdog timer consists of an 8-bit watchdog timer H and an 8-bit watchdog timer L, being a 16-bit counter.

1. Standard operation of watchdog timer

The watchdog timer is valid by setting "0" to bit 0 of the Function set ROM data (address FFDA16) of the built-in QzROM.
When an internal clock is supplied after waiting the oscillation stabilizing time by timer 1 after system is released from reset, the watchdog timer starts operation. When the watchdog timer H underflows, an internal reset occurs. Accordingly, it is programmed that the watchdog timer control register (address 003916) can be set before an underflow occurs.
When the watchdog timer control register (address 003916) is read, the values of the high-order 6-bit of the watchdog timer H and watchdog timer H count source selection bit are read.

2. Initial value of watchdog timer

By a reset or writing to the watchdog timer control register (address 003916), the watchdog timer H is set to "FF16" and the watchdog timer L is set to "FF16".

3. Operation of watchdog timer H count source selection bit

A watchdog timer H count source can be selected by bit 7 of the watchdog timer control register (address 003916). When this bit is "0", the count source becomes a watchdog timer L underflow signal. The detection time is 262.144 ms at f(XIN) = 4 MHz.
When this bit is "1", the count source becomes f(XIN)/16. In this case, the detection time is 1024 μs at f(XIN) = 4 MHz.
This bit is cleared to "0" after reset.

4. STP instruction function selection bit

The function of the STP instruction can be selected by the bit 1 in FSROM. This bit cannot be used for rewriting by executing the STP instruction.

- When this bit is set to "0", internal reset occurs by executing the STP instruction.
- When this bit is set to "1", stop mode is entered by executing the STP instruction.

<Notes on Watchdog Timer>

1. The watchdog timer is operating during the wait mode. Write data to the watchdog timer control register to prevent timer underflow.
2. The watchdog timer stops during the stop mode. However, the watchdog timer is running during the oscillation stabilizing time after the STP instruction is released. In order to avoid the underflow of the watchdog timer, the watchdog timer H count source selection bit (bit 7 of watchdog timer control register (address 003916)) must be set to "0" just before executing the STP instruction.

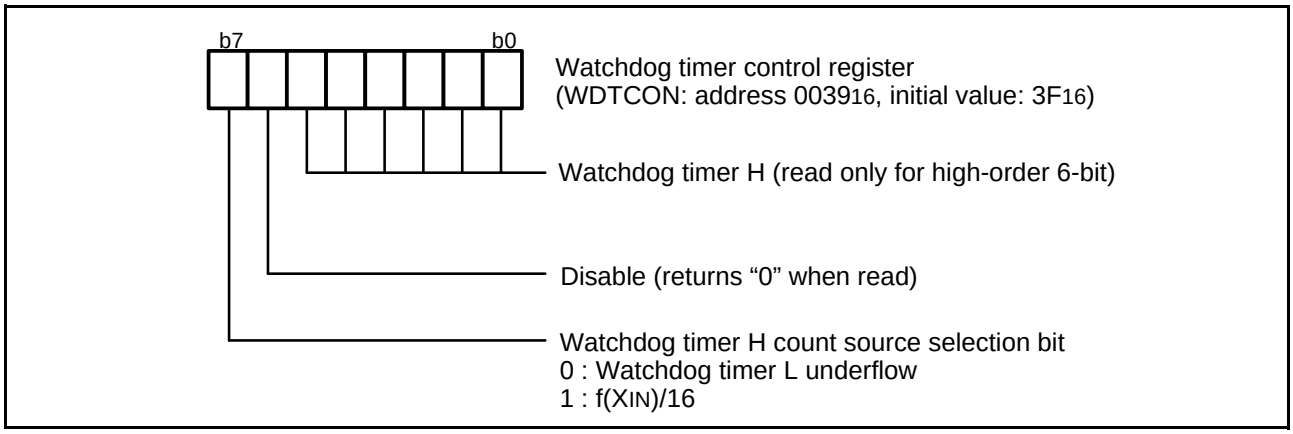


Fig. 33 Structure of watchdog timer control register

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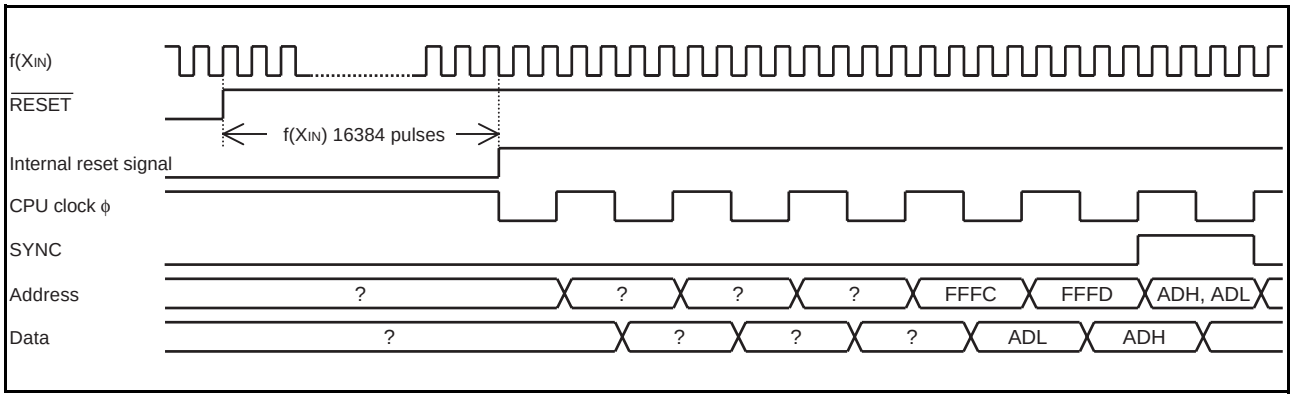


Fig. 34 Timing diagram at reset

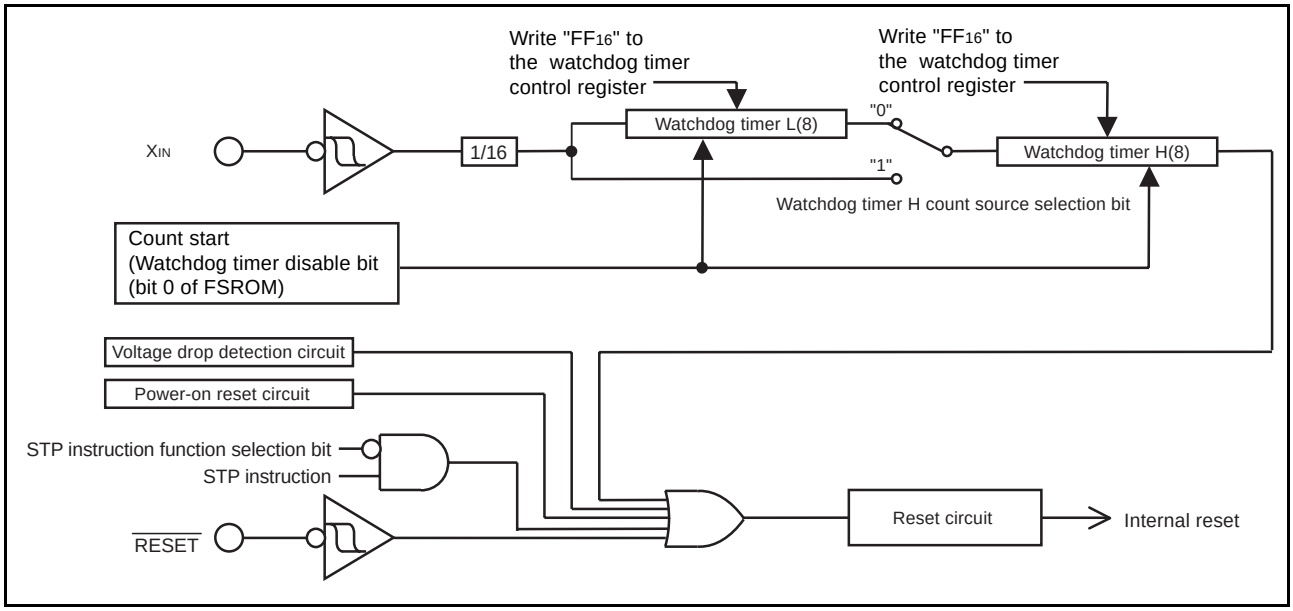


Fig. 35 Block diagram of watchdog timer and reset circuit

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Power-on Reset Circuit

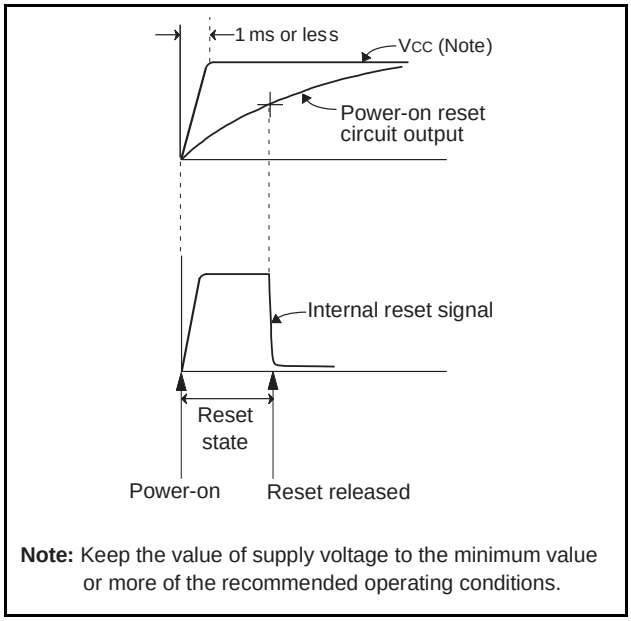
Reset can be automatically performed at power on (power-on reset) by the built-in power-on reset circuit.
In order to use the power-on reset circuit effectively, the time for the supply voltage to rise from 0 V to 1.8 V must be set to 1 ms or less.

Voltage Drop Detection Circuit

The built-in voltage drop detection circuit is designed to detect a drop in voltage and to reset the microcomputer if the supply voltage drops below a set value (Typ.1.75 V). When the STP instruction is executed, the voltage drop detection circuit is stopped, so that the power dissipation is reduced.
The operation of the voltage drop detection circuit is disabled by setting "0" to bit 4 of the Function set ROM data (address FFDA16) of the built-in QzROM.
Note: The emulator MCU "M37545RLSS" is not equipped with the voltage drop detection circuit.

RESETOUT Output

RESETOUT function is used to output "L" level from $\overline{\text{RESET}}$ pin when system reset occurs by the power-on reset, the voltage drop detection circuit or the watchdog timer. Also, the built-in pull-up transistor is connected to the $\overline{\text{RESET}}$ pin.



Note: Keep the value of supply voltage to the minimum value or more of the recommended operating conditions.

Fig. 36 Operation waveform diagram of power-on reset circuit

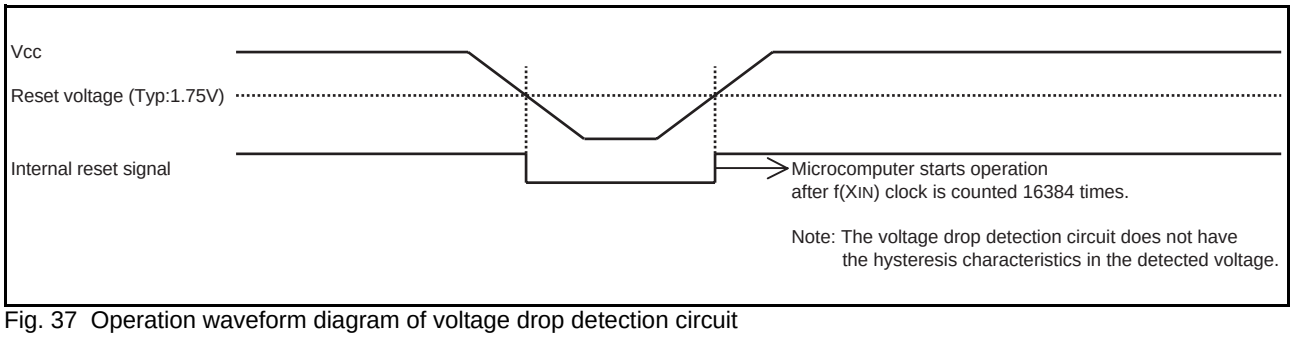


Fig. 37 Operation waveform diagram of voltage drop detection circuit

<Note on Voltage Drop Detection Circuit>

The voltage drop detection circuit detection voltage of this product is set up lower than the minimum value of the supply voltage of the recommended operating conditions.
When the supply voltage of a microcomputer falls below to the minimum value of recommended operating conditions and regoes up (ex. battery exchange of an application product), depending on the capacity value of the bypass capacitor added to the power supply pin, the following case may cause program failure;
supply voltage does not fall below to VDET, and its voltage re-goes up with no reset.
In such a case, please design a system which supply voltage is once reduced below to VDET and re-goes up after that.

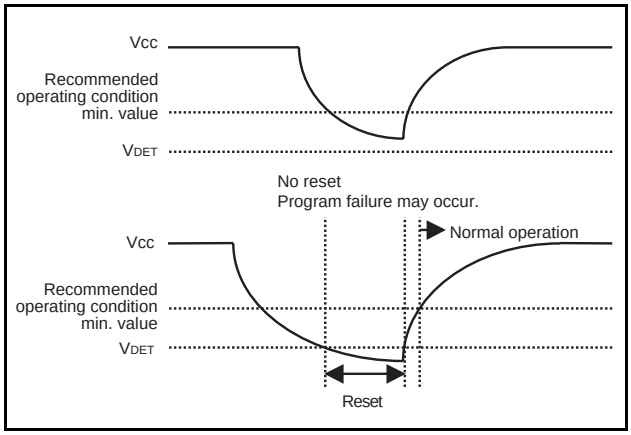


Fig. 38 VCC and VDET

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MISRG

The 7545 Group has two power source supply pins. One is the V_{CC} pin, and the other is the V_{DDR} pin only for RAM2. A potential difference between V_{CC} and V_{DDR} may cause some failures in reading from RAM2 or writing to RAM2. Accordingly, if there is a potential difference between V_{CC} and V_{DDR} at power-on, confirm the bit 1 (RAM2 status flag) of MISRG (address 0038_{16}) before reading from RAM2 or writing to RAM2.

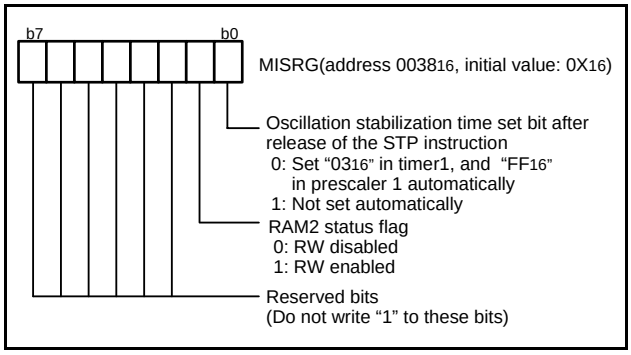


Fig. 39 Structure of MISRG

(1) Port P0 direction register (P0D)
(2) Port P1 direction register (P1D)
(3) Port P2 direction register (P2D)
(4) Port P3 direction register (P3D)
(5) Port P4 direction register (P4D)
(6) Pull-up control register (PULL)
(7) Port output mode switch register (PMOD)
(8) Key-on wakeup pin selection register (KEYSEL)
(9) Key-on wakeup edge selection register (KEYEDGE)
(10) Carrier wave control register (CARCNT)
(11) Prescaler 1 (PRE1)
(12) Timer 1 (T1)
(13) Timer count source set register (TCSS)
(14) Timer 1, 2, 3 control register (TC123)
(15) Timer 2 primary (T2P)
(16) Timer 2 secondary (T2S)
17) Timer 3 (T3)
(18) MISRG
(19) Watchdog timer control register (WDTCON)
(20) Interrupt edge selection register (INTEDGE)
(21) CPU mode register (CPUM)
(22) Interrupt request register 1 (IREQ1)
(23) Interrupt control register 1 (ICON1)
(24) Processor status register
(25) Program counter

Address	Register contents
0001_{16}	00_{16}
0003_{16}	X X X X X X 0 0
0005_{16}	00_{16}
0007_{16}	00_{16}
0009_{16}	X X X X X 0 0 0
0016_{16}	00_{16}
0017_{16}	00_{16}
0018_{16}	00_{16}
0019_{16}	00_{16}
0027_{16}	00_{16}
0028_{16}	FF_{16}
0029_{16}	03_{16}
$002A_{16}$	00_{16}
$002B_{16}$	06_{16}
$002C_{16}$	FF_{16}
$002D_{16}$	FF_{16}
$002E_{16}$	FF_{16}
0038_{16}	0 0 0 0 0 0 X 0
0039_{16}	0 0 1 1 1 1 1 1
$003A_{16}$	0 0 0 0 0 0 0 0
$003B_{16}$	1 0 0 0 0 0 0 0
$003C_{16}$	00_{16}
$003E_{16}$	00_{16}
(PS)	X X X X X 1 X X
(PCH)	Contents of address $FFFD_{16}$
(PCL)	Contents of address $FFFC_{16}$

X : Undefined

The content of other registers and RAM are undefined when the microcomputer is reset.
The initial values must be surely set before you use it.

Fig. 40 Internal status of microcomputer at reset

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CLOCK GENERATING CIRCUIT

An oscillation circuit can be formed by connecting a resonator between XIN and XOUT.
Use the circuit constants in accordance with the resonator manufacturer's recommended values.
No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip. (An external feed-back resistor may be needed depending on conditions.)

<Ceramic resonator/quartz-crystal oscillator>
When the ceramic resonator/quartz-crystal oscillator is used for the main clock, connect the ceramic resonator/quartz-crystal oscillator and the external circuit to pins XIN and XOUT at the shortest distance. A feedback resistor is built in between pins XIN and XOUT. (An external feed-back resistor may be needed depending on conditions.)

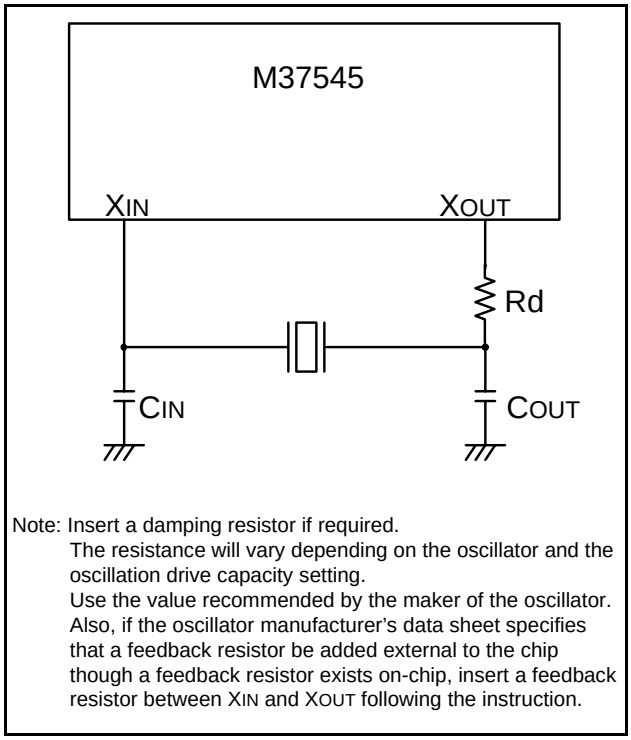
Oscillation Control

1. Stop mode

When the STP instruction is executed, the internal clock ϕ stops at an "H" level and the XIN oscillator stops. At this time, timer 1 is set to "03$_{16}$" and prescaler 1 is set to "FF$_{16}$"when the oscillation stabilization time set bit after release of the STP instruction is "0". On the other hand, timer 1 and prescaler 1 are not set when the above bit is "1". Accordingly, set the wait time fit for the oscillation stabilization time of the oscillator to be used. When an external interrupt is accepted, oscillation is restarted but the internal clock ϕ remains at "H" until timer 1 underflows. As soon as timer 1 underflows, the internal clock ϕ is supplied. This is because when a ceramic resonator is used, some time is required until a start of oscillation.
In the stop mode, the voltage drop detection circuit is stopped, so that the power dissipation is reduced.

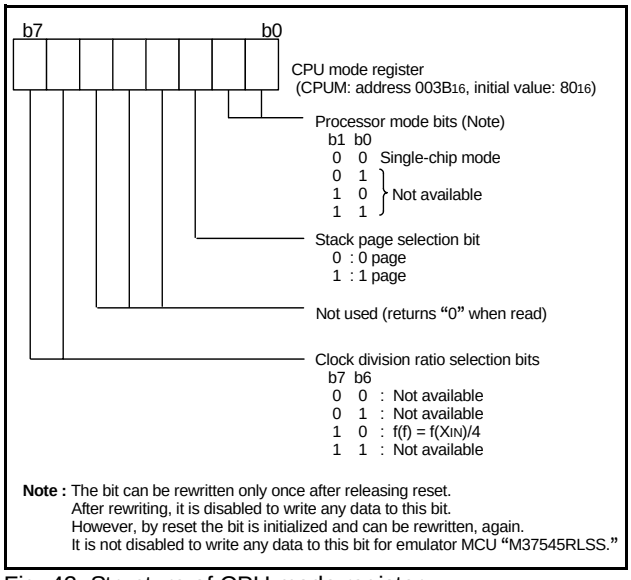
2. Wait mode

If the WIT instruction is executed, the internal clock ϕ stops at an "H" level, but the oscillator does not stop. The internal clock restarts if a reset occurs or when an interrupt is accepted. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted. To ensure that an interrupt will be accepted to release the STP or WIT state, the corresponding interrupt enable bit must be set to "1" before the STP or WIT instruction is executed.



Note: Insert a damping resistor if required.
The resistance will vary depending on the oscillator and the oscillation drive capacity setting.
Use the value recommended by the maker of the oscillator.
Also, if the oscillator manufacturer's data sheet specifies that a feedback resistor be added external to the chip though a feedback resistor exists on-chip, insert a feedback resistor between XIN and XOUT following the instruction.

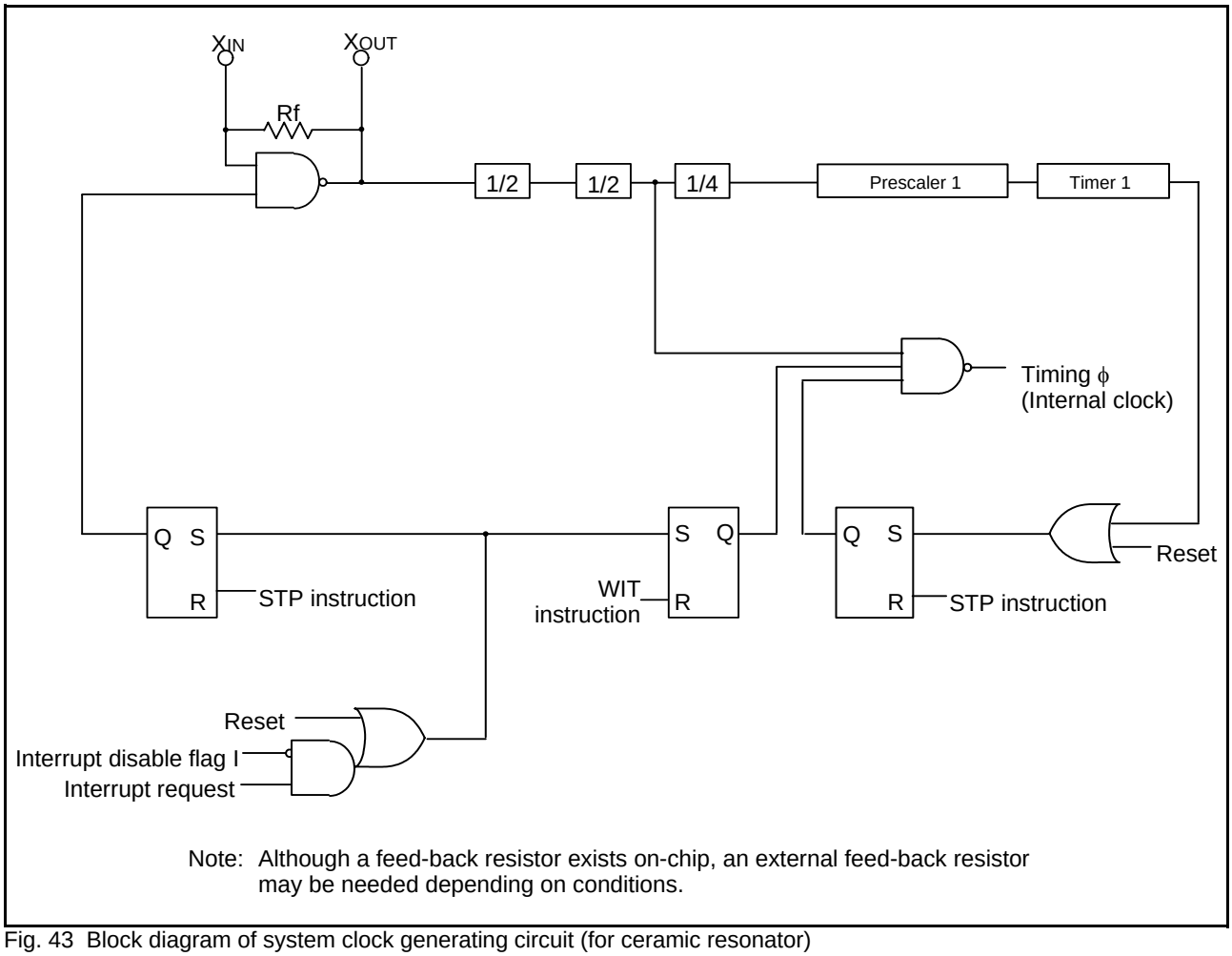
Fig. 41 External circuit of ceramic resonator/quartz-crystal oscillator



Note : The bit can be rewritten only once after releasing reset.
After rewriting, it is disabled to write any data to this bit.
However, by reset the bit is initialized and can be rewritten, again.
It is not disabled to write any data to this bit for emulator MCU "M37545RLSS."

Fig. 42 Structure of CPU mode register

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Note: Although a feed-back resistor exists on-chip, an external feed-back resistor may be needed depending on conditions.

Fig. 43 Block diagram of system clock generating circuit (for ceramic resonator)

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QzROM Writing Mode

In the QzROM writing mode, the user ROM area can be rewritten while the microcomputer is mounted on-board by using a serial programmer which is applicable for this microcomputer.
Table 10 lists the pin description (QzROM writing mode) and Figure 44 and Figure 45 show the pin connections.
Refer to Figure 46 and Figure 47 for examples of a connection with a serial programmer.
Contact the manufacturer of your serial programmer for serial programmer. Refer to the user's manual of your serial programmer for details on how to use it.

Table 10 Pin description (QzROM writing mode)

Pin	Name	I/O	Function
V_{CC}, V_{SS}, V_{DDR}	Power source	Input	• Apply 1.8 to 3.6 V to V_{CC}, and 0 V to V_{SS} and V_{DDR}.
$\overline{RESET}$	Reset input	Input	• Reset input pin for active "L". Reset occurs when $\overline{RESET}$ pin is hold at an "L"level for 16 cycles or more of X_{IN}.
X_{IN}	Clock input	Input	• Set the same termination as the single-chip mode.
X_{OUT}	Clock output	Output	
$P0_0$–$P0_5$ $P2_1$–$P2_7$ $P3_0$–$P3_7$ $P4_2$	I/O port	I/O	• Input "H" or "L" level signal or leave the pin open.
CNV_{SS}	V_{PP} input	Input	• QzROM programmable power source pin.
$P0_7$	ESDA input/output	I/O	• Serial data I/O pin.
$P2_0$	ESCLK input	Input	• Serial clock input pin.
$P0_6$	ESPGMB input	Input	• Read/program pulse input pin.

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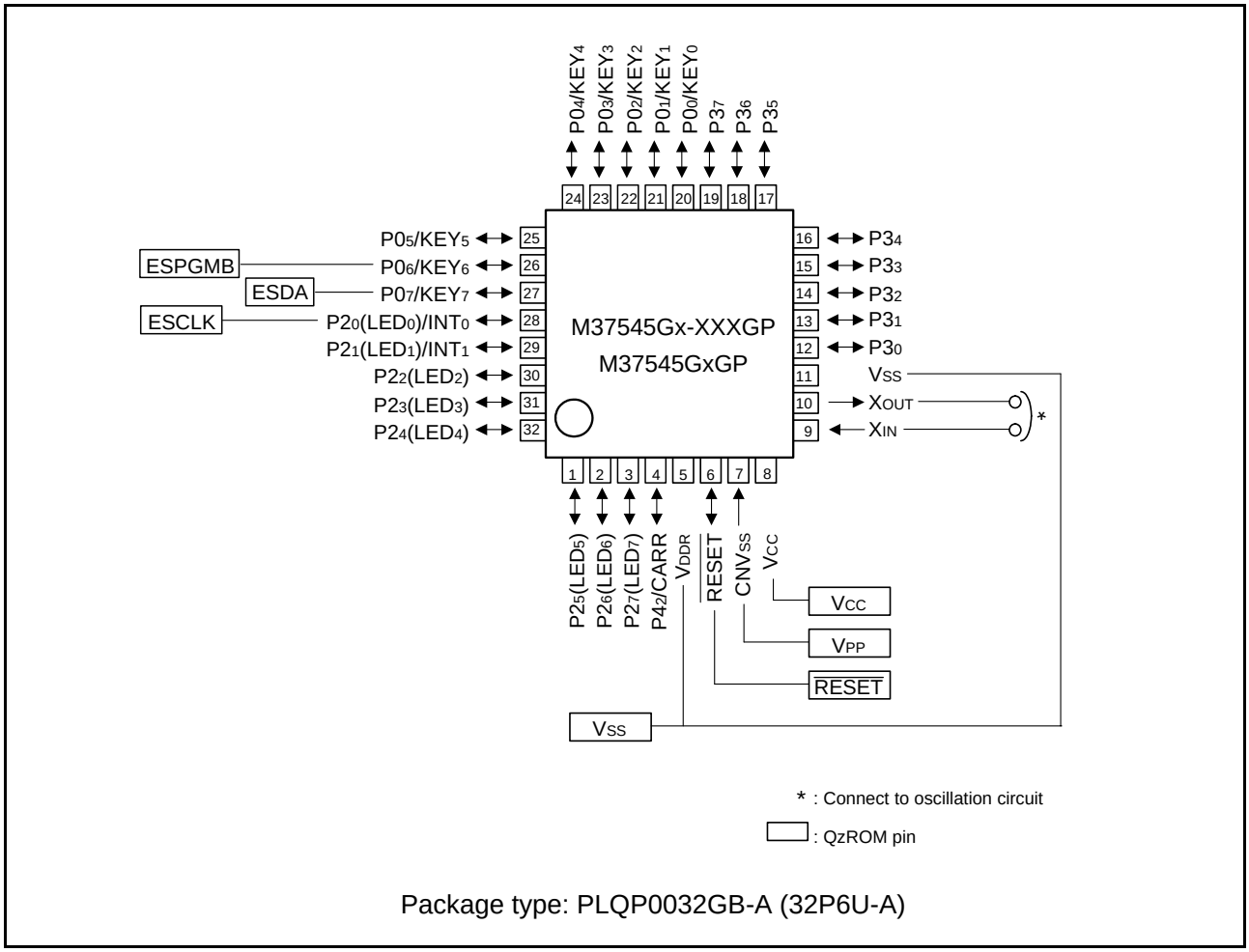


Fig. 44 Pin connection diagram (M37545Gx-XXXGP)

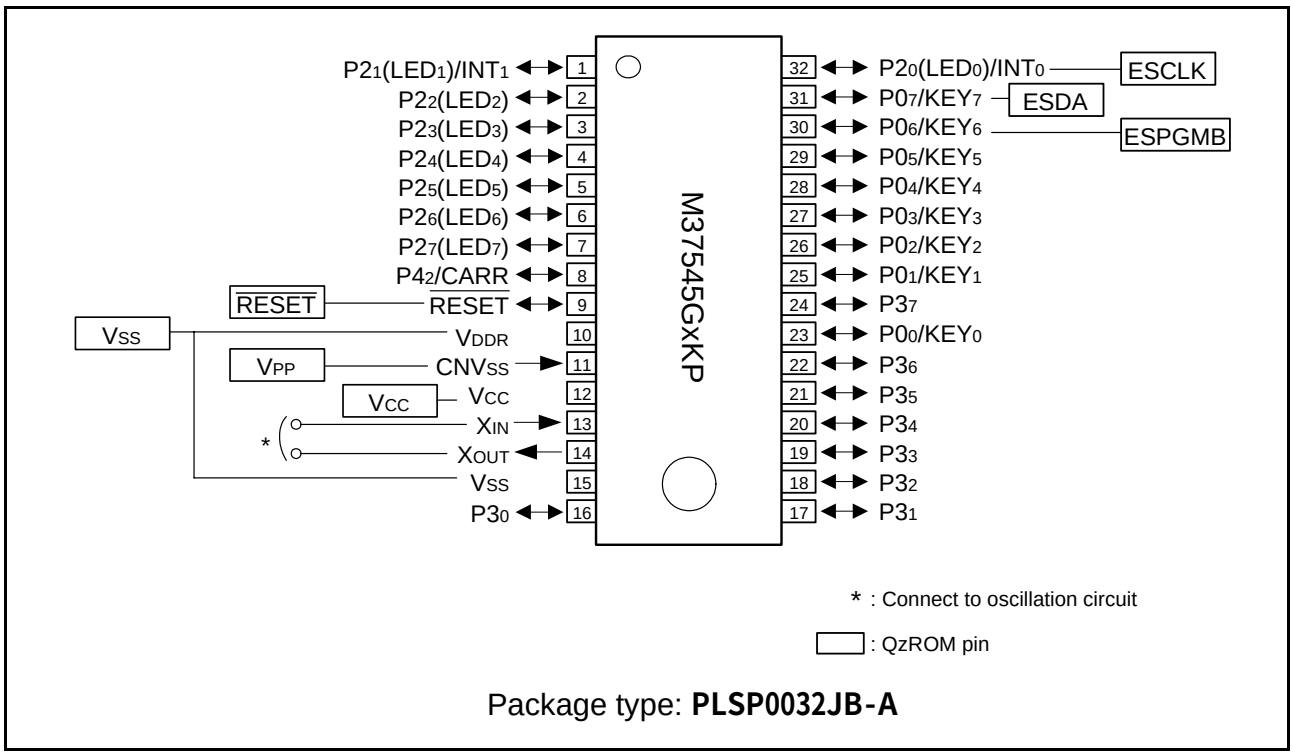


Fig. 45 Pin connection diagram (M37545GxKP)

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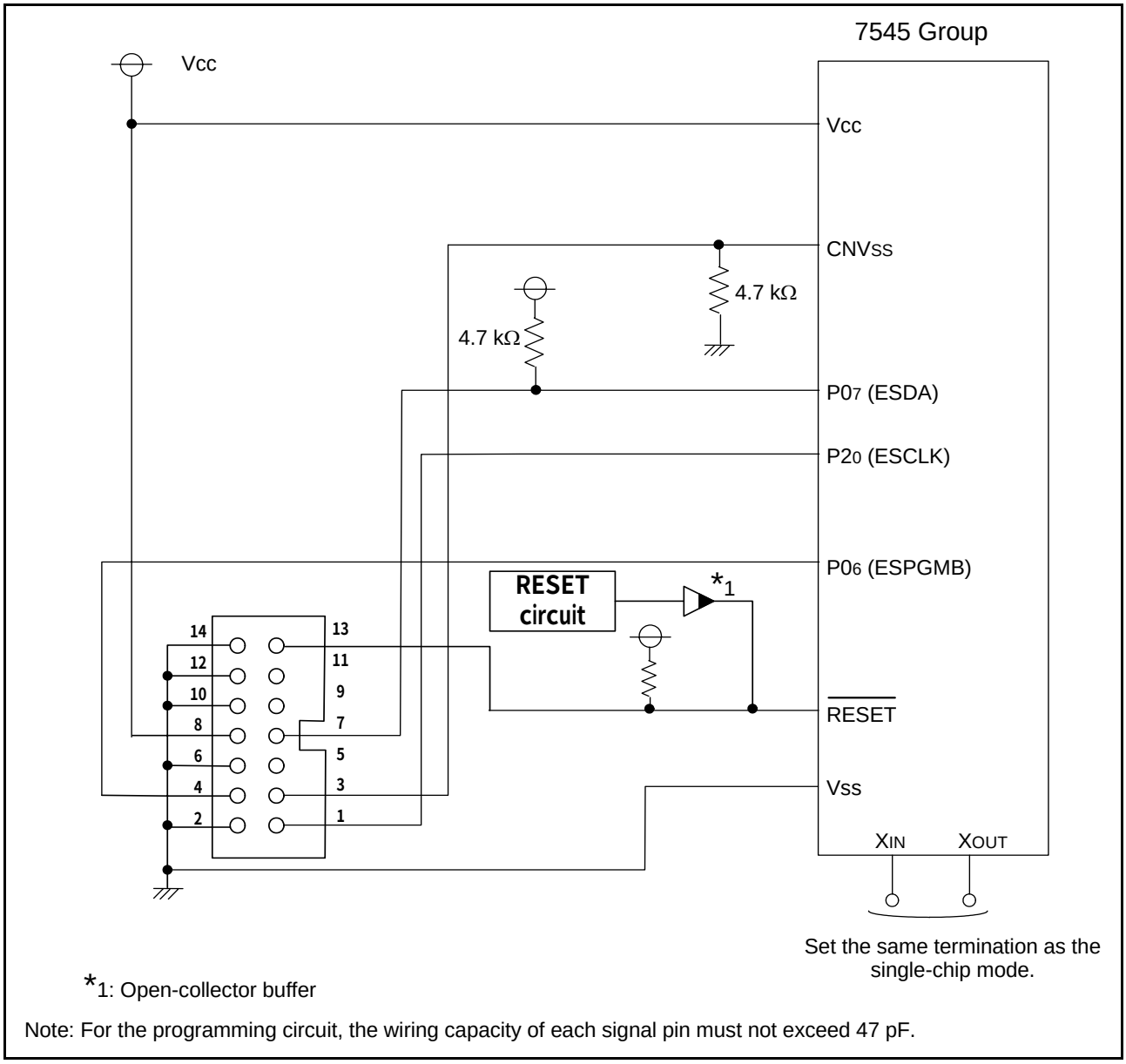


Fig. 46 When using E8 programmer, connection example

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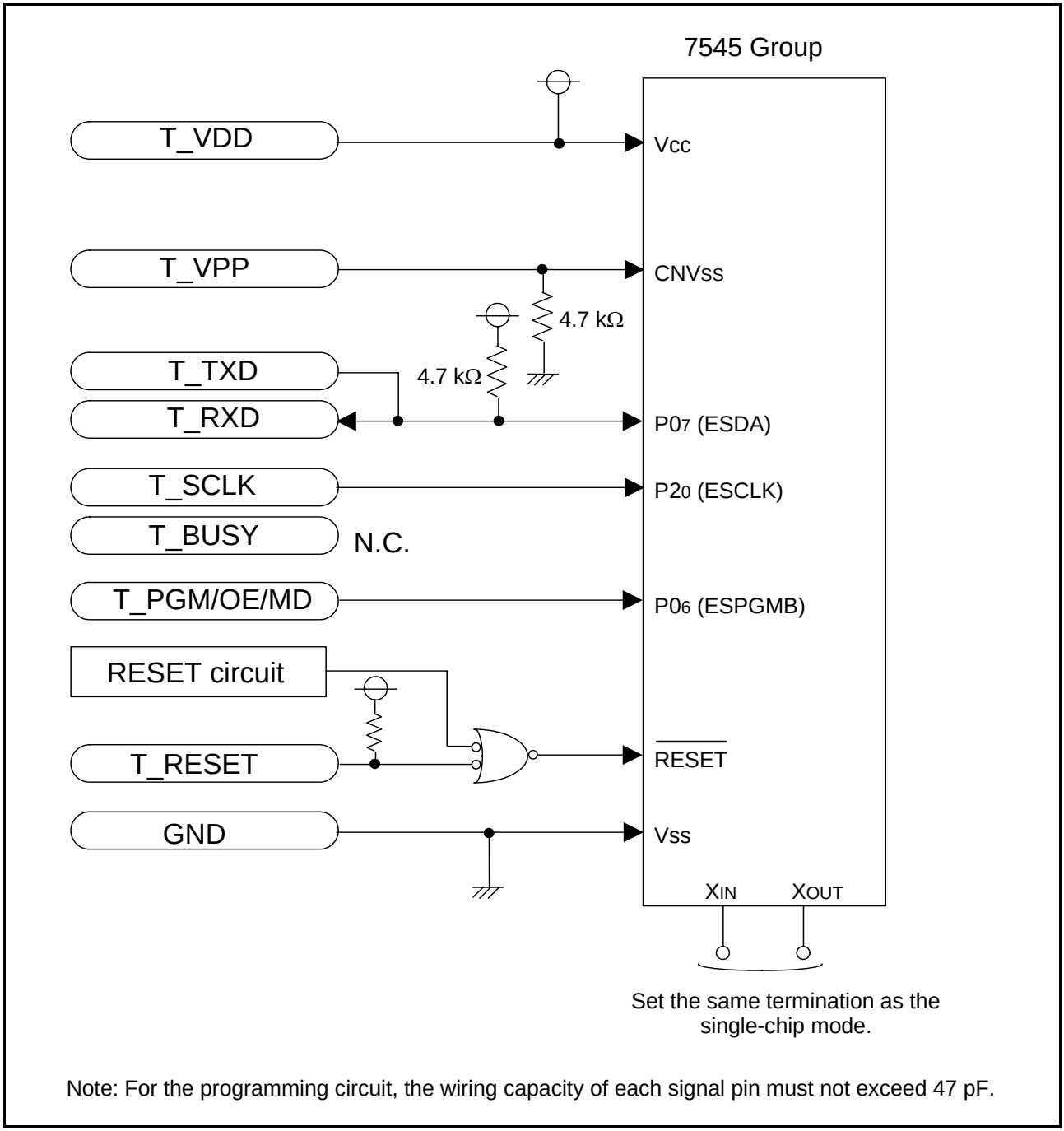


Fig. 47 When using programmer of Suisei Electronics System Co., LTD, connection example

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NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after reset are undefined except for the interrupt disable flag I which is "1". After reset, initialize flags which affect program execution. In particular, it is essential to initialize the T flag and the D flag because of their effect on calculations. Initialize these flags at beginning of the program.

Interrupts

The contents of the interrupt request bit do not change even if the BBC or BBS instruction is executed immediately after they are changed by program because this instruction is executed for the previous contents. For executing the instruction for the changed contents, execute one instruction before executing the BBC or BBS instruction.

Decimal Calculations

- For calculations in decimal notation, set the decimal mode flag D to "1", then execute the ADC instruction or SBC instruction. In this case, execute SEC instruction, CLC instruction or CLD instruction after executing one instruction before the ADC instruction or SBC instruction.
- In the decimal mode, the values of the N (negative), V (overflow) and Z (zero) flags are invalid.

Ports

The values of the port direction registers cannot be read.
That is, it is impossible to use the LDA instruction, memory operation instruction when the T flag is "1", addressing mode using direction register values as qualifiers, and bit test instructions such as BBC and BBS.
It is also impossible to use bit operation instructions such as CLB and SEB and read/modify/write instructions of direction registers for calculations such as ROR.
For setting direction registers, use the LDM instruction, STA instruction, etc.

Instruction Execution Timing

The instruction execution time can be obtained by multiplying the frequency of the internal clock ϕ by the number of cycles mentioned in the machine-language instruction table.
The frequency of the internal clock ϕ is 4 times the X_{IN} cycle.

CPU Mode Register

The processor mode bits can be rewritten only once after releasing reset. However, after rewriting it is disable to write any value to the bit. (Emulator MCU is excluded.)

NOTES ON HARDWARE

Handling of Power Source Pin

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (V_{CC} pin) and GND pin (V_{SS} pin). Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, a ceramic capacitor of 0.01 μF to 0.1 μF is recommended.

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NOTES ON USE

Countermeasures Against Noise

1. Shortest wiring length

(1) Package

Select the smallest possible package to make the total wiring length short.
<Reason>
The wiring length depends on a microcomputer package. Use of a small package, for example QFP and not DIP, makes the total wiring length short to reduce influence of noise.

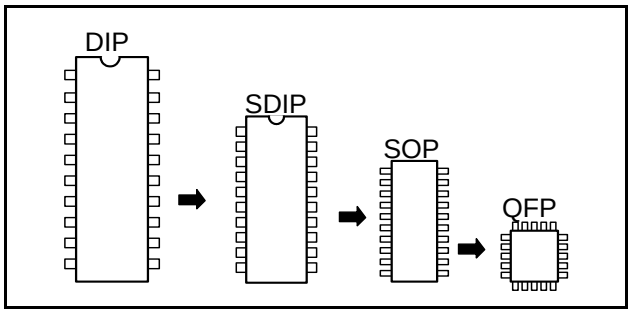


Fig. 48 Selection of packages

(2) Wiring for $\overline{\text{RESET}}$ pin

Make the length of wiring which is connected to the $\overline{\text{RESET}}$ pin as short as possible. Especially, connect a capacitor across the $\overline{\text{RESET}}$ pin and the Vss pin with the shortest possible wiring (within 20 mm).
<Reason>
The width of a pulse input into the $\overline{\text{RESET}}$ pin is determined by the timing necessary conditions. If noise having a shorter pulse width than the standard is input to the $\overline{\text{RESET}}$ pin, the reset is released before the internal state of the microcomputer is completely initialized. This may cause a program runaway.

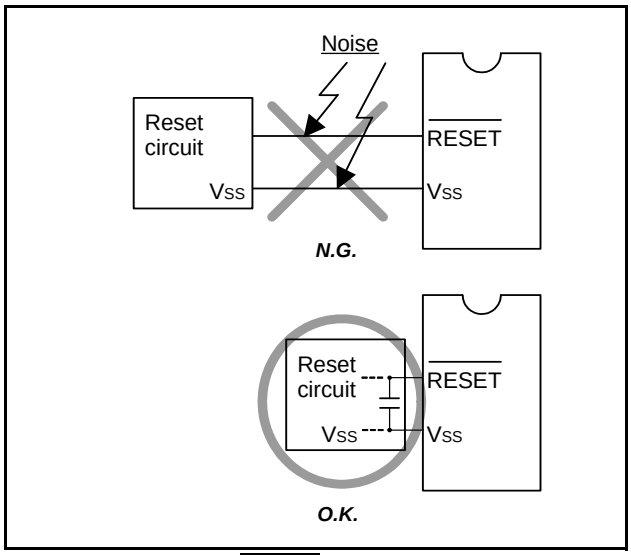


Fig. 49 Wiring for the $\overline{\text{RESET}}$ pin

(3) Wiring for clock input/output pins

- Make the length of wiring which is connected to clock I/O pins as short as possible.
- Make the length of wiring (within 20 mm) across the grounding lead of a capacitor which is connected to an oscillator and the Vss pin of a microcomputer as short as possible.
- Separate the Vss pattern only for oscillation from other Vss patterns.

<Reason>
If noise enters clock I/O pins, clock waveforms may be deformed. This may cause a program failure or program runaway. Also, if a potential difference is caused by the noise between the Vss level of a microcomputer and the Vss level of an oscillator, the correct clock will not be input in the microcomputer.

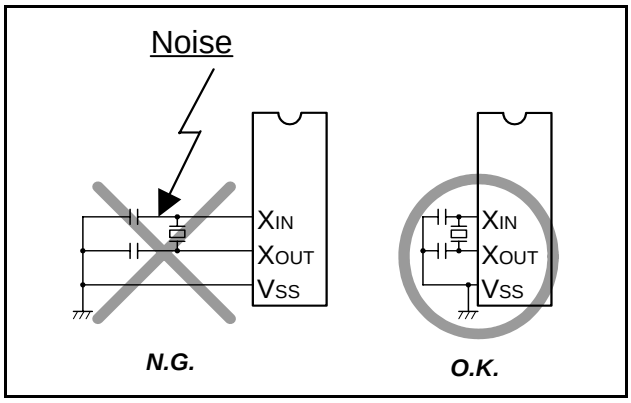


Fig. 50 Wiring for clock I/O pins

(4) Wiring to CNVss pin

Connect CNVss pin to a GND pattern at the shortest distance.
The GND pattern is required to be as close as possible to the GND supplied to Vss.
In order to improve the noise reduction, to connect a 5 kΩ resistor serially to the CNVss pin - GND line may be valid.
As well as the above-mentioned, in this case, connect to a GND pattern at the shortest distance. The GND pattern is required to be as close as possible to the GND supplied to Vss.
<Reason>
The CNVss pin of the QzROM is the power source input pin for the built-in QzROM. When programming in the built-in QzROM, the impedance of the CNVss pin is low to allow the electric current for writing flow into the QzROM. Because of this, noise can enter easily. If noise enters the CNVss pin, abnormal instruction codes or data are read from the built-in QzROM, which may cause a program runaway.

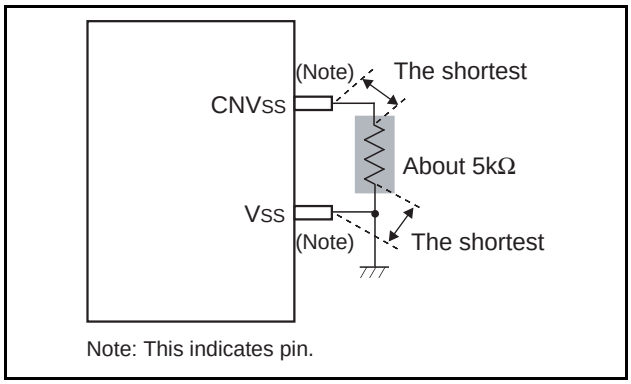


Fig. 51 Wiring for the VPP pin of the QzROM

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2. Connection of bypass capacitor

(1) Connection of bypass capacitor across Vss line and Vcc line

Connect an approximately 0.1 µF bypass capacitor across the VSS line and the VCC line as follows:

- Connect a bypass capacitor across the VSS pin and the VCC pin at equal length.
- Connect a bypass capacitor across the VSS pin and the VCC pin with the shortest possible wiring.
- Use lines with a larger diameter than other signal lines for VSS line and VCC line.
- Connect the power source wiring via a bypass capacitor to the VSS pin and the VCC pin.

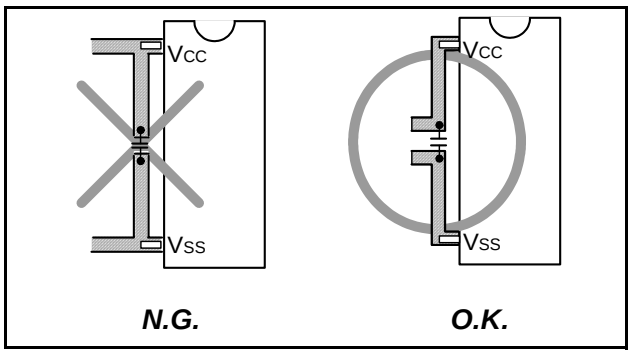


Fig. 52 Bypass capacitor across the VSS line and the VCC line

(2) Connection of bypass capacitor across Vss line and VDDR line

Connect an approximately 0.1 µF bypass capacitor across the VSS line and the VDDR line as follows:

- Connect a bypass capacitor across the VSS pin and the VDDR pin at equal length.
- Connect a bypass capacitor across the VSS pin and the VDDR pin with the shortest possible wiring.
- Use lines with a larger diameter than other signal lines for VSS line and VDDR line.
- Connect the power source wiring via a bypass capacitor to the VSS pin and the VDDR pin.

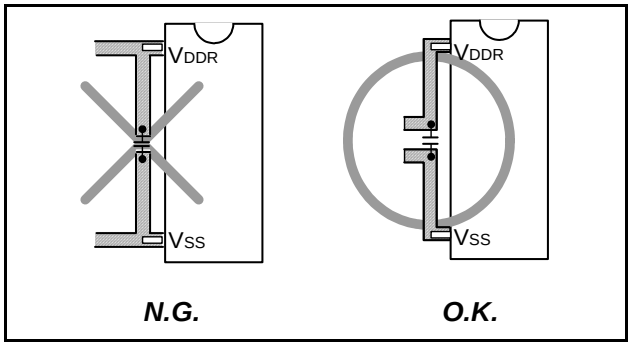


Fig. 53 Bypass capacitor across the VSS line and the VDDR line

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3. Oscillator concerns

So that the product obtains the stabilized operation clock on the user system and its condition, contact the resonator manufacturer and select the resonator and oscillation circuit constants.
Be careful especially when range of voltage and temperature is wide.
Take care to prevent an oscillator that generates clocks for a microcomputer operation from being affected by other signals.

(1) Keeping oscillator away from large current signal lines

Install a microcomputer (and especially an oscillator) as far as possible from signal lines where a current larger than the tolerance of current value flows.
<Reason>
In the system using a microcomputer, there are signal lines for controlling motors, LEDs, and thermal heads or others. When a large current flows through those signal lines, strong noise occurs because of mutual inductance.

(2) Installing oscillator away from signal lines where potential levels change frequently

Install an oscillator and a connecting pattern of an oscillator away from signal lines where potential levels change frequently. Also, do not cross such signal lines over the clock lines or the signal lines which are sensitive to noise.
<Reason>
Signal lines where potential levels change frequently (such as the CARR pin signal line) may affect other lines at signal rising edge or falling edge. If such lines cross over a clock line, clock waveforms may be deformed, which causes a microcomputer failure or a program runaway.

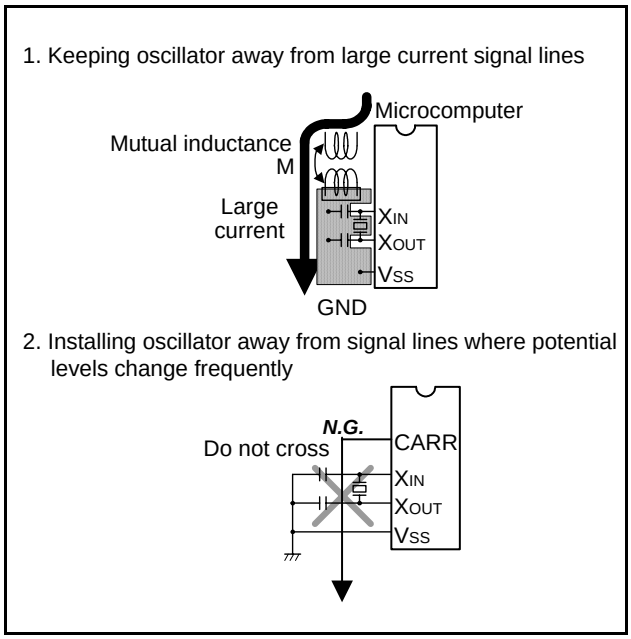


Fig. 54 Wiring for a large current signal line/Writing of signal lines where potential levels change frequently

(3) Oscillator protection using Vss pattern

As for a two-sided printed circuit board, print a VSS pattern on the underside (soldering side) of the position (on the component side) where an oscillator is mounted.
Connect the VSS pattern to the microcomputer VSS pin with the shortest possible wiring. Besides, separate this VSS pattern from other VSS patterns.

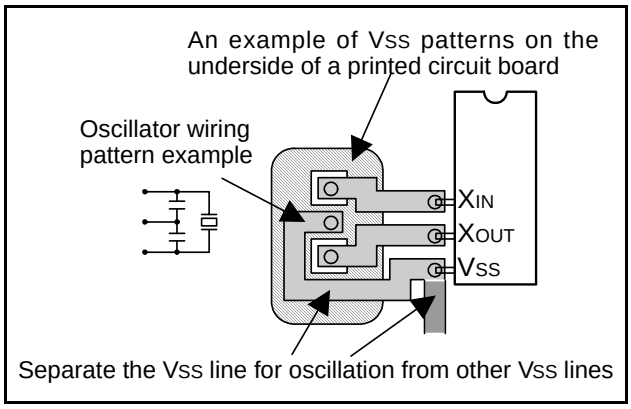


Fig. 55 Vss pattern on the underside of an oscillator

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4. Setup for I/O ports

Setup I/O ports using hardware and software as follows:

<Hardware>
- Connect a resistor of 100 Ω or more to an I/O port in series.

<Software>
- As for an input port, read data several times by a program for checking whether input levels are equal or not.
- As for an output port, since the output data may reverse because of noise, rewrite data to its port latch at fixed periods.
- Rewrite data to direction registers and pull-up control registers at fixed periods.

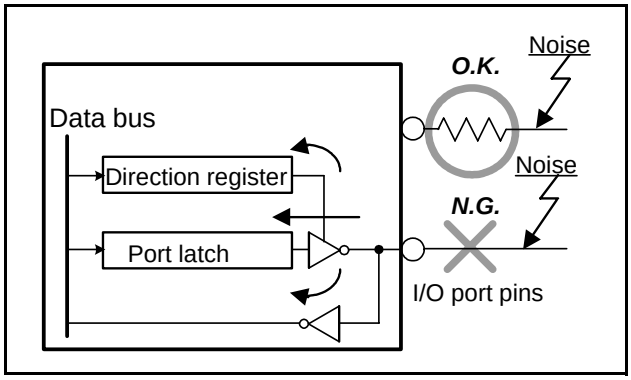


Fig. 56 Setup for I/O ports

5. Providing of watchdog timer function by software

If a microcomputer runs away because of noise or others, it can be detected by a software watchdog timer and the microcomputer can be reset to normal operation. This is equal to or more effective than program runaway detection by a hardware watchdog timer.

The following shows an example of a watchdog timer provided by software.

In the following example, to reset a microcomputer to normal operation, the main routine detects errors of the interrupt processing routine and the interrupt processing routine detects errors of the main routine.

This example assumes that interrupt processing is repeated multiple times in a single main routine processing.

<The main routine>
- Assigns a single byte of RAM to a software watchdog timer (SWDT) and writes the initial value N in the SWDT once at each execution of the main routine. The initial value N should satisfy the following condition:
  N+1 ≥ (Counts of interrupt processing executed in each main routine)
  As the main routine execution cycle may change because of an interrupt processing or others, the initial value N should have a margin.
- Watches the operation of the interrupt processing routine by comparing the SWDT contents with counts of interrupt processing after the initial value N has been set.
- Detects that the interrupt processing routine has failed and determines to branch to the program initialization routine for recovery processing in the following case:
  If the SWDT contents do not change after interrupt processing.

<The interrupt processing routine>
- Decrements the SWDT contents by 1 at each interrupt processing.
- Determines that the main routine operates normally when the SWDT contents are reset to the initial value N at almost fixed cycles (at the fixed interrupt processing count).
- Detects that the main routine has failed and determines to branch to the program initialization routine for recovery processing in the following case:
  If the SWDT contents are not initialized to the initial value N but continued to decrement and if they reach 0 or less.

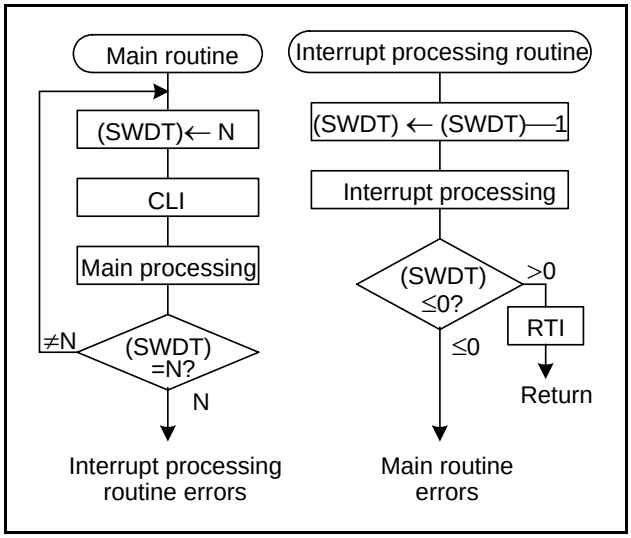


Fig. 57 Watchdog timer by software

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Notes on QzROM

1. Note on Product shipped in blank

As for the product shipped in blank, Renesas does not perform the writing test to user ROM area after the assembly process though the QzROM writing test is performed enough before the assembly process. Therefore, a writing error of approx.0.1 % may occur.
Moreover, please note the contact of cables and foreign bodies on a socket, etc. because a writing environment may cause some writing errors.

2. Precautions Regarding Overvoltage

Make sure that voltage exceeding the V_{CC} pin voltage is not applied to other pins. In particular, ensure that the state indicated by bold lines in Figure below does not occur for pin CNV_{SS} (V_{PP} power source pin for QzROM) during power-on or power-off. Otherwise the contents of QzROM could be rewritten.

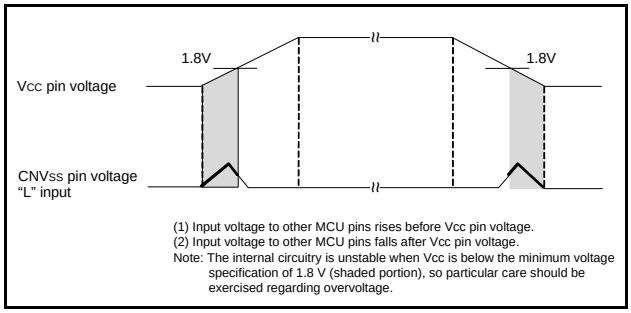


Fig. 58 Timing Diagram (bold-lined periods are applicable)

3. QzROM Writing Orders

When ordering the QzROM product shipped after writing, submit the mask file (extension: .mask) which is made by the mask file converter MM.
Be sure to set the ROM option ("MASK option" written in the mask file converter) setup when making the mask file by using the mask file converter MM.

- Be sure to set the ROM option data* setup when making the mask file by using the mask file converter MM.. The ROM code protect is specified according to the ROM option data* in the mask file which is submitted at ordering. Note that the mask file which has nothing at the ROM option data* or has the data other than "00_{16}" and "FF_{16}" can not be accepted.
- Set "FF_{16}" to the ROM code protect address in ROM data regardless of the presence or absence of a protect. When data other than "FF_{16}" is set, we may ask that the ROM data be submitted again.

* ROM option data: mask option noted in MM

4. Data Required for QzROM Writing Orders

The following are necessary when ordering a QzROM product shipped after writing:
1. QzROM Writing Confirmation Form*
2. Mark Specification Form*
3. ROM data.....Mask file

* For the QzROM writing confirmation form and the mark specification form, refer to the "Renesas Technology Corp." Homepage (http://www.renesas.com/homepage.jsp).
Note that we cannot deal with special font marking (customer's trademark etc.) in QzROM microcomputer.

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ELECTRICAL CHARACTERISTICS (QzROM version)

Absolute Maximum Ratings

Table 11 Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage V_{CC}, V_{DDR}	All voltages are based on V_{SS}. When an input voltage is measured, output transistors are cut off.	–0.3 to 5.0	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_1$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_2$		–0.3 to V_{CC} + 0.3	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		–0.3 to V_{CC} + 0.3	V
V_I	Input voltage CNV_{SS}		–0.3 to V_{CC} + 0.3	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_1$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_2$, X_{OUT}, $\overline{RESET}$		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation	Ta = 25°C	200	mW
T_{opr}	Operating temperature	–	–20 to 85	°C
T_{stg}	Storage temperature	–	–40 to 125	°C

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Recommended Operating Conditions

Table 12 Recommended operating conditions (1) (Vcc = 1.8 to 3.6 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage (At 4MHz)		1.8	3.0	3.6	V
V_{SS}	Power source voltage			0		V
V_{IH}	"H" input voltage $P0_0$–$P0_7$, $P1_0$–$P1_1$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_2$		0.7Vcc		Vcc	V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}		0.8Vcc		Vcc	V
V_{IL}	"L" input voltage $P0_0$–$P0_7$, $P1_0$–$P1_1$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_2$		0		0.3Vcc	V
V_{IL}	"L" input voltage $\overline{RESET}$, CNV_{SS}		0		0.2Vcc	V
V_{IL}	"L" input voltage X_{IN}		0		0.16Vcc	V
ΣI_{OH}(peak)	"H" total peak output current (1) $P0_0$–$P0_7$, $P1_0$–$P1_1$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_2$				–80	mA
ΣI_{OL}(peak)	"L" total peak output current (1) $P0_0$–$P0_7$, $P1_0$–$P1_1$, $P3_0$–$P3_7$				80	mA
ΣI_{OL}(peak)	"L" total peak output current (1) $P2_0$–$P2_7$, $P4_0$–$P4_2$				80	mA
ΣI_{OH}(avg)	"H" total average output current (1) $P0_0$–$P0_7$, $P1_0$–$P1_1$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_2$				–40	mA
ΣI_{OL}(avg)	"L" total average output current (1) $P0_0$–$P0_7$, $P1_0$–$P1_1$, $P3_0$–$P3_7$				40	mA
ΣI_{OL}(avg)	"L" total average output current (1) $P2_0$–$P2_7$, $P4_0$–$P4_2$				40	mA
I_{OH}(peak)	"H" peak output current (2) $P0_0$–$P0_7$, $P1_0$–$P1_1$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_1$	Vcc = 3.0 V			–4	mA
I_{OH}(peak)	"H" peak output current (2) $P4_2$	Vcc = 3.0 V			–20	mA
I_{OL}(peak)	"L" peak output current (2) $P0_0$–$P0_7$, $P1_0$–$P1_1$, $P3_0$–$P3_7$	Vcc = 3.0 V			4	mA
I_{OL}(peak)	"L" peak output current (2) $P2_0$–$P2_7$, $P4_0$–$P4_2$	Vcc = 3.0 V			24	mA
I_{OH}(avg)	"H" average output current (3) $P0_0$–$P0_7$, $P1_0$–$P1_1$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_1$	Vcc = 3.0 V			–2	mA
I_{OH}(avg)	"H" average output current (3) $P4_2$	Vcc = 3.0 V			–10	mA
I_{OL}(avg)	"L" average output current (3) $P0_0$–$P0_7$, $P1_0$–$P1_1$, $P3_0$–$P3_7$	Vcc = 3.0 V			2	mA
I_{OL}(avg)	"L" average output current (3) $P2_0$–$P2_7$, $P4_0$–$P4_2$	Vcc = 3.0 V			12	mA
f(X_{IN})	Internal clock oscillation frequency (4) at ceramic oscillation or external clock input	Vcc = 1.8 to 3.6 V			4	MHz
V_{DET}	Detection voltage of voltage drop detection circuit	Ta = –20 to 85 °C	1.65	1.75	1.85	V
		Ta = 0 to 50 °C	1.70	1.75	1.80	V
T_{DET}	Low-voltage detection time of voltage drop detection circuit	When detected voltage passes detection voltage at ±50V/S		0.2	1.2	ms
T_{PON}	Power-on reset circuit valid supply voltage rising time	Vcc = 0 to 1.8 V			1	ms

NOTES:
1. The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.
2. The peak output current is the peak current flowing in each port.
3. The average output current I_{OL} (avg), I_{OH} (avg) in an average value measured over 100 ms.
4. When the oscillation frequency has a duty cycle of 50 %.

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Electrical Characteristics

Table 13 Electrical characteristics (1) (V_{CC} = 1.8 to 3.6 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_1$, $P2_0$–$P2_7$, $P3_0$–$P3_7$ (1) $P4_0$–$P4_1$	I_{OH} = –2.0 mA V_{CC} = 3.0 V	2.1			V
V_{OH}	"H" output voltage $P4_2$	I_{OH} = –10 mA V_{CC} = 3.0 V	1.0			V
V_{OL}	"L" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_1$, $P3_0$–$P3_7$	I_{OL} = 2 mA V_{CC} = 3.0 V			0.9	V
V_{OL}	"L" output voltage $P2_0$–$P2_7$, $P4_0$–$P4_2$	I_{OL} = 12 mA V_{CC} = 3.0 V			1.5	V
V_{T+}–V_{T-}	Hysteresis INT_0, INT_1, $P0_0$–$P0_7$ (2)	V_{CC} = 3.0 V		0.3		V
V_{T+}–V_{T-}	Hysteresis $\overline{RESET}$	V_{CC} = 3.0 V		0.45		V
I_{IH}	"H" input current $P0_0$–$P0_7$, $P1_0$–$P1_1$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_2$	V_I = V_{CC} (Pin floating. Pull up transistors "off")			5.0	µA
I_{IH}	"H" input current $\overline{RESET}$	V_I = V_{CC}			5.0	µA
I_{IL}	"L" input current $P0_0$–$P0_7$, $P1_0$–$P1_1$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_2$	V_I = V_{SS} (Pin floating. Pull up transistors "off")			–5.0	µA
R_{FB}	Feed-back resistor value between X_{IN}-X_{OUT}	V_{CC} = 3.0 V, V_I = 3.0 V	700		3200	kΩ
R_{PH}	Pull-up resistor value $P0_0$–$P0_7$	V_{CC} = 3.0 V, V_I = 0 V	50	120	250	kΩ
R_{PH}	Pull-up resistor value $\overline{RESET}$	V_{CC} = 3.0 V, V_I = 0 V	25	60	130	kΩ
R_{PL}	Pull-down resistor value $\overline{RESET}$	V_{CC} = 3.0 V, V_I = 3.0 V		7.0		kΩ
V_{RAM1}	RAM1 hold voltage (V_{CC})	When clock stopped	1.1		3.6	V
V_{RAM2}	RAM2 hold voltage (V_{DDR})	When clock stopped and reset by voltage drop detection	1.1			V

NOTES:
1. In this case, CMOS output is selected by the port output mode selection register.
2. It is available only when operating key-on wake up.

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Electrical Characteristics (continued)

Table 14 Electrical characteristics (2) (**Vcc** = 1.8 to 3.6 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
I_{CC}	Power source current	V_{CC} = 3.0 V, f(X_{IN}) = 4 MHz Output transistors “off”			0.6	1.2	mA
		V_{CC} = 3.0 V, f(X_{IN}) = 4 MHz (in WIT state), functions except timer 1 disabled, Output transistors “off”			0.3	0.6	mA
		All oscillation stopped (in STP state) Output transistors “off” $V_{CC} \geq V_{DDR} \geq V_{CC} - 0.6$ V	Ta = 25°C		0.1	1.0	µA
			Ta = 85°C			10.0	µA
I_{DDR}		During reset by voltage drop detection circuit V_{DDR} = 1.1 V, 1.8 V ≥ V_{CC} ≥ 0 V	Ta = 25°C		0.1	1.0	µA
			Ta = 85°C			10.0	µA

Timing Requirements

Table 15 Timing Requirements (V_{CC} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{w(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{C(X_{IN})}$	External clock input cycle time	250			ns
$t_{WH(X_{IN})}$	External clock input “H” pulse width	100			ns
$t_{WL(X_{IN})}$	External clock input “L” pulse width	100			ns
$t_{WH(INT_0)}$	INT_0, INT_1, input “H” pulse width	460			ns
$t_{WL(INT_0)}$	INT_0, INT_1, input “L” pulse width	460			ns

Switching Characteristics

Table 16 Switching Characteristics (V_{CC} = 1.8 to 3.6 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{r(CMOS)}$	CMOS output rising time (1)		25	100	ns
$t_{f(CMOS)}$	CMOS output falling time (1)		25	100	ns

NOTE:
1. Pin X_{OUT} is excluded

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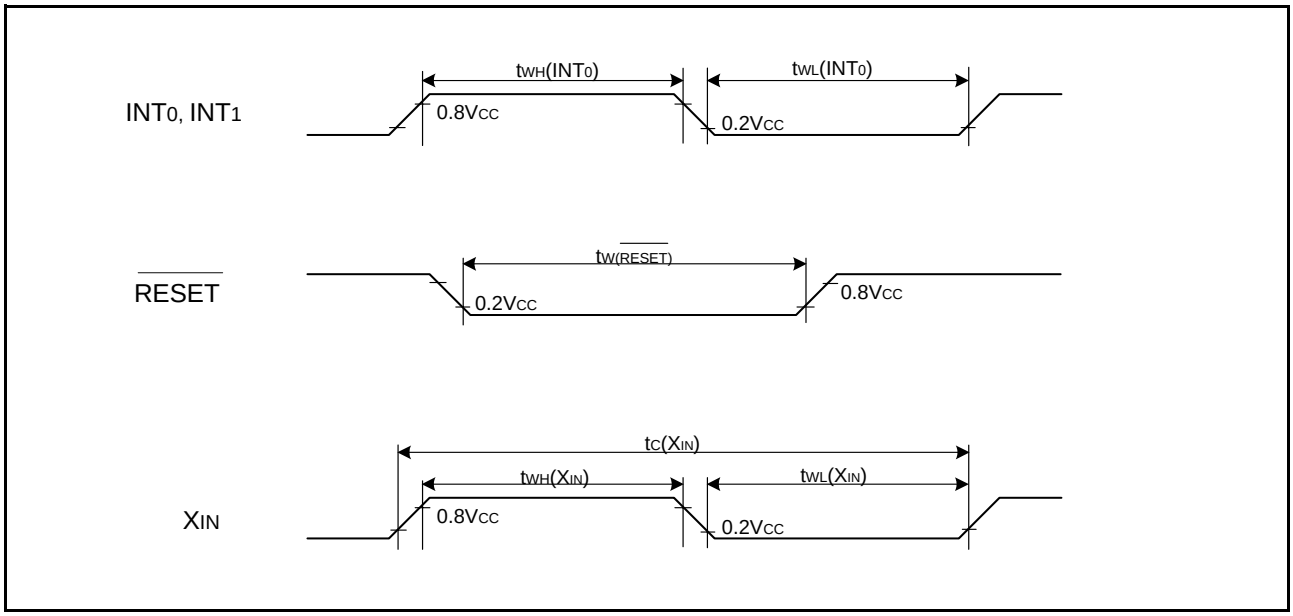


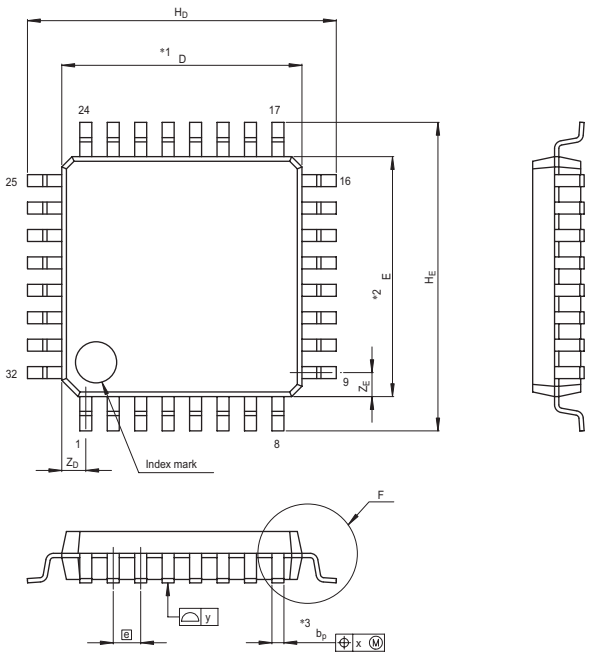
Fig 59. Timing chart

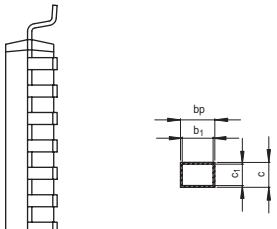
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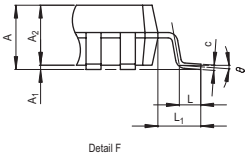
PACKAGE OUTLINE

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP32-7x7-0.80	PLQP0032GB-A	32P6U-A	0.2g



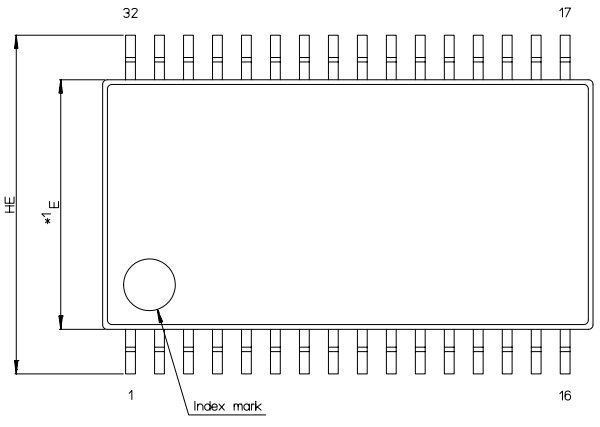


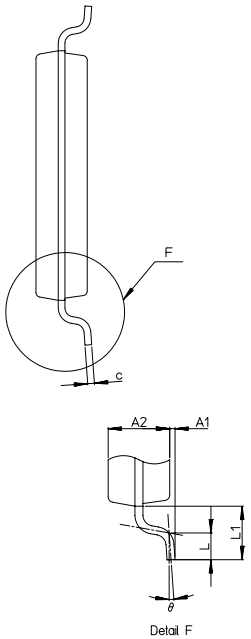


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	0.7	—
Z_E	—	0.7	—
L	0.3	0.5	0.7
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS [Typ.]
P-LSSOP32-5.6x11-0.65	PLSP0032JB-A	32P2X-B	0.18 g





NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	10.9	11.0	11.3
E	5.4	5.6	5.8
A2	—	1.15	—
A	—	—	1.45
A1	0.0	0.1	0.2
bp	0.12	0.22	0.32
c	0.10	0.15	0.25
θ	0°	—	10°
HE	7.3	7.6	7.9
e	—	0.65	—
y	—	—	0.10
L	0.30	0.50	0.70
L1	—	1.00	—

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APPENDIX

NOTES ON PROGRAMMING

Processor Status Register

1. Initializing of processor status register

Flags which affect program execution must be initialized after a reset.
In particular, it is essential to initialize the T and D flags because they have an important effect on calculations. Initialize these flags at beginning of the program.
<Reason>
After a reset, the contents of the processor status register (PS) are undefined except for the I flag which is "1".

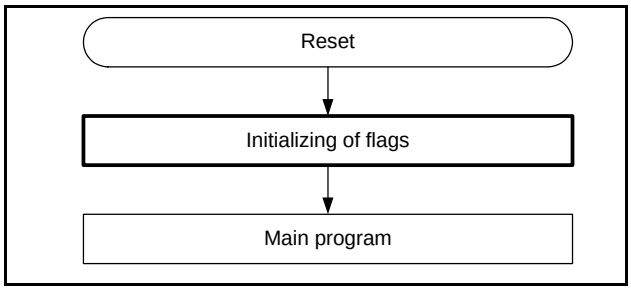


Fig 1. Initialization of processor status register

2. How to reference the processor status register

To reference the contents of the processor status register (PS), execute the PHP instruction once then read the contents of (S+1). If necessary, execute the PLP instruction to return the PS to its original status.

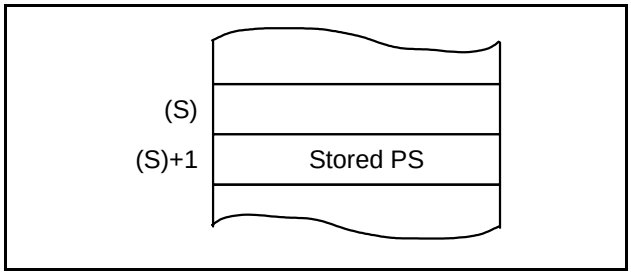


Fig 2. Stack memory contents after PHP instruction execution

Decimal Calculations

1. Execution of decimal calculations

The ADC and SBC are the only instructions which will yield proper decimal notation, set the decimal mode flag (D) to "1" with the SED instruction. After executing the ADC or SBC instruction, execute another instruction before executing the SEC, CLC, or CLD instruction.

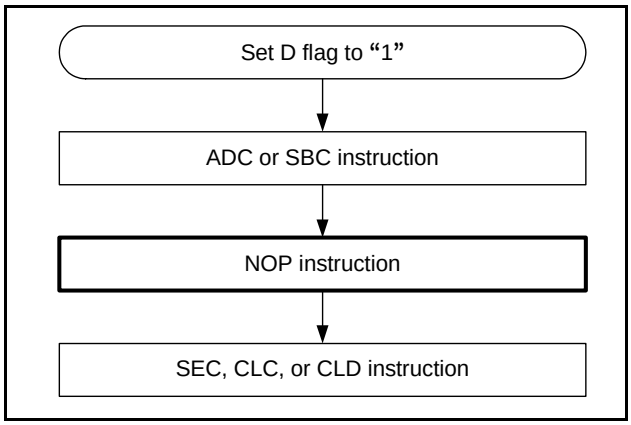


Fig 3. Instructions for decimal calculations

2. Notes on status flag in decimal mode

When decimal mode is selected, the values of three of the flags in the status register (the N, V, and Z flags) are invalid after a ADC or SBC instruction is executed.
The carry flag (C) is set to "1" if a carry is generated as a result of the calculation, or is cleared to "0" if a borrow is generated. To determine whether a calculation has generated a carry, the C flag must be initialized to "0" before each calculation. To check for a borrow, the C flag must be initialized to "1" before each calculation.

3. JMP instruction

When using the JMP instruction in indirect addressing mode, do not specify the last address on a page as an indirect address.

4. Multiplication and division instructions

(1) The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
(2) The execution of these instructions does not change the contents of the processor status register.

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5. Read-modify-write instruction

Do not execute a read-modify-write instruction to the read invalid address (SFR).
The read-modify-write instruction operates in the following sequence: read one-byte of data from memory, modify the data, write the data back to original memory. The following instructions are classified as the read-modify-write instructions in the 740 Family.

(1) Bit management instructions: CLB, SEB
(2) Shift and rotate instructions: ASL, LSR, ROL, ROR, RRF
(3) Add and subtract instructions: DEC, INC
(4) Logical operation instructions (1's complement): COM

Add and subtract/logical operation instructions (ADC, SBC, AND, EOR, and ORA) when T flag = "1" operate in the way as the read-modify-write instruction. Do not execute the read invalid SFR.
<Reason>
When the read-modify-write instruction is executed to read invalid SFR, the instruction may cause the following consequence: the instruction reads unspecified data from the area due to the read invalid condition. Then the instruction modifies this unspecified data and writes the data to the area. The result will be random data written to the area or some unexpected event.

NOTES ON PERIPHERAL FUNCTIONS

Notes on I/O Ports

1. Pull-up control register

When using each port which built in pull-up resistor as an output port, the pull-up control bit of corresponding port becomes invalid, and pull-up resistor is not connected.
<Reason>
Pull-up control is effective only when each direction register is set to the input mode.

2. Notes in stand-by state

In stand-by state*1 for low-power dissipation, do not make input levels of an input port and an I/O port "undefined".
Pull-up (connect the port to Vcc) or pull-down (connect the port to Vss) these ports through a resistor.
When determining a resistance value, note the following points:

- External circuit
- Variation of output levels during the ordinary operation
  When using a built-in pull-up resistor, note on varied current values:
- When setting as an input port : Fix its input level
- When setting as an output port : Prevent current from flowing out to external.

<Reason>
The output transistor becomes the OFF state, which causes the ports to be the high-impedance state. Note that the level becomes "undefined" depending on external circuits.
Accordingly, the potential which is input to the input buffer in a microcomputer is unstable in the state that input levels of an input port and an I/O port are "undefined". This may cause power source current.

*1 stand-by state : the stop mode by executing the STP instruction

3. Modifying output data with bit managing instruction

When the port latch of an I/O port is modified with the bit managing instruction*1, the value of the unspecified bit may be changed.
<Reason>
I/O ports are set to input or output mode in bit units. Reading from a port register or writing to it involves the following operations.

- Port in input mode
  Read: Read the pin level.
  Write: Write to the port latch.
- Port in output mode
  Read: Read the port latch or read the output from the peripheral function (specifications differ depending on the port).
  Write: Write to the port latch. (The port latch value is output from the pin.)

Since bit managing instructions*1 are read-modify-write instructions,*2 using such an instruction on a port register causes a read and write to be performed simultaneously on the bits other than the one specified by the instruction.
When an unspecified bit is in input mode, its pin level is read and that value is written to the port latch. If the previous value of the port latch differs from the pin level, the port latch value is changed.
If an unspecified bit is in output mode, the port latch is generally read. However, for some ports the peripheral function output is read, and the value is written to the port latch. In this case, if the previous value of the port latch differs from the peripheral function output, the port latch value is changed.

*1 Bit managing instructions: SEB and CLB instructions
*2 Read-modify-write instructions: Instructions that read memory in byte units, modify the value, and then write the result to the same location in memory in byte units

4. Direction register

The values of the port direction registers cannot be read.
That is, it is impossible to use the LDA instruction, memory operation instruction when the T flag is "1", addressing mode using direction register values as qualifiers, and bit test instructions such as BBC and BBS.
It is also impossible to use bit operation instructions such as CLB and SEB and read-modify-write instructions of direction registers for calculations such as ROR.
For setting direction registers, use the LDM instruction, STA instruction, etc.

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Termination of Unused Pins

1. Terminate unused pins

Perform the following wiring at the shortest possible distance (20 mm or less) from microcomputer pins.

(1) I/O ports

Set the I/O ports for the input mode and connect each pin to V_{CC} or V_{SS} through each resistor of 1 kΩ to 10 kΩ. The port which can select a built-in pull-up resistor can also use the built-in pull-up resistor.

When using the I/O ports as the output mode, open them at "L" or "H".

- When opening them in the output mode, the input mode of the initial status remains until the mode of the ports is switched over to the output mode by the program after reset. Thus, the potential at these pins is undefined and the power source current may increase in the input mode. With regard to an effects on the system, thoroughly perform system evaluation on the user side.
- Since the direction register setup may be changed because of a program runaway or noise, set direction registers by program periodically to increase the reliability of program.

2. Termination remarks

(1) I/O ports setting as input mode

(1) Do not open in the input mode.

<Reason>

- The power source current may increase depending on the first-stage circuit.
- An effect due to noise may be easily produced as compared with proper termination (1) shown on the above "1. Terminate unused pins".

(2) Do not connect to V_{CC} or V_{SS} directly.

<Reason>

If the direction register setup changes for the output mode because of a program runaway or noise, a short circuit may occur.

(3) Do not connect multiple ports in a lump to V_{CC} or V_{SS} through a resistor.

<Reason>

If the direction register setup changes for the output mode because of a program runaway or noise, a short circuit may occur between ports.

Notes on Interrupts

1. Change of relevant register settings

When not requiring for the interrupt occurrence synchronous with the following case, take the sequence shown in Figure 4.

- When switching external interrupt active edge
- When switching interrupt sources of an interrupt vector address where two or more interrupt sources are allocated

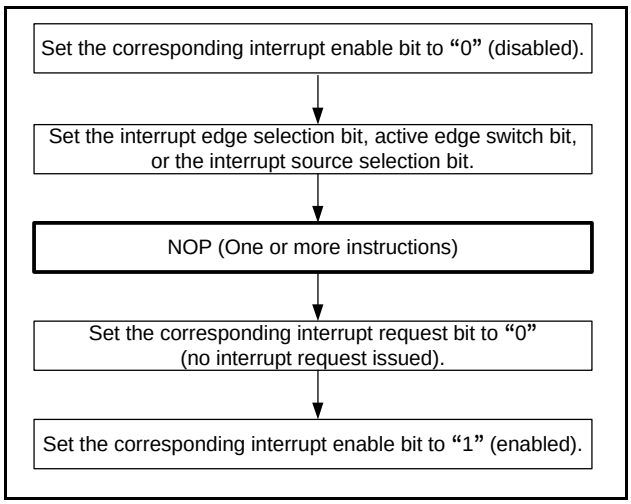


Fig 4. Sequence of changing relevant register

<Reason>

When setting the followings, the interrupt request bit of the corresponding interrupt may be set to "1".

- When switching external interrupt active edge
  INT_0 interrupt edge selection bit (bit 0 of Interrupt edge selection register (address $3A_{16}$))
  INT_1 interrupt edge selection bit (bit 1 of Interrupt edge selection register)
  Key-on wakeup edge selection register (address 19_{16})

2. Check of interrupt request bit

When executing the BBC or BBS instruction to determine an interrupt request bit immediately after this bit is set to "0", take the following sequence.

<Reason>

If the BBC or BBS instruction is executed immediately after an interrupt request bit is cleared to "0", the value of the interrupt request bit before being cleared to "0" is read.

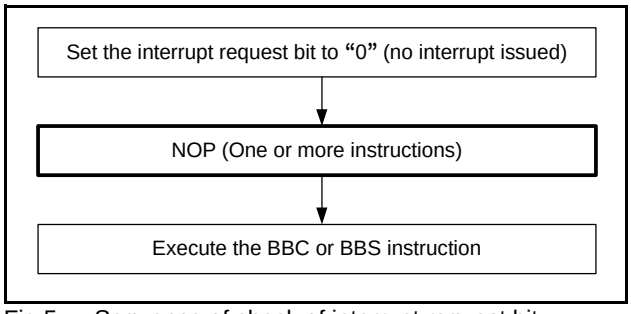


Fig 5. Sequence of check of interrupt request bit

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Notes on Timers

1. When n (0 to 255) is written to a timer latch, the frequency division ratio is 1/(n+1).
2. Timer count source
   Stop timer 2, timer 3 counting to change its count source.
3. Timer 1, timer 2, timer 3 count start timing and count time when operation starts
   Time to first underflow is different from time among next underflow by the timing to start the timer and count source operations after count starts.
4. Timer 2, timer 3, carrier wave generating circuit
   The timing adjustment of the output waveform causes the gap between the timer count value and the output waveform, and the output waveform changes in the reload cycle after the timer underflow.
   Moreover, the timer interrupt occurs at the change point of the output waveform.
   (The timing of the interrupt occurrence is behind a half cycle of the count source, compared with timer 1.)

Notes on Watchdog Timer

1. The watchdog timer is operating during the wait mode. Write data to the watchdog timer control register to prevent timer underflow.
2. The watchdog timer stops during the stop mode. However, the watchdog timer is running during the oscillation stabilizing time after the STP instruction is released. In order to avoid the underflow of the watchdog timer, the watchdog timer H count source selection bit (bit 7 of watchdog timer control register (address 39_{16})) must be set to "0" just before executing the STP instruction.

Notes on $\overline{\text{RESET}}$ Pin

(1) Connecting capacitor

In case where the $\overline{\text{RESET}}$ signal rise time is long, connect a ceramic capacitor or others across the $\overline{\text{RESET}}$ pin and the Vss pin.
And use a 1000 pF or more capacitor for high frequency use.
When connecting the capacitor, note the following:

- Make the length of the wiring which is connected to a capacitor as short as possible.
- Be sure to verify the operation of application products on the user side.

<Reason>
If the several nanosecond or several ten nanosecond impulse noise enters the $\overline{\text{RESET}}$ pin, it may cause a microcomputer failure.

Notes on Power-on Reset Circuit

Reset occurs by the power-on reset circuit under the following conditions;

- when the power source voltage rises from 0 V to 1.8 V within 1 ms.
  Also, note that reset may not occur under the following conditions;
- when the power source voltage rises from the voltage higher than 0 V.
- when it takes longer than 1 ms that the power source voltage rises from 0 V to 1.8 V.

Note on Voltage Drop Detection Circuit

The voltage drop detection circuit detection voltage of this product is set up lower than the minimum value of the supply voltage of the recommended operating conditions.
When the supply voltage of a microcomputer falls below to the minimum value of recommended operating conditions and regoes up (ex. battery exchange of an application product), depending on the capacity value of the bypass capacitor added to the power supply pin, the following case may cause program failure;
supply voltage does not fall below to V_{DET}, and its voltage re-goes up with no reset.
In such a case, please design a system which supply voltage is once reduced below to V_{DET} and re-goes up after that.

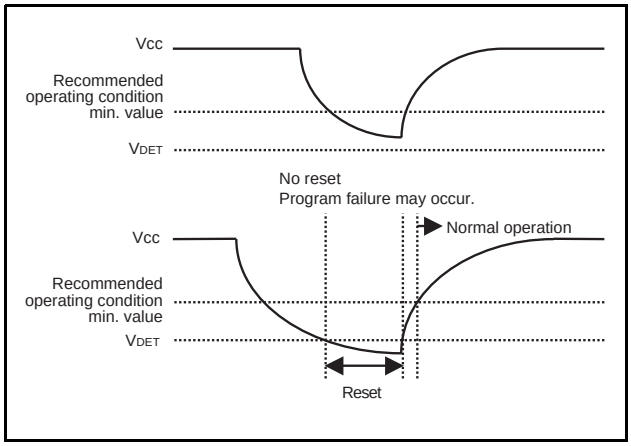


Fig 6. V_{CC} and V_{DET}

Notes on Clock Generating Circuit

(1) CPU mode register

Processor mode bits (bits 1 and 0) of CPU mode register (address $3B_{16}$) is used to control operation modes of the microcomputer. In order to prevent the dead-lock by erroneously writing (ex. program run-away), these bits can be rewritten only once after releasing reset.
After rewriting, it is disabled to write any data to the bit. (The emulator MCU "M37545RLSS" is excluded.)
Also, when the read-modify-write instructions (SEB, CLB, etc.) are executed to bits 2, 6, 7, bits 1 and 0 are locked.

(2) Ceramic resonator

When the ceramic resonator/quartz-crystal oscillation is used for the main clock, connect the ceramic resonator and the external circuit to pins X_{IN} and X_{OUT} at the shortest distance. A feedback resistor is built-in.

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Notes on Oscillation Control

1. Stop mode

(1) When the stop mode is used, set "1" (STP instruction enabled) to the STP instruction function selection bit (bit 1 of Function set ROM data (address FFDA16)).

(2) The oscillation stabilizing time after release of STP instruction can be selected from "set automatically"/"not set automatically" by the oscillation stabilizing time set bit after release of the STP instruction (bit 0 of MISRG (address 3816)). When "0" is set to this bit, "0316" is set to timer 1 and "FF16" is set to prescaler 1 automatically at the execution of the STP instruction. When "1" is set to this bit, set the wait time to timer 1 and prescaler 1 according to the oscillation stabilizing time of the oscillation. Also, when timer 1 is used, set values again to timer 1 and prescaler 1 after system is returned from the stop mode.

Note on Power Source Voltage

When the power source voltage value of a microcomputer is less than the value which is indicated as the recommended operating conditions, the microcomputer does not operate normally and may perform unstable operation.
In a system where the power source voltage drops slowly when the power source voltage drops or the power supply is turned off, reset a microcomputer when the supply voltage is less than the recommended operating conditions and design a system not to cause errors to the system by this unstable operation.

NOTES ON HARDWARE

Handling of Power Source Pin

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (VCC pin, VDDR pin) and GND pin (VSS pin). Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, a ceramic capacitor of 0.1 µF is recommended.

Handling of CNVss Pin

The CNVSS pin is connected to the internal memory circuit block by a low-ohmic resistance, since it has the multiplexed function to be a programmable power source pin (VPP pin) as well.
To improve the noise reduction, make the length of wiring between the CNVSS pin and the VSS pin the shortest possible.

Notes on QzROM

1. Note on Product shipped in blank

As for the product shipped in blank, Renesas does not perform the writing test to user ROM area after the assembly process though the QzROM writing test is performed enough before the assembly process. Therefore, a writing error of approx.0.1 % may occur.
Moreover, please note the contact of cables and foreign bodies on a socket, etc. because a writing environment may cause some writing errors.

2. Precautions Regarding Overvoltage

Make sure that voltage exceeding the VCC pin voltage is not applied to other pins. In particular, ensure that the state indicated by bold lines in Figure below does not occur for pin CNVSS (VPP power source pin for QzROM) during power-on or power-off. Otherwise the contents of QzROM could be rewritten.

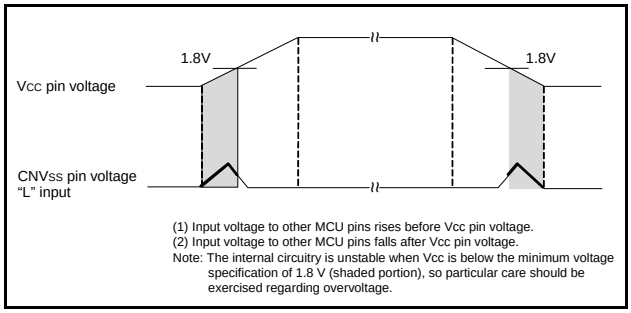


Fig 7. Timing Diagram (bold-lined periods are applicable)

3. QzROM Writing Orders

When ordering the QzROM product shipped after writing, submit the mask file (extension: .mask) which is made by the mask file converter MM.
Be sure to set the ROM option ("MASK option" written in the mask file converter) setup when making the mask file by using the mask file converter MM.

- Be sure to set the ROM option data* setup when making the mask file by using the mask file converter MM.. The ROM code protect is specified according to the ROM option data* in the mask file which is submitted at ordering. Note that the mask file which has nothing at the ROM option data* or has the data other than "0016" and "FF16" can not be accepted.
- Set "FF16" to the ROM code protect address in ROM data regardless of the presence or absence of a protect. When data other than "FF16" is set, we may ask that the ROM data be submitted again.

* ROM option data: mask option noted in MM

4. Data Required for QzROM Writing Orders

The following are necessary when ordering a QzROM product shipped after writing:
1. QzROM Writing Confirmation Form*
2. Mark Specification Form*
3. ROM data.....Mask file

* For the QzROM writing confirmation form and the mark specification form, refer to the "Renesas Technology Corp." Homepage (http://www.renesas.com/homepage.jsp).
Note that we cannot deal with special font marking (customer's trademark etc.) in QzROM microcomputer.

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REVISION HISTORY	7545 Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Feb. 07, 2005	–	First edition issued
1.01	May. 10, 2005	20	Fig.22 : Carrier wave auto-control bit; “1” and “0” added.
		26	Standard operation of watchdog timer and Operation of STP instruction disable bit: address FFFA16 → address FFDA16 Note on Watchdog Timer 2: ... set to “1” just before ... → ... set to “0” just before ...
		28	Voltage Drop Detection Circuit: address FFFA16 → address FFDA16
		33	State transition deleted
		36	Fig. 51 partly revised
		40	Table 9: RPL; V → kΩ
		42	Fig. 55: CNTR0 → INT0
		47	Notes on Watchdog timer: ... set to “1” just before ... → ... set to “0” just before ... Notes on Clock Generating Circuit 1: bits 2 to 4 to 7 → bits 2, 6, 7
1.02	Jul. 20, 2005	All pages	ROM option → Function set ROM
		3	Table 1: added.
		11	ROM Code Protect Address (address FFDB16) added.
		16	Termination of unused pins added.
		35	[ROM option data] ROMOP → [Function set ROM] FSROM Fig. 42, 43: partly revised.
		37	(4) Wiring to CNVSS pin → (4) Wiring to VPP pin
		51	DATA REQUIRED FOR QzROM WRITING ORDERS, Notes On QzROM Writing Orders, Notes On ROM Code Protect added.
1.03	Oct. 21, 2005	–	STP instruction disable bit → STP instruction function selection bit
		29	“Operation of STP instruction function selection bit” revised.
		30	Fig.33 Block diagram of watchdog timer and reset circuit “Count start (Watchdog timer disable bit (bit 0 of FSROM))” added.
		35	Function set ROM : Description revised. Fig.42: Reserved → Renesas shipment test area “When the checksum is included in the user program, avoid assigning it to these areas.” added to Note. Fig.43: Bit 0, bit 1 and bit 4 of FSROM revised.
1.04	May. 17, 2006	–	“PRELIMINARY” eliminated.
1.05	May. 18, 2006	6	Fig.4 “Under development” eliminated.
1.06	Feb. 29, 2008	1	Revised by additional new products (memory size)
		2	Fig. 2 is added
		3	Revised by additional new products (memory size and package)
		6	Fig. 5 is added
		8	Revised by additional new products (memory size, package, Fig. 6, and Table 4)
		12	Fig. 9 is revised
		13	Function set ROM Area and Notes (2) - (5) added Clock circuit is deleted from [Function set ROM data] FSROM Notes on use deleted
		14	Fig. 10 is revised
		16	Fig.12 added
		20 to 24	Interrupts is revised whole

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REVISION HISTORY	7545 Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.06	Feb. 29, 2008	34	Initial value of watchdog timer: Description added Operation of STP instruction function selection bit deleted STP instruction function selection bit added
		35	Fig. 35 is revised
		38	Fig. 42 is revised
		40	Function set ROM is moved to Memory (page 13)
		40 to 44	QzROM Writing Mode is added
		45	Notes on Hardware is added
		46	(4) Wiring to V_{PP} pin: "V_{PP}" → "CNV_{SS}" Fig.52 is revised
		52	Symbol of Feed-back resistor value between X_{IN}-X_{OUT} is revised
		55	PLSP0032JB-A package is added.
		56	Fig.2, 4, and BRK instruction deleted
		57	Modifying output data with bit managing instruction is revised
		59	Notes on Watchdog Timer: 3. is added
		60	Notes on Oscillation Control is revised ("0" → "1") Precautions Regarding Overvoltage is added
1.07	Mar 19, 2009	8	Fig.6 "Under development" deleted Table 4 M37545GCKP and M37545GFKP deleted
		41	Fig. 44 and Fig.45 RESET→$\overline{\text{RESET}}$
		44	"Processor Status Register" revised
		49	"Notes on QzROM" added
		56	"1. Initializing of processor status register" revised / Figure title of Fig.3 revised
		60	"Notes On QzROM Writing Orders" is revised "Precautions Regarding Overvoltage" revised: CNV_{SS} power source pin for QzROM→V_{PP} power source pin for QzROM

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