



PSMN6R1-40HL

N-channel 40 V, 7.2 mOhm, logic level MOSFET in LPAK56D using TrenchMOS technology

30 September 2022

Product data sheet

1. General description

Dual logic level N-channel MOSFET in an LPAK56D (Dual Power-SO8) package using TrenchMOS technology.

2. Features and benefits

- Dual MOSFET
- Repetitive avalanche rated
- High reliability LPAK56D package
- Copper-clip, solder die attach
- Qualified to 175 °C

3. Applications

- Brushless DC motor control
- DC-to-DC converters
- High-performance synchronous rectification
- High performance and high efficiency server power supply

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	-	40	V
I _D	drain current	V _{GS} = 5 V; T _{mb} = 25 °C; Fig. 2	[1]	-	-	40	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	-	64	W
T _j	junction temperature			-55	-	175	°C
Static characteristics FET1 and FET2							
R _{DSon}	drain-source on-state resistance	V _{GS} = 5 V; I _D = 10 A; T _j = 25 °C; Fig. 11		-	6	7.2	mΩ
		V _{GS} = 5 V; I _D = 10 A; T _j = 175 °C; Fig. 11		-	12.1	14.5	mΩ
Dynamic characteristics FET1 and FET2							
Q _{GD}	gate-drain charge	I _D = 10 A; V _{DS} = 32 V; V _{GS} = 5 V; T _j = 25 °C; Fig. 13 ; Fig. 14		-	6.8	-	nC
Q _{G(tot)}	total gate charge			-	22.2	-	nC
Avalanche ruggedness FET1 and FET2							
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 40 A; V _{sup} ≤ 40 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; Fig. 4	[2] [3]	-	-	125	mJ

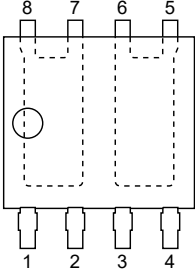
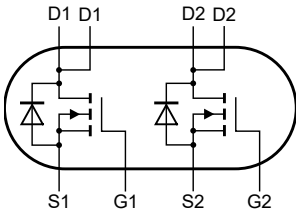
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode FET1 and FET2						
Q _r	recovered charge	I _S = 10 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 20 V; T _J = 25 °C	-	18	-	nC

- [1] Continuous current is limited by package.
- [2] Refer to application note AN10273 for further information
- [3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 LFPAK56D; Dual LFPAK (SOT1205)	 mbk725
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN6R1-40HL	LFPAK56D; Dual LFPAK	plastic, single ended surface mounted package (LFPAK56D); 8 leads	SOT1205

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN6R1-40HL	6R1L40H

8. Limiting values

Table 5. Limiting values

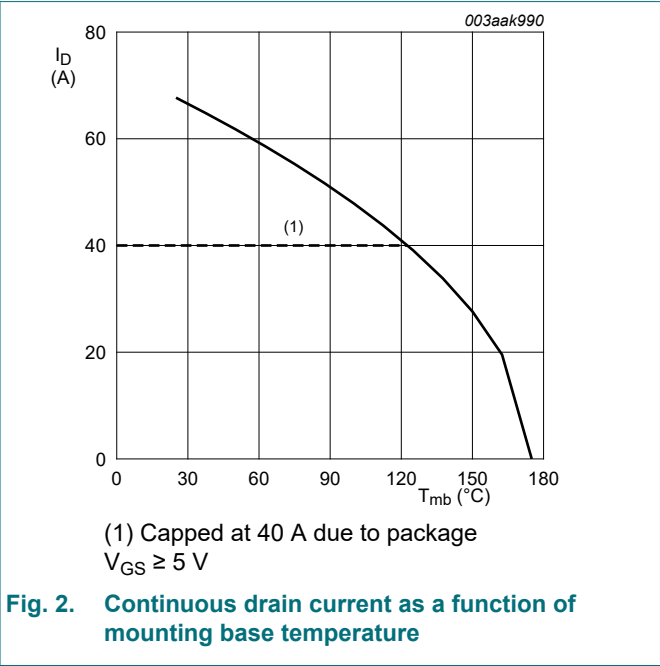
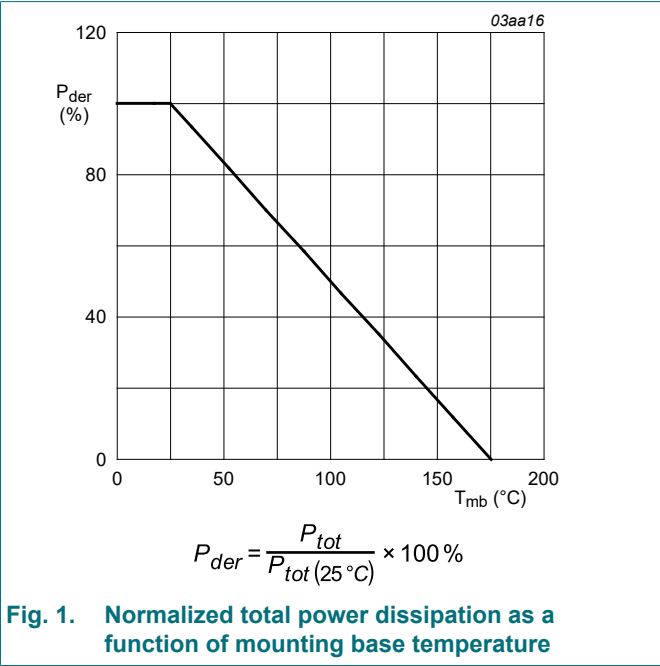
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _J ≤ 175 °C	-	40	V
V _{DGR}	drain-gate voltage	R _{GS} = 20 kΩ	-	40	V
V _{GS}	gate-source voltage	Pulsed; T _J ≤ 175 °C	[1] [2] -15	15	V
		DC; T _J ≤ 175 °C	-10	10	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1	-	64	W

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Symbol	Parameter	Conditions		Min	Max	Unit
I _D	drain current	V _{GS} = 5 V; T _{mb} = 25 °C; Fig. 2	[3]	-	40	A
		V _{GS} = 5 V; T _{mb} = 100 °C; Fig. 2	[3]	-	40	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3		-	265	A
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
Source-drain diode FET1 and FET2						
I _S	source current	T _{mb} = 25 °C	[3]	-	40	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	265	A
Avalanche ruggedness FET1 and FET2						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 40 A; V _{sup} ≤ 40 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; Fig. 4	[4] [5]	-	125	mJ

- [1] Accumulated Pulse duration up to 50 hours delivers zero defect ppm
- [2] Significantly longer life times are achieved by lowering T_j and or V_{GS}.
- [3] Continuous current is limited by package.
- [4] Refer to application note AN10273 for further information
- [5] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C



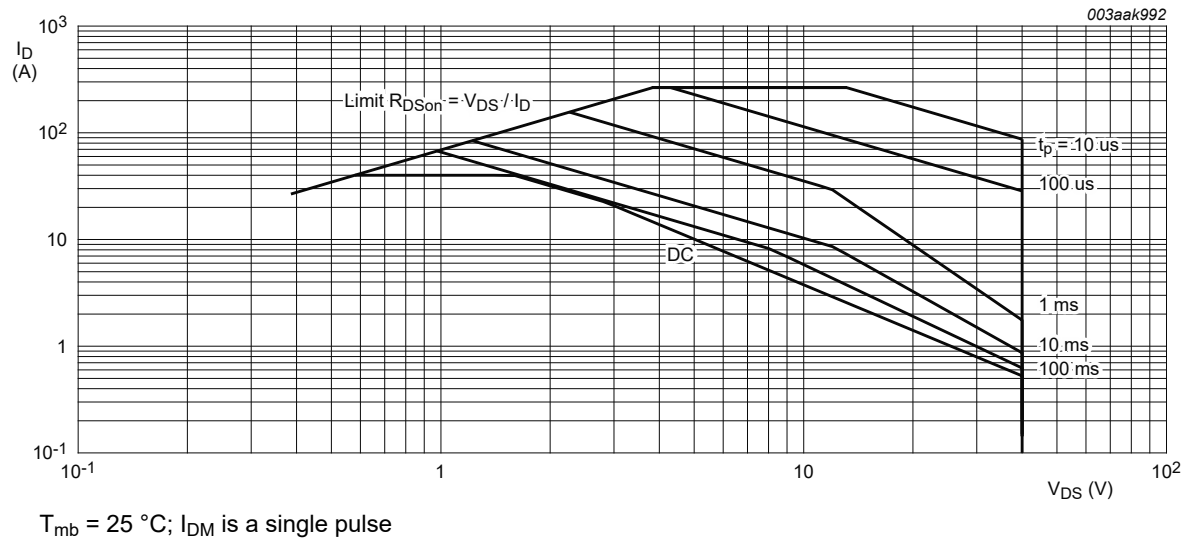
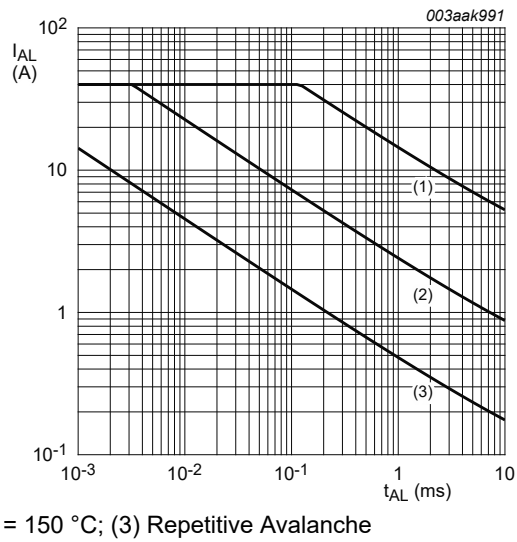


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



(1) $T_{j\ (init)} = 25^\circ\text{C}$; (2) $T_{j\ (init)} = 150^\circ\text{C}$; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	-	2.36	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	95	-	K/W

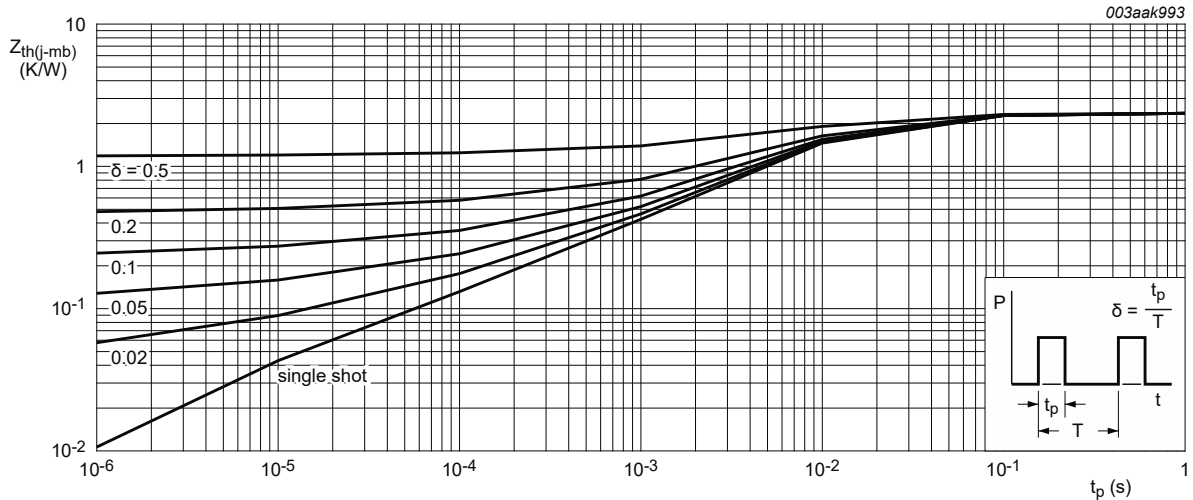


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

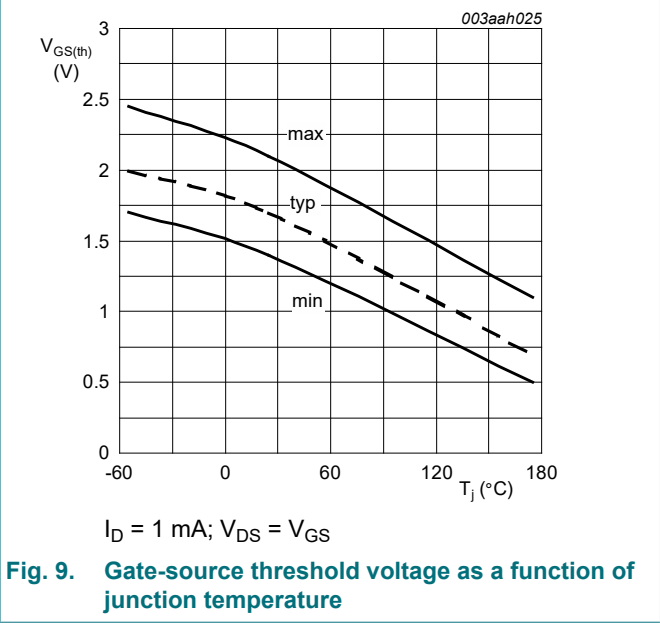
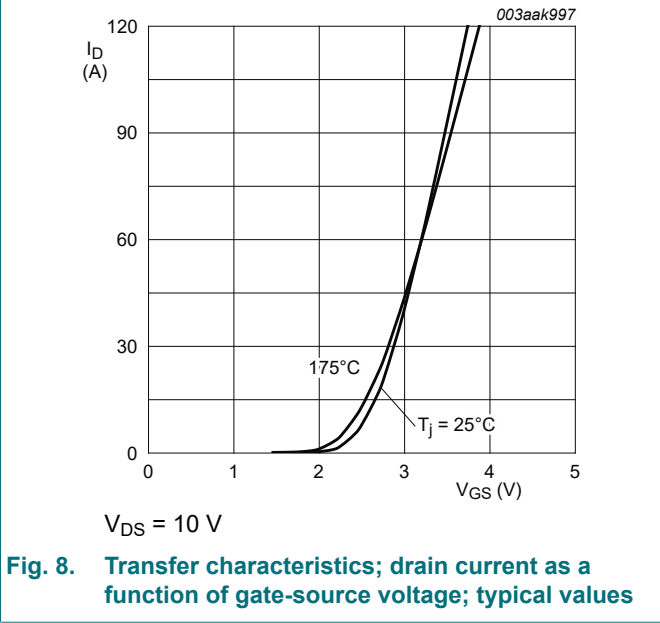
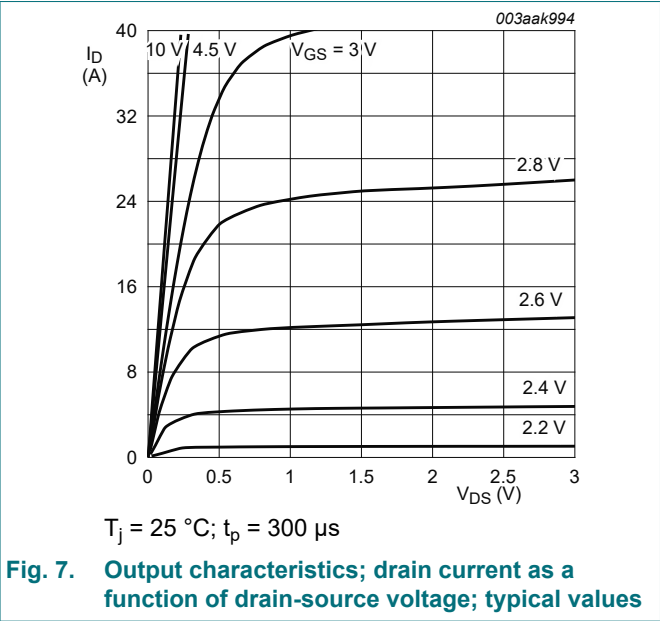
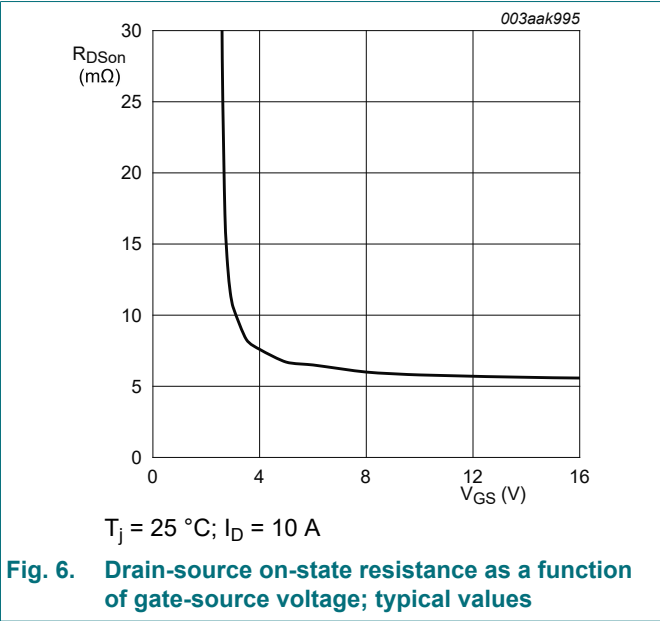
10. Characteristics

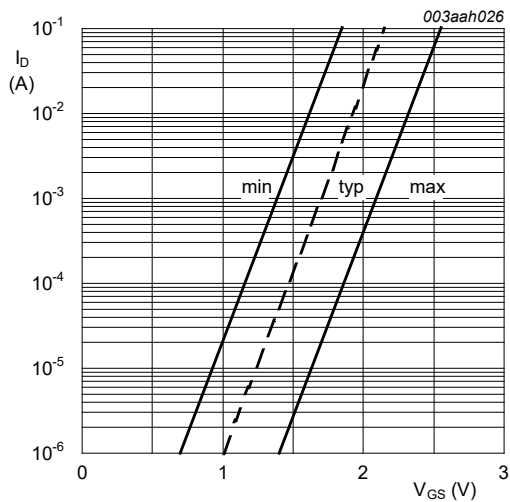
Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics FET1 and FET2							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = -55 °C		36	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C		40	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} =V _{GS} ; T _j = 25 °C; Fig. 9 ; Fig. 10		1.4	1.7	2.1	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _j = 175 °C; Fig. 9 ; Fig. 10		0.5	-	-	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _j = -55 °C; Fig. 9 ; Fig. 10		-	-	2.45	V
I _{DSS}	drain leakage current	V _{DS} = 40 V; V _{GS} = 0 V; T _j = 175 °C		-	-	500	μA
		V _{DS} = 40 V; V _{GS} = 0 V; T _j = 25 °C		-	0.02	1	μA
I _{GSS}	gate leakage current	V _{GS} = -10 V; V _{DS} = 0 V; T _j = 25 °C		-	2	100	nA
		V _{GS} = 10 V; V _{DS} = 0 V; T _j = 25 °C		-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 5 V; I _D = 10 A; T _j = 25 °C; Fig. 11		-	6	7.2	mΩ
		V _{GS} = 5 V; I _D = 10 A; T _j = 175 °C; Fig. 11		-	12.1	14.5	mΩ
		V _{GS} = 10 V; I _D = 10 A; T _j = 25 °C; Fig. 11 ; Fig. 12		-	5	6.1	mΩ
Dynamic characteristics FET1 and FET2							
Q _{G(tot)}	total gate charge	I _D = 10 A; V _{DS} = 32 V; V _{GS} = 5 V; T _j = 25 °C; Fig. 13 ; Fig. 14		-	22.2	-	nC
Q _{GS}	gate-source charge			-	5.2	-	nC
Q _{GD}	gate-drain charge			-	6.8	-	nC
C _{iss}	input capacitance	V _{DS} = 25 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; Fig. 15		-	2250	3000	pF
C _{oss}	output capacitance			-	305	366	pF
C _{rss}	reverse transfer capacitance			-	148	202	pF
t _{d(on)}	turn-on delay time	V _{DS} = 32 V; R _L = 3.2 Ω; V _{GS} = 5 V; R _{G(ext)} = 5 Ω; T _j = 25 °C		-	13	-	ns
t _r	rise time			-	22	-	ns

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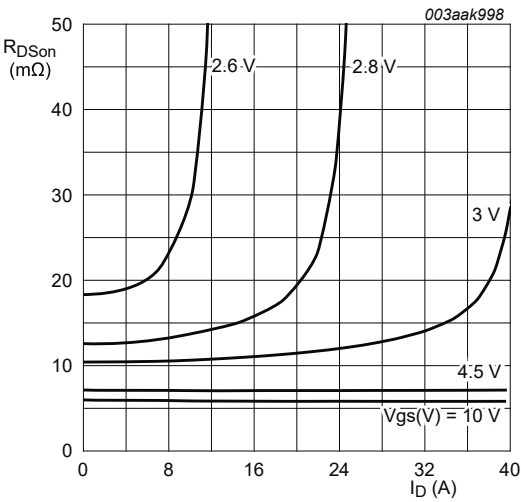
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t _{d(off)}	turn-off delay time			-	27	-	ns
t _f	fall time			-	20	-	ns
Source-drain diode FET1 and FET2							
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _J = 25 °C; Fig. 16		-	0.78	1.2	V
t _{rr}	reverse recovery time	I _S = 10 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 20 V; T _J = 25 °C		-	23	-	ns
Q _r	recovered charge			-	18	-	nC





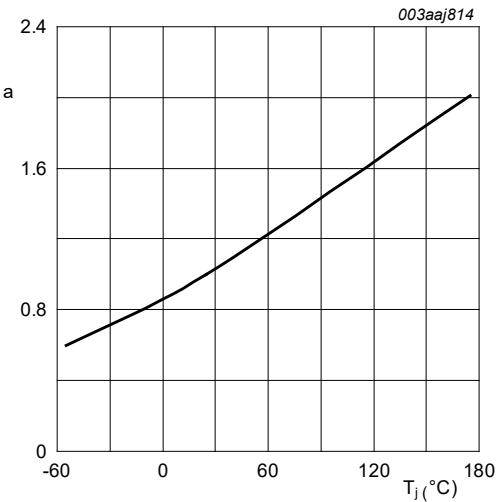
Tj = 25 °C; VDS = 5 V

Fig. 10. Sub-threshold drain current as a function of gate-source voltage



Tj = 25 °C; tp = 300 μs

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}\text{C})}$$

Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

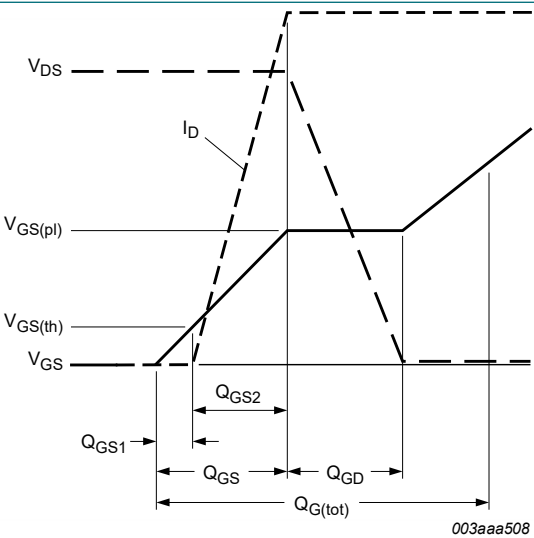
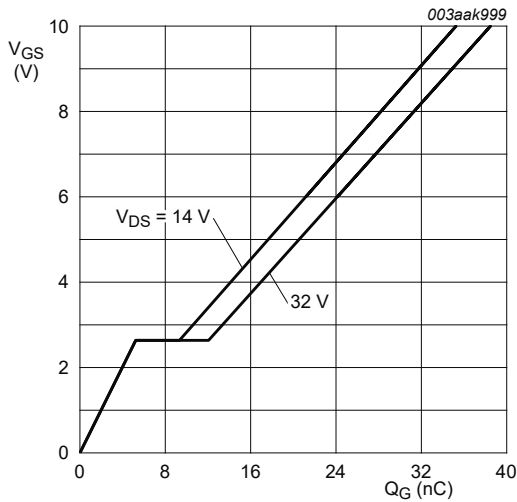
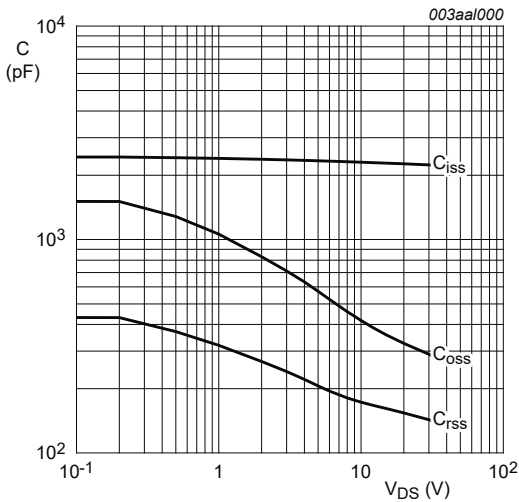


Fig. 13. Gate charge waveform definitions



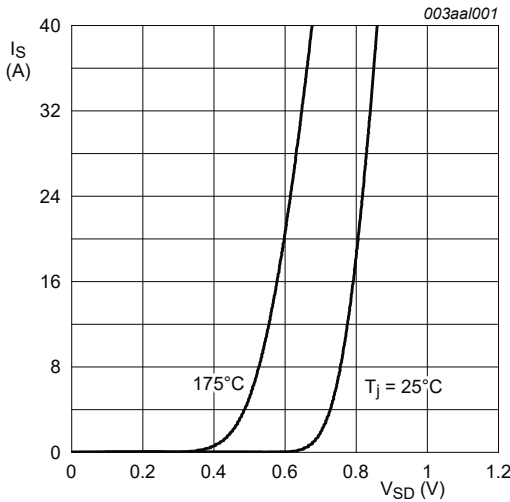
$T_j = 25\text{ }^{\circ}\text{C}$; $I_D = 10\text{ A}$

Fig. 14. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0\text{ V}$

Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

11. Package outline

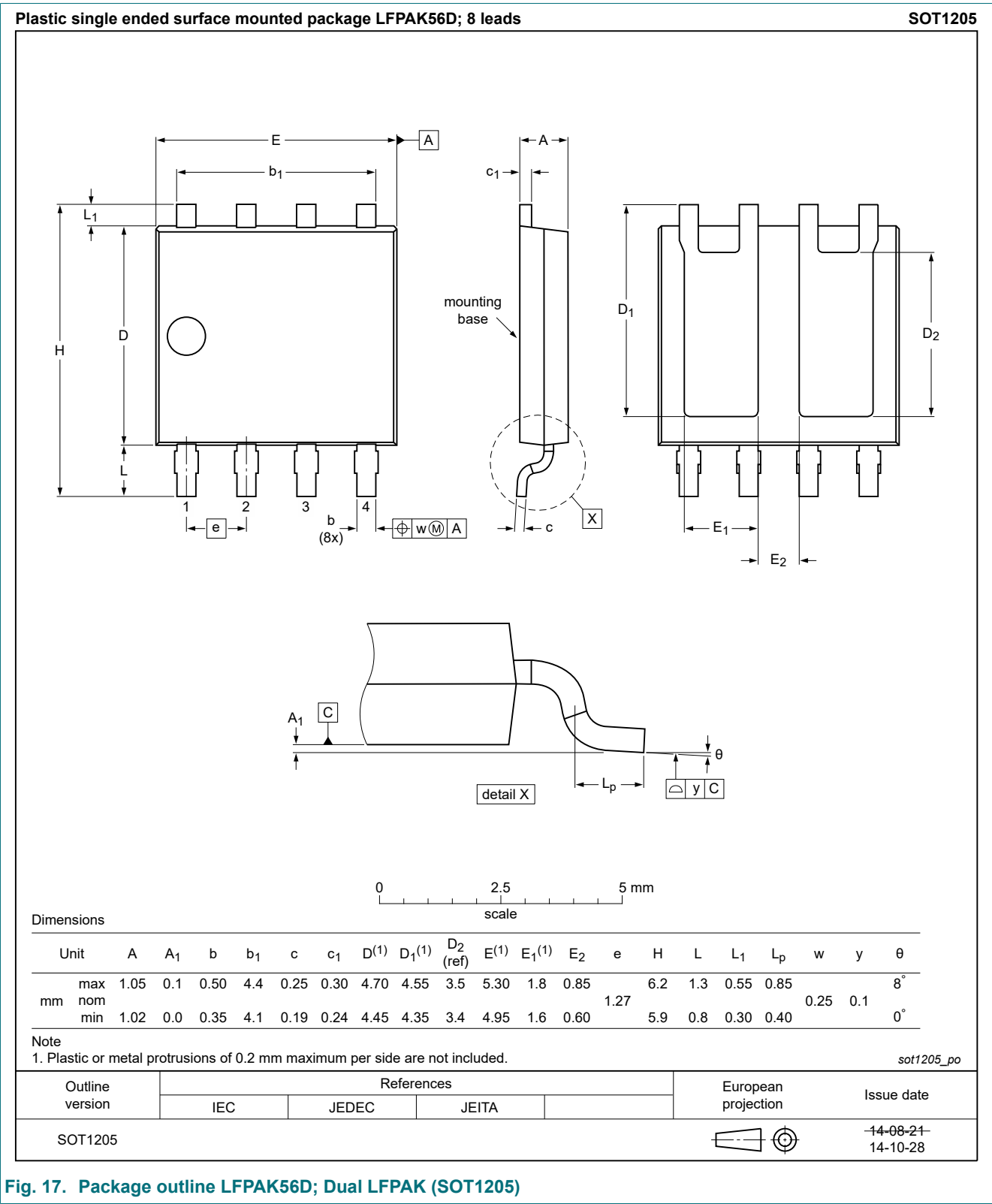


Fig. 17. Package outline LPAK56D; Dual LPAK (SOT1205)

12. Soldering

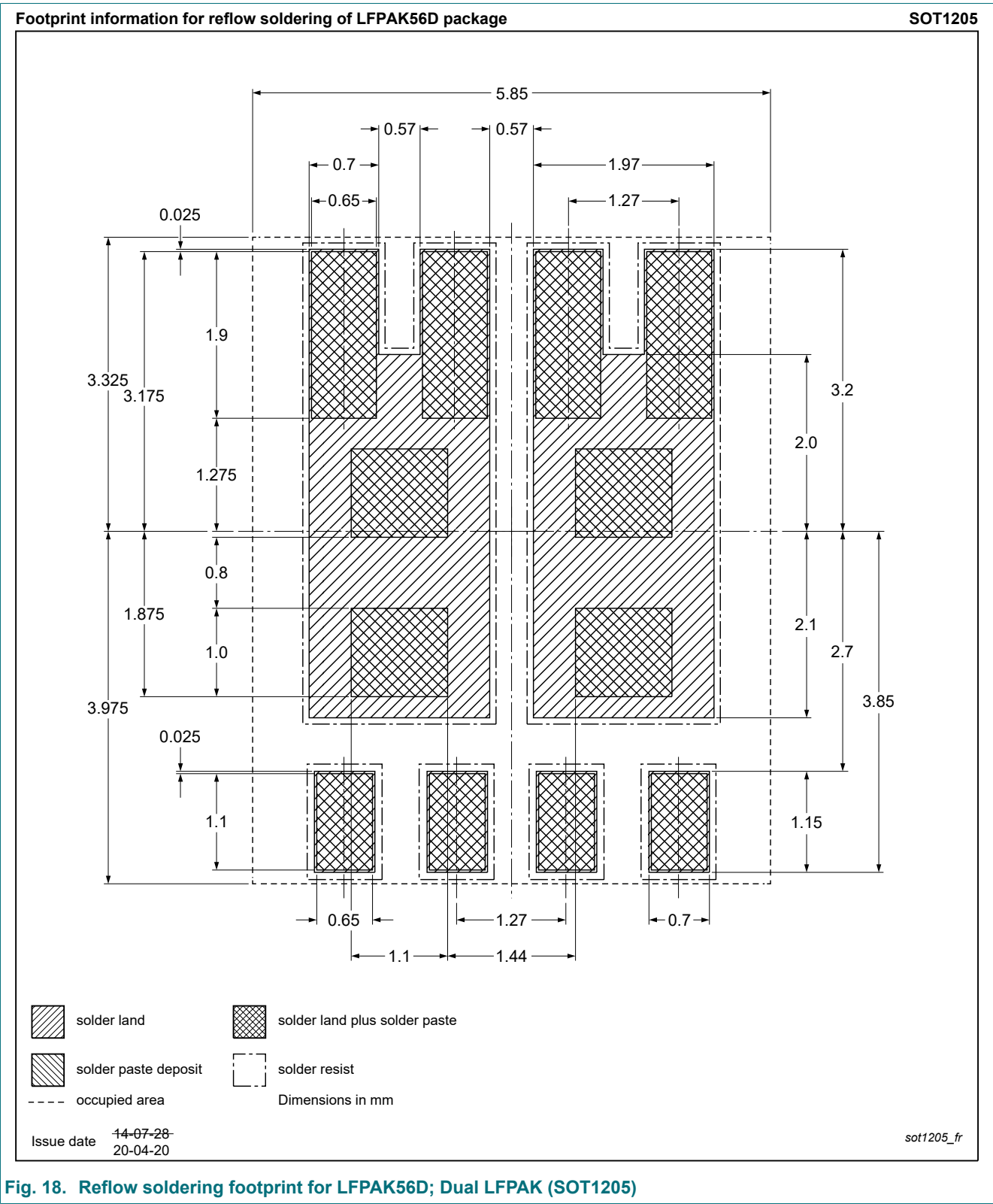


Fig. 18. Reflow soldering footprint for LPAK56D; Dual LPAK (SOT1205)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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