

TC74AC273P, TC74AC273F, TC74AC273FT

Octal D-Type Flip Flop with Clear

The TC74AC273 is an advanced high speed CMOS OCTAL D-TYPE FLIP FLOP fabricated with silicon gate and double-layer metal wiring C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

Information signals applied to D inputs are transferred to the Q output on the positive going edge of the clock pulse.

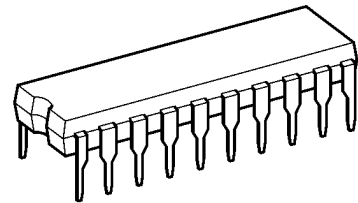
When the CLR input is held "L", the Q outputs are at a low logic level independent of the other inputs.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

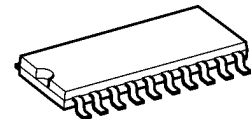
- High speed: $f_{\max} = 170 \text{ MHz}$ (typ.) at $V_{CC} = 5 \text{ V}$
- Low power dissipation: $I_{CC} = 8 \mu\text{A}$ (max) at $T_a = 25^\circ\text{C}$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (min)
- Symmetrical output impedance:
 $|I_{OH}| = I_{OL} = 24 \text{ mA}$ (min) Capability of driving 50Ω transmission lines.
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range: $V_{CC} (\text{opr}) = 2 \text{ V}$ to 5.5 V
- Pin and function compatible with 74F273

TC74AC273P



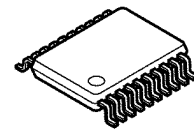
DIP20-P-300-2.54A

TC74AC273F



SOP20-P-300-1.27A

TC74AC273FT



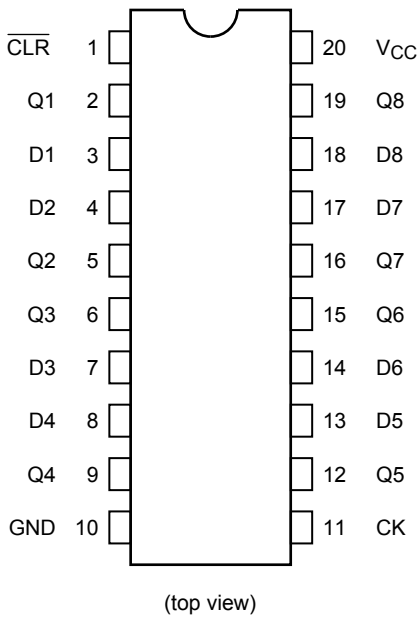
TSSOP20-P-0044-0.65A

Weight

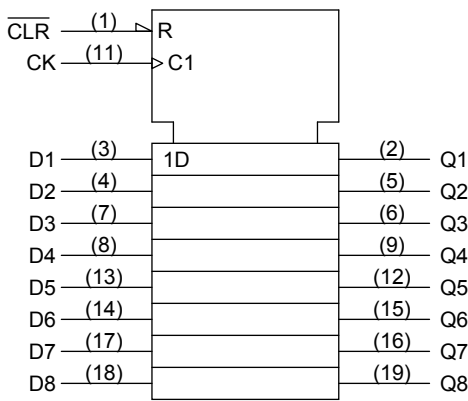
DIP20-P-300-2.54A	: 1.30 g (typ.)
SOP20-P-300-1.27A	: 0.22 g (typ.)
TSSOP20-P-0044-0.65A	: 0.08 g (typ.)

Start of commercial production
1988-05

Pin Assignment



IEC Logic Symbol

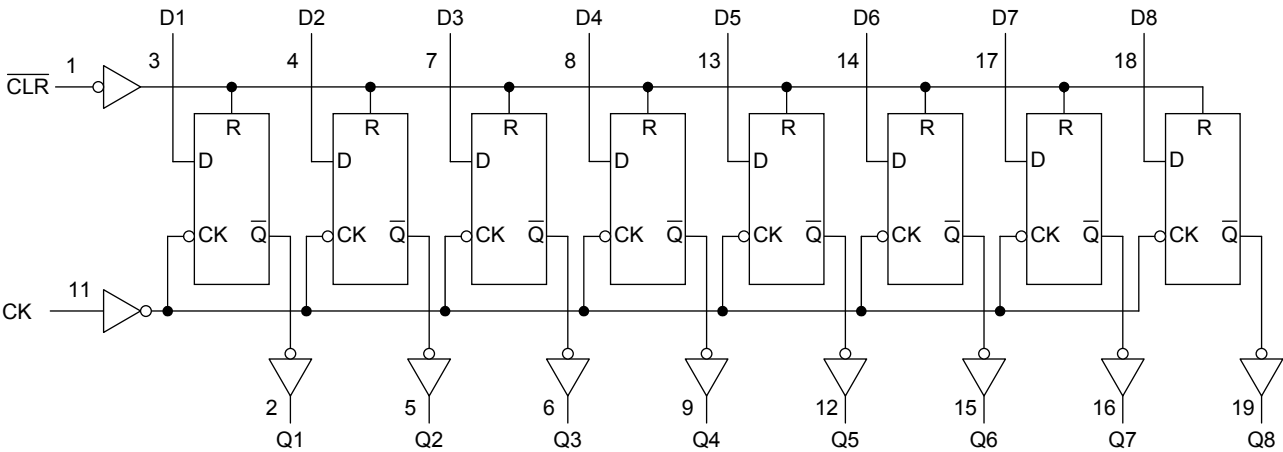


Truth Table

Inputs			Output	Function
CLR	D	CK	Q	
L	X	X	L	Clear
H	L		L	—
H	H		H	—
H	X		Q _n	No Change

X: Don't care

System Diagram



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
DC input voltage	V_{IN}	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}	± 20	mA
Output diode current	I_{OK}	± 50	mA
DC output current	I_{OUT}	± 50	mA
DC V_{CC} /ground current	I_{CC}	± 200	mA
Power dissipation	P_D	500 (DIP) (Note 2)/180 (SOP/TSSOP)	mW
Storage temperature	T_{stg}	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 2: 500 mW in the range of $T_a = -40$ to 65°C . From $T_a = 65$ to 85°C , a derating factor of $-10\text{ mW}/^\circ\text{C}$ should be applied up to 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 5.5	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	°C
Input rise and fall time	dt/dV	0 to 100 ($V_{CC} = 3.3 \pm 0.3\text{ V}$) 0 to 20 ($V_{CC} = 5 \pm 0.5\text{ V}$)	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C				Ta = −40 to 85°C		Unit
				V _{CC} (V)	Min	Typ.	Max	Min	Max	
High-level input voltage	V _{IH}	—		2.0 3.0 5.5	1.50 2.10 3.85	— — —	— — —	1.50 2.10 3.85	— — —	V
Low-level input voltage	V _{IL}	—		2.0 3.0 5.5	— — —	— — —	0.50 0.90 1.65	— — —	0.50 0.90 1.65	V
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = −50 μA	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
			I _{OH} = −4 mA I _{OH} = −24 mA I _{OH} = −75 mA (Note)	3.0	2.58	—	—	2.48	—	
				4.5	3.94	—	—	3.80	—	
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 μA	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
			I _{OL} = 12 mA I _{OL} = 24 mA I _{OL} = 75 mA (Note)	3.0	—	—	0.36	—	0.44	
				4.5	—	—	0.36	—	0.44	
Input leakage current	I _{IN}	V _{IN} = V _{CC} or GND		5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND		5.5	—	—	8.0	—	80.0	μA

Note: This spec indicates the capability of driving 50 Ω transmission lines.
One output should be tested at a time for a 10 ms maximum duration.

Timing Requirements (input: t_r = t_f = 3 ns)

Characteristics	Symbol	Test Condition		Ta = 25°C	Ta = -40 to 85°C	Unit
				V _{CC} (V)	Limit	
Minimum pulse width (CK)	t _w (L)	—	—	3.3 ± 0.3	8.0	ns
	t _w (H)			5.0 ± 0.5	5.0	
Minimum pulse width ($\overline{\text{CLR}}$)	t _w (L)	—	—	3.3 ± 0.3	7.5	ns
				5.0 ± 0.5	5.0	
Minimum set-up time	t _s	—	—	3.3 ± 0.3	8.5	ns
				5.0 ± 0.5	4.5	
Minimum hold time	t _h	—	—	3.3 ± 0.3	0.0	ns
				5.0 ± 0.5	0.0	
Minimum removal time ($\overline{\text{CLR}}$)	t _{rem}	—	—	3.3 ± 0.3	7.0	ns
				5.0 ± 0.5	3.5	

AC Characteristics ($C_L = 50 \text{ pF}$, $R_L = 500 \Omega$, input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit
			V _{CC} (V)	Min	Typ.	Max	Min	Max	
Propagation delay time (CK-Q)	t _{pLH} t _{pHL}	—	3.3 ± 0.3 5.0 ± 0.5	— —	9.0 6.5	15.8 9.6	1.0 1.0	18.0 11.0	ns
Propagation delay time ($\overline{\text{CLR}}$ -Q)	t _{pHL}	—	3.3 ± 0.3 5.0 ± 0.5	— —	8.0 5.9	14.0 9.2	1.0 1.0	16.0 10.5	ns
Maximum clock frequency	f _{max}	—	3.3 ± 0.3 5.0 ± 0.5	55 90	110 150	— —	55 90	— —	MHz
Input capacitance	C _{IN}	—		—	5	10	—	10	pF
Power dissipation capacitance	C _{PD}	(Note)		—	40	—	—	—	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(\text{opr})} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per F/F)}$$

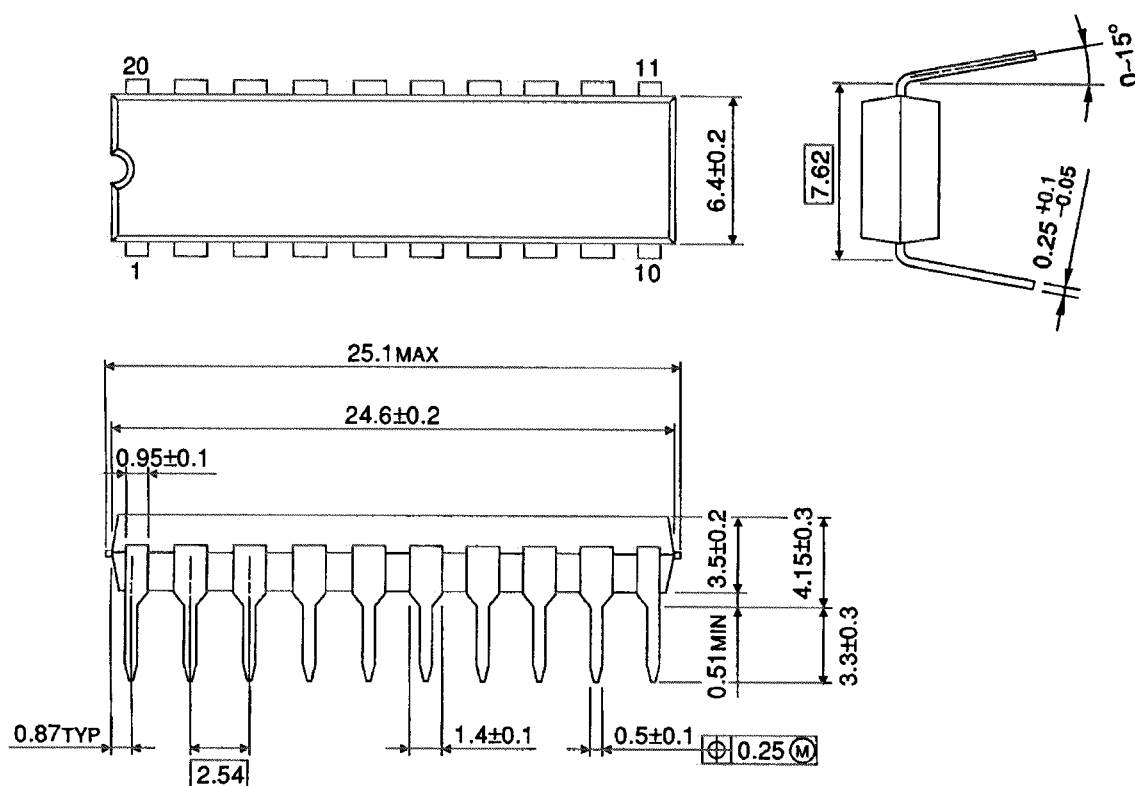
And the total C_{PD} when n pcs. of flip flop operate can be gained by the following equation:

$$C_{PD(\text{total})} = 29 + 11 \cdot n$$

Package Dimensions

DIP20-P-300-2.54A

Unit : mm

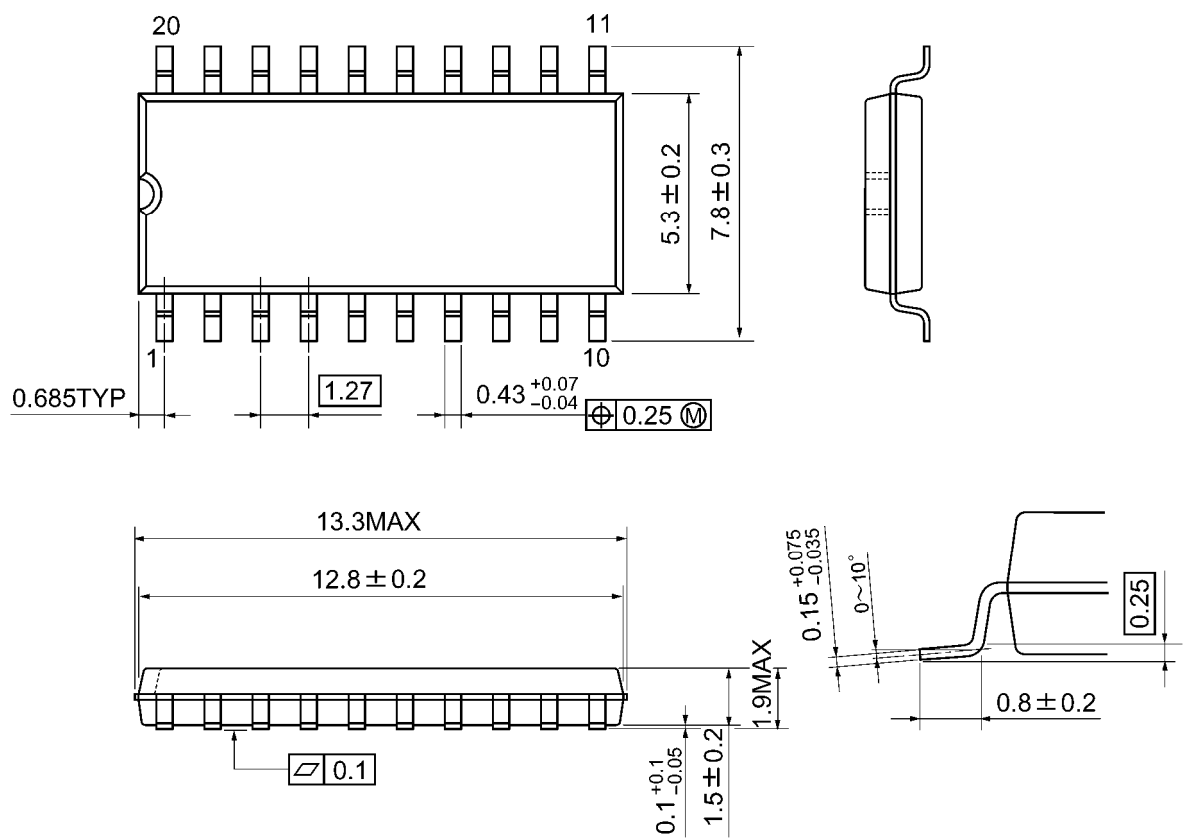


Weight: 1.30 g (typ.)

Package Dimensions

SOP20-P-300-1.27A

Unit: mm

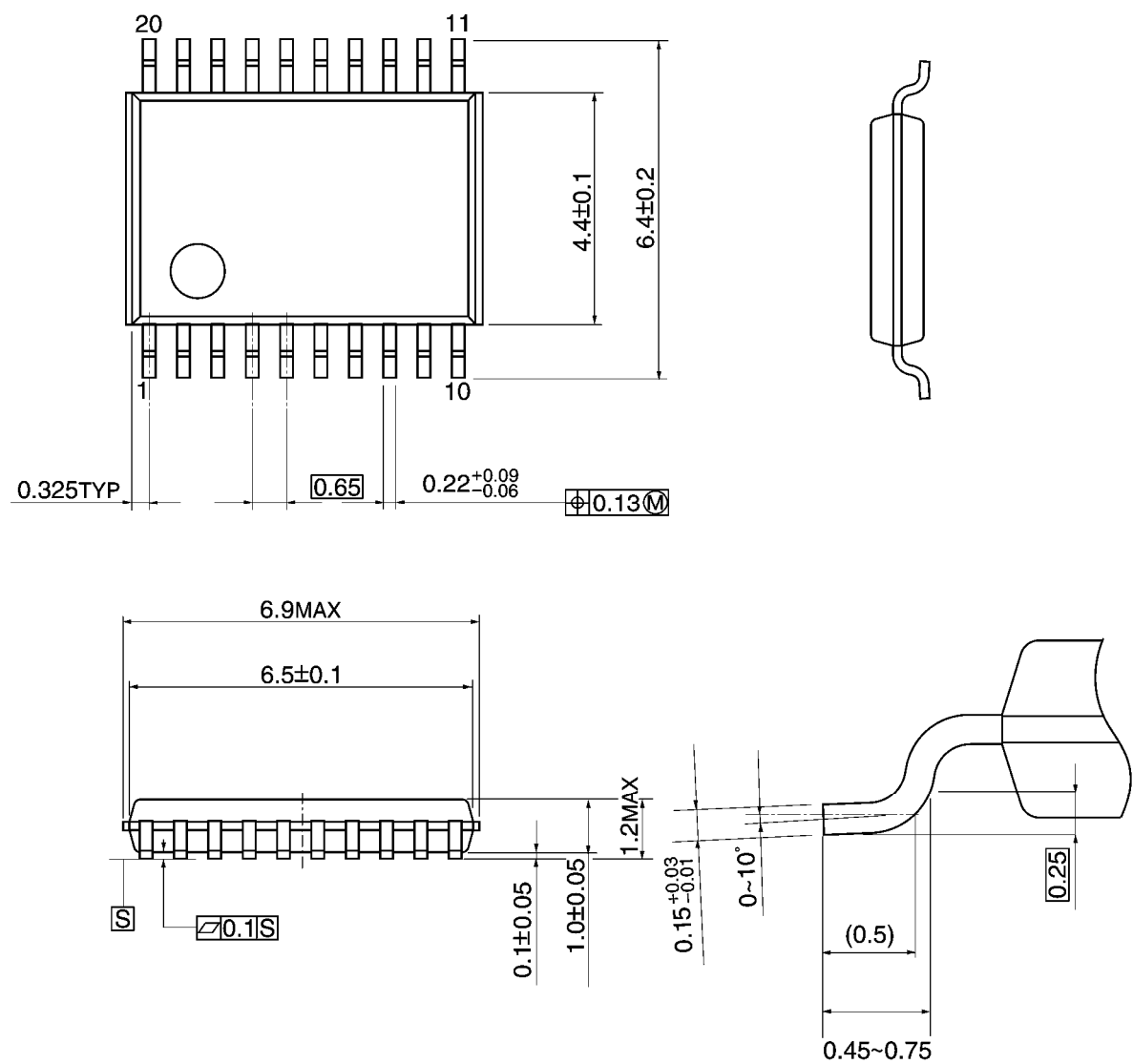


Weight: 0.22 g (typ.)

Package Dimensions

TSSOP20-P-0044-0.65A

Unit: mm



Weight: 0.08 g (typ.)

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