CY7B991V

3.3 V RoboClock® Low Voltage Programmable Skew Clock Buffer

Features

- All output pair skew <100 ps typical (250 ps max)
- 3.75 MHz to 80 MHz output operation
- User-selectable output functions:
  - Selectable skew up to 18 ns
  - Inverted and non-inverted
  - Operation at one-half and one-quarter input frequency
  - Operation at 2 × and 4 × input frequency (input as low as 3.75 MHz)
- Zero input to output delay
- 50% duty cycle outputs
- Low-voltage transistor-transistor logic (LVTTL) outputs drive 50 Ω terminated lines
- Operates from a single 3.3 V supply
- Low operating current
- 32-pin plastic leaded chip carrier (PLCC) package
- Low cycle-to-cycle jitter (100 ps typical)

Functional Description

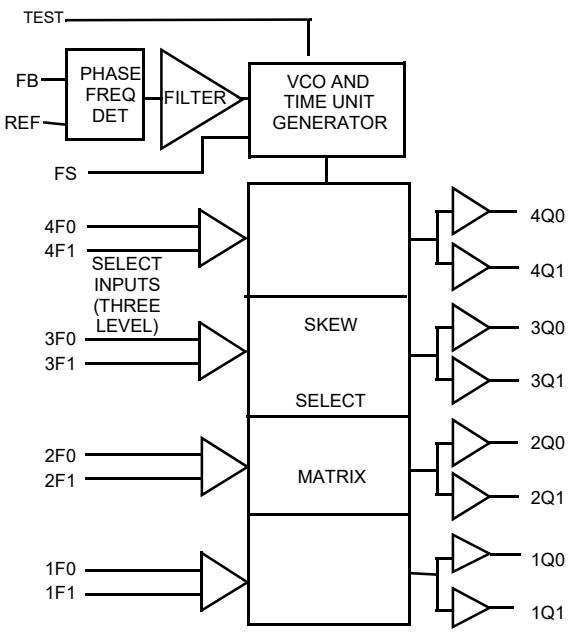
The CY7B991V 3.3 V RoboClock® low-voltage programmable skew clock buffer (LVPSCB) offers user-selectable control over system clock functions. These multiple output clock drivers provide the system integrator with functions necessary to optimize the timing of high-performance computer systems. Each of the eight individual drivers – arranged in four pairs of user controllable outputs – can drive terminated transmission lines with impedances as low as 50 Ω. This delivers minimal output skews and full-swing logic levels (LVTTL).

Each output is hardwired to one of nine delay or function configurations. Delay increments of 0.7 to 1.5 ns are determined by the operating frequency, with outputs able to skew up to ±6 time units from their nominal ‘zero’ skew position. The completely-integrated phase-locked loop (PLL) allows external load and transmission line delay effects to be canceled. When this ‘zero delay’ capability of the LVPSCB is combined with the selectable output skew functions, the user can create output-to-output delays of up to ±12 time units.

Divide-by-two and divide-by-four output functions are provided for additional flexibility in designing complex clock systems. When combined with the internal PLL, these divide functions enable distribution of a low frequency clock that is multiplied by two or four at the clock destination. This feature minimizes clock distribution difficulty, allowing maximum system clock speed and flexibility.

For a complete list of related resources, click here.

Logic Block Diagram



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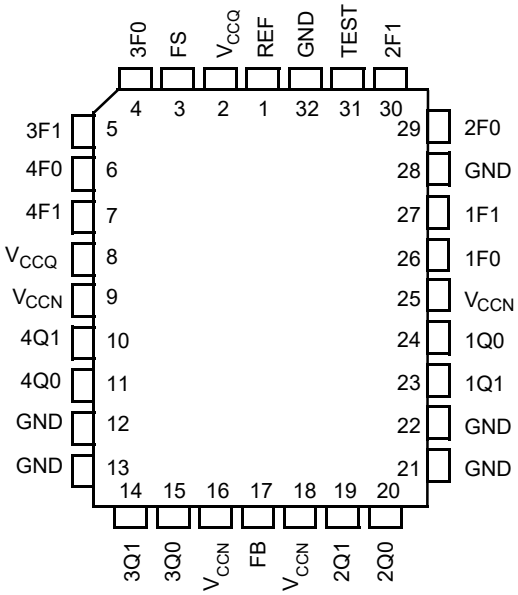
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Pinouts

Figure 1. 32-pin PLCC pinout



Pin Definitions

Pin Name	Pin Number	I/O	Description
REF	1	I	Reference frequency input. This input supplies the frequency and timing against which all functional variations are measured.
FB	17	I	PLL feedback input (typically connected to one of the eight outputs).
FS	3	I	Three-level frequency range select. See Table 1.
1F0, 1F1	26, 27	I	Three-level function select inputs for output pair 1 (1Q0, 1Q1). See Table 2.
2F0, 2F1	29, 30	I	Three-level function select inputs for output pair 2 (2Q0, 2Q1). See Table 2.
3F0, 3F1	4, 5	I	Three-level function select inputs for output pair 3 (3Q0, 3Q1). See Table 2.
4F0, 4F1	6, 7	I	Three-level function select inputs for output pair 4 (4Q0, 4Q1). See Table 2.
TEST	31	I	Three-level select. See test mode section under the block diagram descriptions.
1Q0, 1Q1	24, 23	O	Output pair 1. See Table 2.
2Q0, 2Q1	20, 19	O	Output pair 2. See Table 2.
3Q0, 3Q1	15, 14	O	Output pair 3. See Table 2.
4Q0, 4Q1	11, 10	O	Output pair 4. See Table 2.
V_{CCN}	9, 16, 18, 25	PWR	Power supply for output drivers.
V_{CCQ}	2, 8	PWR	Power supply for internal circuitry.
GND	12, 13, 21, 22, 28, 32	PWR	Ground.

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Block Diagram Description

Phase Frequency Detector and Filter

The phase frequency detector and filter blocks accept inputs from the reference frequency (REF) input and the feedback (FB) input. They generate correction information to control the frequency of the voltage controlled oscillator (VCO). These blocks, along with the VCO, form a PLL that tracks the incoming REF signal.

VCO and Time Unit Generator

The VCO accepts analog control inputs from the PLL filter block. It generates a frequency that is used by the time unit generator to create discrete time units, selected in the skew select matrix. The operational range of the VCO is determined by the FS control pin. The time unit (t_U) is determined by the operating frequency of the device and the level of the FS pin as shown in Table 1.

Table 1. Frequency Range Select and t_U Calculation[1]

FS[2, 3]	f_{NOM} (MHz)		$t_U = \frac{1}{f_{NOM} \times N}$ where N =	Approximate Frequency (MHz) At Which t_U = 1.0 ns
	Min	Max		
LOW	15	30	44	22.7
MID	25	50	26	38.5
HIGH	40	80	16	62.5

Skew Select Matrix

The skew select matrix is comprised of four independent sections. Each section has two low-skew, high fanout drivers (xQ0, xQ1), and two corresponding three-level function select (xF0, xF1) inputs. Table 2 shows the nine possible output functions for each section as determined by the function select inputs. All times are measured with respect to the REF input assuming that the output connected to the FB input has $0t_U$ selected.

Table 2. Programmable Skew Configurations [1]

Function Selects		Output Functions		
1F1, 2F1, 3F1, 4F1	1F0, 2F0, 3F0, 4F0	1Q0, 1Q1, 2Q0, 2Q1	3Q0, 3Q1	4Q0, 4Q1
LOW	LOW	$-4t_U$	Divide by 2	Divide by 2
LOW	MID	$-3t_U$	$-6t_U$	$-6t_U$
LOW	HIGH	$-2t_U$	$-4t_U$	$-4t_U$
MID	LOW	$-1t_U$	$-2t_U$	$-2t_U$
MID	MID	$0t_U$	$0t_U$	$0t_U$
MID	HIGH	$+1t_U$	$+2t_U$	$+2t_U$
HIGH	LOW	$+2t_U$	$+4t_U$	$+4t_U$
HIGH	MID	$+3t_U$	$+6t_U$	$+6t_U$
HIGH	HIGH	$+4t_U$	Divide by 4	Inverted

Notes

1. For all three state inputs, HIGH indicates a connection to V_{CC}, LOW indicates a connection to GND, and MID indicates an open connection. Internal termination circuitry holds an unconnected input to $V_{CC}/2$.
2. The level to be set on FS is determined by the "normal" operating frequency (f_{NOM}) of the V_{CO} and Time Unit Generator (see Logic Block Diagram). Nominal frequency (f_{NOM}) always appears at the outputs when they are operated in their undivided modes (see Table 2). The frequency appearing at the REF and FB inputs is f_{NOM} when the output connected to FB is undivided. The frequency of the REF and FB inputs is $f_{NOM}/2$ or $f_{NOM}/4$ when the part is configured for a frequency multiplication using a divided output as the FB input.
3. When the FS pin is selected HIGH, the REF input must not transition upon power up until V_{CC} has reached 2.8 V.

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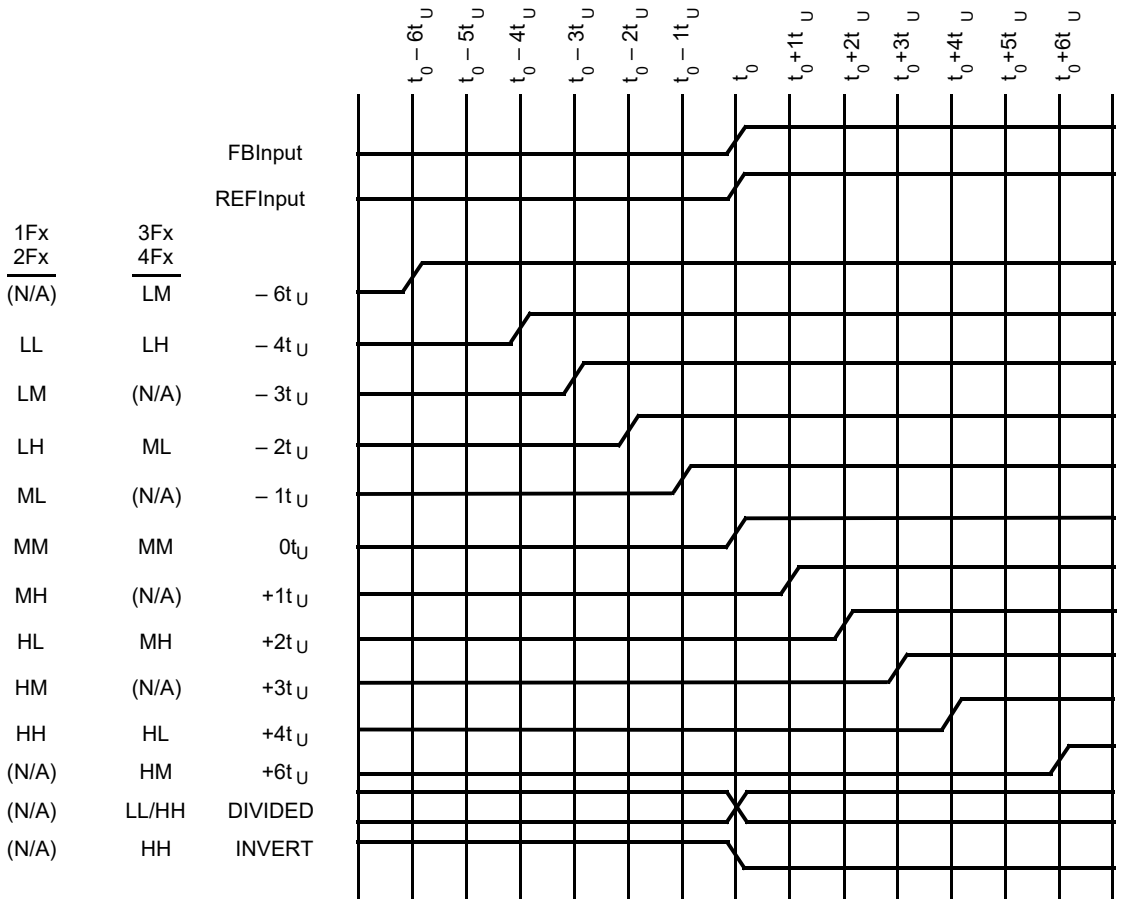
Test Mode

The TEST input is a three-level input. In normal system operation, this pin is connected to ground, allowing the CY7B991V to operate as explained in the Block Diagram Description on page 4. For testing purposes, any of the three-level inputs can have a removable jumper to ground or be tied LOW through a 100-Ω resistor. This enables an external tester to change the state of these pins.

If the TEST input is forced to its MID or HIGH state, the device operates with its internal phase locked loop disconnected, and input levels supplied to REF directly controls all outputs. Relative output to output functions are the same as in normal mode.

In contrast with normal operation (TEST tied LOW), all outputs function based only on the connection of their own function select inputs (xF0 and xF1) and the waveform characteristics of the REF input.

Figure 2. Typical Outputs with FB Connected to a Zero Skew Output Test Mode [4]



Note
4. FB connected to an output selected for “zero” skew (that is, xF1 = xF0 = MID).

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Operational Mode Descriptions

Figure 3. Zero Skew and Zero Delay Clock Driver

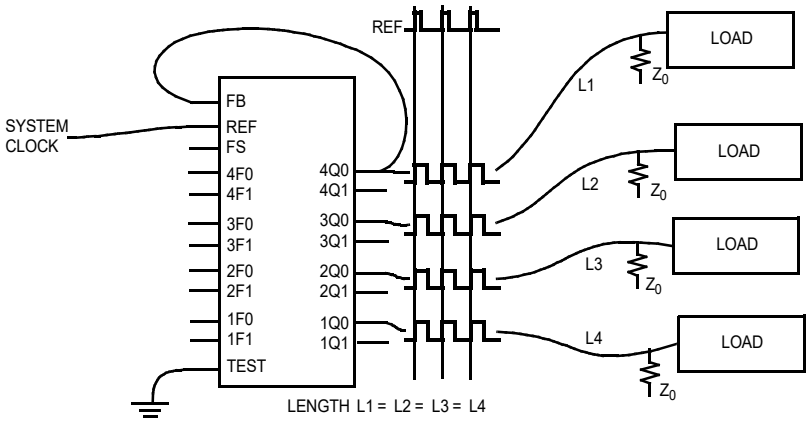


Figure 2 shows the LVPSCB configured as a zero skew clock buffer. In this mode, the CY7B991V is the basis for a low-skew clock distribution tree. When all of the function select inputs (×F0, ×F1) are left open, the outputs are aligned and drive a terminated transmission line to an independent load. The FB input is tied to any output in this configuration and the operating frequency range is selected with the FS pin. The low skew specification, coupled with the ability to drive terminated transmission lines (with impedances as low as 50 Ω), enables efficient printed circuit board design.

Figure 4. Programmable Skew Clock Driver

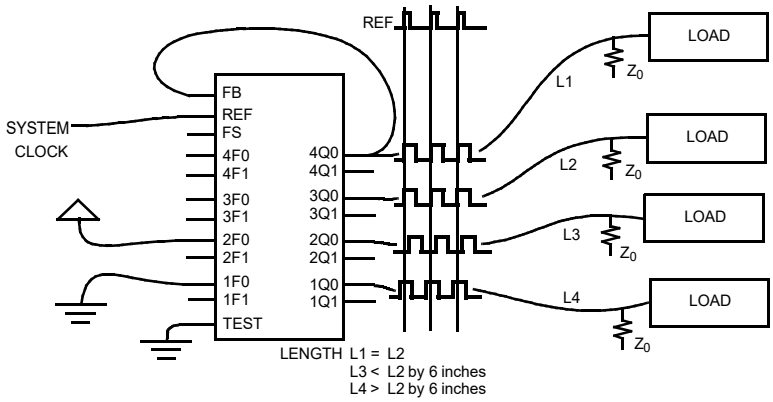


Figure 4 shows a configuration to equalize skew between metal traces of different lengths. In addition to low skew between outputs, the LVPSCB is programmed to stagger the timing of its outputs. The four groups of output pairs are each programmed to different output timing. Skew timing is adjusted over a wide range in small increments using the function select pins. In this configuration, the 4Q0 output is sent back to FB and configured for zero skew. The other three pairs of outputs are programmed to yield different skews relative to the feedback. By advancing the clock signal on the longer traces or retarding the clock signal on shorter traces, all loads receive the clock pulse at the same time.

Figure 4 shows the FB input connected to an output with 0 ns skew (xF1, xF0 = MID) selected. The internal PLL synchronizes the FB and REF inputs and aligns their rising edges to make certain that all outputs have precise phase alignment.

Clock skews are advanced by ±6 time units (tU) when using an output selected for zero skew as the feedback. A wider range of delays is possible if the output connected to FB is also skewed. Since “Zero Skew”, +tU, and –tU are defined relative to output groups, and the PLL aligns the rising edges of REF and FB, wider output skews are created by proper selection of the xFn inputs. For example, a +10 tU between REF and 3Qx is achieved by connecting 1Q0 to FB and setting 1F0 = 1F1 = GND, 3F0 = MID, and 3F1 = High. (Since FB aligns at –4 tU, and 3Qx skews to +6 tU, a total of +10 tU skew is realized.) Many other configurations are realized by skewing both the outputs used as the FB input and skewing the other outputs.

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Figure 5. Inverted Output Connections

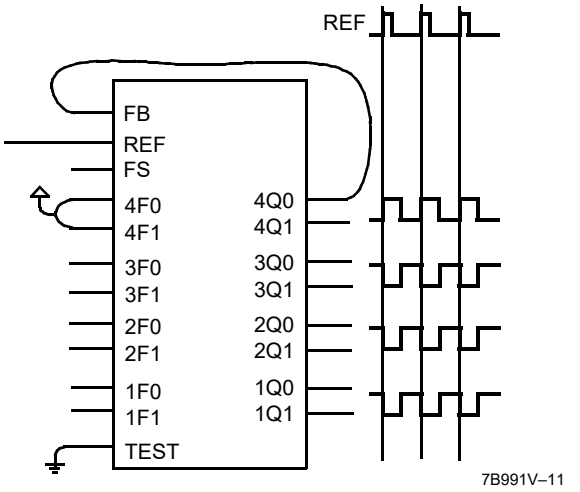


Figure 5 shows an example of the invert function of the LVPSCB. In this example the 4Q0 output used as the FB input is programmed for invert (4F0 = 4F1 = HIGH) while the other three pairs of outputs are programmed for zero skew. When 4F0 and 4F1 are tied high, 4Q0 and 4Q1 become inverted zero phase outputs. The PLL aligns the rising edge of the FB input with the rising edge of the REF. This causes the 1Q, 2Q, and 3Q outputs to become the “inverted” outputs to the REF input. By selecting the output connected to FB, you can have two inverted and six non-inverted outputs or six inverted and two non-inverted outputs. The correct configuration is determined by the need for more (or fewer) inverted outputs. 1Q, 2Q, and 3Q outputs can also be skewed to compensate for varying trace delays independent of inversion on 4Q.

Figure 6. Frequency Multiplier with Skew Connections

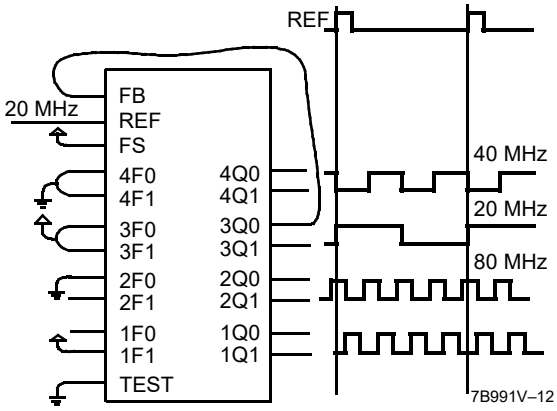


Figure 6 shows the LVPSCB configured as a clock multiplier. The 3Q0 output is programmed to divide by four and is sent back to FB. This causes the PLL to increase its frequency until the 3Q0 and 3Q1 outputs are locked at 20 MHz, while the 1Qx and 2Qx outputs run at 80 MHz. The 4Q0 and 4Q1 outputs are programmed to divide by two that results in a 40 MHz waveform at these outputs. Note that the 20- and 40-MHz clocks fall simultaneously and are out of phase on their rising edge. This enables the designer to use the rising edges of the 1/2 frequency and 1/4 frequency outputs without concern for rising edge skew. The 2Q0, 2Q1, 1Q0, and 1Q1 outputs run at 80 MHz and are skewed by programming their select inputs accordingly. Note that the FS pin is wired for 80 MHz operation as that is the frequency of the fastest output.

Figure 7. Frequency Divider Connections

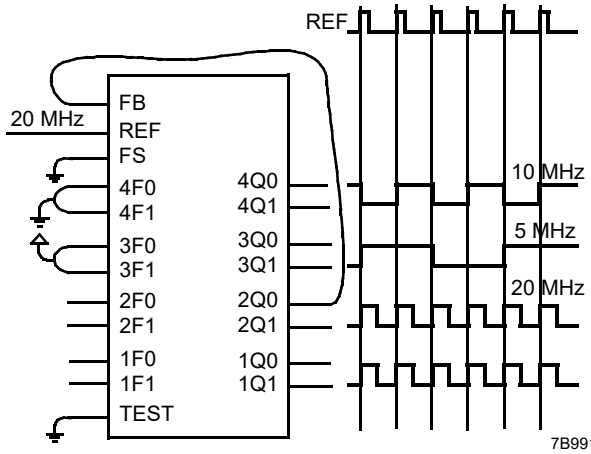


Figure 7 shows the LVPSCB in a clock divider application. 2Q0 is sent back to the FB input and programmed for zero skew. 3Qx is programmed to divide by four. 4Qx is programmed to divide by two. Note that the falling edges of the 4Qx and 3Qx outputs are aligned. This enables use of the rising edges of the 1/2 frequency and 1/4 frequency without concern for skew mismatch. The 1Qx outputs are programmed to zero skew and are aligned with the 2Qx outputs. In this example, the FS input is grounded to configure the device in the 15 to 30 MHz range since the highest frequency output is running at 20 MHz.

Figure 8 on page 8 shows some of the functions that are selectable on the 3Qx and 4Qx outputs. These include inverted outputs and outputs that offer divide-by-2 and divide-by-4 timing. An inverted output enables the system designer to clock different subsystems on opposite edges without suffering from the pulse asymmetry typical of non-ideal loading. This function enables each of the two subsystems to clock 180 degrees out of phase, but still is aligned within the skew specification.

The divided outputs offer a zero delay divider for portions of the system that divide the clock by either two or four, and still remain within a narrow skew of the “1X” clock. Without this feature, an external divider is added, and the propagation delay of the divider adds to the skew between the different clock signals.

These divided outputs, coupled with the PLL, enable the LVPSCB to multiply the clock rate at the REF input by either two or four. This mode allows the designer to distribute a low frequency clock between various portions of the system. It also locally multiplies the clock rate to a more suitable frequency, while still maintaining the low skew characteristics of the clock driver. The LVPSCB performs all of the functions described in this section at the same time. It can multiply by two and four or divide by two (and four) at the same time that it shifts its outputs over a wide range or maintains zero skew between selected outputs.

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Figure 8. Multi-Function Clock Driver

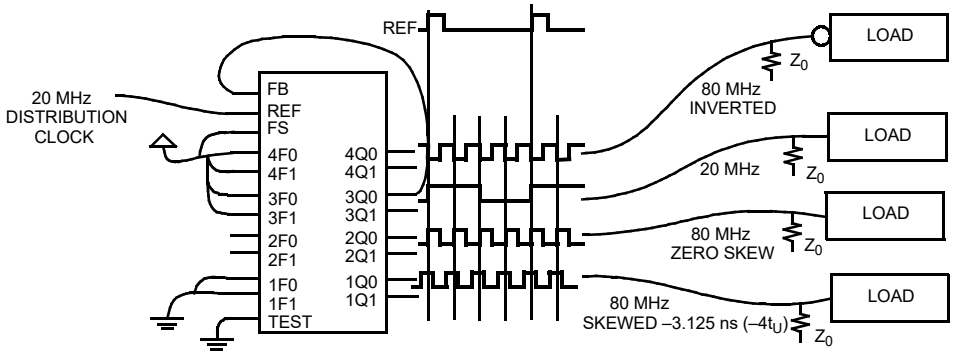


Figure 9. Board-to-Board Clock Distribution

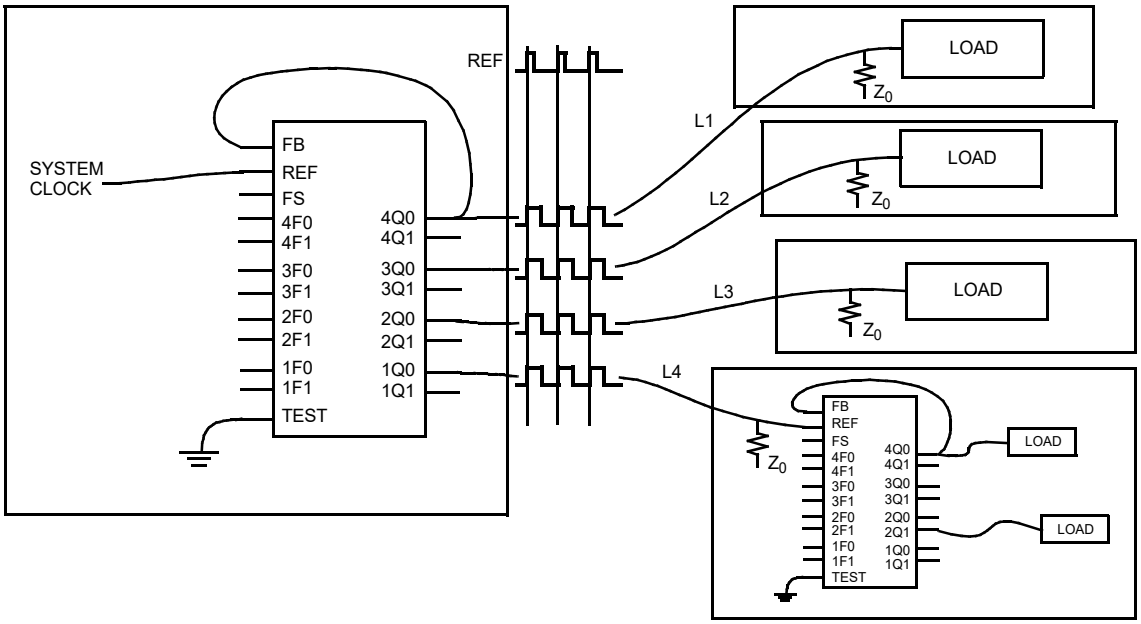


Figure 9 shows the CY7B991V connected in series to construct a zero skew clock distribution tree between boards. Delays of the downstream clock buffers are programmed to compensate for the wire length (that is, select negative skew equal to the wire delay) necessary to connect them to the master clock source, approximating a zero delay clock tree. Cascaded clock buffers accumulate low frequency jitter because of the non-ideal filtering characteristics of the PLL filter. Do not connect more than two clock buffers in a series.

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Maximum Ratings

Operating outside these boundaries may affect the performance and life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to 150 °C

Ambient temperature with power applied ..... –55 °C to 125 °C

Supply voltage to ground potential .....–0.5 V to +7.0 V

DC input voltage .....–0.5 V to +7.0 V

Output current into outputs (LOW) ..... 64 mA

Static discharge voltage (MIL-STD-883, Method 3015) .....>2001 V

Latch up current .....>200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0 °C to 70 °C	3.3 V ± 10%
Industrial	–40 °C to 85 °C	3.3 V ± 10%

Electrical Characteristics

Over the Operating Range

Parameter [5]	Description	Test Conditions		CY7B991V		Unit
				Min	Max	
V_{OH}	Output HIGH voltage	V_{CC} = Min, I_{OH} = –12 mA		2.4	–	V
V_{OL}	Output LOW voltage	V_{CC} = Min, I_{OL} = 35 mA		–	0.45	V
V_{IH}	Input HIGH voltage (REF and FB inputs only)			2.0	V_{CC}	V
V_{IL}	Input LOW voltage (REF and FB inputs only)			–0.5	0.8	V
V_{IHH}	Three-level input HIGH Voltage (Test, FS, xFn) [6]	Min ≤ V_{CC} ≤ Max.		0.87 × V_{CC}	V_{CC}	V
V_{IMM}	Three-level input MID voltage (Test, FS, xFn) [6]	Min ≤ V_{CC} ≤ Max.		0.47 × V_{CC}	0.53 × V_{CC}	V
V_{ILL}	Three-level input LOW voltage (Test, FS, xFn) [6]	Min ≤ V_{CC} ≤ Max.		0.0	0.13 × V_{CC}	V
I_{IH}	Input HIGH leakage current (REF and FB inputs only)	V_{CC} = Max, V_{IN} = Max.		–	20	µA
I_{IL}	Input LOW leakage current (REF and FB inputs only)	V_{CC} = Max, V_{IN} = 0.4 V		–20	–	µA
I_{IHH}	Input HIGH current (Test, FS, xFn)	V_{IN} = V_{CC}		–	200	µA
I_{IMM}	Input MID current (Test, FS, xFn)	V_{IN} = V_{CC}/2		–50	50	µA
I_{ILL}	Input LOW current (Test, FS, xFn)	V_{IN} = GND		–200	–	µA
I_{OS}	Short circuit current [7]	V_{CC} = Max, V_{OUT} = GND (25 °C only)		–200	–	mA
I_{CCQ}	Operating current used by internal circuitry	V_{CCN} = V_{CCQ} = Max, All Input Selects Open	Commercial	–	95	mA
			Military / Industrial	–	100	mA
I_{CCN}	Output buffer current per output pair [8]	V_{CCN} = V_{CCQ} = Max, I_{OUT} = 0 mA, Input Selects Open, f_{MAX}		–	19	mA

Notes

5. See the last page of this specification for Group A subgroup testing information.
6. These inputs are normally wired to V_{CC}, GND, or left unconnected (actual threshold voltages vary as a percentage of V_{CC}). Internal termination resistors hold unconnected inputs at V_{CC}/2. If these inputs are switched, the function and timing of the outputs glitch and the PLL requires an additional t_{LOCK} time before all datasheet limits are achieved.
7. CY7B991V is tested one output at a time, output shorted for less than one second, less than 10% duty cycle. Room temperature only.
8. Total output current per output pair is approximated by the following expression that includes device current plus load current:
   CY7B991V:I_{CCN} = [(4 + 0.11F) + [((835 –3F)/Z) + (.0022FC)]N] x 1.1
   Where
   F = frequency in MHz
   C = capacitive load in pF
   Z = line impedance in ohms
   N = number of loaded outputs; 0, 1, or 2
   FC = F × C

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Electrical Characteristics (continued)

Over the Operating Range

Parameter [5]	Description	Test Conditions	CY7B991V		Unit
			Min	Max	
PD	Power dissipation per output pair	$V_{CCN} = V_{CCQ}$ = Max, I_{OUT} = 0 mA, Input Selects Open, f_{MAX}	–	104	mW

Capacitance

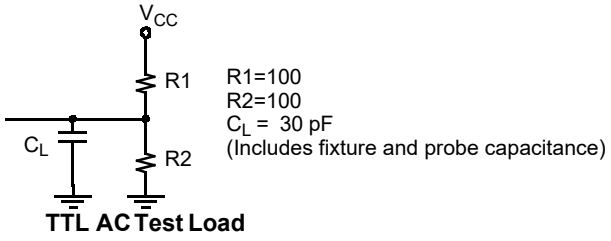
Parameter [9, 10]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 3.3 V	10	pF

Thermal Resistance

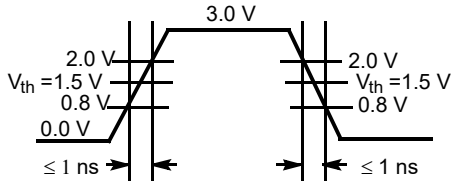
Parameter [10]	Description	Test Conditions	32-pin PLCC Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, according to EIA/JESD51.	44	°C/W
Θ_{JC}	Thermal resistance (junction to case)		26	°C/W

AC Test Loads and Waveforms

Figure 10. AC Test Loads and Waveforms



TTL AC Test Load



TTL Input Test Waveform

Notes
9. Applies to REF and FB inputs only. Tested initially and after any design or process changes that may affect these parameters.
10. Tested initially and after any design or process changes that may affect these parameters.

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Switching Characteristics (-2 option)

Over the Operating Range

Parameter [11, 12]	Description		CY7B991V-2			Unit
			Min	Typ	Max	
f_{NOM}	Operating clock Frequency in MHz	FS = LOW [11, 13]	15	–	30	MHz
		FS = MID [11, 13]	25	–	50	
		FS = HIGH [11, 13, 14]	40	–	80	
t_{RPWH}	REF pulse width HIGH measured at 1/2 × V_{CCQ} threshold		3.65	–	–	ns
t_{RPWL}	REF pulse width LOW measured at 1/2 × V_{CCQ} threshold		3.65	–	–	ns
t_U	Programmable skew unit		See Table 1			
t_{SKEWPR}	Zero output matched-pair skew (XQ0, XQ1)[15, 16]		–	0.05	0.2	ns
t_{SKEW0}	Zero output skew (all outputs)[15, 17]		–	0.1	0.25	ns
t_{SKEW1}	Output skew (rise-rise, fall-fall, same class outputs)[15, 18]		–	0.1	0.5	ns
t_{SKEW2}	Output skew (rise-fall, nominal-inverted, divided-divided)[15, 18]		–	0.5	1.0	ns
t_{SKEW3}	Output skew (rise-rise, fall-fall, different class outputs)[15, 18]		–	0.25	0.5	ns
t_{SKEW4}	Output skew (rise-fall, nominal-divided, divided-inverted)[15, 18]		–	0.5	0.9	ns
t_{DEV}	Device-to-device skew[19, 20]		–	–	1.25	ns
t_{PD}	Propagation delay, REF rise to FB rise		–0.25	0.0	+0.25	ns
t_{ODCV}	Output duty cycle variation[21]		–0.65	0.0	+0.65	ns
t_{PWH}	Output HIGH time deviation from 50%[22]		–	–	2.0	ns
t_{PWL}	Output LOW time deviation from 50%[22]		–	–	1.5	ns
t_{ORISE}	Output rise time[22, 23]		0.15	1.0	1.2	ns
t_{OFALL}	Output fall time[22, 23]		0.15	1.0	1.2	ns
t_{LOCK}	PLL lock time[24]		–	–	0.5	ms
t_{JR}	Cycle-to-cycle output jitter	RMS[19]	–	–	25	ps
		Peak[19]	–	100	200	ps

Notes

11. The level to be set on FS is determined by the “normal” operating frequency (f_{NOM}) of the V_{CO} and Time Unit Generator (see Logic Block Diagram). Nominal frequency (f_{NOM}) always appears at the outputs when they are operated in their undivided modes (see Table 2). The frequency appearing at the REF and FB inputs is f_{NOM} when the output connected to FB is undivided. The frequency of the REF and FB inputs is $f_{NOM}/2$ or $f_{NOM}/4$ when the part is configured for a frequency multiplication using a divided output as the FB input.
12. Test measurement levels for the CY7B991V are TTL levels (1.5 V to 1.5 V). Test conditions assume signal transition times of 2 ns or less and output loading as shown in the AC Test Loads and Waveforms unless otherwise specified.
13. For all three state inputs, HIGH indicates a connection to V_{CC}, LOW indicates a connection to GND, and MID indicates an open connection. Internal termination circuitry holds an unconnected input to $V_{CC}/2$.
14. When the FS pin is selected HIGH, the REF input must not transition upon power up until V_{CC} has reached 2.8 V.
15. SKEW is defined as the time between the earliest and the latest output transition among all outputs for which the same t_U delay has been selected when all are loaded with 30 pF and terminated with 50Ω to $V_{CC}/2$ (CY7B991V).
16. t_{SKEWPR} is defined as the skew between a pair of outputs (XQ0 and XQ1) when all eight outputs are selected for $0t_U$.
17. t_{SKEW0} is defined as the skew between outputs when they are selected for $0t_U$. Other outputs are divided or inverted but not shifted.
18. There are three classes of outputs: Nominal (multiple of t_U delay), Inverted (4Q0 and 4Q1 only with 4F0 = 4F1 = HIGH), and Divided (3Qx and 4Qx only in Divide-by-2 or Divide-by-4 mode).
19. Guaranteed by statistical correlation. Tested initially and after any design or process changes that may affect these parameters.
20. t_{DEV} is the output-to-output skew between any two devices operating under the same conditions (V_{CC} ambient temperature, air flow, etc.)
21. t_{ODCV} is the deviation of the output from a 50% duty cycle. Output pulse width variations are included in t_{SKEW2} and t_{SKEW4} specifications.
22. Specified with outputs loaded with 30 pF for the CY7B991V–5 and –7 devices. Devices are terminated through 50Ω to $V_{CC}/2$. t_{PWH} is measured at 2.0 V. t_{PWL} is measured at 0.8 V.
23. t_{ORISE} and t_{OFALL} measured between 0.8 V and 2.0 V.
24. t_{LOCK} is the time that is required before synchronization is achieved. This specification is valid only after V_{CC} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.

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Switching Characteristics (-5 Option)

Over the Operating Range

Parameter [25, 26]	Description		CY7B991V-5			Unit
			Min	Typ	Max	
f_{NOM}	Operating clock frequency in MHz	FS = LOW [25, 27]	15	–	30	MHz
		FS = MID [25, 27]	25	–	50	
		FS = HIGH [25, 27]	40	–	80	
t_{RPWH}	REF pulse width HIGH measured at 1/2 × V_{CCQ} threshold		3.65	–	–	ns
t_{RPWL}	REF pulse width LOW measured at 1/2 × V_{CCQ} threshold		3.65	–	–	ns
t_U	Programmable skew unit		See Table 1			
t_{SKEWPR}	Zero output matched-pair skew (XQ0, XQ1)[28, 29]		–	0.1	0.25	ns
t_{SKEW0}	Zero output skew (all outputs)[28, 29]		–	0.25	0.5	ns
t_{SKEW1}	Output skew (rise-rise, fall-fall, same class outputs)[28, 30]		–	0.6	0.7	ns
t_{SKEW2}	Output skew (rise-fall, nominal-inverted, divided-divided)[28, 30]		–	0.5	1.0	ns
t_{SKEW3}	Output skew (rise-rise, fall-fall, different class outputs)[28, 30]		–	0.5	0.7	ns
t_{SKEW4}	Output skew (rise-fall, nominal-divided, divided-inverted)[28, 30]		–	0.5	1.0	ns
t_{DEV}	Device-to-device skew[32, 33]		–	–	1.25	ns
t_{PD}	Propagation delay, REF rise to FB rise		–0.5	0.0	+0.5	ns
t_{ODCV}	Output duty cycle variation[34]		–1.0	0.0	+1.0	ns
t_{PWH}	Output HIGH time deviation from 50%[35]		–	–	2.5	ns
t_{PWL}	Output LOW time deviation from 50%[35]		–	–	3	ns
t_{ORISE}	Output rise time[35, 36]		0.15	1.0	1.5	ns
t_{OFALL}	Output fall time[35, 36]		0.15	1.0	1.5	ns
t_{LOCK}	PLL lock time[36]		–	–	0.5	ms
t_{JR}	Cycle-to-cycle output jitter	RMS[32]	–	–	25	ps
		Peak-to-peak[32]	–	–	200	ps

Notes

25. The level to be set on FS is determined by the "normal" operating frequency (f_{NOM}) of the V_{CO} and Time Unit Generator (see Logic Block Diagram). Nominal frequency (f_{NOM}) always appears at the outputs when they are operated in their undivided modes (see Table 2). The frequency appearing at the REF and FB inputs is f_{NOM} when the output connected to FB is undivided. The frequency of the REF and FB inputs is $f_{NOM}/2$ or $f_{NOM}/4$ when the part is configured for a frequency multiplication using a divided output as the FB input.
26. Test measurement levels for the CY7B991V are TTL levels (1.5 V to 1.5 V). Test conditions assume signal transition times of 2 ns or less and output loading as shown in the AC Test Loads and Waveforms unless otherwise specified.
27. For all three state inputs, HIGH indicates a connection to V_{CC}, LOW indicates a connection to GND, and MID indicates an open connection. Internal termination circuitry holds an unconnected input to $V_{CC}/2$.
28. t_{SKEWPR} is defined as the skew between a pair of outputs (XQ0 and XQ1) when all eight outputs are selected for $0t_U$.
29. t_{SKEW0} is defined as the skew between outputs when they are selected for $0t_U$. Other outputs are divided or inverted but not shifted.
30. t_{DEV} is the output-to-output skew between any two devices operating under the same conditions (V_{CC} ambient temperature, air flow, etc.)
31. C_L = 0 pF. For C_L = 30 pF, t_{SKEW0} = 0.35 ns.
32. SKEW is defined as the time between the earliest and the latest output transition among all outputs for which the same t_U delay has been selected when all are loaded with 30 pF and terminated with 50Ω to $V_{CC}/2$ (CY7B991V).
33. t_{ODCV} is the deviation of the output from a 50% duty cycle. Output pulse width variations are included in t_{SKEW2} and t_{SKEW4} specifications.
34. Specified with outputs loaded with 30 pF for the CY7B991V–5 and –7 devices. Devices are terminated through 50Ω to $V_{CC}/2$. t_{PWH} is measured at 2.0 V. t_{PWL} is measured at 0.8 V.
35. t_{ORISE} and t_{OFALL} measured between 0.8 V and 2.0 V.
36. t_{LOCK} is the time that is required before synchronization is achieved. This specification is valid only after V_{CC} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.

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Switching Characteristics (-7 Option)

Over the Operating Range

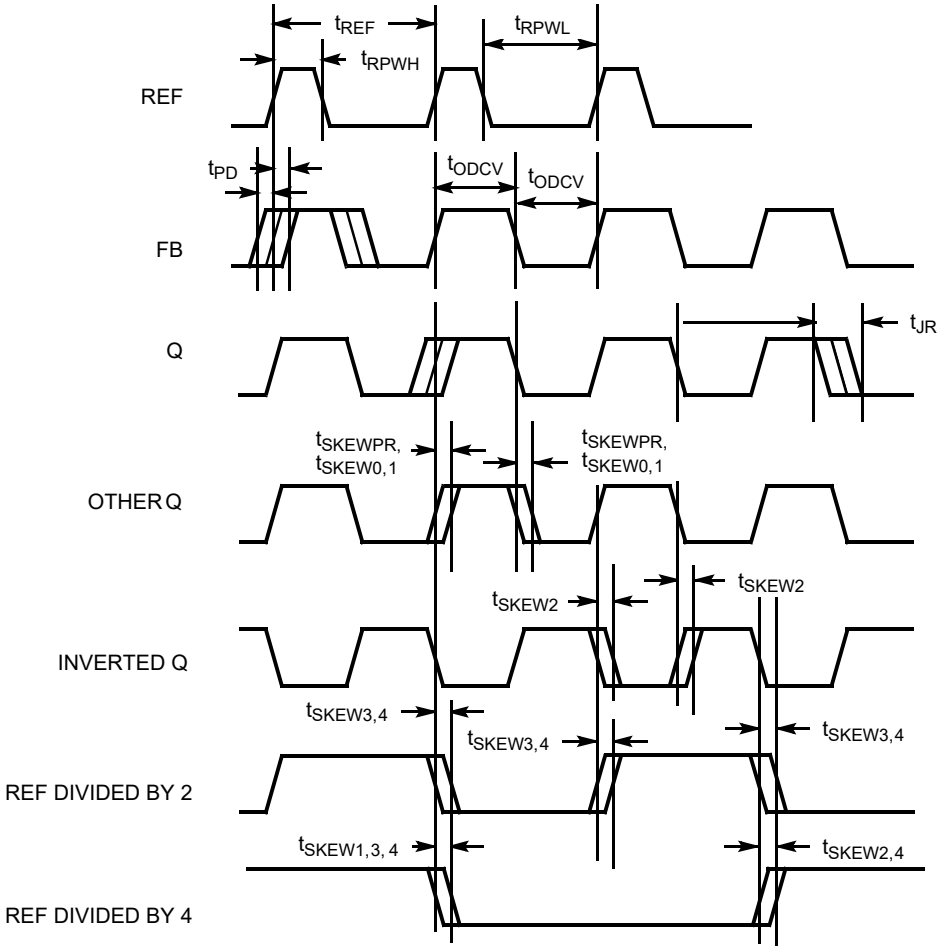
Parameter [37, 38]	Description		CY7B991V–7			Unit
			Min	Typ	Max	
f_{NOM}	Operating clock Frequency in MHz	FS = LOW [37, 39]	15	–	30	MHz
		FS = MID [37, 39]	25	–	50	
		FS = HIGH [37, 39]	40	–	80	
t_{RPWH}	REF pulse width HIGH measured at 1/2 × V_{CCQ} threshold		3.65	–	–	ns
t_{RPWL}	REF pulse width LOW measured at 1/2 × V_{CCQ} threshold		3.65	–	–	ns
t_U	Programmable skew unit		See *Table 1*			
t_{SKEWPR}	Zero output matched pair skew (XQ0, XQ1)[40, 41]		–	0.1	0.25	ns
t_{SKEW0}	Zero output skew (All Outputs)[40, 42]		–	0.3	0.75	ns
t_{SKEW1}	Output skew (rise-rise, fall-fall, same class outputs)[43, 44]		–	0.6	1.0	ns
t_{SKEW2}	Output skew (rise-fall, nominal-inverted, divided-divided)[40, 45]		–	1.0	1.5	ns
t_{SKEW3}	Output skew (rise-rise, fall-fall, different class outputs)[40, 45]		–	0.7	1.2	ns
t_{SKEW4}	Output skew (rise-fall, nominal-divided, divided-inverted)[40, 45]		–	1.2	1.7	ns
t_{DEV}	Device-to-device skew[43, 46]		–	–	1.65	ns
t_{PD}	Propagation delay, REF rise to FB rise		–0.7	0.0	+0.7	ns
t_{ODCV}	Output duty cycle variation[46]		–1.2	0.0	+1.2	ns
t_{PWH}	Output HIGH time deviation from 50%[47]		–	–	3	ns
t_{PWL}	Output LOW time deviation from 50%[47]		–	–	3.5	ns
t_{ORISE}	Output rise time[47, 48]		0.15	1.5	2.5	ns
t_{OFALL}	Output fall time[47, 48]		0.15	1.5	2.5	ns
t_{LOCK}	PLL lock time[49]		–	–	0.5	ms
t_{JR}	Cycle-to-cycle output jitter	RMS[50]	–	–	25	ps
		Peak-to-peak[50]	–	–	200	ps

Notes

37. The level to be set on FS is determined by the "normal" operating frequency (f_{NOM}) of the V_{CO} and Time Unit Generator (see Logic Block Diagram). Nominal frequency (f_{NOM}) always appears at the outputs when they are operated in their undivided modes (see Table 2). The frequency appearing at the REF and FB inputs is f_{NOM} when the output connected to FB is undivided. The frequency of the REF and FB inputs is $f_{NOM}/2$ or $f_{NOM}/4$ when the part is configured for a frequency multiplication using a divided output as the FB input.
38. Test measurement levels for the CY7B991V are TTL levels (1.5 V to 1.5 V). Test conditions assume signal transition times of 2 ns or less and output loading as shown in the AC Test Loads and Waveforms unless otherwise specified.
39. For all three state inputs, HIGH indicates a connection to V_{CC}, LOW indicates a connection to GND, and MID indicates an open connection. Internal termination circuitry holds an unconnected input to $V_{CC}/2$.
40. t_{SKEWPR} is defined as the skew between a pair of outputs (XQ0 and XQ1) when all eight outputs are selected for $0t_U$.
41. t_{SKEW0} is defined as the skew between outputs when they are selected for $0t_U$. Other outputs are divided or inverted but not shifted.
42. C_L = 0 pF. For C_L = 30 pF, t_{SKEW0} = 0.35 ns.
43. SKEW is defined as the time between the earliest and the latest output transition among all outputs for which the same t_U delay has been selected when all are loaded with 30 pF and terminated with 50Ω to $V_{CC}/2$ (CY7B991V).
44. There are three classes of outputs: Nominal (multiple of t_U delay), Inverted (4Q0 and 4Q1 only with 4F0 = 4F1 = HIGH), and Divided (3Qx and 4Qx only in Divide-by-2 or Divide-by-4 mode).
45. t_{DEV} is the output-to-output skew between any two devices operating under the same conditions (V_{CC} ambient temperature, air flow, etc.)
46. t_{ODCV} is the deviation of the output from a 50% duty cycle. Output pulse width variations are included in t_{SKEW2} and t_{SKEW4} specifications.
47. Specified with outputs loaded with 30 pF for the CY7B991V–5 and –7 devices. Devices are terminated through 50Ω to $V_{CC}/2$. t_{PWH} is measured at 2.0 V. t_{PWL} is measured at 0.8 V.
48. t_{ORISE} and t_{OFALL} measured between 0.8 V and 2.0 V.
49. t_{LOCK} is the time that is required before synchronization is achieved. This specification is valid only after V_{CC} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.
50. Guaranteed by statistical correlation. Tested initially and after any design or process changes that may affect these parameters.

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AC Timing Diagrams

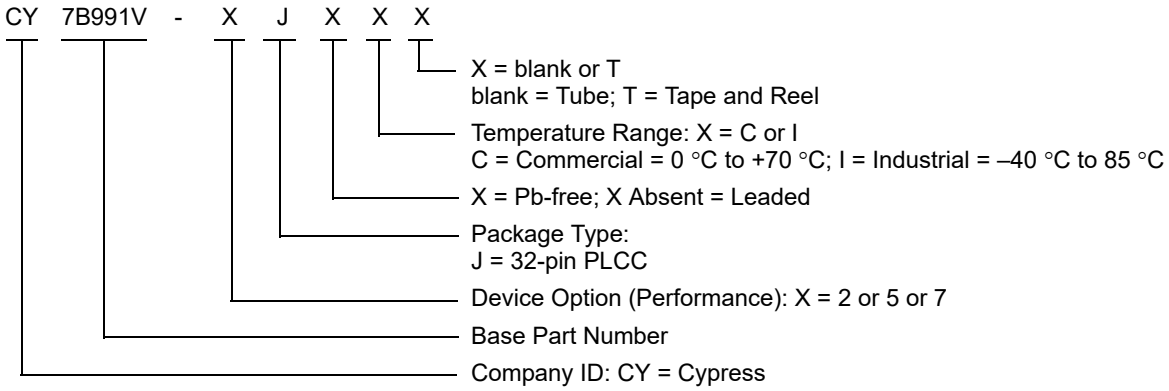


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Ordering Information

Speed (ps)	Ordering Code	Package Type	Operating Range
Pb-free			
250	CY7B991V-2JXC	32-pin PLCC	Commercial
	CY7B991V-2JXCT	32-pin PLCC – Tape and Reel	Commercial
500	CY7B991V-5JXC	32-pin PLCC	Commercial
	CY7B991V-5JXCT	32-pin PLCC – Tape and Reel	Commercial
	CY7B991V-5JXI	32-pin PLCC	Industrial
	CY7B991V-5JXIT	32-pin PLCC – Tape and Reel	Industrial
750	CY7B991V-7JXC	32-pin PLCC	Commercial
	CY7B991V-7JXCT	32-pin PLCC – Tape and Reel	Commercial

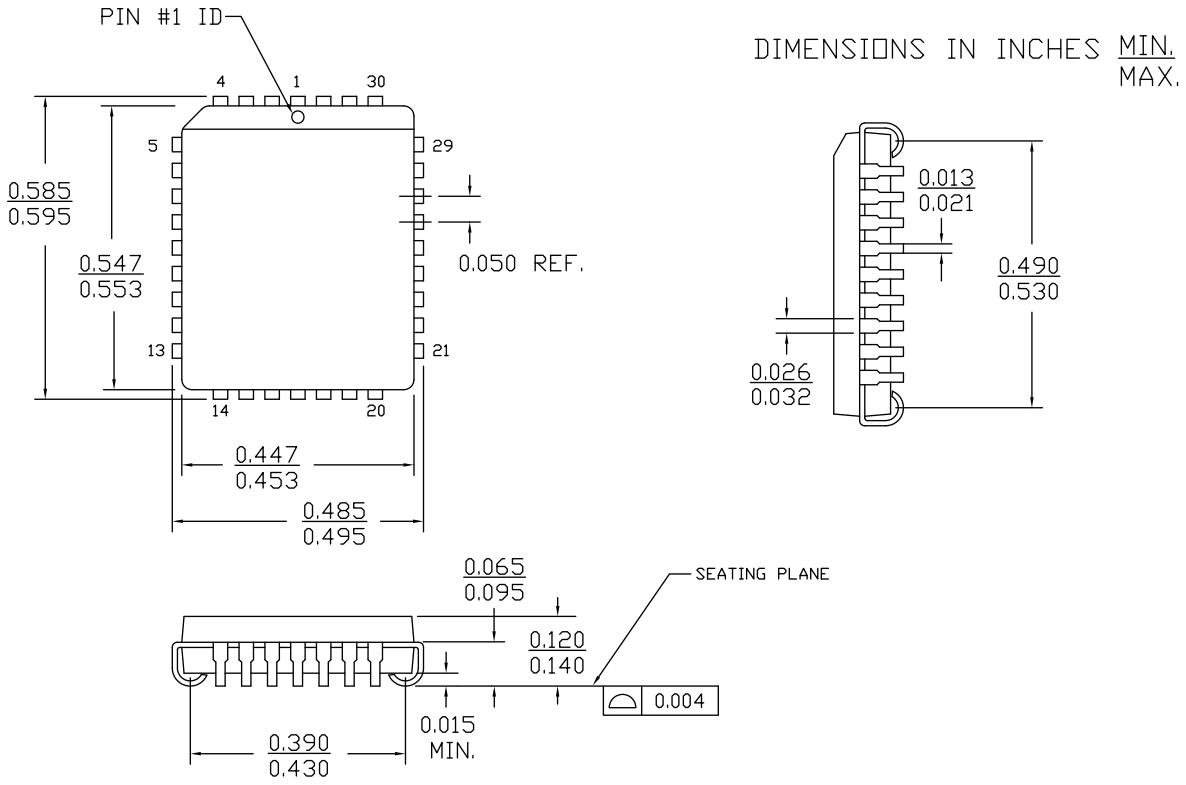
Ordering Code Definitions



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Package Diagram

Figure 11. 32-pin PLCC (0.453 × 0.553 Inches) J32 Package Outline, 51-85002



51-85002 *E

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Acronyms

Table 3. Acronyms Used in this Document

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
FB	Feedback
LVPSCB	Low-Voltage Programmable Skew Clock Buffer
LVTTL	Low-Voltage Transistor-Transistor Logic
PLL	Phase-Locked Loop
PLCC	Plastic Leaded Chip Carrier
RF	Reference Frequency
RMS	Root Mean Square
VCO	Voltage Controlled Oscillator

Document Conventions

Units of Measure

Table 4. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kΩ	kilohm
µA	microampere
µs	microsecond
mA	milliampere
ms	millisecond
mW	milliwatt
MHz	megahertz
ns	nanosecond
Ω	ohm
pF	picofarad
ps	picosecond
V	volt
W	watt

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Document History Page

Document Title: CY7B991V, 3.3 V RoboClock® Low Voltage Programmable Skew Clock Buffer Document Number: 38-07141				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	110250	SZV	12/17/2001	Change from Specification number: 38-00641 to 38-07141.
*A	293239	RGL	11/29/2004	Updated Features: Removed “Jitter < 200 ps peak-to-peak (< 25 ps RMS)”. Added “Jitter 100 ps (typical)”. Updated Switching Characteristics (-2 option): Added typical value of t_{JR} parameter as “100 ps” corresponding to “Peak”. Updated Ordering Information: Updated part numbers.
*B	1199925	KVM / AESA	06/29/2007	Removed “Switching Characteristics (-2 option)”. Updated Ordering Information: No change in part numbers. Changed format only.
*C	1286064	AESA	07/18/2007	Change status from Preliminary to Final.
*D	2584293	AESA	10/10/2008	Added Switching Characteristics (-2 option). Updated to new template.
*E	2761988	CXQ	09/10/2009	Updated Test Mode: Replaced “100W resistor” with “100Ω resistor”. Updated Ordering Information: No change in part numbers. Replaced “Pb” with “pin” in “Package Type” column.
*F	2905834	CXQ	04/06/2010	Updated Ordering Information: Removed inactive part numbers CY7B991V-5JC, CY7B991V-5JCT, CY7B991V-7JC and CY7B991V-7JCT. Updated Package Diagram.
*G	3041840	CXQ	09/29/2010	Fixed various format and typographical errors. Updated Pinouts: Updated Figure 1 (Fixed pin 8 label). Updated Pin Definitions: Added “Pin Number” column. Updated Electrical Characteristics: Removed values from “Max” column of I_{LL} and I_{OS} parameters and added the same values in “Min” column. Removed note “These inputs are normally wired to V_{CC}, GND, or left unconnected (actual threshold voltages vary as a percentage of V_{CC}). Internal termination resistors hold unconnected inputs at $V_{CC}/2$. If these inputs are switched, the function and timing of the outputs may glitch and the PLL may require an additional t_{LOCK} time before all datasheet limits are achieved.” and its reference in “Description” column of PD parameter. Completing Sunset Review.
*H	4161003	CINM	10/16/2013	Updated Package Diagram: spec 51-85002 – Changed revision from *C to *D. Updated to new template. Completing Sunset Review.
*I	4598452	TAVA	12/16/2014	Updated Functional Description: Added “For a complete list of related resources, click here.” at the end. Added AC Timing Diagrams.

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Document History Page (continued)

Document Title: CY7B991V, 3.3 V RoboClock® Low Voltage Programmable Skew Clock Buffer Document Number: 38-07141				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*J	4644120	TAVA	01/28/2015	Updated Switching Characteristics (-2 option): Updated description of t_{RPWH} and t_{RPWL} parameters. Changed minimum value of t_{RPWH} parameter from 5 ns to 3.65 ns. Changed minimum value of t_{RPWL} parameter from 5 ns to 3.65 ns. Updated Switching Characteristics (-5 Option): Updated description of t_{RPWH} and t_{RPWL} parameters. Changed minimum value of t_{RPWH} parameter from 5 ns to 3.65 ns. Changed minimum value of t_{RPWL} parameter from 5 ns to 3.65 ns. Updated Switching Characteristics (-7 Option): Updated description of t_{RPWH} and t_{RPWL} parameters. Changed minimum value of t_{RPWH} parameter from 5 ns to 3.65 ns. Changed minimum value of t_{RPWL} parameter from 5 ns to 3.65 ns. Updated Package Diagram: spec 51-85002 – Changed revision from *D to *E.
*K	5276098	PSR	05/18/2016	Updated Electrical Characteristics: Updated Note 8 (Replaced “FC = F < C” with “FC = F × C”). Added Thermal Resistance. Updated to new template.
*L	5507104	PAWK	11/02/2016	Updated to new template. Completing Sunset Review.
*M	6011930	PAWK	01/03/2018	Updated Ordering Information: Updated part numbers. Updated to new template.

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