Datasheet

BL54L15, BL54L10 Series

Version 1.8

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Revision History

Version	Date	Notes	Contributor(s)	Approver
0.1	10 June 2024	Initial PRELIMINARY release.	Raj Khatri	Jonathan Kaye
0.2	2 Oct 2024	Updated pin list names and notes below table1. Added section External Antenna Integration with BL54L15/BL54L10 MHF4 variant (453-00044/453-00226) Added section on Programmability.	Raj Khatri	Jonathan Kaye
0.3	24 Oct 2024	Removed Medium voltage mode (VDDM_nRF) from Specification Summary table and updated Normal voltage mode (VDD_nRF) operating range from 1.7V-2.6V to 1.7V-3.6V. Updated Block Diagram and Pin-out for 39 connection pins. Updated SCH symbol to remove pin40. Updated pin list in Table 1 (removed pin 40 VDDM_nRF). Updated BL54L15/ BL54L10 Power Supply Updated Table 4 external antenna Mag Layers EDA-8709-2G4C1-B27-CY antenna gain from 2dBi to 2.32dBi.	Raj Khatri	Jonathan Kaye
0.4	6 Dec 2024	Updated maximum Tx power to +7 dBm.	Dave Drogowski	Jonathan Kaye
0.5	11 Dec 2024	Updated sensitivity value Added trace antenna performance	Louis Chang	Jonathan Kaye
0.6	16 Dec 2024	Updated maximum Tx power to +6 dBm.	Louis Chang	Jonathan Kaye
1.0	16 Dec 2024	Initial release	Dave Drogowski	Jonathan Kaye
1.1	19 Dec 2024	Updated maximum Tx power to +7 dBm.	Louis Chang	Jonathan Kaye
1.2	13 Jan 2025	Updated title of 7.4 Updated some typo	Louis Chang	Jonathan Kaye
1.3	21 Feb. 2025	Change (VDD_nRF) operating range from 1.7V-3.6V to 1.7V-3.5V. Add VDD_nRF supply voltage (1.7V-3.3V) under extended operating Temperature (85 to 105C) Update Absolute maximum ratings of VDD_nRF (-0.3V-3.6V)	Louis Chang	Jonathan Kaye
1.4	25 Feb. 2025	Update Minimum Transmit Power Setting to -40dBm Update Active Modes Peak Current	Louis Chang	Jonathan Kaye
1.5	27 Feb. 2025	Update 32MHz crystal oscillator internal capacitor setting value Update 32.768KHz crystal oscillator internal capacitor setting value Update NFC antenna pin current value	Louis Chang	Jonathan Kaye
1.6	3 Mar. 2025	Update Idle mode and off mode current BL54L10 Antenna performance shares with BL54L15	Louis Chang	Jonathan Kaye
1.7	10 Mar. 25	Update 2.4GHz Radiated Performance Update flash specs in Absolute Maximum Ratings	Louis Chang	Jonathan Kaye
1.8	18 Mar. 25	Update power consumption in 2.1	Louis Chang	Jonathan Kaye

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1 Overview and Key Features



Experience a new pinnacle of performance, efficiency, and security with our new BL54L15 and BL54L10 series, built on Nordic Semiconductor's powerful **nRF54L QFN** silicon. Elevating what you know and love from the nRF52 series, this next generation redefines Bluetooth LE and 802.15.4 solutions. Unleashing enhanced processing power, expanded memory, and innovative peripherals, the BL54L15 is the ultimate choice for low power connectivity.

Powered by **Nordic's nRF54L15 and nRF54L10** SoC, our compact BL54L15 and BL54L10 modules deliver secure and robust Bluetooth LE and 802.15.4 with flexible programming via Nordic's nRF Connect SDK or Ezurio Canvas Software Suite.

Featuring a **128MHz ARM Cortex M33** and **128MHz RISC-V coprocessor**, supported by 1.5 MB non-volatile memory and 256 KB RAM for BL54L15, 1.0 MB non-volatile memory and 192 KB RAM for BL54L10, the BL54L15 and BL54L10 modules offer double the processing power (vs prior BL654 – nRF52840). The BL54L15 / L10 series brings out all nRF54L15/ L10 hardware features and capabilities including up to **+7 dBm** transmit power, **1.7V – 3.5V** supply considerations, and **NFC A-Tag** implementation.

It's further enhanced with state-of-the-art security and is designed for PSA Certified level 3 and supports services such as Secure Boot, Secure Firmware Update, Secure Storage plus protection from physical attacks.

Note: BL54L15/ BL54L10 hardware provides all functionality of the nRF54L15/ nRF54L10 chipset used in the module design. This is a hardware datasheet only – it does not cover the software aspects of the BL54L15 and BL54L10. This is to acknowledge that information in this datasheet is referenced from the nRF54L15/ nRF54L10 datasheet.

1.1 Features and Benefits

- **Nordic nRF54L15/ nRF54L10** – 6x6 mm QFN48 with 31 GPIOs utilized.
- **Multi-protocol support:** Bluetooth LE, 802.15.4 (Thread & Matter)
- **Cortex M33** processor core: 128 MHz ARM Cortex M33
- **RISC-V** co-processor core: 128 MHz VPR
- **Memory:** 1.5MB non-volatile memory, 256 KB RAM for BL54L15
  1.0MB non-volatile memory, 192 KB RAM for BL54L10
- **High Speed Peripherals**: - HS-SPI/UART, software defined peripherals on 128 MHz VPR, GPIO - 1x 64 MHz Port, 1.7 – 3.5V, 11 GPIOs
- **Low Leakage Peripherals:** 2x QDEC, 7x Timer, Global RTC, 2x WDT, NFC A-Tag, TEMP, I2S, COMP, 3x PWM, LPCOMP, 14-bit 8CH ADC, 5x TWI/SPI/UART, GPIO (2x 16 MHz Port (P0, P1), 20 GPIO's, 1.7-3.5V, 31 GPIO)
- **Antenna choice** – integrated pre-certified **PCB Trace antenna** or external antenna support via **MHF4 connector**
- **Ultra-small footprint** (14 mm x 10 mm x 1.6 mm)
- **Extended** Industrial **Temperature Rating** (-40° to +105 °C)
- **Bluetooth LE**: Channel Sounding, LE 2M, LE Coded, LE Secure Connections & more
- **Qualified against Bluetooth Core 6.0**
- Firmware Over the Air **(FOTA)** via MCUboot and nRF Connect SDK
- **Hostless operation** – Multi Core MCU reduces BOM
- **Fully featured development kits** to jump start Bluetooth LE development
- **BL54L15 and Bl54L10 are 100% drop in options, pin for pin**

1.2 Application Areas

- Building Automation
- Security
- Medical Peripherals
- Industrial Sensors

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2 Specification

2.1 Specification Summary

Categories/Feature	Implementation
Specification	
Bluetooth®	Bluetooth Core 6.0 • Channel Sounding • GATT client & GATT server – Any adopted/custom services • Central/Peripheral roles • Mesh networking • LE CODED • LE 2M • LE Secure Connections • Extended Advertising • LE Power Control • DTM Firmware (Test Modes)
IEEE 802.15.4-2020 PHY	2405–2480 MHz IEEE 802.15.4-2006 radio transceiver, implementing IEEE 802.15.4-2006 compliant • 250kbps, 2450MHz, O-QPSK PHY • Channels 11-26. Channel 11 2405MHz and CH26 2480MHz. • Clear channel assessment (CCA) • Energy detection (ED) scan • CRC generation
Nordic proprietary 1Mbps, 2Mbps, 4Mbps modes radio	2402–2480 MHz Nordic proprietary 1Mbps and 2Mbps modes radio transceiver • 1Mbps nRF proprietary mode (ideal transmitter) • 2Mbps nRF proprietary mode (ideal transmitter) • 4Mbps nRF proprietary mode (ideal transmitter)
Frequency	2.402 - 2.480 GHz for BLE (CH0 to CH39) 2.405 - 2.480 GHz for IEEE 802.15.4-2006 PHY (CH11 to CH26)
Raw Data Rates	1 Mbps BLE (over-the-air) 2 Mbps BLE (over-the-air) 125 kbps BLE (over-the-air) 500 kbps BLE (over-the-air) 250 kbps IEEE 802.15.4-2020 (over-the-air) Nordic proprietary 1Mbps, 2Mbps and 4Mbps modes (over-the-air)
Maximum Transmit Power Setting	+7 dBm — Conducted 453-00001, 453-00225 (Integrated antenna) (Exclude antenna gain) +7 dBm — Conducted 453-00044, 453-00226 (External antenna) (Test at MHF4 connector)
Minimum Transmit Power Setting	-40 dBm
Receive Sensitivity[1] (≤37byte packet for BLE)	BLE 1 Mbps (BER=1E-3) — -94 dBm typical BLE 2 Mbps — -92 dBm typical BLE 125 kbps — -102 dBm typical BLE 500 kbps — -98 dBm typical IEEE 802.15.4-2020 250kbps — TBD dBm typical
Link Budget (conducted)	101 dB @ BLE 1 Mbps (TX power used is 7dBm) 109 dB @ BLE 125 kbps (TX power used is 7dBm)
NFC	
NFC-Type A Listen	**Based on NFC forum specification:** 13.56 MHz, Date rate 106 kbps, NFC Type2 and Type 4 emulation

Note1 Known Noise on channels 2432MHz and 2464MHz degrades receiver sensitivity, in which sensitivity are not within the typical value

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mode compliant	**Modes of Operation:** Disable, Sense, Activated **Use Cases:** Touch-to-Pair with NFC, NFC enabled Out-of-Band Pairing
Security	Designed for PSA Certified Level 3 with Secure Boot, Secure Firmware Update, and Secure Storage. Integrated tamper sensors detect attacks and take action, and cryptographic accelerators are hardened against side-channel attacks.

Host Interfaces and Peripherals	Application Core (High Performance)	Software defined peripheral Core (ultra-low power)
Total		31 x multifunction I/O lines
Two co-processors	Arm Cortex-M33 with DSP, FPU, TrustZone support. 1524KB non-volatile RRAM (BL54L15) 1022KB non-volatile RRAM (BL54L10) 256KB RAM (BL54L15) 192KB RAM (BL54L10) L1 cache 128MHz clock Uses voltage and clock frequency scaling	RISC-V CPU (VPR) fast lightweight peripheral processor (FLPR) dedicated for software defined peripherals 16MHz clock
GPIO		Up to 31 multifunction GPIO's
	64MHz 1.7-3.5V GPIO port P2.00-P2.10	16MHz 1.7-3.5V GPIO port P1.00-P1.14; P0.00-P0.04
ADC (14-bit)	14-bit 31.25KS/s with oversampling 12-bit 250KS/s 10-bit 2MS/s AIN0-AIN7 pins upto 8 programmable gain channels	
Global RTC (GRTC)		Implements full real time clock and calendar as shared system time. Can run in System OFF mode. Ultra low power, 1us resolution, 52bits wide, uses 16MHz clock, 32.76kHz when other power modes.
RTC		2x low power runs off LFCLK
High Speed SPI/UART	1 x	
SPI/UART/TWI		4x
PWM		3x 4channel PWM
I2S		1x I2S (Inter-IC sound interface)
PDM		1x PDM (Pulse code modulation interface) for digital microphones
TIMER		7x Timer (32bit)
QDEC		2x QDEC (Quadrature decoder)
COMP		1x COMP (comparator)
LPCOMP		1x LPCOMP (low power comparator)
TEMP		1x Temperature sensor Temperature range equal to operating temperature range
WDT		2x WDT (Watchdog timer)
NFC A-Tag		1x
Wakeup pins		20x

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Host Interfaces and Peripherals	Application Core (High Performance)	Software defined peripheral Core (ultra-low power)
External optional 32.768 kHz crystal		Not needed for normal radio operation. Optionally, connect +/-20ppm accuracy crystal for more accurate protocol timing. Fit associated load capacitor for crystal or use nRF54L15/nRF54L10 internal load capacitor, which is configurable as 4 pF to 18 pF in 0.5 pF steps on pins XL1, XL2.
Security	Designed for PSA Certified Level 3 with Secure Boot, Secure Firmware Update, and Secure Storage. Integrated tamper sensors detect attacks and take action, and cryptographic accelerators are hardened against side-channel attacks.	

Programmability	**Via SWD (JTAG) 2 wire interface**	
Options	**Nordic nRFConnect SDK:** Software/Support available from Nordic directly https://devzone.nordicsemi.com/ **Canvas SW Suite**: Software/ Support available from https://www.ezurio.com/canvas/software-suite	
FW upgrade	Via SWD (JTAG) 2 wire interface or UART	
Supply Voltage	Normal Voltage Mode (VDD_nRF): 1.7V-3.5V (Internal DCDC convertor or LDO)	
Power Consumption		
Active Modes Peak Current (for max Tx power +7dBm) – Radio only	30 mA peak Tx@ 1.8V, LE1M 25 mA peak Tx@ 1.8V, CW 17 mA peak Tx@ 3.3V, LE1M 14 mA peak Tx@ 3.3V, CW	
Active Modes Peak Current (for Tx power -40dBm) – Radio only	8 mA peak Tx @ 1.8V, LE1M 7 mA peak Tx @ 1.8V, CW 6.5 mA peak Tx @ 3.3V, LE1M 5 mA peak Tx @ 3.3V, CW	
Active Modes Average Current	Depends on many factors.	
Ultra-low Power Modes	System ON Idle	3 uA (System ON IDLE with GRTC (XOSC) and 256 KB RAM) 2.6uA (System ON IDLE with GRTC (XOSC) and 192 KB RAM)
	System OFF	0.6 uA
Antenna Options		
Internal	PCB Trace antenna – on-board (**453-00001 variant for BL54L15, 453-00225 variant for BL54L10)**	
External	Connection via *on module* IPEX MHF4 (**453-00044 variant for BL54L15, 453-00226 variant for BL54L10)**	
Physical		
Dimensions	14mm x 10mm x 1.6mm Pad Pitch – 0.75 mm Pad Type – Three rows of pads (LGA - Land Grid Array).	
Weight	<1 gram	
Environmental		
Operating	-40 °C to +105 °C	
Storage	-40 °C to +105 °C	
Miscellaneous		
Lead Free	Lead-free and RoHS compliant	
Warranty	One-Year Warranty	
Development Tools		
Development Kit	Development kit per module SKU (453-00001-K1 and 453-00044-K1 respectively, BL54L15 only)	

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	Utilise the above development kits for projects planned with BL54L10.
Development Tools	Nordic nRFConnect - Android and iOS applications UART firmware upgrade Xbit Tools and utilities
Bluetooth®	Full Bluetooth SIG Declaration ID
FCC/ISED/CE/MIC/RCM/UKCA/KC	All BL54L15/ BL54L10 Series

3 Hardware Specifications

3.1 Block Diagram and Pin-out

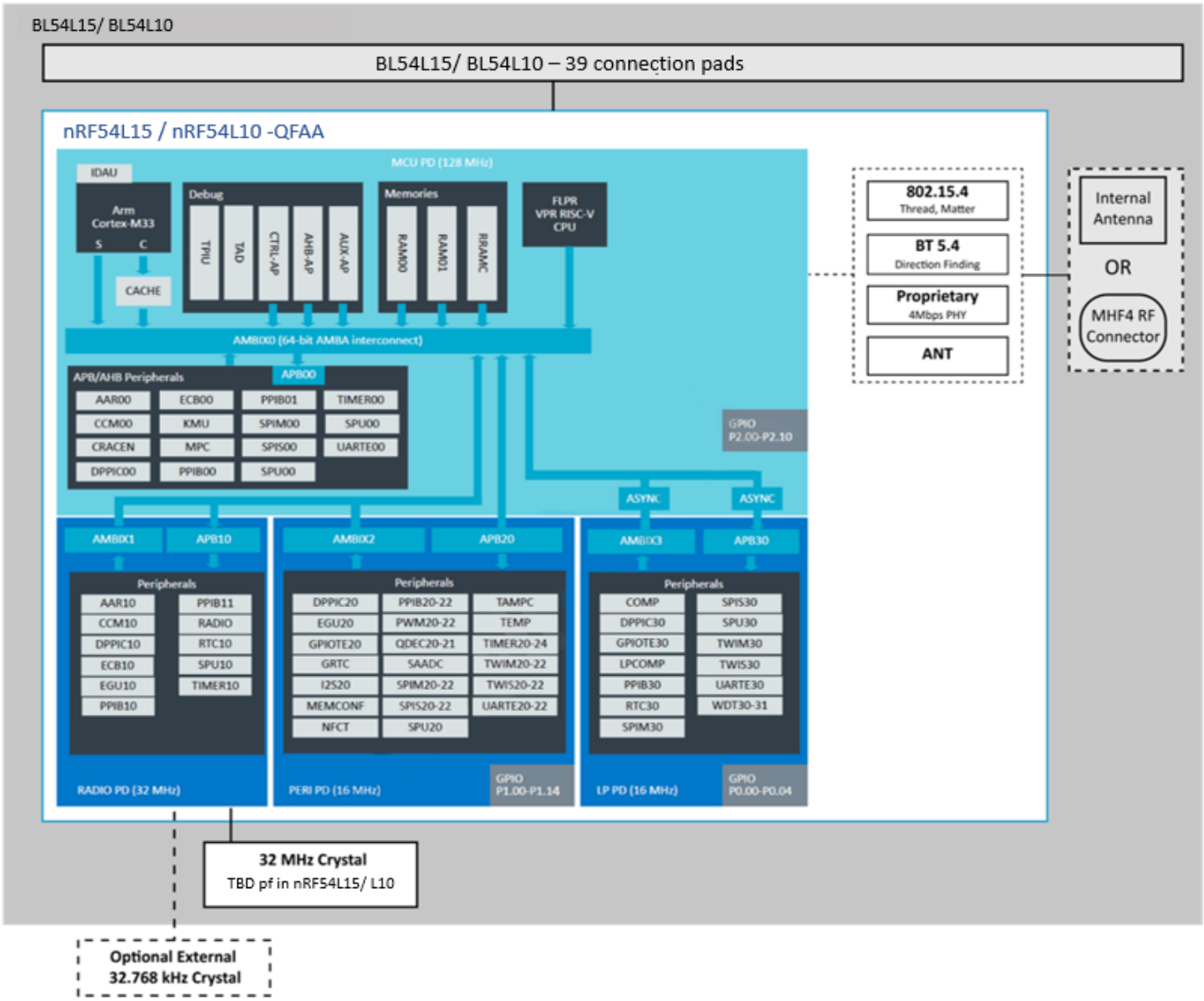


Figure 1: BL54L15/ BL54L10 HW block diagram

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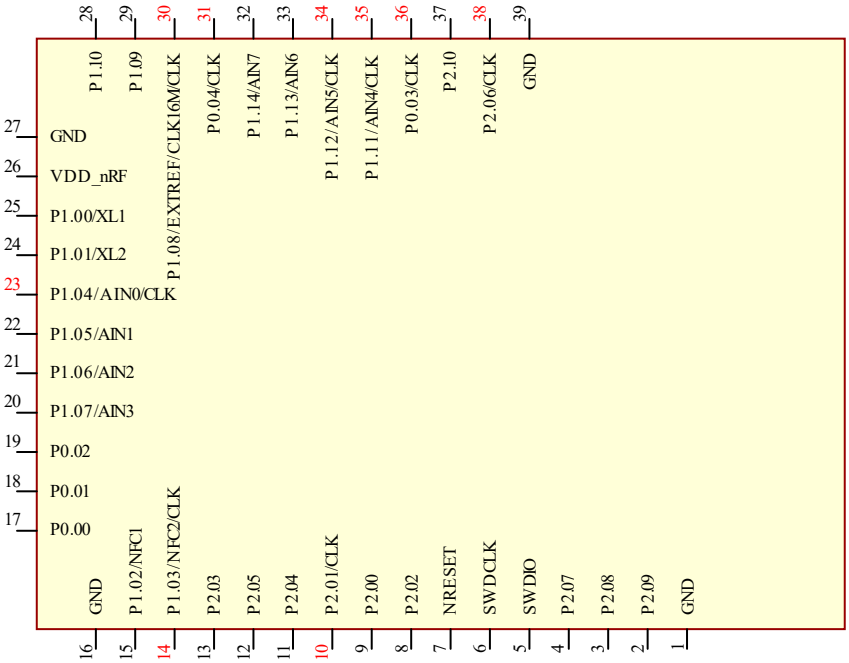


Figure 2: Top view - Schematic symbol for 453-00001/453-00225 BL54L15/L10 Module (Nordic nRF54L15/L10) - Integrated PCB Trace Antenna variant or 453-00044/453-00226 MHF4 RF connector variant

3.2 Pin Definitions

Table 1: Pin definitions

Pin #	Pin Name (red coloured pins for clock for interfaces, trace)	nRF54L15 nRF54L10 QFN48 Pin	nRF54L15/ nRF54L10 QFN48 Name	Description	Example usage
1	GND	-	VSS		
2	P2.09	20	P2.09/TRACEDATA[2]/SPI.SDI/SDO	General purpose I/O Trace data SPIM SDI SPIS SDI UARTE CTS	 Trace SPIM00/SPIM21 SPIS00/SPIS21 UARTE00/UARTE21
3	P2.08	19	P2.08/TRACEDATA[1]/SPI.SDI/SDO	General purpose I/O Trace data SPIM SDO SPIS SDO UARTE TXD	 Trace SPIM00/SPIM21 SPIS00/SPIS21 UARTE00/UARTE21
4	P2.07	18	P2.07/TRACEDATA[0]/SWO/SPI.DCX	General purpose I/O Trace data Serial wire output (SWO) SPIM DCX UARTE RXD	 Trace Trace SPIM00/SPIM21 UARTE00/UARTE21
5	SWDIO	25	SWDIO	Serial Wire Debug IO for debug and programming	
6	SWDCLK	26	SWDCLK	Serial Wire Debug clock input for debug and programming	
7	NRESET	30	nRESET	Pin RESET with internal pull-up resistor (13k Ohms). System Reset (Active Low).	

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Pin #	Pin Name (red coloured pins for clock for interfaces, trace)	nRF54L15 nRF54L10 QFN48 Pin	nRF54L15/ nRF54L10 QFN48 Name	Description	Example usage
8	P2.02	13	P2.02/SPI.SDI/SDO	General purpose I/O SPIM SDO SPIS SDO UARTE TXD QSPI D0 Serial wire output (SWO)	 SPIM00/SPIM20 SPIS00/SPIS20 UARTE00/UARTE20 FLPR Trace
9	P2.00	11	P2.00/SPI.DCX	General purpose I/O SPIM DCX UARTE RXD QSPI D3	 SPIM00/SPIM20 UARTE00/UARTE20 FLPR (QSPI)
10	P2.01/CLK	12	P2.01/SPI.SCK	General purpose I/O SPIM SCK SPIS SCK QSPI SCK	Clock pin SPIM00/SPIM20 SPIS00/SPIS20 FLPR
11	P2.04	15	P2.04/SPI.SDI/SDO	General purpose I/O SPIM SDI SPIS SDI UARTE CTS QSPI D1	 SPIM00/SPIM20 SPIS00/SPIS20 UARTE00/UARTE20 FLPR
12	P2.05	16	P2.05/SPI.CS	General purpose I/O SPIM CS UARTE RTS QSPI CS	 SPIM00/SPIM20 UARTE00/UARTE20 FLPR
13	P2.03	14	P2.03	General purpose I/O QSPI D2	 FLPR
14	P1.03/NFC2/CLK	4	P1.03/NFC2	General purpose I/O Dedicated pin for NFC input	Clock pin
15	P1.02/NFC1	3	P1.02/NFC1	General purpose I/O Dedicated pin for NFC input	
16	GND				
17	P0.00	23	P0.00	General purpose I/O	
18	P0.01	24	P0.01	General purpose I/O	
19	P0.02	27	P0.02	General purpose I/O	
20	P1.07/AIN3	8	P1.07/AIN3/TAMPC	General purpose I/O TAMPC active shield 1 input Analog input	 TAMPC
21	P1.06/AIN2	7	P1.06/AIN2/TAMPC	General purpose I/O TAMPC active shield 1 output Analog input	 TAMPC

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Pin #	Pin Name (red coloured pins for clock for interfaces, trace)	nRF54L15 nRF54L10 QFN48 Pin	nRF54L15/ nRF54L10 QFN48 Name	Description	Example usage
22	P1.05/AIN1	6	P1.05/AIN1/TAMPC	General purpose I/O TAMPC active shield 0 input RADIO DFEGPIO Analog input	TAMPC RADIO
23	P1.04/AIN0/CLK	5	P1.04/AIN0/TAMPC	General purpose I/O TAMPC active shield 0 output Analog input	Clock pin TAMPC
24	P1.01/XL2	2	P1.01/XL2	General purpose I/O General purpose I/O Connection for 32.768kHz crystal	Ezurio Devkit: Optional 32.768kHz crystal pad XL2, XL1 and associated 9pF load capacitor inside nRF54L15 chipset.
25	P1.00/XL1	1	P1.00/XL1	General purpose I/O Connection for 32.768kHz crystal	Ezurio Devkit: Optional 32.768kHz crystal pad XL2, XL1 and associated 9pF load capacitor inside nRF54L15 chipset.
26	VDD_nRF	48	VDD	1.7V-3.5V input for Normal Voltage Mode where connect external supply to VDD_nRF(pin26). See 3.5 BL54L15/ BL54L10 Power Supply	
27	GND				
28	P1.10	38	P1.10/TAMPC	General purpose I/O TAMPC active shield 2 input RADIO DFEGPIO	TAMPC RADIO
29	P1.09	37	P1.09/TAMPC	General purpose I/O TAMPC active shield 2 output RADIO DFEGPIOO	TAMPC RADIO
30	P1.08/EXTREF/CLK16M/ CLK	9	P1.08/CLK16M/TAMPC	General purpose I/O GRTC HF clock output External reference for SAADC	Clock pin
31	P0.04/CLK	29	P0.04/GRTC_CLKOUT32K	General purpose I/O GRTC LF clock output	Clock pin GRTC
32	P1.14/AIN7	42	P1.14/AIN7	General purpose I/O RADIO DFEGPIO Analog input	RADIO
33	P1.13/AIN6	41	P1.13/AIN6	General purpose I/O RADIO DFEGPIO Analog input	RADIO

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Pin #	Pin Name (red coloured pins for clock for interfaces, trace)	nRF54L15 nRF54L10 QFN48 Pin	nRF54L15/ nRF54L10 QFN48 Name	Description	Example usage
34	P1.12/AIN5/CLK	40	P1.12/AIN5	General purpose I/O TAMPC active shield 3 input RADIO DFEGPIO Analog input	Clock pin TAMPC RADIO
35	P1.11/AIN4/CLK	39	P1.11/AIN4	General purpose I/O TAMPC active shield 3 output RADIO DFEGPIO Analog input	Clock pin TAMPC RADIO
36	P0.03/CLK	28	P0.03/GRTC_PWMOUT	General purpose I/O GRTC PWM output	Clock pin GRTC
37	P2.10	21	P2.10/TRACEDATA[3]/SPIM.CS	General purpose I/O Trace SPIM CS UARTE RTS	 Trace SPIM00/SPIM21 UARTE00/UARTE21
38	P2.06/CLK	17	P2.06/TRACECLK/SPI.SCK	General purpose I/O SPIM SCK SPIS SCK Trace clock	Clock pin SPIM00/SPIM21 SPIS00/SPIS21 Trace
39	GND				

Pin Definition Notes:

Note 1 GPIO

GPIO = General Input or Output (GPIO level voltage tracks VDD pin). AIN =Analog input.
If GPIO is selected as an input, ensure the input is not floating (which can cause current consumption to drive with time in low power modes (such as System ON Idle), by selecting the internal pull up or pull down.
Must connect all GND pads to host board PCB GND plane.

Note2 Clock for serial interfaces or trace

Some peripherals (SPI, TWI, PDM, I2S, TRACE, GRTC) have clock signals. Dedicated clock pins have been optimized to ensure correct timing relationship between clock and data signal for these peripherals. Pins that can be used as clock signals are shown with pin name in red colour.

The peripheral data signal must be configured to use pins close to the clock pin. This ensures that the internal paths from the peripheral to the pin have the same delay, so that the data and clock signals reach the pins at the same time.

For high-speed signals, the printed circuit board (PCB) layout must use short PCB traces of identical length. This makes sure any delays are kept to a minimum and it assures close to identical delay and clock path.

Note 3 Dedicated pins

UARTE20/21: Can use any pin son GPIO port P1. Can be connected across power domains to dedicated pin on P2.
SPIM00: Has dedicated pins on GPIO port P2. For 32MHz operation, the pins must be configured using extra high drive E0/E1 configuration.
SPIM20/21: Can use any pin son GPIO port P1. Can be connected across power domains to dedicated pin on P2.
SPIS20/21: Can use any pin son GPIO port P1. Can be connected across power domains to dedicated pin on P2.
TRACE: Has dedicated pins on GPIO port P2. For 32MHz operation, the pins must be configured using extra high drive E0/E1 configuration.
GRTC: Has dedicated pins for clock and PWM output.
TAMPC: Has dedicated pins for active shield inputs and outputs.
FLPR: Uses dedicated pins on GPIO port P2 for emulated peripherals such as QSPI.
RADIO: Uses dedicated pins on GPIO port P1 for antenna switch control (DFEGPIO for direction finding).
NFC: Uses dedicated pins listed in pin definitions table1.

Note 4 SWDIO / SWCLK / nRESET / VDD / GND

Customer MUST bring out SWDIO, SWCLK, nRESET, VDD, GND for programming purposes.

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3.3 Electrical Specifications

3.3.1 Absolute Maximum Ratings

Absolute maximum ratings are the extreme limits for supply voltage and voltages on digital and analogue pins of the module are listed below; exceeding these values causes permanent damage.

Table 2: Absolute maximum ratings

Parameter	Min	Max	Unit
Supply Voltages			
VDD_nRF	-0.3	3.6	V
I/O pin voltage			
Voltage at GPIO pin (at VDD≤3.5V)	-0.3	VDD_nRF + 0.3	V
Voltage at GPIO pin (at VDD>3.5V)		3.6	V
NFC antenna pin current (NFC1/2)	-	130	mA
Environmental			
Storage temperature	-40	+105	°C
MSL (Moisture Sensitivity Level)	-	4	-
ESD (as per EN301-489) Conductive Air Coupling		 4 8	 kV kV
Flash Memory (Endurance) (Note 2)	10,000		Write/erase cycles
Flash Memory (Retention)	10 years at 85°C 2 years at 105°C		years at TBD °C

Absolute maximum Ratings Notes:	
Note 1	The absolute maximum rating for VDD pin (max) is 3.6 V for the BL54L15.
Note 2	Wear levelling can be implemented by customer.

3.3.2 Recommended Operating Parameters

Table 3: Power supply operating parameters

Parameter	Min	Typ	Max	Unit
VDD_nRF (independent of DCDC) supply range	1.7		3.5	V
VDD_nRF_{ext} (**VDD_nRF** supply voltage under extended operating temperature)	1.7		3.3	V
VDD_nRF Maximum ripple or noise (See Note 1)	-	-	10	mV
Operating Temperature Range	-40	+25	+85	°C
Extended operating temperature	85		105	°C

Recommended Operating Parameters Notes:	
Note 1	This is the maximum VDD_nRF ripple or noise (at any frequency) that does not disturb the radio.
Note 2	The on-board power-on reset circuitry may not function properly for rise times longer than the specified maximum.
Note 3	Some electrical parameters are valid only for the operating temperature range conditions. When this is the case, an additional parameter for the extended operating temperature condition is provided.

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3.4 Clocks

3.4.1 HFXO - 32MHz crystal oscillator and nRF54L15/nRF54L10 internal load capacitor mandatory setting

The BL54L15/BL54L10 module contains the 32 MHz crystal, but the load capacitors to create 32MHz crystal oscillator circuit are inside the nRF54L15/nRF54L10 chipset. Customer can set the internal nRF54L15/nRF54L10 capacitors from 4 pF to 17 pF in 0.25pF if needed or use default value without changing.

The 32 MHz crystal inside the BL54L15/BL54L10 module is a high accuracy crystal (±15 ppm at room temperature) that helps with radio operation and reducing power consumption in the active modes.

3.4.2 LFCLK – Low Frequency clock source

There are four possibilities (see figure 5) for the low frequency clock (LFCLK) and options are:

LFRC (32.768kHz RC oscillator): The Internal 32.768 kHz RC oscillator (LFRC) is fully embedded in nRF54L15/nRF54L10 (and does not require additional external components) with an accuracy ±250 ppm (after calibration of LFRC at least every eight seconds using the HFXO as a reference oscillator).

LFXO (32.768kHz crystal oscillator): For higher LFCLK accuracy (greater than ±250ppm accuracy is required), the low frequency crystal oscillator (LFXO) must be used. To use LFXO, a 32.768kHz crystal must be connected between the XL1 and XL2 pins and the load capacitance between each crustal terminal and ground. Optionally internal (to nRF54L15/nRF54L10) capacitor of maximum 18 pF in 0.5 pF steps are provided on pins XL1 and XL2.

Low frequency (32.768 kHz) external source: The 32.768 kHz oscillator (LFXO) is designed to work with external sources

LFSYNTH (32.768kHz Synthesised clock) from HFCLK (LFSYNTH): The LFCLK can be synthesised from the HFCLK source. LFSYNTH depends on the HFCLK to run. The accuracy of the LFCLK clock with LFSYNTH as a source assumes the accuracy of the HFCLK. If high accuracy is required, the HFCLK must generated from the HFXO. Using the LFSYNT clock removes the requirement for an external 32.768kHz crystal but the increases the average power consumption as the HFCLK will turned on in the system.

3.4.3 Other Internal Clocks

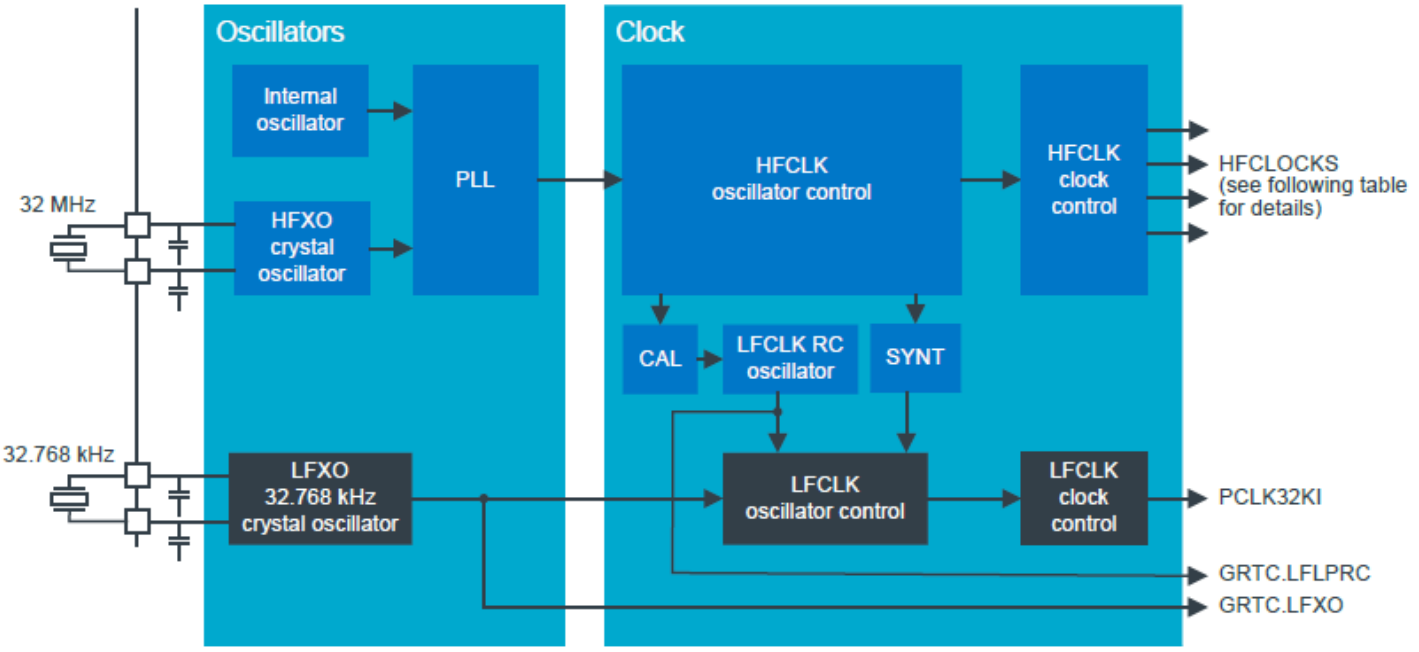


Figure 3: nRF54L15/nRF54L10 Clock System Overview (adapted from Nordic)

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3.5 BL54L15/ BL54L10 Power Supply

Normal voltage mode power supply mode is entered when the external supply voltage (1.7V-3.5V) is connected to both VDD_nRF pin (pin26). See Figure 4.

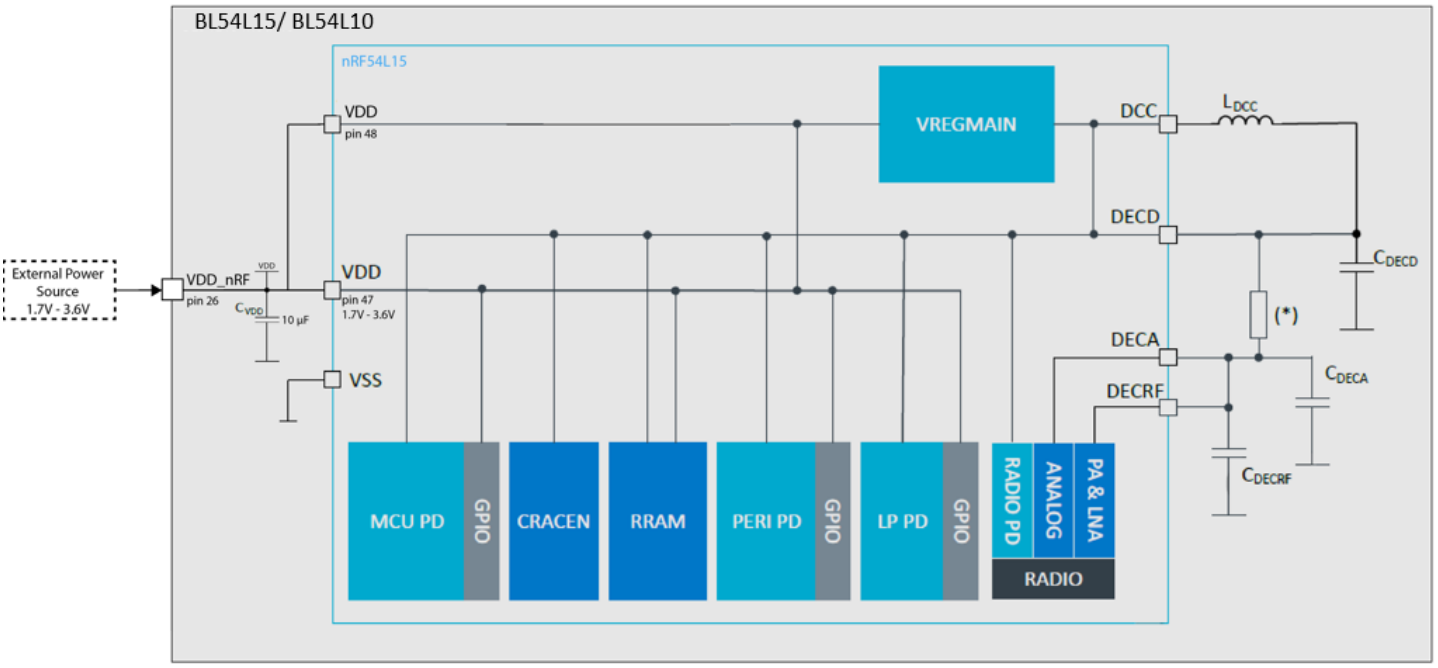


Figure 4: Normal Voltage Mode

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4 Programmability

4.1 BL54L15/ BL54L10 Default Firmware

The BL54L15/BL54L10 module is shipped from Ezurio manufacturing facilities with no firmware programmed.

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4.2 BL54L15/ BL54L10 Firmware Options

Firmware for use with the BL54L15/BL54L10 can be divided into the following types.

- **Bootloader** – This is the application that resides on the Application Core used to perform firmware updates of the Application and FLPR cores.

  The MCU Boot or Trusted Firmware M Bootloaders are recommended to be used as the basis for the BL54L15 Bootloader functionality.

- **Application** – This is the main application running on the Application core. In interfaces with the integrated radio stack(s) and provides supplementary functionality in addition to the time critical activities performed for radio activity.

- **Software Defined Peripheral** – This is the application running on the RISC-V FLPR core.

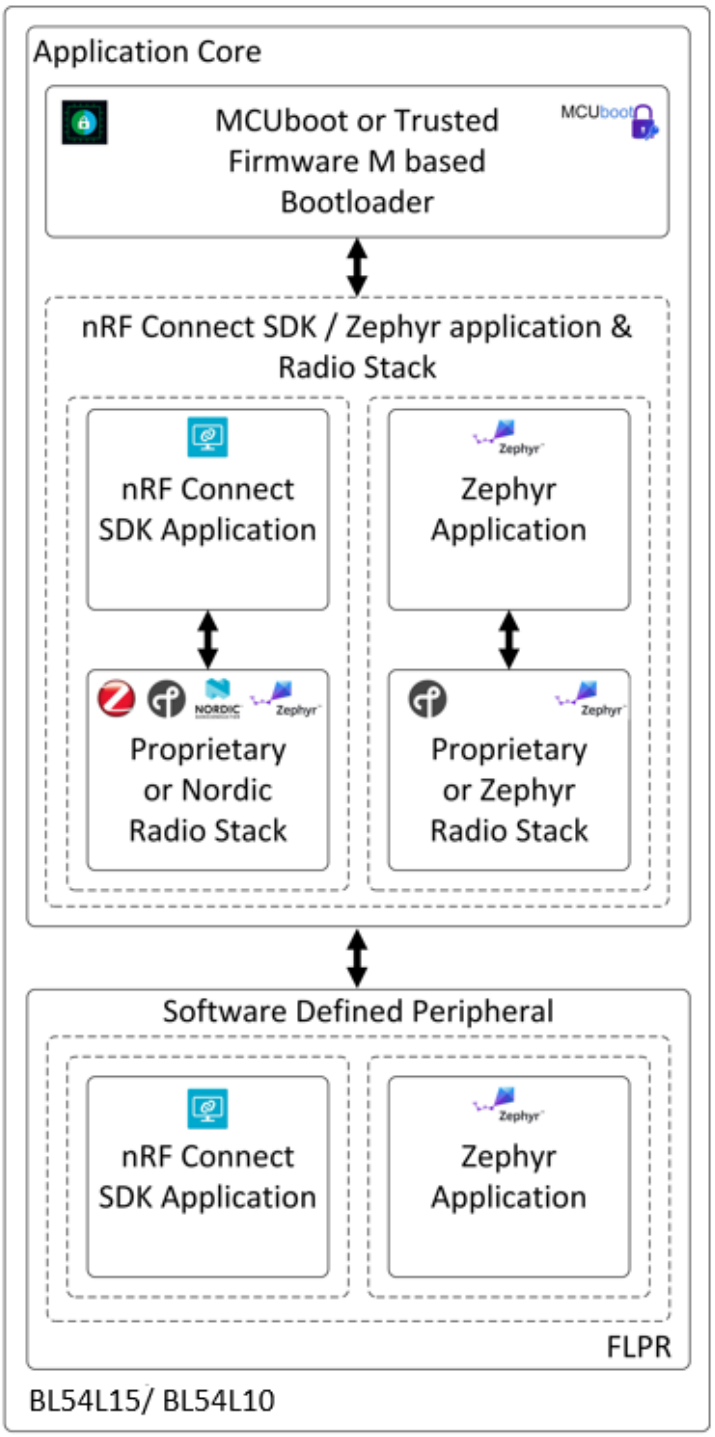


Figure 5 : Functional SW block diagram for BL54L15/BL54L10 series module

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5 Peripherals

Feature		Module	
		BL54L15	BL54L10
		nRF54L15-QFAA	nRF54L10-QFAA
Memory	Non-volatile memory (RRAM)	1524 KB	1022 KB
	Random access memory (RAM)	256 KB	192 KB
Radio	Bluetooth Low Energy	Yes	
	Bluetooth Low Energy Coded PHY (Long range)	Yes	
	Bluetooth Constant Tone Extension (Direction-finding)	Yes	
	IEEE 802.15.4	Yes	
GPIO pins	GPIO pins	31	
	Wakeup-pins	20	
	Analog input pins	8	
	GPIO voltage	VDD (1.7V-3.5V)	
Peripherals	Timers (TIMER)	7	
	Real-time counter (RTC)	2	
	Global real-time counter (GRTC)	Yes	
	Serial interfaces (UART, SPI, TWI)	5	
	Temperature sensor	Yes	
	Comparator (COMP)	Yes	
	Analog-to-digital converter (ADC)	Yes	
	Quadrature decoder (QDEC)	2	
	Inter-IC sound interface (I2S)	2	
	Near-field communication (NFC)	Yes	
	Pulse density modulation interface (PDM)	2	
	Pulse-width modulator (PWM)	3	
	Watchdog timer (WDT)	2	
Security	Active tamper shield pin pairs (in/out)	4	
	Glitch detectors	Yes	
	Key management unit	Yes	
	Encryption accelerator	Yes	
Debug	ITM parallel trace	Yes	

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6 SW requirements related to hardware

6.1 32MHz crystal internal load capacitor setting

BL54L15/ BL54L10 module contains the 32 MHz crystal but the load capacitors to create 32 MHz crystal oscillator circuit are inside the nRF54L15/ nRF54L10 chipset. Customer can set the internal nRF54L15/nRF54L10 capacitors from 4 pF to 17 pF in 0.25pF if needed, or use default value without changing.

7 Hardware Integration Suggestions

7.1 Circuit

The BL54L15/ BL54L10 is easy to integrate, requiring one mandatory external 10uF capacitor on customers board and apart from that those components which customer require for development and in your end application.

The following are suggestions for your design for the best performance and functionality.

Checklist (for Schematic):

- **BL54L15/ BL54L10 power supply:**

  Normal voltage mode power supply mode is entered when the external supply voltage (1.7V-3.5V) is connected to both VDD_nRF pin (pin26).

  External power source should be within the operating range, rise time and noise/ripple specification of the BL54L15/ BL54L10. Add decoupling capacitors for filtering the external source. Power-on reset circuitry within BL54L15/ BL54L10 series module incorporates brown-out detector, thus simplifying your power supply design. Upon application of power, the internal power-on reset ensures that the module starts correctly.

- **AIN (ADC) and GPIO pin IO voltage levels**
  BL54L15/BL54L10 GPIO voltage levels are at VDD_nRF. Ensure input voltage levels into GPIO pins are at VDD_nRF also. Ensure ADC pin maximum input voltage for damage is not violated.

- **AIN (ADC) impedance and external voltage divider setup**
  If you need to measure with ADC a voltage higher than 3.5V, you can connect a high impedance voltage divider to lower the voltage to the ADC input pin.

- **SWD**
  This is REQUIRED for loading firmware. MUST wire out the SWD two wire interface on host design. Five lines should be wired out, namely SWDIO, SWDCLK, nRESET, GND and VDD.

- **UART and flow control (CTS, RTS)**
  Required if customer requires UART.

- **TWI (I2C)**
  It is essential to remember that pull-up resistors on both SCL and SDA lines are required, the value as per I2C standard. nRF54L15/ nRF54L10 can provide 13K Ohms typical pull up values internally. For other values, fit external pull-up resistor on both SCL and SDA as per I2C specification to set speed. The I2C specification allows a line capacitance of 400pF.

- **QSPI, High Speed SPI, High speed TWI (I2C, 1Mbps) and Trace**
  High-Speed SPI, TWI and Trace come on dedicated GPIO pins only. Other lower speed SPI and TWI can come out on any GPIO pins.
  For all high-speed signal, the printed circuit board (PCB) layout must ensure that connections are made using short PCB traces.

- **GPIO pins**
  If GPIO is selected as an input, ensure the input is not floating (which can cause current consumption to drive with time in low power modes (such as System ON Idle), by selecting the internal pull up or pull down.

- **NFC antenna connector**
- To make use of the Ezurio flexi-PCB NFC antenna (part # 0600-00061), fit connector:
  - Description – FFC/FPC Connector, Right Angle, SMD/90d, Dual Contact,1.2 mm Mated Height
  - Manufacturer – Molex
  - Manufacturers Part number – 512810594

  Add tuning capacitors of 300 pF on NFC1 pin to GND and 300 pF on NFC2 pins to GND if the PCB track length is similar as development board.

- **nRESET pin (active low)**
  Hardware reset. Wire out to push button or drive by host.

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By default module is out of reset when power applied to VDD_nRF pins (13K pull-up inside BL54L15/ BL54L10 (nRF54L15-QFAA/nRF54L10-QFAA)).

- **Optional External 32.768kHz crystal**

  If the optional external 32.768kHz crystal is needed, then use a crystal that meets specification and add load capacitors (either inside nRF54L15-QFAA/nRF54L10-QFAA or discrete capacitors outside BL54L15/BL54L10 (nRF54L15-QFAA/nRF54L10-QFAA) whose values should be tuned to meet all specification for frequency and oscillation margin.

7.2 PCB Layout on Host PCB - General

Checklist (for PCB):

- MUST locate BL54L15/ BL54L10 module close to the edge of PCB (mandatory for the 453-00001/453-00225 for on-board PCB trace antenna to radiate properly).
- Use solid GND plane on inner layer (for best EMC and RF performance).
- All module GND pins MUST be connected to host PCB GND.
- Place GND vias close to module GND pads as possible.
- Unused PCB area on surface layer can flooded with copper but place GND vias regularly to connect the copper flood to the inner GND plane. If GND flood copper is on the bottom of the module, then connect it with GND vias to the inner GND plane.
- Route traces to avoid noise being picked up on VDD_nRF supply and AIN (analogue), GPIO (digital) traces and high-speed traces.
- Ensure no exposed copper is on the underside of the module (refer to land pattern of BL54L15/BL54L10 development board).

7.3 PCB Layout on Host PCB for the 453-00001 and 453-00225

7.3.1 Antenna Keep-out on Host PCB

The 453-00001/453-00225 has an integrated PCB trace antenna and its performance is sensitive to host PCB. It is critical to locate the 453-00001/453-00225 on the edge of the host PCB (or corner) to allow the antenna to radiate properly. Refer to guidelines in section ***PCB land pattern and antenna keep-out area for the 453-00001/453-00225***. Some of those guidelines repeated below.

- Ensure there is no copper in the antenna keep-out area on any layers of the host PCB. Keep all mounting hardware and metal clear of the area to allow proper antenna radiation.
- For best antenna performance, place the 453-00001/453-00225 module on the edge of the host PCB, preferably in the edge center.
- The BL54L15 development board (453-00001-K1) has the 453-00001 module on the edge of the board (not in the corner). The antenna keep-out area is defined by the BL54L15 development board which was used for module development and antenna performance evaluation is shown in Figure 6, where the antenna keep-out area is ~5mm wide, ~28.6mm long; with PCB dielectric (no copper) height ~1.57mm sitting under the 453-00001 PCB trace antenna module. Bl54L10 module (453-00225) please follow the same design of BL54L15.
- The 453-00001 PCB trace antenna is tuned when the 453-00001 is sitting on development board (host PCB) with size of 113 mm x 63.5 mm x 1.6mm.
- A different host PCB thickness dielectric will have small effect on antenna.
- The antenna-keep-out defined in the 8.2 Host PCB Land Pattern and Antenna Keep-out for the 453-00001 and 453-00225 section.
- Host PCB land pattern and antenna keep-out for the BL54L15/BL54L10 applies when the 453-00001/453-00225 is placed in the edge of the host PCB preferably in the edge center. **Error! Reference source not found.** shows an example.

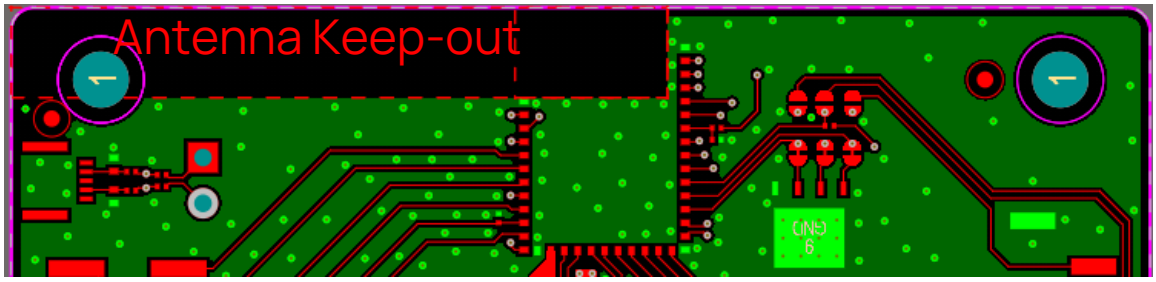


Figure 6 : PCB trace Antenna keep-out area (shown in red), corner of the BL54L15 development board for the 453-00001 module.

Antenna Keep-out Notes:	
Note 1	The BL54L15/BL54L10 module is placed on the edge, preferably edge centre of the host PCB.
Note 2	Copper cut-away on all layers in the *Antenna Keep-out* area under the 453-00001/453-00225 on host PCB.

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7.3.2 Antenna Keep-out and Proximity to Metal or Plastic

Checklist (for metal /plastic enclosure):

- Minimum safe distance for metals without seriously compromising the antenna (tuning) is 40 mm top/bottom and 30 mm left or right.
- Metal close to the 453-00001/453-00225 PCB trace monopole antenna (bottom, top, left, right, any direction) will have degradation on the antenna performance. The amount of that degradation is entirely system dependent, meaning you will need to perform some testing with your host application.
- Any metal closer than 20 mm will begin to significantly degrade performance (S11, gain, radiation efficiency).
- It is best that you test the range with a mock-up (or actual prototype) of the product to assess effects of enclosure height (and materials, whether metal or plastic) and host PCB ground (GND plane size).

7.4 External Antenna Integration with BL54L15/BL54L10 MHF4 variant (453-00044/453-00226)

Please refer to the regulatory sections for FCC, ISED, CE, MIC, UKCA and RCM details of use of BL54L15 with external antennas in each regulatory region.

The BL54L15/BL54L10 family has been designed to operate with the below external antennas (with a maximum gain of 2.32 dBi). The required antenna impedance is 50 ohms. See Table 4. External antennas improve radiation efficiency.

Table 4: External antennas for the BL54L15/BL54L10 RF trace pin variant module (453-00044/453-00226)

Manufacturer	Model	Ezurio Part Number	Type	Connector	Peak Gain	
					2400-2500 MHz	2400-2480 MHz
Ezurio (Laird Connectivity)	NanoBlue	EBL2400A1-10MH4L	PCB Dipole	IPEX MHF4	2 dBi	-
Ezurio (Laird Connectivity)	FlexPIFA	001-0022	PIFA	IPEX MHF4	-	2 dBi
Mag.Layers	EDA-8709-2G4C1-B27-CY	0600-00057	Dipole	IPEX MHF4	2.32 dBi	-
Ezurio (Laird Connectivity)	mFlexPIFA	EFA2400A3S-10MH4L	PIFA	IPEX MHF4	-	2 dBi
Ezurio (Laird Connectivity)	iFlexPIFA Mini	EFG2401A3S-10MH4L	PIFA	IPEX MHF4	-	2 dBi
Ezurio (Laird Connectivity)	Ezurio NFC	0600-00061	NFC	N/A	-	-

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8 Mechanical Details

8.1 BL54L15/BL54L10 Mechanical Details

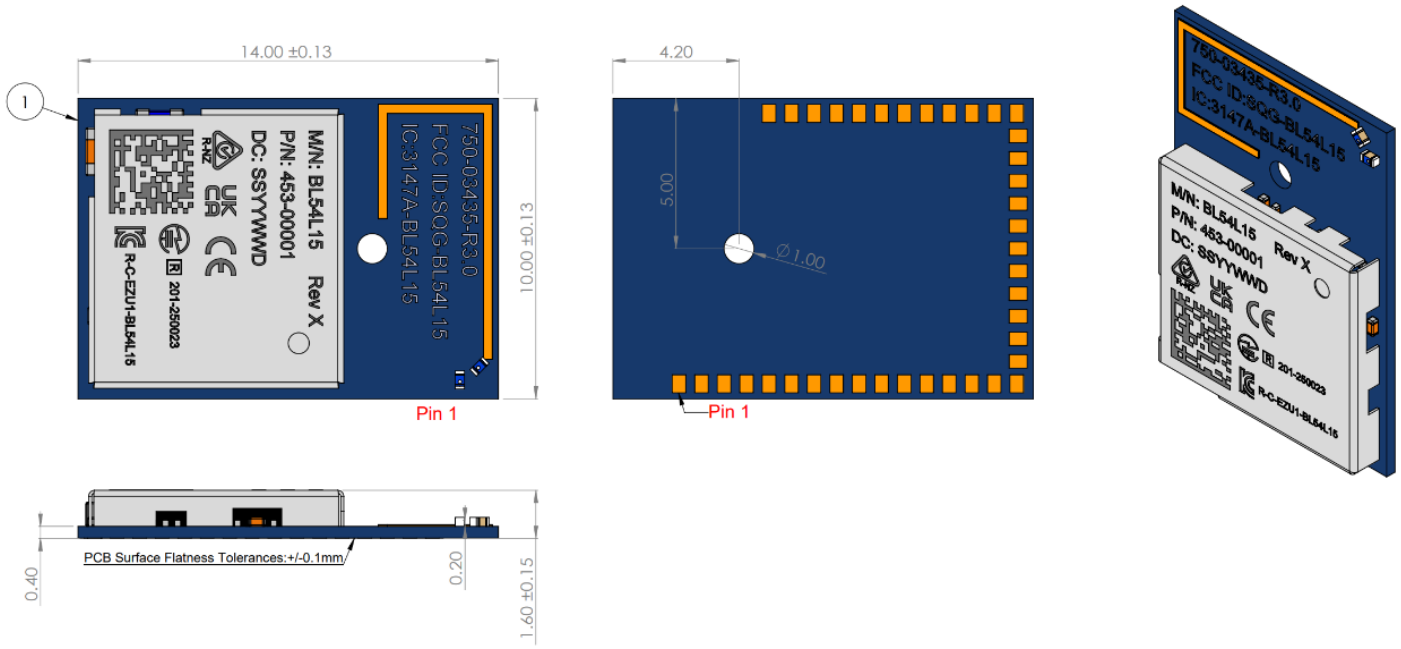


Figure 7 : Mechanical Details – Internal Antenna variant module (453-00001)

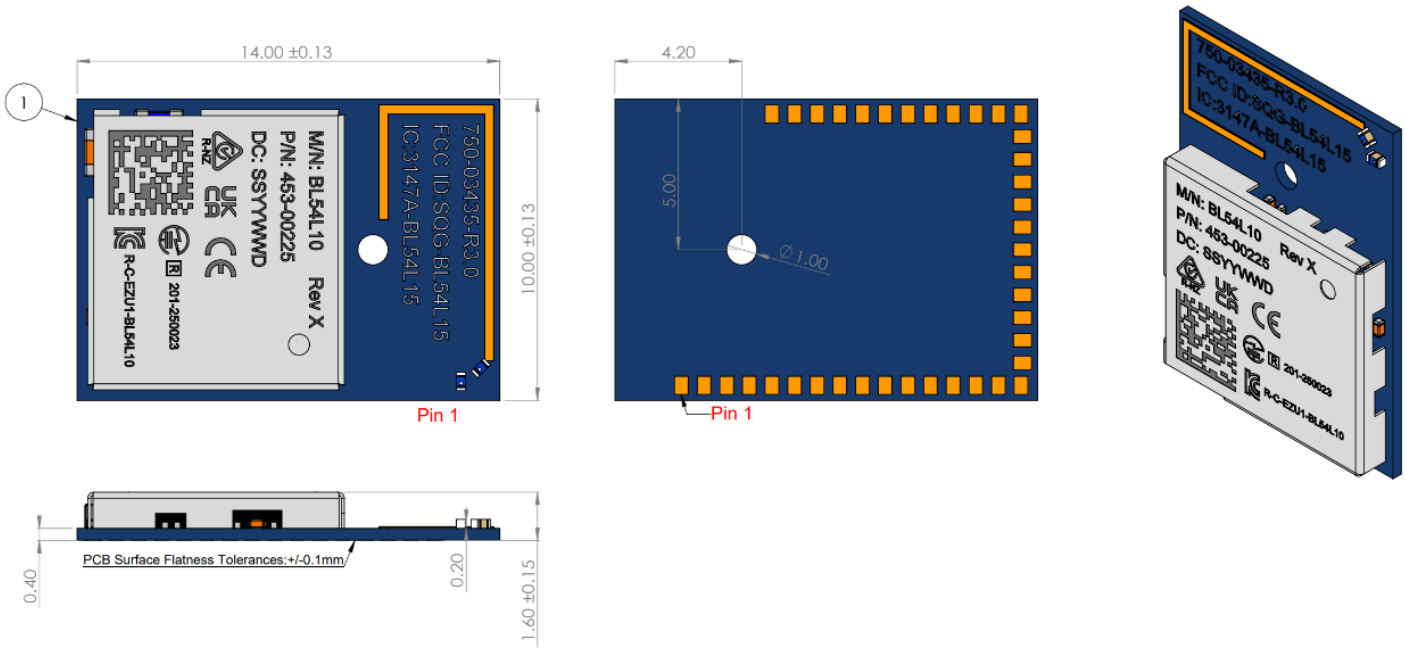


Figure 8 : Mechanical Details – Internal Antenna variant module (453-00225)

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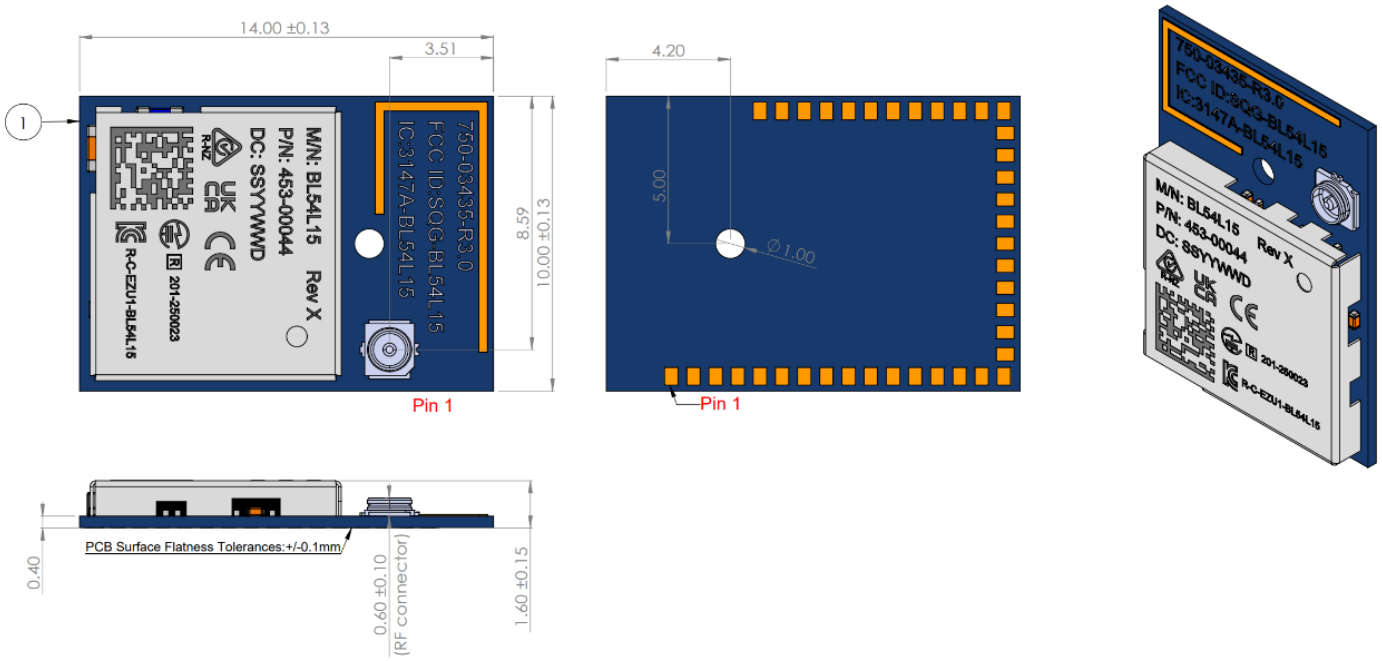


Figure 9 : Mechanical Details – MHF4 RF connector variant module (453-00044)

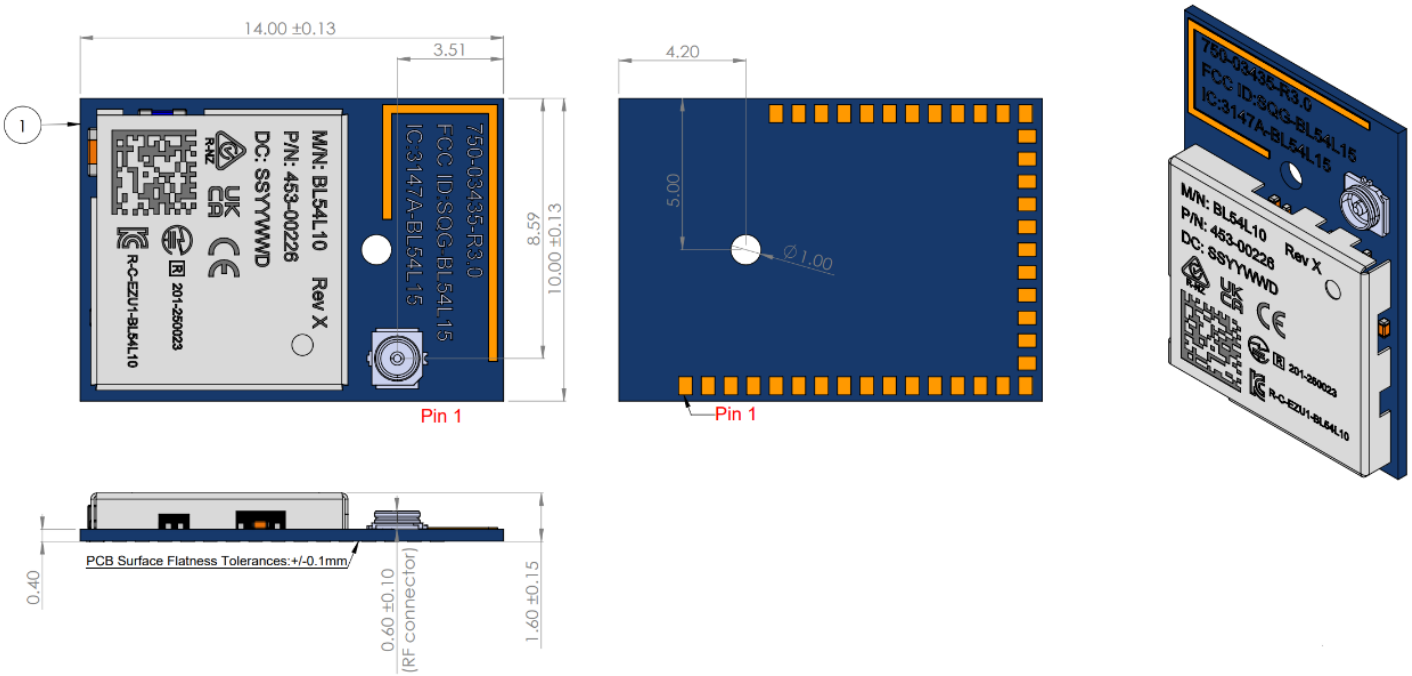


Figure 10 : Mechanical Details – MHF4 RF connector variant module (453-00226)

3D models for BL54L15 Module, MHF4 (453-00044) and BL54L15 Module, Trace Antenna (453-00001) on the BL54L15 product page – https://www.ezurio.com/product/bl54l15-series-bluetooth-le-80215-4-nfc

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8.2 Host PCB Land Pattern and Antenna Keep-out for the 453-00001 and 453-00225

PCB footprint - BL54L15 (DXF and Altium format) and SCH Symbol - BL54L15 (Altium format) can be found on the BL54L15 product page – https://www.ezurio.com/product/bl54l15-series-bluetooth-le-80215-4-nfc

BL54L10 use the same footprint of BL54L15

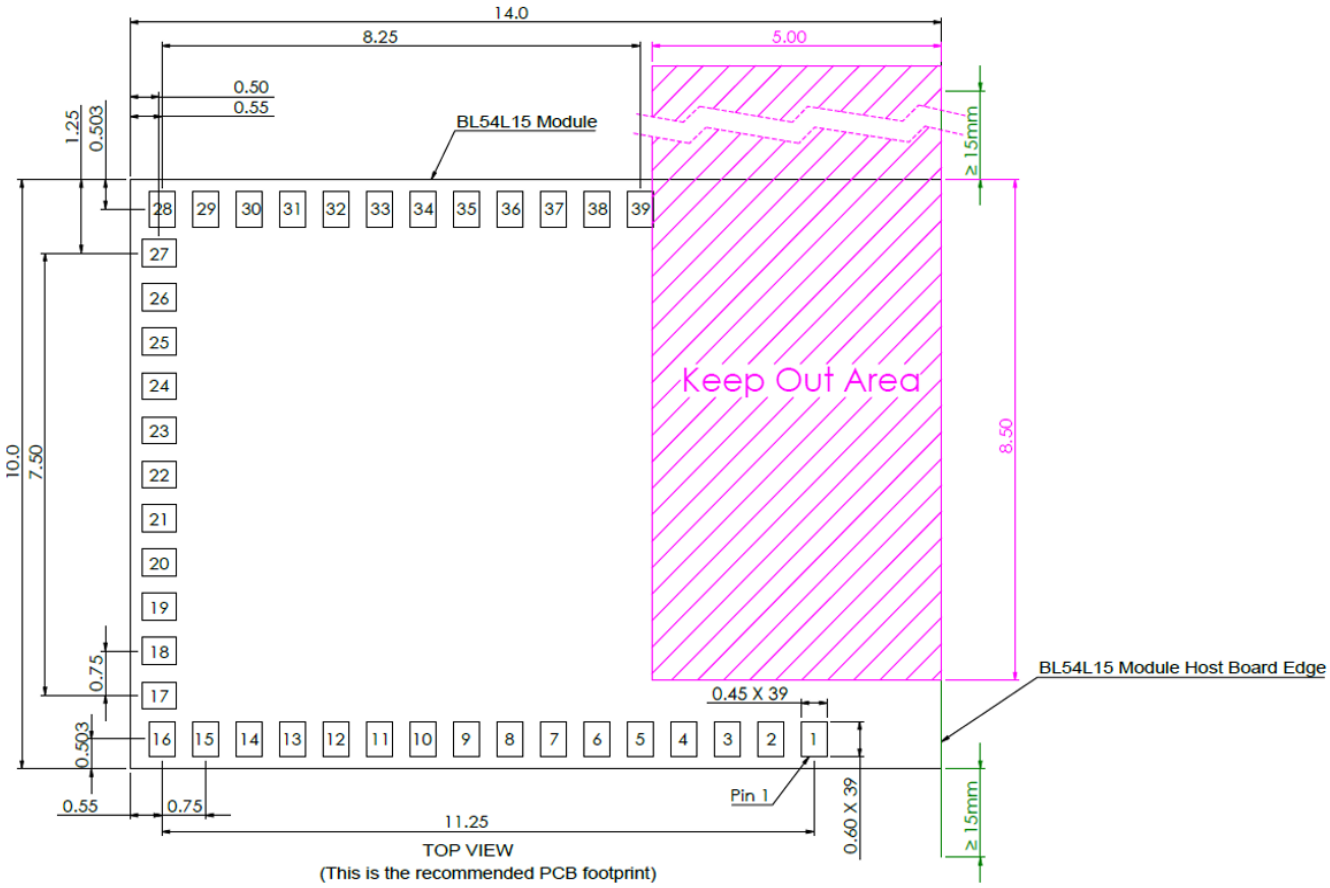


Figure 11 : Land pattern and Keep-out for the 453-00001 and 453-00225

All dimensions are in mm.

Host PCB Land Pattern and Antenna Keep-out for the 453-000xx Notes:	
Note 1	Ensure there is no copper in the antenna 'keep out area' on any layers of the host PCB. Also keep all mounting hardware or any metal clear of the area (Refer to 7.3.2) to reduce effects of proximity detuning the antenna and to help antenna radiate properly.
Note 2	For the best on-board antenna performance, the module 453-00001/453-00225 MUST be placed on the edge of the host PCB and preferably in the edge centre and host PCB, the antenna "Keep Out Area" is extended (see Note 4).
Note 3	BL54L15 development board has the 453-00001 placed on the edge of the PCB board (and not in corner) for that the Antenna keep out area is extended down to the corner of the development board, see section 8.2 Host PCB Land Pattern and Antenna Keep-out for the 453-00001 and 453-00225.
Note 4	Ensure that there is no exposed copper under the module on the host PCB.
Note 5	You may modify the PCB land pattern dimensions based on their experience and/or process capability.

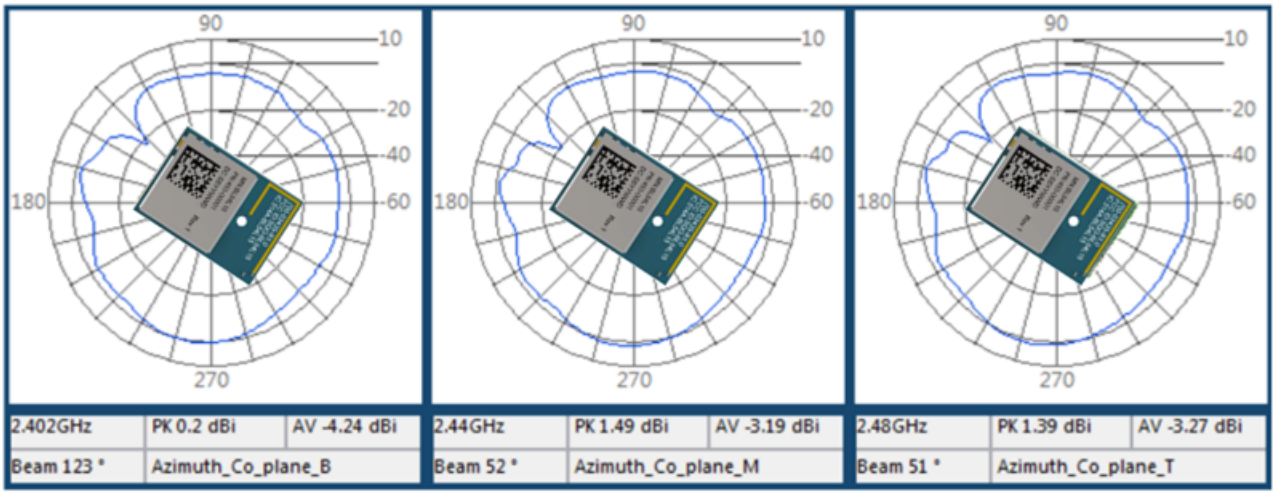
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9 On -Board PCB Trace Antenna Characteristics

9.1 Summary of Antenna Performance

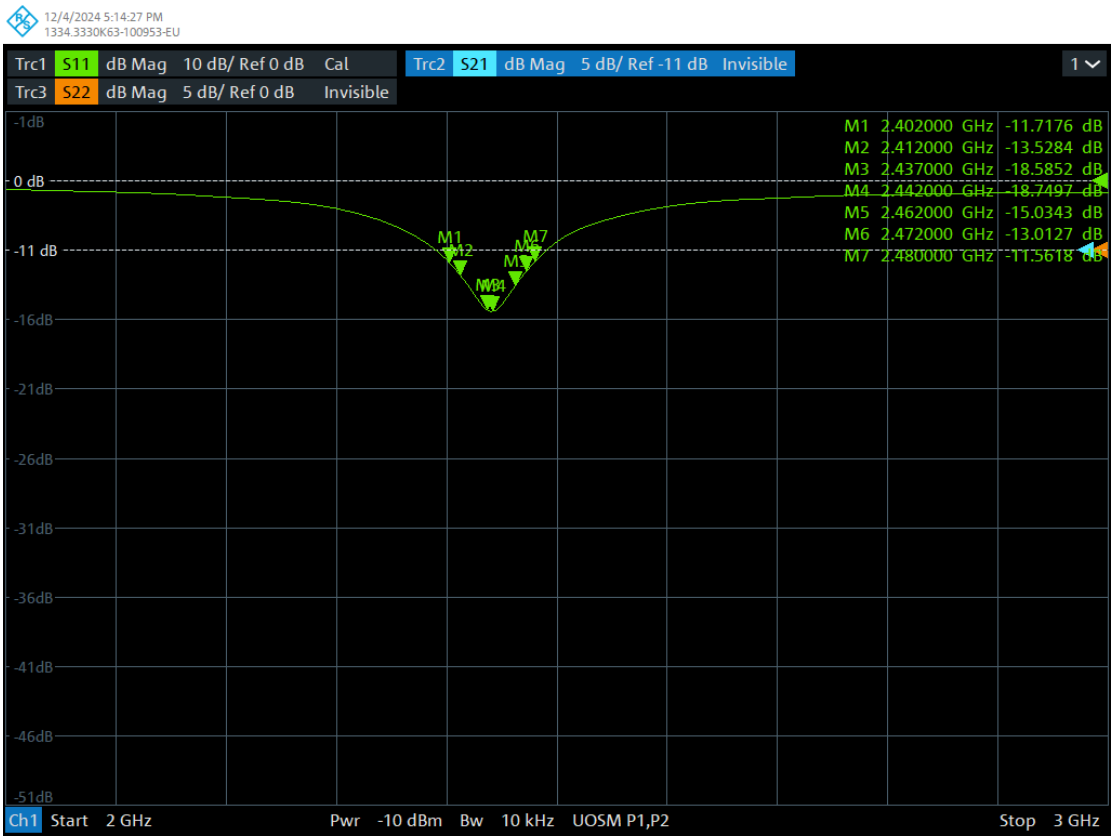
	2402MHz		2440MHz		2480MHz	
	Peak	Avg	Peak	Avg	Peak	Avg
453-00001/453-00225 PCB trace antenna	+0.2dBi	-4.24dBi	+1.49dBi	-3.19dBi	+1.39dBi	-3.27dBi

9.2 2.4GHz Radiated Performance



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9.3 Antenna S11 measuring data



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10 Application Note for Surface Mount Modules

10.1 Introduction

Ezurio's surface mount modules are designed to conform to all major manufacturing guidelines. This application note is intended to provide additional guidance beyond the information that is presented in the user manual. This application note is considered a living document and will be updated as new information is presented.

The modules are designed to meet the needs of several commercial and industrial applications. They are easy to manufacture and conform to current automated manufacturing processes.

Part numbers – **453-00001R/453-00225R and 453-00044R/453-00226R** are shipped as Tape / Reel, with a reel containing 1,000 pcs.

10.2 Module Packaging Configuration

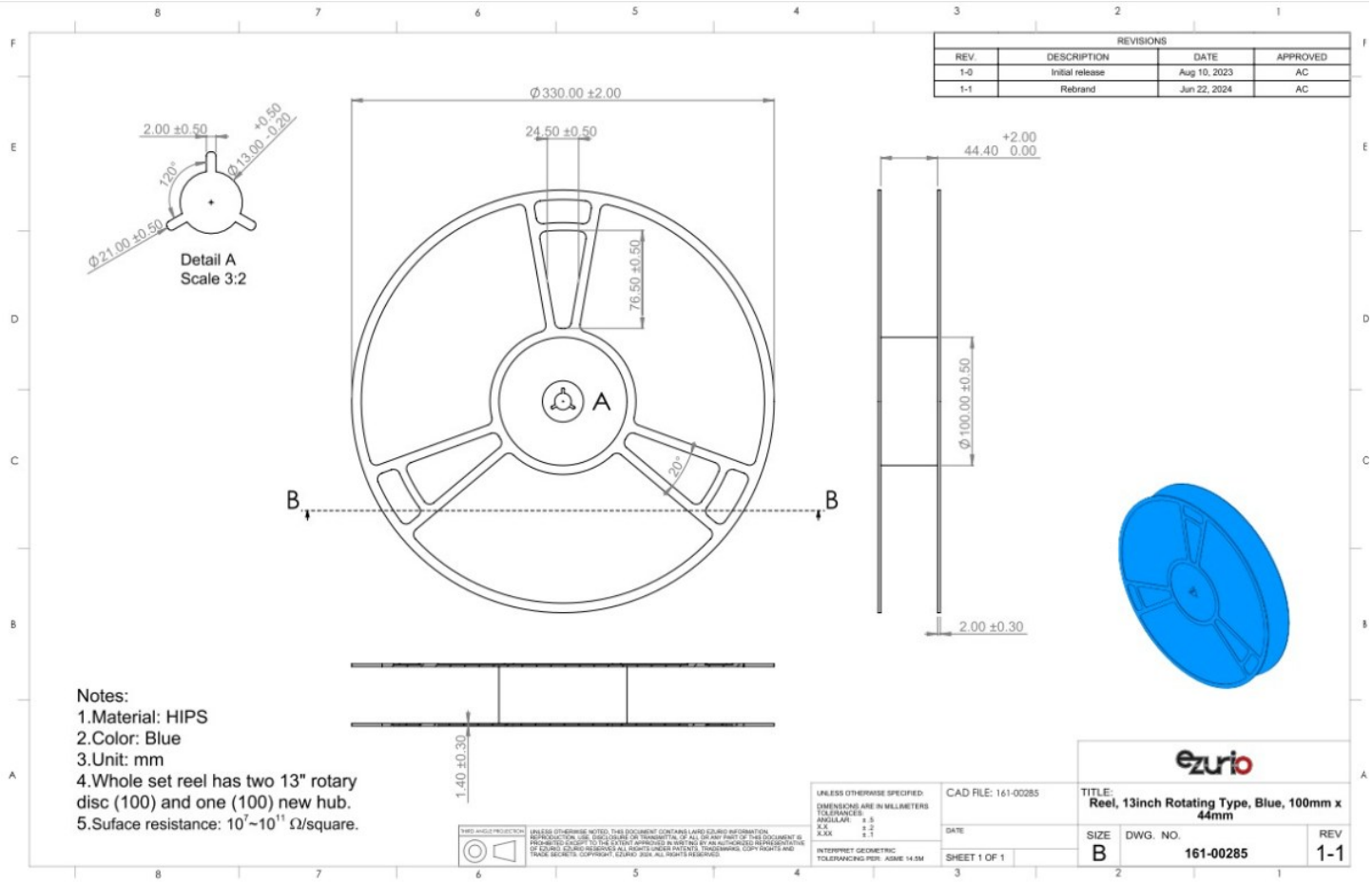


Figure 12: Reel specifications – 1,000 pieces per reel

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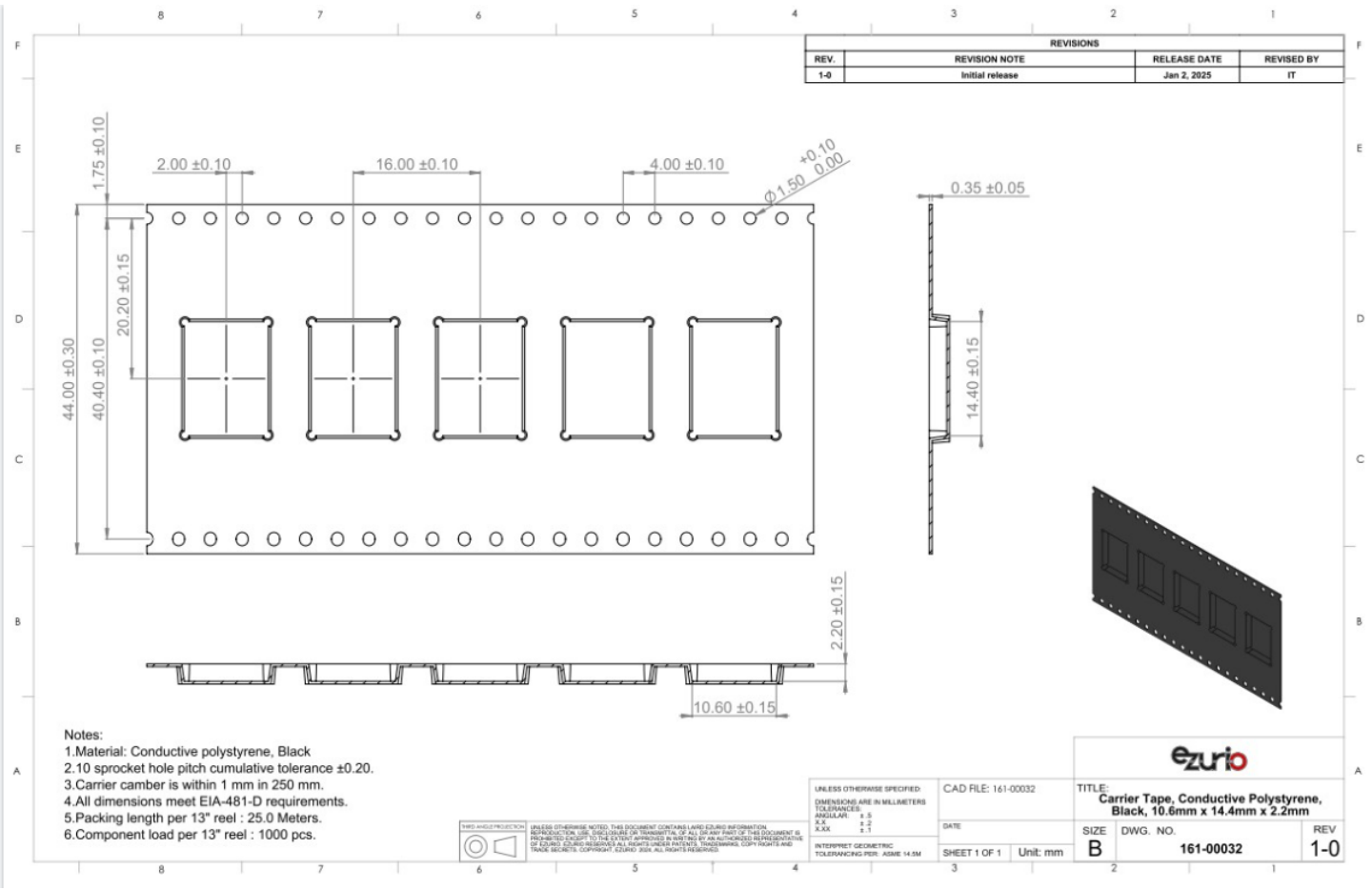
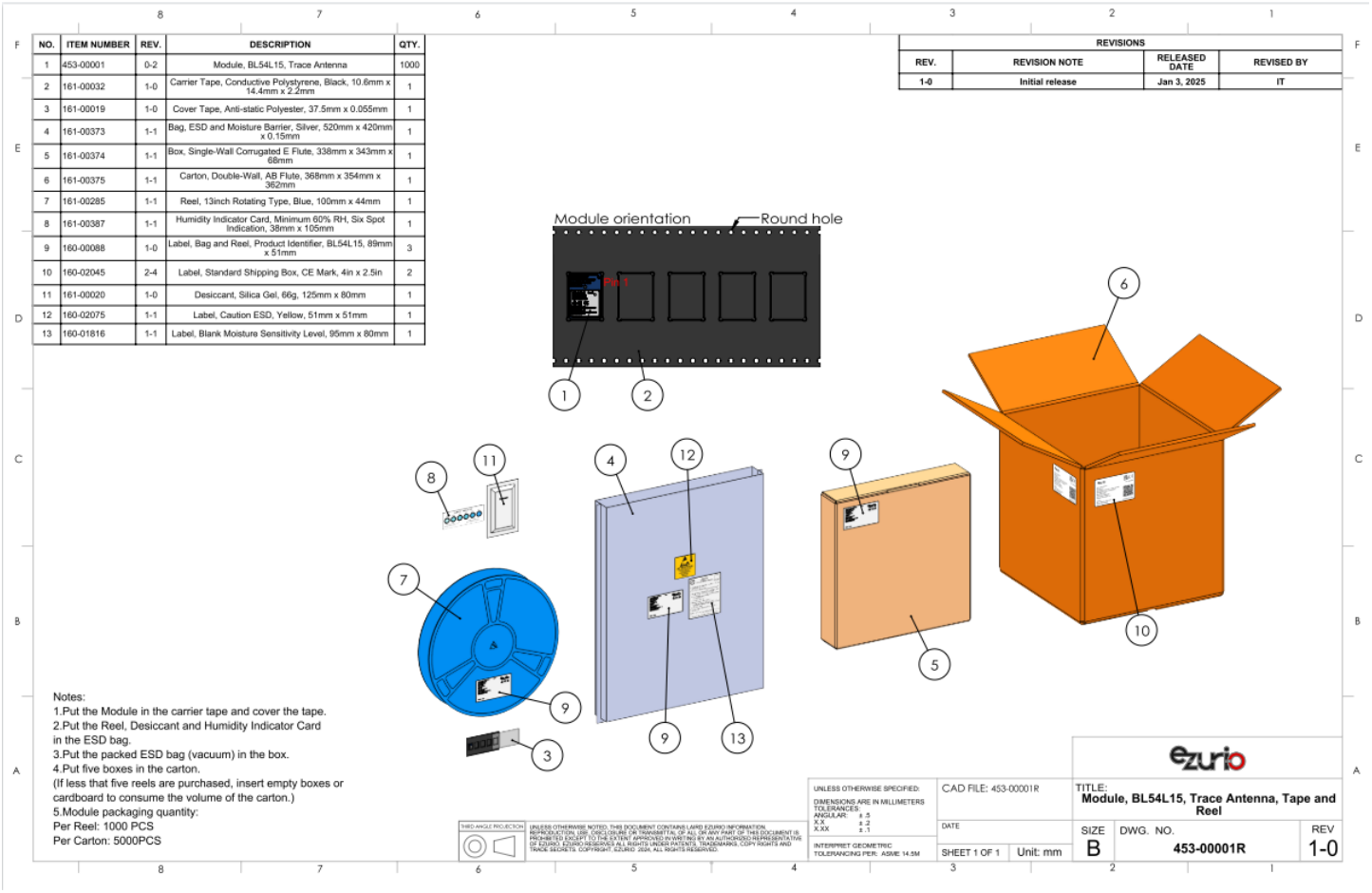


Figure 13: Carrier Tape specifications

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NO.	ITEM NUMBER	REV.	DESCRIPTION	QTY.
1	453-00001	0-2	Module, BL54L15, Trace Antenna	1000
2	161-00032	1-0	Carrier Tape, Conductive Polystyrene, Black, 10.6mm x 14.4mm x 2.2mm	1
3	161-00019	1-0	Cover Tape, Anti-static Polyester, 37.5mm x 0.055mm	1
4	161-00373	1-1	Bag, ESD and Moisture Barrier, Silver, 520mm x 420mm x 0.15mm	1
5	161-00374	1-1	Box, Single-Wall Corrugated E Flute, 338mm x 343mm x 68mm	1
6	161-00375	1-1	Carton, Double-Wall, AB Flute, 368mm x 354mm x 362mm	1
7	161-00285	1-1	Reel, 13inch Rotating Type, Blue, 100mm x 44mm	1
8	161-00387	1-1	Humidity Indicator Card, Minimum 60% RH, Six Spot Indication, 38mm x 105mm	1
9	160-00088	1-0	Label, Bag and Reel, Product Identifier, BL54L15, 89mm x 51mm	3
10	160-02045	2-4	Label, Standard Shipping Box, CE Mark, 4in x 2.5in	2
11	161-00020	1-0	Desiccant, Silica Gel, 66g, 125mm x 80mm	1
12	160-02075	1-1	Label, Caution ESD, Yellow, 51mm x 51mm	1
13	160-01816	1-1	Label, Blank Moisture Sensitivity Level, 95mm x 80mm	1

REVISIONS			
REV.	REVISION NOTE	RELEASED DATE	REVISED BY
1-0	Initial release	Jan 3, 2025	IT

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN MILLIMETERS
TOLERANCES:
ANGULAR: ± .5
X.X ± .2
X.XX ± .1
INTERPRET GEOMETRIC TOLERANCING PER: ASME Y14.5M

CAD FILE: 453-00001R

DATE

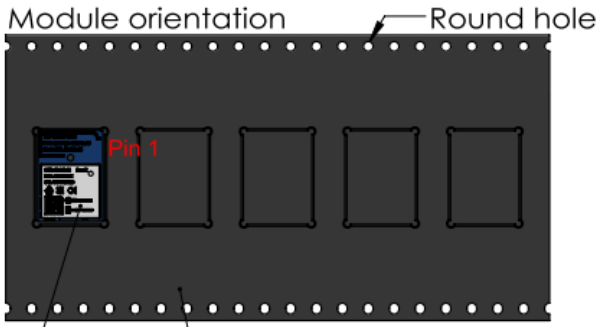
SHEET 1 OF 1 Unit: mm

TITLE: Module, BL54L15, Trace Antenna, Tape and Reel

SIZE B | DWG. NO. 453-00001R | REV 1-0

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Figure 14: BL54L15/BL54L10 Packaging Process



10.3 Module Shipping

All modules are shipped in tape and reel package and sealed in ESD Bags.

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10.4 Labeling

The following labels are placed on the anti-static bag. The BL54L15/BL54L10 modules are classified as MSL4 devices.

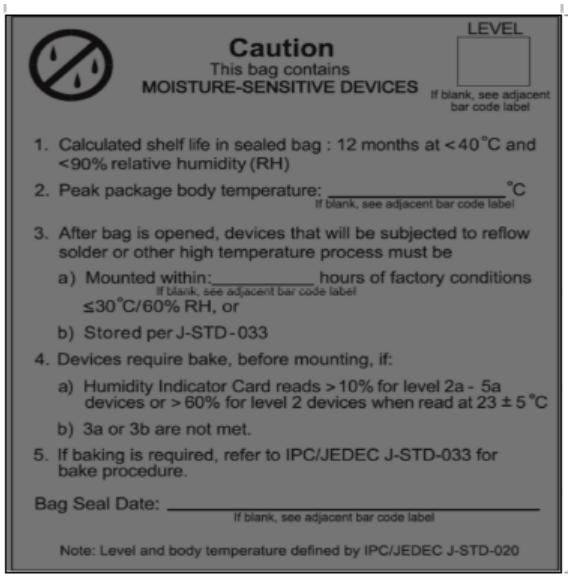


Figure 15: Moisture Sensitivity Level Label



Figure 16: Product Identifier Label

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The following labels are placed on the pizza box.



Figure 17: Product Identifier Label

The following labels are placed on the master shipping carton.



Figure 18: Standard Shipping Carton Label

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10.5 Required Storage Conditions

10.5.1 Prior to Opening the Dry Packing

The following are required storage conditions ***prior* to opening the dry packing**:

- Normal temperature: 5~40˚C
- Normal humidity: 80% (Relative humidity) or less
- Storage period: One year or less

Note: Humidity means relative humidity.

10.5.2 After Opening the Dry Packing

The following are required storage conditions ***after* opening the dry packing** (to prevent moisture absorption):

- Storage conditions for one-time soldering:
  - Temperature: 5-25°C
  - Humidity: 60% or less
  - Period: 72 hours or less after opening
- Storage conditions for two-time soldering
  - Storage conditions following opening and prior to performing the 1st reflow:
    - Temperature: 5-25°C
    - Humidity: 60% or less
    - Period: A hours or less after opening
  - Storage conditions following completion of the 1st reflow and prior to performing the 2nd reflow
    - Temperature: 5-25°C
    - Humidity: 60% or less
    - Period: B hours or less after completion of the 1st reflow

---

Note: Should keep A+B within 72 hours.

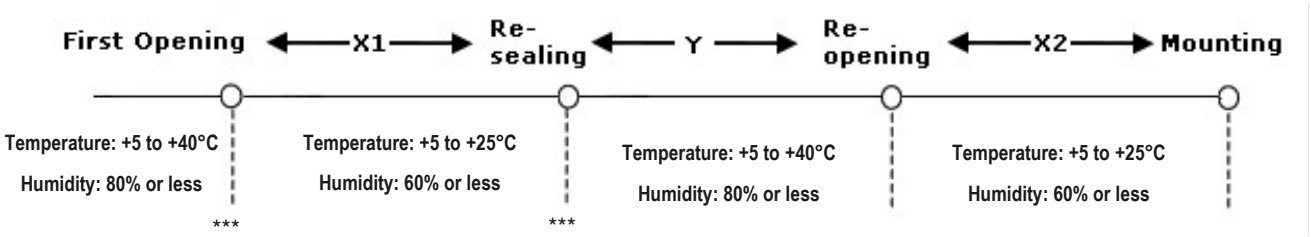
10.5.3 Temporary Storage Requirements after Opening

The following are temporary storage requirements after opening:

- Only re-store the devices *once* prior to soldering.
- Use a dry box or place desiccant (with a blue humidity indicator) with the devices and perform dry packing again using vacuumed heat-sealing.

The following indicate the required storage period, temperature, and humidity for this temporary storage:

- Storage temperature and humidity:



*** - External atmosphere temperature and humidity of the dry packing

- Storage period:
  - X1+X2 – Refer to After Opening the Dry Packing storage requirements. Keep is X1+X2 within 72 hours.
  - Y – Keep within two weeks or less.

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10.6 Baking Conditions

Baking conditions and processes for the module follow the J-STD-033 standard which includes the following:

- The calculated shelf life in a sealed bag is 12 months at <40℃ and <80% relative humidity.
- Once the packaging is opened, the module must be mounted (per MSL4/Moisture Sensitivity Level 4) within 72 hours at <30 °C and <60% relative humidity.
- If the module is not mounted within 72 hours or if, when the dry pack is opened, the humidity indicator card displays >10% humidity, then the product must be baked for 48 hours at 125 °C (±5 °C).

10.7 Surface Mount Conditions

The following soldering conditions are recommended to ensure device quality.

10.7.1 Soldering

Note: When soldering, the stencil thickness should be ≥ 0.1 mm.

Convection reflow or IR/Convection reflow (one-time soldering or two-time soldering in air or nitrogen environment)

- Measuring point – IC package surface
- Temperature profile:

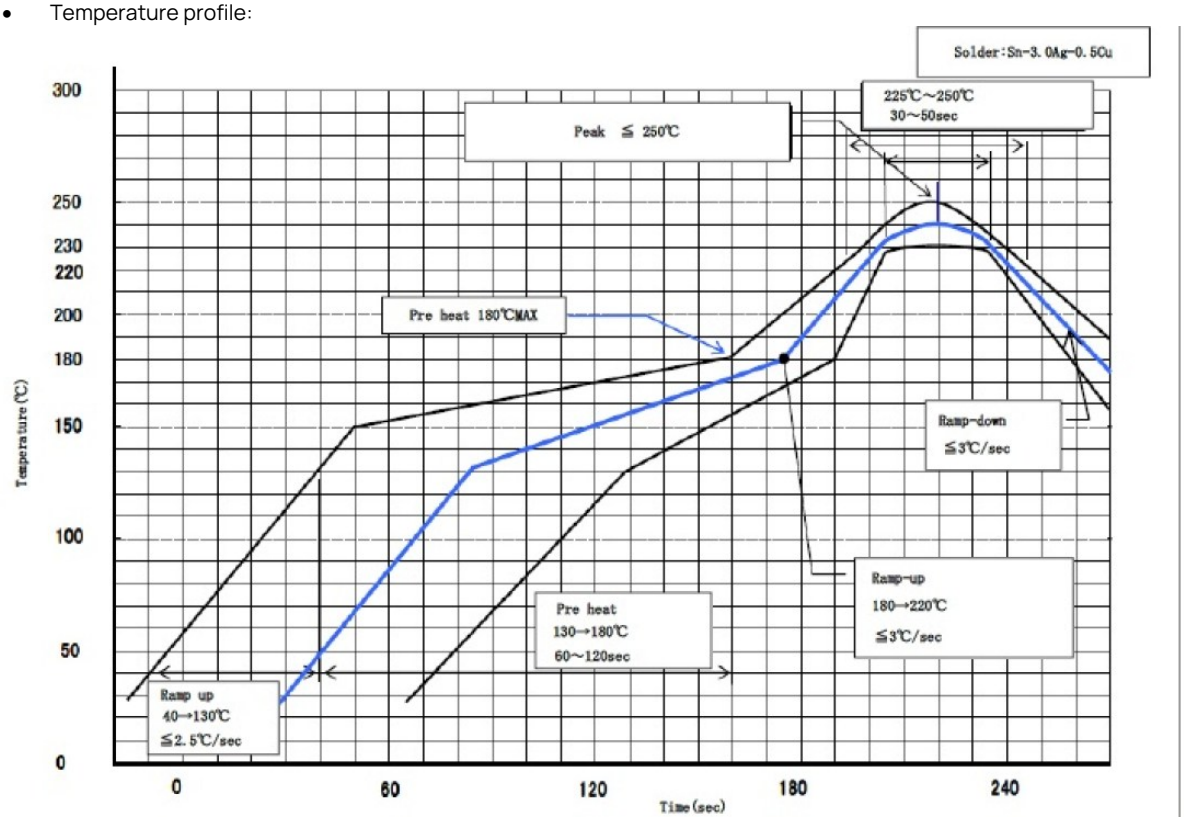


Figure 19: Temperature profile

- Ramp-up: 40-130 °C. Less than 2.5 °C/sec
- Pre heat: 130-180 °C 60-120 sec, 180 °C MAX
- Ramp-up: 180-220 °C. Less than 3 °C/sec
- Peak Temperature: MAX 250 °C
  - 225 °C ~ 250 °C, 30 ~ 50 sec
- Ramp-down: Less than 3 °C/sec

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10.7.2 Cautions When Removing the BL54L15/BL54L10 from the Platform for RMA

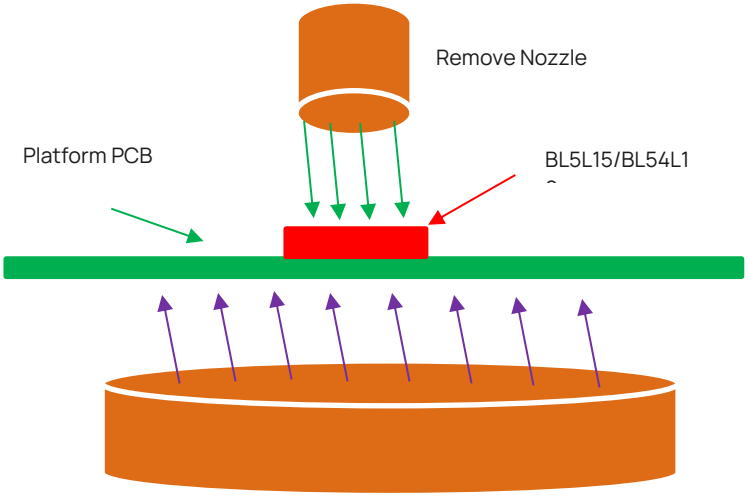
- Bake the platform before removing the BL54L15/BL54L10 from the platform. Reference baking conditions.
- Remove the BL54L15/BL54L10 by using a hot air gun. This process should be carried out by a skilled technician.

Suggestion conditions:

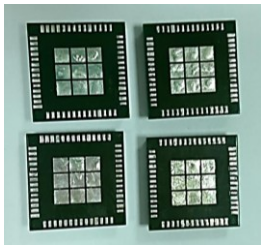


- One-side component platform:
  - Set the hot plate at 280 °C.
  - Put the platform on the hot plate for 8~10 seconds.
  - Remove the SIP from platform.
- Two-side components platform:
  - Use two hot air guns
  - On the bottom side, use a pre-heated nozzle (temperature setting of 200~250 °C) at a suitable distance from the platform PCB.
  - On the top side, apply a remove nozzle (temperature setting of 330 °C). Heat the SIP until it can be removed from platform PCB.



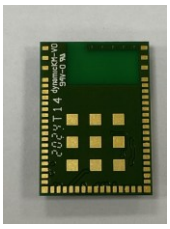


- Remove the residue solder under the bottom side of module. (Note: Alternate module pictured as an example)



(Not accepted for RMA)

Example module with residue solder on the bottom



(Accepted for RMA analysis)

Example Module, no residue solder

- Remove and clean the residue flux as needed.

10.7.3 Precautions for Use

- Opening/handing/removing must be done on an anti-ESD treated workbench. All workers must also have undergone anti-ESD treatment.
- The devices should be mounted within one year of the date of delivery.
- The BL54L15/BL54L10 modules are MSL 4 rated.

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11 Reliability Test

11.1 Climatic And Dynamic Reliability Test

Table 5: Climatic and Dynamic Reliability Test Results for BL54L15/BL54L10 Modules

Test Item	Specification	Standard	Test Result
Thermal Shock	Temperature: -40 ~ 85℃ Ramp time: Less than 10 seconds. Dwell Time: 10 minutes Number of Cycles: 350 times	*JESD22-A106 *IEC 60068-2-14 for dwell time and number of cycles	PASS
Vibration Non-Operating Unpackaged device	Vibration Wave Form: Sine Waveform Vibration frequency / Displacement: 20-80 Hz/1.5mm Vibration frequency / Acceleration: 80-2000 Hz/20g Cycle Time: 4 min/cycle Number of Cycles: 4 cycle/axis Vibration Axes: X, Y and Z (Rotate each axis on vertical vibration table)	JEDEC 22-B103B (2016)	PASS
Mechanical Shock Non-Operating Unpackaged device	Pulse shape: Half-sine waveform Impact acceleration: 1500 g Pulse duration: 0.5 ms Number of shocks: 30 shocks (5 shocks for each face) Orientation: Bottom, top, left, right, front, and rear faces	JEDEC 22-B110B.01 (2019)	PASS

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11.2 Reliability MTBF Prediction

Table 6: MTBF Predictions for BL54L15/BL54L10 Modules

Ezurio Part Number	Environment	Standard	Test Result 45 ℃ (Hours)
453-00001R 453-00001C 453-00225R 453-00225C	Ground, Fixed, Uncontrolled	Telcordia Issue 4	1,559,211
453-00044R 453-00044C 453-00226R 453-00226C	Ground, Fixed, Uncontrolled	Telcordia Issue 4	1,559,211
453-00001R 453-00001C 453-00225R 453-00225C	Mobile, Fixed, Uncontrolled	Telcordia Issue 4	605,957
453-00044R 453-00044C 453-00226R 453-00226C	Mobile, Fixed, Uncontrolled	Telcordia Issue 4	605,957
Ezurio Part Number	**Environment**	**Standard**	**Test Result 105 ℃ (Hours)**
453-00001R 453-00001C 453-00225R 453-00225C	Ground, Fixed, Uncontrolled	Telcordia Issue 4	980,517
453-00044R 453-00044C 453-00226R 453-00226C	Ground, Fixed, Uncontrolled	Telcordia Issue 4	980,517
453-00001R 453-00001C 453-00225R 453-00225C	Mobile, Fixed, Uncontrolled	Telcordia Issue 4	283,138
453-00044R 453-00044C 453-00226R 453-00226C	Mobile, Fixed, Uncontrolled	Telcordia Issue 4	283,138

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12 Regulatory

Full regulatory information on the BL54L15/BL54L10, including the Regulatory Information Guide, grants, and test reports are available on the BL54L15 product page and BL54L10 product page.

The BL54L15/BL54L10 holds current certifications in the following countries:

Table 7: BL54L15 Certifications

Country/Region	Regulatory ID
USA (FCC)	SQG-BL54L15
EU (ETSI)	N/A (No ID Number Required)
UKCA	N/A (No ID Number Required)
Canada (ISED)	3147A-BL54L15
Japan (MIC)	201-250023
Australia (RCM)	N/A
New Zealand (RCM)	N/A
Korea	R-C-EZU1-BL54L15 (for BL54L15) R-C-EZU1-BL54L10 (for BL54L10)

12.1 Certified Antennas for the BL54L15/BL54L10

Table 8: Certified Antennas for BL54L15/BL54L10 Modules

Model	MPN	Manufacturer	Type	Connector	Peak Gain (2400 – 2500 MHz)
NanoBlue	EBL2400A1-10MH4L	Ezurio	PCB Dipole	IPEX MHF4	2 dBi
FlexPIFA	001-0022	Ezurio	FlexPIFA	IPEX MHF4L	2 dBi
EDA-8709-2G4C1-B27-CY	EDA-8709-2G4C1-B27-CY (Ezurio Part#0600-00057)	MAG.LAYERS	Dipole	IPEX MHF4	2.32 dBi
mFlexPIFA	EFA2400A3S-10MH4L	Ezurio	PIFA	IPEX MHF4L	2 dBi
I-FlexPIFATM Mini Series	EFG2401A3S-10MHF4L	Ezurio	I-FlexPIFA	IPEX MHF4L	2 dBi
Ezurio NFC	0600-00061	Ezurio	Coiled Inductor	FFC/FPC Connector	-

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13 Bluetooth Qualification Process

13.1 Overview

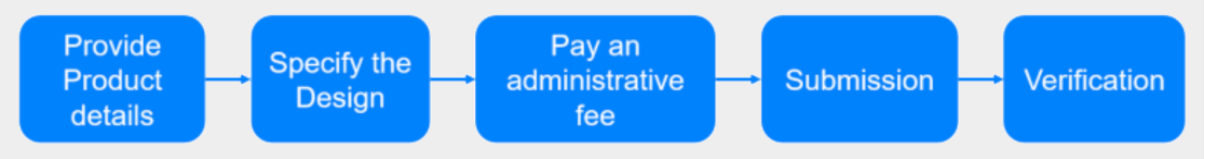
The Bluetooth Qualification Process promotes global product interoperability and reinforces the strength of the Bluetooth® brand and ecosystem to the benefit of all Bluetooth SIG members. The Bluetooth Qualification Process helps member companies ensure their products that incorporate Bluetooth technology comply with the Bluetooth Patent & Copyright License Agreement and the Bluetooth Trademark License Agreement (collectively, the Bluetooth License Agreement) and Bluetooth Specifications.

The Bluetooth Qualification Process is defined by the Qualification Program Reference Document (QPRD) v3.

To demonstrate that a product complies with the Bluetooth Specification(s), each member must for each of its products:

- Identify the product, the design included in the product, the Bluetooth Specifications that the design implements, and the features of each implemented specification
- Complete the Bluetooth Qualification Process by submitting the required documentation for the product under a user account belonging to your company

The Bluetooth Qualification Process consists of the phases shown below:



To complete the Qualification Process the company developing a Bluetooth End Product shall be a member of the Bluetooth SIG. To start the application please use the following link: Apply for Adopter Membership

13.2 Scope

This guide is intended to provide guidance on the Bluetooth Qualification Process for End Products that reference a single existing design, that has not been modified, (refer to Section 3.2.1 of the Qualification Program Reference Document v3).

This option applies to a Member qualifying a Product that includes an existing Design that has a DN, QDID, or DID and that Design has not been modified (e.g., rebranding a Qualified Product from another Member). The Design identified by the DN, QDID, or DID may only implement Bluetooth Specifications that are active or deprecated at the time of Submission. No modifications may be made to the Design, including changes to the ICS Form.

Changes to the Product outside the Design are allowed, including:

- Enabling technologies
- Changes to the industrial design
- Changes to the communication technology other than Bluetooth
- Changes to the features that are unrelated to Bluetooth, branding, packaging, colour, shape, Product name, or Model number

Members are responsible for assessing that modifications to the Product outside of the Design do not affect compliance with Bluetooth Specifications or result in a change to the ICS Form.

For the purposes of this document, it is assumed that the member is combining a single unmodified Core-Complete Configuration.

13.3 Qualification Steps When Referencing a single existing design, (unmodified) – Option 1 in the QPRDv3

For this qualification, follow these steps:

1. To start a listing, go to: https://qualification.bluetooth.com/
2. Select **Start the Bluetooth Qualification Process**.
3. Product Details to be entered:
    - Project Name (this can be the product name or the Bluetooth Design name).
    - Product Description
    - Model Number
    - Product Publication Date (the product publication date may not be later than 90 days after submission)

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- Product Website (optional)
- Internal Visibility (this will define if the product will be visible to other users prior to publication)
- If you have multiple End Products to list then you can select 'Import Multiple Products', firstly downloading and completing the template, then by 'Upload Product List'. This will populate Qualification Workspace with all your products.

4. Specify the Design:
   - Do you include any existing Design(s) in your Product? Answer Yes, I do.
   - Enter the single DN or QDID used in your, (for Option 1 only one DN or QDID can be referenced)
   - Once the DN or QDID is selected it will appear on the left-hand side, indicating the layers covered by the design.
   - Select 'I'm finished entering DN's
   - What do you want to do next? Answer, 'Use this Design without Modification'
   - Save and go to Product Qualification Fee
5. Product Qualification Fee:
   - It's important to make sure a Prepaid Product Qualification fee is available as it is required at this stage to complete the Qualification Process.
   - Prepaid Product Qualification Fee's will appear in the available list so select one for the listing.
   - If one is not available select 'Pay Product Qualification Fee', payment can be done immediately via credit card, or you can pay via Invoice. Payment via credit will release the number immediately, if paying via invoice the number will not be released until the invoice is paid.
   - Once you have selected the Prepaid Qualification Fee, select 'Save and go to Submission'
6. Submission:
   - Some automatic checks occur to ensure all submission requirements are complete.
   - To complete the listing any errors must be corrected
   - Once you have confirmed all design information is correct, tick all of the three check boxes and add your name to the signature page.
   - Now select 'Complete the Submission'.
   - You will be asked a final time to confirm you want to proceed with the submission, select 'Complete the Submission'.
   - Qualification Workspace will confirm the submission has been submitted. The Bluetooth SIG will email confirmation once the submission has been accepted, (normally this takes 1 working day).
7. Download Product and Design Details:
   a. You can now download a copy of the confirmed listing from the design listing page and save a copy in your Compliance Folder

For further information, please refer to the following webpage:
https://www.bluetooth.com/develop-with-bluetooth/qualification-listing/

13.4 Example Designs for reference

The following gives an example of a design possible under option 1:

Ezurio End Product design using Nordic Component based design

Design Name	Owner	Design ID	Link to listing on the SIG website
BL54L15/BL54L15µ	Ezurio	Q345095	https://qualification.bluetooth.com/ListingDetails/274104

13.5 Qualify More Products

If you develop further products based on the same design in the future, it is possible to add them free of charge. The new product must not modify the existing design i.e add ICS functionality, otherwise a new design listing will be required.

To add more products to your design, select 'Manage Submitted Products' in the Getting Started page, Actions, Qualify More Products. The tool will take you through the updating process.

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14 Ordering Information

Part Number	Product Description
453-00001R	Module, BL54L15, (Nordic nRF54L15), Trace antenna, Tape/Reel
453-00044R	Module, BL54L15, (Nordic nRF54L15), MHF4 Connector, Tape/Reel
453-00001C	Module, BL54L15, (Nordic nRF54L15), Trace antenna, Cut Tape
453-00044C	Module, BL54L15, (Nordic nRF54L15), MHF4 Connector, Cut Tape
453-00001-K1	Development kit, Module, BL54L15 (Nordic nRF54L15), Trace antenna
453-00044-K1	Development kit, Module, BL54L15 (Nordic nRF54L15), MHF4 Connector
453-00225R	Module, BL54L10, (Nordic nRF54L10), Trace antenna, Tape/Reel
453-00226R	Module, BL54L10, (Nordic nRF54L10), MHF4 Connector, Tape/Reel
453-00225C	Module, BL54L10, (Nordic nRF54L10), Trace antenna, Cut Tape
453-00226C	Module, BL54L10, (Nordic nRF54L10), MHF4 Connector, Cut Tape

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15 Additional Information

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Website	http://www.ezurio.com
Technical Support	http://www.ezurio.com/resources/support
Sales Contact	http://www.ezurio.com/contact

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