NAU88L24

Ultra-Low Power Audio CODEC with Stereo Class D Drivers and Ground-Referenced Headphone Amplifier with Advanced Headset Detection

Description

The NAU88L24 is an ultra-low power high performance audio codec designed for smartphone, tablet PC, and other portable devices that supports both analog and digital audio functions. It includes one I2S/PCM interface, one digital mixer, two high quality DACs, two high quality ADCs, two mono differential or one stereo differential analog microphone inputs, four analog single-ended microphone inputs, four digital PDM microphone inputs, one single ended stereo auxilary or one differenital mono inputs, one differential headset mic input, one stereo 2.9W class D loudspeaker amplifier driver for 4 Ω loads and 5V supply, and one stereo class G headphone amplifier with advanced headset detection.

The advanced on-chip signal processing engine that includes programmable dynamic range compressors (DRC), 5-band parametric equalizer (PEQ), and high pass and notch filter block, can maximize audio quality and eliminate any undesirable frequency components.

The NAU88L24 also has powerful headset detection that supports jack insertion / ejection, microphone detection, distinct key / short key / long key / key release detection, microphone presence detection, speaker impedance detection, headphone crosstalk detection & suppression features as well as an integrated frequency locked loop (FLL) to support various clocks.

Features

- DAC: Headphone Playback SNR = 103dB (48KHz, 0dB Gain, RL= 32Ω, A-weighted)
- ADC: Microphone Recording SNR = 100dB (48KHz, 0dB Gain, A-weighted)
- 1 Digital I2S/PCM/TDM
- Dynamic Range Compressor (DRC)
- 5 Band Parametric Equalizer
- 1 Headset Microphone, 4 Analog or 4 Digital PDM MIC input supports
- Stereo 970mW Class D Loudspeaker @ 4.2V, 8Ω, 1% THD+N (or 2.9W @ 5.0V, 4Ω, 10% THD+N)
- Class G Headphone Amplifier(27mW @ 32Ω, 1% THD+N)
- Sampling rate from 8K to 96 KHz
- Jack Insertion and Ejection Detection
- MIC Presence Detection
- Up to 8 Distinct Button Detection with Long / Short Button Press Supports
- Speaker Impedance Detection
- Headphone Crosstalk Detection / Suppression
- Package : 48 Pin QFN package (6mm x 6mm)
- Optional Packages: 56 Balls WLCSP package with 0.4mm Pitch

Applications

- Tablets / Ultra-Portable Laptops
- Smartphones
- Audio Docking Systems
- Portable Game Players
- TV with Multi-MICs Beam Forming Application
- Cameras

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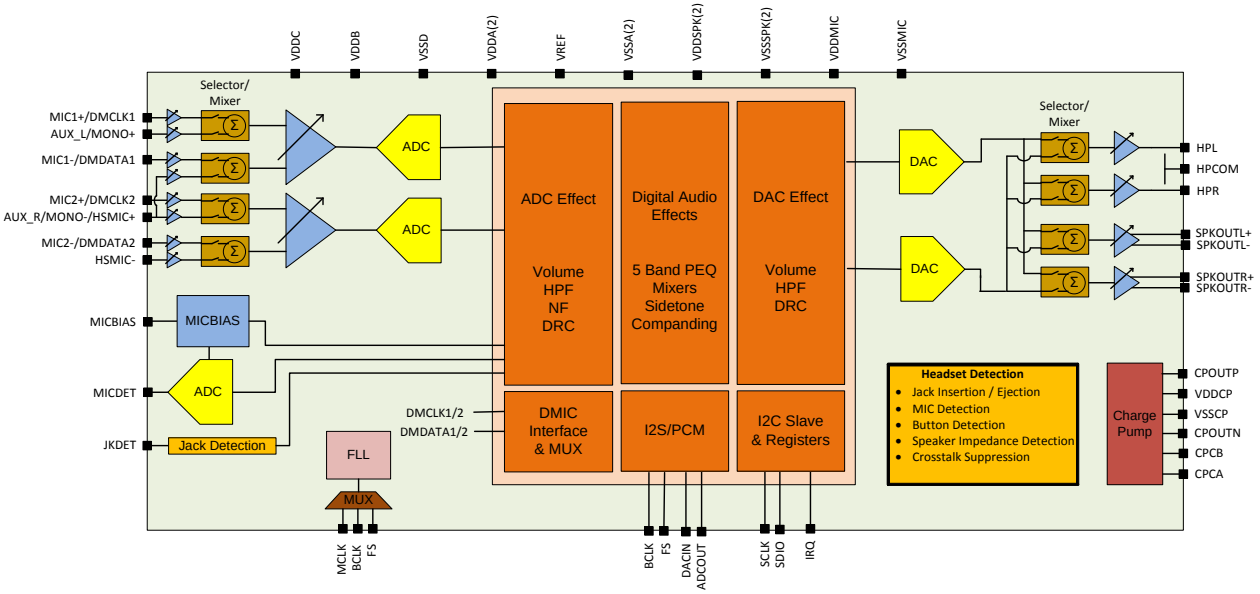
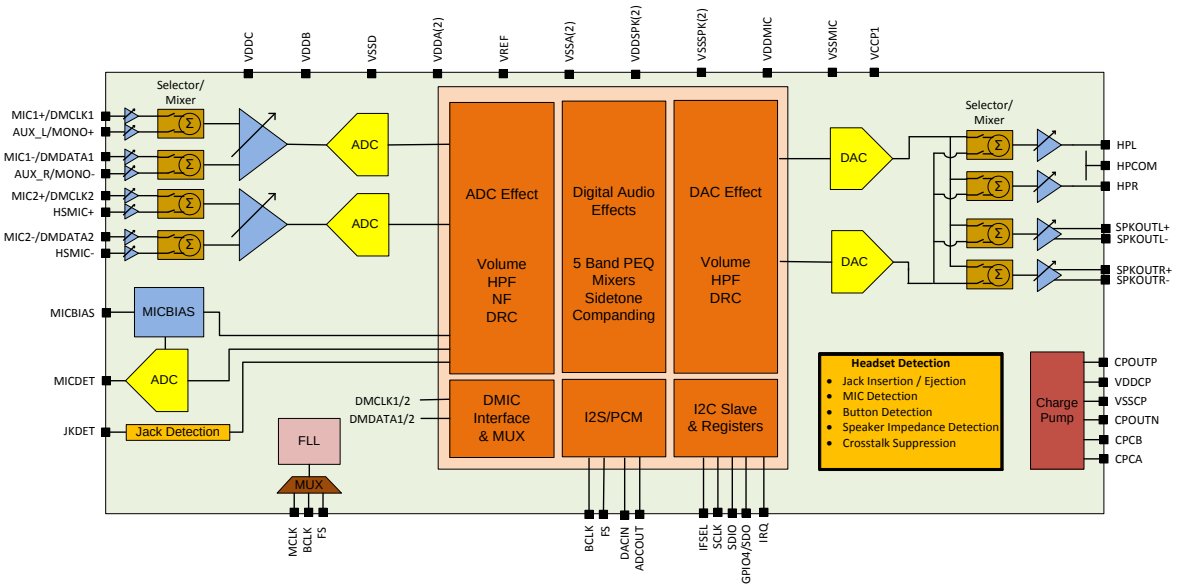
Block Diagram

QFN 48 Pin



56 Balls WLCSP



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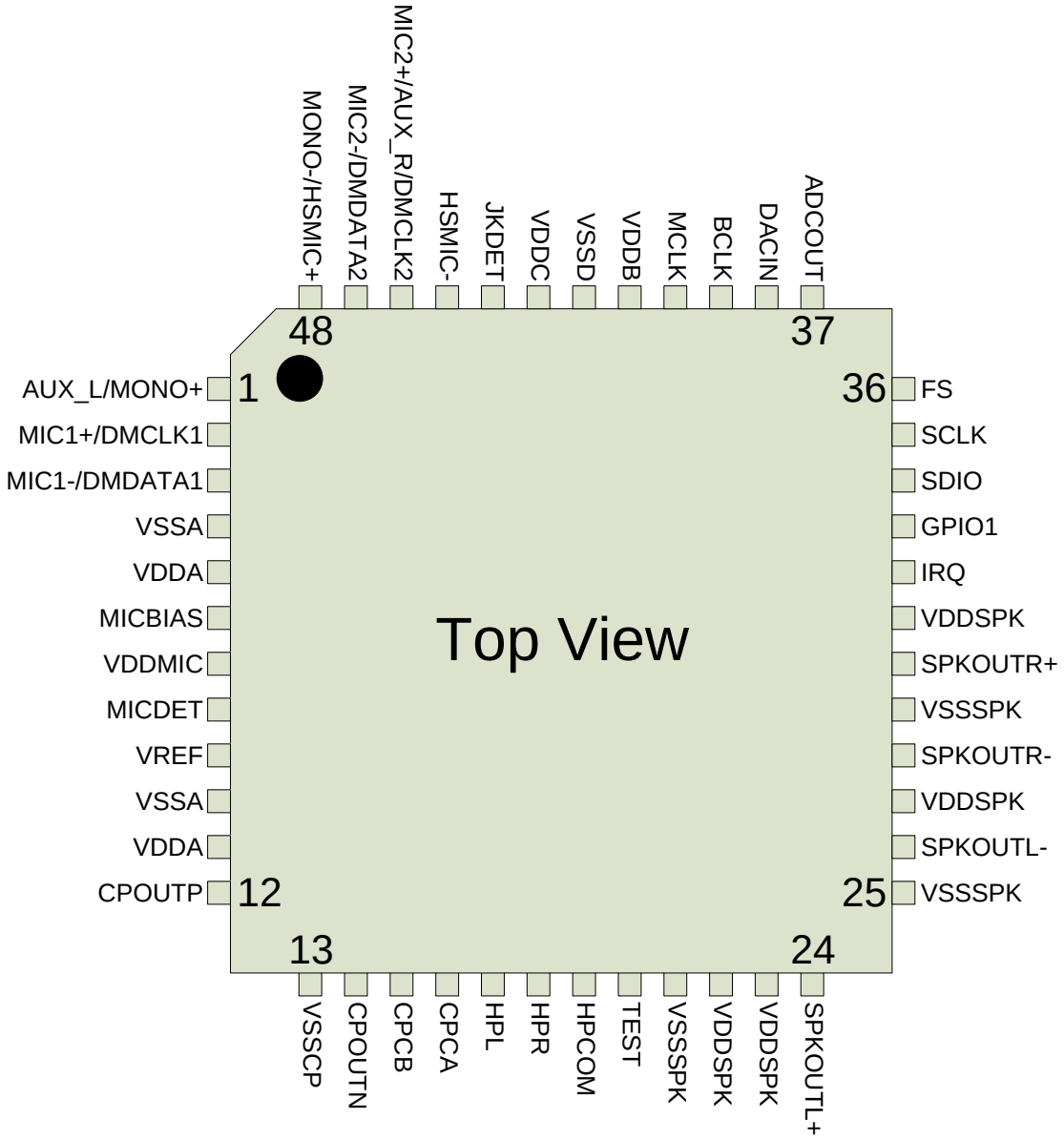
Pin Diagram – QFN 48



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Pin Description – QFN 48

Pin #	Name	Type	Functionality
1	AUX_L/MONO +	Analog Input	PGA Mono+ or Left channel Auxiliary Analog Input
2	MIC1+/DMCLK1	Analog Input / Digital Output	PGA MIC1+ Analog Input or Digital Microphone 1 Clock Output
3	MIC1-/DMDATA1	Analog Input / Digital Input	PGA MIC1- Analog Input or Digital Microphone 1 Data Input
4	VSSA	Ground	Analog Supply Ground
5	VDDA	Supply	Analog Supply
6	MICBIAS	Analog Output	Microphone Bias Output
7	VDDMIC	Supply	Microphone supply
8	MICDET	Analog Input	Microphone button detection input
9	VREF	Analog I/O	Internal DAC & ADC voltage reference decoupling I/O
10	VSSA	Ground	Analog Supply Ground
11	VDDA	Supply	Analog Supply
12	CPOUTP	Analog I/O	Charge Pump positive voltage
13	VSSCP	Ground	Charge Pump Supply ground
14	CPOUTN	Analog I/O	Charge Pump negative voltage
15	CPCB	Analog I/O	Charge Pump switching capacitor node B
16	CPCA	Analog I/O	Charge Pump switching capacitor node A
17	HPL	Analog Output	Headphone left channel output
18	HPR	Analog Output	Headphone right channel output
19	HPCOM	Analog Input	Headphone ground reference
20	TEST	N/C	Class-D amplifier Test point
21	VSSSPK	Ground	Class-D amplifier supply ground
22	VDDSPK	Supply	Class-D amplifier supply
23	VDDSPK	Supply	Class-D amplifier supply
24	SPKOUTL+	Analog Output	Class-D amplifier Left Channel positive Output
25	VSSSPK	Ground	Class-D amplifier supply ground
26	SPKOUTL-	Analog Output	Class-D amplifier Left Channel negative Output
27	VDDSPK	Supply	Class-D amplifier supply
28	SPKOUTR-	Analog Output	Class-D amplifier Right Channel negative Output
29	VSSSPK	Ground	Class-D amplifier supply ground
30	SPKOUTR+	Analog Output	Class-D amplifier Right Channel positive Output
31	VDDSPK	Supply	Class-D amplifier supply
32	IRQ	Digital Output	Programmable Interrupt Output
33	GPIO1	Digital I/O	General Purpose IO (I2C)
34	SDIO	Digital I/O	Serial Data for I2C or SPI
35	SCLK	Digital Input	Serial Data Clock for I2C or SPI
36	FS	Digital I/O	Frame Sync input or output for I2S or PCM data
37	ADCOUT	Digital Output	Serial Audio data Output for I2S or PCM data
38	DACIN	Digital Input	Serial Audio data input for I2S or PCM data
39	BCLK	Digital I/O	Serial data bit clock input or output for I2S or PCM data
40	MCLK	Digital Input	CODEC Master clock input
41	VDDB	Supply	Digital IO Supply
42	VSSD	Ground	Digital IO ground
43	VDDC	Supply	Digital core supply
44	JKDET	Analog Input	Jack detect input

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45	HSMIC-	Analog Input	Headset Microphone negative Analog input
46	MIC2+/AUX_R /DMCLK2	Analog Input / Digital Output	PGA MIC2+ or AUXR Analog Input or Digital Microphone 2 Clock Output
47	MIC2-/DMDATA2	Analog Input / Digital Input	PGA MIC2- Analog Input or Digital Microphone 2 Data Input
48	MONO-/HSMIC+	Analog Input	PGA Mono-, or Headset Microphone positive Analog Input

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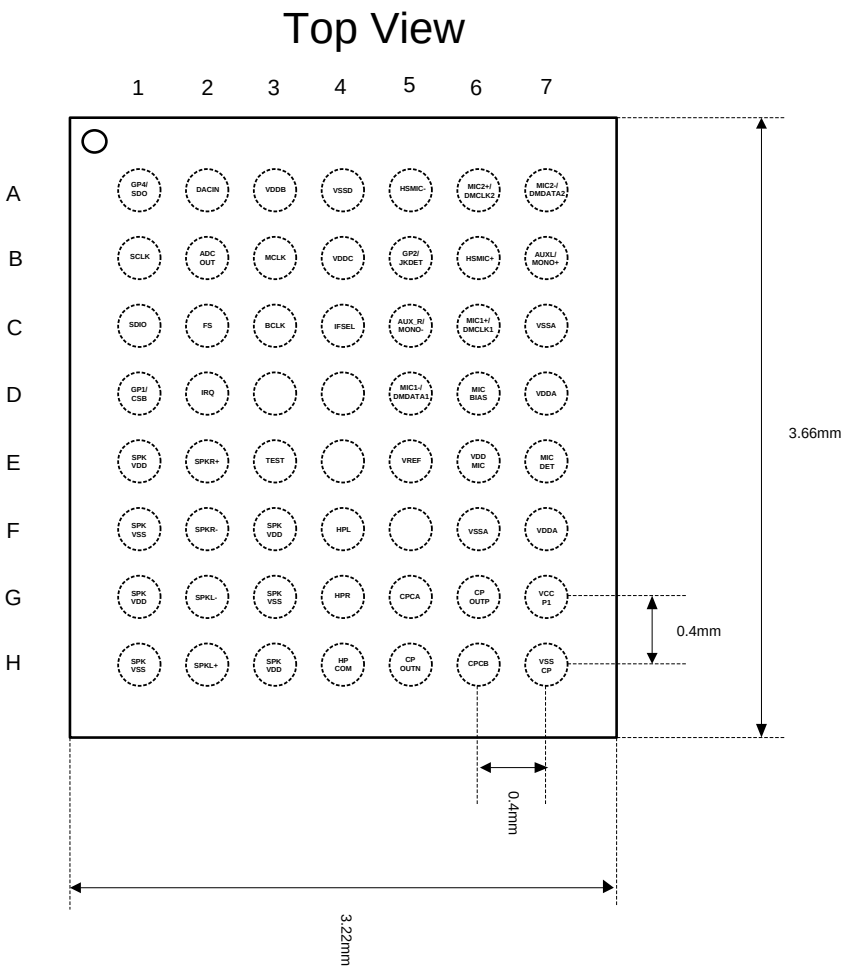
Pin Diagram – WLCSP Package



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Pin Description – 56 Balls WLCSP

Pin #	Name	Type	Functionality
A1	GPIO4/SDO	Digital I/O	General Purpose IO / 3 Wire Data Output
A2	DACIN	Digital Input	Serial Audio data input for I2S or PCM data
A3	VDDB	Supply	Digital IO Supply
A4	VSSD	Ground	Digital IO ground
A5	HSMIC-	Analog Input	Headset Microphone negative Analog input
A6	MIC2+/DMCLK2	Analog Input / Digital Output	PGA MIC2+ Analog Input or Digital Microphone 2 Clock Output
A7	MIC2-/DMDATA2	Analog Input / Digital Input	PGA MIC2- Analog Input or Digital Microphone 2 Data Input
B1	SCLK	Digital Input	Serial Data Clock for I2C or SPI
B2	ADCOUT	Digital Output	Serial Audio data Output for I2S or PCM data
B3	MCLK	Digital Input	CODEC Master clock input
B4	VDDC	Supply	Digital core supply
B5	GPIO2/JKDET	Analog Input	General purpose IO or Jack detect input
B6	AUX_R/MONO-	Analog Input	PGA Mono or Right channel Auxiliary Analog Input
B7	AUX_L/MONO +	Analog Input	PGA Mono or Left channel Auxiliary Analog Input
C1	SDIO	Digital I/O	Serial Data for I2C or SPI
C2	FS	Digital I/O	Frame Sync input or output for I2S or PCM data
C3	BCLK	Digital I/O	Serial data bit clock input or output for I2S or PCM data
C4	IFSEL	Digital I/O	Select Control Interface for 3 wire or 2 wire mode
C5	HSMIC+	Analog Input	Headset Microphone positive Analog Input
C6	MIC1+/DMCLK1	Analog Input / Digital Output	PGA MIC1+ Analog Input or Digital Microphone 1 Clock Output
C7	VSSA	Ground	Analog Supply Ground
D1	GPIO1/CSB	Digital I/O	General Purpose IO (I2C) or Chip Select Bar (SPI)
D2	IRQ	Digital Output	Programmable Interrupt Output
D5	MIC1-/DMDATA1	Analog Input / Digital Input	PGA MIC1- Analog Input or Digital Microphone 1 Data Input
D6	MICBIAS	Analog Output	Microphone Bias Output
D7	VDDA	Supply	Analog Supply
E1	VDDSPK	Supply	Class-D amplifier supply
E2	SPKOUTR+	Analog Output	Class-D amplifier Right Channel positive Output
E3	TEST	N/C	Class-D amplifier Test point

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E5	VREF	Analog I/O	Internal DAC & ADC voltage reference decoupling I/O
E6	VDDMIC	Supply	Microphone supply
E7	MICDET	Analog Input	Microphone button detection input
F1	VSSSPK	Ground	Class-D amplifier supply ground
F2	SPKOUTR-	Analog Output	Class-D amplifier Right Channel negative Output
F3	VDDSPK	Supply	Class-D amplifier supply
F4	HPL	Analog Output	Headphone left channel output
F6	VSSA	Ground	Analog Supply Ground
F7	VDDA	Supply	Analog Supply
G1	VDDSPK	Supply	Class-D amplifier supply
G2	SPKOUTL-	Supply	Class-D amplifier Left Channel negative Output
G3	VSSSPK	Ground	Class-D amplifier supply ground
G4	HPR	Analog Output	Headphone right channel output
G5	CPCA	Analog I/O	Charge Pump switching capacitor node A
G6	CPOUTP	Analog I/O	Charge Pump positive voltage
G7	VCCP1	Supply	Charge Pump Supply
H1	VSSSPK	Ground	Class-D amplifier supply ground
H2	SPKOUTL+	Analog Output	Class-D amplifier Left Channel positive Output
H3	VDDSPK	Supply	Class-D amplifier supply
H4	HPCOM	Analog Input	Headphone ground reference
H5	CPOUTN	Analog I/O	Charge Pump negative voltage
H6	CPCB	Analog I/O	Charge Pump switching capacitor node B
H7	VSSCP	Ground	Charge Pump Supply ground

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Recommended Operating Conditions

Condition	Symbol	Min	Typical	Max	Units
Digital Supply Range	$V_{DD}C$	1.1	1.2	1.98	V
Digital Supply Range for FLL operation and for Fs > 48KHz	$V_{DD}C$	1.61	1.8	1.98	V
Digital I/O Supply Range	$V_{DD}B$	1.6	1.8	3.6	V
Analog Supply Range	$V_{DD}A$	1.6	1.8	2.0	V
Headphone Supply Range	$V_{DD}A$	1.6	1.8	2.0	V
Loudspeaker Supply Range	$V_{DD}SPK$	2.5	4.2	5.0	V
Microphone Bias Supply Voltage	$V_{DD}MIC$	2.5	4.2	5.0	V
Temperature Range	T_A	-40		+85	°C

Absolute Maximum Ratings

Parameter	Min	Max	Units
Digital Supply Range	-0.3	2.2	V
Digital I/O Supply Range	-0.3	6.0	V
Analog Supply Range	-0.3	2.2	V
Headphone Supply Range	-0.3	2.2	V
Loudspeaker Supply Range	-0.3	6.0	V
Microphone Bias Supply Voltage	-0.3	6.0	V
Voltage Input Digital Range	DGND - 0.3	V_{DD} + 0.3	V
Voltage Input Analog Range	AGND - 0.3	V_{DD} + 0.3	V
Junction Temperature, T_J	-40	+150	°C
Storage Temperature	-65	+150	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods. Exposure to such conditions may adversely influence product reliability and result in failures not covered by warranty.

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Electrical Characteristics

Conditions: $V_{DD}A = V_{DD}B = V_{DD}C = 1.8V$; $V_{DD}SPK = V_{DD}MIC = 4.2V$, MCLK = 12.288MHz, R_L(Loudspeaker) = 8 Ω+68uH, R_L(Headphone) = 32 Ω, f = 1kHz, fs = 48KHz unless otherwise specified. Limits apply for T_A = 25°C

Symbol	Parameter	Conditions	Typical	Limit	Units (Limit)
ISD	Shutdown Current	$V_{DD}A$	0.2	1	µA
		$V_{DD}A$	0.2	1	
		$V_{DD}B$	0.2	1	
		$V_{DD}C$	2	10	
		$V_{DD}SPK$	0.2	1	
		$V_{DD}MIC$	0.2	1	
I_{DD}	Standby Mode	MCLK off, Jack Insertion IRQ enabled	5		µA
Speaker Amplifier					
P_O	Output Power	DAC Input, $V_{DD}SPK$ = 4.2V, f = 1kHz, 20kHz BW R_L = 8Ω, THD+N = 1%	970		mW
		DAC Input, $V_{DD}SPK$ = 3.7V, f = 1kHz, 20kHz BW R_L = 8Ω, THD+N = 1%	740		mW
		$V_{DD}SPK$ = 5.0V, f = 1kHz, 20kHz BW R_L = 4Ω, THD+N = 10%	2.9		W
THD+N	Total Harmonic Distortion + Noise	R_L = 8Ω, f = 1kHz, P_O = 300mW	-77		dB
SNR	Signal to Noise Ratio	P_O = 1W, $V_{DD}SPK$ = 4.2V, DAC Input, f = 1kHz, A-Weighted	100		dB
PSRR	Power Supply Rejection Ratio	f_{RIPPLE} = 217Hz, V_{RIPPLE} = 200mV_{PP} Input Referred, SPK_GAIN = 0dB DAC Input, DAC_Gain = 0dB, Ripple Applied to $V_{DD}SPK$ = 4.2V	80		dB
η	Efficiency	$V_{DD}SPK$ = 4.2V, 1% THD, R_L = 8Ω	87		%
X_{TALK}	Channel Crosstalk	Left Channel to Right Channel, P_O = 500mW, f = 1kHz	-100		dB
Headphone Amplifier					
P_O	Output Power	Stereo R_L = 32Ω, DAC Input, CPV_{DD} = 1.8V, f = 1kHz, 20kHz BW, THD+N = 1%, QFN Package	27		mW
		Stereo R_L = 32Ω, DAC Input, CPV_{DD} = 1.8V, f = 1kHz, 20kHz BW, THD+N = 1%, CSP Package	30		mW
THD+N	Total Harmonic Distortion + Noise	R_L = 32Ω, f=1kHz, P_O = 20mW	-77		dB
SNR	Signal to Noise Ratio	VOUT = $1V_{RMS}$, DAC Input, DAC_Gain = 0dB, HP_Gain = 0dB, Digital Zero Input, f = 1kHz, A-Weighted	103		dB

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Symbol	Parameter	Conditions	Typical	Limit	Units (Limit)
PSRR	Power Supply Rejection Ratio	f_{RIPPLE} = 217Hz, V_{RIPPLE} = 200mV_{P_P} Input Referred, HP_GAIN = 0dB DAC Input, DAC_Gain = 0dB Ripple Applied to $V_{DD}A$	80		dB
V_{OS}	Output Offset Voltage	HP_Gain = 0dB, DAC_Gain = 0dB, DAC Input	±0.25	±1	mV
X_{TALK}	Channel Crosstalk	Left Channel to Right Channel, P_O = 3mW, f = 1kHz	-75		dB
P_C	Power Consumption	MP3 Playback in Quiescent, VDDC = 1.2V, R_L = 32 ohm, fs = 44.1KHz	6		mW
		MP3 Playback with 1mW/Channel Stereo Output, Input = 1KHz Sine, VDDC = 1.2V, R_L = 32 ohm, fs = 44.1KHz	14.5		mW
ADC					
THD+N	ADC Total Harmonic Distortion + Noise	MIC Input, MIC_GAIN = -3dB, VIN = 1Vrms, f = 1kHz, Fs = 48kHz	-85		dB
SNR	Signal to Noise Ratio	Reference = VOUT(0dBFS), A-Weighted, MIC Input, MIC Gain = 0dB,fs = 8kHz, Mono Differential Input	100		dB
		Reference = VOUT(0dBFS), A-Weighted, MIC Input, MIC Gain = 6dB,fs = 8kHz, Mono Differential Input	98		dB
		Reference = VOUT(0dBFS), A-Weighted, Stereo Input, Gain = 0dB,fs = 48kHz	100		dB
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{PP} applied to $V_{DD}A$, f_{RIPPLE} = 217Hz, Input Referred, MIC_GAIN = 0dB Differential Input	65		dB
FS_{ADC}	ADC Full Scale Input Level	$V_{DD}A$ = 1.8V	1		V_{RMS}

Digital I/O

Parameter	Symbol	Comments/Conditions		Min	Max	Units
Input LOW level	VIL	VDDB = 1.8V			0.33*VDDB	V
		VDDB = 3.3V			0.37*VDDB	
Input HIGH level	VIH	VDDB = 1.8V		0.67*VDDB		V
		VDDB = 3.3V		0.63*VDDB		
Output HIGH level	VOH	ILoad = 1mA	VDDB = 1.8V	0.9*VDDB		V
			VDDB = 3.3V	0.95*VDDB		
Output LOW level	VOL	ILoad = 1mA	VDDB = 1.8V		0.1*VDDB	V
			$V_{DD}B$=3.3V		0.05*$V_{DD}B$	

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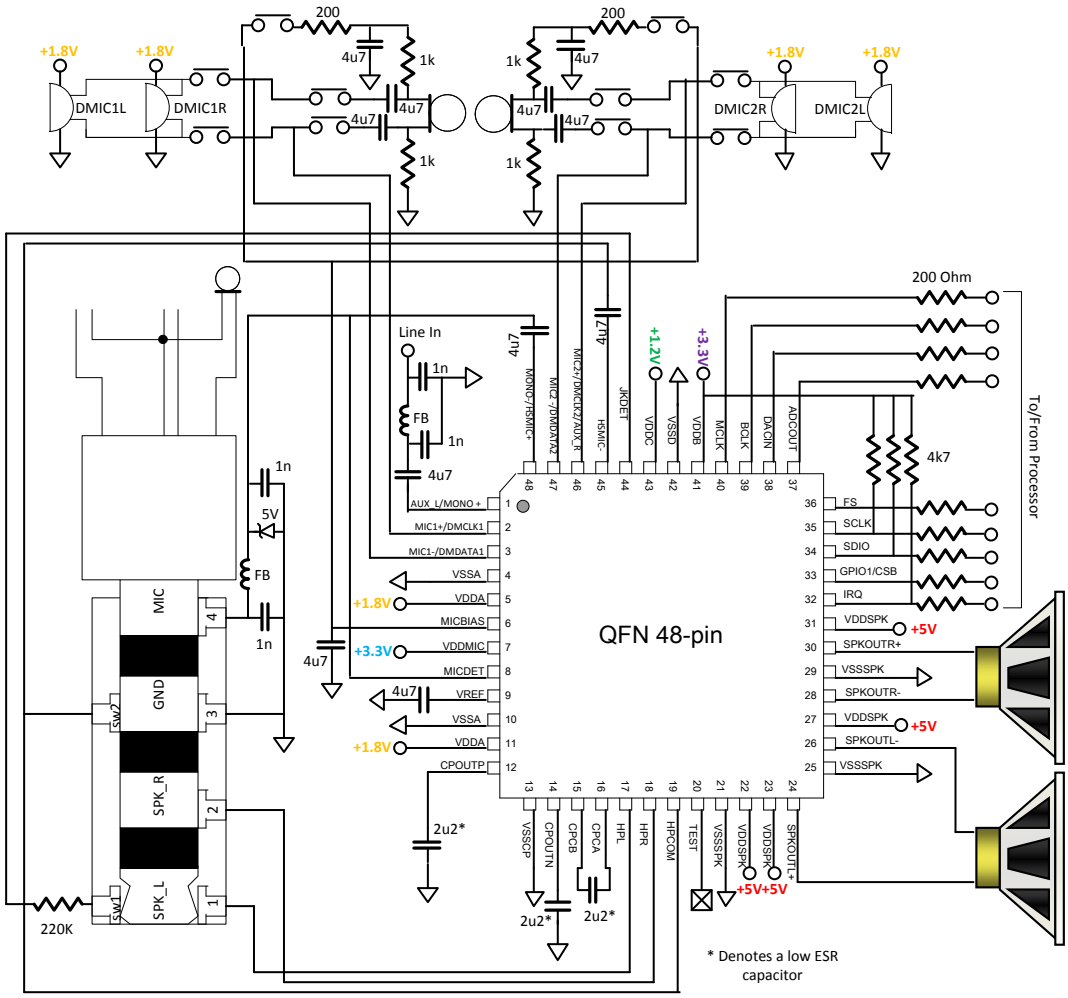
Typical Application Diagram



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Ordering Information

Part Number	Dimension	Package	Package Material
NAU88L24IG	6 X 6 mm	QFN-48L	Green
NAU88L24VG	3.22 X 3.66 mm	56 Balls WLCSP	Green

Nuvoton Part Number Description

NAU88L24IG

Package Material:

G = Green

Package Type:

I = QFN Package

V = WLCSP Package

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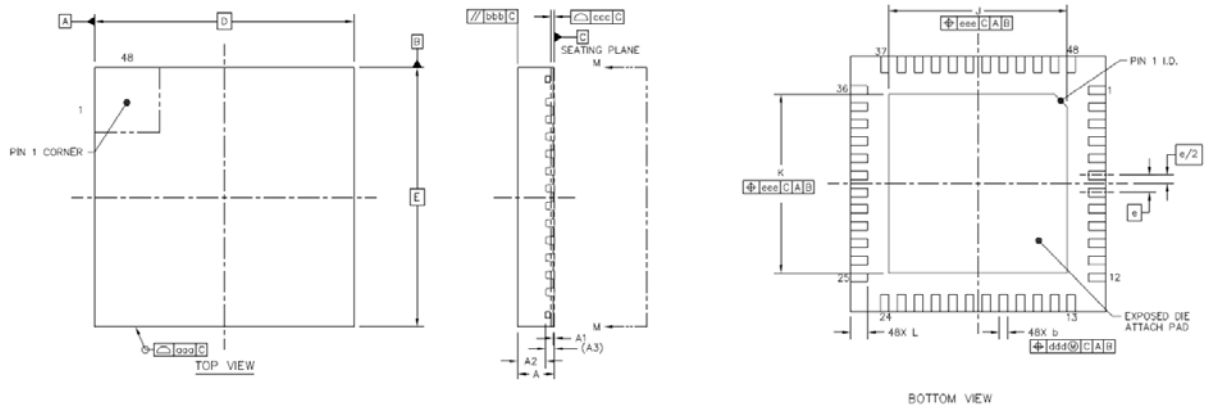
Package Information

Package Information

QFN 48L 6X6 MM^2, Thickness: 0.9 mm (Max) Pitch 0.4mm



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	0.67
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		6 BSC	
	Y	E		6 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	J	4.1	4.2	4.3
	Y	K	4.1	4.2	4.3
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

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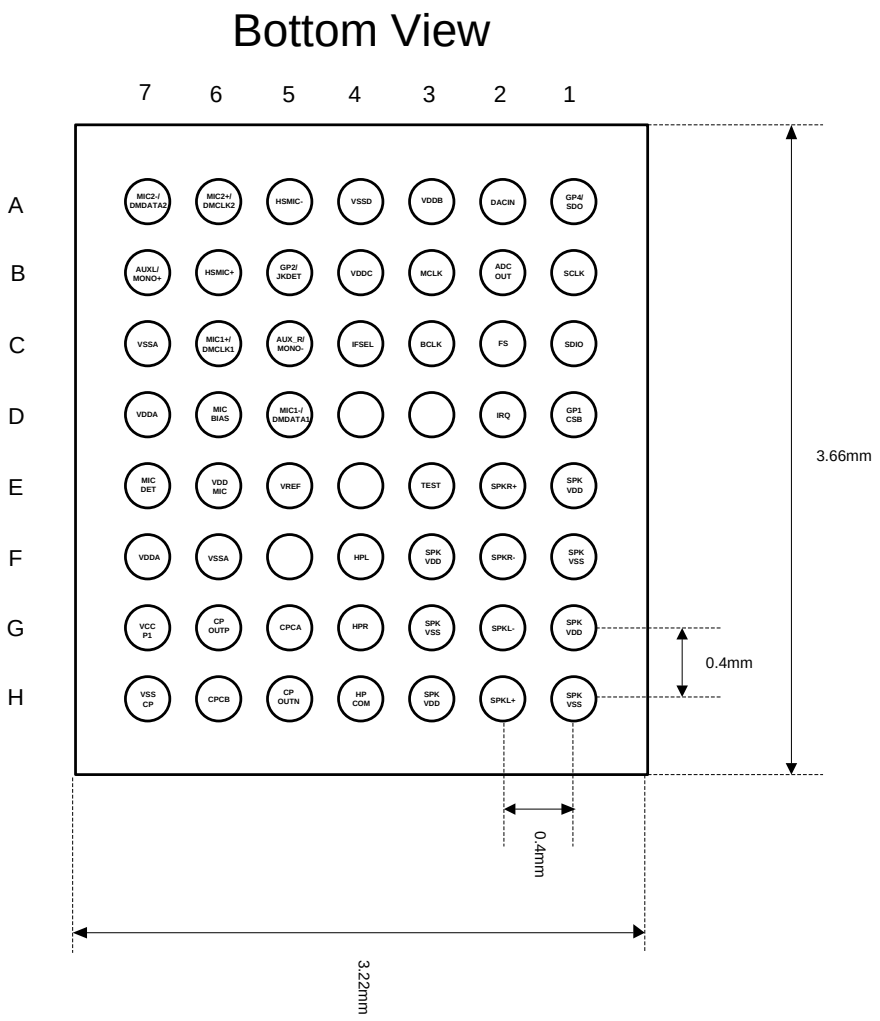
Package Information

56 Balls WLCSP with Pitch 0.4mm



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Version History

VERSION	DATE	PAGE	DESCRIPTION
1.0	12/08/2014	NA	First Created
1.1	2/24/2015	7, 8	Changed the standby current per latest test results Removed active current, and created headphone MP3 playback power consumption SPEC under headphone.
1.2	4/1/2015	11, 10	Updated the package infor. Corrected the package type on ordering info.
1.3	05/18/2015		Added CSP package option. Updated the block diagram.
1.4	05/22/2015		Added 6X6mm QFN 48 package option
1.5	09/28/2015	1, 13, 11	Updated description Updated ordering information with examples Changed VIH (Input High Voltage)
1.6	02/27/2017		Removed 7mm x 7mm QFN 48 package option

Important Notice

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