Datasheet

Voltage Tracker

50 mA Output Voltage Tracker

BD42500G-C

General Description

The BD42500G-C is low quiescent regulators featuring 45 V absolute maximum voltage, and output voltage tracking accuracy of ±15 mV, 50 mA output current and 40 µA (Typ) current consumption.
This tracker is therefore ideal for applications requiring a direct connection to the battery and a low current consumption.
Ceramic capacitors can be used for compensation of the output capacitor phase. Furthermore, this IC also feature overcurrent protection to protect the device from damage caused by short-circuiting and an integrated thermal shutdown to protect the device from overheating at overload conditions.

Features

- AEC-Q100 Qualified (Note 1)
- Qualified for Automotive Applications
- Wide Temperature Range (Tj): -40 °C to +150 °C
- Wide Operating Input Range: 3 V to 42 V
- Low Quiescent Current: 40 µA (Typ)
- Output Voltage Tracking Accuracy: ±15 mV
- Over Current Protection (OCP)
- Thermal Shutdown Protection (TSD)

(Note 1: Grade 1)

Package

W (Typ) x D (Typ) x H (Max)

- G: SSOP5 2.90 mm x 2.80 mm x 1.25 mm

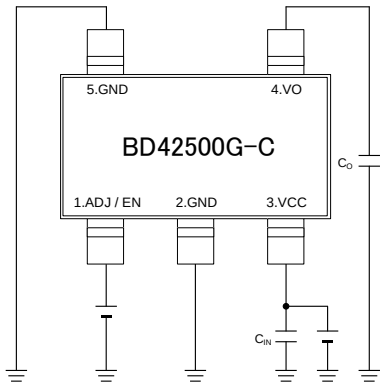


Applications

- Automotive
  (Engine-ECU, Body, Air-Conditioner etc.)

Typical Application Circuits

- Components externally connected: 1 µF ≤ C_{IN}, 1 µF ≤ C_O (Min)
  Electrolytic, tantalum and ceramic capacitors can be used.



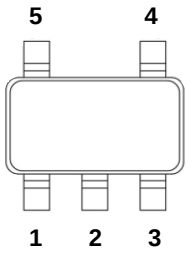
○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

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Pin Configuration

SSOP5
(Top View)



Pin Description

SSOP5

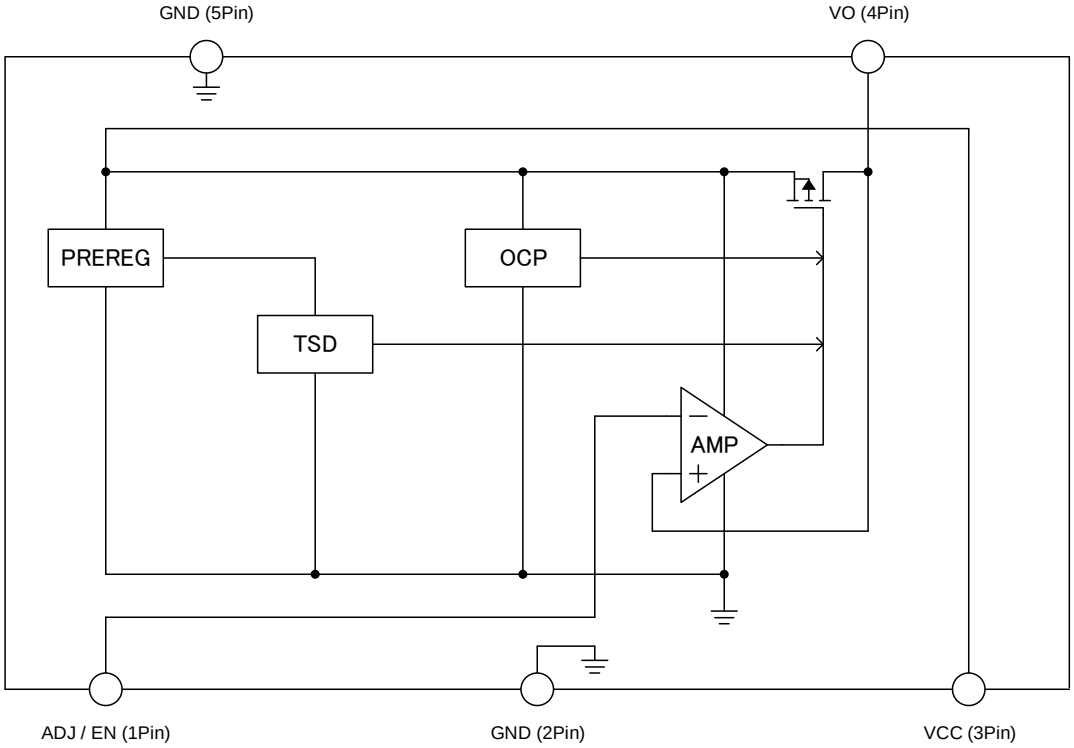
Pin No.	Pin Name	Function
1	ADJ / EN	Output Control Voltage
2	GND	Ground
3	VCC	Input
4	VO	Output
5	GND	Ground

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Block Diagram

SSOP5



Description of Blocks

Block Name	Function	Description of Blocks
PREREG	Internal Power Supply	Power Supply for Internal Circuit.
TSD	Thermal Shutdown Protection	The TSD protect the device from overheating. If the chip temperature (Tj) reaches ca. 175 °C (Typ), the output is turned off.
OCP	Over Current Protection	The OCP protect the device from damage caused by over current.
AMP	Output Power Transistor Driver Amplifier	The amplifier drives output power transistor with ADJ/EN voltage as reference voltage.
Power Tr.	Output Power Transistor	PDMOS type output power transistor.

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Absolute Maximum Ratings

Parameter		Symbol	Ratings	Unit
Supply Voltage (Note 1)		V_{CC}	-0.3 to +45	V
Output Control Voltage		$V_{ADJ\ /\ EN}$	-0.3 to +28	V
Output Voltage		V_O	-0.3 to +28	V
Junction Temperature Range		Tj	-40 to +150	°C
Storage Temperature Range		Tstg	-55 to +150	°C
Maximum Junction Temperature		Tjmax	+150	°C
ESD withstand Voltage	HBM (Note 2)	$V_{ESD,\ HBM}$	±2000	V
	CDM (Note 3)	$V_{ESD,\ CDM}$	±1000	V

(Note 1) Do not exceed Junction Temperature.

(Note 2) Human Body Model.

(Note 3) Charged Device Model.

(Caution) Exceeding the absolute maximum rating for supply voltage, operating temperature or other parameters can result in damages to or destruction of the chip. In this event it also becomes impossible to determine the cause of the damage (e.g. short circuit, open circuit, etc.). Therefore, if any special mode is being considered with values expected to exceed the absolute maximum ratings, implementing physical safety measures, such as adding fuses, should be considered.

Operating Conditions (-40 °C ≤ Tj ≤ +150 °C)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Note 1)	V_{CC}	5.3	42	V
Tracking Voltage (Note 2)	$V_{ADJ\ /\ EN}$	2.5	16	V
Start-Up Voltage (Note 3)	V_{CC}	3	–	V
Output Current	I_O	0	50	mA
Ambient Temperature Range	Ta	-40	125	°C

(Note 1) $V_{ADJ/EN}$ = 5V, I_O = 50 mA

(Note 2) $V_{ADJ/EN}$ ≤ Vcc – 0.5V

(Note 3) I_O = 0 mA

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Thermal Resistance(Note 1)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 3)	2s2p(Note 4)	
SSOP5				
Junction to Ambient	θ_{JA}	376.5	185.4	°C/W
Junction to Top Characterization Parameter(Note 2)	Ψ_{JT}	40	30	°C/W

(Note 1)Based on JESD51-2A(Still-Air)
(Note 2)The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3)Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

(Note 4)Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

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Electrical Characteristics

(Unless otherwise specified, -40 °C ≤ Tj ≤ +150 °C, V_{CC} = 13.5 V, $V_{ADJ / EN}$ = 5 V, I_O = 0 mA.
The Typical value is defined at Tj = 25 °C.)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Circuit Current	I_{CC}	-	40	80	μA	Io ≤ 50 mA
Output Voltage Tracking Accuracy	ΔVo	-15	-	15	mV	6 V ≤ V_{CC} ≤ 40 V 1 mA ≤ I_O ≤ 50 mA
Dropout Voltage	ΔVd	-	0.12	0.3	V	V_{CC} = V_O × 0.95 (= 4.75 V: Typ) I_O = 50 mA
Ripple Rejection	R.R.	-	80	-	dB	f = 120 Hz, ein = 1 Vrms I_O = 10 mA
Thermal Shut Down	TSD	-	175	-	°C	Tj at TSD ON

Electrical Characteristics (Output Control Function)

(Unless otherwise specified, -40 °C ≤ Tj ≤ +150 °C, V_{CC} = 13.5 V, Io = 0 mA. The Typical value is defined at Tj = 25 °C.)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Shutdown Current	Ishut	-	1	5	μA	$V_{ADJ / EN}$ ≤ 0.4 V Tj ≤ 125 °C
ADJ / EN ON Mode Voltage	VthH	2	-	16	V	Active Mode
ADJ / EN OFF Mode Voltage	VthL	0	-	0.4	V	Off Mode
ADJ / EN Bias Current	$I_{ADJ / EN}$	-	1	3	μA	$V_{ADJ / EN}$ = 5V

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Typical Performance Curves

Unless otherwise specified: -40 °C ≤ Tj ≤ +150 °C, V_{CC} = 13.5 V, $V_{ADJ/EN}$ = 5 V, Io = 0 mA.

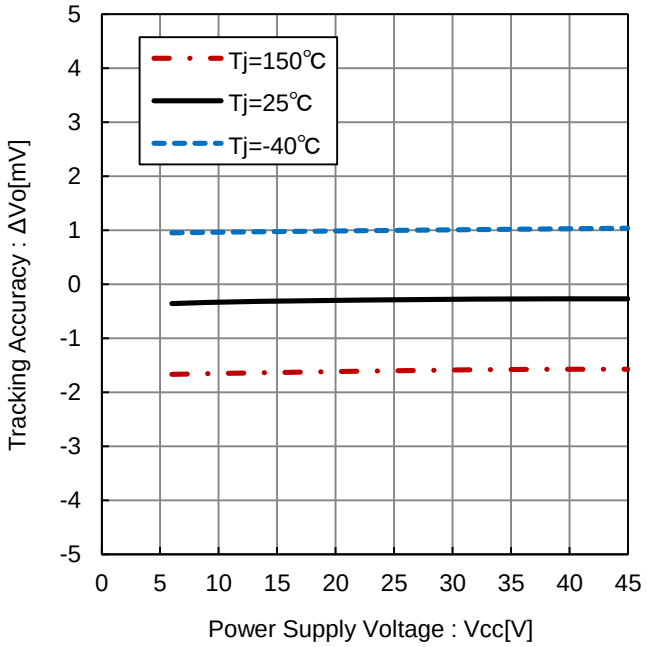


Figure 1. Tracking Accuracy vs. Power Supply Voltage

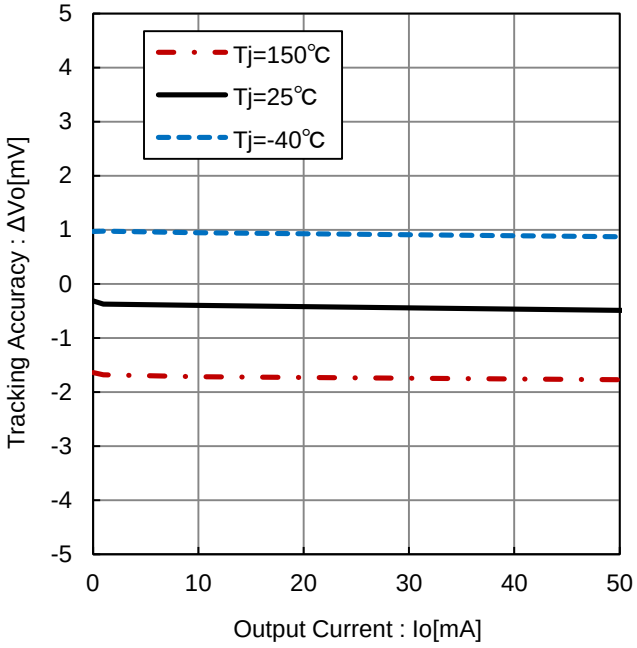


Figure 2. Tracking Accuracy vs. Output Current

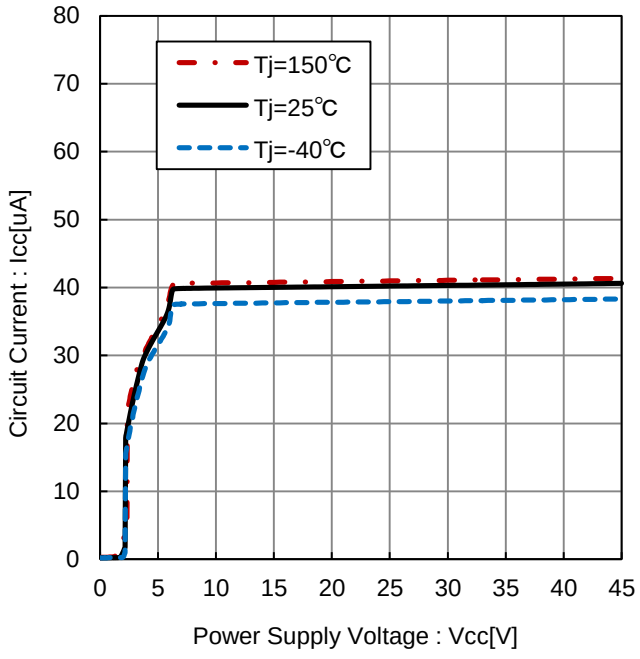


Figure 3. Circuit Current vs. Power Supply Voltage

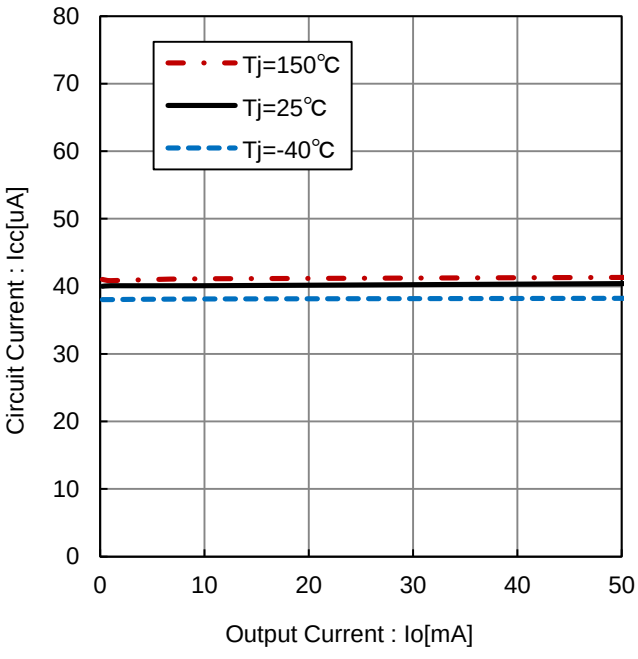


Figure 4. Circuit Current vs. Output Current

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Typical Performance Curves – continued

Unless otherwise specified: -40 °C ≤ Tj ≤ +150 °C, V_{CC} = 13.5 V, $V_{ADJ/EN}$ = 5 V, Io = 0 mA.

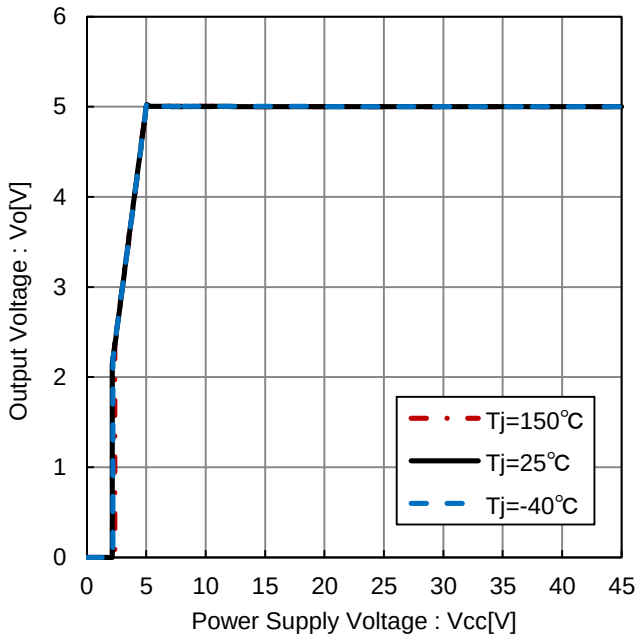


Figure 5. Output Voltage vs. Power Supply Voltage

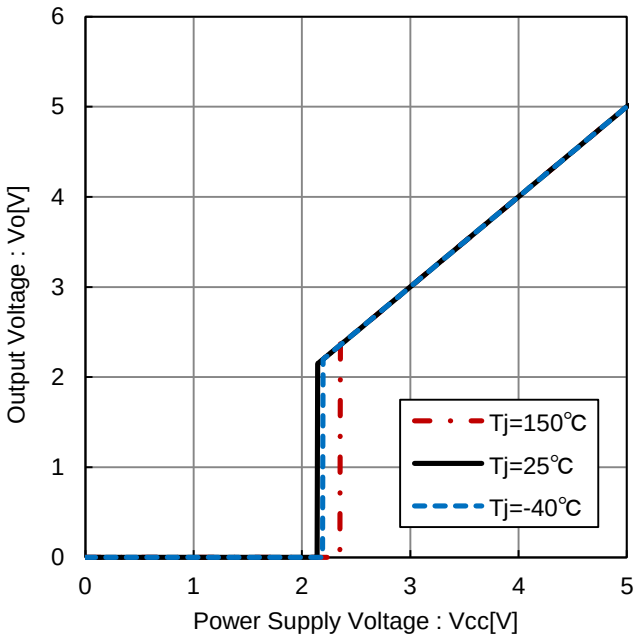


Figure 6. Output Voltage vs. Power Supply Voltage at Low Supply Voltage

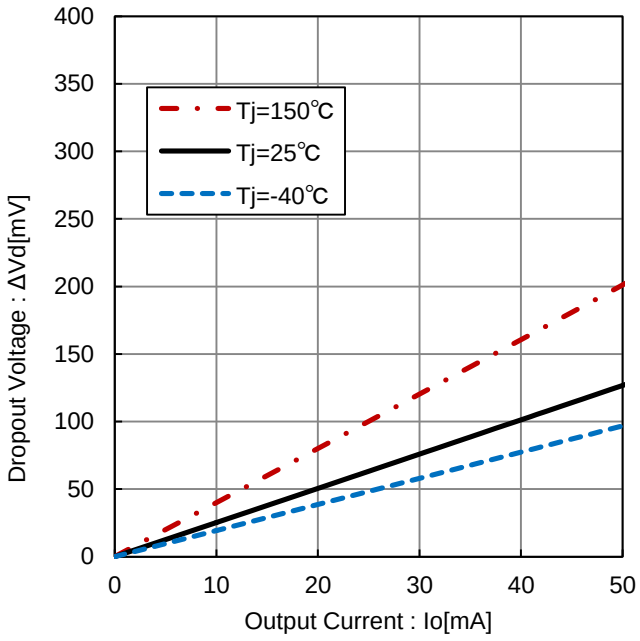


Figure 7. Dropout Voltage vs. Output Current (Vcc=4.75V)

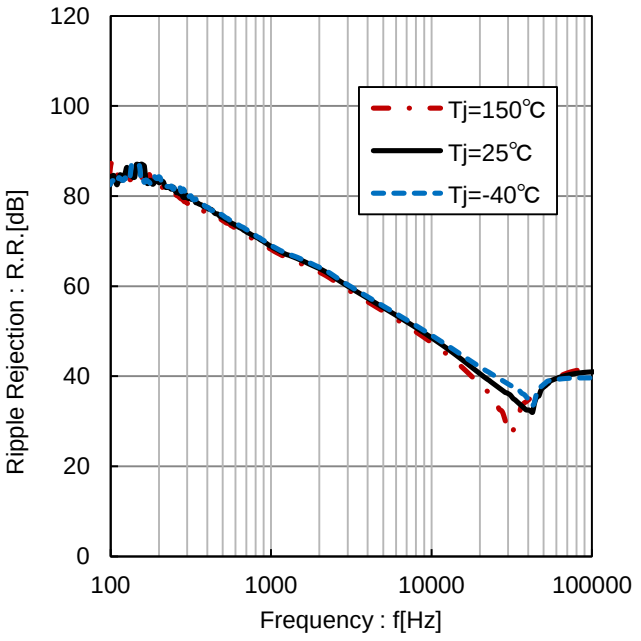


Figure 8. Ripple Rejection vs. Frequency (ein=1Vrms, Io=10mA)

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Typical Performance Curves – continued

Unless otherwise specified: -40 °C ≤ Tj ≤ +150 °C, V_{CC} = 13.5 V, $V_{ADJ/EN}$ = 5 V, Io = 0 mA.

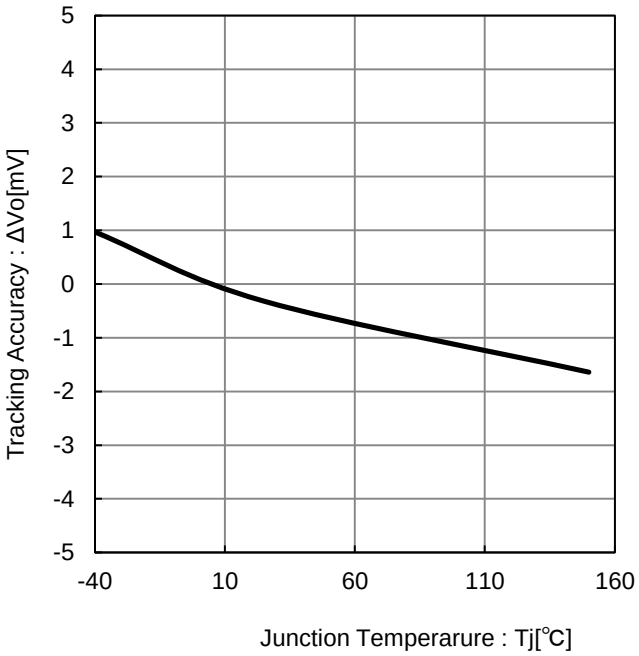


Figure 9. Tracking Accuracy vs. Junction Temperature (Io=10mA)

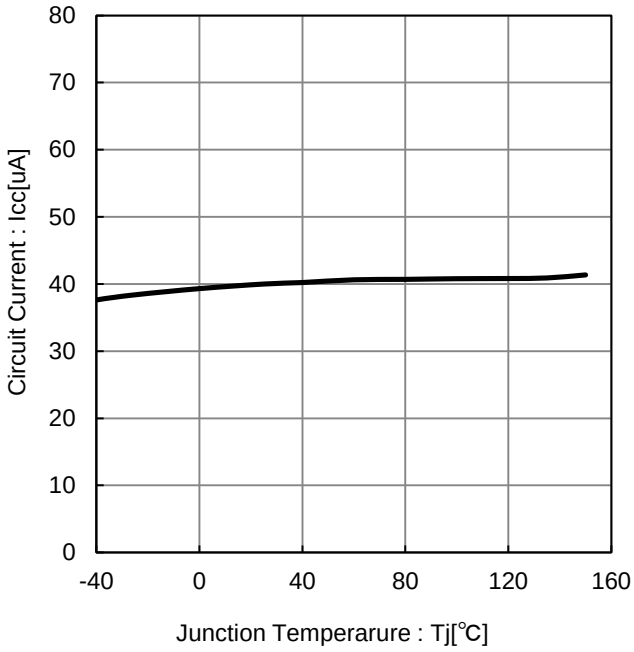


Figure 10. Circuit Current vs. Junction Temperature

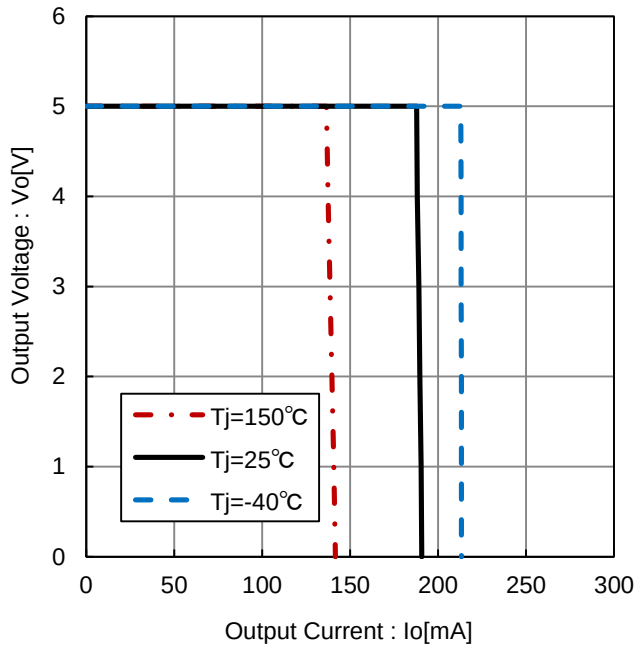


Figure 11. Output Voltage vs. Output Current (Over Current Protection)

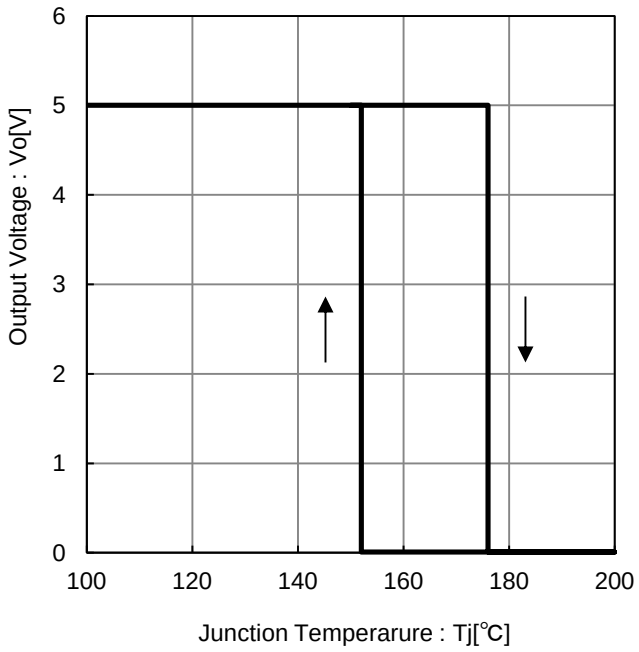


Figure 12. Output Voltage vs. Junction Temperature (Thermal Shut Down)

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Typical Performance Curves – continued

Unless otherwise specified: -40 °C ≤ Tj ≤ +150 °C, V_{CC} = 13.5 V, $V_{ADJ/EN}$ = 5 V, Io = 0 mA.

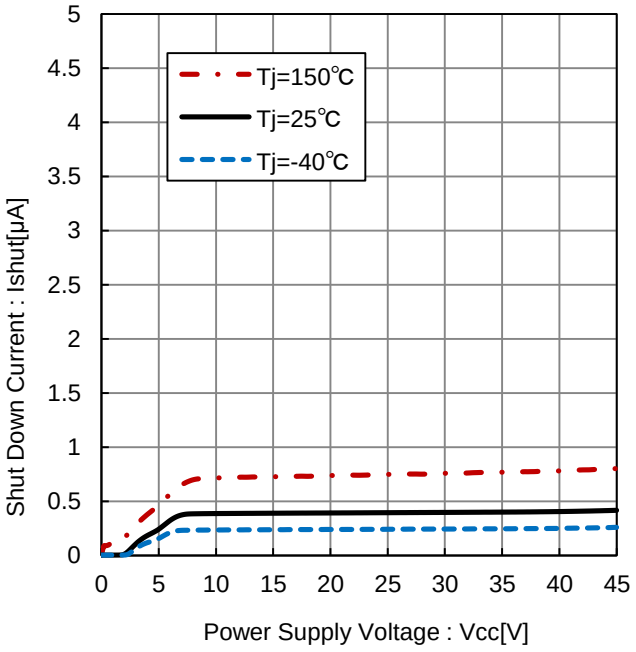


Figure 13. Shut Down Current vs. Power Supply Voltage

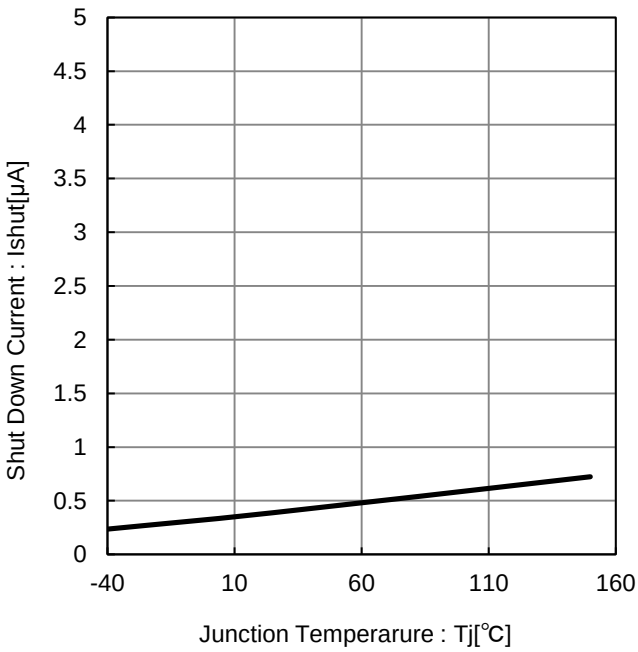


Figure 14. Shut Down Current vs. Junction Temperature

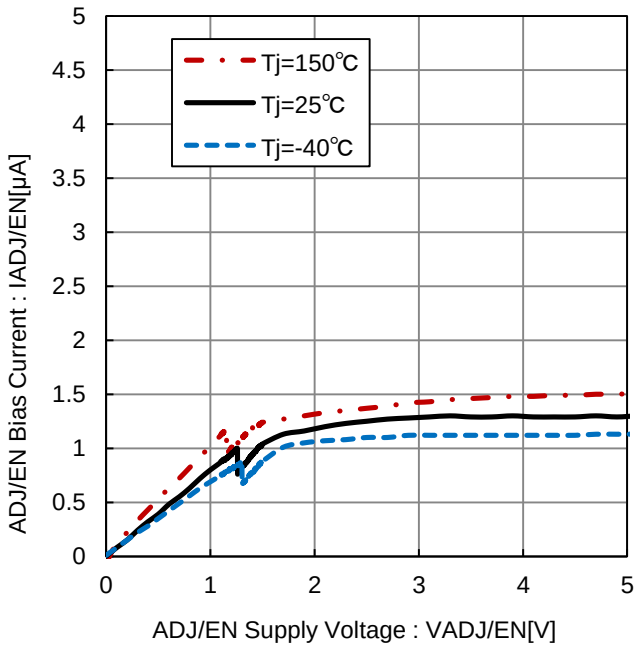


Figure 15. ADJ/EN Bias Current vs. ADJ/EN Supply Voltage

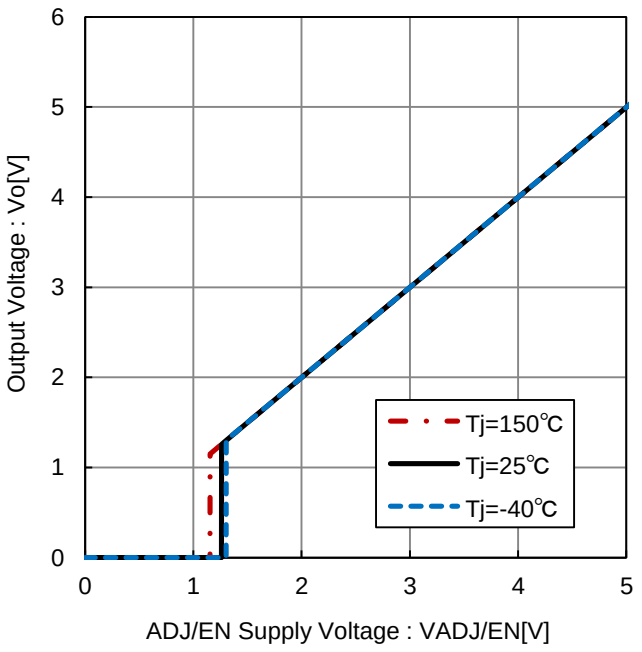
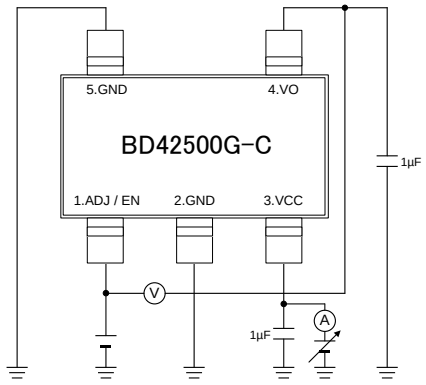


Figure 16. Output Voltage vs. ADJ/EN Supply Voltage

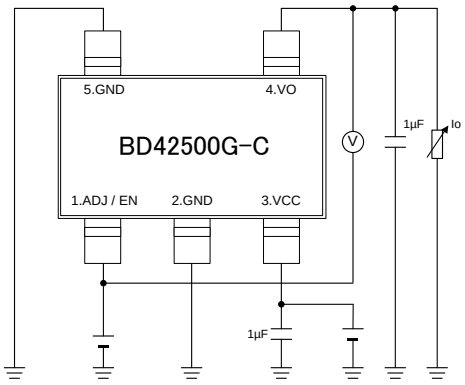
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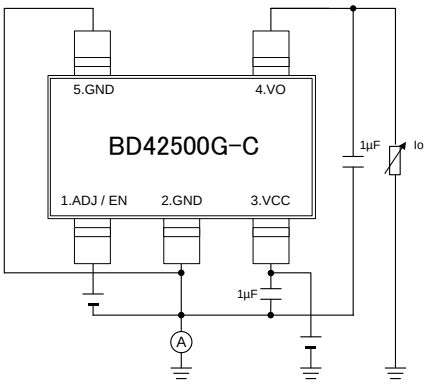
Measurement Circuit



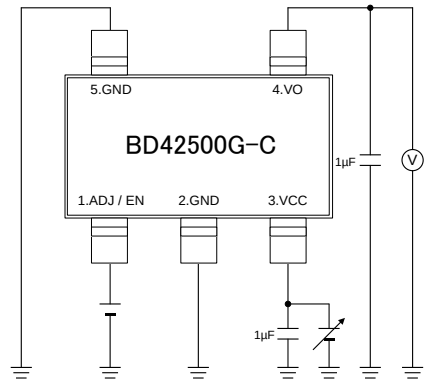
Measurement Setup for
Figure 1, 3, 10



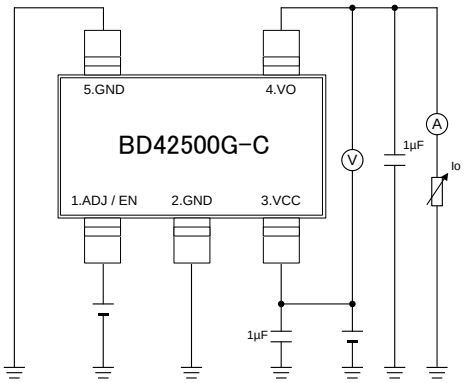
Measurement Setup for
Figure 2, 9



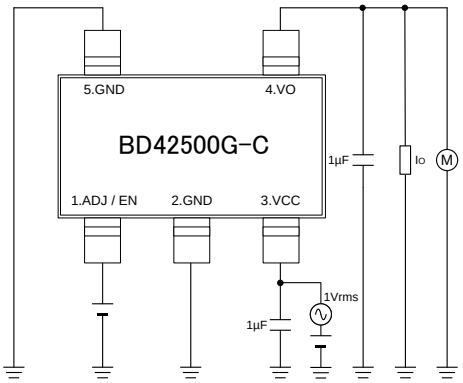
Measurement Setup for
Figure 4



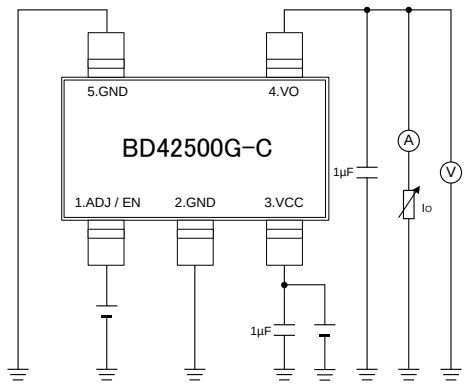
Measurement Setup for
Figure 5, 6, 12



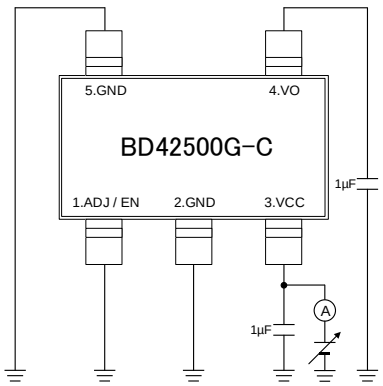
Measurement Setup for
Figure 7



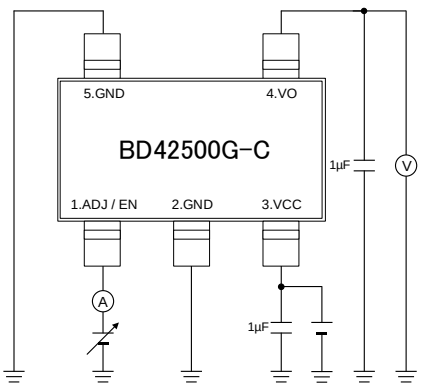
Measurement Setup for
Figure 8



Measurement Setup for
Figure 11



Measurement Setup for
Figure 13, 14



Measurement Setup for
Figure 15, 16

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Selection of Components Externally Connected

- VCC Pin

  Insert Capacitors with a capacitance of 1 µF (Min) or higher between the VCC and GND. Choose the capacitance according to the line between the power smoothing circuit and the VCC. Selection of the capacitance also depends on the application. Verify the application and allow sufficient margins in the design. We recommend to mount the capacitor as close as possible to the pin. When selecting the capacitor ensure that the capacitance of 1 µF or higher is maintained at the intended applied voltage and temperature range.

- Output Pin Capacitor

  In order to prevent oscillation, a capacitor needs to be placed between the output pin and GND. We recommend using a capacitor with a capacitance of 1 µF (Min) or higher. Electrolytic, tantalum and ceramic capacitors can be used. When selecting the capacitor ensure that the capacitance of 1 µF or higher is maintained at the intended applied voltage and temperature range. Capacitance fluctuation due to changes in temperature can possibly result in oscillation. For selection of the capacitor refer to the data of Figure 18.

  The stable operation range given in the data of Figure 17 is based on the standalone IC and resistive load. For actual applications the stable operating range is influenced by the PCB impedance, input supply impedance and load impedance. Therefore verification of the final operating environment is needed.

  When selecting a ceramic type capacitor, we recommend using X5R, X7R or better with excellent temperature and DC-biasing characteristics and high voltage tolerance.

  Also, in case of rapidly changing input voltage and load current, select the capacitance in accordance with verifying that the actual application meets with the required specification. Mount the capacitor as close as possible to the connected pin.

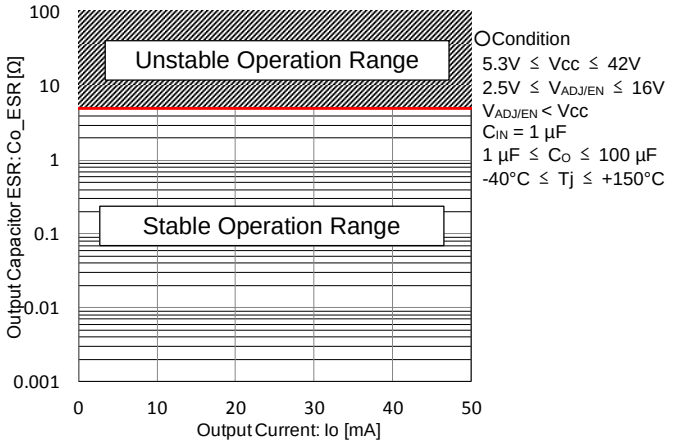


Figure 17. Output Pin Capacitor ESR vs Output Current

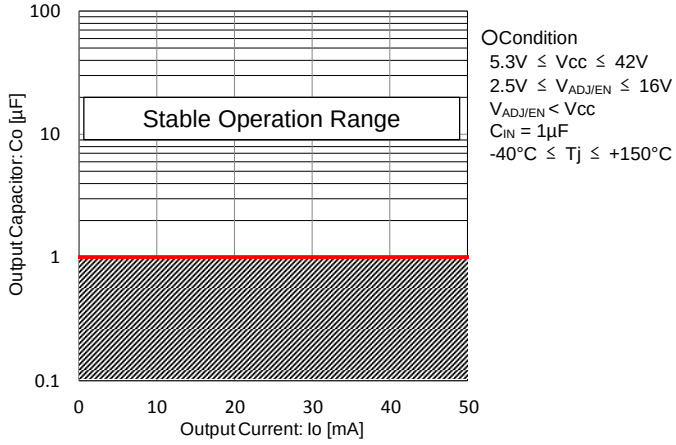


Figure 18. Output Pin Capacitor vs Output Current

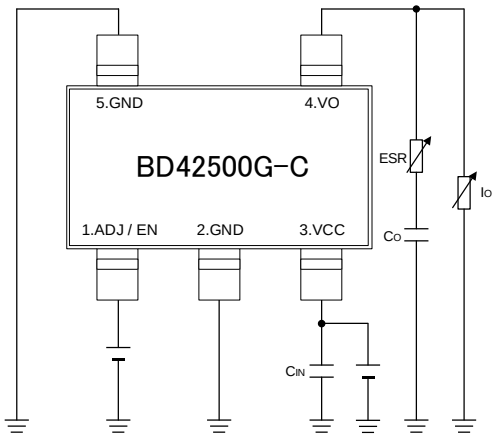


Figure 19. Measurement Setup for ESR Reference Data

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Power Dissipation

■SSOP5

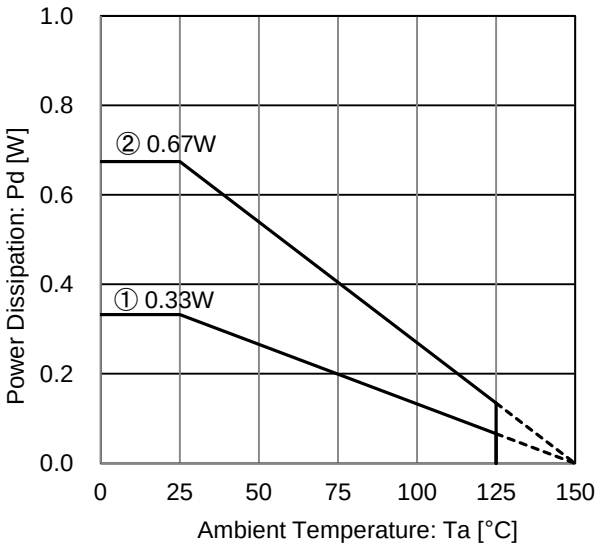


Figure 20. Package Data
(SSOP5)

IC mounted on ROHM standard board based on JEDEC.

① : 1 - layer PCB
(Copper foil area on the reverse side of PCB: 0 mm x 0 mm)
Board material: FR4
Board size: 114.3 mm x 76.2 mm x 1.57 mmt
Mount condition: PCB and exposed pad are soldered.
Top copper foil: ROHM recommended
footprint + wiring to measure, 2 oz. copper.

② : 4 - layer PCB
(2 inner layers and Copper foil area on the reverse side of PCB: 74.2 mm x 74.2 mm)
Board material: FR4
Board size: 114.3 mm x 76.2 mm x 1.60 mmt
Mount condition: PCB and exposed pad are soldered.
Top copper foil: ROHM recommended
footprint + wiring to measure, 2 oz. copper.
2 inner layers copper foil area of PCB
: 74.2 mm x 74.2 mm, 1 oz. copper.
Copper foil area on the reverse side of PCB
: 74.2 mm x 74.2 mm, 2 oz. copper.

Condition①: θ_{JA} = 376.5 °C / W, Ψ_{JT} (top center) = 40 °C / W
Condition②: θ_{JA} = 185.4 °C / W, Ψ_{JT} (top center) = 30 °C / W

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Thermal Design

Within this product, the power consumption is decided by the dropout voltage condition, the load current and the circuit current. Refer to Package Data illustrated in Figure 20 when using the IC in an environment of Ta ≥ 25 °C. Even if the ambient temperature Ta is at 25 °C, depending on the input voltage and the load current, chip junction temperature can be very high. Consider the design to be Tj ≤ Tjmax = 150 °C in all possible operating temperature range.
Should by any condition the maximum junction temperature Tjmax = 150 °C rating be exceeded by the temperature increase of the chip, it may result in deterioration of the properties of the chip. The thermal impedance in this specification is based on recommended PCB and measurement condition by JEDEC standard. Verify the application and allow sufficient margins in the thermal design by the following method is used to calculate the junction temperature Tj.
Tj can be calculated by either of the two following methods.

1. The following method is used to calculate the junction temperature Tj.

$$Tj = Ta + P_C \times \theta_{JA}$$

Where:

Tj	: Junction Temperature
Ta	: Ambient Temperature
P_C	: Power Consumption
θ_{JA}	: Thermal Impedance (Junction to Ambient)

2. The following method is also used to calculate the junction temperature Tj.

$$Tj = T_T + P_C \times \Psi_{JT}$$

Where:

Tj	: Junction Temperature
T_T	: Top Center of Case's (mold) Temperature
P_C	: Power consumption
Ψ_{JT}	: Thermal Impedance (Junction to Top Center of Case)

The following method is used to calculate the power consumption Pc (W).

$$Pc = (V_{CC} - V_O) \times I_O + V_{CC} \times I_{CC}$$

Where:

P_C	: Power Consumption
V_{CC}	: Input Voltage
V_O	: Output Voltage
I_O	: Load Current
I_{CC}	: Circuit Current

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- **Calculation Example (SSOP5)**

If V_{CC} = 13.5 V, V_O = 5.0 V, I_O = 50 mA, I_{CC} = 40 μA, the power consumption Pc can be calculated as follows:

$$P_C = (V_{CC} - V_O) \times I_O + V_{CC} \times I_{CC}$$
$$= (13.5\ V - 5.0\ V) \times 10\ mA + 13.5\ V \times 40\ \mu A$$
$$= 0.085\ W$$

At the ambient temperature Tamax = 85°C, the thermal impedance (Junction to Ambient) θ_{JA} = 185.4 °C / W (4-layer PCB),

$$Tj = Tamax + P_C \times \theta_{JA}$$
$$= 85\ ℃ + 0.085\ W \times 185.4\ ℃ / W$$
$$= 100.8\ ℃$$

When operating the IC, the top center of case's (mold) temperature T_T = 100 °C, Ψ_{JT} = 15 °C / W (1-layer PCB),

$$Tj = T_T + P_C \times \Psi_{JT}$$
$$= 100\ ℃ + 0.085\ W \times 40\ ℃ / W$$
$$= 103.4\ ℃$$

For optimum thermal performance, it is recommended to expand the copper foil area of the board, increasing the layer and thermal via between thermal land pad.

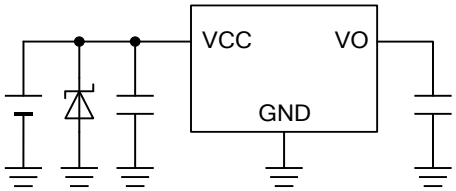
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Application Examples

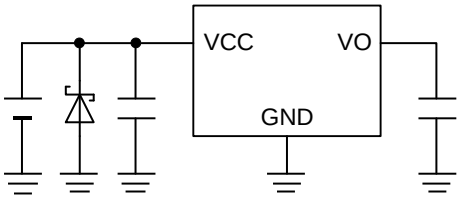
・Applying positive surge to the VCC

If the possibility exists that surges higher than 45 V will be applied to the VCC, a Zener Diode should be placed between the VCC and GND as shown in the figure below.



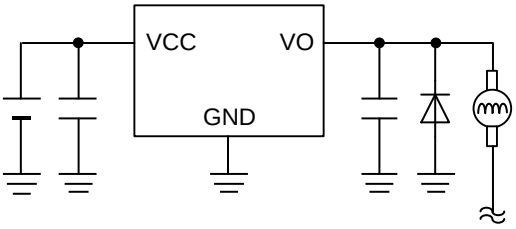
・Applying negative surge to the VCC

If the possibility exists that negative surges lower than the GND are applied to the VCC, a Shottky Diode should be place between the VCC and GND as shown in the figure below.



・Implementing a Protection Diode

If the possibility exists that a large inductive load is connected to the output pin resulting in back-EMF at time of startup and shutdown, a protection diode should be placed as shown in the figure below.



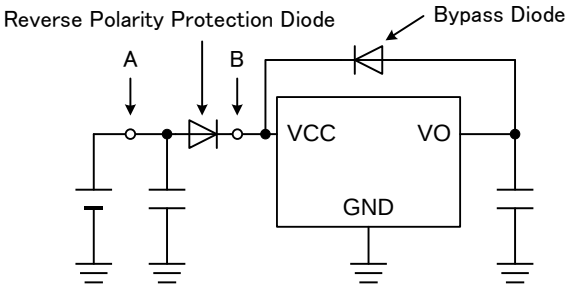
・Reverse Polarity Protection Diode

In some applications, the VCC and pin potential might be reversed, possibly resulting in damage to internal circuit or damage to the element. In instance, when VCC shorts to GND while external capacitor at VO is charged.

Reverse current in case of point A described in below diagram can be prevented by inserting Reverse polarity protection diode in series to the VCC.

When a short of the point B and the GND is concerned after having reverse polarity protection diode inserted, we recommend inserting a bypass diode between the VCC and the VO.

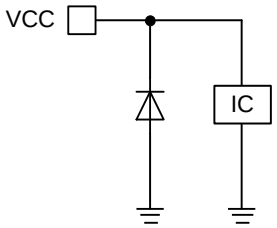
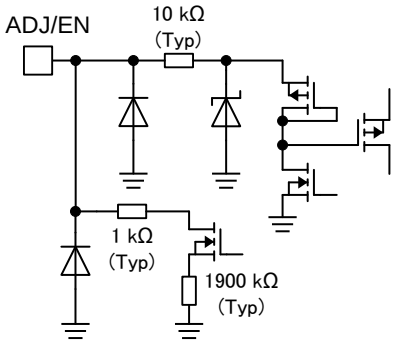
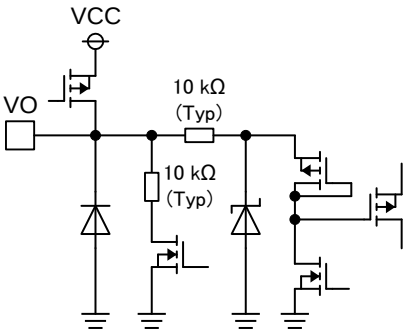
If the reverse polarity protection diode and bypass diode cannot be inserted due to any reasons, use a capacitor with a capacitance with less than 1000µF at $V_{ADJ\,/\,EN}$ = 5V and 100µF at $V_{ADJ\,/\,EN}$ = 16V to avoid damage to the internal circuits or the elements.



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I/O equivalence circuits

1 VCC	2 ADJ/EN	3 VO
		

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

10. **Unused Input Terminals**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

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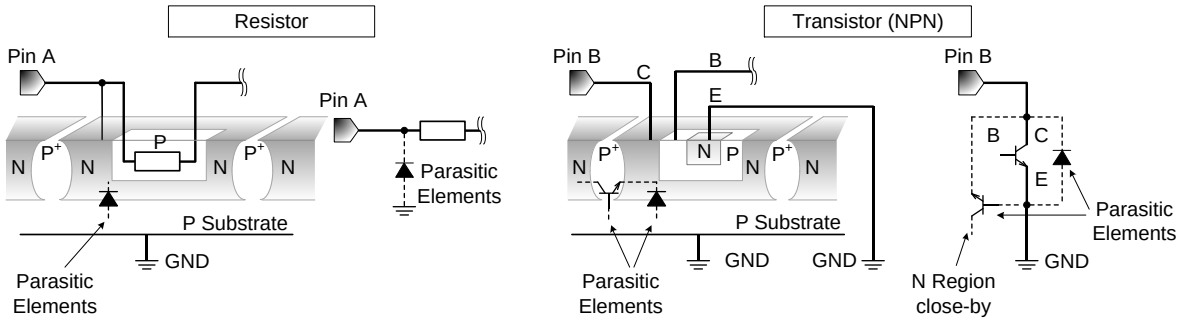
Operational Notes – continued

11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



12. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

13. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

14. Over Current Protection Circuit (OCP)

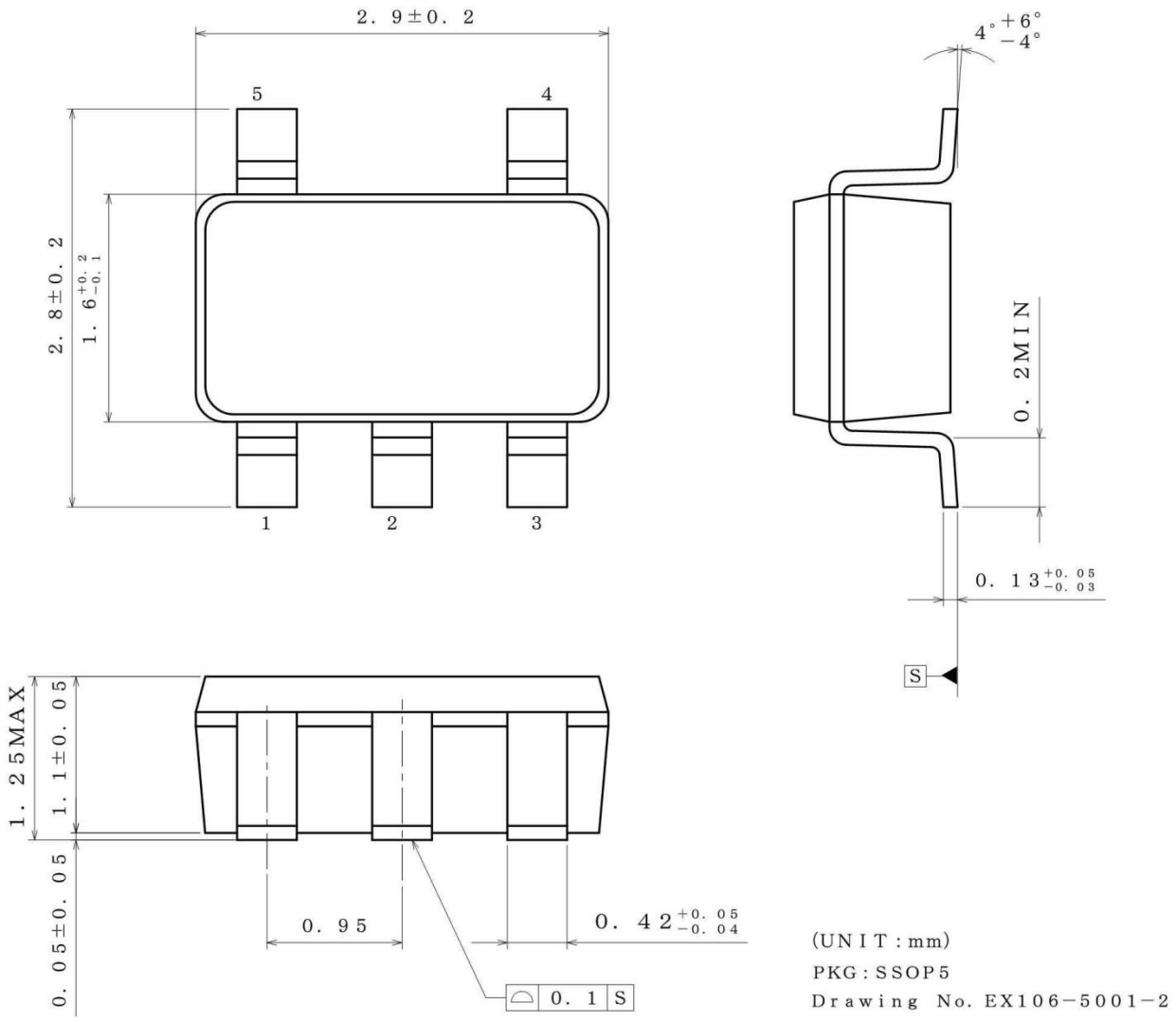
This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

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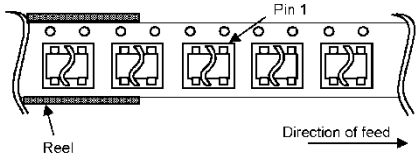
Physical Dimension, Tape and Reel Information

Package Name	SSOP5



< Tape and Reel Information >

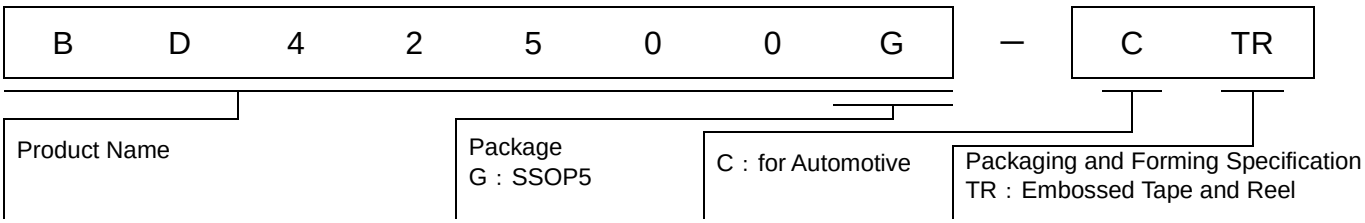
Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



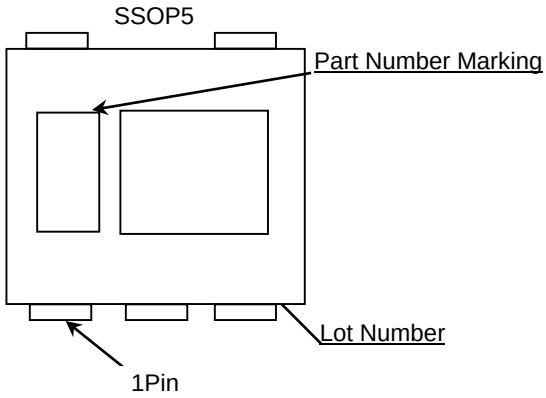
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Ordering Information



Marking Diagrams (Top View)



Part Number	Package	Part Number Marking
BD42500G-C	SSOP5	QY

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Revision History

Date	Revision	Changes
2.Jun.2016	001	New Release

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

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