

1200 V 75 mΩ SiC MOSFET

Silicon Carbide MOSFET

Trench-Assisted Planar Technology

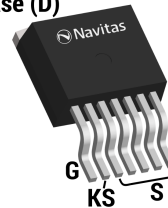
V_{DS}	=	1200 V
$R_{DS(ON)}(Typ.)$	=	75 mΩ
$I_D(T_C = 100^\circ C)$	=	22 A

Features

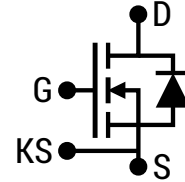
- Gen3F (3rd Generation) Technology
- Most Stable $R_{DS(ON)}$ over Temperature
- Low C_{OSS} , C_{RSS} and Balanced C_{ISS}/C_{RSS}
- Lower Q_{GD} and Balanced $R_{G(INT)}$
- Electromagnetically Optimized Design
- Robust Body Diode with Low V_F and Low Q_{RR}
- 100% Avalanche (UIL) Tested
- AEC-Q101 Qualified

Package

Case (D)



TO-263-7



D = Drain
G = Gate
S = Source
KS = Kelvin Source



Advantages

- Superior Performance and Robustness
- Lowest Conduction Losses at all Temperatures
- Lesser Switching Spikes and Lower Losses
- Faster and More Efficient Switching
- Reduced Ringing
- Ease of Paralleling without Thermal Runaway
- Excellent Power Density and System Efficiency
- Enhanced System Reliability

Applications

- Solar Inverters
- EV/HEV Charging
- UPS
- High Voltage DC-DC Converters
- Switched Mode Power Supplies
- Motor Drives
- Smart Grid Transmission and Distribution
- Induction Heating and Welding

Absolute Maximum Ratings (At $T_C = 25^\circ C$ Unless Otherwise Stated)

Parameter	Symbol	Conditions	Values	Unit	Note
Drain-Source Voltage	$V_{DS(max)}$	$V_{GS} = 0\text{ V}, I_D = 100\text{ }\mu\text{A}$	1200	V	
Gate-Source Voltage (Dynamic)	$V_{GS(max)}$		-10 / +22	V	
Gate-Source Voltage (Static)	$V_{GS(op)-ON}$	Recommended Operation	18	V	Note 1
	$V_{GS(op)-OFF}$		-5 to -3		
Continuous Drain Current	I_D	$T_C = 25^\circ C, V_{GS} = -5 / +18\text{ V}$	31	A	Fig. 16
		$T_C = 100^\circ C, V_{GS} = -5 / +18\text{ V}$	22		
		$T_C = 135^\circ C, V_{GS} = -5 / +18\text{ V}$	16		
Pulsed Drain Current	$I_{D(pulse)}$	$t_P \leq 3\text{ }\mu\text{s}, D \leq 1\%, V_{GS} = 18\text{ V}$	72	A	Note 2
Power Dissipation	P_D	$T_C = 25^\circ C$	140	W	Fig. 17
Non-Repetitive Avalanche Energy	E_{AS}	$L = 36\text{ mH}, I_{AV} = 3\text{ A}$	162	mJ	
Operating Junction and Storage Temperature	T_J, T_{stg}		-55 to 175	$^\circ C$	

Note 1: This product can support 0V turn-off gate drive voltage with optimized PCB layout and gate drive circuit configuration.

Note 2: Pulse Width t_P Limited by $T_{J(max)}$



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Electrical Characteristics (At $T_C = 25^\circ\text{C}$ Unless Otherwise Stated)

Parameter	Symbol	Conditions	Values			Unit	Note
			Min.	Typ.	Max.		
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 100\text{ }\mu\text{A}$	1200			V	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 1200\text{ V}, V_{GS} = 0\text{ V}$		1	50	μA	
Gate Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = 22\text{ V}$			100	nA	
		$V_{DS} = 0\text{ V}, V_{GS} = -10\text{ V}$			-100		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 9\text{ mA}$	2.2	2.9	4.3	V	Note 3
Transconductance	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 12\text{ A}$		6.7		S	Fig. 5
		$V_{DS} = 10\text{ V}, I_D = 12\text{ A}, T_j = 175^\circ\text{C}$		7.0			
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 18\text{ V}, I_D = 12\text{ A}$		75	100	m Ω	Fig. 6-9
		$V_{GS} = 18\text{ V}, I_D = 12\text{ A}, T_j = 175^\circ\text{C}$		130			
Input Capacitance	C_{iss}			988		pF	Fig. 12
Output Capacitance	C_{oss}			44			
Reverse Transfer Capacitance	C_{rss}			4.6		μJ	Fig. 13
C_{oss} Stored Energy	E_{oss}	$V_{DS} = 800\text{ V}, V_{GS} = 0\text{ V}$ $f = 500\text{ KHz}, V_{AC} = 25\text{ mV}$		17			
C_{oss} Stored Charge	Q_{oss}			62		nC	
Effective Output Capacitance (Energy Related)	$C_{o(er)}$			53		pF	Note 4
Effective Output Capacitance (Time Related)	$C_{o(tr)}$			78			
Gate-Source Charge	Q_{gs}	$V_{DS} = 800\text{ V}, V_{GS} = -5 / +18\text{ V}$		12		nC	Fig. 11
Gate-Drain Charge	Q_{gd}	$I_D = 12\text{ A}$		12			
Total Gate Charge	Q_g	Per JEDEC JEP-192		48			
Internal Gate Resistance	$R_{G(int)}$	$V_{GS} = 18\text{ V}, f = 1\text{ MHz}, V_{AC} = 25\text{ mV}$		1.1		Ω	
Turn-On Switching Energy (Body Diode)	E_{on}	$T_j = 25^\circ\text{C}, V_{GS} = -5/+18\text{ V}, R_{G(ext)} = 8\text{ }\Omega, L = 80.0\text{ }\mu\text{H}, I_D = 12\text{ A}, V_{DD} = 800\text{ V}$		90		μJ	Fig. 24-27
Turn-Off Switching Energy (Body Diode)	E_{off}			23			
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 800\text{ V}, V_{GS} = -5/+18\text{ V}$ $R_{G(ext)} = 8\text{ }\Omega, L = 80.0\text{ }\mu\text{H}, I_D = 12\text{ A}$ Timing relative to V_{DS} , Inductive load		20		ns	Fig. 26
Rise Time	t_r			9			
Turn-Off Delay Time	$t_{d(off)}$			17			
Fall Time	t_f			8			

Note 3: Tested after applying 30ms pulse at $V_{GS} = +25\text{ V}$

Note 4: $C_{o(er)}$, a lumped capacitance that gives same stored energy as C_{oss} while V_{DS} is rising from 0 to 800V.

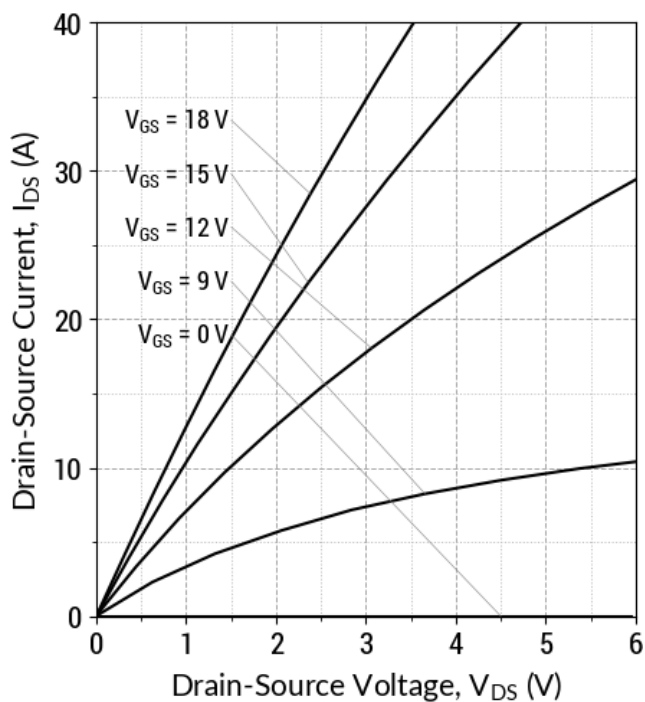
$C_{o(tr)}$, a lumped capacitance that gives same charging times as C_{oss} while V_{DS} is rising from 0 to 800V.

Reverse Diode Characteristics

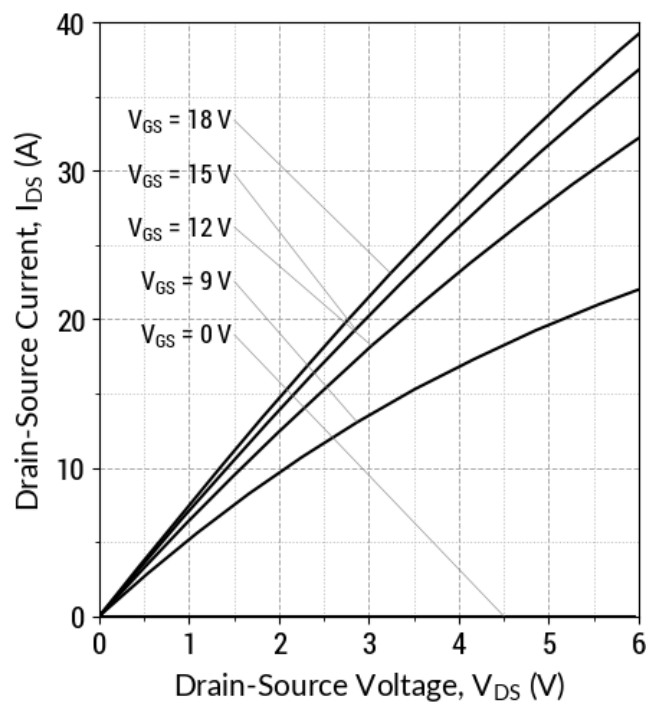
Parameter	Symbol	Conditions	Values			Unit	Note
			Min.	Typ.	Max.		
Diode Forward Voltage	V_{SD}	$V_{GS} = -5\text{ V}, I_{SD} = 6\text{ A}$ $V_{GS} = -5\text{ V}, I_{SD} = 6\text{ A}, T_j = 175^\circ\text{C}$		4.4 4.0		V	Fig. 18-19
Continuous Diode Forward Current	I_S	$V_{GS} = -5\text{ V}, T_c = 25^\circ\text{C}$ $V_{GS} = -5\text{ V}, T_c = 100^\circ\text{C}$			21 13	A	
Diode Pulse Current	$I_{S(pulse)}$	$V_{GS} = -5\text{ V}$		52		A	Note 2
Reverse Recovery Time	t_{rr}	$V_{GS} = -5\text{ V}, I_{SD} = 12\text{ A}, V_R = 800\text{ V}$ $dif/dt = 1200\text{ A}/\mu\text{s}, T_j = 25^\circ\text{C}$		12		ns	
Reverse Recovery Charge	Q_{rr}			51		nC	
Peak Reverse Recovery Current	I_{rrm}			3.5		A	
Reverse Recovery Time	t_{rr}	$V_{GS} = -5\text{ V}, I_{SD} = 12\text{ A}, V_R = 800\text{ V}$ $dif/dt = 1200\text{ A}/\mu\text{s}, T_j = 175^\circ\text{C}$		18		ns	
Reverse Recovery Charge	Q_{rr}			126		nC	
Peak Reverse Recovery Current	I_{rrm}			5.6		A	

Package Characteristics

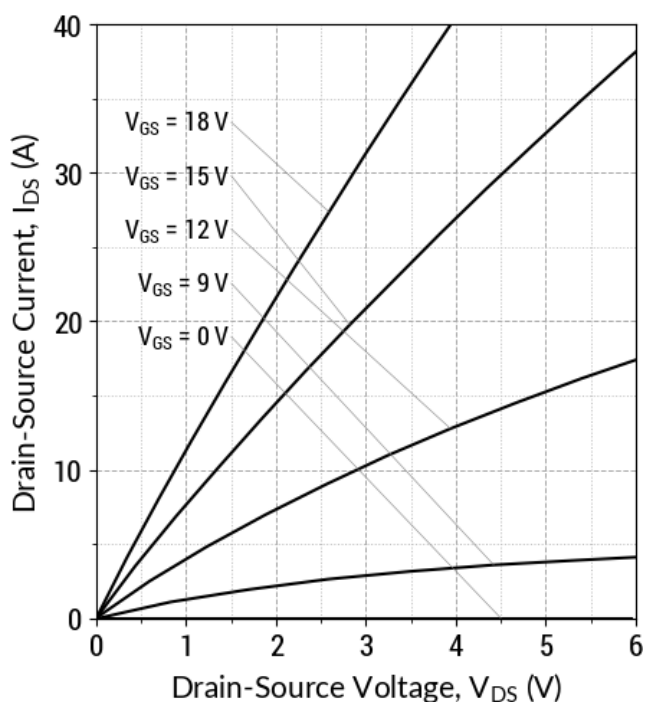
Parameter	Symbol	Conditions	Values	Unit	Note
Max Thermal Resistance, Junction - Case	$R_{thJC-Max}$	Maximum	1.07	$^\circ\text{C}/\text{W}$	Fig. 14
Weight	W_T		1.45	g	
Moisture Sensitivity Level	MSL		1		
EMC Material Group			II		

Fig 1: Typical Output Characteristics ($T_j = 25^\circ\text{C}$)

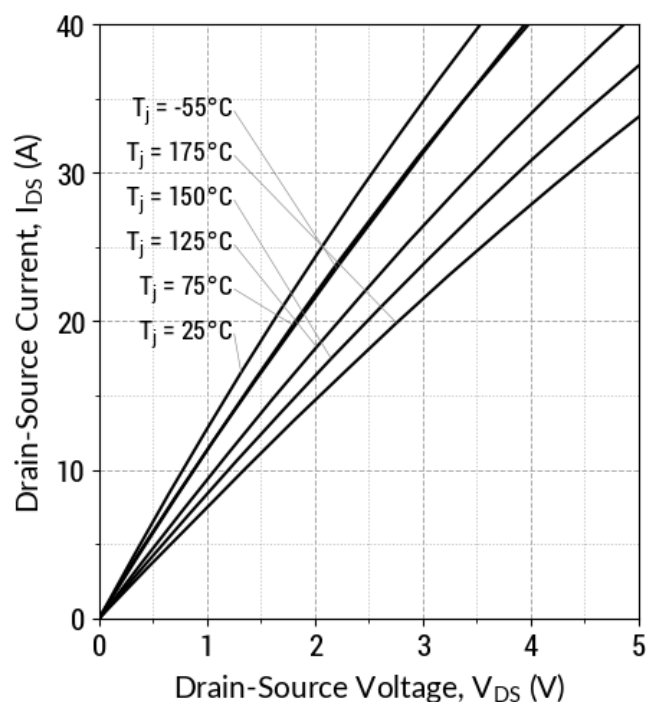
$$I_D = f(V_{DS}, V_{GS}); t_P = 50 \mu\text{s}$$

Fig 2: Typical Output Characteristics ($T_j = 175^\circ\text{C}$)

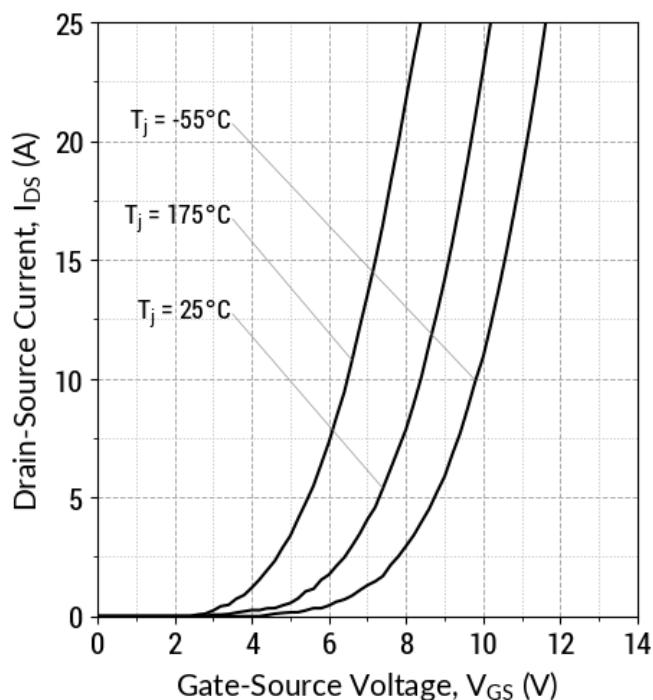
$$I_D = f(V_{DS}, V_{GS}); t_P = 50 \mu\text{s}$$

Fig 3: Typical Output Characteristics ($T_j = -55^\circ\text{C}$)

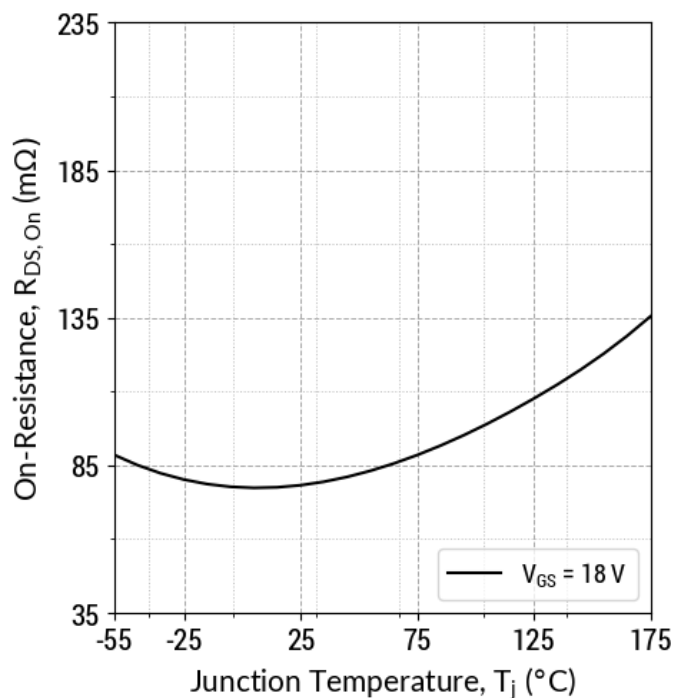
$$I_D = f(V_{DS}, V_{GS}); t_P = 50 \mu\text{s}$$

Fig 4: Typical Output Characteristics ($V_{GS} = 18 \text{ V}$)

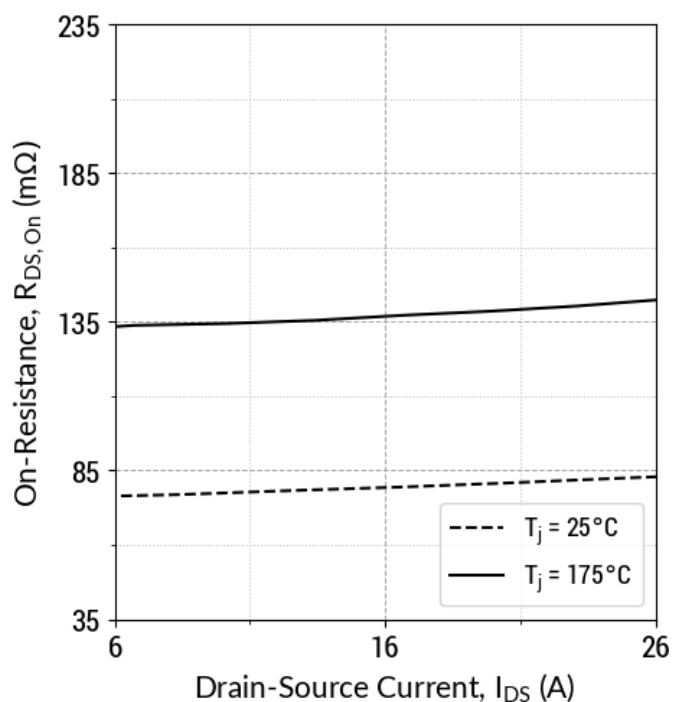
$$I_D = f(V_{DS}, T_j); t_P = 50 \mu\text{s}$$

Fig 5: Typical Transfer Characteristics ($V_{DS} = 10\text{ V}$)

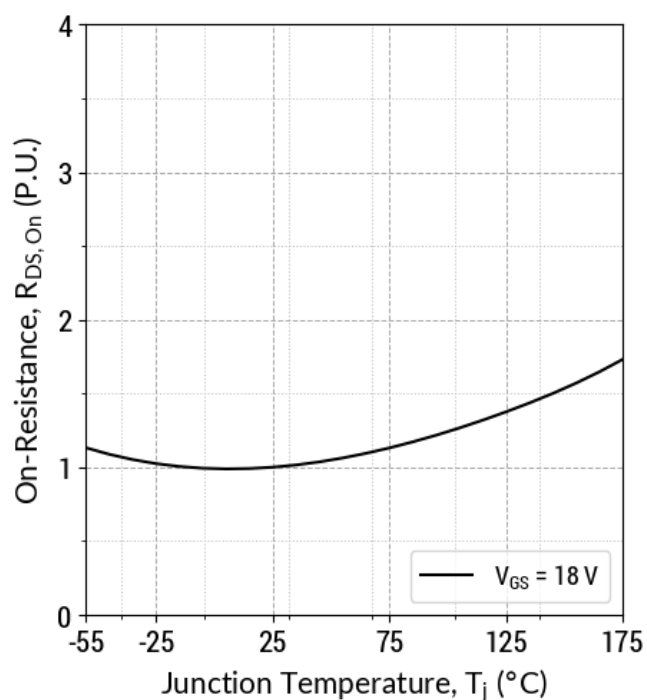
$$I_D = f(V_{GS}, T_j); t_P = 100\ \mu\text{s}$$

Fig 6: Typical $R_{DS(ON)}$ v/s Temperature

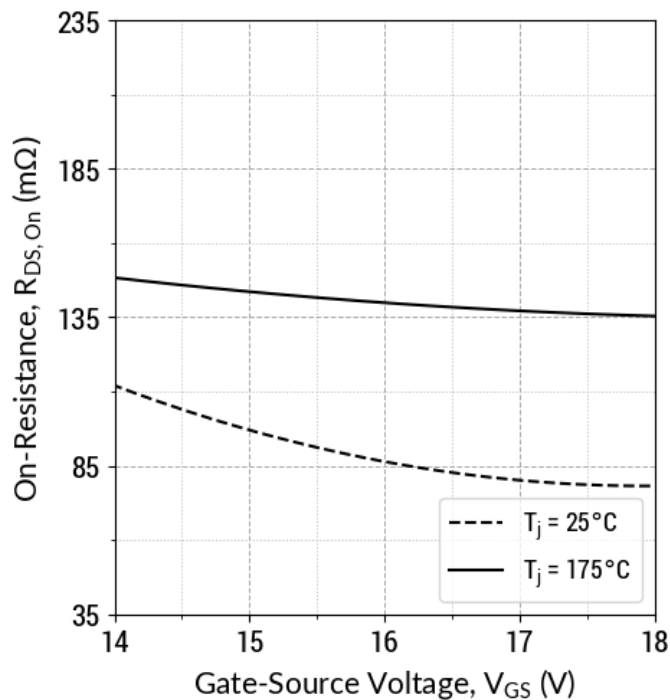
$$R_{DS(ON)} = f(T_j, V_{GS}); t_P = 50\ \mu\text{s}; I_D = 12\text{ A}$$

Fig 7: Typical $R_{DS(ON)}$ v/s Drain Current

$$R_{DS(ON)} = f(T_j, I_D); t_P = 50\ \mu\text{s}; V_{GS} = 18\text{ V}$$

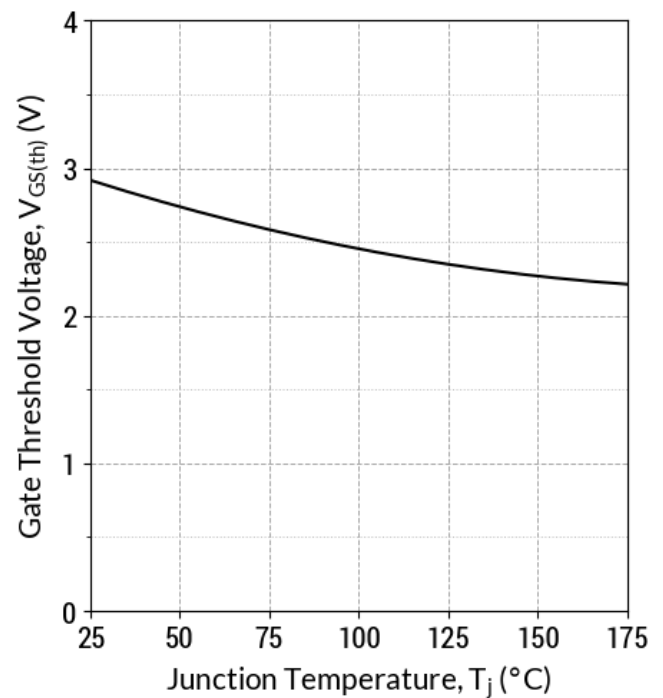
Fig 8: Typical Normalized $R_{DS(ON)}$ v/s Temperature

$$R_{DS(ON)} = f(T_j); t_P = 50\ \mu\text{s}; I_D = 12\text{ A}$$

Fig 9: Typical $R_{DS(ON)}$ v/s Gate Voltage

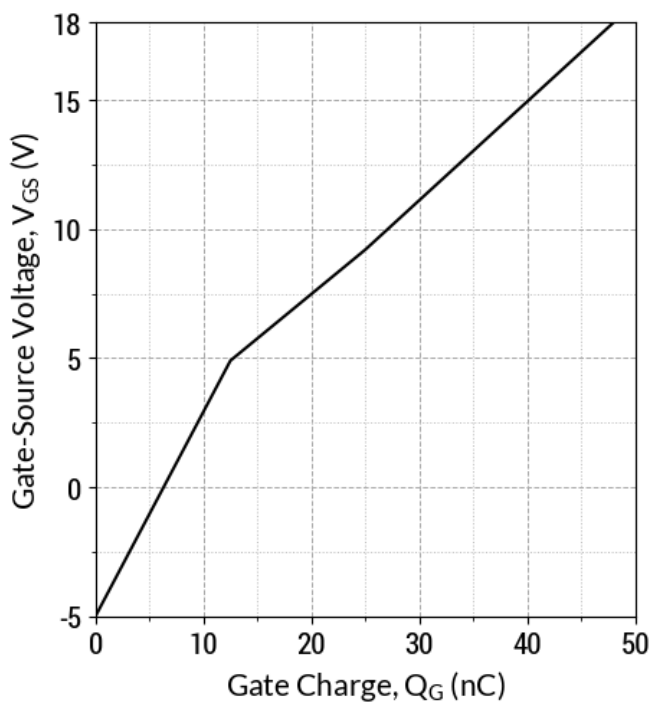
$$R_{DS(ON)} = f(T_j, V_{GS}); t_P = 50 \mu\text{s}; I_D = 12 \text{ A}$$

Fig 10: Typical Threshold Voltage Characteristics



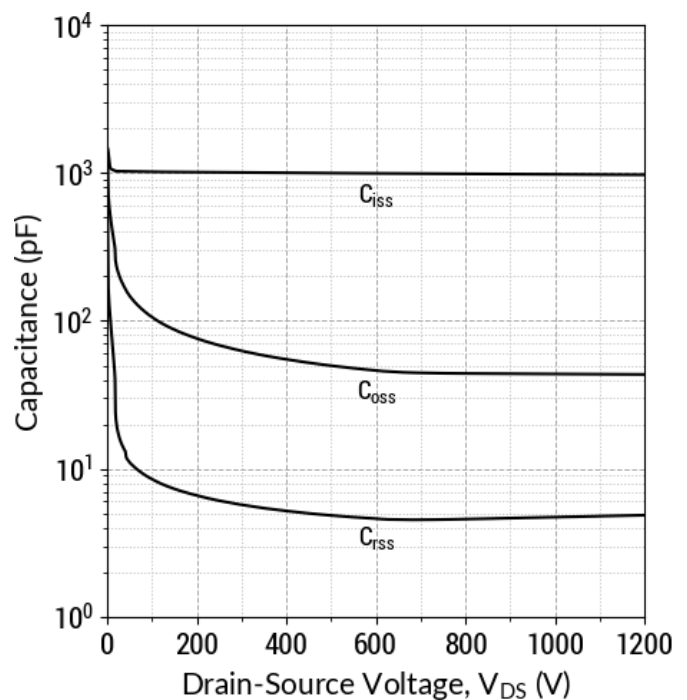
$$V_{GS(th)} = f(T_j); V_{DS} = V_{GS}; I_D = 9 \text{ mA}$$

Fig 11: Typical Gate Charge Characteristics



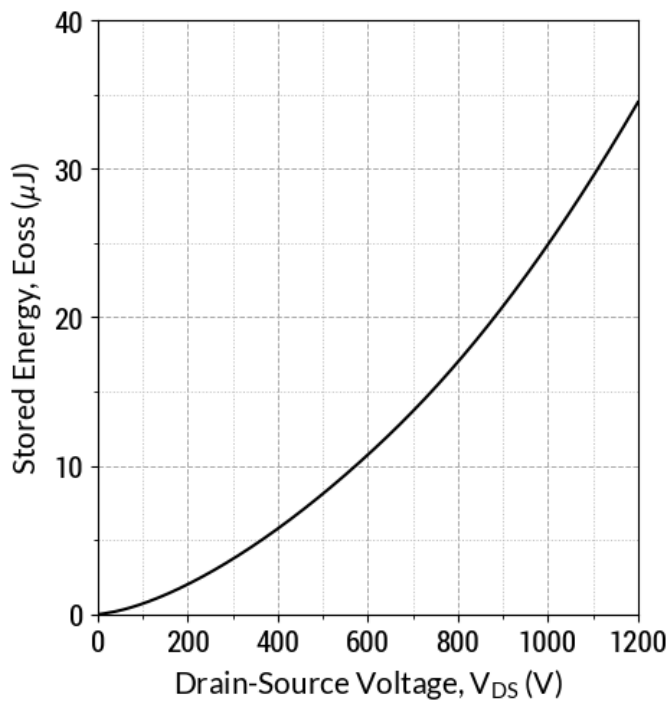
$$I_D = 12 \text{ A}; V_{DS} = 800 \text{ V}; T_c = 25^\circ\text{C}$$

Fig 12: Typical Capacitance v/s Drain-Source Voltage



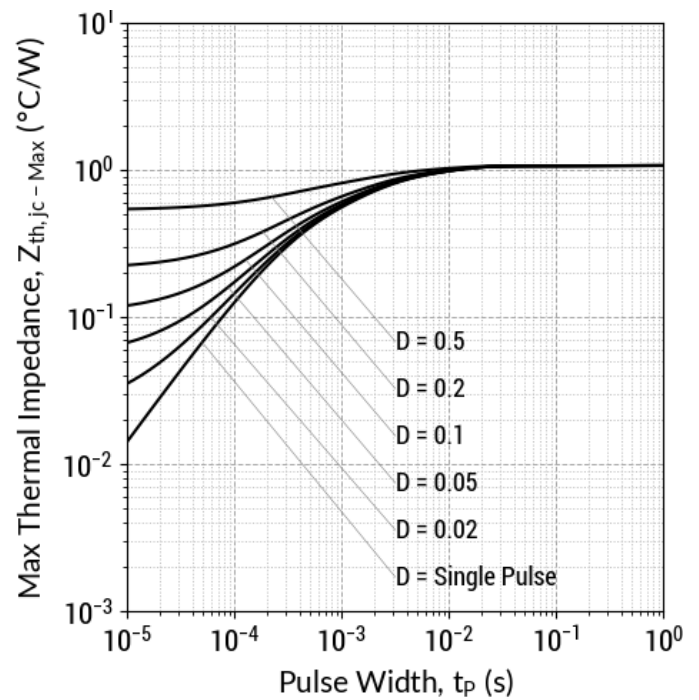
$$f = 500 \text{ KHz}; V_{AC} = 25 \text{ mV}$$

Fig 13: Output Capacitor Stored Energy

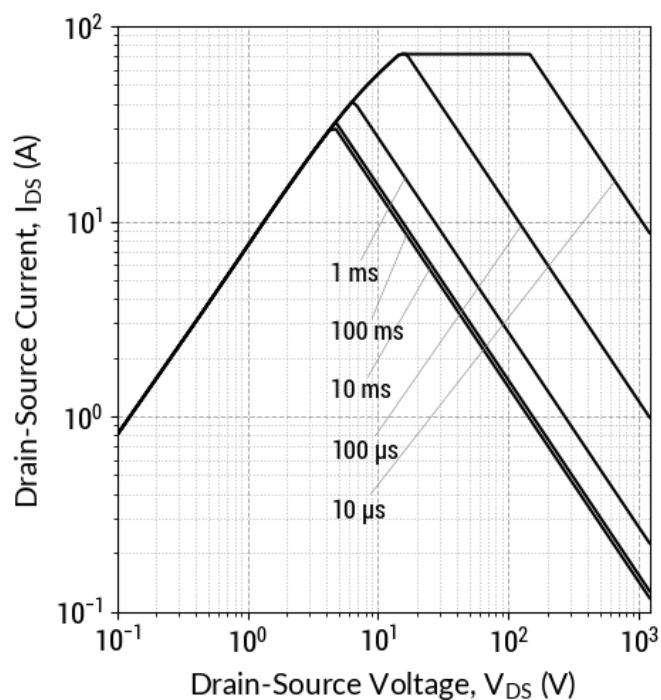


$$E_{oss} = f(V_{DS})$$

Fig 14: Max. Transient Thermal Impedance

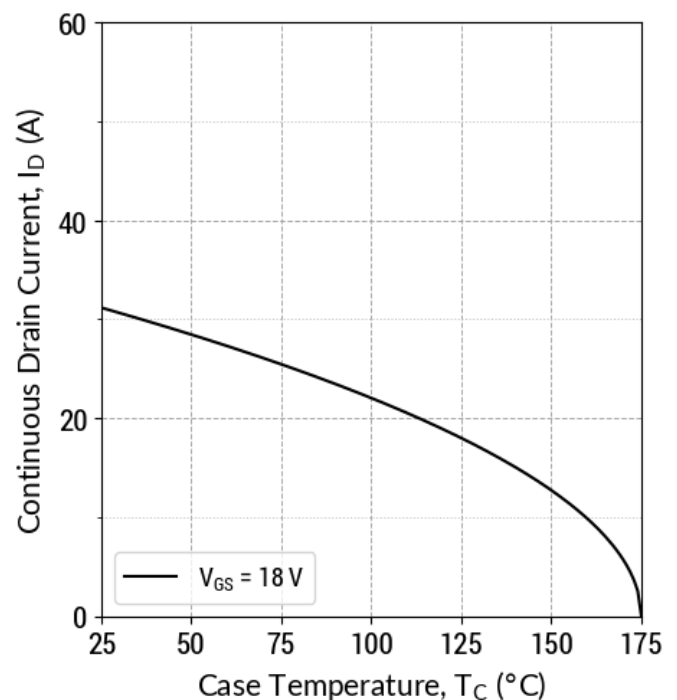


$$Z_{th,jc} = f(t_p, D); D = t_p/T$$

Fig 15: Safe Operating Area ($T_c = 25^{\circ}C$)

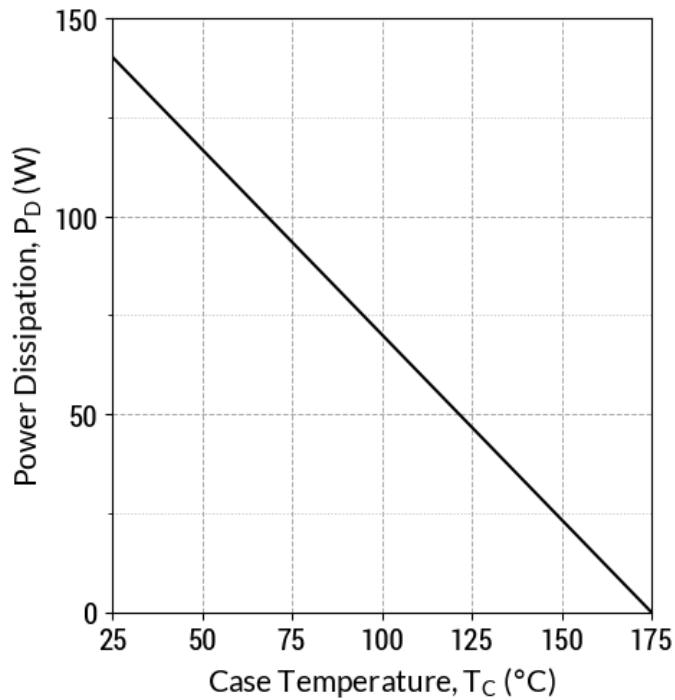
$$I_D = f(V_{DS}, t_p); T_j \leq 175^{\circ}C; D = 0$$

Fig 16: Current De-rating Curve

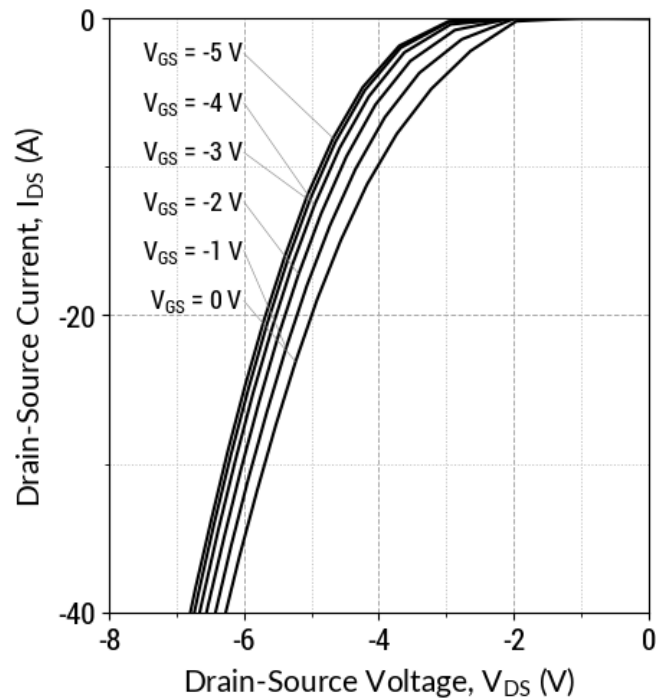


$$I_D = f(T_C); T_j \leq 175^{\circ}C$$

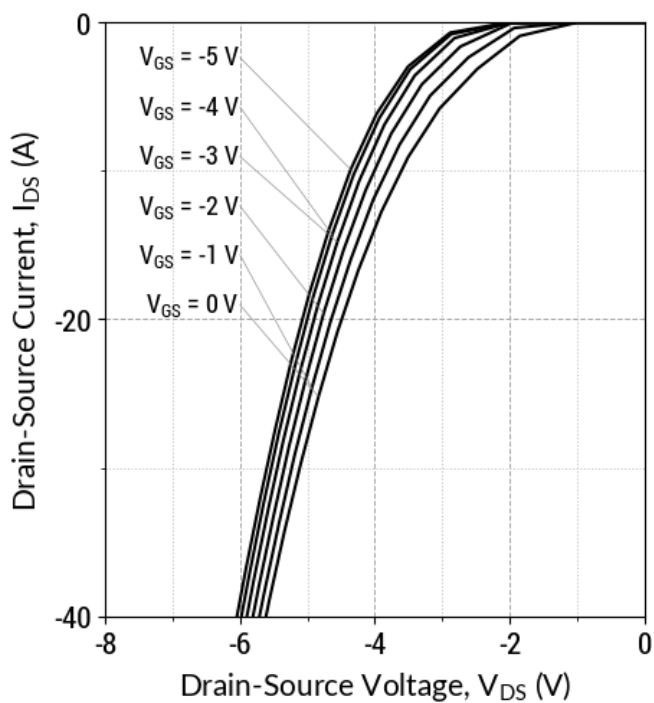
Fig 17: Power De-rating Curve



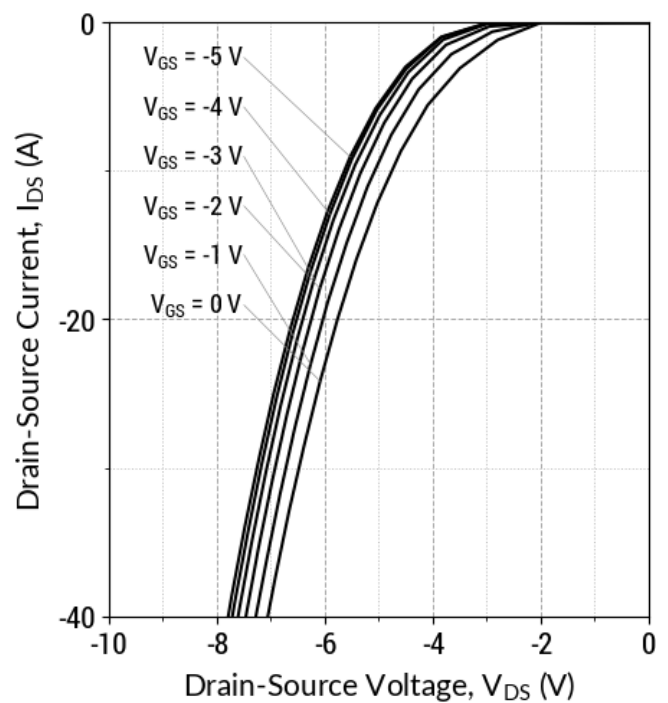
$$P_D = f(T_C); T_j \leq 175^\circ\text{C}$$

Fig 18: Typical Body Diode Characteristics ($T_j = 25^\circ\text{C}$)

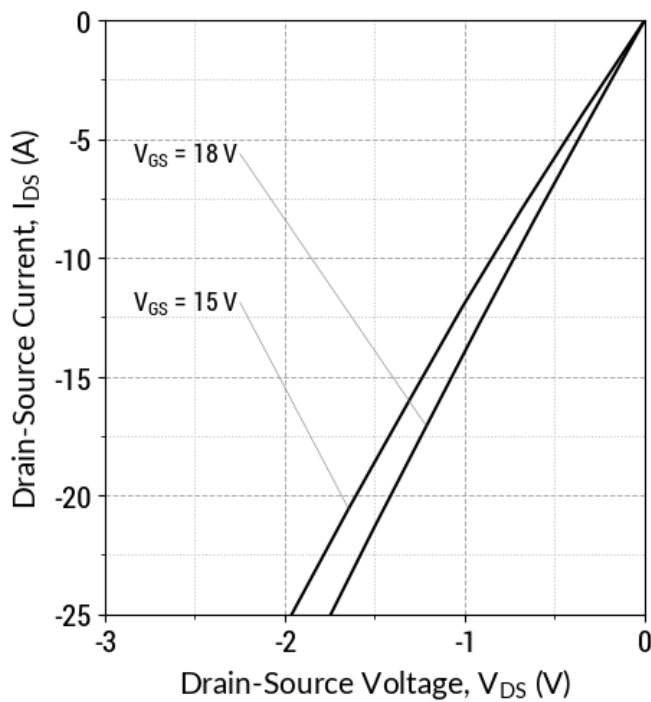
$$I_D = f(V_{DS}, V_{GS}); t_P = 50 \mu\text{s}$$

Fig 19: Typical Body Diode Characteristics ($T_j = 175^\circ\text{C}$)

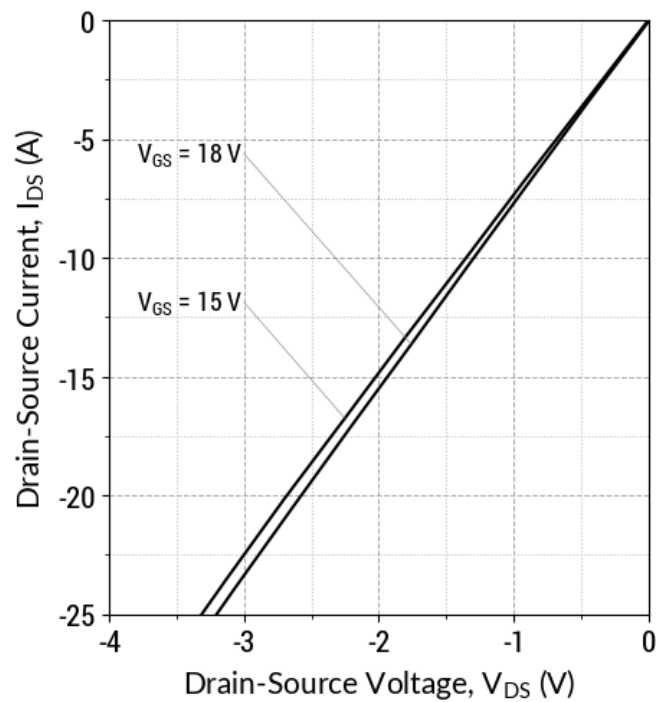
$$I_D = f(V_{DS}, V_{GS}); t_P = 50 \mu\text{s}$$

Fig 20: Typical Body Diode Characteristics ($T_j = -55^\circ\text{C}$)

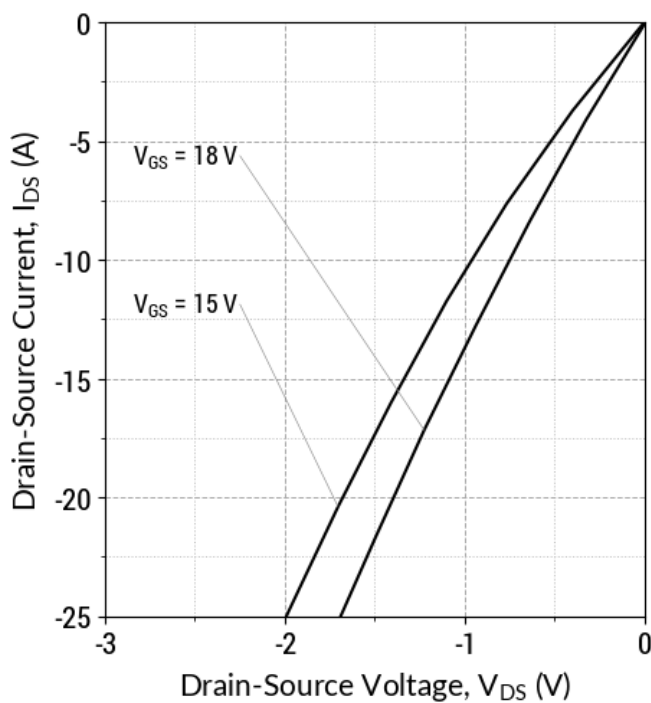
$$I_D = f(V_{DS}, V_{GS}); t_P = 50 \mu\text{s}$$

Fig 21: Typical Third Quadrant Characteristics ($T_j = 25^\circ\text{C}$)

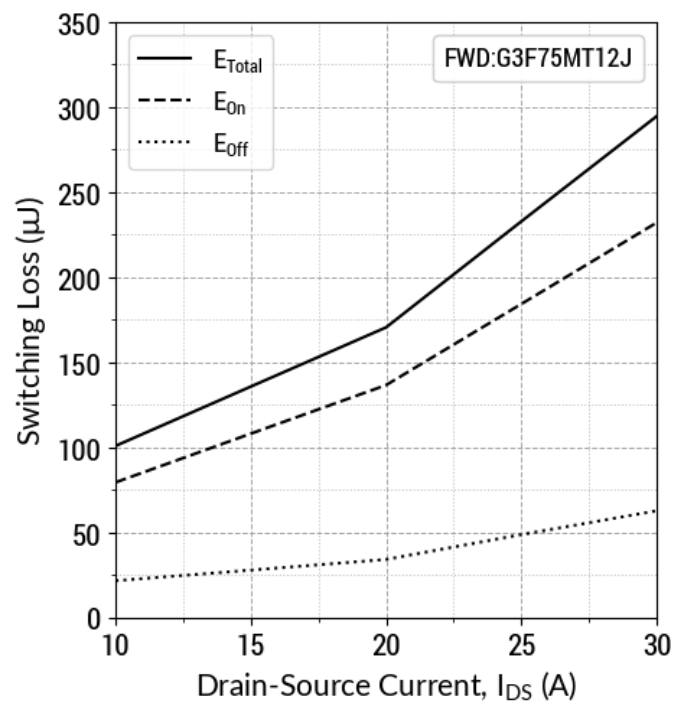
$$I_D = f(V_{DS}, V_{GS}); t_P = 50 \mu\text{s}$$

Fig 22: Typical Third Quadrant Characteristics ($T_j = 175^\circ\text{C}$)

$$I_D = f(V_{DS}, V_{GS}); t_P = 50 \mu\text{s}$$

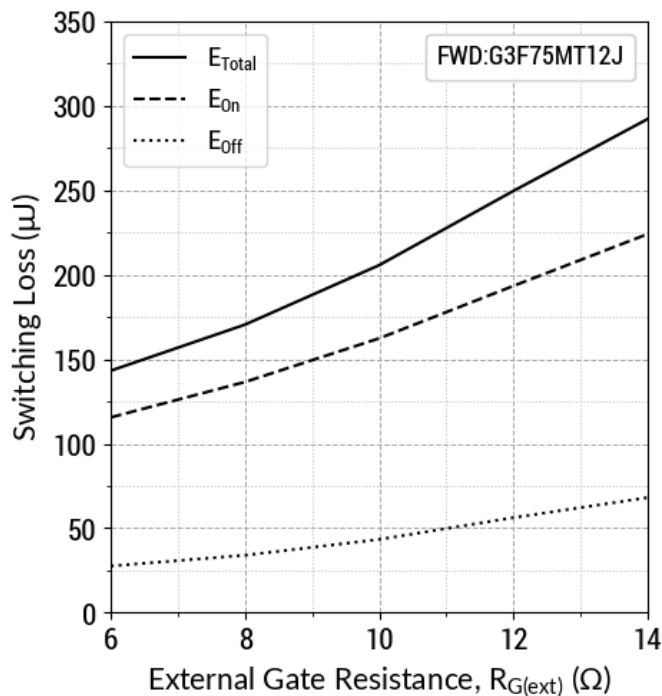
Fig 23: Typical Third Quadrant Characteristics ($T_j = -55^\circ\text{C}$)

$$I_D = f(V_{DS}, V_{GS}); t_P = 50 \mu\text{s}$$

Fig 24: Inductive Switching Energy v/s Drain Current ($V_{DD} = 800\text{V}$)

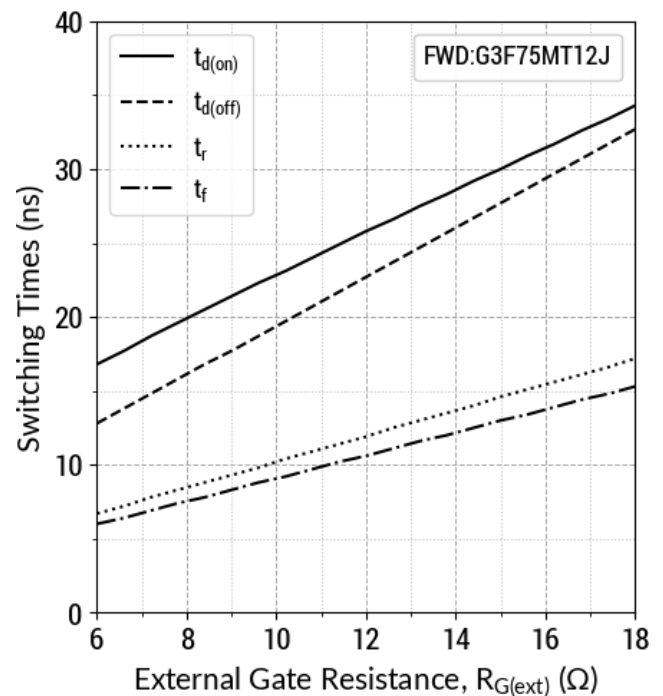
$$T_j = 25^\circ\text{C}; V_{GS} = -5/+18\text{V}; R_{G(\text{ext})} = 8 \Omega; L = 80.0 \mu\text{H}$$

Fig 25: Inductive Switching Energy v/s $R_{G(ext)}$
($V_{DD} = 800V$)



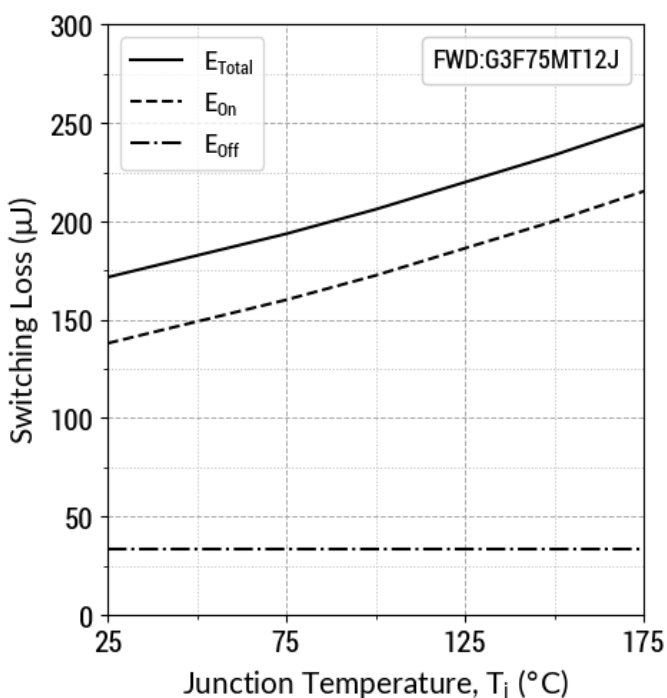
$T_j = 25^\circ C$; $V_{GS} = -5/+18V$; $I_{DS} = 12 A$; $L = 80.0\mu H$

Fig 26: Switching Time v/s $R_{G(ext)}$
($V_{DD} = 800V$)



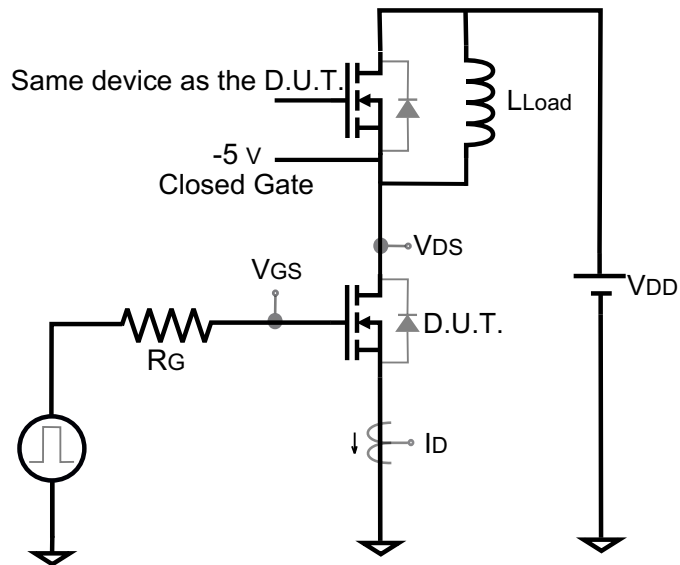
$T_j = 25^\circ C$; $V_{GS} = -5/+18V$; $I_{DS} = 12 A$; $L = 80.0\mu H$

Fig 27: Inductive Switching Energy v/s Temperature
($V_{DD} = 800V$)



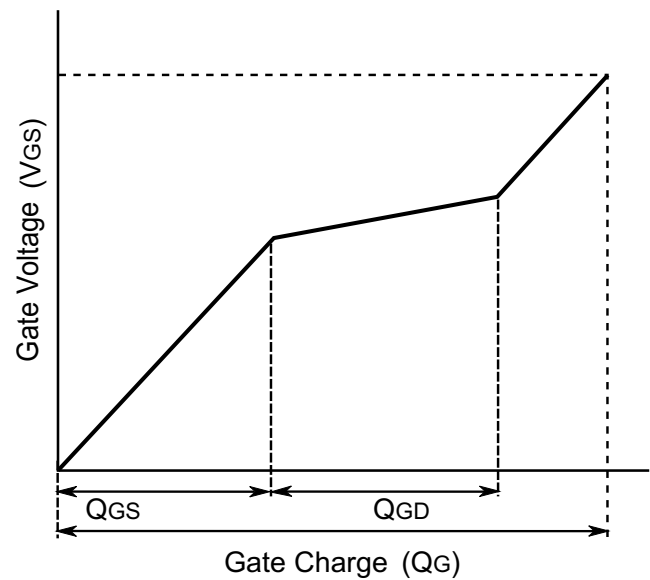
$T_j = 25^\circ C$; $V_{GS} = -5/+18V$; $R_{G(ext)} = 8 \Omega$; $I_{DS} = 12 A$; $L = 80.0\mu H$

Dynamic Test Circuit

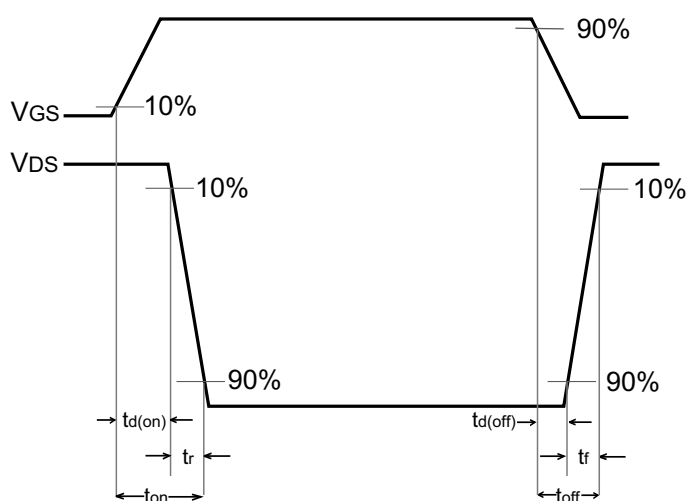


Note: Gate Charge, Switching Time and Energy Circuit

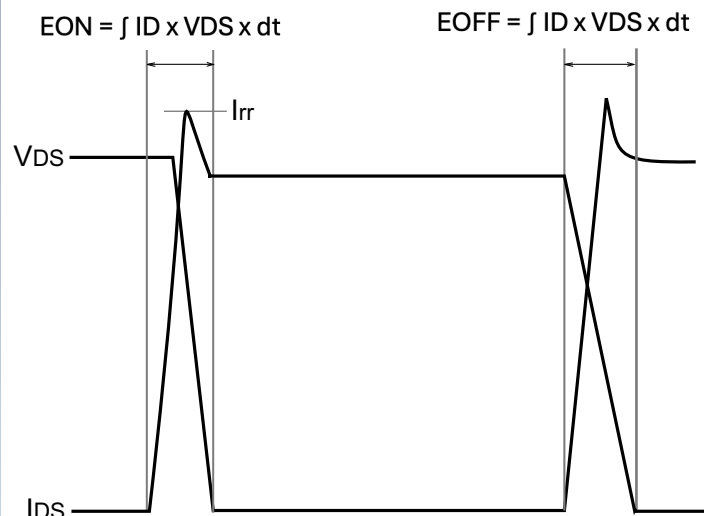
Gate Charge Waveform



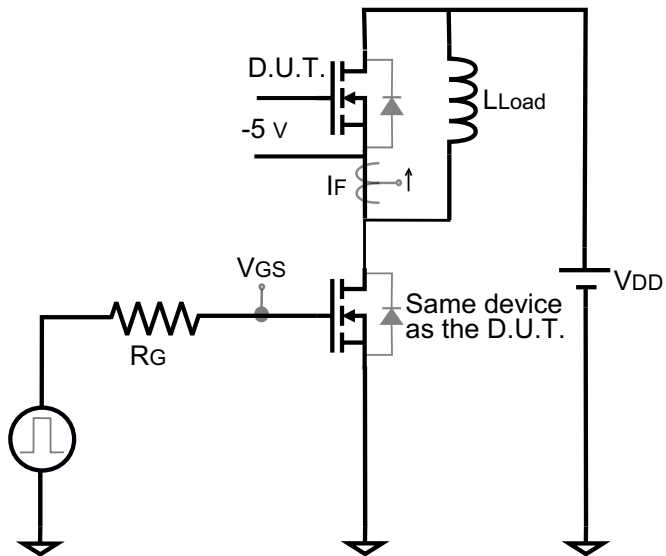
Switching Time Waveform



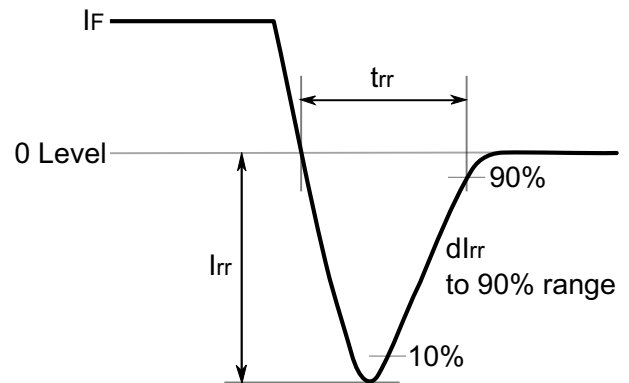
Switching Energy Waveform



Reverse Recovery Circuit

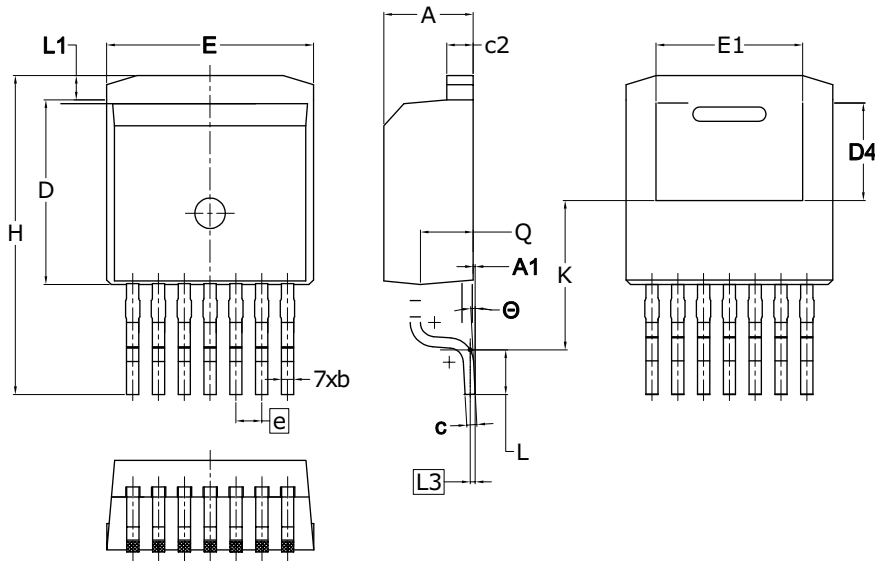


Reverse Recovery Waveform



Package Dimensions

TO-263-7 Package Outline



- Note:
1. All Dimensions Are In mm.
 2. Dimension D & E Do Not Include Mold Flash.
These Dimensions Are Measured At The Outermost Extreme Of The Plastic Body.
 3. Thermal Pad Contour Optional Within Dimensions E, L1, D4 & E1.
 4. Dimension D4 & E1 Establish A Minimum Mounting Surface for The Thermal Pad.
 5. ■ is Exposed Cu.
 6. There Is Exposed Cu and Molding Flash Bleeding At The Pin Which Is Close To Package.

SYMBOL	DIMENSIONS	
	MIN.	MAX.
A	4.30	4.50
A1	0.00	0.25
b	0.50	0.70
c	0.45	0.60
c2	1.20	1.40
D	8.93	9.23
D4	4.65	4.95
E	10.08	10.28
E1	6.82	7.62
e	1.27 BSC	
H	15.00	16.00
K	7.30	
L	1.90	2.50
L1	1.00	1.40
L3	0.25 BSC	
Q	2.45	2.75
Θ	0°	7°

NOTE

1. CONTROLLED DIMENSION IS MILLIMETER.
2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS.
3. THE SOURCE AND KELVIN-SOURCE PINS ARE NOT INTERCHANGABLE. THEIR EXCHANGE MIGHT LEAD TO MALFUNCTION.

Revision History

• Rev 24/Aug: Initial Release (Rev 1.0)

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