TPS768xx-Q1 Fast-Transient-Response 1-A Low-Dropout Voltage Regulators

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C4B
- 1-A Low-Dropout (LDO) Voltage Regulator
- Available in 1.8-V, 2.5-V, 3.3-V, and 5-V Fixed-Output and an Adjustable Version
- Dropout Voltage Down to 230 mV at 1 A (TPS76850-Q1)
- Ultralow 85-μA Typical Quiescent Current
- Fast Transient Response
- 2% Tolerance Over Specified Conditions for Fixed-Output Versions
- Open-Drain Power Good (See TPS767xx-Q1 for Power-On Reset With 200-ms Delay Option)
- 20-Pin TSSOP (PWP) Package
- Thermal Shutdown Protection

2 Applications

- Automotive
- Power Train
- Cluster
- ADAS

3 Description

This device is designed to have a fast transient response and be stable with 10 μF capacitors. This combination provides high performance at a reasonable cost.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 230 mV at an output current of 1 A for the TPS76850-Q1) and is directly proportional to the output current. Additionally, because the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 85 μA over the full range of output current, 0 mA to 1 A). These two key specifications yield a significant improvement in operating life for battery-powered systems. This LDO family also features a shutdown mode; applying a TTL high signal to the enable ($\overline{EN}$) input shuts down the regulator, reducing the quiescent current to less than 1 μA at T_J = 25°C.

Power good (PG) is an active-high output, which can be used to implement a power-on reset or a low-battery indicator.

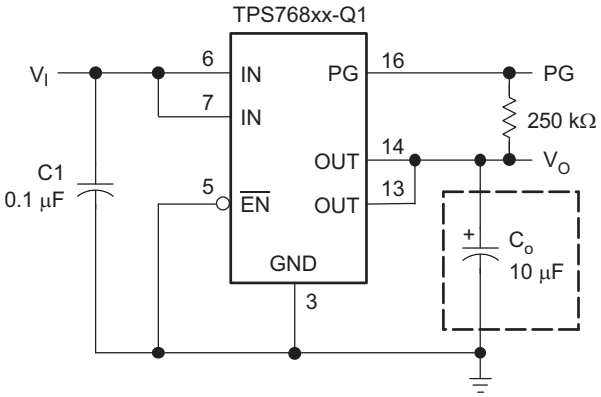
The TPS768xx-Q1 is offered in 1.8-V, 2.5-V, 3.3-V, and 5-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.2 V to 5.5 V). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges. The TPS768xx-Q1 family is available in a 20-pin PWP package.

Device Information[1]

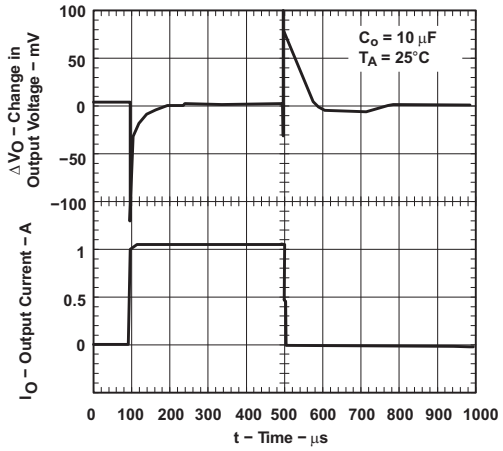
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS768xx-Q1	HTSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



Load Transient Response



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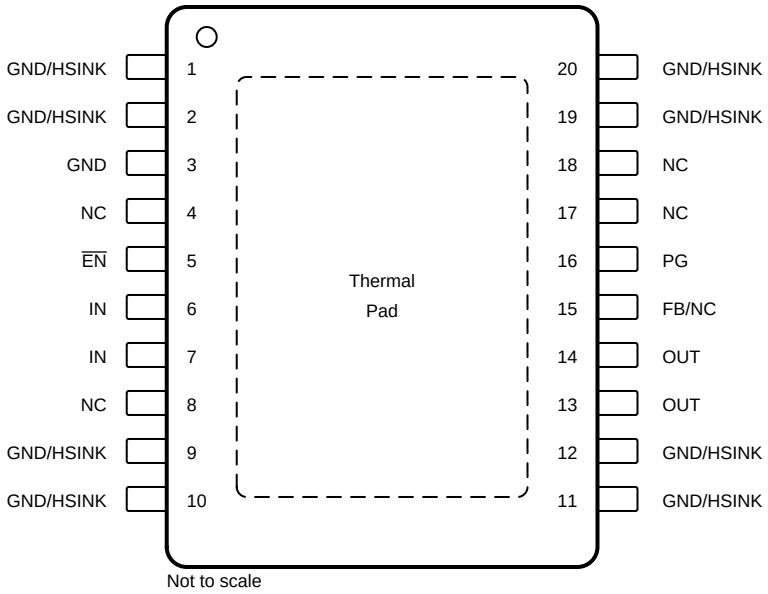
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2008) to Revision B	Page
• Added AEC-Q100 qualifications	1
• Deleted *Ordering Information* table	1
• Added Applications section, *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1
• Deleted 1.5-V, 2.7-V, and 3-V versions throughout the data sheet	1
• Changed *Pin Configuration and Functions* section	3
• Deleted the "Continuous total power dissipation" row from the *Absolute Maximum Ratings* table	4
• Changed T_J to T_A in the *Recommended Operating Conditions* table	4
• Deleted *Dissipation Ratings* table	4

5 Pin Configuration and Functions

PWP PowerPAD™ Package
20-Pin HTSSOP With Exposed Thermal Pad
Top View



Not to scale

NC – No internal connection

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{EN}$	5	I	Enable input
FB/NC	15	I	Feedback input voltage for adjustable device (no connect for fixed options)
GND	3	—	LDO ground
GND/HSINK	1, 2, 9, 10, 11, 12, 19, 20	—	Ground and heatsink
IN	6, 7	I	Input
NC	4, 8, 17, 18	—	No connect
OUT	13, 14	O	Regulated output voltage
PG	16	O	Power-good output
NC	17	—	No connect
Thermal pad	—	—	Solder the thermal pad to the board.

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating ambient temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Input voltage, V_I (2)	–0.3	13.5	V
Voltage at $\overline{EN}$	–0.3	V_I + 0.3	V
Maximum PG voltage		16.5	V
Peak output current	Internally limited		
Output voltage, V_O (OUT, FB)		7	V
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network terminal ground.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 4, 5, and 8)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_I	Input voltage(1)	2.7	10	V
V_O	Voltage at OUT	1.2	5.5	V
I_O	Output current(2)	0	1	A
T_A	Operating ambient temperature(2)	–40	125	°C

(1) To calculate the minimum input voltage for the maximum output current, use the following equation: $V_{I(min)} = V_{O(max)} + V_{(DO,max\_load)}$, where $V_{(DO,max\_load)}$ is the dropout voltage at maximum load.
(2) Continuous current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

6.4 Thermal Information

THERMAL METRIC(1)		TPS768xx-Q1 PWP (HTSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	39.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	21.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating ambient temperature range, $V_I = V_{O(typ)} + 1$ V, $I_O = 1$ mA, $\overline{EN} = 0$ V, $C_O = 10$ µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output voltage (10-µA to 1-A load)(1)	TPS76801-Q1	5.5 V ≥ V_O ≥ 1.5 V	T_J = 25°C		V_O		V
			T_J = –40°C to 125°C	0.98 × V_O		1.02 × V_O	
	TPS76818-Q1	2.8 V < V_{IN} < 10 V	T_J = 25°C		1.8		
			T_J = –40°C to 125°C	1.764		1.836	
	TPS76825-Q1	3.5 V < V_{IN} < 10 V	T_J = 25°C		2.5		
			T_J = –40°C to 125°C	2.45		2.55	
	TPS76833-Q1	4.3 V < V_{IN} < 10 V	T_J = 25°C		3.3		
			T_J = –40°C to 125°C	3.234		3.366	
	TPS76850-Q1	6 V < V_{IN} < 10 V	T_J = 25°C		5		
			T_J = –40°C to 125°C	4.9		5.1	
Quiescent current (GND current), $\overline{EN}$ = 0 V(1)		T_J = 25°C 10 µA < I_O < 1 A, T_J = 25°C			85		µA
		T_J = –40°C to 125°C I_O = 1 A, T_J = –40°C to 125°C				125	
Output voltage line regulation (ΔV_O / V_O) (1) (2)		T_J = 25°C V_O + 1 V < V_I ≤ 10 V, T_J = 25°C			0.01		%/V
Load regulation					3		mV
Output noise voltage	TPS76818-Q1	T_J = 25°C BW = 200 Hz to 100 kHz, C_O = 10 µF, I_C = 1 A, T_J = 25°C			55		µVrms
Output current limit		V_O = 0 V			1.7	2	A
Thermal shutdown junction temperature					150		°C
Standby current		$\overline{EN}$ = V_I, 2.7 V < V_I < 10 V	T_J = 25°C		1		µA
			T_J = –40°C to 125°C			10	
FB input current	TPS76801-Q1	V_{FB} = 1.5 V			2		nA
High-level enable input voltage				1.7			V
Low-level enable input voltage						0.9	V
Power-supply ripple rejection (1)		T_J = 25°C f = 1 kHz, C_O = 10 µF, T_J = 25°C			60		dB
PG	Minimum input voltage for valid PG	$I_{O(PG)}$ = 300 µA			1.1		V
	Trip threshold voltage	V_O decreasing		92		98	%V_O
	Hysteresis voltage	Measured at V_O			0.5		%V_O
	Output low voltage	V_I = 2.7 V, $I_{O(PG)}$ = 1 mA			0.15	0.4	V
	Leakage current	$V_{(PG)}$ = 5 V				1	µA
$\overline{EN}$ input current		$\overline{EN}$ = 0 V		–1	0	1	µA
		$\overline{EN}$ = V_I		–1		1	
Dropout voltage (3)	TPS76833-Q1	I_O = 1 A	T_J = 25°C		350		mV
			T_J = –40°C to 125°C			575	
	TPS76850-Q1		T_J = 25°C		230		
			T_J = –40°C to 125°C			380	

(1) Minimum IN operating voltage is 2.7 V or $V_{O(typ)}$ + 1 V, whichever is greater. Maximum IN voltage 10 V.

(2) If V_O ≤ 1.8 V then $V_{I(max)}$ = 10 V, $V_{I(min)}$ = 2.7 V: $\text{Line Reg. (mV)} = (\%/V) \times V_O \frac{(V_{Imax} - 2.7V)}{100} \times 1000$

If V_O ≥ 2.5 V then $V_{I(max)}$ = 10 V, $V_{I(min)} = V_O + 1$ V: $\text{Line Reg. (mV)} = (\%/V) \times V_O \frac{(V_{Imax} - (V_O + 1V))}{100} \times 1000$

(3) IN voltage equals V_O(typ) – 100 mV.

6.6 Typical Characteristics

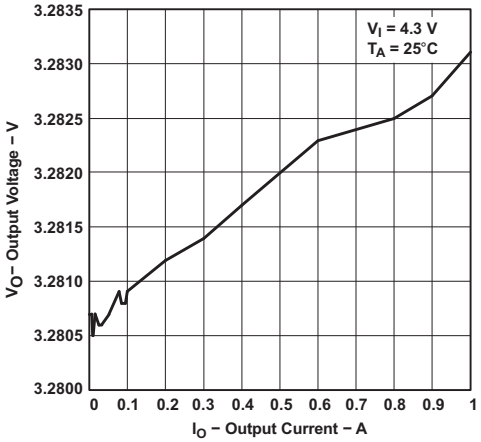


Figure 1. TPS76833-Q1 Output Voltage vs Output Current

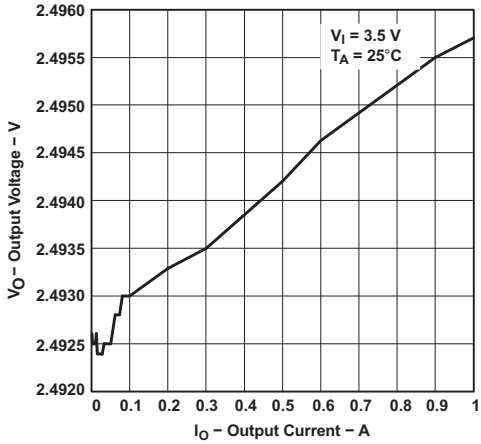


Figure 2. TPS76825-Q1 Output Voltage vs Output Current

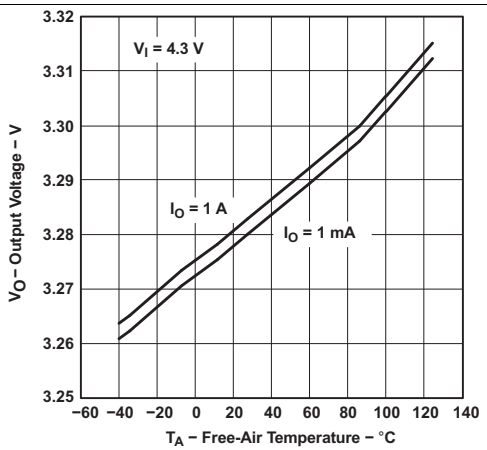


Figure 3. TPS76833-Q1 Output Voltage vs Ambient Temperature

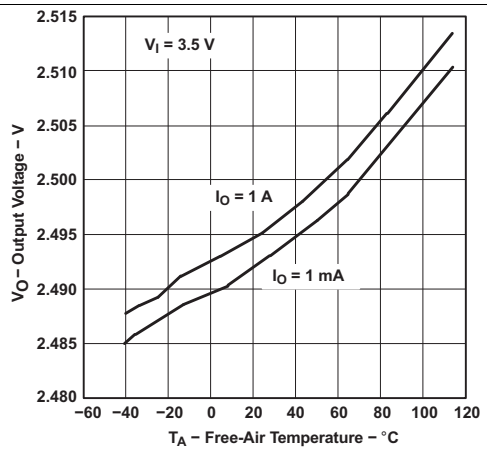


Figure 4. TPS76825-Q1 Output Voltage vs Ambient Temperature

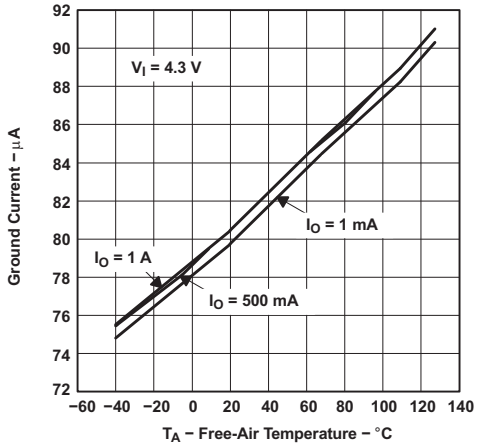


Figure 5. TPS76833-Q1 Ground Current vs Ambient Temperature

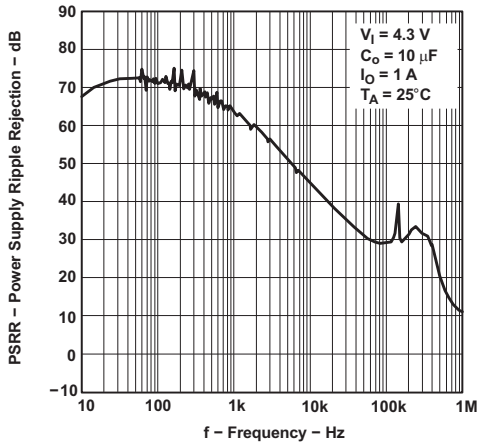


Figure 6. TPS76833-Q1 Power-Supply Ripple Rejection vs Frequency

Typical Characteristics (continued)

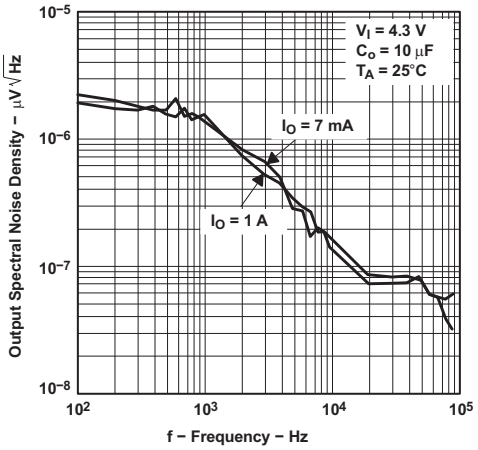


Figure 7. TPS76833-Q1 Output Spectral Noise Density vs Frequency

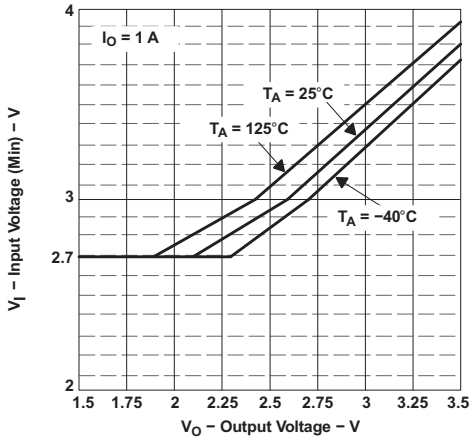


Figure 8. Input Voltage (Min.) vs Output Voltage

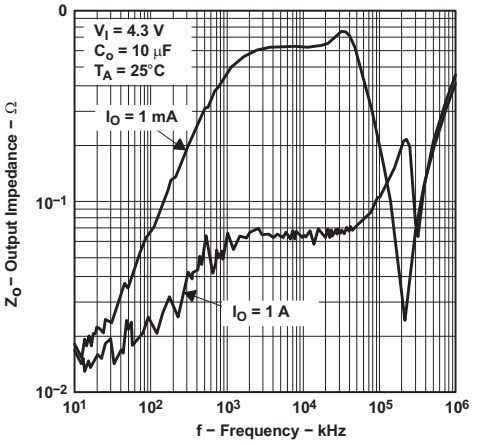


Figure 9. TPS76833-Q1 Output Impedance vs Frequency

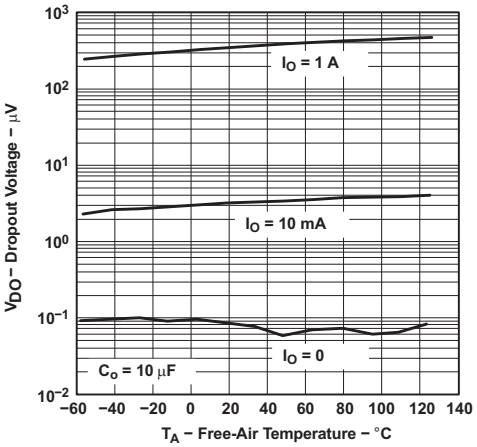


Figure 10. TPS76833-Q1 Dropout Voltage vs Ambient Temperature

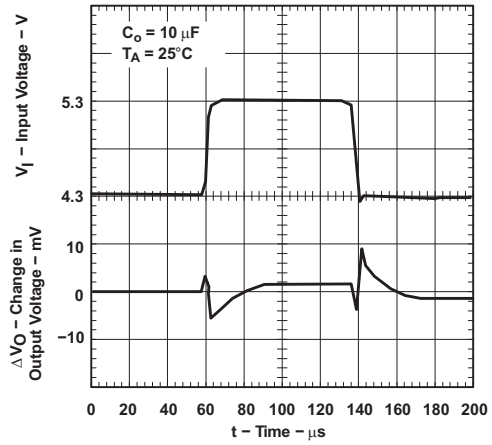


Figure 11. TPS76833-Q1 Line Transient Response

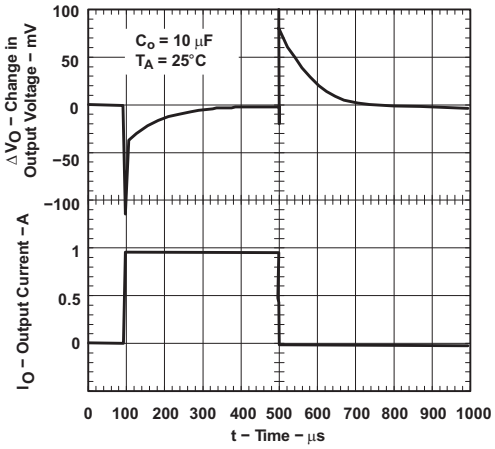


Figure 12. TPS76833-Q1 Load Transient Response

Typical Characteristics (continued)

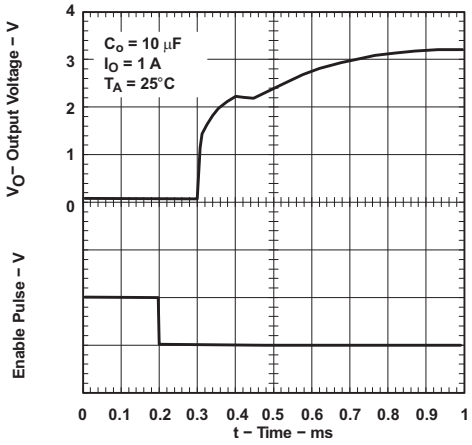


Figure 13. TPS76833-Q1 Output Voltage vs Time (at Start-Up)

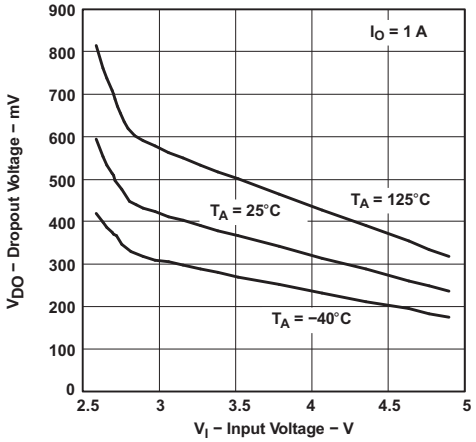


Figure 14. TPS76801-Q1 Dropout Voltage vs Input Voltage

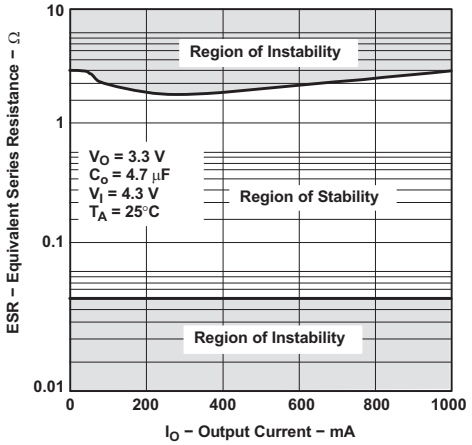


Figure 15. Typical Region of Stability Equivalent Series Resistance (4) vs Output Current

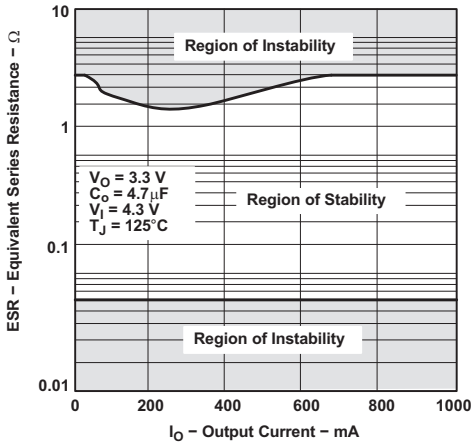


Figure 16. Typical Region of Stability Equivalent Series Resistance(4) vs Output Current

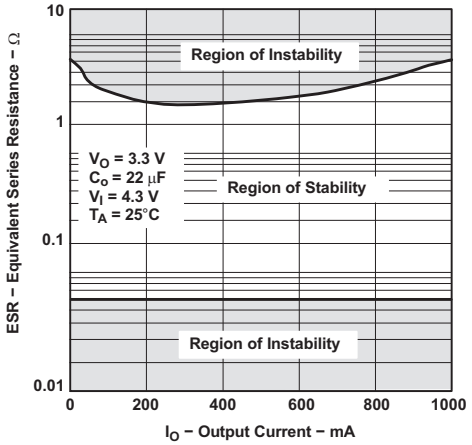


Figure 17. Typical Region of Stability Equivalent Series Resistance(4) vs Output Current

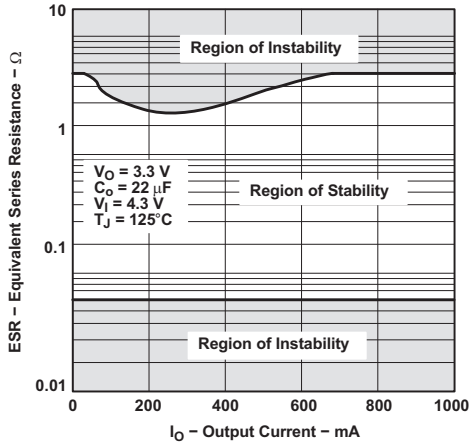


Figure 18. Typical Region of Stability Equivalent Series Resistance(4) vs Output Current

(4) Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

7 Parameter Measurement Information

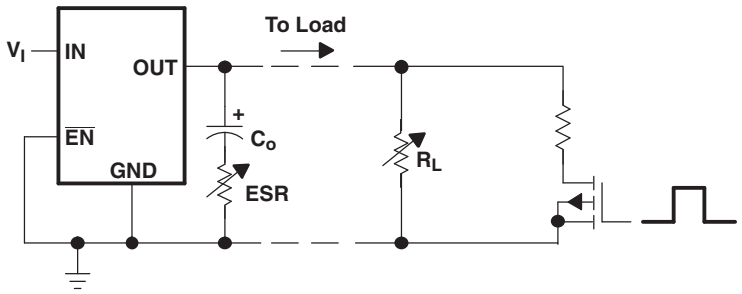


Figure 19. Test Circuit for Typical Regions of Stability (Figure 15 to Figure 18) (Fixed-Output Options)

8 Detailed Description

8.1 Overview

The TPS768xx-Q1 family includes four fixed-output voltage regulators (1.8 V, 2.5 V, 3.3 V, and 5 V), and offers an adjustable version, the TPS76801-Q1 (adjustable from 1.2 V to 5.5 V).

8.1.1 Device Operation

The TPS768xx-Q1 device features very low quiescent current, which remains virtually constant even with varying loads. Conventional LDO regulators use a PNP pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C / \beta$). The TPS768xx-Q1 device uses a PMOS transistor to pass current. Because the gate of the PMOS is voltage-driven, operating current is low and invariable over the full load range.

Another pitfall associated with the PNP pass element is its tendency to saturate when the device goes into dropout. The resulting drop in β forces an increase in I_B to maintain the load. During power up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS768xx-Q1 quiescent current remains low even when the regulator drops out, eliminating both problems.

The TPS768xx-Q1 family also features a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to 2 μA. If the shutdown feature is not used, $\overline{EN}$ should be tied to ground.

8.2 Functional Block Diagrams

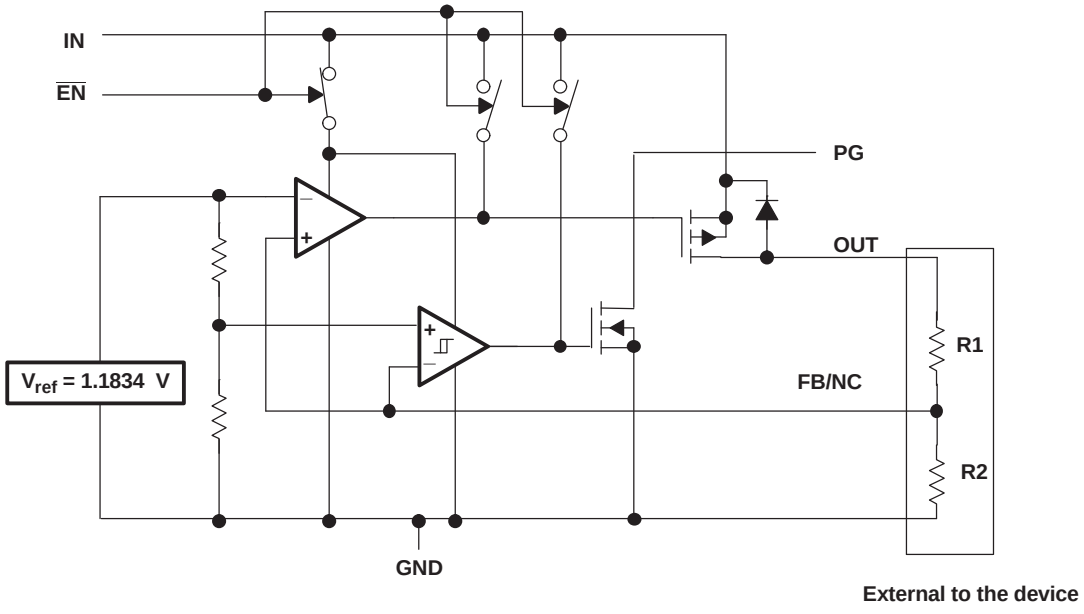


Figure 20. Functional Block Diagram—Adjustable Version

Functional Block Diagrams (continued)

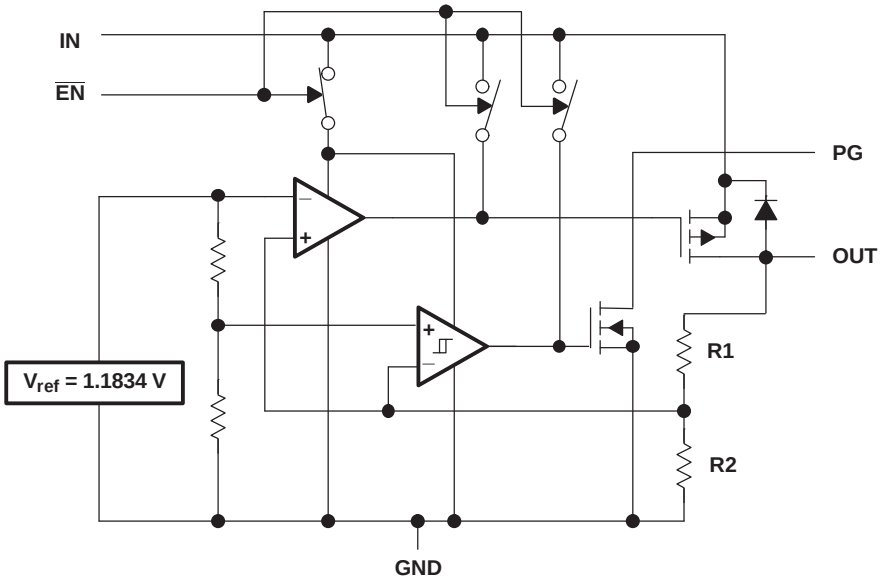


Figure 21. Functional Block Diagram—Fixed-Voltage Versions

8.3 Feature Description

8.3.1 Power-Good Indicator

The TPS768xx-Q1 device features a power-good (PG) output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the PG output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, the PG pin can be left floating. PG can be used to drive power-on reset circuitry or used as a low-battery indicator. PG does not assert itself when the regulated output voltage falls out of the specified 2% tolerance, but instead reports an output voltage low, relative to its nominal regulated value.

8.3.2 Regulator Protection

The TPS768xx-Q1 PMOS-pass transistor has a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (for example, during power-down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS768xx-Q1 device also features internal current limiting and thermal protection. During normal operation, the TPS768xx-Q1 device limits output current to approximately 1.7 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C (typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C (typ), regulator operation resumes.

8.4 Device Functional Modes

8.4.1 Shutdown

The enable pin ($\overline{EN}$) is active-low. The device is enabled when the voltage at the $\overline{EN}$ pin goes below 0.9 V. The device is turned off when the $\overline{EN}$ pin is held above 1.7 V. When shutdown capability is not required, $\overline{EN}$ can be connected directly to GND.

Device Functional Modes (continued)

8.4.2 Operation With V_{IN} Less Than 2.7 V

The TPS768xx-Q1 family of devices operates with input voltages above 2.7 V. When input voltage falls below 2.7 V, the device shuts down.

8.4.3 Operation With V_{IN} Greater Than 2.7 V

When V_{IN} is greater than 2.7 V, if the input voltage is higher than the desired output voltage plus dropout voltage, the output voltage is equal to the desired value. Otherwise, output voltage will be V_{IN} minus the dropout voltage.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS768xx-Q1 device is offered in 1.8-V, 2.5-V, 3.3-V, and 5-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.2 V to 5.5 V). Output voltage tolerance is specified as a maximum of ±2% over line, load, and temperature ranges.

9.2 Typical Application

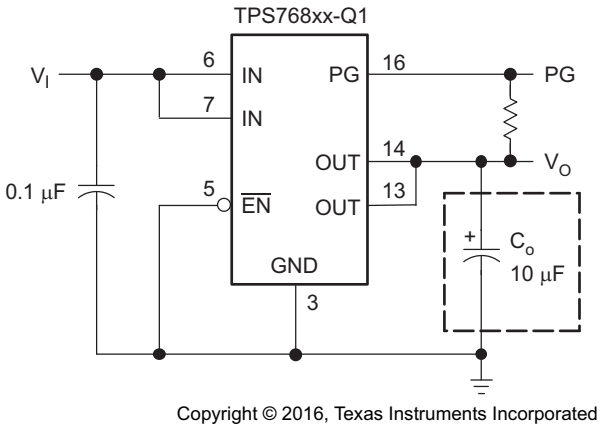


Figure 22. Typical Application Configuration (for Fixed-Output Options)

9.2.1 Design Requirements

For this design example use, the parameters listed in the following table as the input parameters.

PARAMETER	EXAMPLE VALUE
Input voltage range	2.7 V to 10 V
Output voltage	Fixed: 1.8 V, 2.5 V, 3. 3 V, and 5 V Adjustable: 1.2 V to 5.5 V
Output current rating	1 A
Output capacitor range	>10 µF
Output capacitor ESR range	50 mΩ to 1.5 Ω

9.2.2 Detailed Design Procedure

9.2.2.1 Minimum Load Requirements

The TPS768xx-Q1 family is stable even at zero load; no minimum load is required for operation.

9.2.2.2 FB Pin Connection (Adjustable Version Only)

The FB pin is an input pin to sense the output voltage and close the loop for the adjustable version. The output voltage is sensed through a resistor-divider network to close the loop as shown in Figure 23. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit to improve performance at that point. Internally, FB connects to a high-impedance wide-bandwidth amplifier, and noise pickup feeds through to the regulator output. Routing the FB connection to minimize or avoid noise pickup is essential.

9.2.2.3 Programming the TPS76801-Q1 Adjustable LDO Regulator

The output voltage of the TPS76801-Q1 adjustable regulator is programmed using an external resistor divider as shown in Figure 23. The output voltage is calculated using Equation 1:

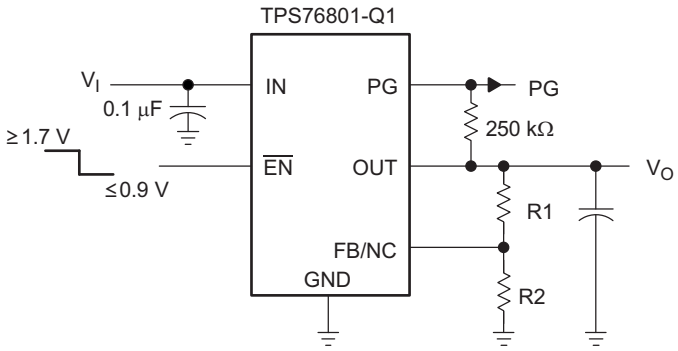
$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

where:

V_{ref} = 1.1834 V (typ) (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately 50-μA divider current. Lower-value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided, as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 30.1 kΩ to set the divider current at 50 μA and then calculate R1 using Equation 2:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \quad (2)$$



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	UNIT
2.5 V	33.2	30.1	kΩ
3.3 V	53.6	30.1	kΩ
3.6 V	61.9	30.1	kΩ
4.75 V	90.8	30.1	kΩ

Figure 23. TPS76801-Q1 Adjustable LDO Regulator Programming

9.2.2.4 External Capacitor Requirements

An input capacitor is not usually required; however, a ceramic bypass capacitor (0.047 μF or larger) improves load transient response and noise rejection if the TPS768xx-Q1 is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

Like all LDO regulators, the TPS768xx-Q1 requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 10 μF, and the equivalent series resistance (ESR) must be between 50 mΩ and 1.5 Ω. Capacitor values 10 μF or larger are acceptable, provided the ESR is less than 1.5 Ω . Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements previously described. Most of the commercially available 10-μF surface-mount ceramic capacitors meet the ESR requirements previously stated.

9.2.3 Application Curve

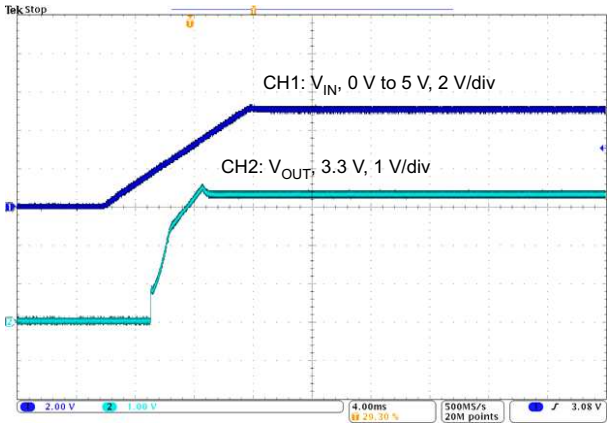


Figure 24. Power-Up Waveform of TPS76833-Q1

10 Power Supply Recommendations

The device is designed to operate from an input-voltage supply range between 2.7 V and 10 V. This input supply must be well regulated. If the input supply is located more than a few inches from the device, TI recommends adding a capacitor with a value of 0.1 µF and a ceramic bypass capacitor at the input.

11 Layout

11.1 Layout Guidelines

Input and output capacitors should be placed as close to the device pins as possible. To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for IN and OUT, with the ground planes connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should be connected directly to the GND pin of the device. High-ESR capacitors may degrade PSRR performance.

11.2 Layout Example

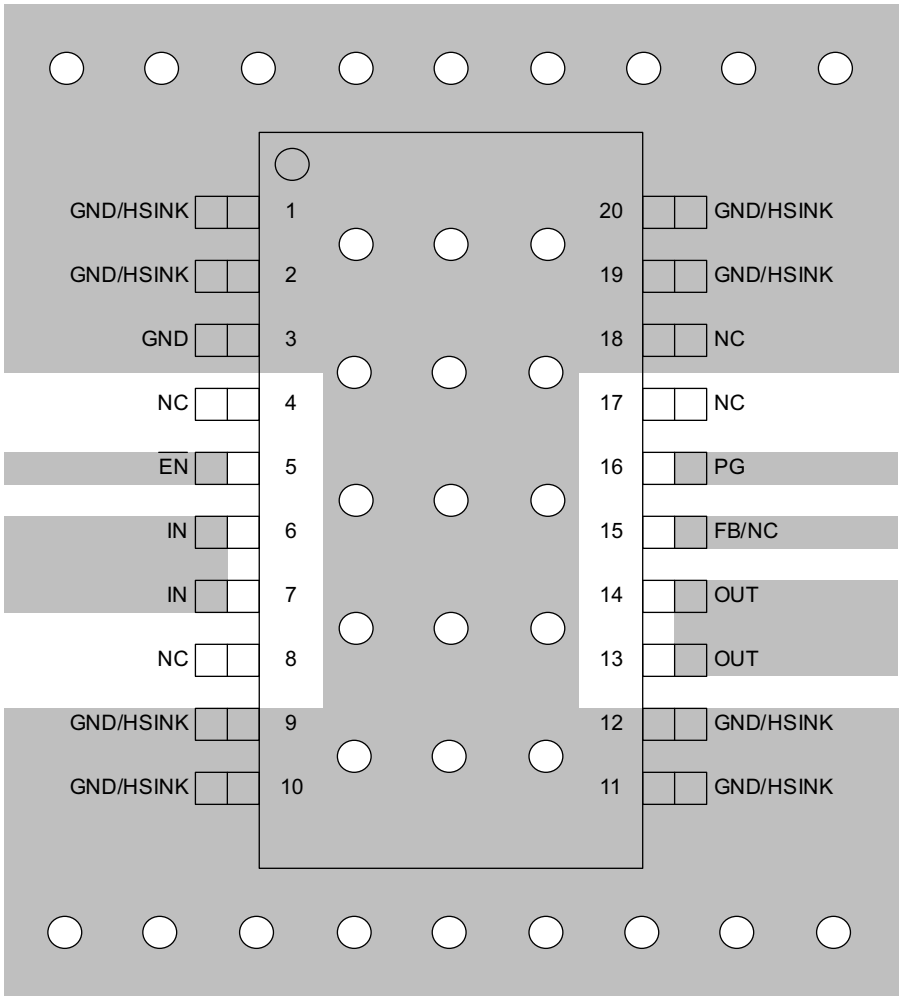


Figure 25. TPS768xx-Q1 Layout Example

11.3 Power Dissipation and Junction Temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_D$max, and the actual dissipation, P_D, which must be less than or equal to $P_D$max.

The maximum power dissipation limit is determined using Equation 3:

$$P_D\text{max} = \frac{T_J\text{max} - T_A}{R_{\theta JA}} \tag{3}$$

where:

$T_J$max = maximum allowable junction temperature

$R_{\theta JA}$ = junction-to-ambient thermal resistance for the package; that is, 32.6°C/W for the 20-pin TSSOP (PWP) with no airflow

T_A = ambient temperature

The regulator dissipation is calculated using Equation 4:

Power Dissipation and Junction Temperature (continued)

$$P_D = \left(V_I - V_O\right) \times I_O \quad (4)$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS76801QPWPRG4Q1	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	76801Q1
TPS76801QPWPRQ1	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	76801Q1
TPS76818QPWPRQ1	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	76818Q1
TPS76825QPWPRQ1	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	76825Q1
TPS76833QPWPRQ1	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	76833Q1
TPS76850QPWPRQ1	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	76850Q1

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TPS768-Q1 :

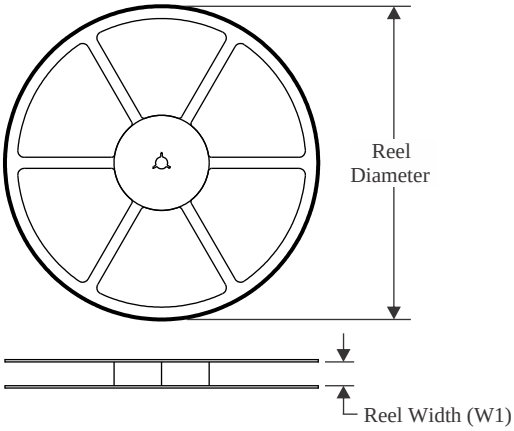
- Catalog : TPS768

NOTE: Qualified Version Definitions:

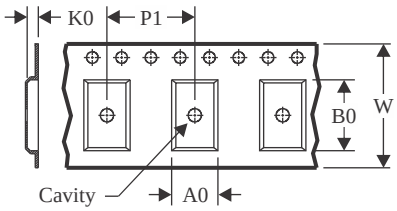
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

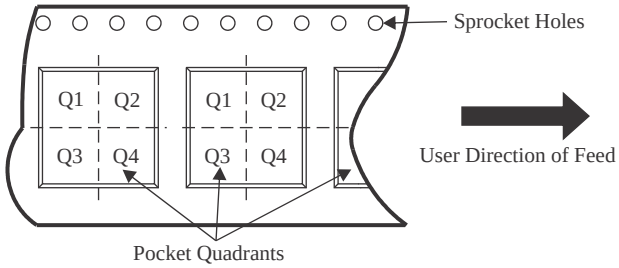


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

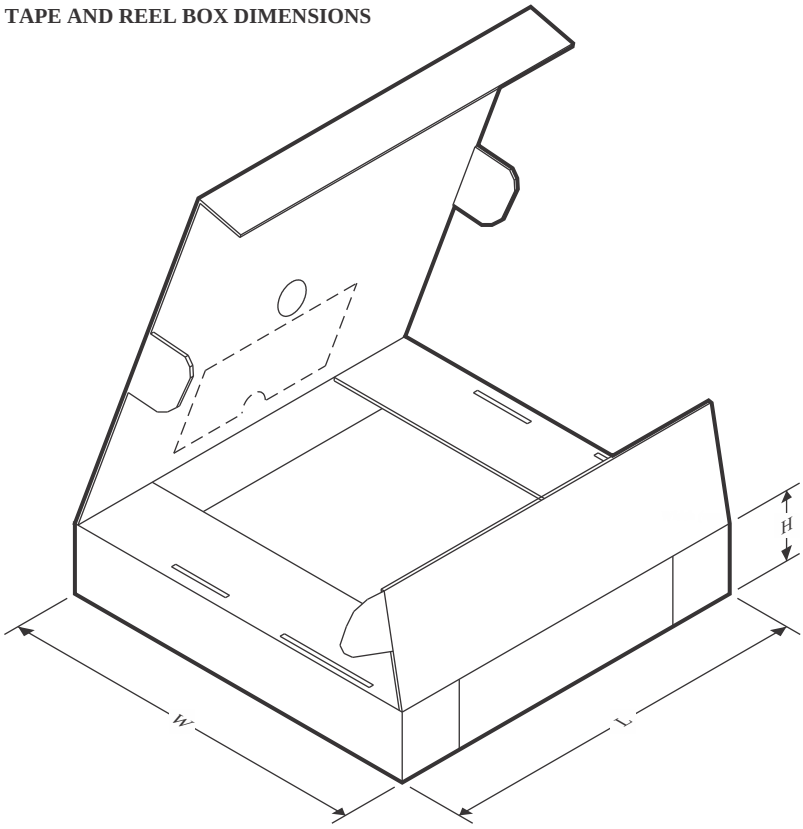
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS76801QPWPRG4Q1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS76801QPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS76818QPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS76825QPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS76833QPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS76850QPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS76801QPWPRG4Q1	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS76801QPWPRQ1	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS76818QPWPRQ1	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS76825QPWPRQ1	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS76833QPWPRQ1	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS76850QPWPRQ1	HTSSOP	PWP	20	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

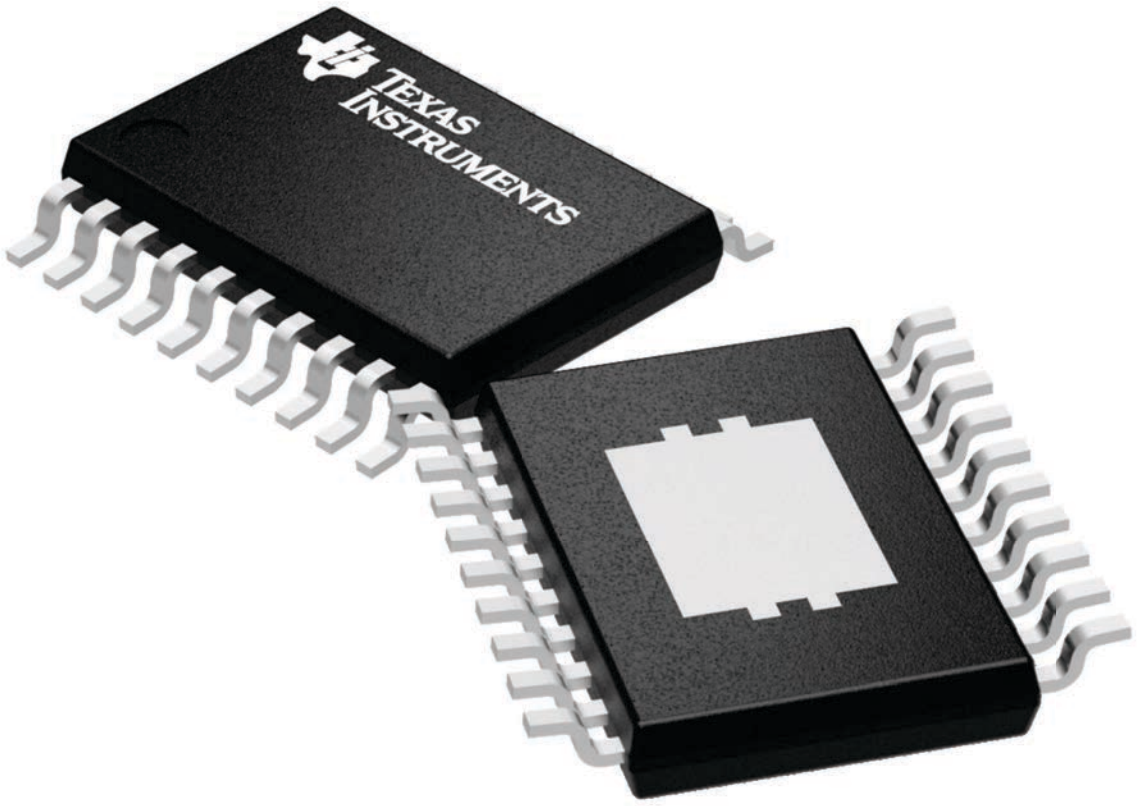
PWP 20

HTSSOP - 1.2 mm max height

6.5 x 4.4, 0.65 mm pitch

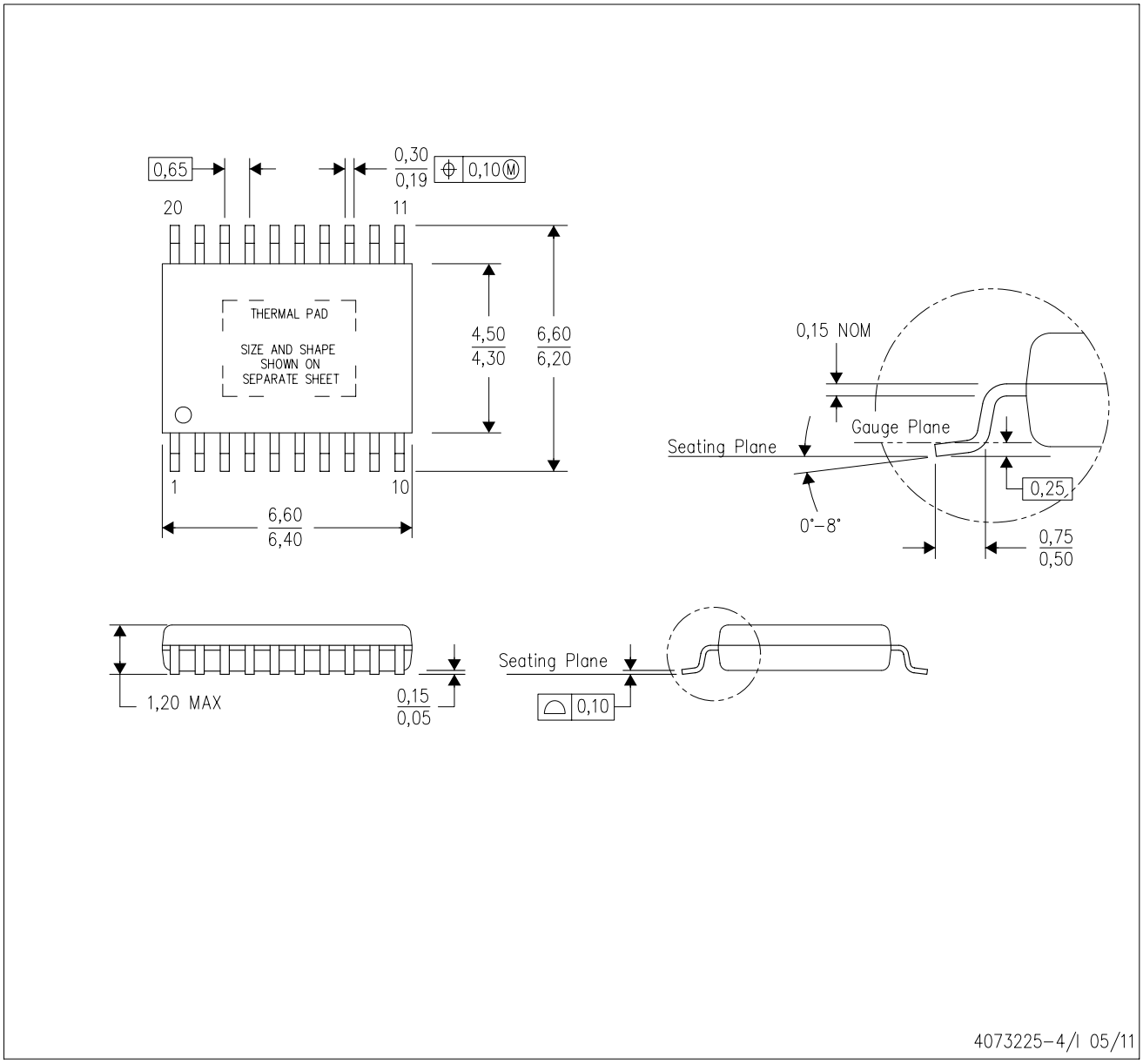
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224669/A

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

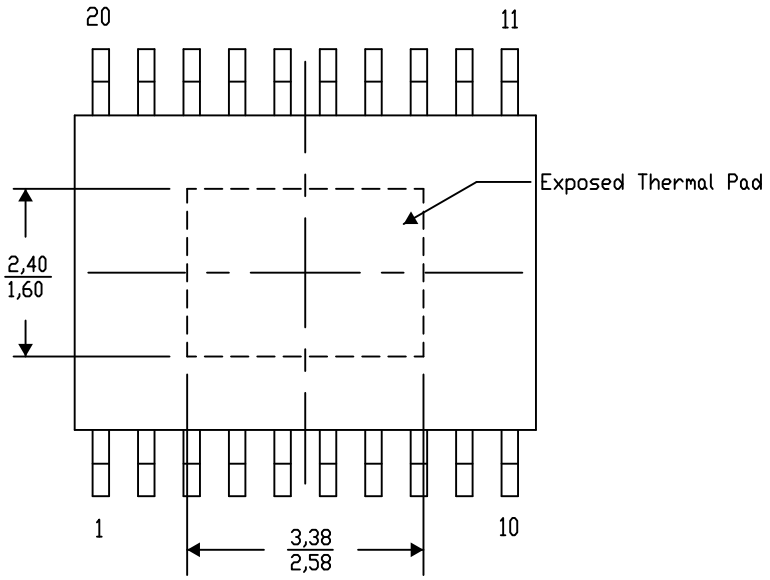
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

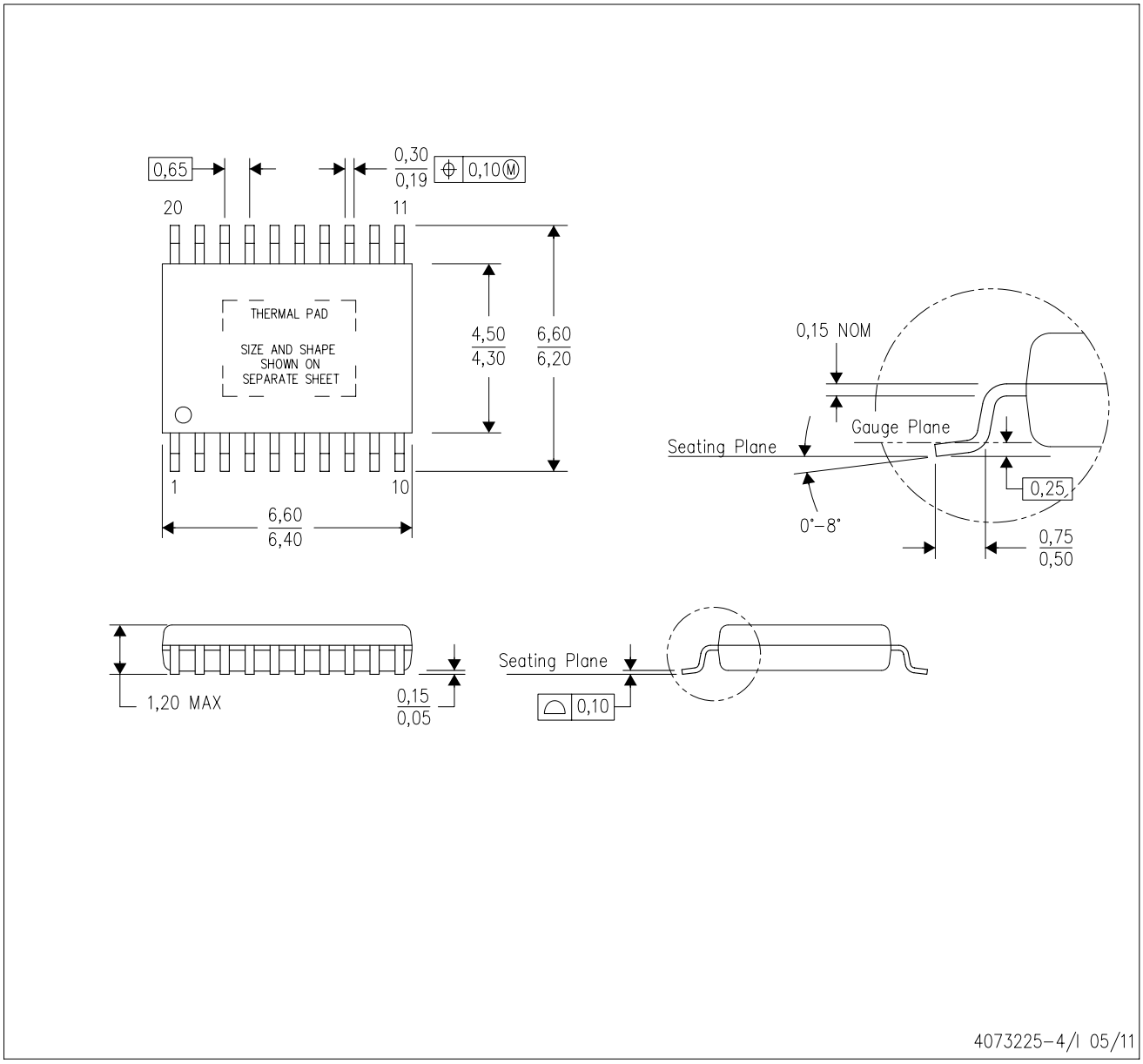
Exposed Thermal Pad Dimensions

4206332–21/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



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E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

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PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

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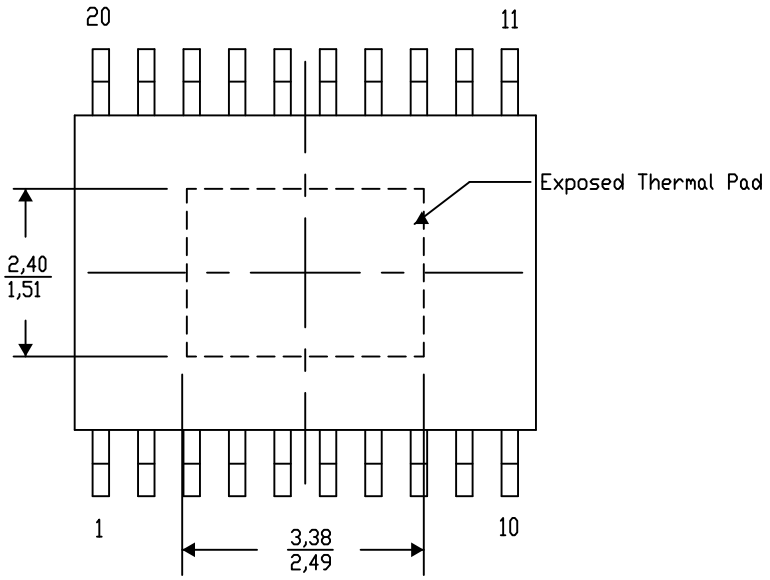


Top View

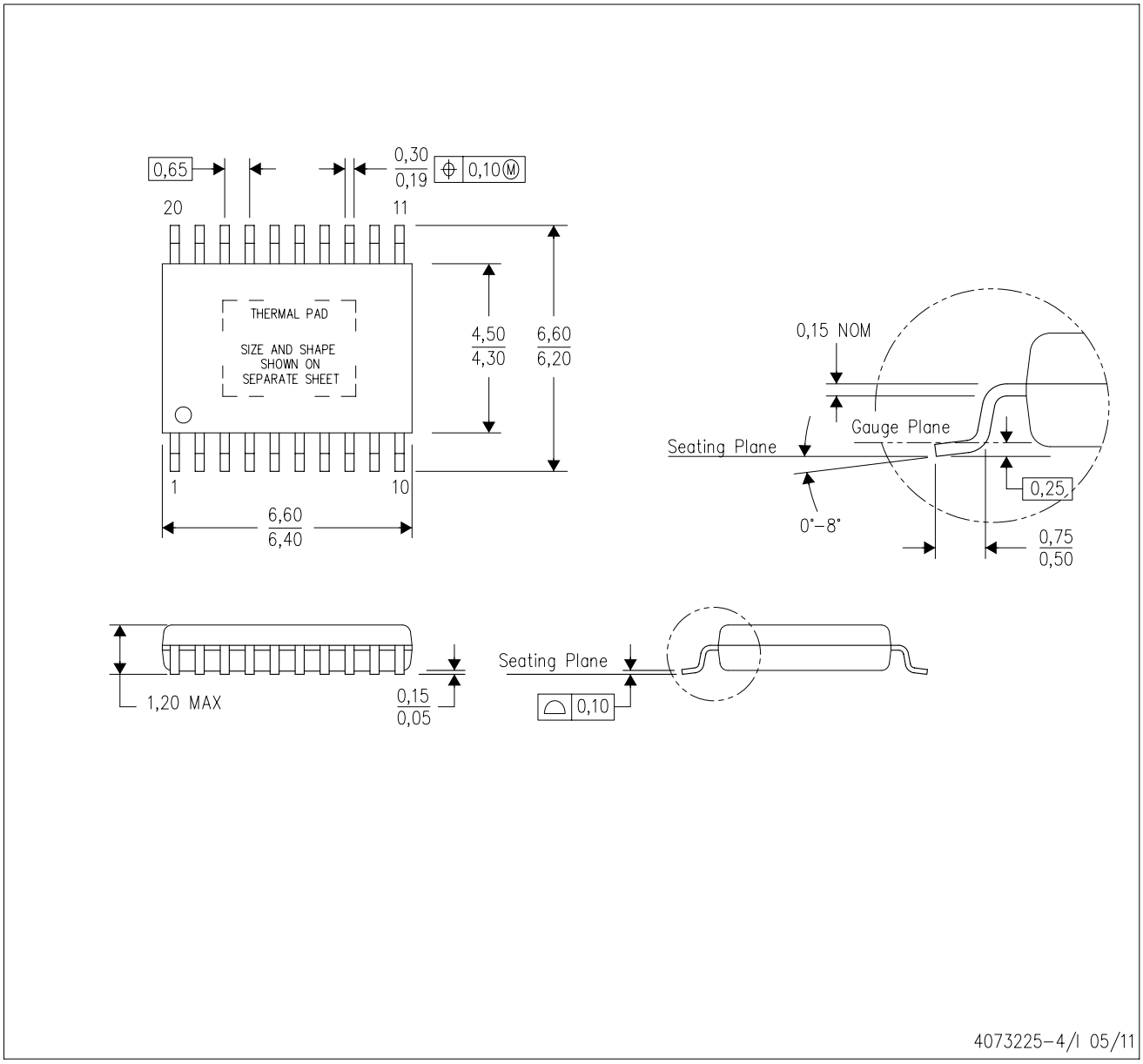
Exposed Thermal Pad Dimensions

4206332–20/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

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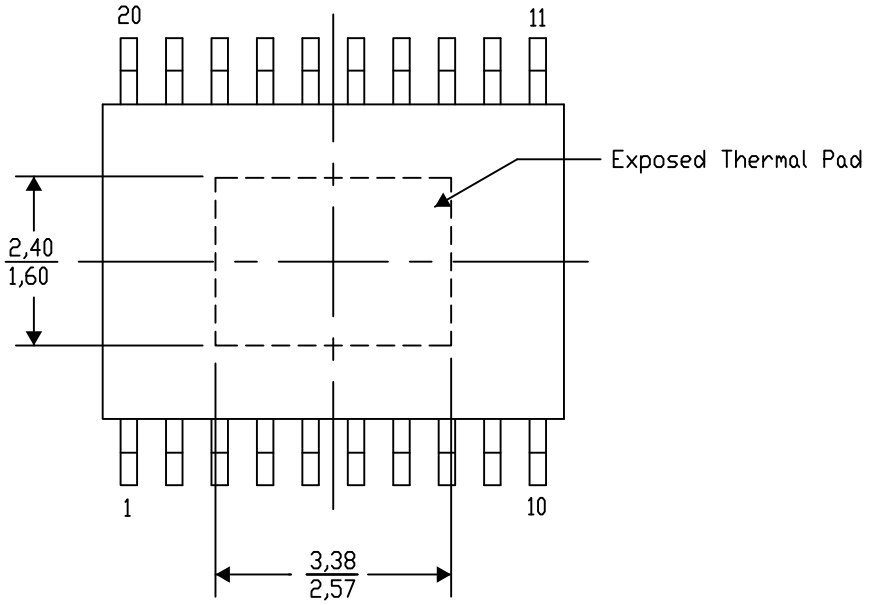
The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

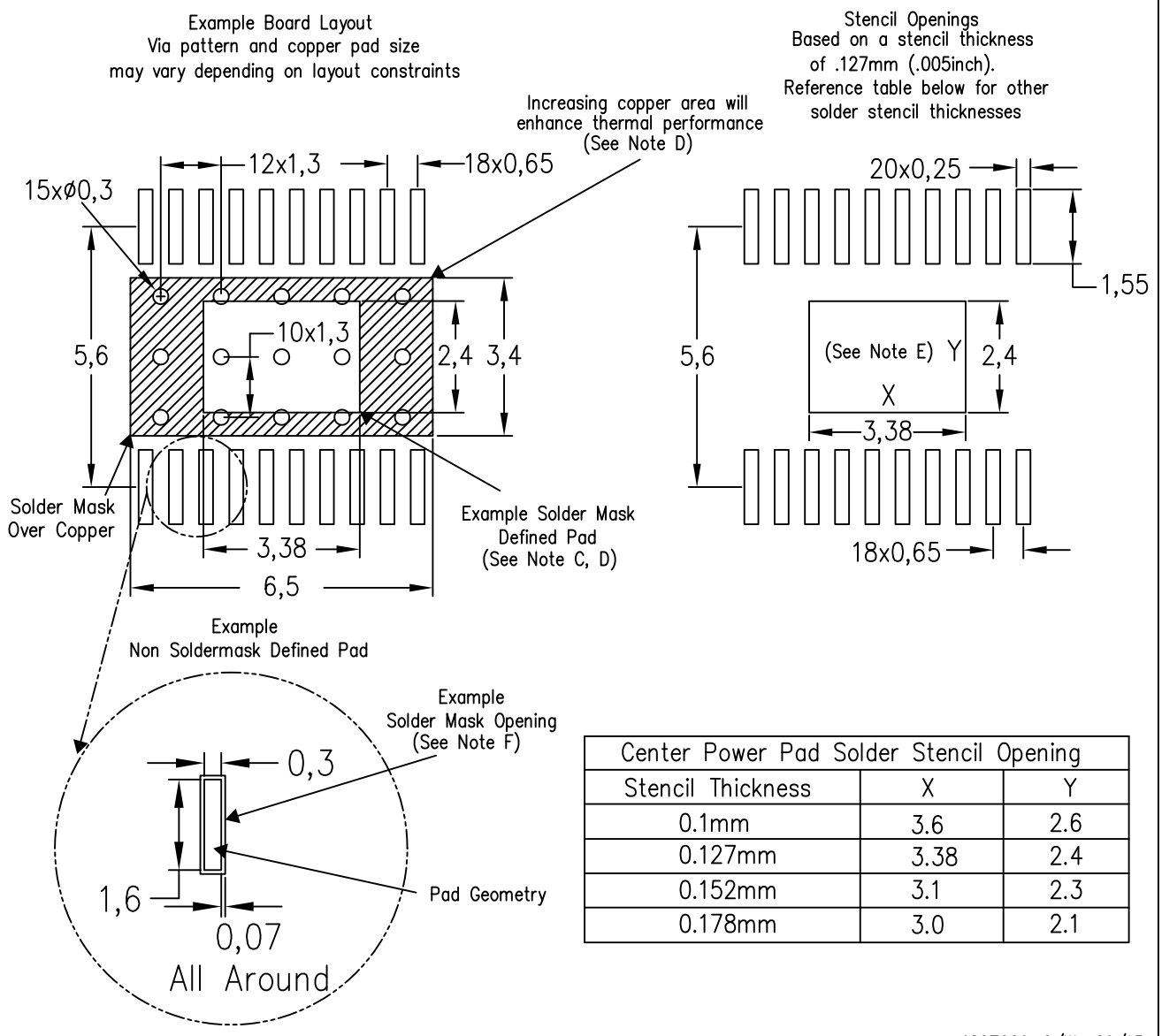
Exposed Thermal Pad Dimensions

4206332–13/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE

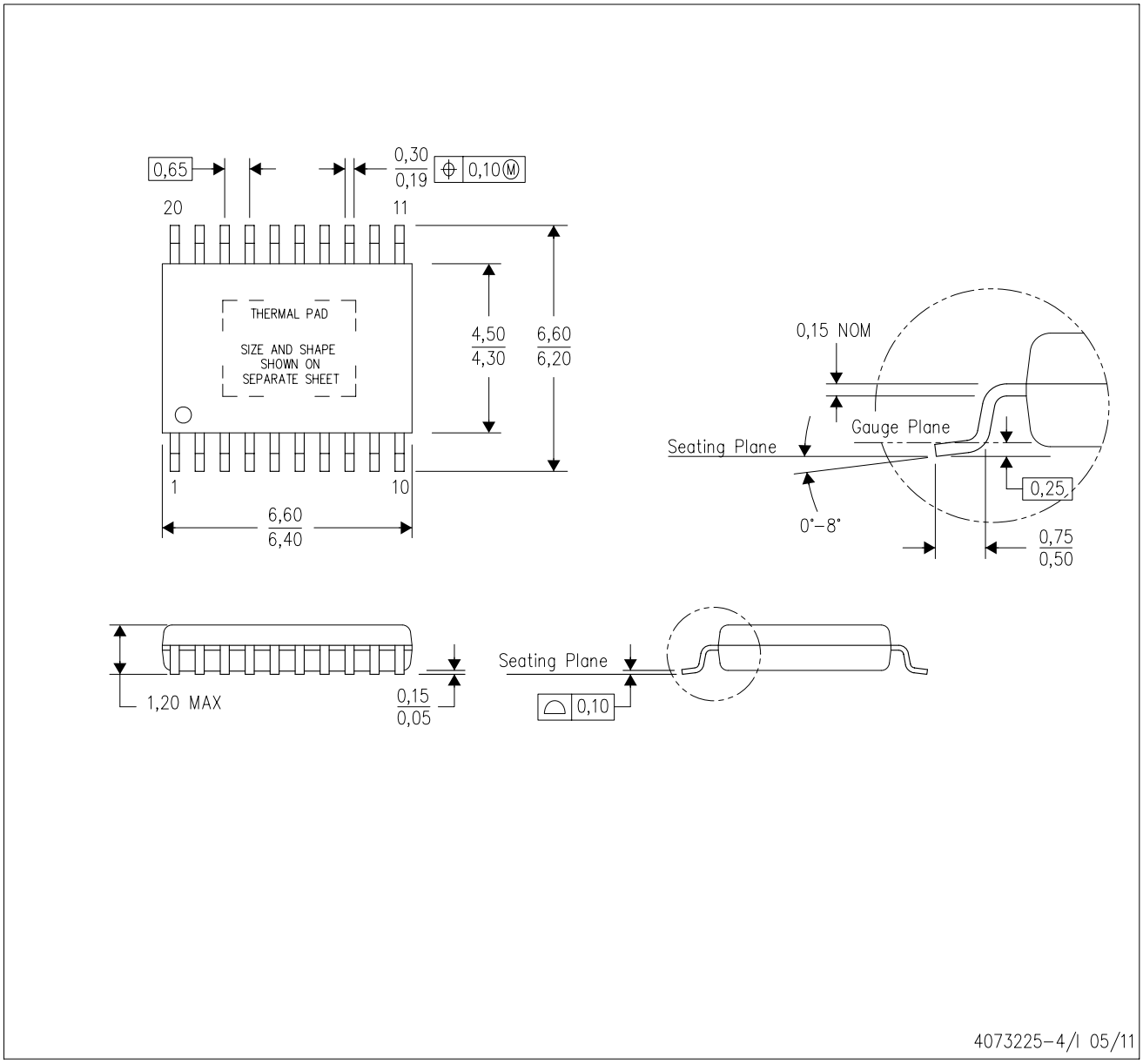


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.6	2.6
0.127mm	3.38	2.4
0.152mm	3.1	2.3
0.178mm	3.0	2.1

4207609–6/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
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E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

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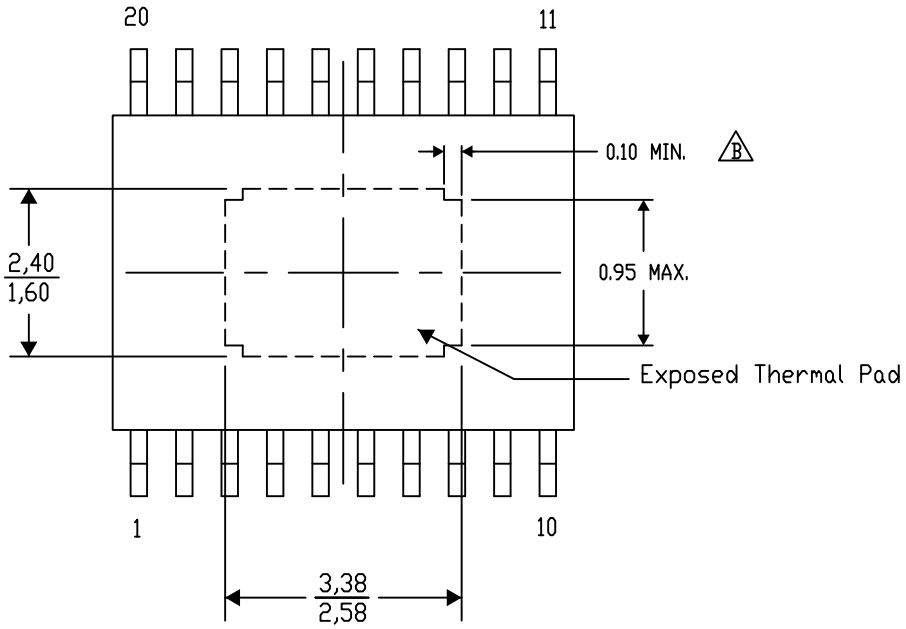
For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332–23/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B Exposed tie strap features may not be present.

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