

# AD7801–SPECIFICATIONS

( $V_{DD} = +2.7\text{ V to }+5.5\text{ V}$ , Internal Reference;  $C_L = 100\text{ pF}$ ,  $R_L = 10\text{ k}\Omega$  to  $V_{DD}$  and GND.  
All specifications  $T_{MIN}$  to  $T_{MAX}$  unless otherwise noted.)

| Parameter                                 | B Versions <sup>1</sup> | Units                            | Conditions/Comments                         |
|---|-------------------------|----------------------------------|---|
| <b>STATIC PERFORMANCE</b>                 |                         |                                  |   |
| Resolution                                | 8                       | Bits                             |   |
| Relative Accuracy <sup>2</sup>            | $\pm 1$                 | LSB max                          |   |
| Differential Nonlinearity                 | $\pm 1$                 | LSB max                          | Guaranteed Monotonic                        |
| Zero-Code Error @ +25°C                   | 3                       | LSB typ                          | All Zeros Loaded to DAC Register            |
| Full-Scale Error                          | -0.75                   | LSB typ                          | All Ones Loaded to DAC Register             |
| Zero-Code Error Drift                     | 100                     | $\mu\text{V}/^\circ\text{C}$ typ |   |
| Gain Error <sup>3</sup>                   | $\pm 1$                 | % FSR typ                        |   |
| <b>DAC REFERENCE INPUT</b>                |                         |                                  |   |
| REFIN Input Range                         | 1 to $V_{DD}/2$         | V min/V max                      |   |
| REFIN Input Impedance                     | 10                      | M $\Omega$ typ                   |   |
| <b>OUTPUT CHARACTERISTICS</b>             |                         |                                  |   |
| Output Voltage Range                      | 0 to $V_{DD}$           | V min/V max                      |   |
| Output Voltage Settling Time              | 2                       | $\mu\text{s}$ max                | Typically 1.2 $\mu\text{s}$                 |
| Slew Rate                                 | 7.5                     | V/ $\mu\text{s}$ typ             |   |
| Digital-to-Analog Glitch Impulse          | 1                       | nV-s typ                         | 1 LSB Change Around Major Carry             |
| Digital Feedthrough                       | 0.2                     | nV-s typ                         |   |
| DC Output Impedance                       | 40                      | $\Omega$ typ                     |   |
| Short Circuit Current                     | 14                      | mA typ                           |   |
| Power Supply Rejection Ratio <sup>4</sup> | 0.0003                  | %/% max                          | $\Delta V_{DD} = \pm 10\%$                  |
| <b>LOGIC INPUTS</b>                       |                         |                                  |   |
| Input Current                             | $\pm 10$                | $\mu\text{A}$ max                |   |
| $V_{INL}$ , Input Low Voltage             | 0.8                     | V max                            | $V_{DD} = +5\text{ V}$                      |
| $V_{INL}$ , Input Low Voltage             | 0.6                     | V max                            | $V_{DD} = +3\text{ V}$                      |
| $V_{INH}$ , Input High Voltage            | 2.4                     | V min                            | $V_{DD} = +5\text{ V}$                      |
| $V_{INH}$ , Input High Voltage            | 2.1                     | V min                            | $V_{DD} = +3\text{ V}$                      |
| Pin Capacitance                           | 7                       | pF max                           |   |
| <b>POWER REQUIREMENTS</b>                 |                         |                                  |   |
| $V_{DD}$                                  | 2.7/5.5                 | V min/V max                      |   |
| $I_{DD}$ (Normal Mode)                    |                         |                                  | DAC Active and Excluding Load Current       |
| $V_{DD} = 3.3\text{ V}$                   |                         |                                  | $V_{IH} = V_{DD}$ and $V_{IL} = \text{GND}$ |
| @ 25°C                                    | 1.55                    | mA max                           | See Figure 6                                |
| $T_{MIN}$ to $T_{MAX}$                    | 1.75                    | mA max                           |   |
| $V_{DD} = 5.5\text{ V}$                   |                         |                                  |   |
| @ 25°C                                    | 2.35                    | mA max                           |   |
| $T_{MIN}$ to $T_{MAX}$                    | 2.5                     | mA max                           |   |
| $I_{DD}$ (Power-Down)                     |                         |                                  |   |
| @ 25°C                                    | 1                       | $\mu\text{A}$ max                | $V_{IH} = V_{DD}$ and $V_{IL} = \text{GND}$ |
| $T_{MIN}$ to $T_{MAX}$                    | 2                       | $\mu\text{A}$ max                | See Figure 18                               |

## NOTES

<sup>1</sup>Temperature ranges are as follows: B Version: -40°C to +105°C

<sup>2</sup>Relative Accuracy is calculated using a reduced code range of 15 to 245.

<sup>3</sup>Gain Error is specified between Codes 15 and 245. The actual error at Code 15 is typically 3 LSB.

<sup>4</sup>Guaranteed by characterization at product release, not production tested.

Specifications subject to change without notice.

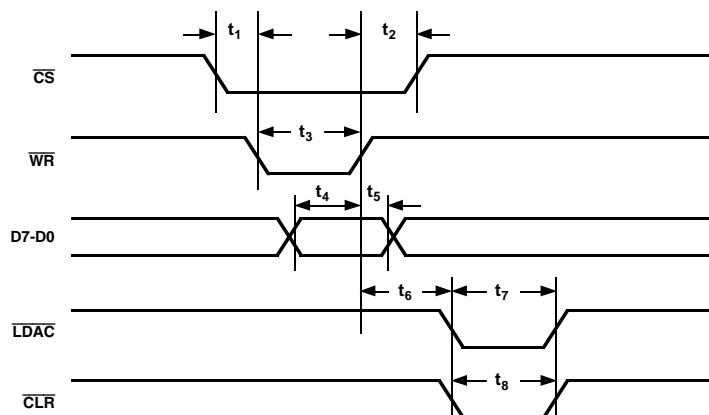


Figure 1. Timing Diagram for Parallel Data Write

# TIMING CHARACTERISTICS<sup>1, 2</sup> ( $V_{DD} = +2.7\text{ V to }+5.5\text{ V}$ ; $GND = 0\text{ V}$ ; Internal $V_{DD}/2$ Reference. All specifications $T_{MIN}$ to $T_{MAX}$ unless otherwise noted.)

| Parameter | Limit at $T_{MIN}$ , $T_{MAX}$<br>(B Version) | Units  | Conditions/Comments                   |
|-----------|---|--------|---------------------------------------|
| $t_1$     | 0   | ns min | Chip Select to Write Setup Time       |
| $t_2$     | 0   | ns min | Chip Select to Write Hold Time        |
| $t_3$     | 20  | ns min | Write Pulse Width                     |
| $t_4$     | 15  | ns min | Data Setup Time                       |
| $t_5$     | 4.5   | ns min | Data Hold Time                        |
| $t_6$     | 20  | ns min | Write to $\overline{LDAC}$ Setup Time |
| $t_7$     | 20  | ns min | $\overline{LDAC}$ Pulse Width         |
| $t_8$     | 20  | ns min | CLR Pulse Width                       |

## NOTES

<sup>1</sup>Sample tested at +25°C to ensure compliance. All input signals are specified with  $t_r = t_f = 5\text{ ns}$  (10% to 90% of  $V_{DD}$ ) and timed from a voltage level of  $(V_{IL} + V_{IH})/2$ .  $t_r$  and  $t_f$  should not exceed 1  $\mu\text{s}$  on any digital input.

<sup>2</sup>See Figure 1.

## ABSOLUTE MAXIMUM RATINGS\*

( $T_A = +25^\circ\text{C}$  unless otherwise noted)

|                                 |                                   |
|---------------------------------|-----------------------------------|
| $V_{DD}$ to GND                 | −0.3 V to +7 V                    |
| Reference Input Voltage to AGND | −0.3 V to $V_{DD} + 0.3\text{ V}$ |
| Digital Input Voltage to DGND   | −0.3 V to $V_{DD} + 0.3\text{ V}$ |
| AGND to DGND                    | −0.3 V to +0.3 V                  |
| $V_{OUT}$ to AGND               | −0.3 V to $V_{DD} + 0.3\text{ V}$ |
| Operating Temperature Range     |                                   |
| Commercial (B Version)          | −40°C to +105°C                   |
| Storage Temperature Range       | −65°C to +150°C                   |
| Junction Temperature            | +150°C                            |
| SSOP Package, Power Dissipation | 700 mW                            |
| $\theta_{JA}$ Thermal Impedance | 143°C/W                           |
| Lead Temperature, Soldering     |                                   |
| Vapor Phase (60 sec)            | +215°C                            |
| Infrared (15 sec)               | +220°C                            |
| SOIC Package, Power Dissipation | 870 mW                            |
| $\theta_{JA}$ Thermal Impedance | 74°C/W                            |
| Lead Temperature, Soldering     |                                   |
| Vapor Phase (60 sec)            | +215°C                            |
| Infrared (15 sec)               | +220°C                            |

\*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7801 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

## ORDERING GUIDE

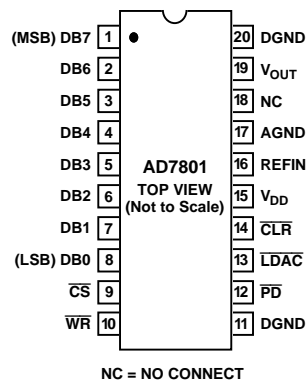
| Model     | Temperature Range | Package Option* |
|-----------|-------------------|-----------------|
| AD7801BR  | −40°C to +105°C   | R-20            |
| AD7801BRU | −40°C to +105°C   | RU-20           |

\*R = Small Outline; RU = Thin Shrink Small Outline.



AD7801

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

| Pin No. | Mnemonic          | Function  |
|---------|-------------------|---|
| 1-8     | D7-D0             | Parallel Data Inputs. 8-bit data is loaded to the input register of the AD7801 under the control of $\overline{CS}$ and $\overline{WR}$ .   |
| 9       | $\overline{CS}$   | Chip Select. Active low logic input.  |
| 10      | $\overline{WR}$   | Write Input. $\overline{WR}$ is an active low logic input used in conjunction with $\overline{CS}$ to write data to the input register.   |
| 11      | DGND              | Digital Ground  |
| 12      | $\overline{PD}$   | Active low input used to put the part into low power mode reducing current consumption to less than 1 $\mu$ A.  |
| 13      | $\overline{LDAC}$ | Load DAC Logic Input. When this logic input is taken low the DAC output is updated with the contents of its DAC register. If $\overline{LDAC}$ is permanently tied low the DAC is updated on the rising edge of $\overline{WR}$ . |
| 14      | $\overline{CLR}$  | Asynchronous Clear Input (Active Low). When this input is taken low the DAC register is loaded with all zeroes and the DAC output is cleared to zero volts.   |
| 15      | $V_{DD}$          | Power Supply Input. This part can be operated from +2.7 V to +5.5 V and should be decoupled to GND.   |
| 16      | REFIN             | External Reference Input. This can be used as the reference for the DAC. The range on this reference input is 1 V to $V_{DD}/2$ . If REFIN is tied directly to $V_{DD}$ the internal $V_{DD}/2$ reference is selected.            |
| 17      | AGND              | Analog Ground reference point and return point for all analog current on the part.  |
| 18      | NC                | No Connect Pin.   |
| 19      | $V_{OUT}$         | Analog Output Voltage from the DAC. The output amplifier can swing rail to rail on its output.  |
| 20      | DGND              | Digital Ground reference point and return point for all digital current on the part.  |

# Typical Performance Characteristics–AD7801

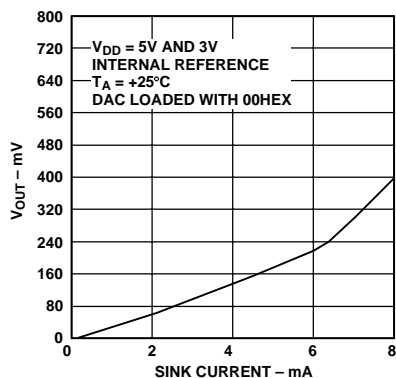


Figure 2. Output Sink Current Capability with  $V_{DD} = 3\text{ V}$  and  $V_{DD} = 5\text{ V}$

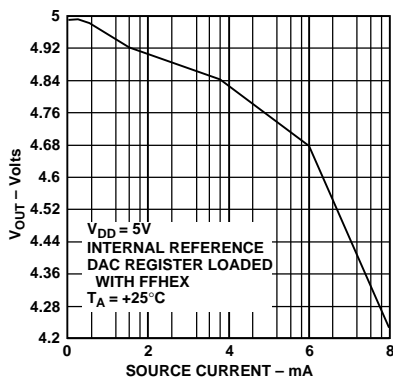


Figure 3. Output Source Current Capability with  $V_{DD} = 5\text{ V}$

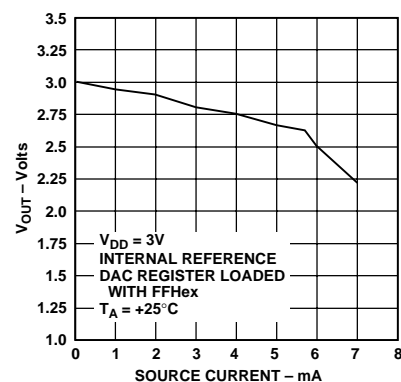


Figure 4. Output Source Current Capability with  $V_{DD} = 3\text{ V}$

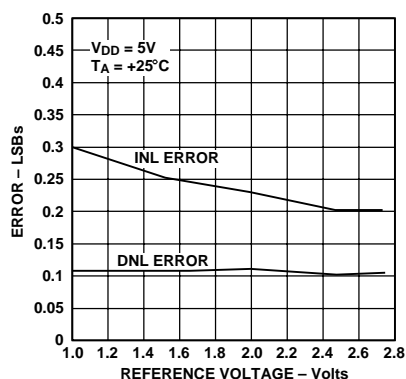


Figure 5. Relative Accuracy vs. External Reference

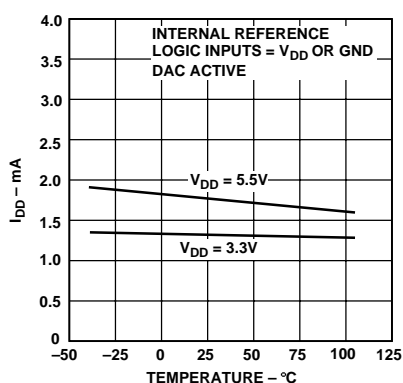


Figure 6. Typical Supply Current vs. Temperature

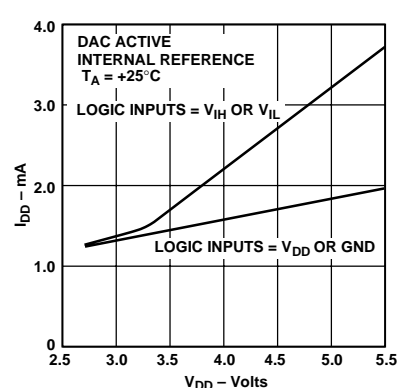


Figure 7. Typical Supply Current vs. Supply Voltage

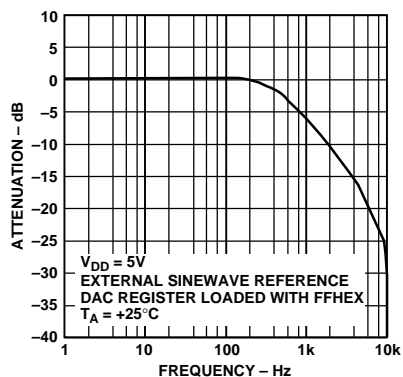


Figure 8. Large Scale Signal Frequency Response

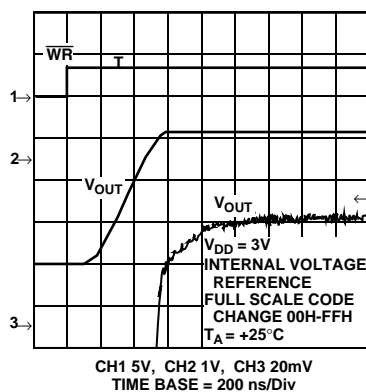


Figure 9. Full-Scale Settling Time

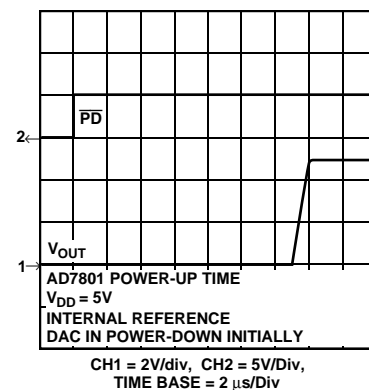


Figure 10. Exiting Power-Down (Full Power-Down)

# AD7801—Typical Performance Characteristics

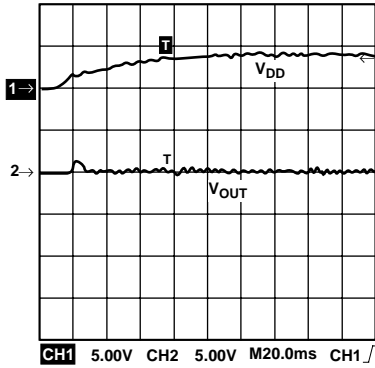


Figure 11. Power-On—Reset

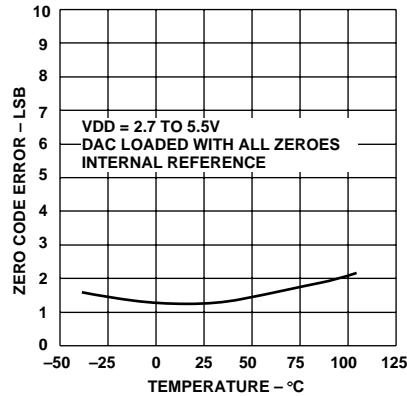


Figure 12. Zero Code Error vs. Temperature

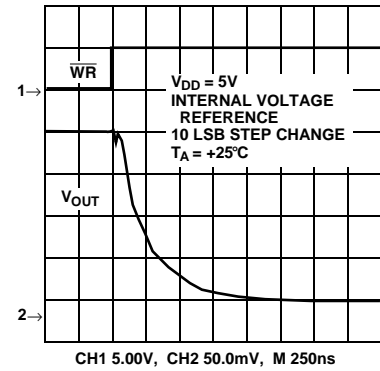


Figure 13. Small-Scale Settling Time

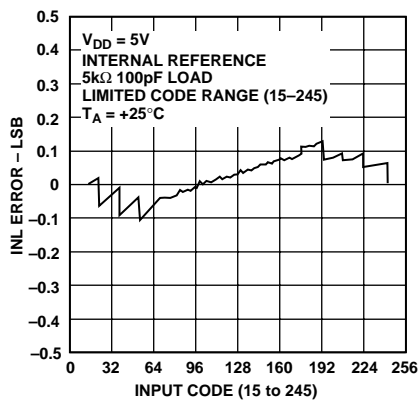


Figure 14. Integral Linearity Plot

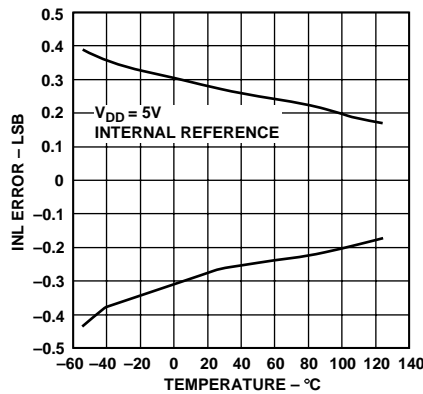


Figure 15. Typical INL vs. Temperature

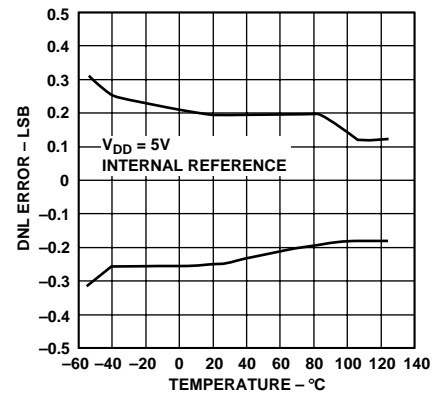


Figure 16. Typical DNL vs. Temperature

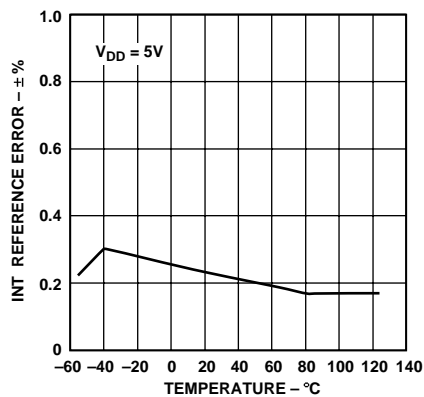


Figure 17. Typical Internal Reference Error vs. Temperature

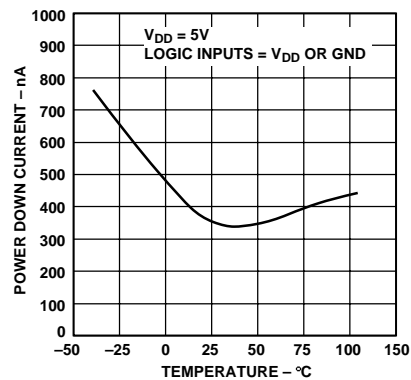


Figure 18. Power-Down Current vs. Temperature



# AD7801

## Reference

The AD7801 has the ability to use either an external reference applied through the REFIN pin or an internal reference generated from  $V_{DD}$ . Figure 20 shows the reference input arrangement where either the internal  $V_{DD}/2$  or the externally applied reference can be selected.

The internal reference is selected by tying the REFIN pin to  $V_{DD}$ . If an external reference is to be used, this can be directly applied to the REFIN pin and if this is 1 V below  $V_{DD}$ , the internal circuitry will select this externally applied reference as the reference source for the DAC.

## Digital Interface

The AD7801 contains a fast parallel interface allowing this DAC to interface to industry standard microprocessors, microcontrollers and DSP machines. There are two modes in which this parallel interface can be configured to update the DAC output. The synchronous update mode allows synchronous updating of the DAC output; the automatic update mode allows the DAC to be updated individually following a write cycle. Figure 21 shows the internal logic associated with the digital interface. The PON STRB signal is internally generated from the power-on reset circuitry and is low during the power-on reset phase of the power up procedure.

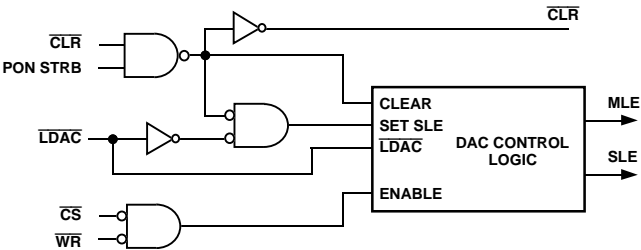


Figure 21. Logic Interface

The AD7801 has a double buffered interface, which allows for synchronous updating of the DAC output. Figure 22 shows a block diagram of the register arrangement within the AD7801.

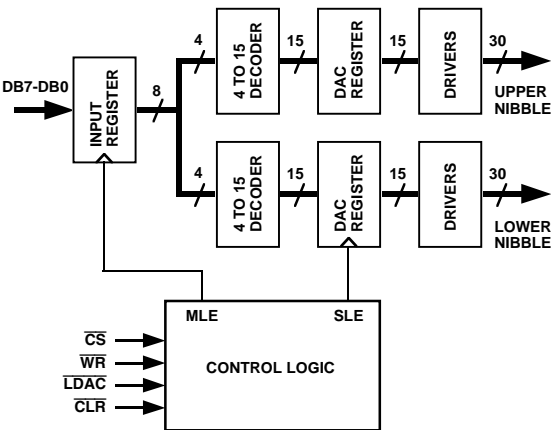


Figure 22. Register Arrangement

## Automatic Update Mode

In this mode of operation the  $\overline{LDAC}$  signal is permanently tied low. The state of the  $\overline{LDAC}$  is sampled on the rising edge of  $\overline{WR}$ .  $\overline{LDAC}$  being low allows the DAC register to be automatically updated on the rising edge of  $\overline{WR}$ . The output update occurs on the rising edge of  $\overline{WR}$ . Figure 23 shows the timing associated with the automatic update mode of operation and also the status of the various registers during this frame.

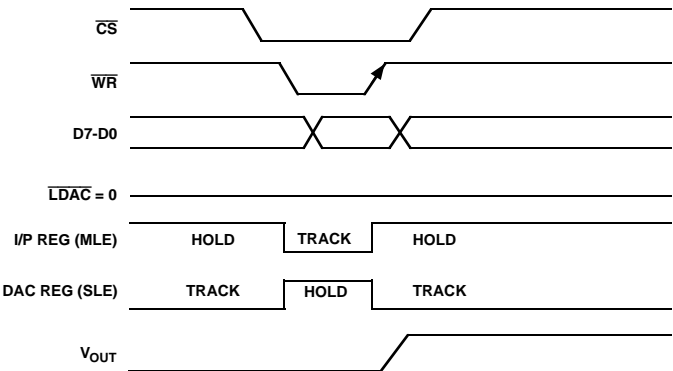


Figure 23. Timing and Register Arrangement for Automatic Update Mode

## Synchronous Update Mode

In this mode of operation the  $\overline{LDAC}$  signal is used to update the DAC output to synchronize with other updates in the system. The state of the  $\overline{LDAC}$  is sampled on the rising edge of  $\overline{WR}$ . If  $\overline{LDAC}$  is high, the automatic update mode is disabled and the DAC latch is updated at any time after the write by taking  $\overline{LDAC}$  low. The output update occurs on the falling edge of  $\overline{LDAC}$ .  $\overline{LDAC}$  must be taken back high again before the next data transfer takes place. Figure 24 shows the timing associated with the synchronous update mode of operation and also the status of the various registers during this frame.

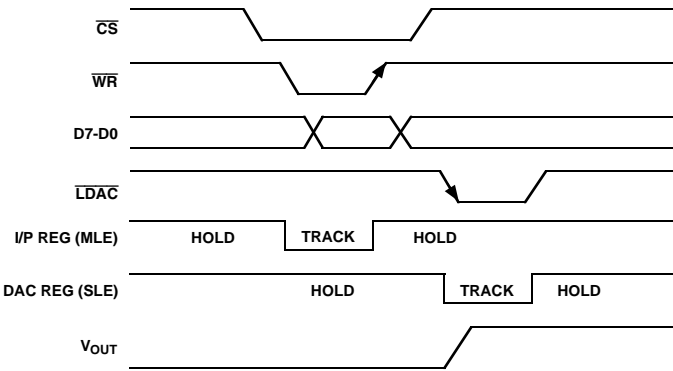


Figure 24. Timing and Register Arrangement for Synchronous Update Mode



### POWER-ON RESET

The AD7801 has a power-on reset circuit designed to allow output stability during power up. This circuit holds the DAC in a reset state until a write takes place to the DAC. In the reset state all zeros are latched into the input register of the DAC and the DAC register is in transparent mode thus the output of the DAC is held at ground potential until a write takes place to the DAC. The power-on reset circuitry generates a PON STRB signal which is a gating signal used within the logic to identify a power-on condition.

### POWER-DOWN FEATURES

The AD7801 has a power-down feature implemented by exercising the external PD pin. An active low signal puts the complete DAC into power-down mode. When in power-down, the current consumption of the device is reduced to less than 1  $\mu\text{A}$  max at +25°C or 2  $\mu\text{A}$  max over temperature, making the device suitable for use in portable battery powered equipment. The internal reference resistors, the reference bias servo loop, the output amplifier and associated linear circuitry are all shut down when the power-down is activated. The output terminal sees a load of  $\approx 23 \text{ k}\Omega$  to GND when in power-down mode as shown in Figure 25. The contents of the data register are unaffected when in power-down mode. The device typically comes out of power-down in 13  $\mu\text{s}$  (see Figure 10).

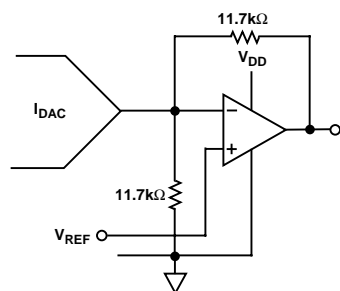


Figure 25. Output Stage During Power-Down

### Analog Outputs

The AD7801 contains a voltage output DAC with 8-bit resolution and rail-to-rail operation. The output buffer provides a gain of two at the output. Figures 2, 3 and 4 show the source and sink capabilities of the output amplifier. The slew rate of the output amplifier is typically 7.5 V/ $\mu\text{s}$  and has a full-scale settling to eight bits with a 100 pF capacitive load in typically 1.2  $\mu\text{s}$ .

The input coding to the DAC is straight binary. Table I shows the binary transfer function for the AD7801. Figure 26 shows the DAC transfer function for binary coding. Any DAC output voltage can be expressed as:

$$V_{OUT} = 2 \times V_{REF} \left( \frac{N}{256} \right)$$

where:

$N$  is the decimal equivalent of the binary input code.  $N$  ranges from 0 to 255.

$V_{REF}$  is the voltage applied to the external REFIN pin when the external reference is selected and is  $V_{DD}/2$  if the internal reference is used.

Table I. Output Voltage for Selected Input Codes

| Digital<br>MSB . . . LSB | Analog Output                               |
|--------------------------|---|
| 1111 1111                | $2 \times \frac{255}{256} \times V_{REF} V$ |
| 1111 1110                | $2 \times \frac{254}{256} \times V_{REF} V$ |
| 1000 0001                | $2 \times \frac{129}{256} \times V_{REF} V$ |
| 1000 0000                | $V_{REF} V$                                 |
| 0111 1111                | $2 \times \frac{127}{256} \times V_{REF} V$ |
| 0000 0001                | $2 \times \frac{V_{REF}}{256} V$            |
| 0000 0000                | 0 V   |

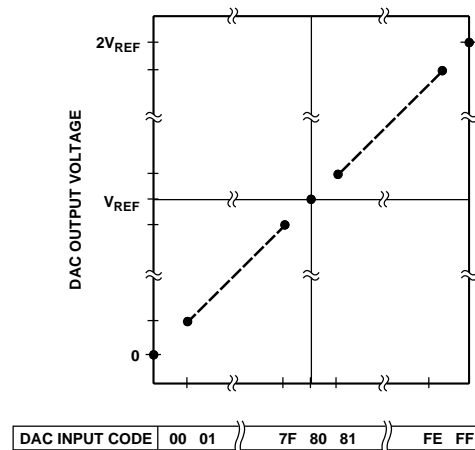


Figure 26. DAC Transfer Function

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Figure 27 shows a typical setup for the AD7801 when using its internal reference. The internal reference is selected by tying the REF IN pin to  $V_{DD}$ . Internally in the reference section there is a reference detect circuit that will select the internal  $V_{DD}/2$  based on the voltage connected to the REF IN pin. If REF IN is within a threshold voltage of a PMOS device (approximately 1 V) of  $V_{DD}$  the internal reference is selected. When the REF IN voltage is more than 1 V below  $V_{DD}$ , the externally applied voltage at this pin is used as the reference for the DAC. The internal reference on the AD7801 is  $V_{DD}/2$ , the output current to voltage converter within the AD7801 provides a gain of two. Thus the output range of the DAC is from 0 V to  $V_{DD}$ , based on Table I.

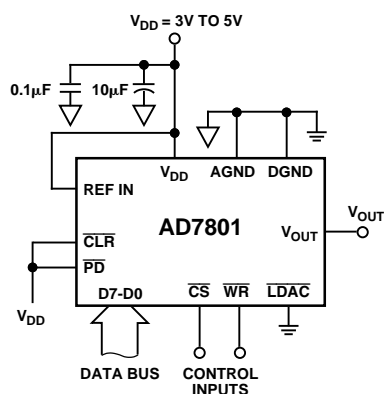


Figure 27. Typical Configuration Selecting the Internal Reference

Figure 28 shows a typical setup for the AD7801 when using an external reference. The reference range for the AD7801 is from 1 V to  $V_{DD}/2$  V. Higher values of reference can be incorporated but will saturate the output at both the top and bottom end of the transfer function. There is a gain of two from input to output on the AD7801. Suitable references for 5 V operation are the AD780 and REF192. For 3 V operation a suitable external reference would be the AD589 a 1.23 V bandgap reference.

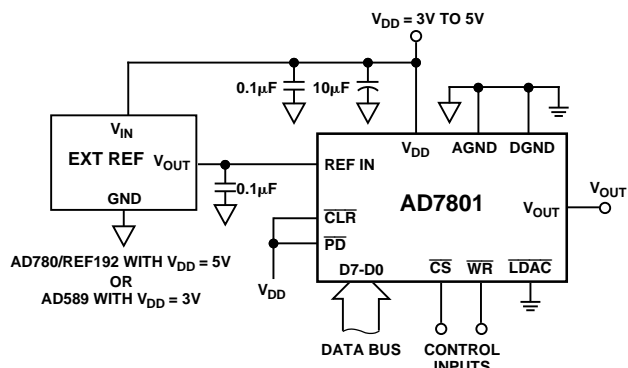


Figure 28. Typical Configuration Using An External Reference

## MICROPROCESSOR INTERFACING

### AD7801-ADSP-2101/ADSP-2103 Interface

Figure 29 shows an interface between the AD7801 and the ADSP-2101/ADSP-2103. The fast interface timing associated with the AD7801 allows easy interface to the ADSP-2101/ADSP-2103.

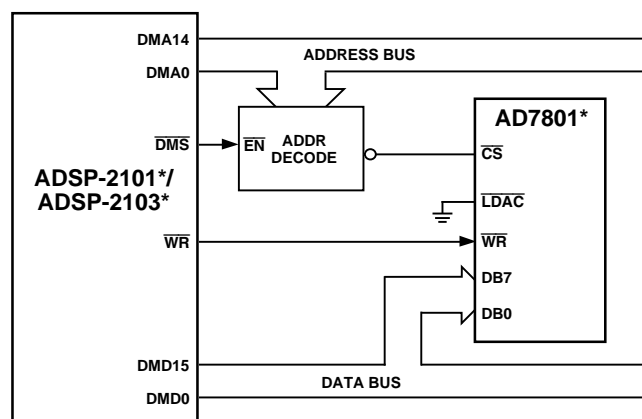
$\overline{LDAC}$  is permanently tied low in this circuit so the DAC output is updated on the rising edge of the  $\overline{WR}$  signal.

Data is loaded to the AD7801 input register using the following ADSP-21xx instruction.

$$DM(DAC) = MR0$$

MR0 = ADSP-21xx MR0 Register.

DAC = Decoded DAC Address.



\*ADDITIONAL CIRCUITRY OMITTED FOR CLARITY.

Figure 29. AD7801-ADSP-2101/ADSP-2103 Interface

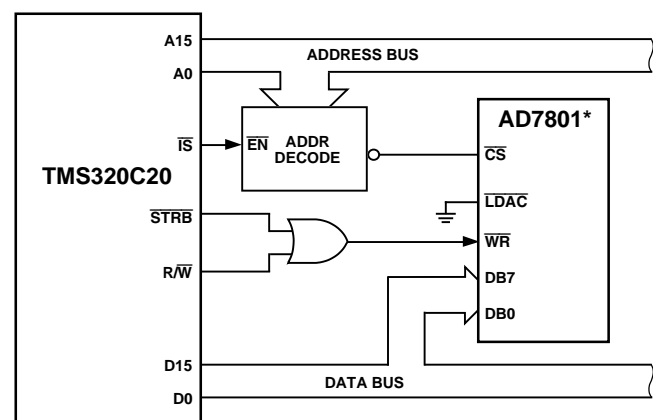
### AD7801-TMS320C20 Interface

Figure 30 shows an interface between the AD7801 and the TMS320C20. Data is loaded to the AD7801 using the following instruction:

$$OUT\ DAC, D$$

DAC = Decoded DAC Address.

D = Data Memory Address.



\*ADDITIONAL CIRCUITRY OMITTED FOR CLARITY.

Figure 30. AD7801-TMS320C20 Interface

## AD7801-8051/8088 Interface

**8051/8088\***

A15

A8

PSEN OR DEN

WR

ALE

A7

A0

ADDRESS BUS

EN

ADDR DECODE

OCTAL LATCH

CS

WR

LDAC

DB7

DB0

**AD7801\***

DATA BUS

\*ADDITIONAL CIRCUITRY OMITTED FOR CLARITY.

## APPLICATIONS

The AD7801 has been designed for unipolar operation but bipolar operation is possible using the circuit in Figure 32. The circuit shown is configured for an output voltage range of  $-5\text{ V}$  to  $+5\text{ V}$ . Rail-to-rail operation at the amplifier output is achievable by using an AD820 or OP295 as the output amplifier.

$$V_O = \left[ R_2 \left( 1 + \frac{R_4}{R_3} \right) / (R_1 + R_2) \times \left( \frac{2 V_{REF} D}{256} \right) - V_{REF} \left( \frac{R_4}{R_3} \right) \right]$$

With  $V_{REF} = 2.5$  V,  $R1 = R3 = 10$  k $\Omega$  and  $R2 = R4 = 20$  k $\Omega$  and  $V_{DD} = 5$  V.

[illegible]

## Decoding Multiple AD7801s in a System

The diagram illustrates a 4-bit DAC circuit. A 74HC139 4-to-16 decoder is powered by  $V_{DD}$  and  $V_{CC}$ , with its ground pin connected to DGND. The decoder's inputs are ENABLE, 1A, 1B, and CODED ADDRESS. Its outputs, 1Y0, 1Y1, 1Y2, and 1Y3, are connected to the CS (Chip Select) pins of four AD7801 DACs. The DATA BUS is connected to the D0-D7 inputs of all DACs. The WR (Write Enable) pin of the first DAC is connected to the DATA BUS, while the WR pins of the other three DACs are connected to ground. The LDAC (Load) pin of each DAC is connected to ground. The outputs of the DACs are labeled V<sub>OUT</sub>.

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# AD7801

## AD7801 as a Digitally Programmable Indicator

A digitally programmable upper limit detector using the DAC is shown in Figure 34. The upper limit for the test is loaded to the DAC, which in turn sets the limit for the CMP04. If a signal at the  $V_{IN}$  input is not below the programmed value, an LED will indicate the Fail condition.

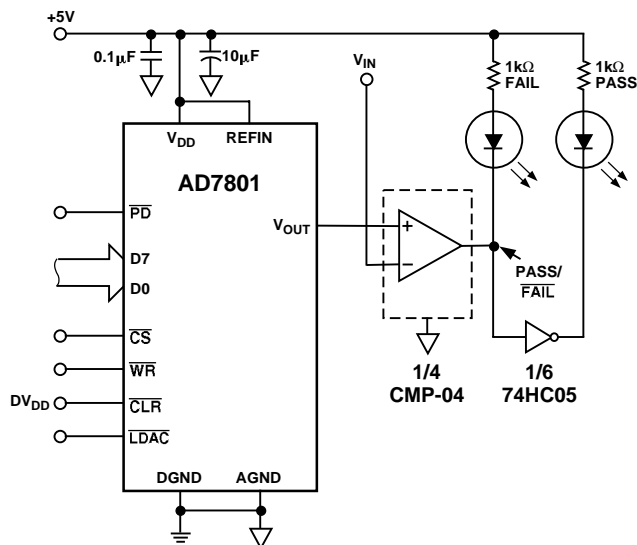


Figure 34. Digitally Programmable Indicator

## Programmable Current Source

Figure 35 shows the AD7801 used as the control element of a programmable current source. In this circuit the full-scale current is set to 1 mA. The output voltage from the DAC is applied across the current setting resistor of 4.7 kΩ in series with the full-scale setting resistor of 470 Ω. Suitable transistors to place in the feedback loop of the amplifier include the BC107 and the 2N3904, which enable the current source to operate from a minimum  $V_{SOURCE}$  of 6 V. The operating range is determined by the operating characteristics of the transistor. Suitable amplifiers include the AD820 and the OP295, both of which have rail-to-rail operation on their outputs. The current for any digital input code can be calculated as follows:

$$I = \frac{(2 V_{REF} D)}{(256 (5 k\Omega))}$$

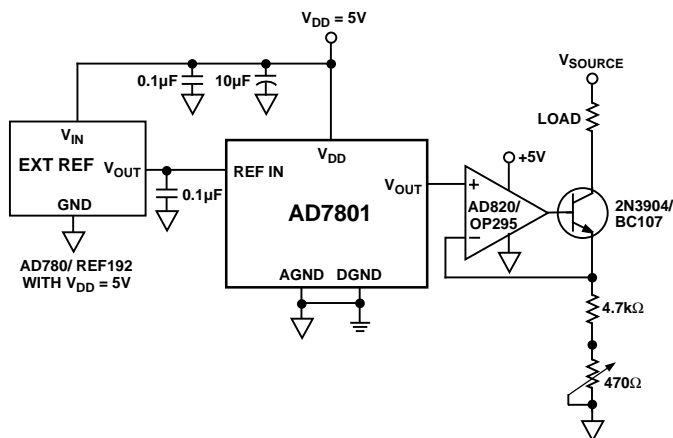


Figure 35. Programmable Current Source

## Coarse and Fine Adjustment using two AD7801s

The two DACs can be paired together to form a coarse and fine adjustment function for a setpoint as shown in Figure 36. In this circuit, the first DAC is used to provide the coarse adjustment and the second DAC is used to provide the fine adjustment. Varying the ratio of R1 and R2 will vary the relative effect of the coarse and fine tune elements in the circuit. For the resistor values shown, the second DAC has a resolution of 148 µV giving a fine tune range of 38 mV (approximately 2 LSB) for operation with a  $V_{DD}$  of 5 V and a reference of 2.5 V. The amplifier shown allows a rail-to-rail output voltage to be achieved on the output. A typical application for the circuit would be in a setpoint controller.

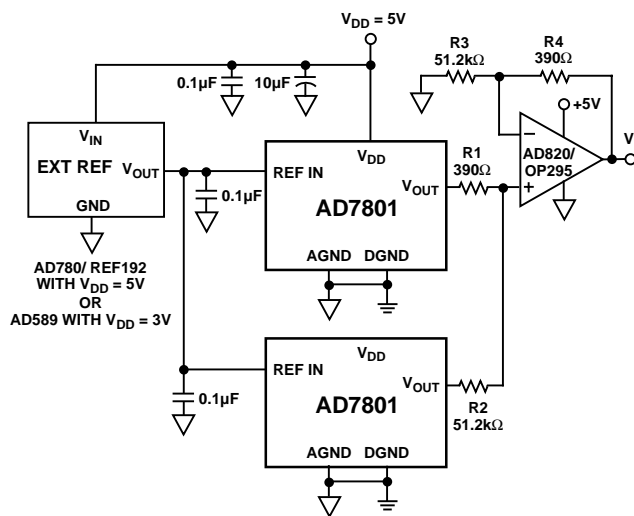


Figure 36. Coarse and Fine Adjustment

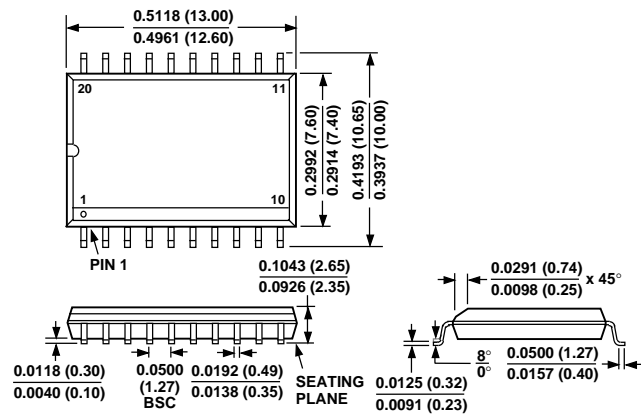
**Power Supply Bypassing and Grounding**

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD7801 is mounted should be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the AD7801 is in a system where multiple devices require an AGND to DGND connection, the connection should be made at one point only, a star ground point which should be established as closely as possible to the AD7801. The AD7801 should have ample supply bypassing of 10  $\mu\text{F}$  in parallel with 0.1  $\mu\text{F}$  located as close to the package as possible, ideally right up against the device. The 10  $\mu\text{F}$  capacitors are the tantalum bead type. The 0.1  $\mu\text{F}$  capacitors should have low Effective Series Resistance (ESR) and Effective Series Inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

The power supply lines of the AD7801 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the supply line. Fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other parts of the board and should never be run near reference inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effect of feedthrough through the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to the ground plane while signal traces are placed on the solder side.

OUTLINE DIMENSIONS  
Dimensions shown in inches and (mm).

20-Lead Wide Body SOIC  
(R-20)



20-Lead TSSOP  
(RU-20)

